CDx4AC245、CDx4ACT245 三态同相八路总线收发器

1 特性

- 缓冲输入
- 典型传播延迟
  - V_{CC} = 5V、T_A = 25°C 且 C_L = 50pF 时为 4ns
- 防 SCR 闩锁 CMOS 工艺和电路设计
- 双极 FAST™/AS/S 的速度，同时功耗显著降低
- 平衡传播延迟
- 交流类型的工作电压范围为 1.5V 至 5.5V，并在电源电压的 30% 时具有平衡的抗噪性能
- ±24mA 输出驱动电流
  - 扇出到 15 个 FAST™ IC
  - 驱动 50Ω 传输线路

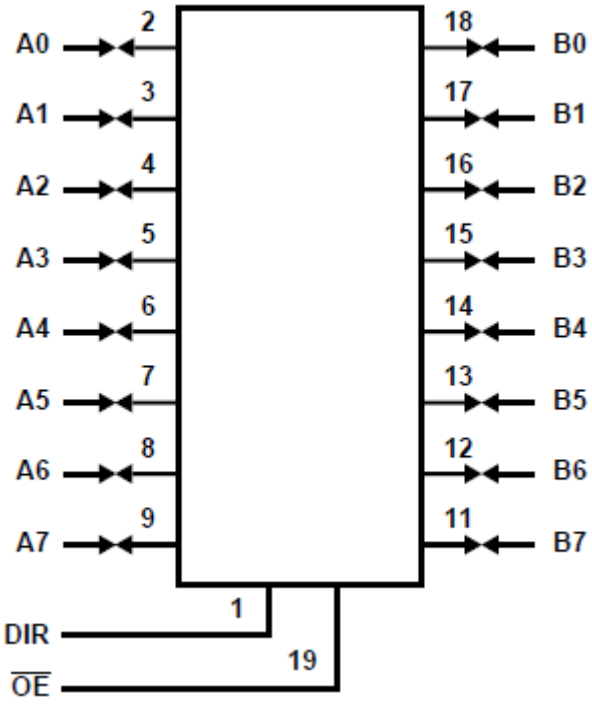
2 说明

'AC245 和 'ACT245 是采用高级 CMOS 逻辑技术的八路总线收发器。

器件信息

器件型号	封装(1)	封装尺寸(2)	本体尺寸(3)
CD74AC245/ CD74ACT245	N（PDIP，20）	24.33mm x 9.4mm	24.33mm x 6.35mm
	DW（SOIC，20）	12.80mm x 10.3mm	12.80mm x 7.50mm
CD54AC245/ CD54ACT245	J（CDIP，20）	24.2mm x 7.62mm	24.2mm x 6.92mm
CD74ACT245	DB（SSOP，20）	7.2mm x 7.8mm	7.2mm x 5.3mm

(1) 更多相关信息，请参阅第 10 节。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 本体尺寸（长 × 宽）为标称值，不包括引脚。



逻辑图（正逻辑）

Table of Contents

3 Pin Configuration and Functions

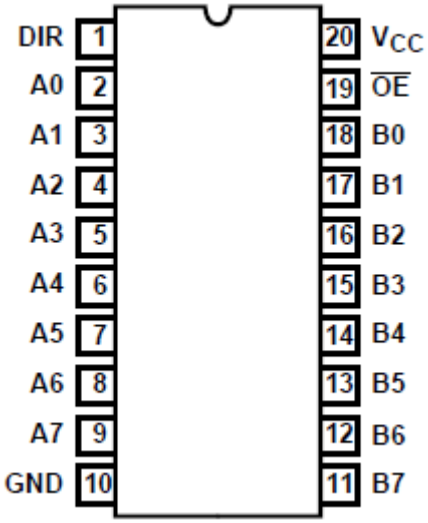


图 3-1. CD54AC245, CD54ACT245 (CERDIP), CD74AC245, CD74ACT245 (PDIP, SOIC, SSOP) Top View

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	DIR	I/O	Direction Pin
2	A0	I/O	A1 Input/Output
3	A1	I/O	A2 Input/Output
4	A2	I/O	A3 Input/Output
5	A3	I/O	A4 Input/Output
6	A4	I/O	A5 Input/Output
7	A5	I/O	A6 Input/Output
8	A6	I/O	A7 Input/Output
9	A7	I/O	A8 Input/Output
10	GND	—	Ground Pin
11	B7	I/O	B7 Input/Output
12	B6	I/O	B6 Input/Output
13	B5	I/O	B5 Input/Output
14	B4	I/O	B4 Input/Output
15	B3	I/O	B3 Input/Output
16	B2	I/O	B2 Input/Output
17	B1	I/O	B1 Input/Output
18	B0	I/O	B0 Input/Output
19	$\overline{OE}$	I/O	Output Enable
20	V_{CC}	—	Power Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		−0.5	6	V
I_{IK}	Input diode current	V_I < -0.5V or V_I > V_{CC} + 0.5V		± 20	mA
I_{OK}	Output diode current	V_O < -0.5V or V_O > V_{CC} + 0.5V		± 50	mA
I_O	Output source or sink current per output pin	V_O > -0.5V or V_O < V_{CC} + 0.5V		± 50	mA
I_{OK} (2)	V_{CC} or ground current	I_{CC} or I_{GND}		± 100	mA
T_{stg}	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For up to 4 outputs per device, add ±25mA for each additional output.

4.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			CDx4AC245		CDx4ACT245		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage(1)		1.5V	5.5V	4.5V	5.5V	V
V_I, V_O	Input or Output Voltage		0V	V_{CC}	0V	V_{CC}	V
dt/dv	Input Rise and Fall Slew Rate	1.5V to 3V		50			ns
		3.6V to 5.5V		20			
		4.5V to 5.5V				10	
T_A	Temperature range		−55	125	−55	125	°C

(1) Unless otherwise specified, all voltages are referenced to ground.

4.3 Thermal Information

THERMAL METRIC(1)		CDx4AC14/ CDx4ACT14			UNIT
		N (PDIP)	DW (SOIC)	DB (SSOP)	
		20 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	69	98.6	105.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C		-40°C TO 85°C		-55°C TO 125°C		UNIT
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
AC TYPES											
V_{IH}	High-level input voltage			1.5	1.2		1.2		1.2		V
				3	2.1		2.1		2.1		
				5.5	3.85		3.85		3.85		
V_{IL}	Low-level input voltage	V_{IL}		1.5		0.3		0.3		0.3	V
				3		0.9		0.9		0.9	
				5.5		1.65		1.65		1.65	
V_{OH}	High-level output voltage	V_{IH} or V_{IL}	-0.05	1.5	1.4		1.4		1.4		VV_{OH}
			-0.05	3	2.9		2.9		2.9		
			-0.05	4.5	4.4		4.4		4.4		
			-4	3	2.58		2.48		2.4		
			-24	4.5	3.94		3.8		3.7		
			-75	5.5			3.85				
			-50	5.5					3.85		
V_{OL}	Low-level output voltage	V_{IH} or V_{IL}	0.05	1.5 V		0.1		0.1		0.1	V
			0.05	3 V		0.1		0.1		0.1	
			0.05	4.5 V		0.1		0.1		0.1	
			12	3 V		0.36		0.44		0.5	
			24	4.5 V		0.36		0.44		0.5	
			75[1]	5.5 V				1.65			
			50[1]	5.5 V						1.65	
I_I	Input leakage current	V_{CC} or GND		5.5		± 0.1		± 1		± 1	μ A
I_{OZ}	Three-state leakage current	V_{IH} or V_{IL}, VO = V_{CC} or GND		5.5 V		± 0.5		± 5		± 10	μ A
I_{CC}	Quiescent supply current MSI	V_{CC} or GND	0	5.5 V		8		80		160	μ A
ACT TYPES											
V_{IH}	High-level input voltage			4.5 V to 5.5 V	2		2		2		V
V_{IL}	Low-level input voltage			4.5 V to 5.5 V		0.8		0.8		0.8	V
V_{OH}	High-level output voltage	V_{IH} or V_{IL}	-0.05	4.5 V	4.4		4.4		4.4	0.8	V
			-24	4.5 V	3.94		3.8		3.7		
			-75[1]	5.5 V			3.85				
			-50	5.5 V					3.85		

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C		-40°C TO 85°C		-55°C TO 125°C		UNIT
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
V_{OL}	Low-level output voltage	V_{IH} or V_{IL}	0.05	4.5		0.1		0.1		0.1	V
			24	4.5		0.36		0.44		0.5	
			75[1]	5.5				1.65			
			50[1]	5.5						1.65	
											V
I_I	Input leakage current	V_{CC} or GND		5.5 V		± 0.1		± 1		± 1	µA
I_{OZ}	Three-state or leakage current	V_{IH} or $V_{IL}V_O$ = V_{CC} or GND		5.5 V		± 0.5		± 5		± 10	µA
I_{CC}	Quiescent supply current MSI	V_{CC} or GND	0	5.5 V		8		80		160	µA
Δ I_{CC}	Additional supply current per input pin TTL inputs high 1 unit load	V_{CC} -2.1		4.5 to 5.5		2.4		2.8		3	mA

1. Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation. Test verifies a minimum 50Ω transmission-line-drive capability at 85°C, 75Ω at 125°C.

4.5 Switching Characteristics

Input t_r, t_f = 3ns, C_L = 50pF (Worst Case). Over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER		V_{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
AC TYPES									
t_{PLH}, t_{PHL}	Propagation delay, data to output	1.5			96			106	ns
		3.3		3.2	10.8	3		11.9	
		5		2.2	7.7	2.1		8.5	
t_{PLZ}, t_{PHZ}	Propagation delay, output disable to output	1.5			159			175	ns
		3.3		4.7	15.9	4.4		17.5	
		5		3.7	12.7	3.5		14	
t_{PZL}, t_{PZH}	Propagation delay, output enable to output	1.5			159			175	ns
		3.3		5.6	19	5.3		21	
		5		3.7	12.7	3.5			
V_{OHV}	Minimum (Valley) V_{OH} During switching of other outputs (output under test not switching)	5		4 at 25°C			4 at 25°C		V

Input t_r, t_f = 3ns, C_L = 50pF (Worst Case). Over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER		V_{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OLP}	Maximum (Peak) V_{OL} During switching of other outputs (output under test not switching)	5		1 at 25°C			1 at 25°C		V
C_O	Three-state output capacitance			15			15		pF
C_I	Input capacitance				10			10	pF
C_{PD}	Power dissipation capacitance			57			57		pF
ACT TYPES									
t_{PLH}, t_{PHL}	Propagation delay, data to output	5	2.7		9.1	2.5		10	ns
t_{PLZ}, t_{PHZ}	Propagation delay, output disable to output	5	3.7		12.7	3.5		14	ns
t_{PZL}, t_{PZH}	Propagation delay, output enable to output	5	3.8		13.1	3.6		14.4	ns
V_{OHV}	Minimum (Valley) V_{OH} During switching of other outputs (output under test not switching)	5		4 at 25°C			4 at 25°C		V
V_{OLP}	Maximum (Peak) V_{OL} During switching of other outputs (output under test not switching)	5		1 at 25°C			1 at 25°C		V
C_O	Three-state output capacitance			15			15		pF
C_I	Input capacitance				10			10	pF
C_{PD}	Power dissipation capacitance			57			57		pF

1. Limits tested 100%
2. 3.3V Min is at 3.6V, Max is at 3V
3. 5V Min is at 5.5V, Max is at 4.5V
4. CPD is used to determine the dynamic power consumption per channel
   - AC: PD = VCC2 fi (CPD + CL)
   - ACT: PD = VCC2 fi (CPD + CL) + VCC Δ ICC where fi = input frequency, CL = output load capacitance, VCC = supply voltage

4.6 Timing Diagrams

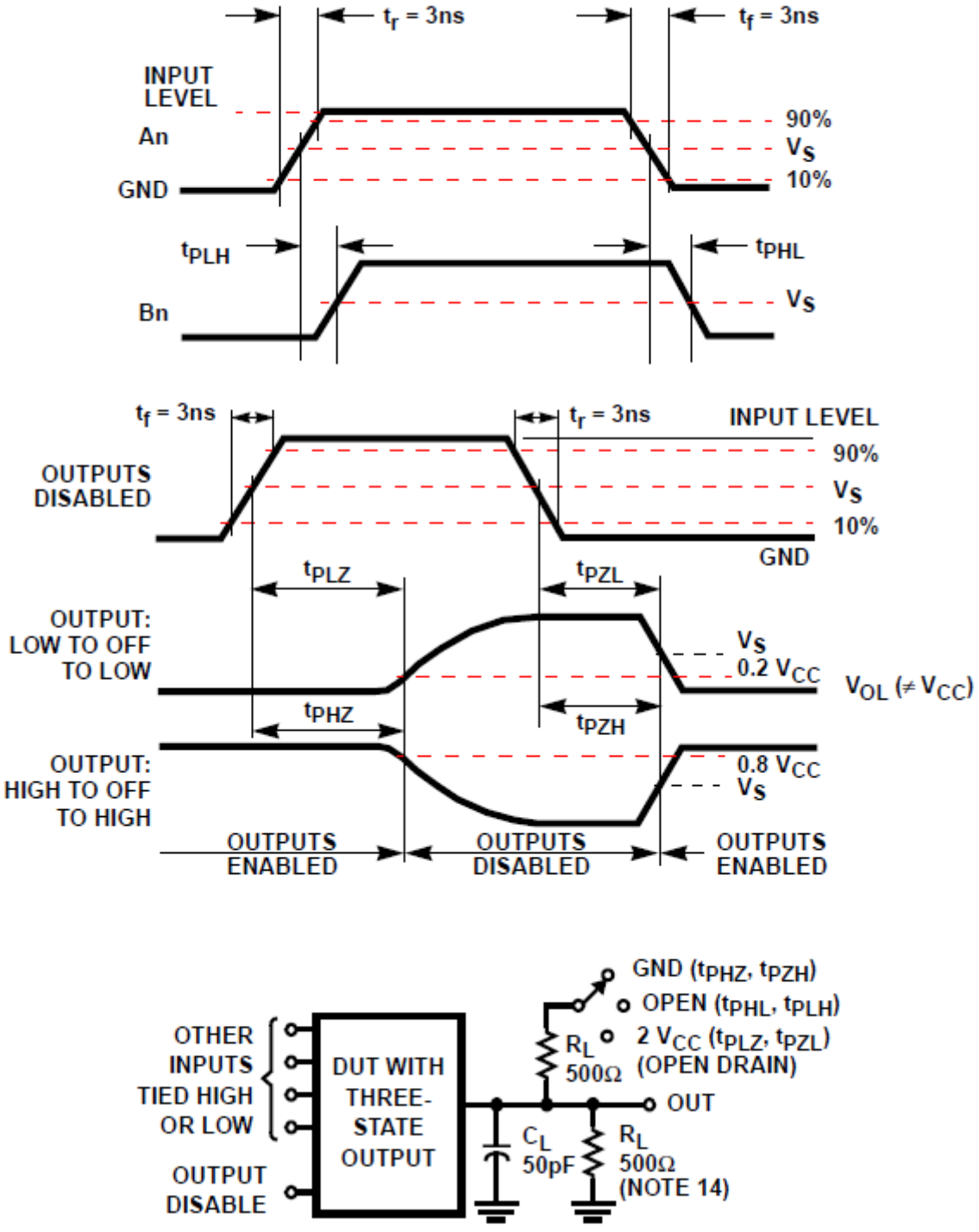


图 4-1. THREE-STATE PROPAGATION DELAY TIMES AND TEST CIRCUIT

图 4-1. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

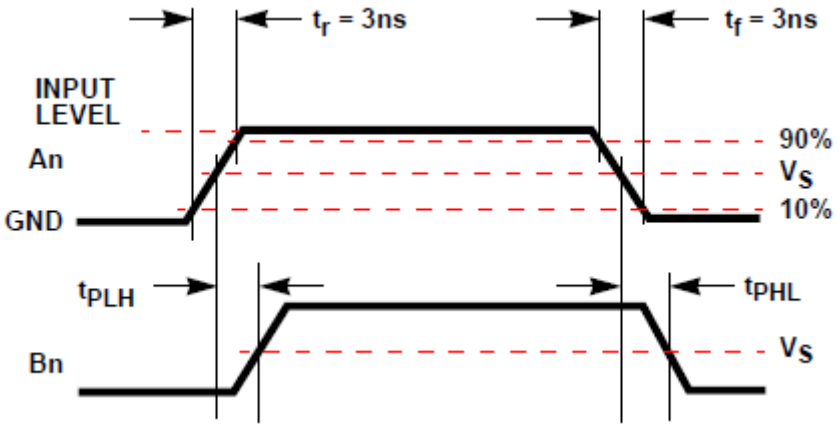
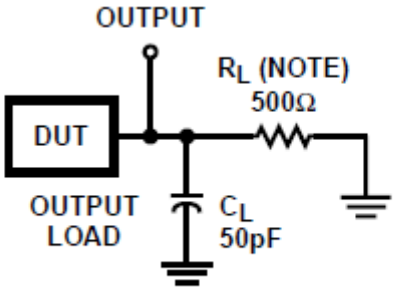


图 4-3. PROPAGATION DELAY TIMES



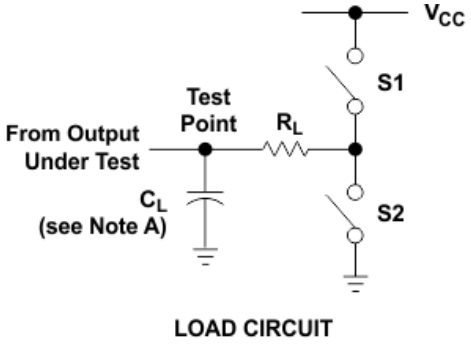
NOTE: For AC Series Only: When V_{CC} = 1.5V, R_L = 1kΩ.

表 4-1.

	AC	ACT
Input Level	V_{CC}	3V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

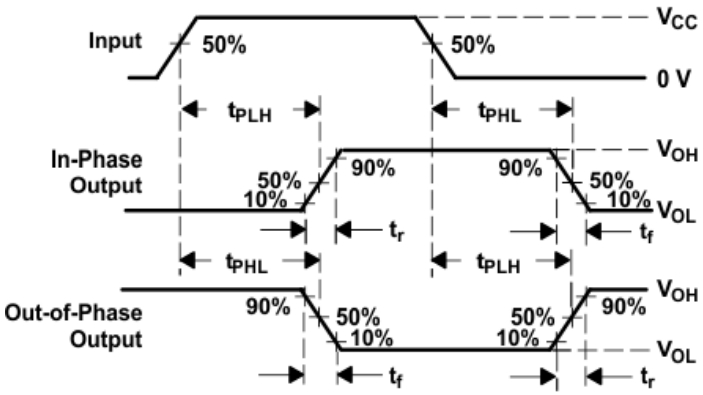
图 4-4. PROPAGATION DELAY TIMES

5 Parameter Measurement Information

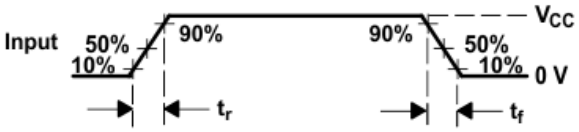


LOAD CIRCUIT

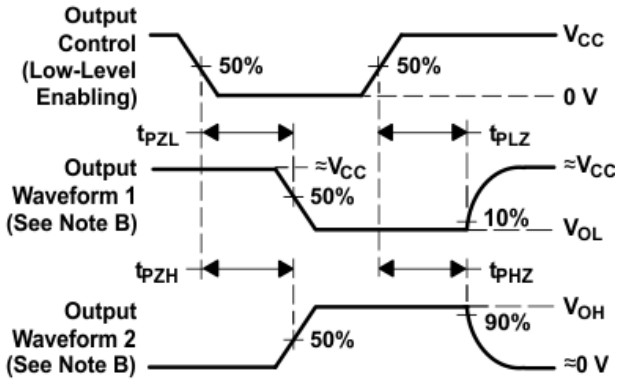
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		--	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



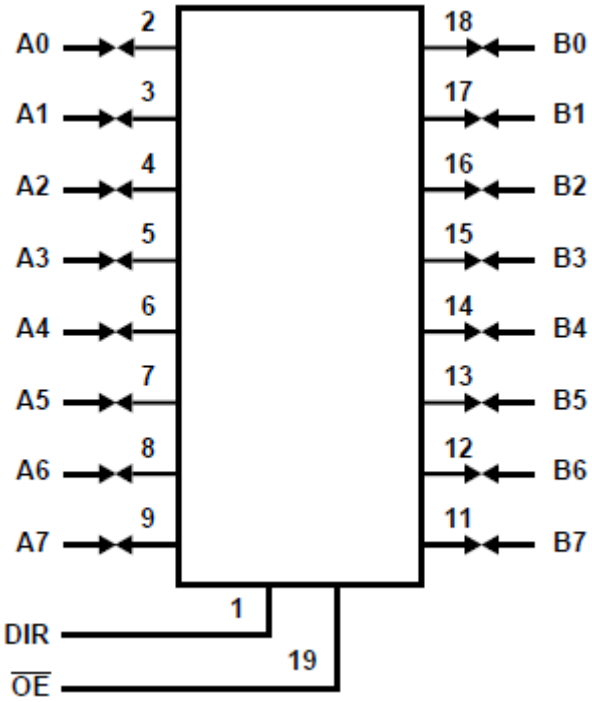
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

6 Detailed Description

6.1 Overview

The 'AC245 and 'ACT245 are non-inverting three-state bidirectional transceiver-buffers intended for two-way transmission from “A” bus to “B” bus or “B” bus to “A”. The logic level present on the direction input (DIR) determines the data direction. When the output enable input ($\overline{OE}$) is HIGH, the outputs are in the high-impedance state.

6.2 Functional Block Diagram



Logic Diagram (Positive Logic)

6.3 Device Functional Modes

Function Table lists the function modes of the CDx4AC245, CDx4ACT245.

表 6-1. Function Table

INPUTS(1)		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

(1) H = High Voltage Level, L = Low Voltage Level, X = Don’t Care

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *节 4.2*.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended; if there are multiple V_{CC} pins, then 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and a 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. 节 7.2.2 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the IOs, so they cannot float when disabled.

7.2.2 Layout Example

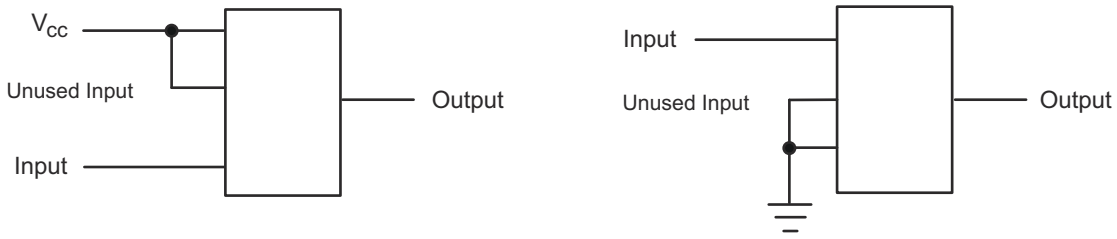


图 7-1. Layout Diagram

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD54AC245	Click here	Click here	Click here	Click here	Click here
CD74AC245	Click here	Click here	Click here	Click here	Click here
CD54ACT245	Click here	Click here	Click here	Click here	Click here
CD74ACT245	Click here	Click here	Click here	Click here	Click here

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (May 2023) to Revision D (April 2024)	Page
• 添加了*应用和实施* 部分、*器件和文档支持* 部分，并向*器件信息* 表添加了封装尺寸	1
• Updated R θ JA values: DW = 58 to 98.6, DB = 70 to 105.4, all values in °C/W	4

Changes from Revision B (April 2002) to Revision C (May 2023)	Page
• 添加了*封装信息* 表、*引脚功能* 表和*热性能信息* 表	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD54AC245F3A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54AC245F3A
CD54AC245F3A.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54AC245F3A
CD54ACT245F3A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54ACT245F3A
CD54ACT245F3A.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54ACT245F3A
CD74AC245E	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74AC245E
CD74AC245E.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74AC245E
CD74AC245EE4	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74AC245E
CD74AC245M	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	-55 to 125	AC245M
CD74AC245M96	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC245M
CD74AC245M96.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC245M
CD74ACT245E	NRND	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74ACT245E
CD74ACT245E.A	NRND	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74ACT245E
CD74ACT245EE4	NRND	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74ACT245E
CD74ACT245M	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	-55 to 125	ACT245M
CD74ACT245M96	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	(ACT245, ACT245M)
CD74ACT245M96.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	(ACT245, ACT245M)
CD74ACT245SM96	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	(ACT245, ACT245SM)
CD74ACT245SM96.A	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	(ACT245, ACT245SM)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54AC245, CD54ACT245, CD74AC245, CD74ACT245 :

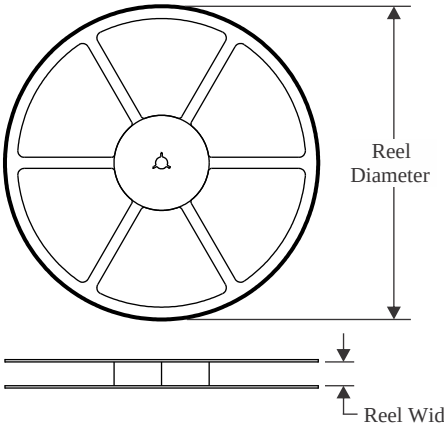
- Catalog : CD74AC245, CD74ACT245
- Military : CD54AC245, CD54ACT245

NOTE: Qualified Version Definitions:

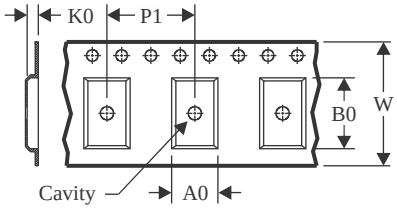
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

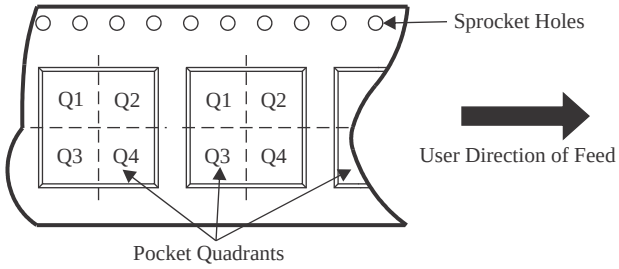


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

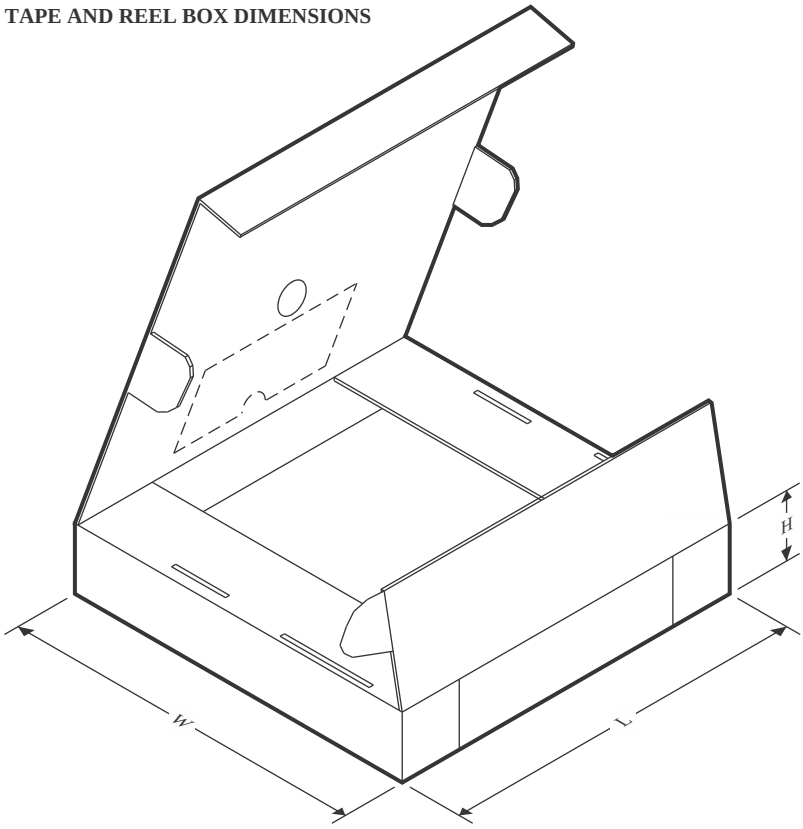
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC245M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74ACT245M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74ACT245M96	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
CD74ACT245SM96	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1

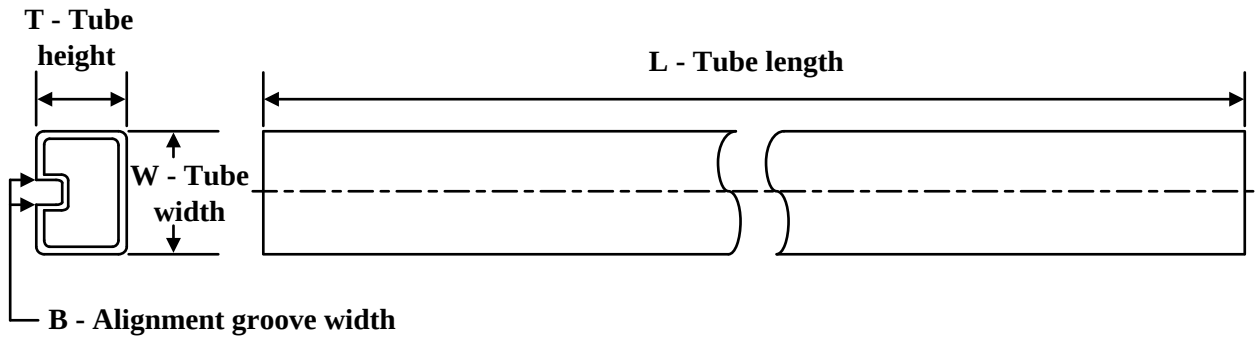
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC245M96	SOIC	DW	20	2000	356.0	356.0	45.0
CD74ACT245M96	SOIC	DW	20	2000	356.0	356.0	45.0
CD74ACT245M96	SOIC	DW	20	2000	356.0	356.0	45.0
CD74ACT245SM96	SSOP	DB	20	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

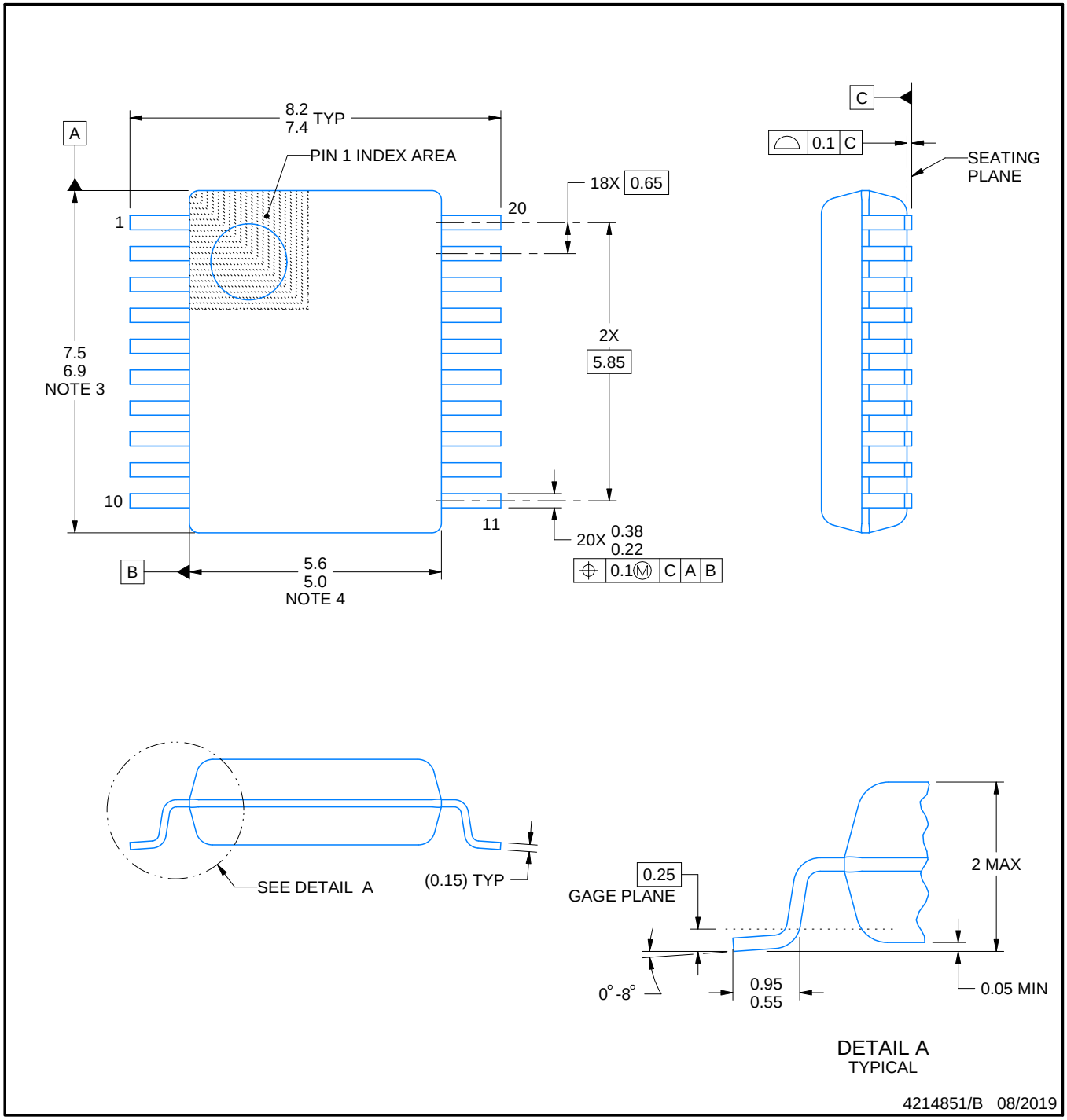
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74AC245E	N	PDIP	20	20	506	13.97	11230	4.32
CD74AC245E.A	N	PDIP	20	20	506	13.97	11230	4.32
CD74AC245EE4	N	PDIP	20	20	506	13.97	11230	4.32
CD74ACT245E	N	PDIP	20	20	506	13.97	11230	4.32
CD74ACT245E.A	N	PDIP	20	20	506	13.97	11230	4.32
CD74ACT245EE4	N	PDIP	20	20	506	13.97	11230	4.32

PACKAGE OUTLINE

DB0020A

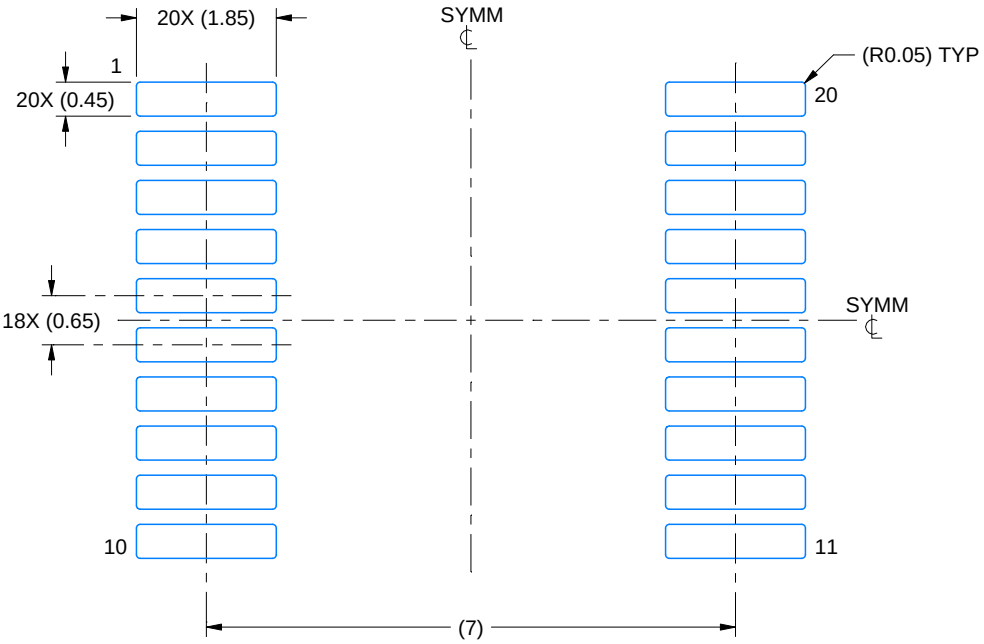
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

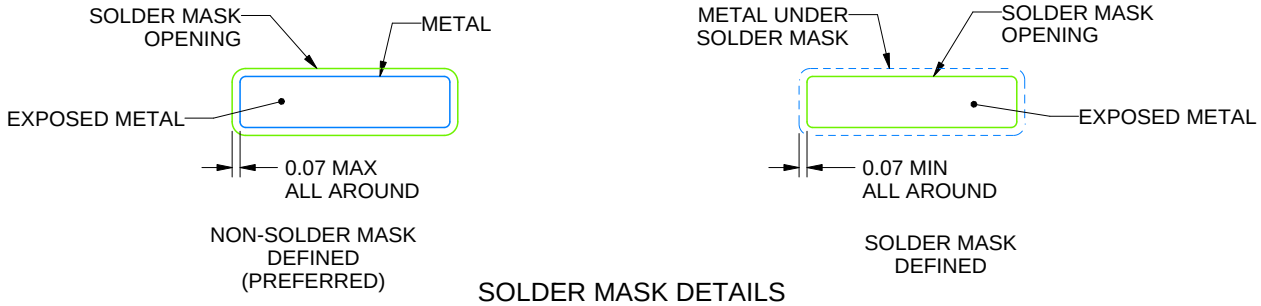


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

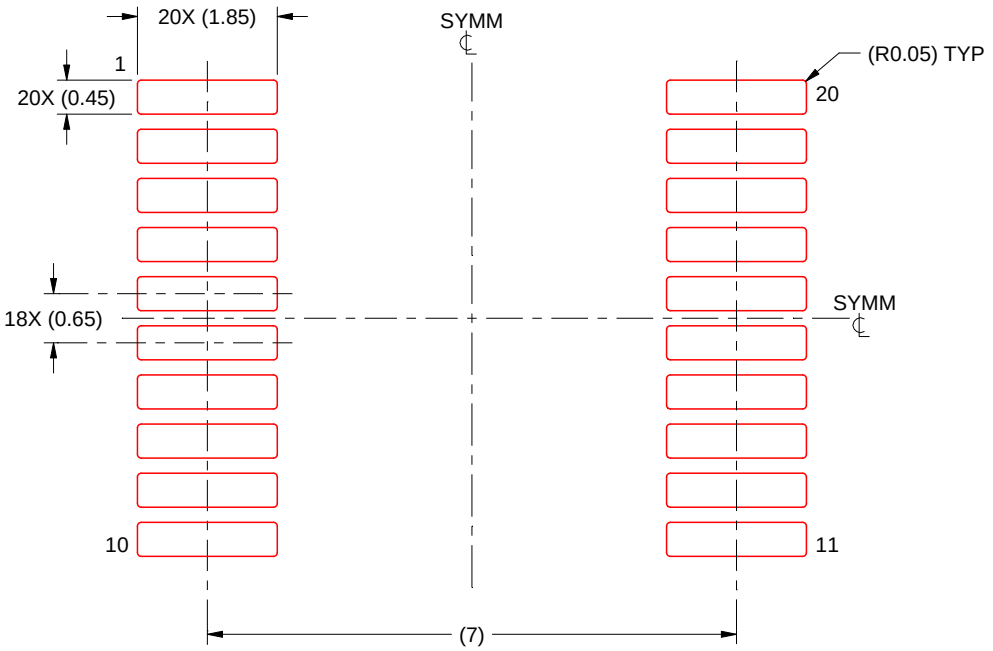
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

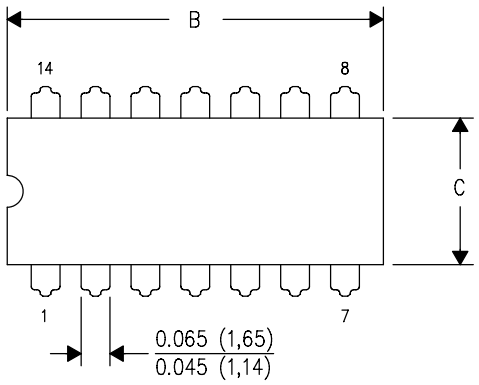
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

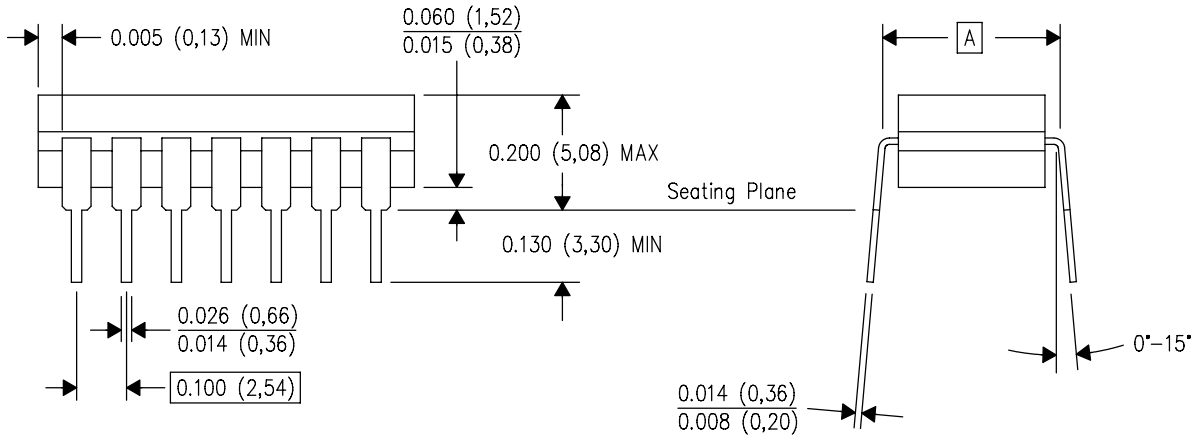
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



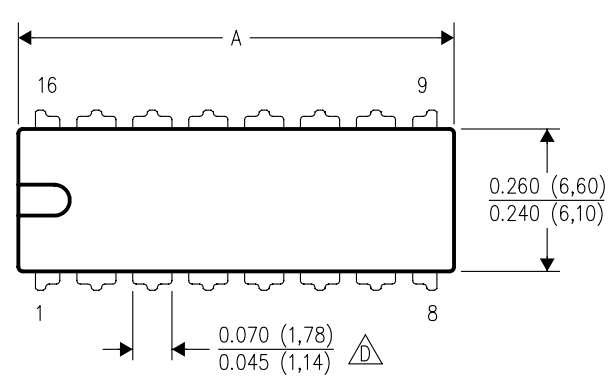
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

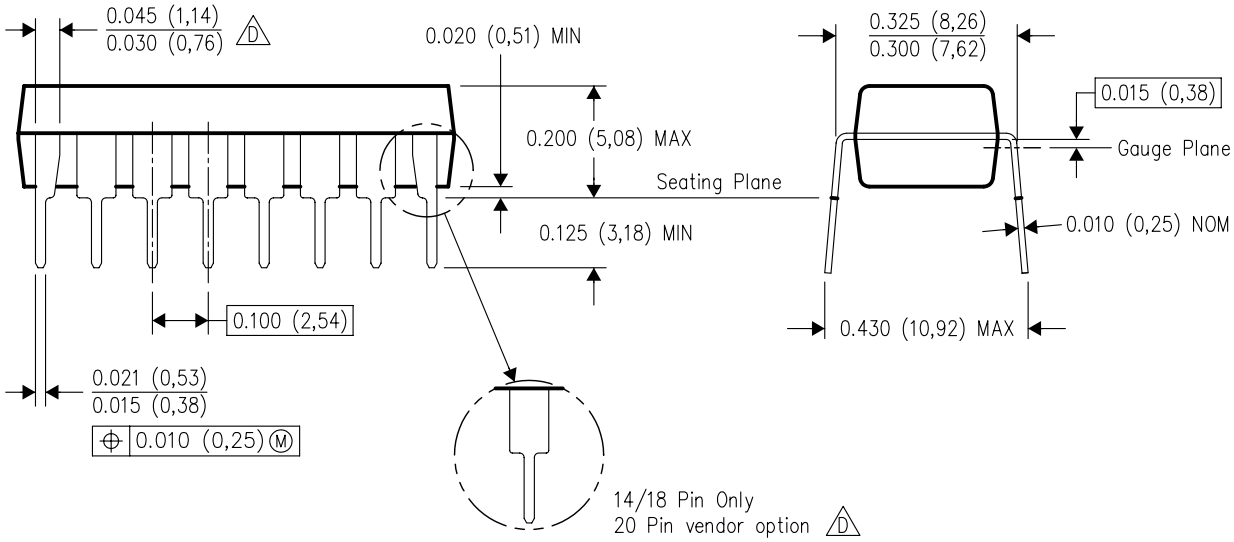
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

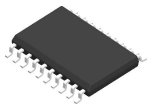


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

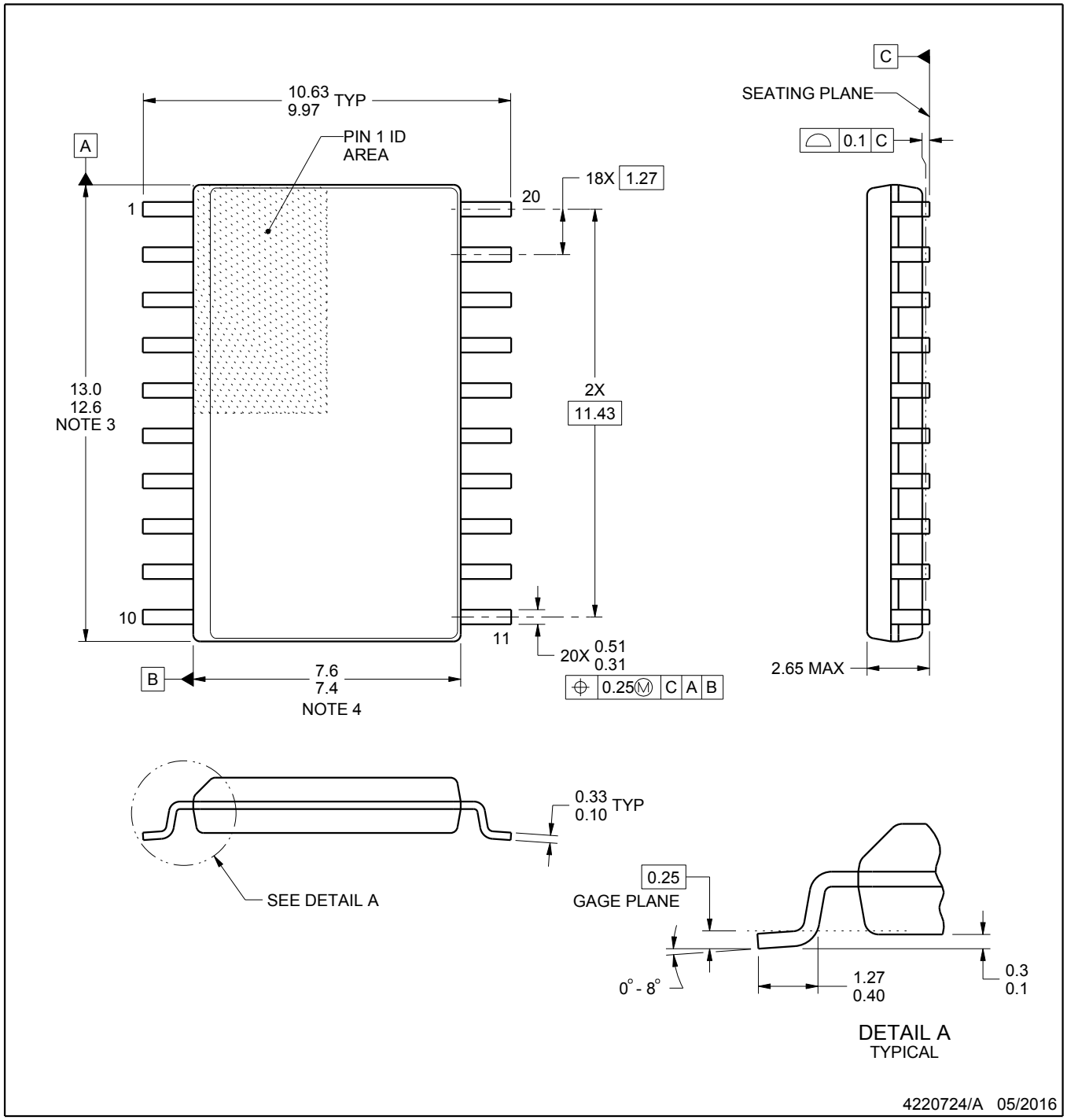


PACKAGE OUTLINE

DW0020A

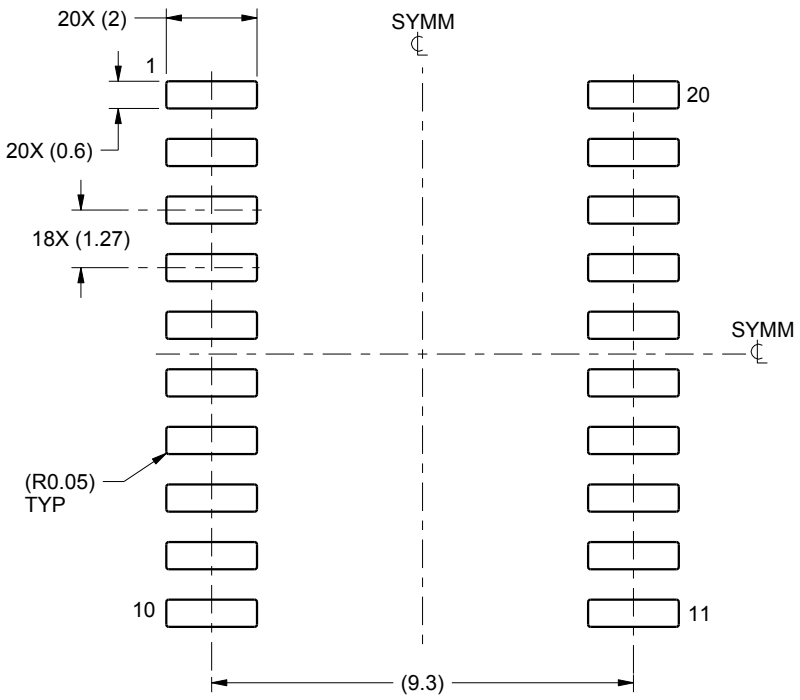
SOIC - 2.65 mm max height

SOIC

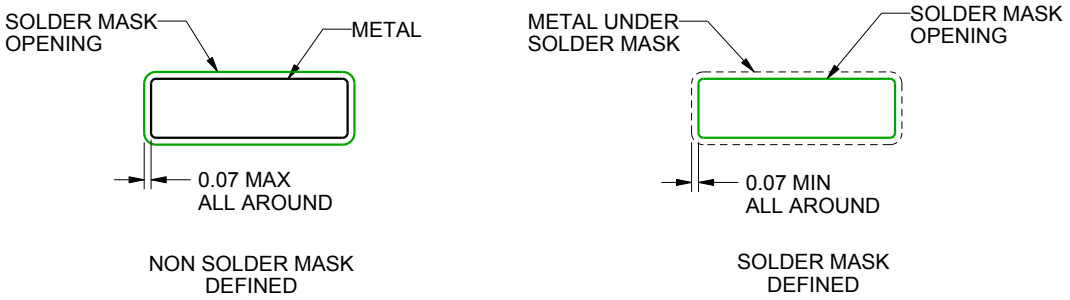


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

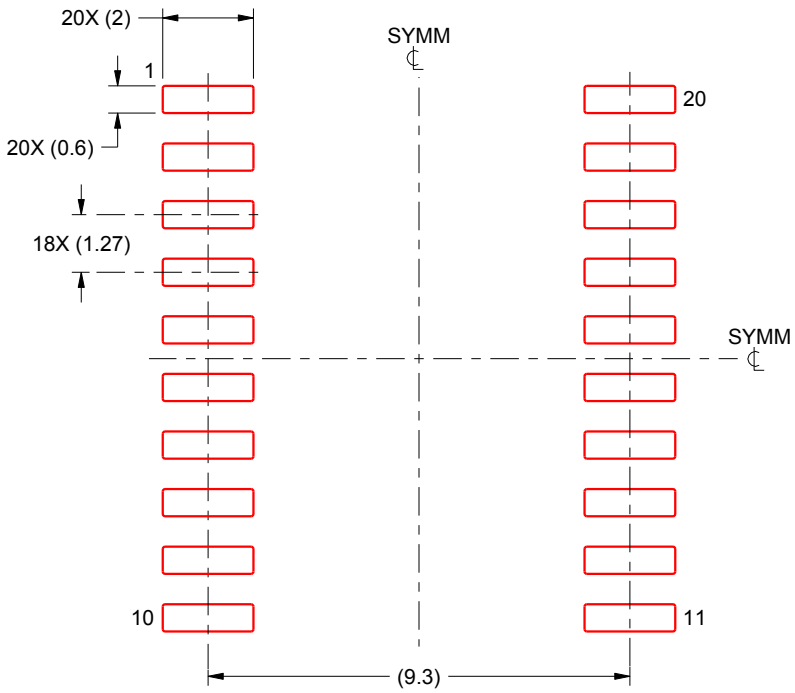


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月