CD74AC175 具有清零功能的四路 D 类触发器

1 特性

- 交流类型的工作电压范围为 1.5V 至 5.5V，并在电源电压的 30% 时具有平衡的抗噪性能
- 缓冲输入
- 包含四个具有双轨输出的触发器
- 双极 F、AS 和 S 的速度，同时功耗显著降低
- 平衡传播延迟
- ±24mA 输出驱动电流
  - 扇出至 15 个 F 器件
- 防 SCR 闩锁 CMOS 工艺和电路设计
- ESD 保护超过 2kV（根据 MIL-STD-883 方法 3015）

2 应用

- 缓冲器/存储寄存器
- 移位寄存器
- 图形发生器

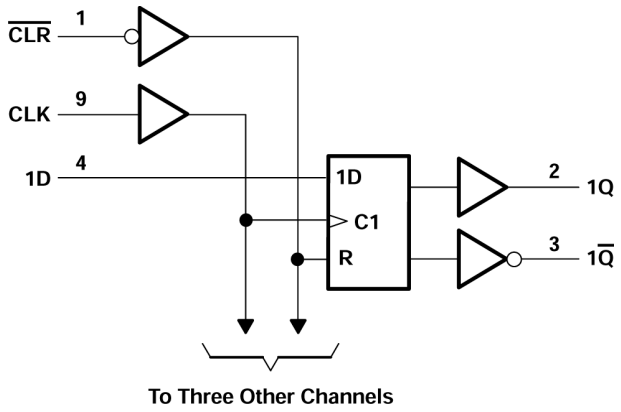
3 说明

这些正边沿触发式 D 类触发器具有直接清零 ($\overline{CLR}$) 输入。CD74AC175 器具有来自每个触发器的互补输出。

封装信息

器件型号	封装(1)	封装尺寸(2)	本体尺寸(3)
CD74AC175	D（SOIC，16）	9.9mm x 6mm	9.9mm x 3.9mm

(1) 如需了解更多信息，请参阅机械、封装和可订购信息。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 本体尺寸（长 × 宽）为标称值，不包括引脚。



逻辑图（正逻辑）

Table of Contents

4 Pin Configurations and Functions

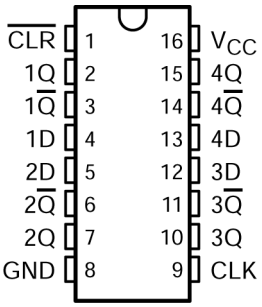


图 4-1. D Package, 16-PIN SCOIC (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	$\overline{CLR}$	I	Clear Pin
2	1Q	O	1Q Output
3	$1\overline{Q}$	O	$1\overline{Q}$ Output
4	1D	I	1D Input
5	2D	I	2D Input
6	$2\overline{Q}$	O	$2\overline{Q}$ Output
7	2Q	O	2Q Output
8	GND	—	Ground Pin
9	CLK	I	Clock Input
10	3Q	O	3Q Output
11	$3\overline{Q}$	O	$3\overline{Q}$Output
12	3D	I	3D Input
13	4D	I	4D Input
14	$4\overline{Q}$	O	$4\overline{Q}$Output
15	4Q	O	4Q Output
16	V_{CC}	—	Power Pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		– 0.5	6	V
I_{IK}	Input clamp current	(V_I < 0 V or V_I > V_{CC}) (2)		±20	mA
I_{OK}	Output clamp current	(V_O < 0 V or V_O > V_{CC})(2)		±50	mA
I_O	Continuous output current	(V_O> 0 V or V_O < V_{CC})		±50	mA
	Continuous current through V_{CC} or GND			±200	mA
T_{stg}	Storage temperature range		– 65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			T_A = 25°C		– 55°C to 125°C		– 40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		1.5	5.5	1.5	5.5	1.5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 1.5V	1.2		1.2		1.2		V
		V_{CC} = 3V	2.1		2.1		2.1		
		V_{CC} = 5.5V	3.85		3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 1.5V		0.3		0.3		0.3	V
		V_{CC} = 3V		0.9		0.9		0.9	
		V_{CC} = 5.5V		1.65		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 4.5V to 5.5V		– 24		- 24		- 24	mA
I_{OL}	Low-level output current	V_{CC} = 4.5V to 5.5V		24		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC}= 1.5V to 3V		50		50		50	ns/V
		V_{CC} = 3.6V to 5.5V		20		20		20	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.4 Thermal Information

THERMAL METRIC(1)		D (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953). The package thermal impedance is calculated in accordance with JESD 51-7.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25 °C		– 55°C to 125°C		– 40°C to 85°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = – 50 μA	1.5V	1.4		1.4		1.4		V
			3V	2.9		2.9		2.9		
			4.5V	4.4		4.4		4.4		
		I_{OH} = – 4mA	3V	2.58		2.4		2.48		
		I_{OH} = – 24mA	4.5V			3.85				
		I_{OH} = – 50mA(1)	5.5V					3.85		
		I_{OH} = – 75mA(1)	5.5V							
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 50 μA	1.5V		0.1		0.1		0.1	V
			3V		0.1		0.1		0.1	
			4.5V		0.1		0.1		0.1	
		I_{OL} = 12mA	3V		0.36		0.5		0.44	
		I_{OL} = 24mA	4.5V		0.36		0.5		0.44	
		I_{OL} = 50mA(1)	5.5V				1.65			
		I_{OL} = 75mA(1)	5.5 V						1.65	
I_I	V_I = V_{CC} or GND		5.5 V		±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V		8		160		80	μA
C_i					10		10		10	pF

(1) Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

表 5-1. Act Input Load Table

INPUT	UNIT LOAD
Data	0.58
$\overline{CLR}$	0.67
CLK	0.92

5.6 Timing Requirements, V_{CC} = 1.5V

over recommended operating free-air temperature range, V_{CC} = 1.5V (unless otherwise noted)

			-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			8		114	MHz
t_w	Pulse duration	$\overline{CLR}$ low	50		44		ns
		CLK high or low	63		55		
t_{su}	Setup time before CLK ↑	Data	2		2		ns
t_h	Hold time, data after CLK ↑		2		2		ns
t_{rec}	Recovery time, before CLK ↑	$\overline{CLR}$ ↑	1		1		ns

5.7 Timing Requirements, V_{CC} = 3.3V ± 0.3V

over recommended operating free-air temperature range, V_{CC} = 3.3V ± 0.3V (unless otherwise noted)

		-55°C to 125°C		-40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		71		81	MHz

over recommended operating free-air temperature range, V_{CC} = 3.3V ± 0.3V (unless otherwise noted)

			-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low	5.6		4.9		ns
		CLK high or low	7		6.1		
t_{su}	Setup time before CLK ↑	Data	2		2		ns
t_h	Hold time, data after CLK ↑		2		2		ns
t_{rec}	Recovery time, before CLK ↑	$\overline{CLR}$ ↑	1		1		ns

5.8 Timing Requirements, V_{CC} = 5V ± 0.5V

over recommended operating free-air temperature range, V_{CC} = 5V ± 0.5V (unless otherwise noted)

			-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			100		114	MHz
t_w	Pulse duration	$\overline{CLR}$ low	4		3.5		ns
		CLK high or low	5		4.4		
t_{su}	Setup time before CLK ↑	Data	2		2		ns
t_h	Hold time, data after CLK ↑		2		2		ns
t_{rec}	Recovery time, before CLK ↑	$\overline{CLR}$ ↑	1		1		ns

5.9 Switching Characteristics, V_{CC} = 1.5V

over recommended operating free-air temperature range, V_{CC} = 1.5V, C_L = 50pF (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			8		9		MHz
t_{PLH}	CLK	Any Q		153		139	ns
t_{PHL}				153		139	
t_{PLH}	$\overline{CLR}$	Any Q		153		139	ns
t_{PHL}				153		139	

5.10 Switching Characteristics, V_{CC} = 3.3V ± 0.3V

over recommended operating free-air temperature range, V_{CC} = 3.3V ± 0.3V, C_L = 50pF (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			71		81		MHz
t_{PLH}	CLK	Any Q	4.3	17.1	4.4	15.5	ns
t_{PHL}			4.3	17.1	4.4	15.5	
t_{PLH}	$\overline{CLR}$	Any Q	4.3	17.1	4.4	15.5	ns
t_{PHL}			4.3	17.1	4.4	15.5	

5.11 Switching Characteristics, V_{CC} = 5V ± 0.5V

over recommended operating free-air temperature range, V_{CC} = 5V ± 0.5V, C_L = 50pF (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

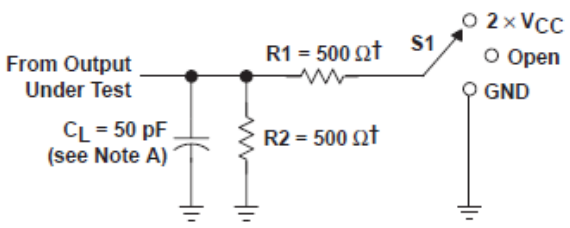
PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			100		114		MHz
t_{PLH}	CLK	Any Q	3.1	12.2	3.2	11.1	ns
t_{PHL}			3.1	12.2	3.2	11.1	
t_{PLH}	$\overline{CLR}$	Any Q	3.1	12.2	3.2	11.1	ns
t_{PHL}			3.1	12.2	3.2	11.1	

5.12 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

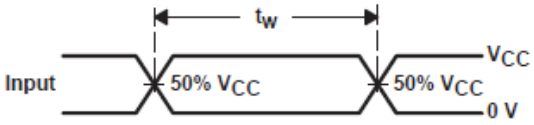
PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance	55	pF

6 Parameter Measurement Information

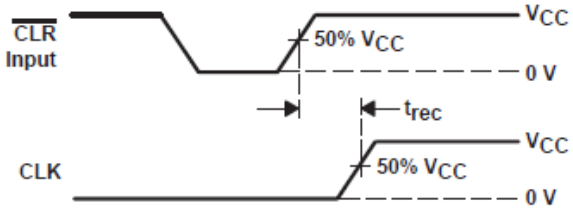


LOAD CIRCUIT

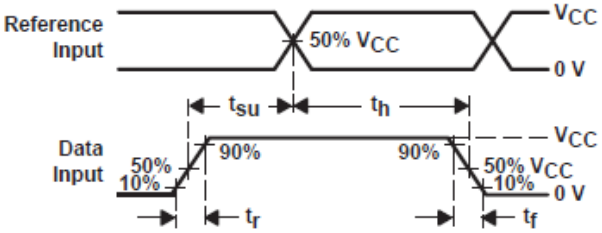
TEST	S1
t_{PLH}/t_{PHL} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 × VCC GND



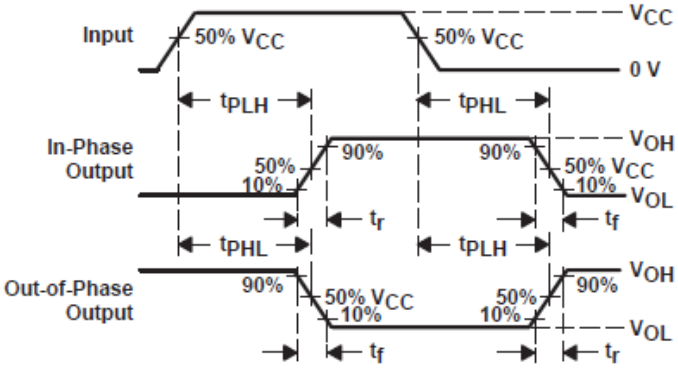
VOLTAGE WAVEFORMS
PULSE DURATION



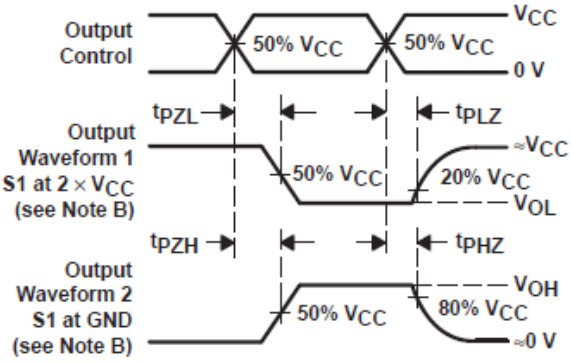
VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. Phase relationships between waveforms are arbitrary.
D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time, with one input transition per measurement.
F. t_{PLH} and t_{PHL} are the same as t_{pd}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

图 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

7.2 Functional Block Diagram

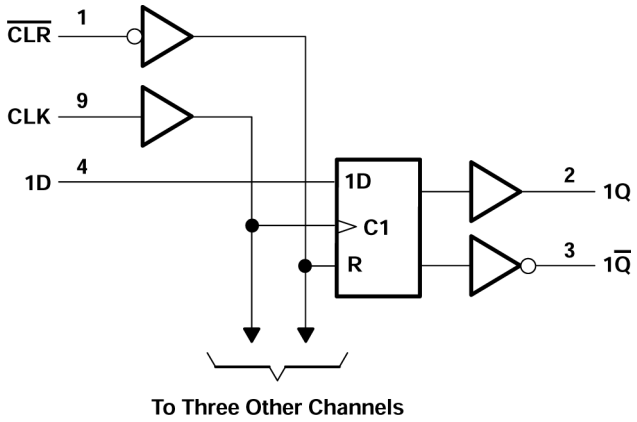


图 7-1. Logic Diagram (Positive Logic)

7.3 Device Functional Modes

表 7-1. Function Table (Each Flip-flop)

INPUTS			OUTPUTS	
$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in 节 5.3.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1 μF and if there are multiple V_{CC} terminals, then TI recommends .01 μF or .022 μF for each power terminal. It is okay to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.2 Layout

8.2.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. It is generally okay to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This does not disable the input section of the IOs so they cannot float when disabled.

9 Device and Documentation Support

9.1 Documentation Support (Analog)

9.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD74AC175	Click here	Click here	Click here	Click here	Click here

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 Trademarks

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9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (April 2003) to Revision A (April 2024)	Page
• 添加了*应用* 部分、*封装信息* 表、*引脚功能* 表、*ESD 等级* 表、*热性能信息* 表、*器件功能模式*、*应用和实施* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分	1
• Updated thermal values for R θ JA: D = 73 to 106.6, all values in °C/W	4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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