

## High-Speed CMOS Logic Dual Monostable Multivibrator with Reset

### Features

- Overriding RESET Terminates Output Pulse
- Triggering from the Leading or Trailing Edge
- Q and  $\bar{Q}$  Buffered Outputs
- Separate Resets
- Wide Range of Output-Pulse Widths
- Schmitt Trigger on B Inputs
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The 'HC221 and CD74HCT221 are dual monostable multivibrators with reset. An external resistor ( $R_X$ ) and an external capacitor ( $C_X$ ) control the timing and the accuracy for the circuit. Adjustment of  $R_X$  and  $C_X$  provides a wide range of output pulse widths from the Q and  $\bar{Q}$  terminals. Pulse triggering on the B input occurs at a particular voltage level and is not related to the rise and fall time of the trigger pulse.

Once triggered, the outputs are independent of further trigger inputs on A and B. The output pulse can be terminated by a LOW level on the Reset ( $\bar{R}$ ) pin. Trailing Edge triggering ( $\bar{A}$ ) and leading-edge-triggering (B) inputs are provided for triggering from either edge of the input pulse. On power up, the IC is reset. If either Mono is not used each input (on the unused device) must be terminated either high or low.

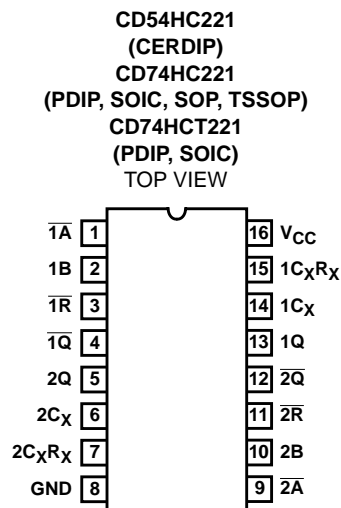
The minimum value of external resistance,  $R_X$ , is typically 500Ω. The minimum value of external capacitance,  $C_X$ , is 0pF. The calculation for the pulse width is  $t_W = 0.7 R_X C_X$  at  $V_{CC} = 4.5V$ .

### Ordering Information

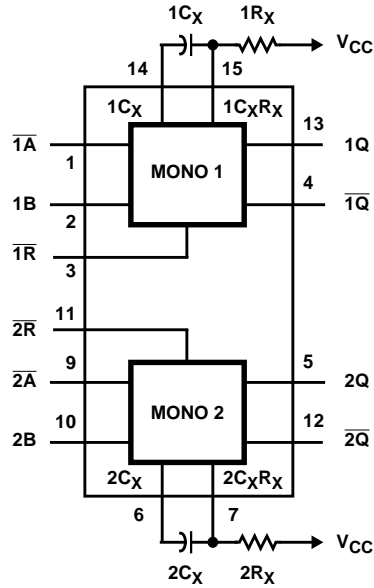
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC221F3A	-55 to 125	16 Ld CERDIP
CD74HC221E	-55 to 125	16 Ld PDIP
CD74HC221M	-55 to 125	16 Ld SOIC
CD74HC221MT	-55 to 125	16 Ld SOIC
CD74HC221M96	-55 to 125	16 Ld SOIC
CD74HC221NSR	-55 to 125	16 Ld SOP
CD74HC221PW	-55 to 125	16 Ld TSSOP
CD74HC221PWR	-55 to 125	16 Ld TSSOP
CD74HC221PWT	-55 to 125	16 Ld TSSOP
CD74HCT221E	-55 to 125	16 Ld PDIP
CD74HCT221M	-55 to 125	16 Ld SOIC
CD74HCT221MT	-55 to 125	16 Ld SOIC
CD74HCT221M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

### Pinout



Functional Diagram



TRUTH TABLE

INPUTS			OUTPUTS	
$\bar{A}$	B	$\bar{R}$	Q	$\bar{Q}$
H	X	H	L	H
X	L	H	L	H
L	↑	H		
↓	H	H		
X	X	L	L	H
L	H	↑		

H = High Voltage Level, L = Low Voltage Level, X = Irrelevant, ↑ = Transition from Low to High Level, ↓ = Transition from High to Low Level, = One High Level Pulse, = One Low Level Pulse

NOTE:

- For this combination the reset input must be low and the following sequence must be used: pin 1 (or 9) must be set high or pin 2 (or 10) set low; then pin 1 (or 9) must be low and pin 2 (or 10) set high. Now the reset input goes from low-to-high and the device will be triggered.

Logic Diagram



# CD54HC221, CD74HC221, CD74HCT221

## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Drain Current, per Output, $I_O$	
For $-0.5V < V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ .....	$\pm 50mA$

## Thermal Information

Package Thermal Impedance, $\theta_{JA}$ (see Note 2):	
E (PDIP) Package .....	67°C/W
M (SOIC) Package .....	73°C/W
NS (SOP) Package .....	64°C/W
PW (TSSOP) Package .....	108°C/W
Maximum Junction Temperature (Plastic Package) .....	150°C
Maximum Storage Temperature Range .....	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) .....	300°C
(SOIC - Lead Tips Only)	

## Operating Conditions

Temperature Range, $T_A$ .....	-55°C to 125°C
Supply Voltage Range, $V_{CC}$	
HC Types .....	.2V to 6V
HCT Types .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I, V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Time, $t_r, t_f$ on Inputs $\bar{A}$ and $\bar{R}$	
2V .....	1000ns (Max)
4.5V .....	500ns (Max)
6V .....	400ns (Max)
Input Rise and Fall Time, $t_r, t_f$ on Input B	
2V .....	Unlimited ns (Max)
4.5V .....	Unlimited ns (Max)
6V .....	Unlimited ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V

**CD54HC221, CD74HC221, CD74HCT221**

**DC Electrical Specifications (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	-	6	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	6	-	-	8	-	80	-	160	μA
<b>HCT TYPES</b>												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> and GND	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub> (Note 3)	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

3. For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

**HCT Input Loading Table**

INPUT	UNIT LOADS
All Inputs	0.3

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

**Prerequisite For Switching Function**

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>										
Input Pulse Width A	t <sub>WL</sub>	2	70	-	-	90	-	105	-	ns
		4.5	14	-	-	18	-	21	-	ns
		6	12	-	-	15	-	18	-	ns
Input Pulse Width B	t <sub>WH</sub>	2	70	-	-	90	-	105	-	ns
		4.5	14	-	-	18	-	21	-	ns
		6	12	-	-	15	-	18	-	ns

**CD54HC221, CD74HC221, CD74HCT221**

**Prerequisite For Switching Function (Continued)**

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Input Pulse Width Reset	t <sub>WL</sub>	2	70	-	-	90	-	105	-	ns
		4.5	14	-	-	18	-	21	-	ns
		6	12	-	-	15	-	18	-	ns
Recovery Time R̄ to Ā or B	t <sub>SU</sub>	2	0	-	-	0	-	0	-	ns
		4.5	0	-	-	0	-	0	-	ns
		6	0	-	-	0	-	0	-	ns
Output Pulse Width Q or Q̄ C <sub>X</sub> = 0.1μF R <sub>X</sub> = 10kΩ	t <sub>W</sub>	5	630	-	770	602	798	595	805	μs
Output Pulse Width Q or Q̄ C <sub>X</sub> = 28pF, R <sub>X</sub> = 2kΩ	t <sub>W</sub>	4.5	-	140	-	-	-	-	-	ns
C <sub>X</sub> = 1000pF, R <sub>X</sub> = 2kΩ	t <sub>W</sub>	4.5	-	1.5	-	-	-	-	-	μs
C <sub>X</sub> = 1000pF, R <sub>X</sub> = 10kΩ	t <sub>W</sub>	4.5	-	7	-	-	-	-	-	μs

**HCT TYPES**

Input Pulse Width A	t <sub>WL</sub>	4.5	14	-	-	18	-	21	-	ns
Input Pulse Width B	t <sub>WH</sub>	4.5	14	-	-	18	-	21	-	ns
Input Pulse Width Reset	t <sub>WL</sub>	4.5	18	-	-	23	-	27	-	ns
Recovery Time R̄ to Ā or B	t <sub>SU</sub>	4.5	0	-	-	0	-	0	-	ns
Output Pulse Width Q or Q̄ C <sub>X</sub> = 0.1μF R <sub>X</sub> = 10kΩ	t <sub>W</sub>	5	630	-	770	602	798	595	805	μs
Output Pulse Width Q or Q̄ C <sub>X</sub> = 28pF, R <sub>X</sub> = 2kΩ	t <sub>W</sub>	4.5	-	140	-	-	-	-	-	ns
C <sub>X</sub> = 1000pF, R <sub>X</sub> = 2kΩ	t <sub>W</sub>	4.5	-	1.5	-	-	-	-	-	μs
C <sub>X</sub> = 1000pF, R <sub>X</sub> = 10kΩ	t <sub>W</sub>	4.5	-	7	-	-	-	-	-	μs

**Switching Specifications** Input t<sub>r</sub>, t<sub>f</sub> = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
Propagation Delay, Trigger Ā, B, R̄ to Q	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	2	-	-	210	-	265	-	315	ns
		C <sub>L</sub> = 50pF	4.5	-	-	42	-	53	-	63	ns
		C <sub>L</sub> = 50pF	6	-	-	36	-	45	-	54	ns
		C <sub>L</sub> = 15pF	5	-	18	-	-	-	-	-	ns
Propagation Delay, Trigger Ā, B, R̄ to Q̄	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	170	-	215	-	255	ns
		C <sub>L</sub> = 50pF	4.5	-	-	34	-	43	-	51	ns
		C <sub>L</sub> = 50pF	6	-	-	29	-	37	-	43	ns
		C <sub>L</sub> = 15pF	5	-	14	-	-	-	-	-	ns

**CD54HC221, CD74HC221, CD74HCT221**

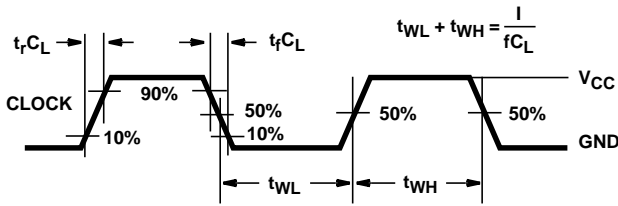
**Switching Specifications** Input  $t_r$ ,  $t_f = 6\text{ns}$  (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Propagation Delay, $\bar{R}$ to Q	$t_{PLH}$	$C_L = 50\text{pF}$	2	-	-	160	-	200	-	240	ns
			4.5	-	-	32	-	40	-	48	ns
			6	-	-	27	-	34	-	41	ns
Propagation Delay, $\bar{R}$ to $\bar{Q}$	$t_{PHL}$	$C_L = 50\text{pF}$	2	-	-	180	-	225	-	270	ns
			4.5	-	-	36	-	45	-	54	ns
			6	-	-	31	-	38	-	46	ns
Output Transition Time	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	$C_{IN}$	-	-	-	10	-	10	-	10	pF	
Pulse Width Match Between Circuits in the Same Package $C_X = 1000\text{pF}$ , $R_X = 10\text{k}\Omega$		-	4.5 to 5.5	-	$\pm 2$	-	-	-	-	-	%
Power Dissipation Capacitance (Notes 4, 5)	CPD	-	5	-	166	-	-	-	-	-	pF
<b>HCT TYPES</b>											
Propagation Delay, Trigger A, B, $\bar{R}$ to Q	$t_{PLH}$	$C_L = 50\text{pF}$	4.5	-	-	42	-	-	-	63	ns
		$C_L = 15\text{pF}$	5	-	18	-	-	-	-	-	ns
Propagation Delay, Trigger $\bar{A}$ , B, $\bar{R}$ to $\bar{Q}$	$t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	34	-	43	-	51	ns
		$C_L = 15\text{pF}$	5	-	14	-	-	-	-	-	ns
Propagation Delay, $\bar{R}$ to Q	$t_{PLH}$	$C_L = 50\text{pF}$	4.5	-	-	38	-	-	-	57	ns
Propagation Delay, $\bar{R}$ to $\bar{Q}$	$t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	37	-	-	-	56	ns
Output Transition Time	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	$C_{IN}$	-	-	-	10	-	10	-	10	pF	
Pulse Width Match Between Circuits in the Same Package $C_X = 1000\text{pF}$ , $R_X = 10\text{k}\Omega$		-	4.5 to 5.5	-	$\pm 2$	-	-	-	-	-	%
Power Dissipation Capacitance (Notes 4, 5)	CPD	-	5	-	166	-	-	-	-	-	pF

**NOTES:**

4.  $C_{PD}$  is used to determine the dynamic power consumption, per multivibrator.
5.  $P_D = (C_{PD} + C_L) V_{CC}^2 f_i + \Sigma$  where  $f_i$  = input frequency,  $f_o$  = output frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

**Test Circuits and Waveforms**



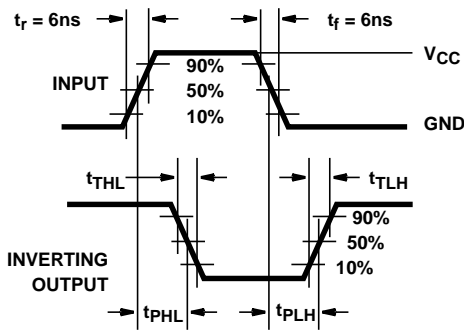
NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

**FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**

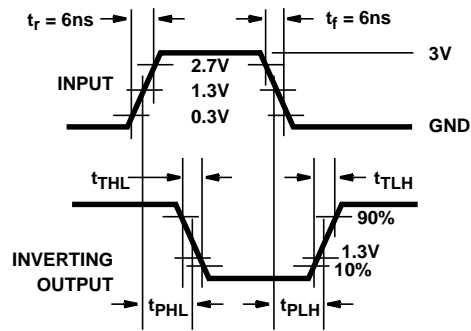


NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

**FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**



**FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**



**FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**

Typical Performance Curves



FIGURE 5. HC/HCT221 OUTPUT PULSE WIDTH vs TEMPERATURE



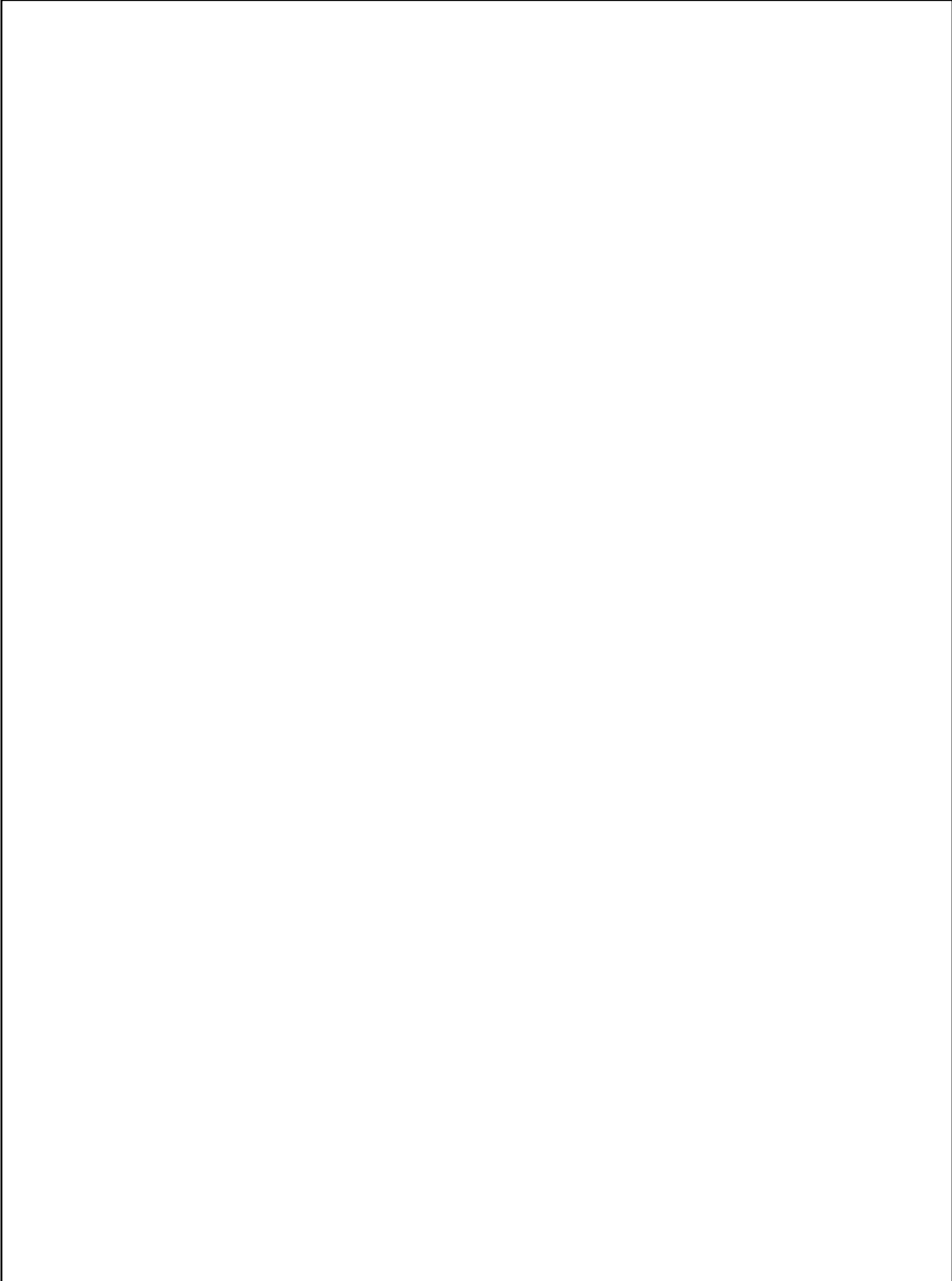
FIGURE 6. HC/HCT221 K FACTOR vs SUPPLY VOLTAGE



FIGURE 7. HC221 OUTPUT PULSE WIDTH vs  $C_X$



FIGURE 8. HC/HCT221 OUTPUT PULSE WIDTH vs  $C_X$



**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">5962-8780501EA</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8780501EA CD54HC221F3A
<a href="#">CD54HC221F</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC221F
CD54HC221F.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC221F
<a href="#">CD54HC221F3A</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8780501EA CD54HC221F3A
CD54HC221F3A.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8780501EA CD54HC221F3A
<a href="#">CD74HC221E</a>	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC221E
CD74HC221E.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC221E
<a href="#">CD74HC221M</a>	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	-55 to 125	HC221M
<a href="#">CD74HC221M96</a>	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC221M
CD74HC221M96.A	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC221M
<a href="#">CD74HC221MT</a>	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	-55 to 125	HC221M
<a href="#">CD74HC221NSR</a>	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC221M
CD74HC221NSR.A	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC221M
<a href="#">CD74HC221PW</a>	Obsolete	Production	TSSOP (PW)   16	-	-	Call TI	Call TI	-55 to 125	HJ221
<a href="#">CD74HC221PWR</a>	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ221
CD74HC221PWR.A	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ221
<a href="#">CD74HC221PWT</a>	Obsolete	Production	TSSOP (PW)   16	-	-	Call TI	Call TI	-55 to 125	HJ221
<a href="#">CD74HCT221E</a>	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT221E
CD74HCT221E.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT221E
<a href="#">CD74HCT221M</a>	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	-55 to 125	HCT221M
<a href="#">CD74HCT221M96</a>	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT221M
CD74HCT221M96.A	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT221M
<a href="#">CD74HCT221MT</a>	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	-55 to 125	HCT221M

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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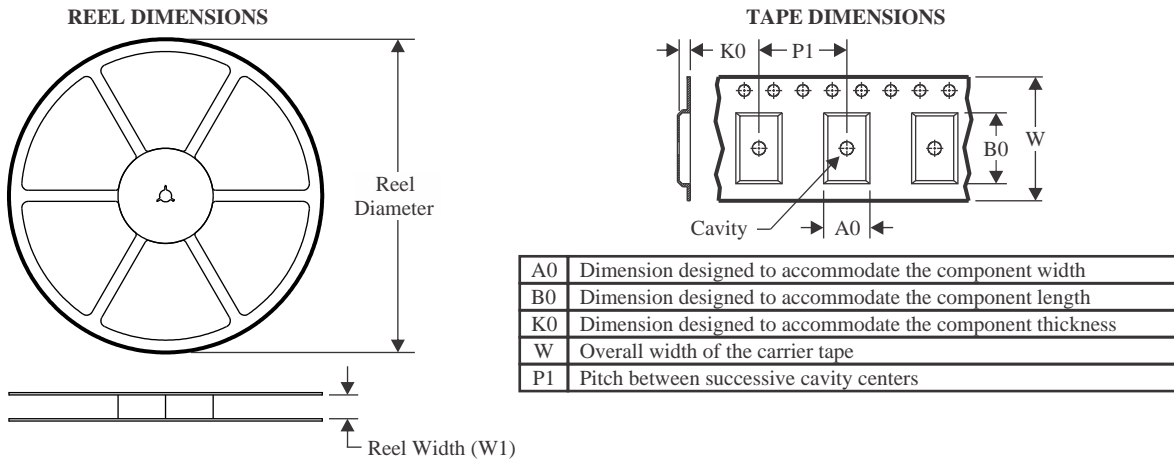
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54HC221, CD74HC221 :**

- Catalog : [CD74HC221](#)
- Military : [CD54HC221](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

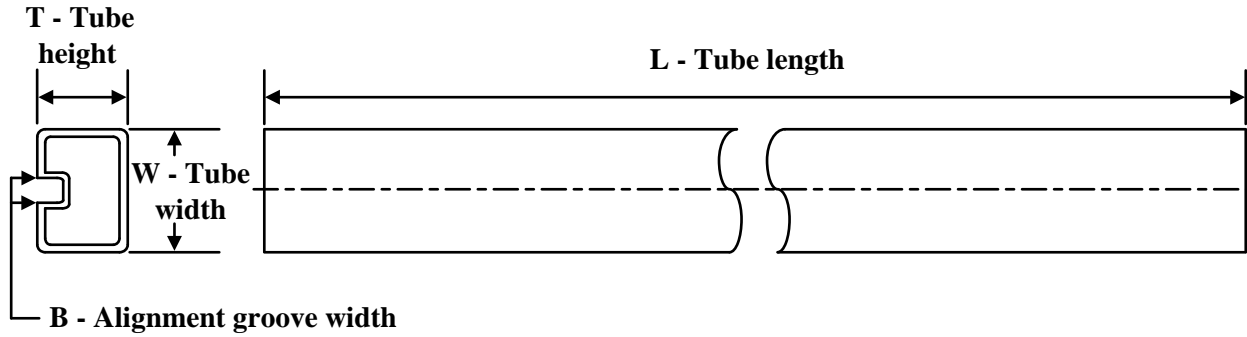
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC221M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC221NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD74HC221PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HCT221M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC221M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HC221NSR	SOP	NS	16	2000	353.0	353.0	32.0
CD74HC221PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
CD74HCT221M96	SOIC	D	16	2500	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC221E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC221E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC221E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC221E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT221E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT221E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT221E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT221E.A	N	PDIP	16	25	506	13.97	11230	4.32

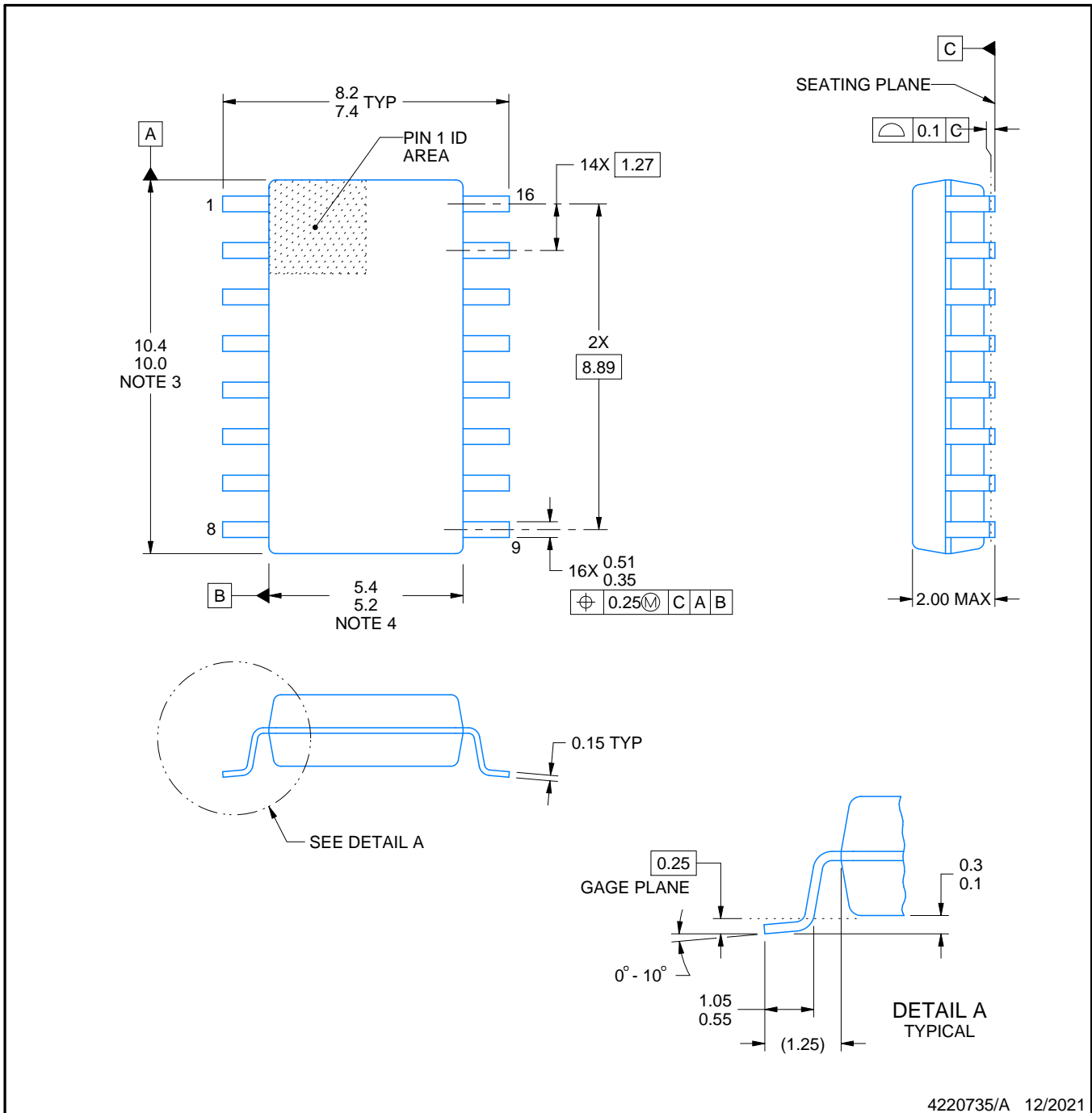


# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



4220735/A 12/2021

#### NOTES:

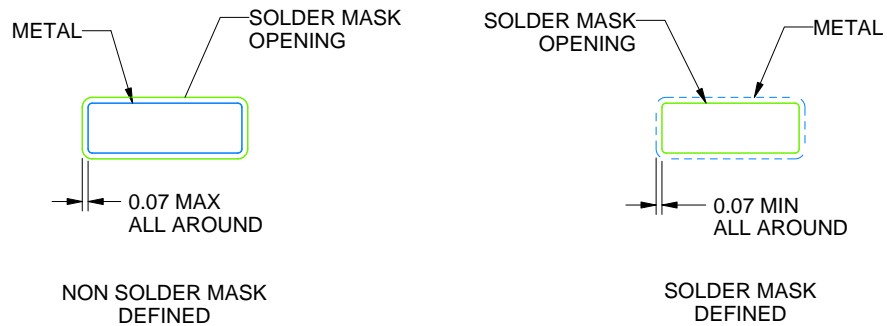
- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

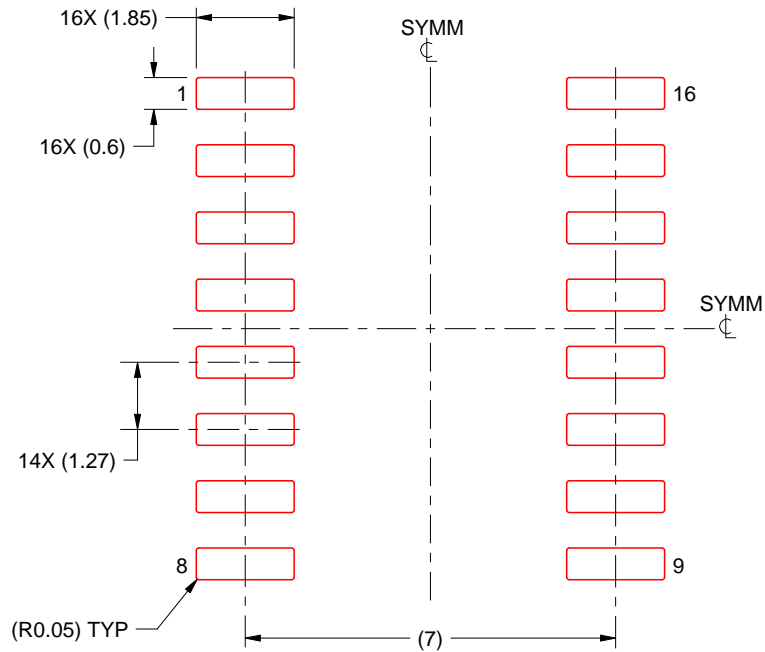
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

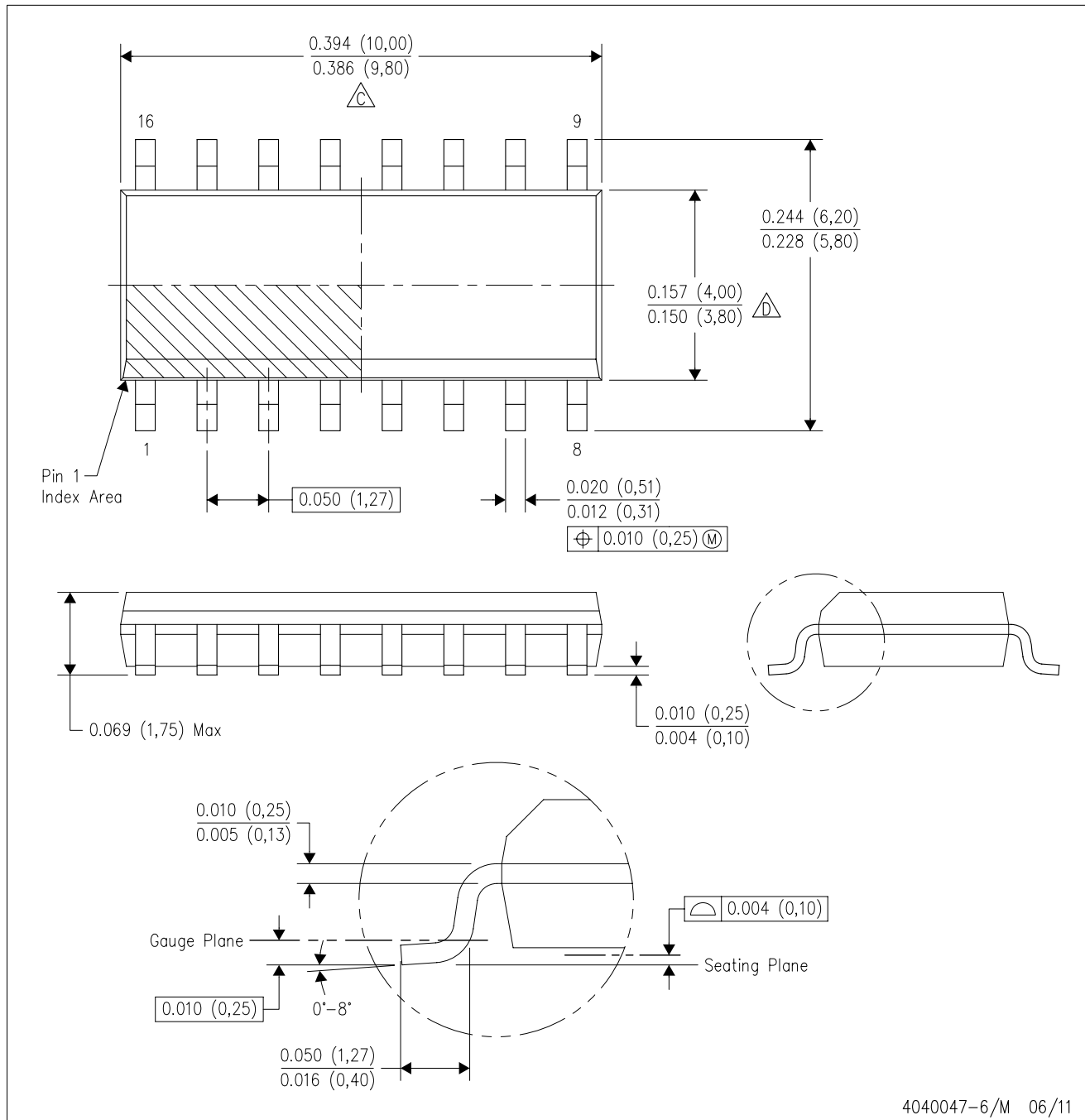
4220735/A 12/2021

NOTES: (continued)



7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE

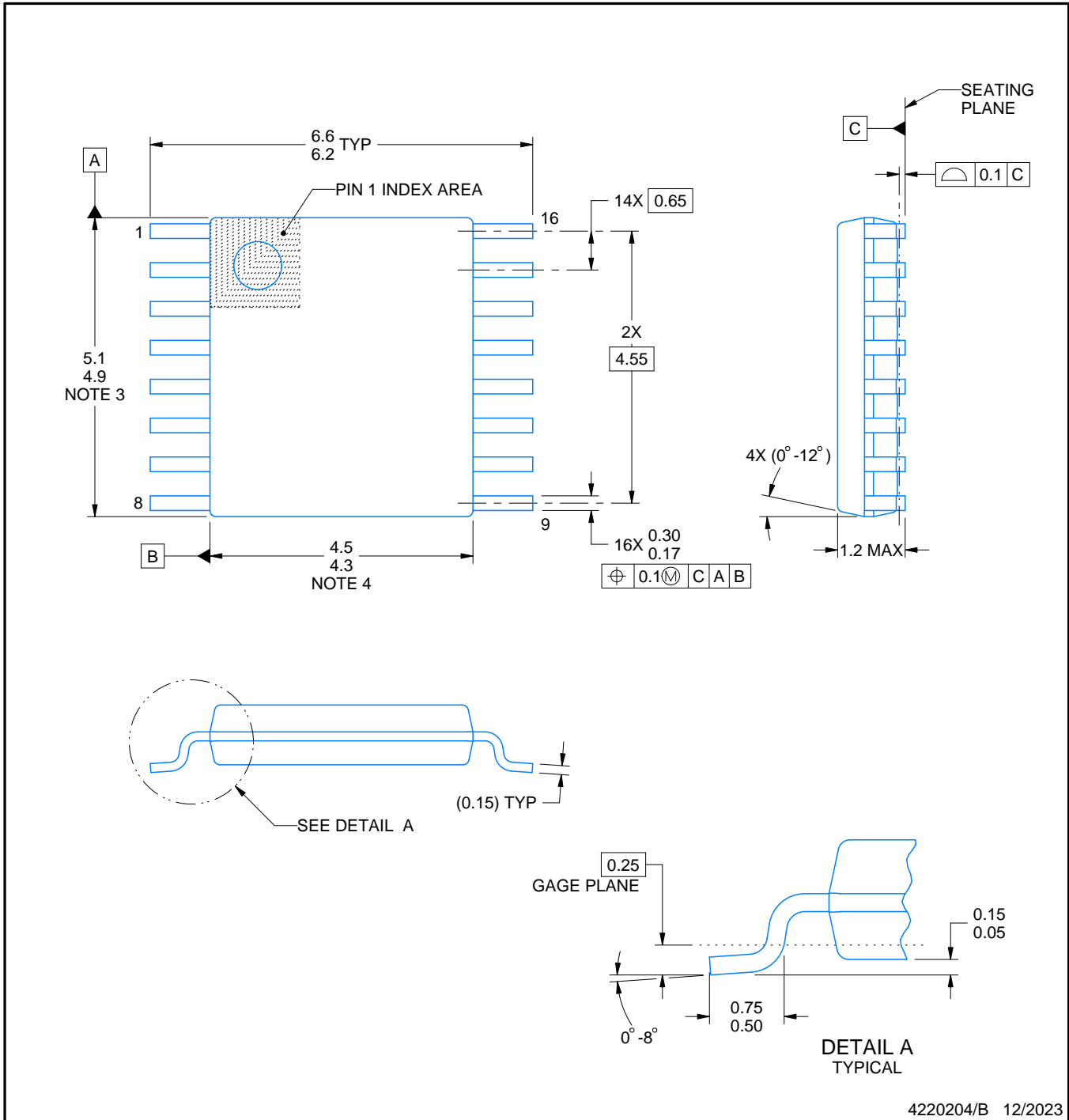


DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



4220204/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

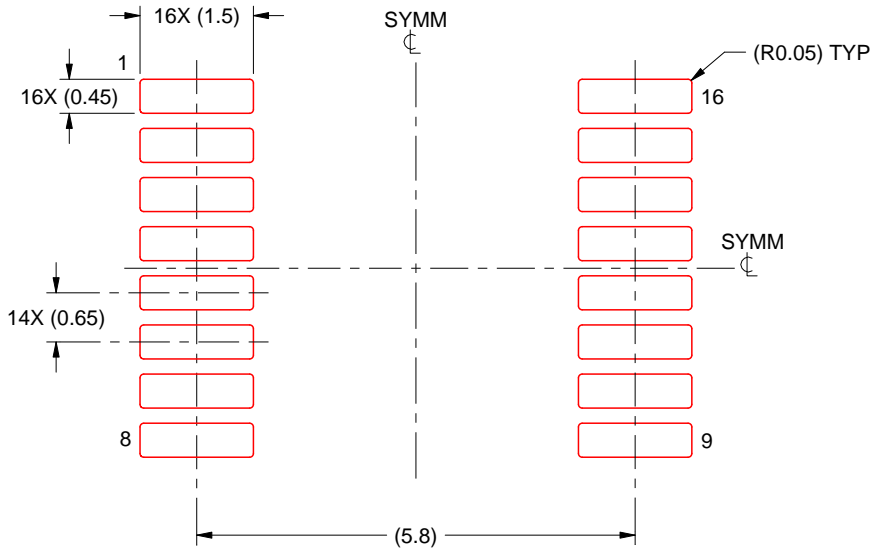
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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