

## CDx4AC05 Hex Inverters With Open-Drain Outputs

### 1 Features

- AC types feature 1.5V to 5.5V operation and balanced noise immunity at 30% of the supply voltage
- Speed of bipolar F, AS, and S, with significantly reduced power consumption
- Fanout to 15 F devices
- SCR-latchup-resistant CMOS process and circuit design
- Exceeds 2kV ESD protection per MIL-STD-883, method 3015

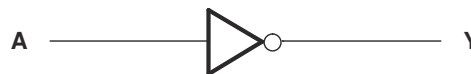
### 2 Description

The 'AC05 devices contain six independent inverters. These devices perform the Boolean function  $Y = \bar{A}$ . The open-drain outputs require pullup resistors to perform correctly, and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

#### Device Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> | BODY SIZE <sup>(3)</sup> |
|-------------|------------------------|-----------------------------|--------------------------|
| CD54AC05    | J (CDIP, 14)           | 19.56mm × 7.9mm             | 19.56mm × 6.67mm         |
| CD74AC05    | BQA (WQFN, 14)         | 3mm × 2.5mm                 | 3mm × 2.5mm              |
|             | D (SOIC, 14)           | 8.65mm × 6mm                | 8.65mm × 3.91mm          |
|             | N (PDIP, 14)           | 19.3mm × 9.4mm              | 19.3mm × 6.35mm          |
|             | PW (TSSOP, 14)         | 5mm × 6.4mm                 | 5mm × 4.4mm              |

- (1) For more information, see [Mechanical, Packaging, and Orderable Information](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



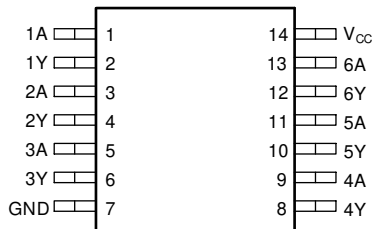
**Logic Diagram, Each Inverter (Positive Logic)**



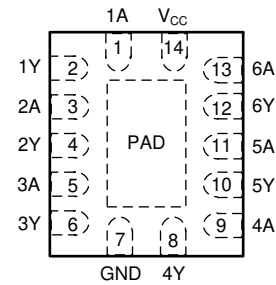
## Table of Contents

|   |   |  |    |
|---|---|--|----|
| <b>1 Features</b> .....   | 1 | 6.1 Functional Block Diagram.....                                | 8  |
| <b>2 Description</b> .....  | 1 | 6.2 Device Functional Modes.....                                 | 8  |
| <b>3 Pin Configuration and Functions</b> .....                                | 3 | <b>7 Application and Implementation</b> .....                    | 9  |
| <b>4 Specifications</b> .....   | 4 | 7.1 Power Supply Recommendations.....                            | 9  |
| 4.1 Absolute Maximum Ratings .....  | 4 | 7.2 Layout.....  | 9  |
| 4.2 ESD Ratings.....  | 4 | <b>8 Device and Documentation Support</b> .....                  | 10 |
| 4.3 Recommended Operating Conditions.....                                     | 4 | 8.1 Documentation Support (Analog).....                          | 10 |
| 4.4 Thermal Information.....  | 4 | 8.2 Receiving Notification of Documentation Updates....          | 10 |
| 4.5 Electrical Characteristics.....   | 5 | 8.3 Support Resources.....                                       | 10 |
| 4.6 Switching Characteristics, $V_{CC} = 1.5\text{ V}$ .....                  | 5 | 8.4 Trademarks.....  | 10 |
| 4.7 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ..... | 5 | 8.5 Electrostatic Discharge Caution.....                         | 10 |
| 4.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .....   | 5 | 8.6 Glossary.....  | 10 |
| 4.9 Operating Characteristics.....  | 6 | <b>9 Revision History</b> .....                                  | 10 |
| <b>5 Parameter Measurement Information</b> .....                              | 7 | <b>10 Mechanical, Packaging, and Orderable Information</b> ..... | 11 |
| <b>6 Detailed Description</b> .....   | 8 |  |    |

### 3 Pin Configuration and Functions



**Figure 3-1. CD54AC05 J Package, 14-Pin CDIP; CD74AC05 D, N, or PW Packages; 14-Pin SOIC, PDIP, or TSSOP (Top View)**



**Figure 3-2. CD74AC05 BQA Package, 14-Pin WQFN**

**Table 3-1. Pin Functions**

| NAME            | PIN           |          | I/O <sup>(1)</sup> | DESCRIPTION  |
|-----------------|---------------|----------|--------------------|--|
|                 | CD74AC05      | CD54AC05 |                    |  |
|                 | BQA, D, N, PW | J        |                    |  |
| 1A              | 1             | 1        | I                  | 1A Input   |
| 1Y              | 2             | 2        | O                  | 1Y Output  |
| 2A              | 3             | 3        | I                  | 2A Input   |
| 2Y              | 4             | 4        | O                  | 2Y Output  |
| 3A              | 5             | 5        | I                  | 3A Input   |
| 3Y              | 6             | 6        | O                  | 3Y Output  |
| GND             | 7             | 7        | —                  | Ground Pin   |
| 4Y              | 8             | 8        | O                  | 4Y Output  |
| 4A              | 9             | 9        | I                  | 4A Input   |
| 5Y              | 10            | 10       | I                  | 5Y Output  |
| 5A              | 11            | 11       | I                  | 5A Input   |
| 6Y              | 12            | 12       | O                  | 6Y Output  |
| 6A              | 13            | 13       | I                  | 6A Input   |
| V <sub>CC</sub> | 14            | 14       | —                  | Power Pin  |
| NC              | —             | —        | —                  | No Connection  |
| Thermal pad     |               |          | —                  | Connect the GND pin to the exposed thermal pad for correct operation. Connect the thermal pad to any internal PCB ground plane using multiple vias for good thermal performance. |

(1) I = input, O = output, P = power, FB = feedback, GND = ground, N/A = not applicable

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                     | MIN  | MAX | UNIT   |
|------------------|-------------------------------------|--|-----|--------|
| V <sub>CC</sub>  | Supply voltage range                | -0.5   | 6   | V      |
| I <sub>IK</sub>  | Input clamp current <sup>(2)</sup>  | V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub> |     | ±20 mA |
| I <sub>OK</sub>  | Output clamp current <sup>(2)</sup> | V <sub>O</sub> < 0                                     |     | -50 mA |
| I <sub>O</sub>   | Continuous current                  |  |     | ±50 mA |
| T <sub>stg</sub> | Storage temperature range           | -65  | 150 | °C     |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative voltage ratings may be exceeded if the input and output current ratings are observed.

### 4.2 ESD Ratings

|                    |                         | VALUE   | UNIT    |
|--------------------|-------------------------|---|---------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup> | ±2000 V |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 4.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                 |                                    | T <sub>A</sub> = 25°C            |                 | -40°C TO 85°C |                 | -55°C TO 125°C |                 | UNIT  |
|-----------------|------------------------------------|----------------------------------|-----------------|---------------|-----------------|----------------|-----------------|-------|
|                 |                                    | MIN                              | MAX             | MIN           | MAX             | MIN            | MAX             |       |
| V <sub>CC</sub> | Supply voltage                     | 1.5                              | 5.5             | 1.5           | 5.5             | 1.5            | 5.5             | V     |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 1.5 V          |                 | 1.2           |                 | 1.2            |                 | V     |
|                 |                                    | V <sub>CC</sub> = 3 V            |                 | 2.1           |                 | 2.1            |                 |       |
|                 |                                    | V <sub>CC</sub> = 5.5 V          |                 | 3.85          |                 | 3.85           |                 |       |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 1.5 V          |                 | 0.3           |                 | 0.3            |                 | V     |
|                 |                                    | V <sub>CC</sub> = 3 V            |                 | 0.9           |                 | 0.9            |                 |       |
|                 |                                    | V <sub>CC</sub> = 5.5 V          |                 | 1.65          |                 | 1.65           |                 |       |
| V <sub>I</sub>  | Input voltage                      | 0                                | V <sub>CC</sub> | 0             | V <sub>CC</sub> | 0              | V <sub>CC</sub> | V     |
| V <sub>O</sub>  | Output voltage                     | 0                                | 5.5             | 0             | 5.5             | 0              | 5.5             | V     |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 4.5 V to 5.5 V |                 | 24            |                 | 24             |                 | 24 mA |
| Δt/Δv           | Input transition rise or fall rate | V <sub>CC</sub> = 1.5 V to 3 V   |                 | 50            |                 | 50             |                 | ns/V  |
|                 |                                    | V <sub>CC</sub> = 3.6 V to 5.5 V |                 | 20            |                 | 20             |                 |       |

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### 4.4 Thermal Information

| THERMAL METRIC <sup>1</sup> | CD74AC05                               |          |          |            | UNIT  |      |
|-----------------------------|--|----------|----------|------------|-------|------|
|                             | BQA (WQFN)                             | D (SOIC) | N (PDIP) | PW (TSSOP) |       |      |
|                             | 14 PINS                                |          |          |            |       |      |
| R <sub>θJA</sub>            | Junction-to-ambient thermal resistance | 85.4     | 89.9     | 80         | 132.2 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, ([SPRA953](#)).

## 4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER       | TEST CONDITIONS   |  | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     | –40°C TO 85°C |     | –55°C TO 125°C |     | UNIT |
|-----------------|---|--|-----------------|-----------------------|-----|---------------|-----|----------------|-----|------|
|                 |   |  |                 | MIN                   | MAX | MIN           | MAX | MIN            | MAX |      |
| V <sub>OL</sub> | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>         | I <sub>OL</sub> = 50 μA                | 1.5 V           | 0.1                   |     | 0.1           |     | 0.1            |     | V    |
|                 |   |  | 3 V             | 0.1                   |     | 0.1           |     | 0.1            |     |      |
|                 |   |  | 4.5 V           | 0.1                   |     | 0.1           |     | 0.1            |     |      |
|                 |   | I <sub>OL</sub> = 12 mA                | 3 V             | 0.36                  |     | 0.44          |     | 0.5            |     |      |
|                 |   | I <sub>OL</sub> = 24 mA                | 4.5 V           | 0.36                  |     | 0.44          |     | 0.5            |     |      |
|                 |   | I <sub>OL</sub> = 50 mA <sup>(1)</sup> | 5.5 V           |                       |     |               |     | 1.65           |     |      |
|                 |   | I <sub>OL</sub> = 75 mA <sup>(1)</sup> | 5.5 V           |                       |     | 1.65          |     |                |     |      |
| I <sub>I</sub>  | V <sub>I</sub> = V <sub>CC</sub> or GND                     |  | 5.5 V           | ±0.1                  |     | ±1            |     | ±1             |     | μA   |
| I <sub>CC</sub> | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 |  | 5.5 V           | 4                     |     | 40            |     | 80             |     | μA   |
| C <sub>I</sub>  |   |  |                 | 10                    |     | 10            |     | 10             |     | pF   |

(1) Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

## 4.6 Switching Characteristics, V<sub>CC</sub> = 1.5 V

over recommended operating free-air temperature range, V<sub>CC</sub> = 1.5 V, C<sub>L</sub> = 50 pF (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| PARAMETER        | FROM (INPUT) | TO (OUTPUT) | –40°C TO 85°C |     | –55°C TO 125°C |     | UNIT |
|------------------|--------------|-------------|---------------|-----|----------------|-----|------|
|                  |              |             | MIN           | MAX | MIN            | MAX |      |
| t <sub>PLZ</sub> | A            | Y           | 94            |     | 103            |     | ns   |
| t <sub>PZL</sub> |              |             | 74            |     | 81             |     |      |

## 4.7 Switching Characteristics, V<sub>CC</sub> = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V, C<sub>L</sub> = 50 pF (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| PARAMETER        | FROM (INPUT) | TO (OUTPUT) | –40°C TO 85°C |      | –55°C TO 125°C |      | UNIT |
|------------------|--------------|-------------|---------------|------|----------------|------|------|
|                  |              |             | MIN           | MAX  | MIN            | MAX  |      |
| t <sub>PLZ</sub> | A            | Y           | 3             | 10.4 | 2.9            | 11.5 | ns   |
| t <sub>PZL</sub> |              |             | 2.3           | 8.3  | 2.3            | 9.1  |      |

## 4.8 Switching Characteristics, V<sub>CC</sub> = 5 V ± 0.5 V

over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V, C<sub>L</sub> = 50 pF (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

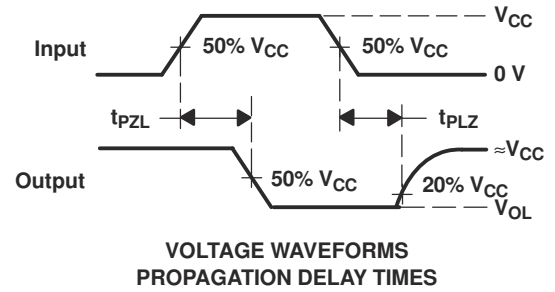
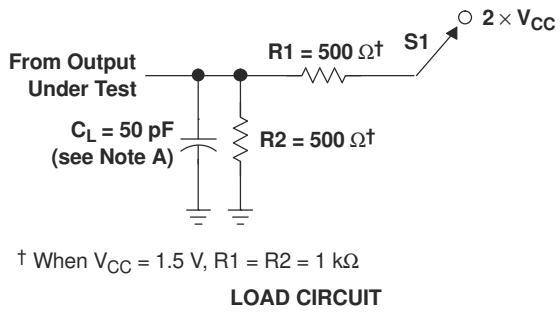
| PARAMETER        | FROM (INPUT) | TO (OUTPUT) | –40°C TO 85°C |     | –55°C TO 125°C |     | UNIT |
|------------------|--------------|-------------|---------------|-----|----------------|-----|------|
|                  |              |             | MIN           | MAX | MIN            | MAX |      |
| t <sub>PLZ</sub> | A            | Y           | 2.2           | 7.5 | 2.1            | 8.2 | ns   |
| t <sub>PZL</sub> |              |             | 1.7           | 5.9 | 1.6            | 6.5 |      |

## 4.9 Operating Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER |                               | TYP | UNIT |
|-----------|-------------------------------|-----|------|
| $C_{pd}$  | Power dissipation capacitance | 105 | pF   |

## 5 Parameter Measurement Information



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 3 \text{ ns}$ ,  $t_f \leq 3 \text{ ns}$ .  
 C. The outputs are measured one at a time, with one input transition per measurement.

**Figure 5-1. Load Circuit and Voltage Waveforms**

## 6 Detailed Description

### 6.1 Functional Block Diagram

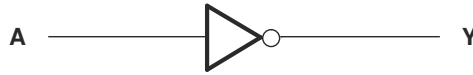


Figure 6-1. Logic Diagram, Each Inverter (Positive Logic)

### 6.2 Device Functional Modes

Function Table  
(Each Inverter)

| INPUT<br>A | OUTPUT<br>Y |
|------------|-------------|
| H          | L           |
| L          | Z           |



## 7 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended. If there are multiple  $V_{CC}$  pins, 0.01  $\mu\text{F}$  or 0.022  $\mu\text{F}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

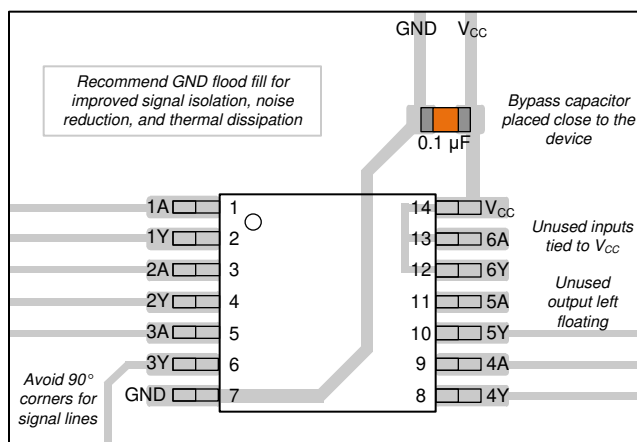
### 7.2 Layout

#### 7.2.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in [Figure 7-1](#) are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ ; whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the IOs, so they cannot float when disabled.

#### 7.2.2 Layout Example



**Figure 7-1. Example Layout for the CD74AC05**

## 8 Device and Documentation Support

### 8.1 Documentation Support (Analog)

#### 8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 8-1. Related Links**

| PARTS    | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| CD54AC05 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| CD74AC05 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision D (August 2024) to Revision E (November 2024) Page

- Added BQA and PW packages to *Device Information* table, *Pin Configuration and Functions* section, and *Thermal Information* table.....1

### Changes from Revision C (June 2002) to Revision D (August 2024) Page

- Added *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Device Functional Modes*, Application and Implementation section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ..... 1
- Updated packages from E and M to N and D throughout data sheet..... 1

- 
- Updated R $\theta$ JA values: D = 86 to 89.9, all values in °C/W.....4
- 

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">CD54AC05F3A</a>  | Active        | Production           | CDIP (J)   14   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54AC05F3A         |
| CD54AC05F3A.A                | Active        | Production           | CDIP (J)   14   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54AC05F3A         |
| <a href="#">CD74AC05BQAR</a> | Active        | Production           | WQFN (BQA)   14 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | AC05                |
| CD74AC05BQAR.A               | Active        | Production           | WQFN (BQA)   14 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | AC05                |
| <a href="#">CD74AC05E</a>    | Active        | Production           | PDIP (N)   14   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74AC05E           |
| CD74AC05E.A                  | Active        | Production           | PDIP (N)   14   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74AC05E           |
| <a href="#">CD74AC05M</a>    | Obsolete      | Production           | SOIC (D)   14   | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | AC05M               |
| <a href="#">CD74AC05M96</a>  | Active        | Production           | SOIC (D)   14   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | AC05M               |
| CD74AC05M96.A                | Active        | Production           | SOIC (D)   14   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | AC05M               |
| CD74AC05M961G4               | Active        | Production           | SOIC (D)   14   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | AC05M               |
| CD74AC05M961G4.A             | Active        | Production           | SOIC (D)   14   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | AC05M               |
| <a href="#">CD74AC05PWR</a>  | Active        | Production           | TSSOP (PW)   14 | 3000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -55 to 125   | AC05                |
| CD74AC05PWR.A                | Active        | Production           | TSSOP (PW)   14 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | AC05                |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54AC05, CD74AC05 :**

- Catalog : [CD74AC05](#)
- Military : [CD54AC05](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74AC05BQAR | WQFN         | BQA             | 14   | 3000 | 180.0              | 12.4               | 2.8     | 3.3     | 1.1     | 4.0     | 12.0   | Q1            |
| CD74AC05M96  | SOIC         | D               | 14   | 2500 | 330.0              | 12.4               | 3.75    | 3.75    | 1.15    | 8.0     | 12.0   | Q1            |
| CD74AC05PWR  | TSSOP        | PW              | 14   | 3000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| CD74AC05PWR  | TSSOP        | PW              | 14   | 3000 | 330.0              | 12.4               | 6.85    | 5.45    | 1.6     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74AC05BQAR | WQFN         | BQA             | 14   | 3000 | 210.0       | 185.0      | 35.0        |
| CD74AC05M96  | SOIC         | D               | 14   | 2500 | 340.5       | 336.1      | 32.0        |
| CD74AC05PWR  | TSSOP        | PW              | 14   | 3000 | 353.0       | 353.0      | 32.0        |
| CD74AC05PWR  | TSSOP        | PW              | 14   | 3000 | 366.0       | 364.0      | 50.0        |

**TUBE**


\*All dimensions are nominal

| Device      | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD74AC05E   | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74AC05E   | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74AC05E.A | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74AC05E.A | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |





# D0014A

# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**BQA 14**

**WQFN - 0.8 mm max height**

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4227145/A



**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

WQFN - 0.8 mm max height

BQA0014A

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 88% PRINTED COVERAGE BY AREA  
 SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G



J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

**NOTES:**

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025