CC2538 适用于 2.4GHz IEEE 802.15.4、6LoWPAN 和 ZigBee®应用的强大无线微控制器片上系统

1 器件概述

1.1 特性

- 微控制器
  - 强大的 ARM® Cortex®-M3，具有代码预提取功能
  - 高达 32MHz 的时钟速度
  - 512KB、256KB 或 128KB 系统内可编程闪存
  - 支持片上无线升级 (OTA)
  - 支持双 Zigbee 应用配置
  - 高达 32KB 的 RAM（其中 16kB 在所有功率模式下具有保持功能）
  - cJTAG 和 JTAG 调试
- 射频 (RF)
  - 2.4GHz IEEE 802.15.4 兼容 RF 收发器
  - -97dBm 的出色接收器灵敏度
  - 在 44dB 的 ACR 干扰情况下可靠耐用
  - 高达 7dBm 的可编程输出功率
- 安全硬件加速
  - 面向未来的 AES-128/256，安全散列算法 (SHA)2 硬件加密引擎
  - 可选 - 用于安全密钥交换的 ECC-128/256，RSA 硬件加速引擎
  - 用于实现底层 MAC 功能性的无线命令选通处理器和数据包操作处理器
- 低功率
  - 有源模式 RX（CPU 闲置）：20mA
  - 0dBm 时的有源模式 TX（CPU 闲置）：24mA
  - 功率模式 1（4µs 唤醒时间，32KB RAM 保持，完全寄存器保持）：0.6mA
  - 功率模式 2（休眠定时器运行，16KB RAM 保持，配置寄存器保持）：1.3µA
  - 功率模式 3（外部中断，16KB RAM 保持，配置寄存器保持）：0.4µA
  - 宽电源电压范围（2V 至 3.6V）
- 外设
  - µDMA
  - 4 个通用定时器（每个定时器为 32 位或 2 x 16 位）
  - 32 位 32kHz 睡眠定时器
  - 具有 8 通道和可配置分辨率的 12 位模数转换器 (ADC)
  - 电池监视器和温度传感器
  - USB 2.0 全速器件 (12Mbps)
  - 2 个串行外设接口 (SPI)
  - 2 个异步收发器 (UART)
  - I2C
  - 32 个通用 I/O 引脚 (28 × 4mA，4 × 20mA)
  - 安全装置定时器
- 布局布线
  - 8mm × 8mm QFN56 封装
  - 可在高达 125°C 的工业温度下运行的耐用器件
  - 极少的外部组件
  - 异步网络只需一个单晶振
- 开发工具
  - CC2538 开发套件
  - 经美国联邦通信委员会 (FCC) 和欧洲电信标准协会 (ETSI) 规则认证的参考设计
  - 为 Contiki/6LoWPAN、智能电网、照明和 Zigbee 家庭自动化提供完整软件支持，其中包括示例 应用 和参考设计
  - Code Composer Studio™
  - IAR Embedded Workbench®用于 ARM
  - SmartRF™Studio
  - SmartRF 闪存编程器

1.2 应用

- 智能电网和家庭局域网
- 家庭和楼宇自动化
- 智能照明系统
- 无线传感器网络
- 物联网

1.3 说明

CC2538xFnn 是适用于高性能 ZigBee 应用的理想无线微控制器片上系统 (SoC)。该器件包含基于 ARM Cortex M3 的强大的 MCU 系统，具有高达 32KB 的片上 RAM 和高达 512KB 的片上闪存以及可靠的 IEEE 802.15.4 射频功能。这使得该器件能够处理涉及安全性、要求严格的 应用程序以及无线下载的复杂网络协议栈。32 个通用输入和输出 (GPIO) 以及串行外设接口可实现到电路板其它部分的简单连接。强大的硬件安全加速器可在 CPU 处理应用任务的同时实现快速且高效的认证和加密。具有保持功能的多个低功耗模式可实现从休眠状态快速唤醒并且显著降低执行周期任务时的能耗。为了实现顺利平稳开发，CC2538xFnn 包括一个强大的调试系统和一个综合性驱动器库。为了减少应用闪存封装尺寸，CC2538xFnn ROM 包含一个实用功能库和一个串行引导加载器。CC2538 与 TI 免费提供的稳健且全面的 Z-Stack 软件解决方案搭配使用，可提供市场上功能最强大、最稳定的 ZigBee 解决方案。

器件信息(1)

器件型号	封装	封装尺寸
CC2538RTQ	RTQ (56)	8.00mm x 8.00mm

(1) 更多信息请参见 节 8，*机械封装和可订购产品信息*。

1.4 功能方框图

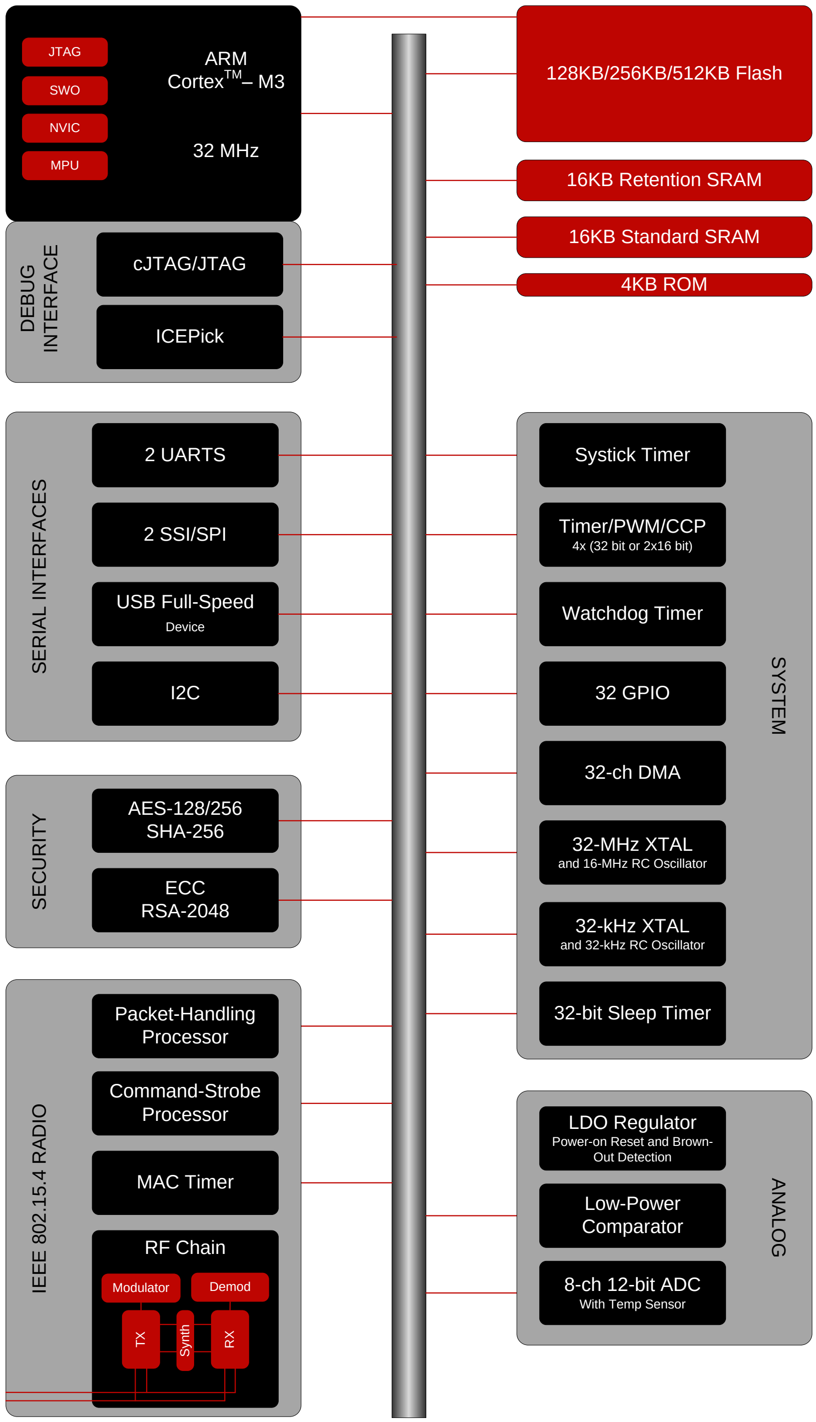


图 **1-1. CC2538** 方框图

内容

2 修订历史记录

Changes from Revision C (February 2015) to Revision D — **Page**

- Changed Figure 6-1 *CC2538xFnn Application Circuit* 19

Changes from Revision B (September 2014) to Revision C — **Page**

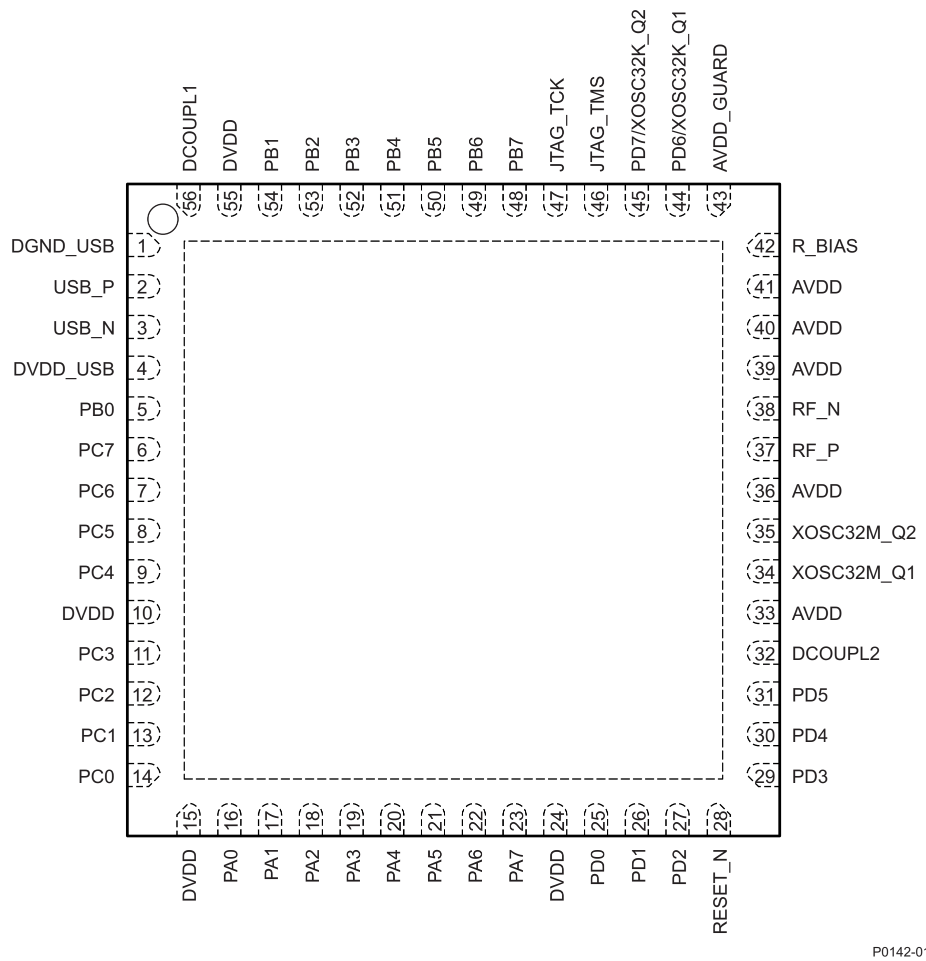
- 已更改 “ZigBee Smart Energy 1.x 和 ZigBee Light Link”至智能电网和照明 1
- 已添加 “8 通道”至“12 位 ADC” 3
- Added ESD Ratings table. 9

3 Device Comparison

Table 3-1. CC2538 Family of Devices Available

DEVICE	FLASH (KB)	RAM (KB)	SECURITY HW AES/SHA	SECURITY HW ECC/RSA
CC2538SF53	512	32	Yes	Yes
CC2538SF23	256	32	Yes	Yes
CC2538NF53	512	32	Yes	No
CC2538NF23	256	32	Yes	No
CC2538NF11	128	16	Yes	No

4 Terminal Configuration and Functions



Connect the exposed ground pad to a solid ground plane, as this is the ground connection for the chip.

Figure 4-1. 56-Pin RTQ Package (Top View)

4.1 Signal Descriptions

Table 4-1. Signal Descriptions

NAME	NUMBER	PIN TYPE	DESCRIPTION
AVDD	33, 36, 39, 40, 41	Power (analog)	2-V–3.6-V analog power-supply connection
AVDD_GUARD	43	Power (analog)	2-V–3.6-V analog power-supply connection
DCOUPL1	56	Power (digital)	1.8-V regulated digital-supply decoupling capacitor
DCOUPL2	32	Power (digital)	1.8-V regulated digital-supply decoupling capacitor. Short this pin to pin 56.
DGND_USB	1	Ground (USB pads)	USB ground
DVDD	10, 15, 24, 55	Power (digital)	2-V–3.6-V digital power-supply connection
DVDD_USB	4	Power (USB pads)	3.3-V USB power-supply connection
JTAG_TCK	47	Digital I/O	JTAG TCK
JTAG_TMS	46	Digital I/O	JTAG TMS
PA0	16	Digital/analog I/O	GPIO port A pin 0. ROM bootloader UART RXD
PA1	17	Digital/analog I/O	GPIO port A pin 1. ROM bootloader UART TXD
PA2	18	Digital/analog I/O	GPIO port A pin 2. ROM bootloader SSI CLK

Table 4-1. Signal Descriptions (continued)

NAME	NUMBER	PIN TYPE	DESCRIPTION
PA3	19	Digital/analog I/O	GPIO port A pin 3. ROM bootloader SSI SEL
PA4	20	Digital/analog I/O	GPIO port A pin 4. ROM bootloader SSI RXD
PA5	21	Digital/analog I/O	GPIO port A pin 5. ROM bootloader SSI TXD
PA6	22	Digital/analog I/O	GPIO port A pin 6
PA7	23	Digital/analog I/O	GPIO port A pin 7
PB0	5	Digital I/O	GPIO port B pin 0
PB1	54	Digital I/O	GPIO port B pin 1
PB2	53	Digital I/O	GPIO port B pin 2
PB3	52	Digital I/O	GPIO port B pin 3
PB4	51	Digital I/O	GPIO port B pin 4
PB5	50	Digital I/O	GPIO port B pin 5
PB6	49	Digital I/O	GPIO port B pin 6, TDI (JTAG)
PB7	48	Digital I/O	GPIO port B pin 7, TDO (JTAG)
PC0	14	Digital I/O	GPIO port C pin 0, 20 mA output capability, no pull-up or pull-down
PC1	13	Digital I/O	GPIO port C pin 1, 20 mA output capability, no pull-up or pull-down
PC2	12	Digital I/O	GPIO port C pin 2, 20 mA output capability, no pull-up or pull-down
PC3	11	Digital I/O	GPIO port C pin 3, 20 mA output capability, no pull-up or pull-down
PC4	9	Digital I/O	GPIO port C pin 4
PC5	8	Digital I/O	GPIO port C pin 5
PC6	7	Digital I/O	GPIO port C pin 6
PC7	6	Digital I/O	GPIO port C pin 7
PD0	25	Digital I/O	GPIO port D pin 0
PD1	26	Digital I/O	GPIO port D pin 1
PD2	27	Digital I/O	GPIO port D pin 2
PD3	29	Digital I/O	GPIO port D pin 3
PD4	30	Digital I/O	GPIO port D pin 4
PD5	31	Digital I/O	GPIO port D pin 5
PD6/XOSC32K_Q1	44	Digital/analog I/O	GPIO port D pin 6 / 32-kHz crystal oscillator pin 1
PD7/XOSC32K_Q2	45	Digital/analog I/O	GPIO port D pin 7 / 32-kHz crystal oscillator pin 1
R_BIAS	42	Analog I/O	External precision bias resistor for reference current
RESET_N	28	Digital input	Reset, active-low
RF_N	38	RF I/O	Negative RF input signal to LNA during RX Negative RF output signal from PA during TX
RF_P	37	RF I/O	Positive RF input signal to LNA during RX Positive RF output signal from PA during TX
USB_P	2	USB I/O	USB differential data plus (D+)
USB_N	3	USB I/O	USB differential data minus (D–)
XOSC32M_Q1	34	Analog I/O	32-MHz crystal oscillator pin 1 or external-clock input
XOSC32M_Q2	35	Analog I/O	32-MHz crystal oscillator pin 2

5 Specifications

5.1 Absolute Maximum Ratings (1)(2)(3)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	All supply pins must have the same voltage	–0.3	3.9	V
Voltage on any digital pin		–0.3	V_{DD} + 0.3, ≤ 3.9	V
Input RF level			10	dBm
T_{stg}	Storage temperature range	–40	125	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.
(3) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge (ESD) performance:	Human body model (HBM), per ANSI/ESDA/JEDEC JS001 (1)		±1	kV
		Charged device model (CDM), per JESD22-C101 (2)	All pins	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating ambient temperature range, T_A	–40	125	°C
Operating supply voltage (1)	2	3.6	V

(1) The CC2538 contains a power on reset (POR) module and a brown out detector (BOD) that prevent the device from operating under unsafe supply voltage conditions. In the two lowest power modes, PM2 and PM3, the POR is active but the BOD is powered down, which gives a limited voltage supervision.
If the supply voltage is lowered to below 1.4 V during PM2/PM3, at temperatures of 70°C or higher, and then brought back up to good operating voltage before active mode is re-entered, registers and RAM contents that are saved in PM2, PM3 may become altered. Hence, care should be taken in the design of the system power supply to ensure that this does not occur. The voltage can be periodically supervised accurately by entering active mode, as a BOD reset is triggered if the supply voltage is below approximately 1.7 V.

5.4 Electrical Characteristics

Measured on TI's CC2538 EM reference design with T_A = 25°C, V_{DD} = 3 V, and 8-MHz system clock, unless otherwise noted. **Boldface** limits apply over the entire operating range, T_A = –40°C to 125°C, V_{DD} = 2 V to 3.6 V, and f_c = 2394 MHz to 2507 MHz.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{core}	Core current consumption	Digital regulator on. 16-MHz RCOSC running. No radio, crystals, or peripherals active. CPU running at 16-MHz with flash access		7		mA
		32-MHz XOSC running. No radio or peripherals active. CPU running at 32-MHz with flash access,.		13		mA
		32-MHz XOSC running, radio in RX mode, –50-dBm input power, no peripherals active, CPU idle		20		mA
		32-MHz XOSC running, radio in RX mode at –100-dBm input power (waiting for signal), no peripherals active, CPU idle		24	27	mA
		32-MHz XOSC running, radio in TX mode, 0-dBm output power, no peripherals active, CPU idle		24		mA
		32-MHz XOSC running, radio in TX mode, 7-dBm output power, no peripherals active, CPU idle		34		mA
		Power mode 1. Digital regulator on; 16-MHz RCOSC and 32-MHz crystal oscillator off; 32.768-kHz XOSC, POR, BOD and sleep timer active; RAM and register retention		0.6		mA
		Power mode 2. Digital regulator off; 16-MHz RCOSC and 32-MHz crystal oscillator off; 32.768-kHz XOSC, POR, and sleep timer active; RAM and register retention		1.3	2	µA
		Power mode 3. Digital regulator off; no clocks; POR active; RAM and register retention		0.4	1	µA
I_{peri}	**Peripheral Current Consumption** (Adds to core current I_{core} for each peripheral unit activated)					
	General-purpose timer	Timer running, 32-MHz XOSC used		120		µA
	SPI			300		µA
	I2C			0.1		mA
	UART			0.7		mA
	Sleep timer	Including 32.753-kHz RCOSC		0.9		µA
	USB	48-MHz clock running, USB enabled		3.8		mA
	ADC	When converting		1.2		mA
	Flash	Erase		12		mA
		Burst-write peak current		8		mA

5.5 General Characteristics

Measured on TI's CC2538 EM reference design with T_A = 25 °C and V_{DD} = 3 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Wake-Up and Timing					
Power mode 1 → active	Digital regulator on, 16-MHz RCOSC and 32-MHz crystal oscillator off. Start-up of 16-MHz RCOSC		4		µs
Power mode 2 or 3 → active	Digital regulator off, 16-MHz RCOSC and 32-MHz crystal oscillator off. Start-up of regulator and 16-MHz RCOSC		136		µs
Active → TX or RX	Initially running on 16-MHz RCOSC, with 32-MHz XOSC off		0.5		ms
	With 32-MHz XOSC initially on			192	µs
RX/TX and TX/RX turnaround				192	µs
USB PLL start-up time	With 32-MHz XOSC initially on		32		µs
Radio Part					
RF frequency range	Programmable in 1-MHz steps, 5 MHz between channels for compliance with (1)	2394		2507	MHz
Radio baud rate	As defined by (1)		250		kbps
Radio chip rate	As defined by (1)		2		MChip/s
Flash Memory					
Flash erase cycles				20	k Cycles
Flash page size			2		KB

(1) IEEE Std. 802.15.4-2006: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs)
http://standards.ieee.org/getieee802/download/802.15.4-2006.pdf

5.6 RF Receive Section

Measured on TI's CC2538 EM reference design with T_A = 25°C, V_{DD} = 3 V, and f_c = 2440 MHz, unless otherwise noted. **Bold** limits apply over the entire operating range, T_A = –40°C to 125°C, V_{DD} = 2 V to 3.6 V, and f_c = 2394 MHz to 2507 MHz.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver sensitivity	PER = 1%, as specified by (1), normal operating conditions (25 °C, 3 V, 2440 MHz) (1) requires –85 dBm		–97	–92	dBm
	PER = 1%, as specified by (1), entire operating conditions (1) requires –85 dBm			**–88**	dBm
Saturation (maximum input level)	PER = 1%, as specified by (1) (1) requires –20 dBm		10		dBm
Adjacent-channel rejection, 5-MHz channel spacing	Wanted signal –82 dBm, adjacent modulated channel at 5 MHz, PER = 1%, as specified by (1). (1) requires 0 dB		44		dB
Adjacent-channel rejection, –5-MHz channel spacing	Wanted signal –82 dBm, adjacent modulated channel at –5 MHz, PER = 1%, as specified by (1). (1) requires 0 dB		44		dB
Alternate-channel rejection, 10-MHz channel spacing	Wanted signal –82 dBm, adjacent modulated channel at 10 MHz, PER = 1%, as specified by (1) (1) requires 30 dB		52		dB
Alternate-channel rejection, –10-MHz channel spacing	Wanted signal –82 dBm, adjacent modulated channel at –10 MHz, PER = 1%, as specified by (1) (1) requires 30 dB		52		dB
Channel rejection ≥ 20 MHz ≤ –20 MHz	Wanted signal at –82 dBm. Undesired signal is an IEEE 802.15.4 modulated channel, stepped through all channels from 2405 to 2480 MHz. Signal level for PER = 1%.		 51 51		dB
Blocking/desensitization 5 MHz from band edge 10 MHz from band edge 20 MHz from band edge 50 MHz from band edge –5 MHz from band edge –10 MHz from band edge –20 MHz from band edge –50 MHz from band edge	Wanted signal 3 dB above the sensitivity level, CW jammer, PER = 1%. Measured according to EN 300 440 class 2.		 –35 –34 –37 –32 –37 –38 –35 –34		dBm
Spurious emission. Only largest spurious emission stated within each band. 30 MHz–1000 MHz 1 GHz–12.75 GHz	Conducted measurement with a 50-Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440, FCC CFR47 Part 15, and ARIB STD-T-66.		 –80 –80		dBm
Frequency error tolerance (2)	(1) requires minimum 80 ppm		±150		ppm
Symbol rate error tolerance (3)	(1) requires minimum 80 ppm		±1000		ppm

(1) IEEE Std. 802.15.4-2006: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs)
http://standards.ieee.org/getieee802/download/802.15.4-2006.pdf
(2) Difference between center frequency of the received RF signal and local oscillator frequency
(3) Difference between incoming symbol rate and the internally generated symbol rate

5.7 RF Transmit Section

Measured on TI's CC2538 EM reference design with T_A = 25°C, V_{DD} = 3 V and f_c = 2440 MHz, unless otherwise noted. **Boldface** limits apply over the entire operating range, T_A = –40°C to 125°C, V_{DD} = 2 V to 3.6 V, and f_c = 2394 MHz to 2507 MHz.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Nominal output power	Delivered to a single-ended 50-Ω load through a balun using maximum-recommended output-power setting (1) requires minimum –3 dBm		7		dBm
Programmable output-power range			30		dB
Spurious emissions Only largest spurious emission stated within each band.	Maximum recommended output power setting (2) Measured according to stated regulations. 25–1000 MHz (outside restricted bands) 25–1000 MHz (within FCC restricted bands) 25–1000 MHz (within ETSI restricted bands) 1800–1900 MHz (ETSI restricted band) 5150–5300 MHz (ETSI restricted band) 1–12.75 GHz (except restricted bands) At 2483.5 MHz and above (FCC restricted band), f_c= 2480 MHz (3)		–56 –58 –58 –60 –54 –51 –42		dBm
Error vector magnitude (EVM)	Measured as defined by (1) using maximum-recommended output-power setting (1) requires maximum 35%.		3%		
Optimum load impedance	Differential impedance on the RF pins		66 + j64		Ω

(1) IEEE Std. 802.15.4-2006: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs) http://standards.ieee.org/getieee802/download/802.15.4-2006.pdf
(2) TI's CC2538 EM reference design is suitable for systems targeting compliance with EN 300 328, EN 300 440, FCC CFR47 Part 15, and ARIB STD-T-66.
(3) To improve margins for passing FCC requirements at 2483.5 MHz and above when transmitting at 2480 MHz, use a lower output-power setting or less than 100% duty cycle.

5.8 32-MHz Crystal Oscillator

Measured on TI's CC2538 EM reference design with T_A = 25°C and V_{DD} = 3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Crystal frequency			32		MHz
	Crystal frequency accuracy requirement(1)		–40		40	ppm
ESR	Equivalent series resistance		6	16	60	Ω
C_0	Crystal shunt capacitance		1	1.9	7	pF
C_L	Crystal load capacitance		10	13	16	pF
	Start-up time			0.3		ms
	Power-down guard time	The crystal oscillator must be in power down for a guard time before using it again. This requirement is valid for all modes of operation. The need for power-down guard time can vary with crystal type and load.	3			ms

(1) Including aging and temperature dependency, as specified by IEEE Std. 802.15.4-2006: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs) http://standards.ieee.org/getieee802/download/802.15.4-2006.pdf

5.9 32.768-kHz Crystal Oscillator

Measured on TI's CC2538 EM reference design with T_A = 25°C and V_{DD} = 3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Crystal frequency			32.768		kHz
	Crystal frequency accuracy requirement(1)		–40		40	ppm
ESR	Equivalent series resistance			40	130	Ω
C_0	Crystal shunt capacitance			0.9	2	pF
C_L	Crystal load capacitance			12	16	pF
	Start-up time			0.4		s

(1) Including aging and temperature dependency, as specified by IEEE Std. 802.15.4-2006: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs) http://standards.ieee.org/getieee802/download/802.15.4-2006.pdf

5.10 32-kHz RC Oscillator

Measured on TI's CC2538 EM reference design with T_A = 25°C and V_{DD} = 3 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Calibrated frequency(1)			32.753		kHz
Frequency accuracy after calibration			±0.2%		
Temperature coefficient(2)			0.4		%/ °C
Supply-voltage coefficient(3)			3		%/V
Calibration time(4)			2		ms

(1) The calibrated 32-kHz RC oscillator frequency is the 32-MHz XTAL frequency divided by 977.
(2) Frequency drift when temperature changes after calibration
(3) Frequency drift when supply voltage changes after calibration
(4) When the 32-kHz RC oscillator is enabled, it is calibrated when a switch from the 16-MHz RC oscillator to the 32-MHz crystal oscillator is performed while SLEEPCMD.OSC32K_CALDIS is 0.

5.11 16-MHz RC Oscillator

Measured on TI's CC2538 EM reference design with T_A = 25°C and V_{DD} = 3 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency(1)			16		MHz
Uncalibrated frequency accuracy			±18%		
Calibrated frequency accuracy			±0.6%	±1%	
Start-up time				10	µs
Initial calibration time(2)			50		µs

(1) The calibrated 16-MHz RC oscillator frequency is the 32-MHz xtal frequency divided by 2.
(2) When the 16-MHz RC oscillator is enabled, it is calibrated when a switch from the 16-MHz RC oscillator to the 32-MHz crystal oscillator is performed while SLEEPCMD.OSC_PD is set to 0.

5.12 RSSI/CCA Characteristics

Measured on TI's CC2538 EM reference design with T_A = 25°C and V_{DD} = 3 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
RSSI range			100		dB
Absolute uncalibrated RSSI/CCA accuracy			±4		dB
RSSI/CCA offset(1)			73		dB
Step size (LSB value)			1		dB

(1) Real RSSI = Register value – offset

5.13 FREQEST Characteristics

Measured on TI's CC2538 EM reference design with T_A = 25°C and V_{DD} = 3 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQEST range			±250		kHz
FREQEST accuracy			±10		kHz
FREQEST offset(1)			15		kHz
Step size (LSB value)			7.8		kHz

(1) Real FREQEST = Register value – offset

5.14 Frequency Synthesizer Characteristics

Measured on TI's CC2538 EM reference design with T_A = 25°C, V_{DD} = 3 V and f_c = 2440 MHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase noise, unmodulated carrier	At ±1-MHz offset from carrier		–111		dBc/Hz
	At ±2-MHz offset from carrier		–119		
	At ±5-MHz offset from carrier		–126		

5.15 Analog Temperature Sensor

Measured on TI's CC2538 EM reference design with T_A = 25°C and V_{DD} = 3 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output at 25°C	Measured using integrated ADC, using internal band-gap voltage reference and maximum resolution		1422		12-bit ADC
Temperature coefficient			4.2		/1°C
Voltage coefficient			1		/0.1 V
Initial accuracy without calibration			±10		°C
Accuracy using 1-point calibration (entire temperature range)			±5		°C
Current consumption when enabled (ADC current not included)			0.3		mA

5.16 ADC Characteristics

T_A = 25°C and V_{DD} = 3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input voltage	V_{DD} is voltage on AVDD5 pin	0		V_{DD}	V
	External reference voltage	V_{DD} is voltage on AVDD5 pin	0		V_{DD}	V
	External reference voltage differential	V_{DD} is voltage on AVDD5 pin	0		V_{DD}	V
	Input resistance, signal	Using 4-MHz clock speed		197		kΩ
	Full-scale signal (1)	Peak-to-peak, defines 0 dBFS		2.97		V
ENOB (1)	Effective number of bits	Single-ended input, 7-bit setting		5.7		Bits
		Single-ended input, 9-bit setting		7.5		
		Single-ended input, 10-bit setting		9.3		
		Single-ended input, 12-bit setting		10.8		
		Differential input, 7-bit setting		6.5		
		Differential input, 9-bit setting		8.3		
		Differential input, 10-bit setting		10.0		
		Differential input, 12-bit setting		11.5		
	Useful power bandwidth	7-bit setting, both single and differential		0–20		kHz
THD (1)	Total harmonic distortion	Single-ended input, 12-bit setting, –6 dBFS		–75.2		dB
		Differential input, 12-bit setting, –6 dBFS		–86.6		
	Signal to nonharmonic ratio (1)	Single-ended input, 12-bit setting		70.2		dB
		Differential input, 12-bit setting		79.3		
		Single-ended input, 12-bit setting, –6 dBFS		78.8		
		Differential input, 12-bit setting, –6 dBFS		88.9		
CMRR	Common-mode rejection ratio	Differential input, 12-bit setting, 1-kHz sine (0 dBFS), limited by ADC resolution		>84		dB
	Crosstalk	Single-ended input, 12-bit setting, 1-kHz sine (0 dBFS), limited by ADC resolution		< –84		dB
	Offset	Midscale		–3		mV
	Gain error			0.68%		
DNL (1)	Differential nonlinearity	12-bit setting, mean		0.05		LSB
		12-bit setting, maximum		0.9		
INL (1)	Integral nonlinearity	12-bit setting, mean		4.6		LSB
		12-bit setting, maximum		13.3		
SINAD (1) (–THD+N)	Signal-to-noise-and-distortion	Single-ended input, 7-bit setting		35.4		dB
		Single-ended input, 9-bit setting		46.8		
		Single-ended input, 10-bit setting		57.5		
		Single-ended input, 12-bit setting		66.6		
		Differential input, 7-bit setting		40.7		
		Differential input, 9-bit setting		51.6		
		Differential input, 10-bit setting		61.8		
		Differential input, 12-bit setting		70.8		
	Conversion time	7-bit setting		20		µs
		9-bit setting		36		
		10-bit setting		68		
		12-bit setting		132		
	Current consumption			1.2		mA
	Internal reference voltage			1.19		V
	Internal reference VDD coefficient			2		mV/V

(1) Measured with 300-Hz sine-wave input and VDD as reference

ADC Characteristics *(continued)*

T_A = 25°C and V_{DD} = 3 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal reference temperature coefficient			0.4		mV/10 °C

5.17 Control Input AC Characteristics

T_A = –40°C to 125°C, V_{DD} = 2 V to 3.6 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System clock, f_{SYSCLK} $t_{SYSCLK} = 1/f_{SYSCLK}$	The undivided system clock is 32 MHz when crystal oscillator is used. The undivided system clock is 16 MHz when calibrated 16-MHz RC oscillator is used.	16		32	MHz
RESET_N low duration (1)	See item 1, Figure 5-1. This is the shortest pulse that is recognized as a complete reset pin request.	1			µs
Interrupt pulse duration	See item 2, Figure 5-1.This is the shortest pulse that is recognized as an interrupt request.	20			ns

(1) Shorter pulses may be recognized, but might not lead to a complete reset of all modules within the chip.

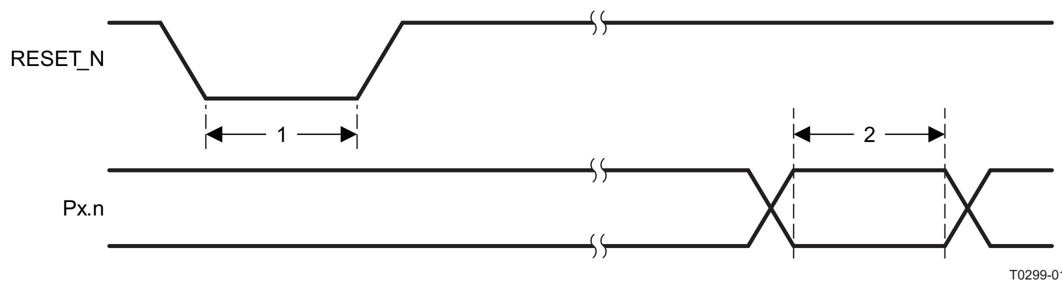


Figure 5-1. Control Input AC Characteristics

5.18 DC Characteristics

T_A = 25°C, VDD = 3 V, drive strength set to high with CC_TESTCTRL.SC = 1, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic-0 input voltage				0.5	V
Logic-1 input voltage		2.5			V
Logic-0 input current	Input equals 0 V	–300		300	nA
Logic-1 input current	Input equals V_{DD}	–300		300	nA
I/O-pin pullup and pulldown resistors			20		kΩ
Logic-0 output voltage, 4-mA pins	Output load 4 mA			0.5	V
Logic-1 output voltage, 4-mA pins	Output load 4 mA	2.4			V
Logic-0 output voltage, 20-mA pins	Output load 20 mA			0.5	V
Logic-1 output voltage, 20-mA pins	Output load 20 mA	2.4			V

5.19 USB Interface DC Characteristics

T_A = 25°C, V_{DD} = 3 V to 3.6 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
USB pad voltage output, high	VDD 3.6 V, 4-mA load		3.4		V
USB pad voltage output, low	VDD 3.6 V, 4-mA load		0.2		V

5.20 Thermal Resistance Characteristics for RTQ Package

NAME	DESCRIPTION	°C/W (1) (2)	AIR FLOW (m/s) (3)
$R\theta_{JC\text{-}top}$	Junction-to-case (top)	8.9	0.00
$R\theta_{JB}$	Junction-to-board	3.1	0.00
$R\theta_{JA}$	Junction-to-free air	25.0	0.00
Psi_{JT}	Junction-to-package top	3.1	0.00
$Psi_{JB\text{-}bottom}$	Junction-to-board (bottom)	0.4	0.00

(1) °C/W = degrees Celsius per watt.
(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(3) m/s = meters per second.

6 Applications, Implementation, and Layout

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Few external components are required for the operation of the CC2538xFnn. Figure 6-1 is a typical application circuit. For a complete USB reference design, see the CC2538xFnn product page on www.ti.com. Table 6-1 lists typical values and descriptions of external components. The USB_P and USB_N pins require series resistors R21 and R31 for impedance matching, and the D+ line must have a pullup resistor, R32. The series resistors should match the 90-Ω ±15% characteristic impedance of the USB bus. Notice that the pullup resistor and DVDD_USB require connection to a voltage source between 3 V and 3.6 V (typically 3.3 V). To accomplish this, it is recommend to connect the D+ pull-up to a port/pin that does not have an internal pullup (that is, PC0..3), instead of connecting it directly to a 3.3 V supply (that is, software control of D+ pullup recommended).

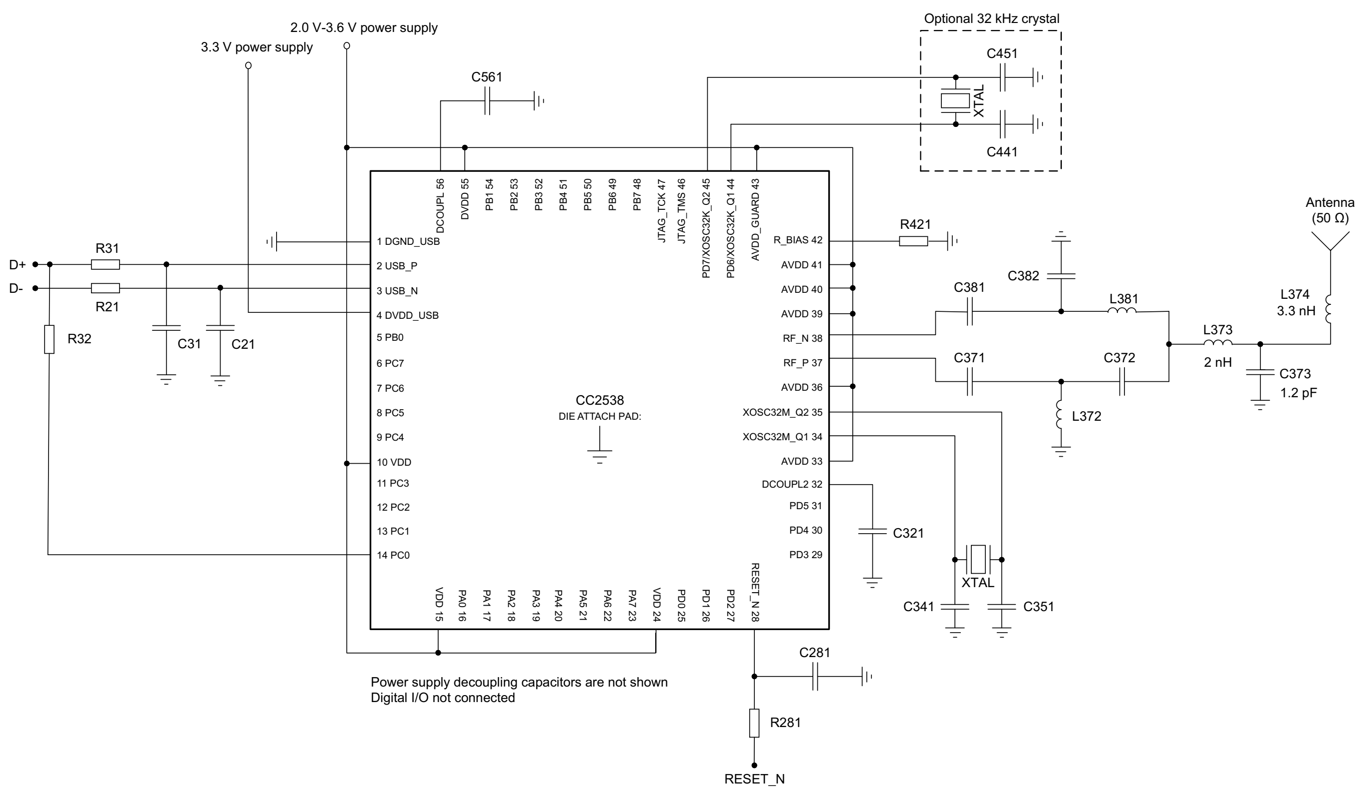


Figure 6-1. CC2538xFnn Application Circuit

Table 6-1. Overview of External Components (Excluding Supply Decoupling Capacitors)

Component	Description	Value
C21	USB D– decoupling	47 pF
C31	USB D+ decoupling	47 pF
C341	32-MHz xtal-loading capacitor	12 pF
C351	32-MHz xtal-loading capacitor	12 pF
C371	Part of the RF matching network	18 pF
C381	Part of the RF matching network	18 pF
C382	Part of the RF matching network	1 pF
C372	Part of the RF matching network	1 pF
C441	32-kHz xtal-loading capacitor	22 pF
C451	32-kHz xtal-loading capacitor	22 pF
C561	Decoupling capacitor for the internal digital regulator	1 µF
C321	Decoupling capacitor for the internal digital regulator	1 µF
C281	Filter capacitor for reset line	1 nF
L372	Part of the RF matching network	2 nH
L381	Part of the RF matching network	2 nH
R21	USB D– series resistor	33 Ω
R31	USB D+ series resistor	33 Ω
R32	USB D+ pullup resistor to signal full-speed device presence	1.5 kΩ
R281	Filter resistor for reset line	2.2 Ω
R421	Resistor used for internal biasing	56 kΩ

6.1 Input, Output Matching

When using an unbalanced antenna such as a monopole, use a balun to optimize performance. One can implement the balun using low-cost, discrete inductors and capacitors. The recommended balun shown in Figure 6-1 consists of L372, C372, C382 and L381.

If a balanced antenna such as a folded dipole is used, omit the balun.

6.2 Crystal

The 32-MHz crystal oscillator uses an external 32-MHz crystal, XTAL1, with two loading capacitors (C341 and C351). See the *32-MHz Crystal Oscillator* section for details. Calculate the load capacitance across the 32-MHz crystal by Equation 1.

$$C_L = \frac{1}{\frac{1}{C_{341}} + \frac{1}{C_{351}}} + C_{parasitic} \quad (1)$$

XTAL2 is an optional 32.768-kHz crystal, with two loading capacitors (C441 and C451) used for the 32.768-kHz crystal oscillator. Use the 32.768-kHz crystal oscillator in applications where both low sleep-current consumption and accurate wake-up times are needed. Calculate the load capacitance across the 32.768-kHz crystal by Equation 2.

$$C_L = \frac{1}{\frac{1}{C_{441}} + \frac{1}{C_{451}}} + C_{parasitic} \quad (2)$$

Use a series resistor, if necessary, to comply with the ESR requirement.

6.3 On-Chip 1.8-V Voltage-Regulator Decoupling

The 1.8-V on-chip voltage regulator supplies the 1.8-V digital logic. This regulator requires decoupling capacitors (C561, C321) and an external connection between them for stable operation.

6.4 Power-Supply Decoupling and Filtering

Optimum performance requires proper power-supply decoupling. The placement and size of the decoupling capacitors and the power supply filtering are important to achieve the best performance in an application. TI provides a recommended compact reference design for the user to follow.

6.5 References

1. IEEE Std. 802.15.4-2006: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs) http://standards.ieee.org/getieee802/download/802.15.4-2006.pdf
2. CC2538xFnn User's Guide
3. Universal Serial Bus Revision 2.0 Specification http://www.usb.org/developers/docs/usb_20_052709.zip

7 器件和文档支持

7.1 器件支持

7.1.1 开发支持

TI 提供大量的开发工具，其中包括评估处理器性能、生成代码、开发算法工具、以及完全集成和调试软件及硬件模块的工具。工具的电子支持文档可从 Code Composer Studio™ 集成开发环境 (IDE) 中获得。

下列产品支持 CC2538 器件的 开发需求：

软件开发工具：Code Composer Studio™ 集成开发环境 (IDE)：其中包括支持任意 CC2538 器件应用所需的以下工具：编辑器、C/C++/汇编代码生成工具、调试工具以及能够提供基本运行时目标软件的可扩展实时基础软件 (DSP/BIOS™)。

硬件开发工具：扩展开发系统 (XDS™) 仿真器

有关 CC2538 平台开发支持工具的完整列表，请访问德州仪器 (TI) 网站 www.ti.com.cn。有关定价和购买信息，请联系最近的 TI 销售办事处或授权分销商。

7.1.2 器件命名规则

为了指出产品开发周期所处的阶段，TI 为所有微处理器 (MPU) 和支持工具的产品型号分配了前缀。每个器件都具有以下三个前缀中的一个：X、P 或无（无前缀）（例如，CC2538）。

器件开发进化流程：

X	试验器件不一定代表最终器件的电气规范标准并且不可使用生产组装流程。
P	原型器件不一定是最终芯片模型并且不一定符合最终电气标准规范。
无	完全合格的芯片模型的生产版本。

支持工具开发进化流程：

X 和 P 器件在供货时附带如下免责声明：

“开发的产品用于内部评估用途。”

生产器件已进行完全特性化，并且器件的质量和可靠性已经完全论证。TI 的标准保修证书适用。

预测显示原型器件（X 或者 P）的故障率大于标准生产器件。由于它们的预计的最终使用故障率仍未定义，德州仪器 (TI) 建议不要将这些器件用于任何生产系统。只有合格的生产器件将被使用。

TI 器件的命名规则也包括一个带有器件系列名称的后缀。这个后缀表示封装类型（例如，RTQ）和温度范围（例如，“空白”是默认的商业级温度范围）。

要获得 RTQ 封装类型的 CC2538 器件订购部件号，请参见本文档的“封装选项附录”（TI 网站 www.ti.com），或者联系您的 TI 销售代表。

7.2 文档支持

以下文档介绍了 CC2538 处理器。在 www.ti.com.cn 内提供这些文档的副本。

SWRZ045 CC2538 适用于 2.4GHz IEEE 802.15.4、6LoWPAN 和 ZigBee 应用的 SoC 勘误

SWRA467 基于 CC2538 开发支持 Zigbee 的低成本智能能量计

SWRA456 支持 Z-Stack 的 CC2538 终端设备功耗测量和优化

SWRA447 使用 CC2592 前端与 CC2538

SWRA437 CC2538 + CC1200 评估模块

SWRA443 使用 GCC/GDB 与 CC2538

SWRU325 CC2538 外设驱动程序库用户指南

SWRU319 用于 2.4GHz IEEE 802.15.4 和 ZigBee/ZigBee IP 应用的 CC2538 SoC 用户指南

SWRU333 CC2538 ROM 用户指南

7.2.1 社区资源

下列链接提供到 TI 社区资源的连接。 链接的内容由各个分销商“按照原样”提供。 这些内容并不构成 TI 技术规范和标准且不一定反映 TI 的观点；请见 TI 的使用条款。

TI E2E™ 在线社区 ***TI 工程师对工程师 (E2E) 社区。*** 此社区的创建目的是为了促进工程师之间协作。 在 e2e.ti.com 中，您可以咨询问题、共享知识、探索思路，在同领域工程师的帮助下解决问题。

德州仪器 **(TI)** 嵌入式处理器维基网站 *德州仪器 **(TI)** 嵌入式处理器维基网站。* 此网站的建立是为了帮助开发人员从德州仪器 (TI) 的嵌入式处理器入门并且也为了促进与这些器件相关的硬件和软件的总体知识的创新和增长。

7.3 其他信息

德州仪器 (TI) 为工业和消费类应用中所使用的专有应用和标准无线 应用 提供各种经济实用的低功耗射频 选择。其中包括适用于 1GHz 以下频段和 2.4GHz 频段的射频收发器、射频发送器、射频前端和片上系统以及各种软件解决方案。

此外，德州仪器 (TI) 还提供广泛的相关支持，例如开发工具、技术文档、参考设计、应用专业技术、客户支持、第三方服务以及大学计划。

低功耗射频 E2E 在线社区设有技术支持论坛并提供视频和博客，您有机会在此与全球同领域工程师交流互动。

凭借丰富的供选产品解决方案、可实现的最终应用以及广泛的技术支持，德州仪器 (TI) 能够为您提供最全面的低功耗射频产品组合。

7.3.1 德州仪器 (TI) 低功耗射频网站

德州仪器 (TI) 的低功耗射频网站提供所有最新产品、应用和设计笔记、FAQ 部分、新闻资讯以及活动更新。请访问 www.ti.com.cn/lprf。

7.3.2 低功耗射频在线社区

- 论坛、视频和博客
- 射频设计帮助
- E2E 交流互动

访问：www.ti.com/lprf-forum 立即体验。

7.3.3 德州仪器 (TI) 低功耗射频开发者网络

德州仪器 (TI) 建立了一个大型低功耗射频开发合作伙伴网络，帮助客户加快应用开发。此网络中包括推荐的公司、射频顾问和独立设计工作室，他们可提供一系列硬件模块产品和设计服务，其中包括：

- 射频电路、低功耗射频和 ZigBee 设计服务
- 低功耗射频和 ZigBee 模块解决方案以及开发工具
- 射频认证服务和射频电路制造

如果需要有关模块、工程服务或开发工具的帮助：

请搜索低功耗射频开发者网络查找适合的合作伙伴。www.ti.com.cn/lprfnetwork

7.3.4 低功耗射频电子新闻简报

通过低功耗射频电子新闻简报，您能够了解到最新的产品、新闻稿、开发者相关新闻以及关于德州仪器 (TI) 低功耗射频产品其它新闻和活动。低功耗射频电子新闻简报文章包含可获取更多在线信息的链接。

访问：www.ti.com.cn/lprfnewsletter 立即注册

7.4 商标

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Cortex is a registered trademark of ARM Limited.
ARM is a registered trademark of ARM Physical IP, Inc.
IAR Embedded Workbench is a registered trademark of IAR Systems AB.
ZigBee is a registered trademark of ZigBee Alliance.

7.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.6 出口管制提示

接收方同意：如果美国或其他适用法律限制或禁止将通过非披露义务的披露方获得的任何产品或技术数据（其中包括软件）（见美国、欧盟和其他出口管理条例之定义）、或者其他适用国家条例限制的任何受管制产品或此项技术的任何直接产品出口或再出口至任何目的地，那么在没有事先获得美国商务部和其他相关政府机构授权的情况下，接收方不得在知情的情况下，以直接或间接的方式将其出口。

7.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

8 机械、封装和可订购信息

8.1 封装信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC2538NF11RTQR	ACTIVE	QFN	RTQ	56	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	CC2538NF11	Samples
CC2538NF11RTQT	ACTIVE	QFN	RTQ	56	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	CC2538NF11	Samples
CC2538NF23RTQR	ACTIVE	QFN	RTQ	56	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	CC2538NF23	Samples
CC2538NF23RTQT	ACTIVE	QFN	RTQ	56	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	CC2538NF23	Samples
CC2538NF53RTQR	ACTIVE	QFN	RTQ	56	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	CC2538NF53	Samples
CC2538NF53RTQT	ACTIVE	QFN	RTQ	56	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	CC2538NF53	Samples
CC2538SF23RTQR	ACTIVE	QFN	RTQ	56	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	CC2538SF23	Samples
CC2538SF23RTQT	ACTIVE	QFN	RTQ	56	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	CC2538SF23	Samples
CC2538SF53RTQR	ACTIVE	QFN	RTQ	56	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	CC2538SF53	Samples
CC2538SF53RTQT	ACTIVE	QFN	RTQ	56	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	CC2538SF53	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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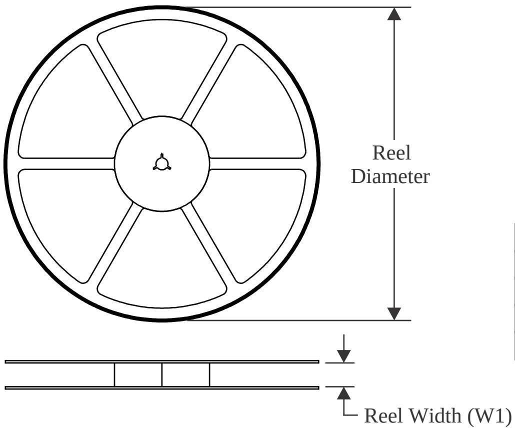
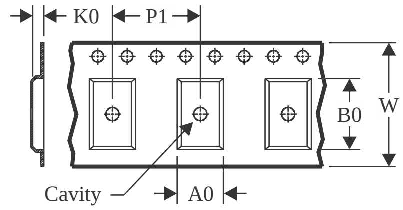
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

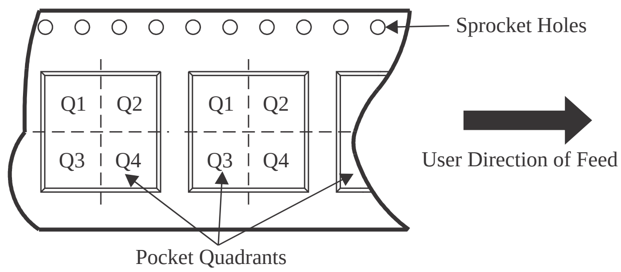


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

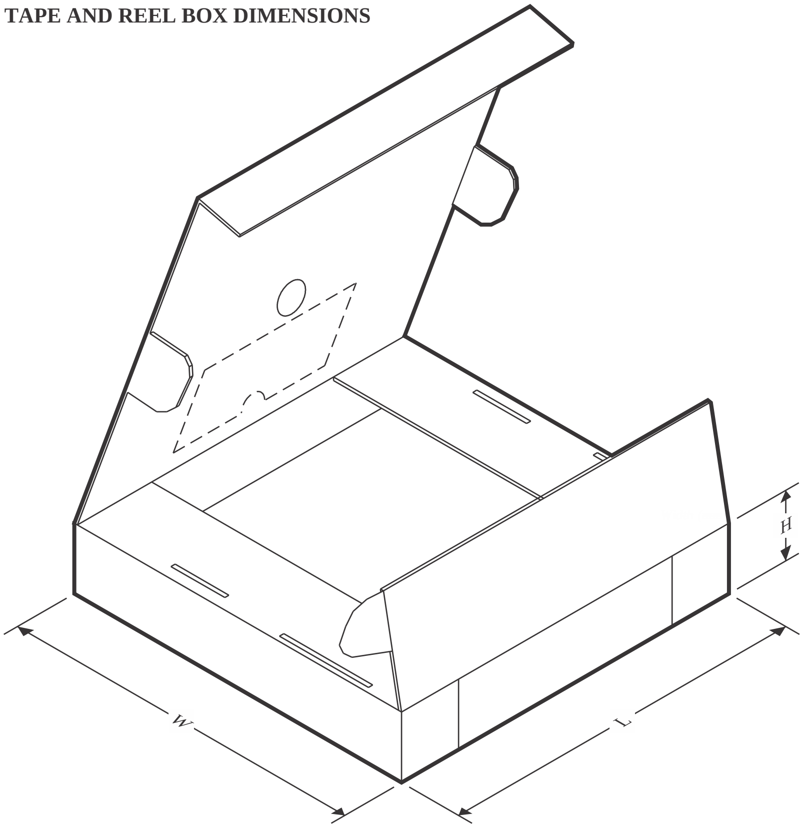
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC2538NF11RTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2
CC2538NF23RTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2
CC2538NF53RTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2
CC2538SF23RTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2
CC2538SF53RTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

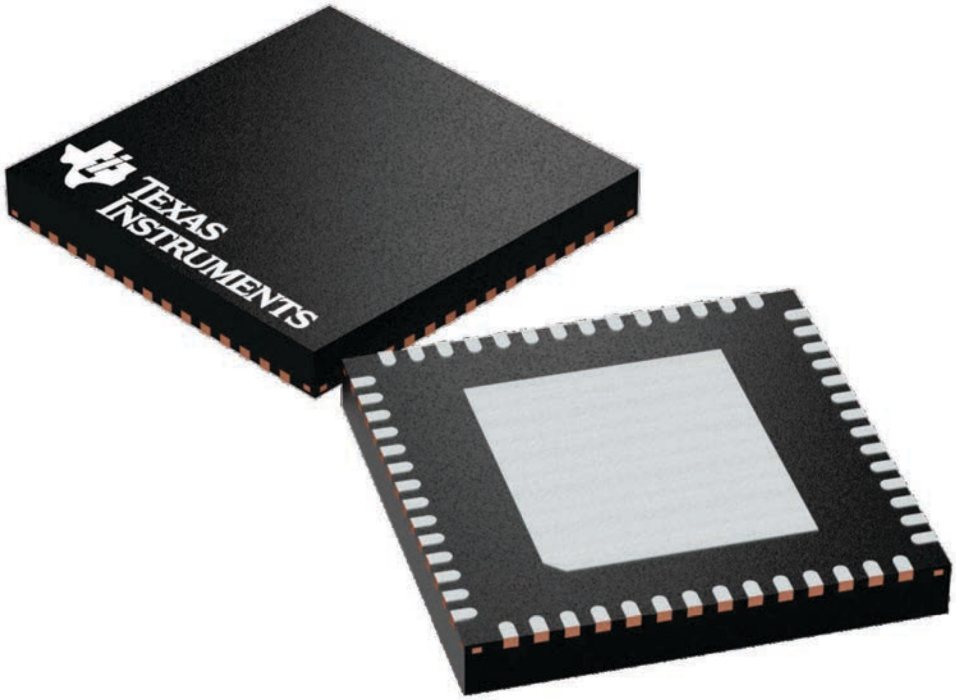
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC2538NF11RTQR	QFN	RTQ	56	2000	350.0	350.0	43.0
CC2538NF23RTQR	QFN	RTQ	56	2000	350.0	350.0	43.0
CC2538NF53RTQR	QFN	RTQ	56	2000	350.0	350.0	43.0
CC2538SF23RTQR	QFN	RTQ	56	2000	350.0	350.0	43.0
CC2538SF53RTQR	QFN	RTQ	56	2000	350.0	350.0	43.0

RTQ 56

VQFN - 1 mm max height

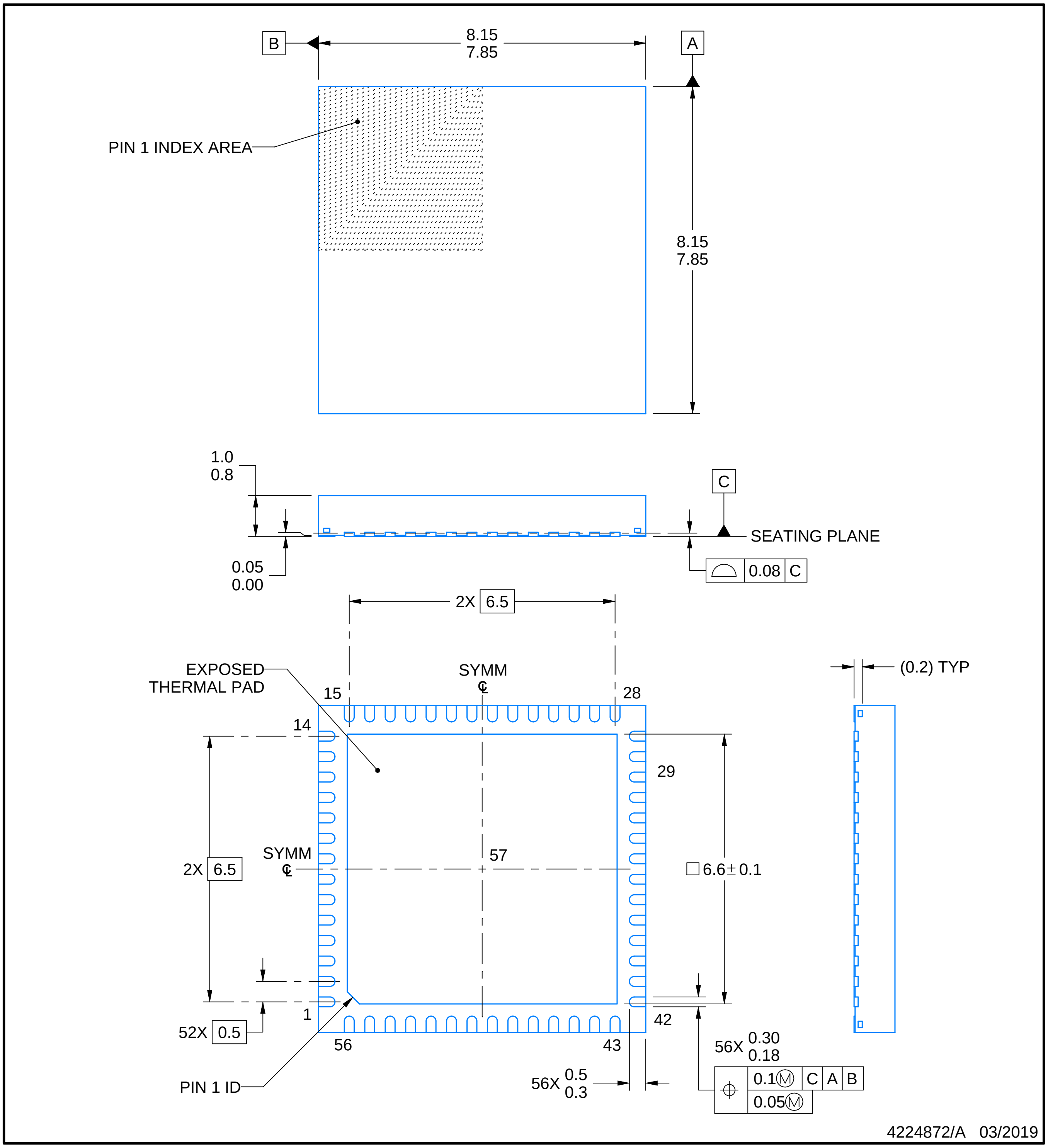
8 x 8, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



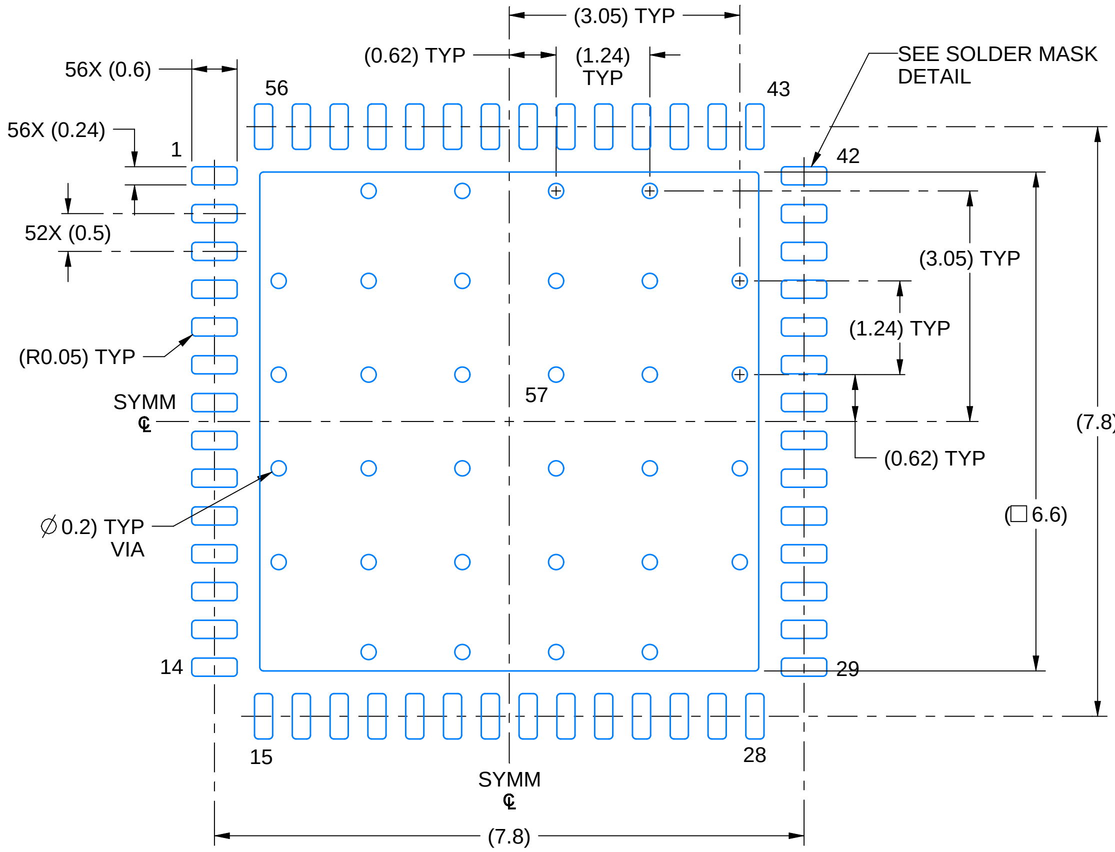
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224653/A

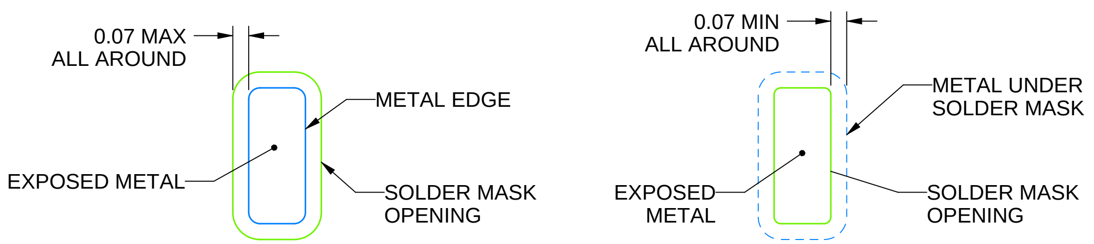


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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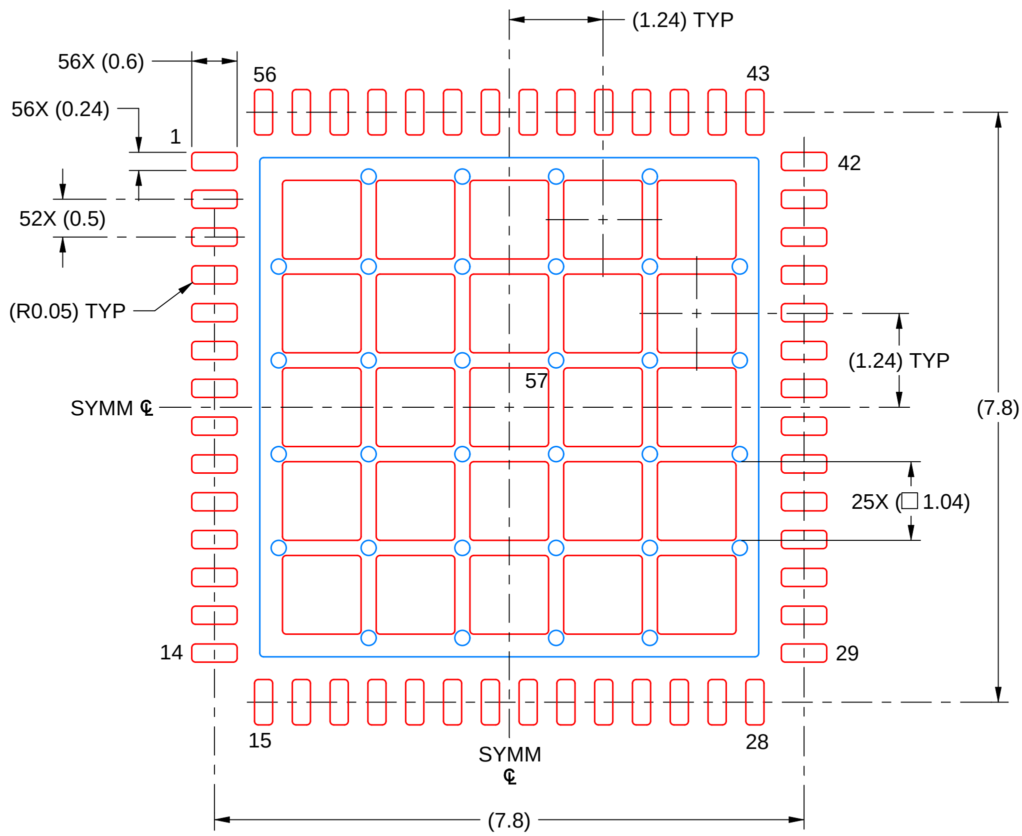
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 57
62% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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