CAB4A - DDR4 寄存器
32 位 1:2 命令/地址/控制缓冲器和 1:4 差分时钟缓冲器

查询样品: CAB4A

特性

- 符合 **DDR4RCD01 JEDEC** 标准
- **DDR4** 带寄存器的双列直插内存模块 **(RDIMM)** 和低负载双列直插内存模块 **(LRDIMM)** 高达 **DDR4-2400**
- **32** 位 **1** 至 **2** 寄存器输出
- **1** 至 **4** 差分时钟缓冲器
- **1.2V** 运行
- 具有内部反馈的锁相环 **(PLL)**
- 可配置驱动器强度
- 可扩展弱驱动器
- 可编程延迟
- 输出驱动器校准
- 地址映射和倒置
- **DDR4** 完全奇偶校验运行
- 片载可编程 V_{REF} 生成
- **CA** 总线协商模式
- I^2C™ 接口支持
- 多达 **16** 个用于支持三维堆叠 **(3DS) RDIMM** 和 **LRDIMM** 的逻辑模组
- 多达 **4** 个用于支持 **RDIMM** 和 **LRDIMM** 的物理模组

说明

CAB4 是一款 32 位 1:2 命令/地址/控制缓冲器和 1:4 差分时钟缓冲器，它被设计用于以 1.2V VDD 模式在 DDR4 带寄存器的 DIMM 上的运行。

所有输入是使用外部或内部电压基准的伪差分输入。所有输出是满摆幅 CMOS 驱动器，此驱动器针对驱动 DDR4 RDIMM，LRDIMM 和 3D 堆叠 DIMM 应用中的 15Ω 至 50Ω 有效端接迹线而进行了优化。 时钟输出、命令/地址输出、控制输出、数据缓冲控制输出可成组启用，并且可采用单独的驱动强度，以补偿不同的 DIMM 网状拓扑结构。 DDR4 寄存器以不同的时钟频率运行（CK_t 和 CK_c）。 输入在 CK_t 变为高电平和 CK_c 变为低电平交叉点时被记录。 如果输入信号 DSC[n:0]_n 中的一个被驱动为低电平，输入信号可被重新驱动至输出，或者它可在满足特定输入条件时被用来访问器件内部控制寄存器。

此器件的特点是可在 -40°C 至 95°C 的温度范围内运行。

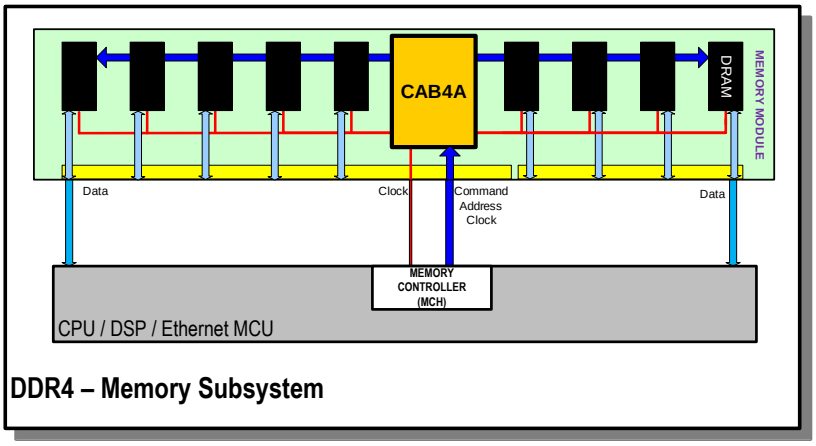


图 1. **DDR4 - RDIMM** 内存子系统

FUNCTIONAL BLOCK DIAGRAM

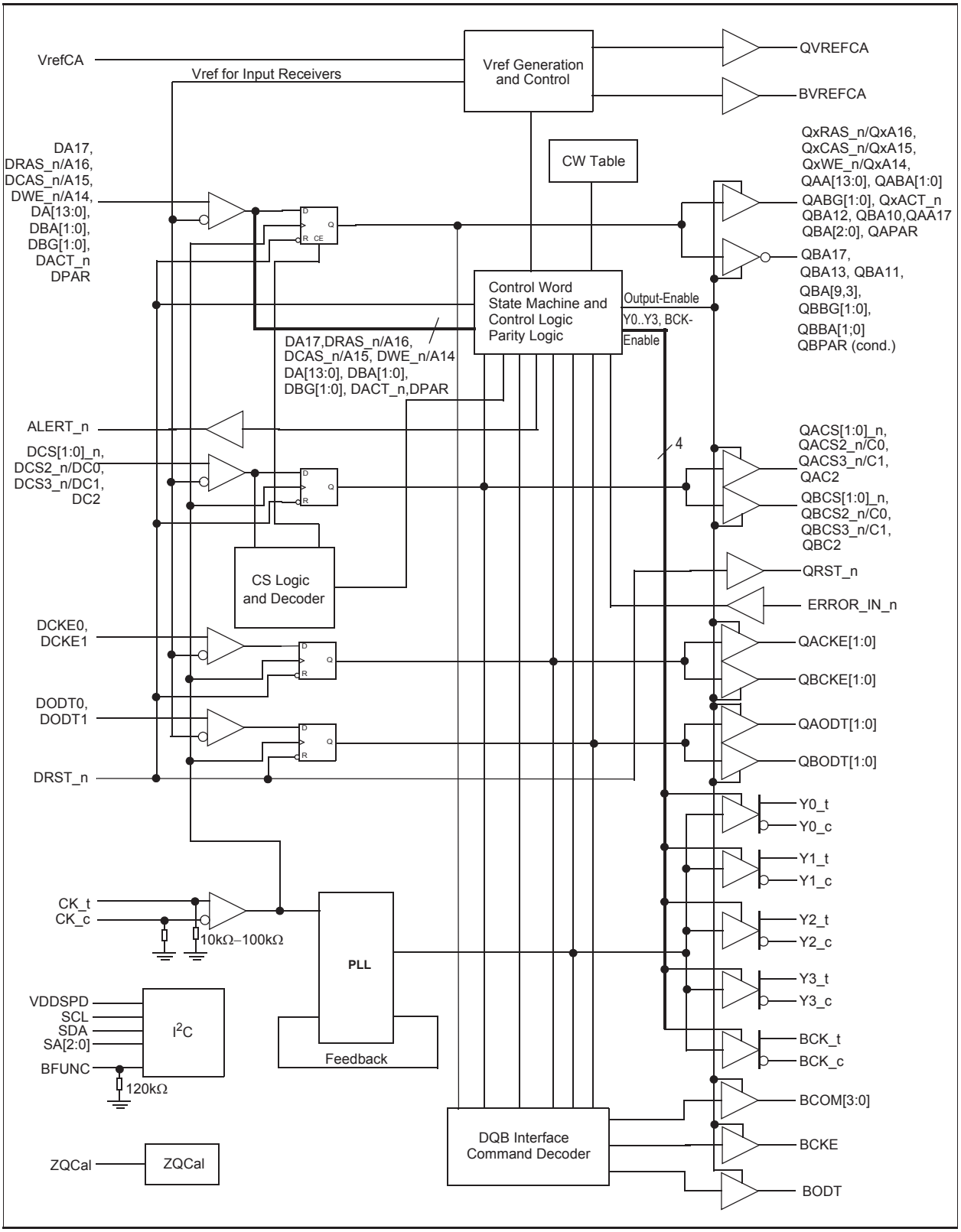


Table 1. TERMINAL FUNCTIONS

SIGNAL		TYPE	DESCRIPTION
GROUP	NAME		
Input Control bus	DCKE0/1 DODT0/1	CMOS(1) VREF based	DRAM corresponding register function pins not associated with Chip Select.
	DCS0_n..DCS1_n		DRAM corresponding register Chip Select signals.
	DCS2_n..DCS3_n or DC0..DC1		DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes, and as such exactly one will be LOW when a valid address/command is present which should be re-driven. Some of these have alternative functions: • DCS2_n ↔ DC0 • DCS3_n ↔ DC1
	DC2		DRAM corresponding register Chip ID 2 signal.
Input Address and Command bus	DA0..DA13, DA17 DBA0..DBA1, DBG0..DBG1	CMOS(1) VREF based	DRAM corresponding register inputs. In case of an ACT command some of these terminals have an alternative function: DRAM corresponding register command signals • DA14 ↔ DWE_n • DA15 ↔ DCAS_n • DA16 ↔ DRAS_n
	DA14..DA16 or DWE_n, DCAS_n, DRAS_n		
	DACT_n		DRAM corresponding register DACT_n signal.
Clock inputs	CK_t, CK_c	CMOS differential	Differential master clock input pair to the PLL with a 10 kΩ ~ 100 kΩ pull-down resistor.
Reset input	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.
Parity input	DPAR	CMOS(2) VREF based	Input parity is received on pin DPAR and should maintain even parity across the address and command inputs (see above), at the rising edge of the input clock.
Error Input	ERROR_IN_n	CMOS input	DRAM address parity and CRC Alert is connected to this input pin, which in turn is buffered and re-driven to the ALERT_n output of the register. Requires external pull-up resistor.(3)
Data buffer control and communication outputs	BODT	CMOS(3)	Data buffer on-die termination signal.
	BCKE		Data buffer clock enable signal for PLL power management.
	BCOM[3:0]		Register communication bus for data buffer programming and control access.
	BCK_t, BCK_c	CMOS differential	Differential clock output pair to the data buffer
	BVREFCA	VDD/2Reference Voltage	Output reference voltage for data buffer control bus receivers.

(1) These receivers use VREFCA as the switching point reference.
(2) These receivers use VREFCA as the switching point reference.
(3) CMOS: These outputs with rail to rail signal swing and programmable impedance are optimized for memory applications to drive DRAM inputs over a terminated transmission line.
Error_In_n: Internal Pull-up resistor can be turned on.

Table 1. TERMINAL FUNCTIONS (continued)

SIGNAL		TYPE	DESCRIPTION
GROUP	NAME		
Output Control Bus	QACKE0/1, QAODT0/1, QBCKE0/1, QBODT0/1	CMOS	Register output CKE and ODT signals.
	QACS0_n..QACS1_n, QBCS0_n..QBCS1_n		Register output Chip Select signals.
	QACS2_n..QACS3_n, QBCS2_n..QBCS3_n or QAC0..QAC1, QBC0..QBC1		Register output Chip Select signals. These pins initiate DRAM address/command decodes, and as such exactly one will be LOW when a valid address/command is present which should be re-driven. Some of these have alternative functions (Chip ID): • QxCS2_n ↔ QxC0 • QxCS2_n ↔ QxC0
	QAC2, QBC2		Register output Chip ID2 signals.
Output Address and Command bus	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAG0..QAG1, QBG0..QBG1		Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
	QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n		Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: • QxA14 ↔ QxWE_n • QxA15 ↔ QxCAS_n • QxA16 ↔ QxRAS_n
	QAACT-n, QBACT_n		Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Vref output	QVREFCA	VDD/2 Reference voltage	Output reference voltage for DRAM receivers
Clock outputs	Y0_t..Y3_t, Y0_c..Y3_c	CMOS differential	Re-driven clocks
Reset output	QRST_n	CMOS	Re-driven reset. This is not an asynchronous output.
Parity outputs	QAPAR, QBPAR		Re-driven parity(4)
Error out	ALERT_n	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs when parity checking is enabled or that the ERROR_IN_n input was asserted, regardless of whether parity checking is enabled or not.
I^2C pins	SDA SCL SA[2:0] BFUNC VDDSPD	Open drain I/O CMOS input CMOS input CMOS input Power input	I^2C Data I^2C Clock I^2C Address signals Reserved(5) I^2C power input

(4) I^2C inputs: These inputs are 2.5V inputs, except BFUNC which is a 1.2V input.
(5) BFUNC has an internal pull-down resistor of 120 kΩ to V.

Table 1. TERMINAL FUNCTIONS (continued)

SIGNAL		TYPE	DESCRIPTION
GROUP	NAME		
Miscellaneous pins	VREFCA	VCC/2Reference voltage	Input reference voltage for the CMOS inputs.
	VDD	Power input	Power supply voltage
	VSS	Ground input	Ground
	AVDD	Analog power	Analog supply voltage
	PVDD	Clock power	Clock logic and clock output driver power supply.
	PVSS	Clock ground	Clock logic and clock output driver ground.
	ZQCAL	Reference	Needs a calibration resistor of 240Ω ±1% to VSS.
	NU	Mechanical ball	Do not connect on PCB.
	RFU[3:0]	I/O	Reserved; must be left floating on DIMM and in DDR4 register.

修订历史记录

将文档更改为生产数据。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CAB4AZNRR	LIFEBUY	NFBGA	ZNR	253	2000	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 95	CAB4A6	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

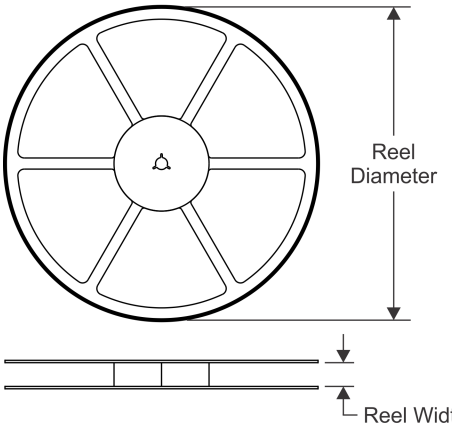
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

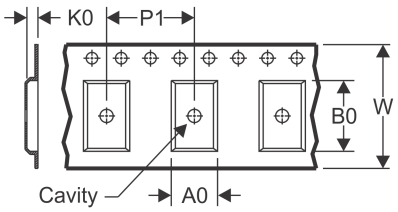
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

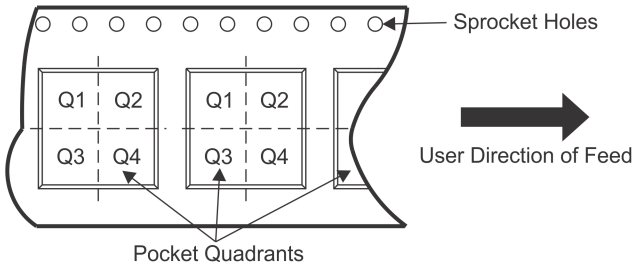


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

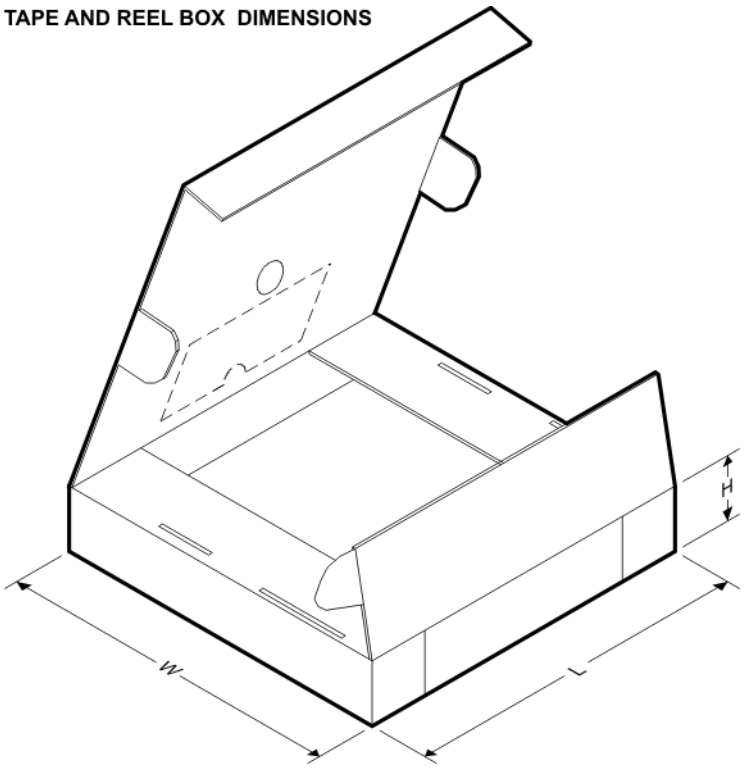
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CAB4AZNRR	NFBGA	ZNR	253	2000	330.0	24.4	8.3	13.8	1.8	12.0	24.0	Q1

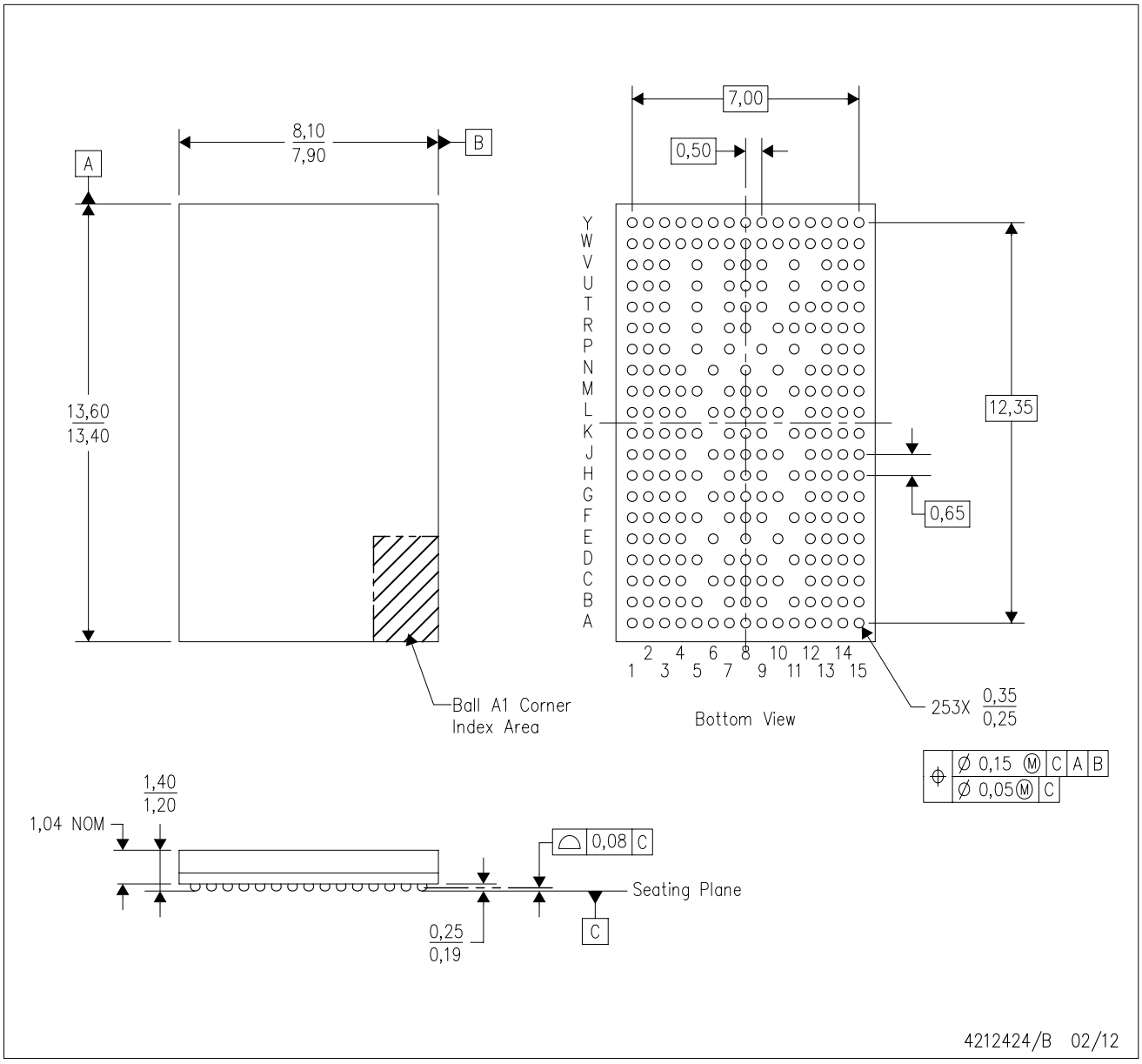
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CAB4AZNRR	NFBGA	ZNR	253	2000	367.0	367.0	38.0

ZNR (R–PBGA–N253) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This package is Pb–free.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265