bq24314C 过压和过流保护 IC 以及锂离子电池充电器前端保护 IC

1 特性

- 针对三个变量提供保护：
  - 输入过压，快速响应时间小于 1µs
  - 带有电流限制的用户可编程过流
  - 电池过压
- 最大输入电压为 30V
- 支持高达 1.5A 的输入电流
- 防止由电流瞬变造成的错误触发
- 过热保护
- 使能输入
- 状态指示
- 采用节省空间的小型 8 引线 2 × 2 WSON 封装

2 应用

- 手机和智能电话
- 掌上电脑 (PDA)
- MP3 播放器
- 低功耗手持器件
- Bluetooth™耳机

3 说明

bq24314C 器件是一款高度集成电路 (IC)，旨在保护锂离子电池免受充电电路故障的影响。该器件可连续监控输入电压、输入电流和电池电压。一旦发生输入过压情况，该器件会关闭内部开关，从而立即将充电电路断电。在发生过流时，它会将系统电流限制在阈值内，而如果过流持续存在，则在一个消隐期后关闭通道元件。此外，该器件还会监控自身的裸片温度，并在温度超过 140°C 时进行关闭。用户可对输入过流阈值进行编程。

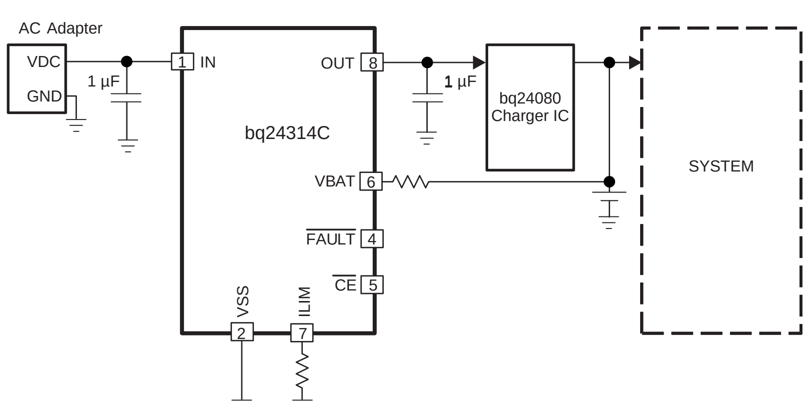
该器件可由处理器进行控制，并且可向主机提供关于故障状况的状态信息。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
bq24314C	WSON (8)	2.00mm x 2.00mm

(1) 要了解所有可用封装，请参阅数据表末尾的可订购产品附录。

图 **1.** 简化原理图



目录

4 修订历史记录

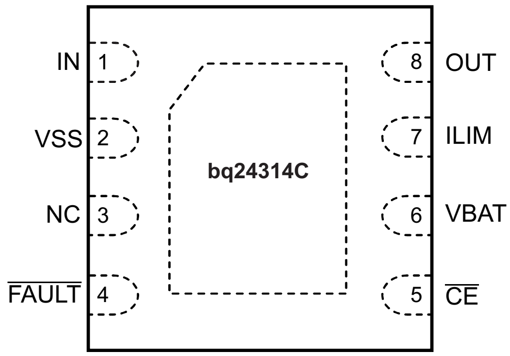
注：之前版本的页码可能与当前版本有所不同。

Changes from Original (August 2012) to Revision A **Page**

- 已添加 *ESD 额定值表，特性 说明部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分* ... 1
- 已更改 将整个文档中的 SON 更改为 WSON ... 1
- Changed R_{ILIM} from 25k to 24.9k throughout document ... 5
- Changed AΩ to AkΩ ... 5
- Moved Figures 2 through 11 from *Typical Characteristics* to *Application Curves* section ... 6

5 Pin Configuration and Functions

DSG Package
8-Pin WSON With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{CE}}$	5	I	Chip enable input. Active low. When $\overline{\text{CE}}$ = High, the input FET is off. Internally pulled down.
$\overline{\text{FAULT}}$	4	O	Open-drain output, device status. $\overline{\text{FAULT}}$ = Low indicates that the input FET Q1 has been turned off due to input overvoltage, input overcurrent, battery overvoltage, or thermal shutdown.
ILIM	7	I/O	Input overcurrent threshold programming. Connect a resistor to VSS to set the overcurrent threshold.
IN	1	I	Input power, connect to external DC supply. Connect external 1 μF ceramic capacitor (minimum) to V_{SS}.
NC	3	—	These pins may have internal circuits used for test purposes. Do not make any external connections at these pins for normal operation.
OUT	8	O	Output terminal to the charging system. Connect external 1 μF ceramic capacitor (minimum) to V_{SS}.
VBAT	6	I	Battery voltage sense input. Connect to pack positive terminal through a resistor.
VSS	2	—	Ground terminal
Thermal PAD		—	There is an internal electrical connection between the exposed thermal pad and the V_{SS} pin of the device. The thermal pad must be connected to the same potential as the V_{SS} pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. The VSS pin must be connected to ground at all times.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_I	Input voltage	IN (with respect to VSS)	–0.3	30	V
		OUT (with respect to VSS)	–0.3	12	
		ILIM, $\overline{\text{FAULT}}$, $\overline{\text{CE}}$, VBAT (with respect to VSS)	–0.3	7	
I_I	Input current	IN		2	A
I_O	Output current	OUT		2	A
	Output sink current	$\overline{\text{FAULT}}$		15	mA
T_J	Junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±500	
		IN(IEC 61000-4-2)(3)	Air Discharge	±15000	
			Contact	±8000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) With IN bypassed to the VSS with a 1-µF low-ESR ceramic capacitor

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	3		30	V
I_{IN}	Input current, IN pin			1.5	A
I_{OUT}	Output current, OUT pin			1.5	A
R_{ILIM}	OCP Programming resistor	15		90	kΩ
T_J	Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		bq24314C DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range –40°C to +125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IN						
UVLO	Undervoltage lock-out, input power detected threshold	$\overline{CE}$ = Low, V_{IN} increasing from 0 V to 3 V	2.6	2.7	2.8	V
$V_{hys(UVLO)}$	Hysteresis on UVLO	$\overline{CE}$ = Low, V_{IN} decreasing from 3 V to 0 V	200	260	300	mV
$T_{DGL(PGOOD)}$	Deglitch time, input power detected status	$\overline{CE}$ = Low. Time measured from V_{IN} 0 V → 5 V 1 μs rise-time, to output turning ON		8		ms
I_{DD}	Operating current	$\overline{CE}$ = Low, No load on OUT pin, V_{IN} = 5 V, R_{ILIM} = 24.9 kΩ		400	600	μA
I_{STDBY}	Standby current	$\overline{CE}$ = High, V_{IN} = 5 V		65	95	μA
INPUT TO OUTPUT CHARACTERISTICS						
VDO	Drop-out voltage IN to OUT	$\overline{CE}$ = Low, V_{IN} = 5 V, I_{OUT} = 1 A		170	280	mV
INPUT OVERVOLTAGE PROTECTION						
V_{OVP}	Input overvoltage protection threshold	$\overline{CE}$ = Low, V_{IN} increasing from 5 V to 7.5 V	5.71	5.85	6.00	V
$t_{PD(OVP)}$	Input OV propagation delay(1)	$\overline{CE}$ = Low		200		ns
$V_{hys(OVP)}$	Hysteresis on OVP	$\overline{CE}$ = Low, V_{IN} decreasing from 7.5 V to 5 V	20	60	110	mV
$t_{ON(OVP)}$	Recovery time from input overvoltage condition	$\overline{CE}$ = Low, Time measured from V_{IN} 7.5 V → 5 V, 1 μs fall-time		8		ms
INPUT OVERCURRENT PROTECTION						
I_{OCP}	Input overcurrent protection threshold range		300		1500	mA
I_{OCP}	Input overcurrent protection threshold	$\overline{CE}$ = Low, R_{ILIM} = 24.9 kΩ, 3 V ≤ V_{IN} < V_{OVP} -$V_{hys(OVP)}$	900	1000	1100	mA
K_{ILIM}	Programmable current limit factor			25		AkΩ
$t_{BLANK(OCP)}$	Blanking time, input overcurrent detected			176		μs
$t_{REC(OCP)}$	Recovery time from input overcurrent condition			64		ms
BATTERY OVERVOLTAGE PROTECTION						
BV_{OVP}	Battery overvoltage protection threshold	$\overline{CE}$ = Low, V_{IN} > 4.4 V	4.4	4.45	4.5	V
$V_{hys(Bovp)}$	Hysteresis on BV_{OVP}	$\overline{CE}$ = Low, V_{IN} > 4.4 V	200	280	350	mV
I_{VBAT}	Input bias current on VBAT pin	V_{BAT} = 4.4 V, T_J = 25°C			10	nA
$T_{DGL(Bovp)}$	Deglitch time, battery overvoltage detected	$\overline{CE}$ = Low, V_{IN} > 4.4 V. Time measured from V_{VBAT} rising from 4.1 V to 4.4 V to $\overline{FAULT}$ going low.		176		μs
THERMAL PROTECTION						
$T_{J(OFF)}$	Thermal shutdown temperature			140	150	°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis			20		°C
LOGIC LEVELS ON $\overline{CE}$						
V_{IL}	Low-level input voltage		0		0.4	V
V_{IH}	High-level input voltage		1.4			V
I_{IL}	Low-level input current	V_{CE} = 0 V			1	μA
I_{IH}	High-level input current	V_{CE} = 1.8 V			15	μA
LOGIC LEVELS ON $\overline{FAULT}$						
V_{OL}	Output low voltage	I_{SINK} = 5 mA			0.2	V
I_{HI-Z}	Leakage current, $\overline{FAULT}$ pin HI-Z	V_{FAULT} = 5 V			10	μA

(1) Not tested in production. Specified by design.

6.6 Typical Characteristics

Test conditions (unless otherwise noted) for typical operating performance: V_{IN} = 5 V, C_{IN} = 1 μF, C_{OUT} = 1 μF, R_{ILIM} = 24.9 kΩ, R_{BAT} = 100 kΩ, T_A = 25°C, V_{PU} = 3.3 V (see Figure 13 for the *Typical Application Circuit*)

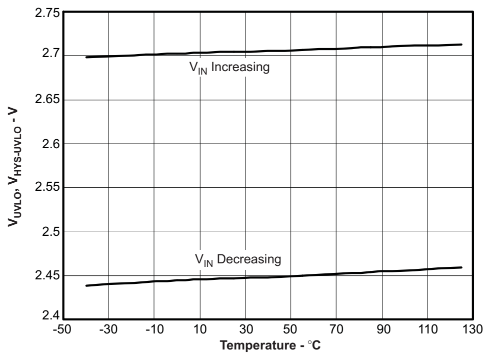


Figure 2. Undervoltage Lockout vs Free-Air Temperature

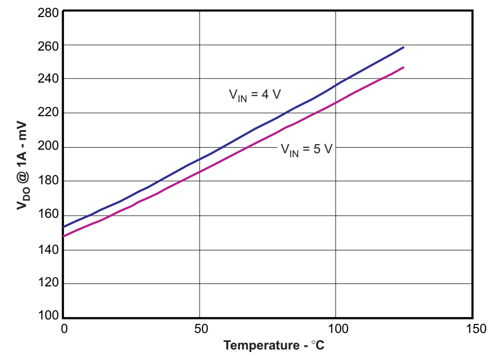


Figure 3. Dropout Voltage (IN to OUT) vs Free-Air Temperature

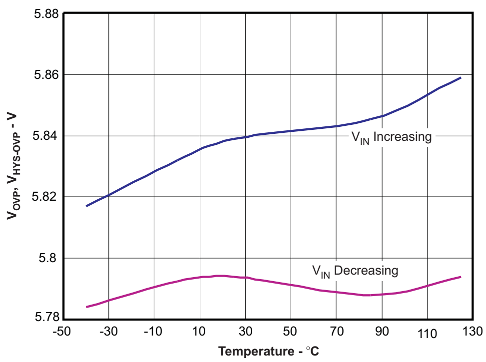


Figure 4. Overvoltage Threshold Protection vs Free-Air Temperature

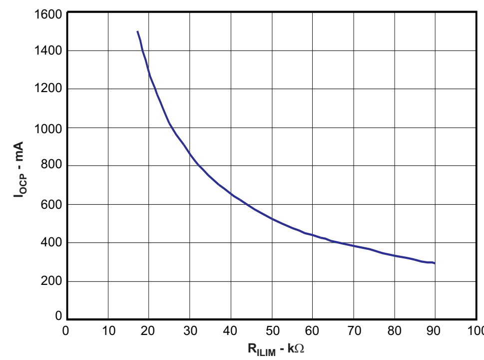


Figure 5. Input Overcurrent Protection vs ILIM Resistance

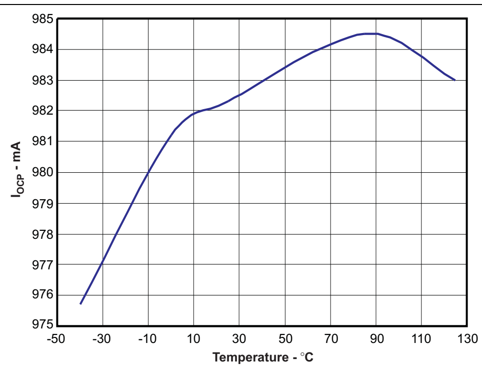


Figure 6. Input Overcurrent Protection vs Free-Air Temperature

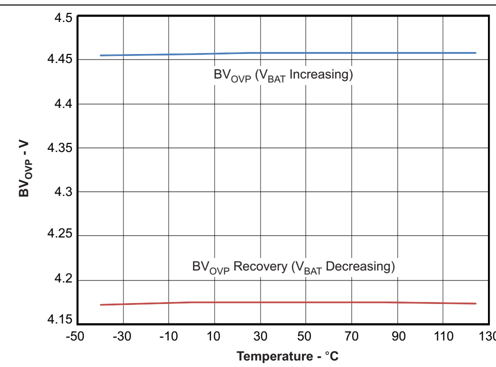


Figure 7. Battery Overvoltage Protection vs Free-Air Temperature

Typical Characteristics (continued)

Test conditions (unless otherwise noted) for typical operating performance: V_{IN} = 5 V, C_{IN} = 1 µF, C_{OUT} = 1 µF, R_{ILIM} = 24.9 kΩ, R_{BAT} = 100 kΩ, T_A = 25°C, V_{PU} = 3.3 V (see Figure 13 for the *Typical Application Circuit*)

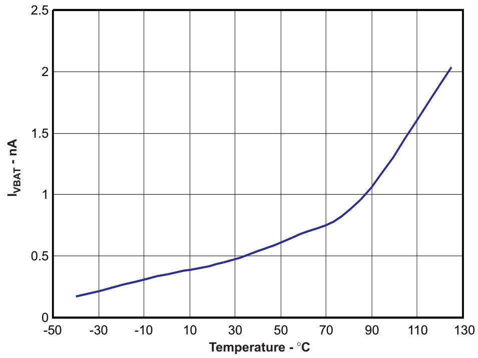


Figure 8. Leakage Current (VBAT Pin) vs Free-Air Temperature

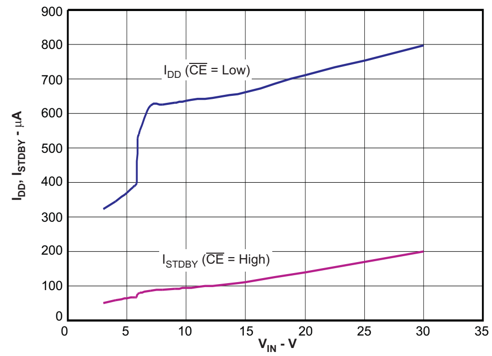


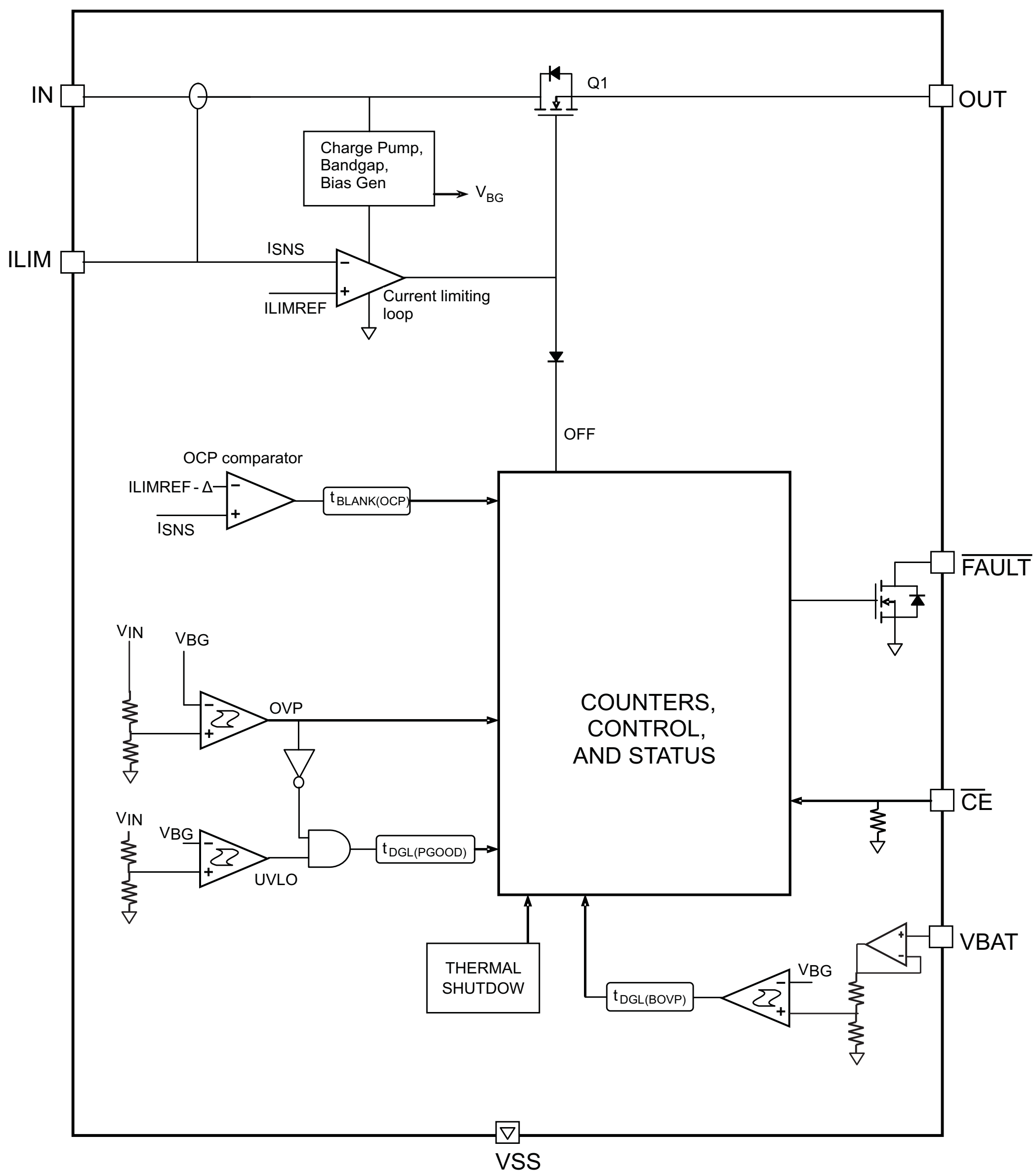
Figure 9. Supply Current vs INPUT Voltage

7 Detailed Description

7.1 Overview

The bq24314C device is a highly integrated circuit designed to provide protection to Li-ion batteries from failures of the charging circuit. The device continuously monitors the input voltage, the input current, and the battery voltage. In case of an input overvoltage condition, the device immediately removes power from the charging circuit by turning off an internal switch. In the case of an overcurrent condition, it limits the system current at the threshold value, and if the overcurrent persists, switches the pass element OFF after a blanking period. If the battery voltage rises to an unsafe level, the device disconnects power from the charging circuit until the battery voltage returns to an acceptable value. Additionally, the device also monitors its own die temperature and switches off if it exceeds 140°C. The input overcurrent threshold is user-programmable. The device can be controlled by a processor and also provides status information about fault conditions to the host.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Overvoltage Protection

The bq24314C device integrates an input overvoltage protection feature to protect downstream devices from faulty input sources. If the input voltage rises above V_{OVP}, the internal FET Q1 is turned off, removing power from the circuit. As shown in Figure 16 to Figure 17, the response is very rapid, with the FET turning off in less than a microsecond. The $\overline{FAULT}$ pin is driven low. When the input voltage returns below $V_{OVP} - V_{hys(OVP)}$ (but is still above UVLO), the FET Q1 is turned on again after a deglitch time of $t_{ON(OVP)}$ to ensure that the input supply has stabilized. Figure 18 shows the recovery from input OVP.

7.3.2 Input Overcurrent Protection

The overcurrent threshold is programmed by a resistor R_{ILIM} connected from the ILIM pin to VSS. Figure 5 shows the OCP threshold as a function of R_{ILIM}, and may be approximated by the following equation:

$I_{OCP} = 25 \div R_{ILIM}$ (current in A, resistance in kΩ),

where

- R_{ILIM} must be between 15 kΩ and 90 kΩ (1)

If the load current tries to exceed the I_{OCP} threshold, the device limits the current for a blanking duration of $t_{BLANK(OCP)}$. If the load current returns to less than I_{OCP} before $t_{BLANK(OCP)}$ times out, the device continues to operate. However, if the overcurrent situation persists for $t_{BLANK(OCP)}$, the FET Q1 is turned off for a duration of $t_{REC(OCP)}$, and the $\overline{FAULT}$ pin is driven low. The FET is then turned on again after $t_{REC(OCP)}$ and the current is monitored all over again. Each time an OCP fault occurs, an internal counter is incremented. If 15 OCP faults occur in one charge cycle, the FET is turned off permanently. The counter is cleared either by removing and re-applying input power, or by disabling and re-enabling the device with the $\overline{CE}$ pin. Figure 19 to Figure 21 show what happens in an overcurrent fault.

To prevent the input voltage from spiking up due to the inductance of the input cable, Q1 is turned off slowly, resulting in a *soft-stop*, as shown in Figure 21.

7.3.3 Battery Overvoltage Protection

The battery overvoltage threshold BV_{OVP} is internally set to 4.45 V. If the battery voltage exceeds the BV_{OVP} threshold, the FET Q1 is turned off, and the $\overline{FAULT}$ pin is driven low. The FET is turned back on once the battery voltage drops to $BV_{OVP} - V_{hys(Bovp)}$ (see Figure 22 and Figure 23). Each time a battery overvoltage fault occurs, an internal counter is incremented. If 15 such faults occur in one charge cycle, the FET is turned off permanently. The counter is cleared either by removing and re-applying input power, or by disabling and re-enabling the device with the $\overline{CE}$ pin. In the case of a battery overvoltage fault, Q1 is switched OFF gradually (see Figure 22).

7.3.4 Thermal Protection

If the junction temperature of the device exceeds $T_{J(OFF)}$, the FET Q1 is turned off, and the $\overline{FAULT}$ pin is driven low. The FET is turned back on when the junction temperature falls below $T_{J(OFF)} - T_{J(OFF\text{-}HYS)}$.

7.3.5 Enable Function

The IC has an enable pin, which can be used to enable or disable the device. When the $\overline{CE}$ pin is driven high, the internal FET is turned off. When the $\overline{CE}$ pin is low, the FET is turned on if other conditions are safe. The OCP counter and the Bat-OVP counter are both reset when the device is disabled and re-enabled. The $\overline{CE}$ pin has an internal pulldown resistor and can be left floating. Note that the $\overline{FAULT}$ pin functionality is also disabled when the $\overline{CE}$ pin is high.

7.3.6 Fault Indication

The $\overline{FAULT}$ pin is an active-low open-drain output. It is in a high-impedance state when operating conditions are safe, or when the device is disabled by setting $\overline{CE}$ high. With $\overline{CE}$ low, the $\overline{FAULT}$ pin goes low whenever any of these events occurs:

- Input overvoltage
- Input overcurrent
- Battery overvoltage
- IC overtemperature

7.4 Device Functional Modes

7.4.1 OPERATION Mode

The device continuously monitors the input voltage, the input current, and the battery voltage. As long as the input voltage is less than VOVP, the output voltage tracks the input voltage (less the drop caused by RDSON of Q1). During fault conditions, the internal FET is turned off and the output is isolated from the input source.

7.4.2 POWER-DOWN Mode

The device remains in POWER-DOWN mode when the input voltage at the IN pin is below the undervoltage threshold UVLO. The FET Q1 connected between IN and OUT pins is off, and the status output, $\overline{\text{FAULT}}$, is set to Hi-Z. See Figure 10.

7.4.3 POWER-ON RESET Mode

The device resets when the input voltage at the IN pin exceeds the UVLO threshold. All internal counters and other circuit blocks are reset. The IC then waits for duration $t_{DGL(PGOOD)}$ for the input voltage to stabilize. If, after $t_{DGL(PGOOD)}$, the input voltage and battery voltage are safe, FET Q1 is turned ON. The device has a soft-start feature to control the inrush current. The soft-start minimizes the ringing at the input (the ringing occurs because the parasitic inductance of the adapter cable and the input bypass capacitor form a resonant circuit). Figure 14 shows the power-up behavior of the device. Because of the deglitch time at power-on, if the input voltage rises rapidly to beyond the OVP threshold, the device will not switch on at all, instead it will go into protection mode and indicate a fault on the $\overline{\text{FAULT}}$ pin, as shown in Figure 15.

Device Functional Modes (continued)

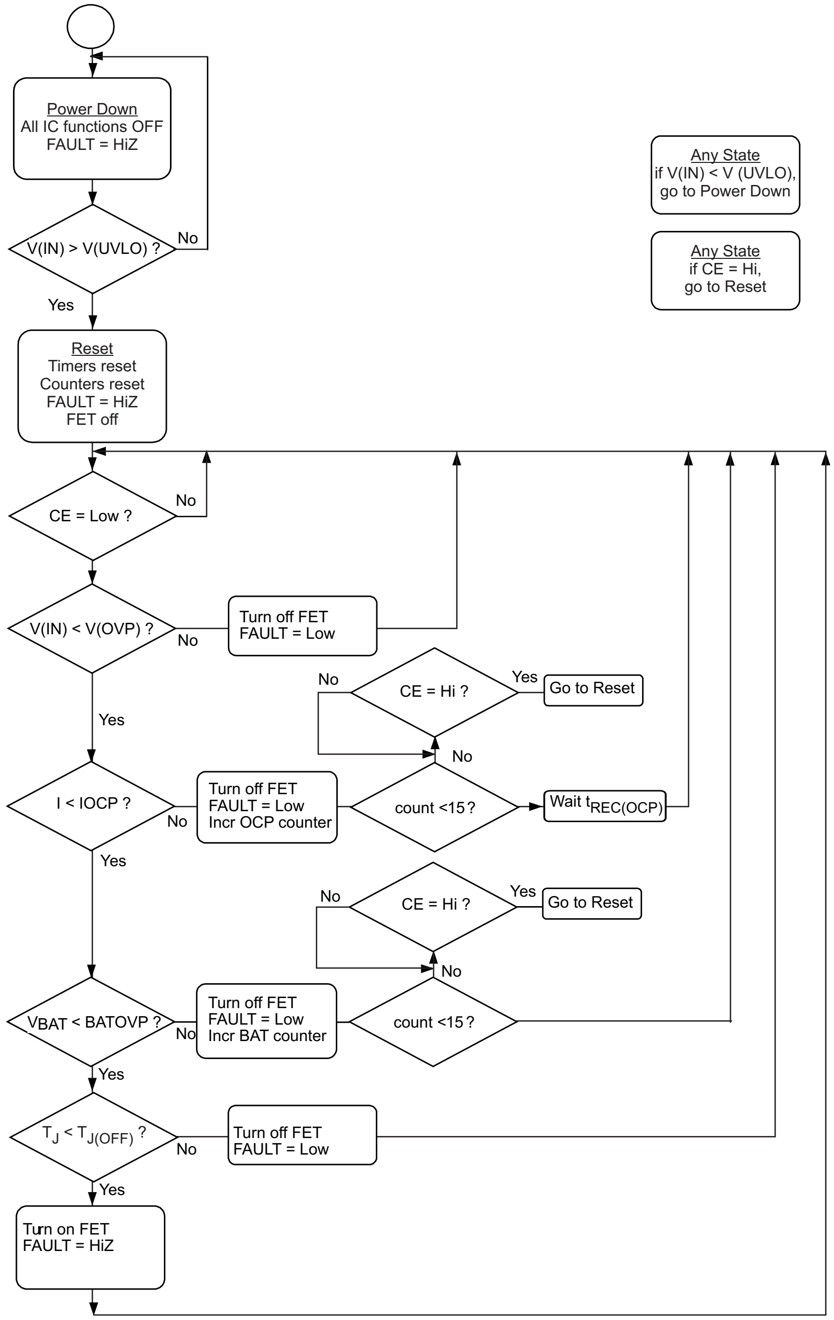


Figure 10. Flow Diagram

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The bq24314C device protects against overvoltage, overcurrent, and battery overvoltage events that occur due to a faulty adapter or other input sources. If any of these faults occur, the bq24314C device isolates the downstream devices from the input source and alerts the host controller with the FAULT open-drain output.

8.1.1 Powering Accessories

In some applications, the equipment that the protection IC resides in may be required to provide power to an accessory (for example, a cellphone may power a headset or an external memory card) through the same connector pins that are used by the adapter for charging. Figure 11 and Figure 12 illustrate typical charging and accessory-powering scenarios:

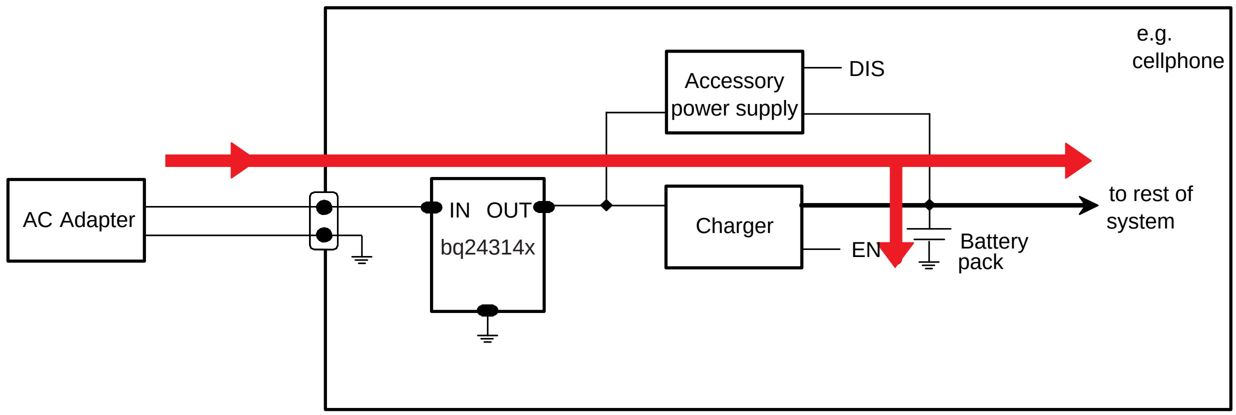


Figure 11. Charging - The Red Arrows Show the Direction of Current Flow

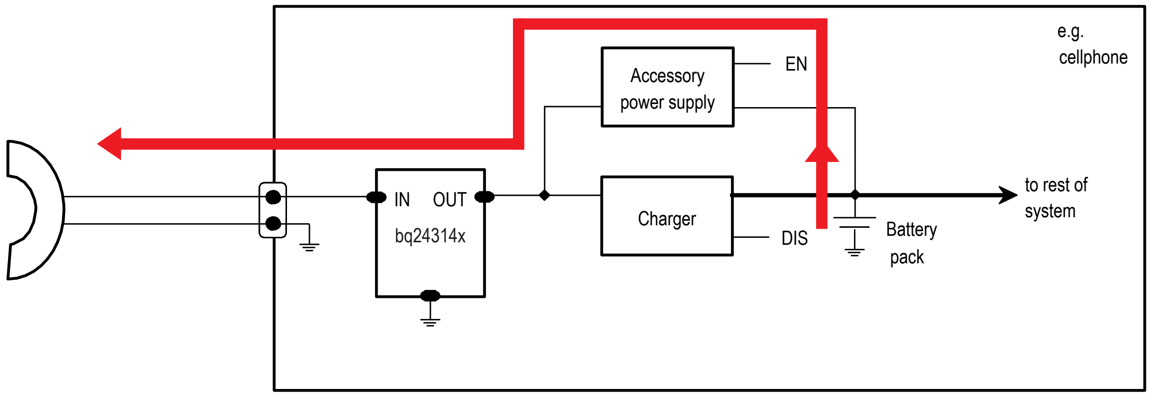


Figure 12. Powering an Accessory - The Red Arrows Show the Direction of Current Flow

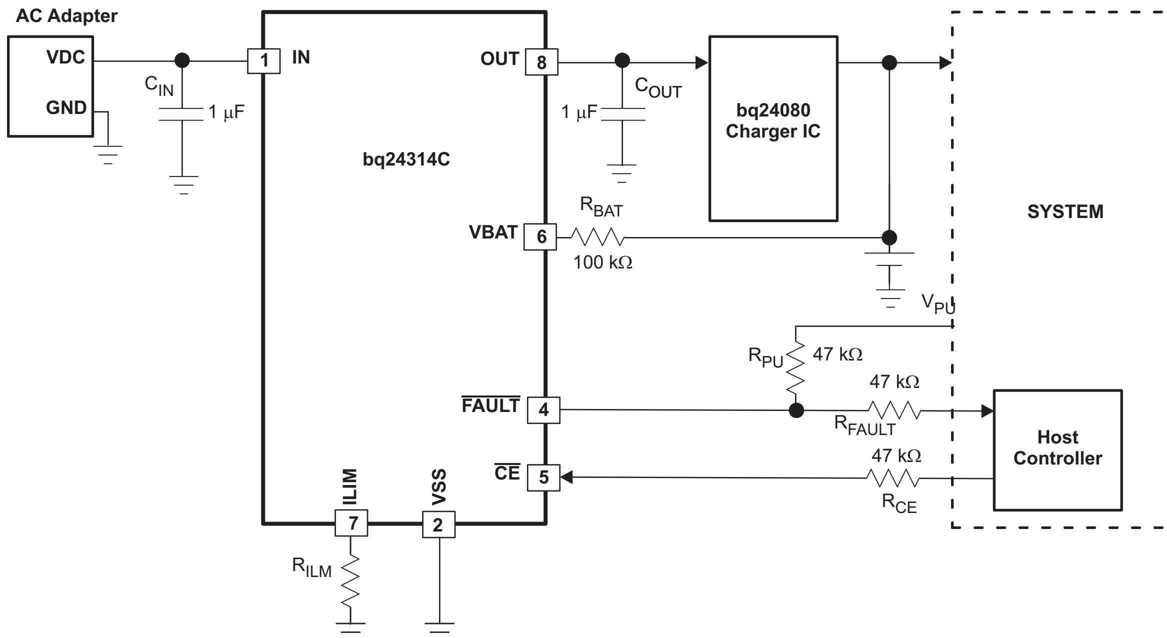
In the second case, when power is being delivered to an accessory, the bq24314C device is required to support current flow from the OUT pin to the IN pin.

Application Information (continued)

If V_{OUT} > UVLO + 0.7 V, FET Q1 is turned on, and the reverse current does not flow through the diode but through Q1. Q1 will then remain ON as long as V_{OUT} > UVLO – $V_{hys(UVLO)}$ + $R_{DS(on)}$ × $I_{ACCESSORY}$. Within this voltage range, the reverse current capability is the same as the forward capability, 1.5 A. It should be noted that there is no overcurrent protection in this direction.

8.2 Typical Application

The typical values for an application are V_{OVP} = 6.8 V, I_{OCP} = 1000 mA, BV_{OVP} = 4.45 V



Terminal numbers shown are for the 2 × 2 DSG package.

Figure 13. Typical Application Circuit

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Supply Voltage	5 V
INILIM	1 A

8.2.2 Detailed Design Procedure

8.2.2.1 Selection of R_{BAT}

It is strongly recommended that the battery not be tied directly to the VBAT pin of the device, as under some failure modes of the IC, the voltage at the IN pin may appear on the VBAT pin. This voltage can be as high as 30 V, and applying 30 V to the battery in case of the failure of the bq24314C device can be hazardous. Connecting the VBAT pin through R_{BAT} prevents a large current from flowing into the battery in case of a failure of the device. In the interests of safety, R_{BAT} should have a very high value. The problem with a large R_{BAT} is that the voltage drop across this resistor because of the VBAT bias current I_{VBAT} causes an error in the BV_{OVP} threshold. This error is over and above the tolerance on the nominal 4.45 V BV_{OVP} threshold.

Choosing R_{BAT} in the range 100 kΩ to 470 kΩ is a good compromise. In the case of an device failure, with R_{BAT} equal to 100 kΩ, the maximum current flowing into the battery would be (30 V – 3 V) ÷ 100 kΩ = 246 µA, which is low enough to be absorbed by the bias currents of the system components. R_{BAT} equal to 100 kΩ would result in a worst-case voltage drop of $R_{BAT} \times I_{VBAT}$ = 1 mV. This is negligible to compared to the internal tolerance of 50 mV on BV_{OVP} threshold.

If the Bat-OVP function is not required, the VBAT pin should be connected to VSS.

8.2.2.2 Selection of R_{CE}, R_{FAULT}, and R_{PU}

The $\overline{CE}$ pin can be used to enable and disable the IC. If host control is not required, the $\overline{CE}$ pin can be tied to ground or left un-connected, permanently enabling the device.

In applications where external control is required, the $\overline{CE}$ pin can be controlled by a host processor. As in the case of the VBAT pin (see above), the $\overline{CE}$ pin should be connected to the host GPIO pin through as large a resistor as possible. The limitation on the resistor value is that the minimum V_{OH} of the host GPIO pin less the drop across the resistor should be greater than V_{IH} of the bq24314C device's $\overline{CE}$ pin. The drop across the resistor is given by $R_{CE} \times I_{IH}$.

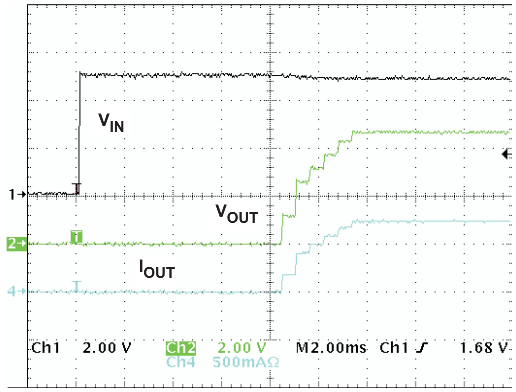
The $\overline{FAULT}$ pin is an open-drain output that goes low during OV, OC, battery-OV, and OT events. If the application does not require monitoring of the $\overline{FAULT}$ pin, it can be left unconnected. But if the $\overline{FAULT}$ pin has to be monitored, it should be pulled high externally through R_{PU}, and connected to the host through R_{FAULT}. R_{FAULT} prevents damage to the host controller if the bq24314C device fails (see above). The resistors should be of high value, in practice values between 22 kΩ and 100 kΩ should be sufficient.

8.2.2.3 Selection of Input and Output Bypass Capacitors

The input capacitor C_{IN} in Figure 13 is for decoupling, and serves an important purpose. Whenever there is a step change downwards in the system load current, the inductance of the input cable causes the input voltage to spike up. C_{IN} prevents the input voltage from overshooting to dangerous levels. It is strongly recommended that a ceramic capacitor of at least 1 µF be used at the input of the device. It should be located in close proximity to the IN pin.

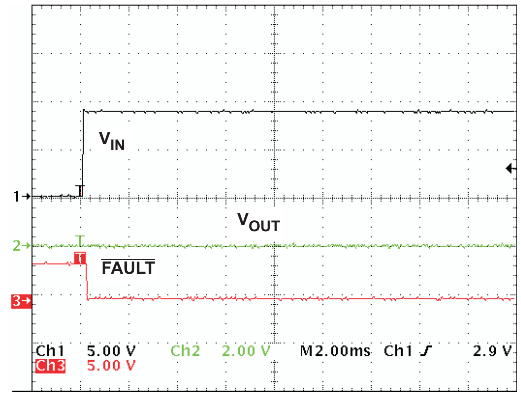
C_{OUT} in Figure 13 is also important: If a very fast (< 1 µs rise time) overvoltage transient occurs at the input, the current that charges C_{OUT} causes the device's current-limiting loop to kick in, reducing the gate-drive to FET Q1. This results in improved performance for input overvoltage protection. C_{OUT} should also be a ceramic capacitor of at least 1 µF, located close to the OUT pin. C_{OUT} also serves as the input decoupling capacitor for the charging circuit downstream of the protection IC.

8.2.3 Application Curves



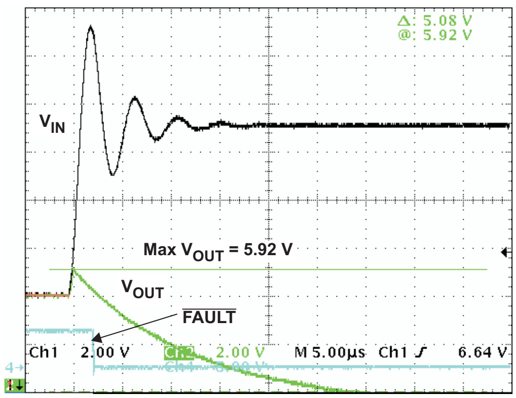
R_{OUT} = 6.6Ω

Figure 14. Normal Power-On Showing Soft-Start



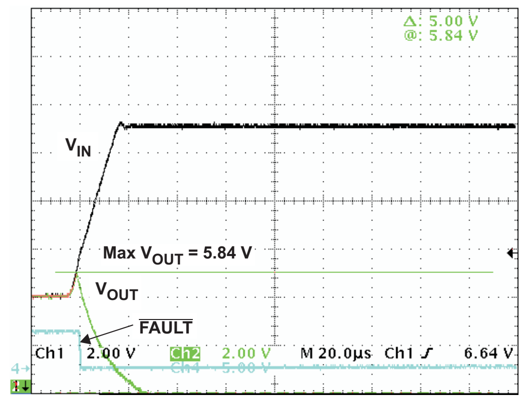
V_{IN} = 0V to 9V t_r = 50µs

Figure 15. OVP at Power-On



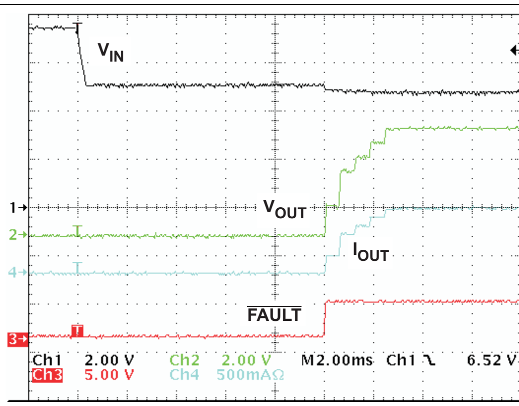
V_{IN} = 5V to 12V t_r = 1µs

Figure 16. OVP Response for Input Step



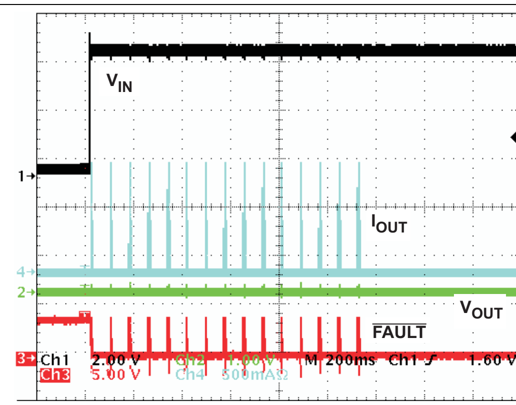
V_{IN} = 5V to 12V t_r = 20µs

Figure 17. OVP Response for Input Step



V_{IN} = 7.5V to 5V t_f = 400µs

Figure 18. Recovery from OVP



OCP Counter Counts to 15 Before Switching OFF Device

Figure 19. Powering Up into a Short Circuit on OUT Pin

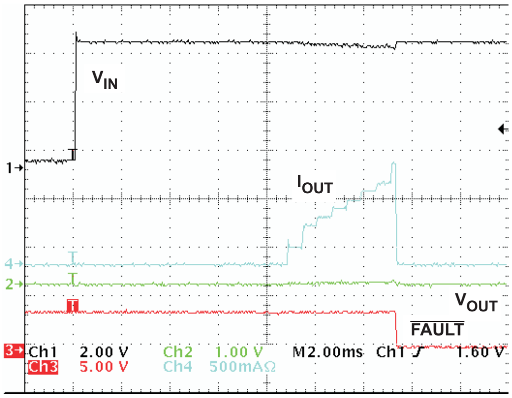
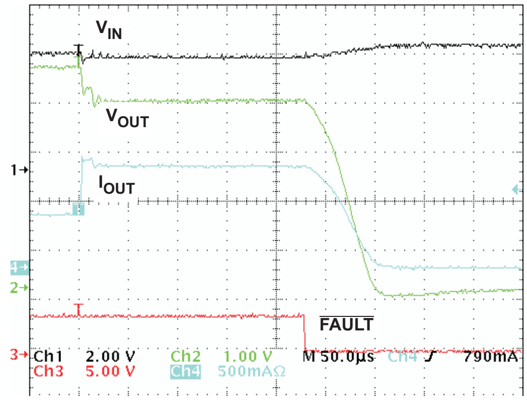
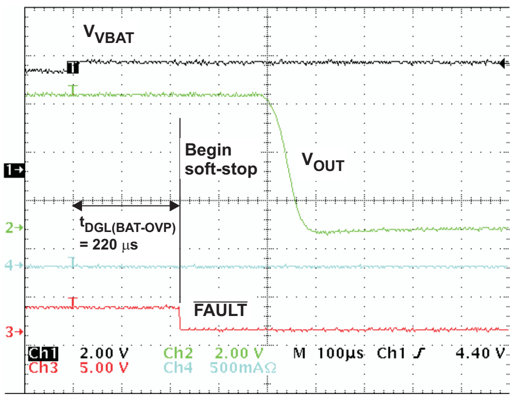


Figure 20. OCP, Zoom-in on the First Cycle of Figure 19



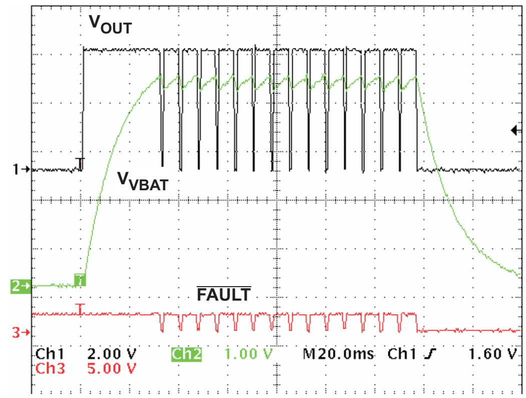
R_{OUT} Switches from 6.6 Ω to 3.3 Ω

Figure 21. OCP, Current Limiting and Soft-Stop



V_{VBAT} Steps from 4.2 V to 4.4 V

Figure 22. BAT-OVP, $t_{DGL(BAT-OVP)}$ and Soft-Stop



V_{VBAT} Cycles Between 4.1 V and 4.4 V

Figure 23. BAT-OVP, BAT-OVP Counter

9 Power Supply Recommendations

The intention is for the bq24314C device to operate with 5-V adapters with a maximum current rating of 1.5 A. The device operates from sources from 3 V to 5.7 V. Outside of this range, the output is disconnected due to either UVLO or the OVP function.

10 Layout

10.1 Layout Guidelines

- This device is a protection device, and is meant to protect down-stream circuitry from hazardous voltages. Potentially, high voltages may be applied to this IC. It has to be ensured that the edge-to-edge clearances of PCB traces satisfy the design rules for high voltages. See Figure 24.
- The device uses WSON packages with a thermal pad. For good thermal performance, the thermal pad must be thermally coupled with the PCB ground plane (GND). This requires a copper pad directly under the device. This copper pad should be connected to the ground plane with an array of thermal vias.
- Ensure that external C_{IN} and C_{OUT} are located close to the device. Other external components like R_{ILIM} and R_{BAT} must also be located close to the device.

10.2 Layout Example

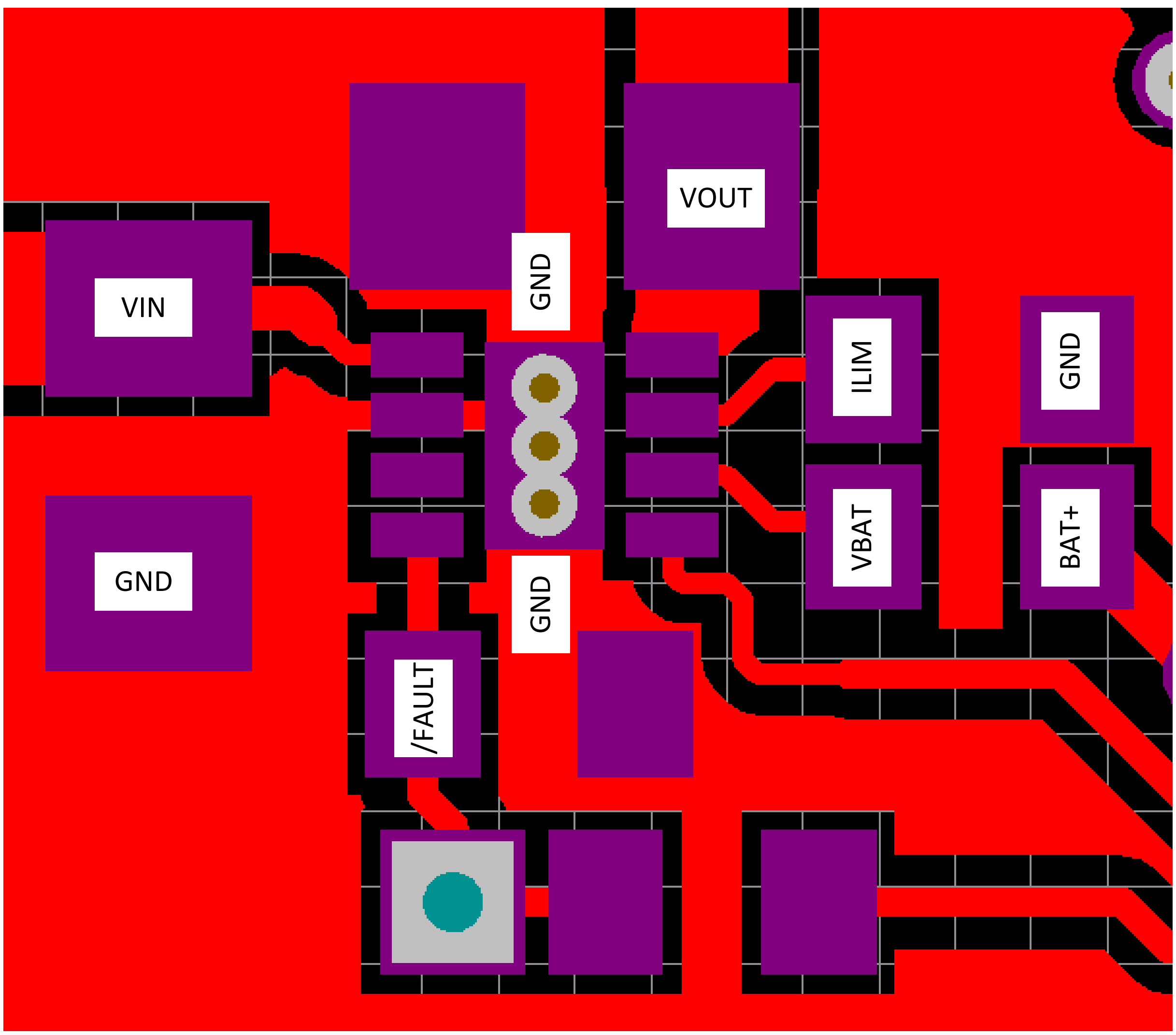


Figure 24. Layout Example Recommendation

11 器件和文档支持

11.1 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.2 商标

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Bluetooth is a trademark of Bluetooth SIG, Inc.
All other trademarks are the property of their respective owners.

11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ24314CDSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDL
BQ24314CDSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDL
BQ24314CDSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDL
BQ24314CDSGT.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDL

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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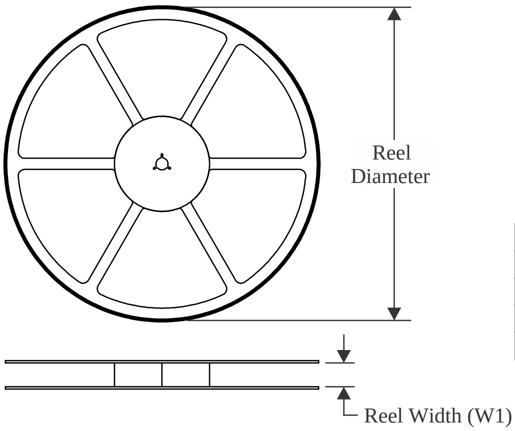
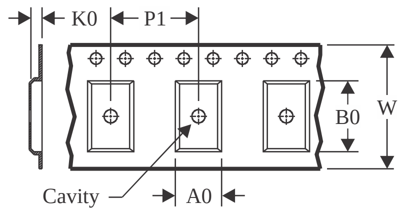
TAPE AND REEL INFORMATION

REEL DIMENSIONS

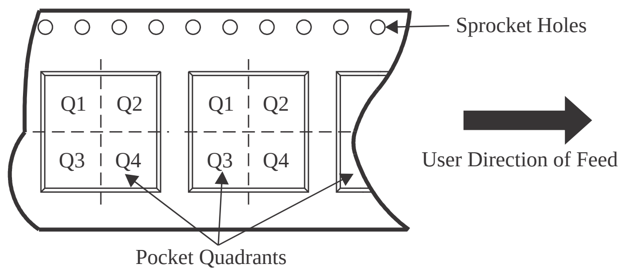


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

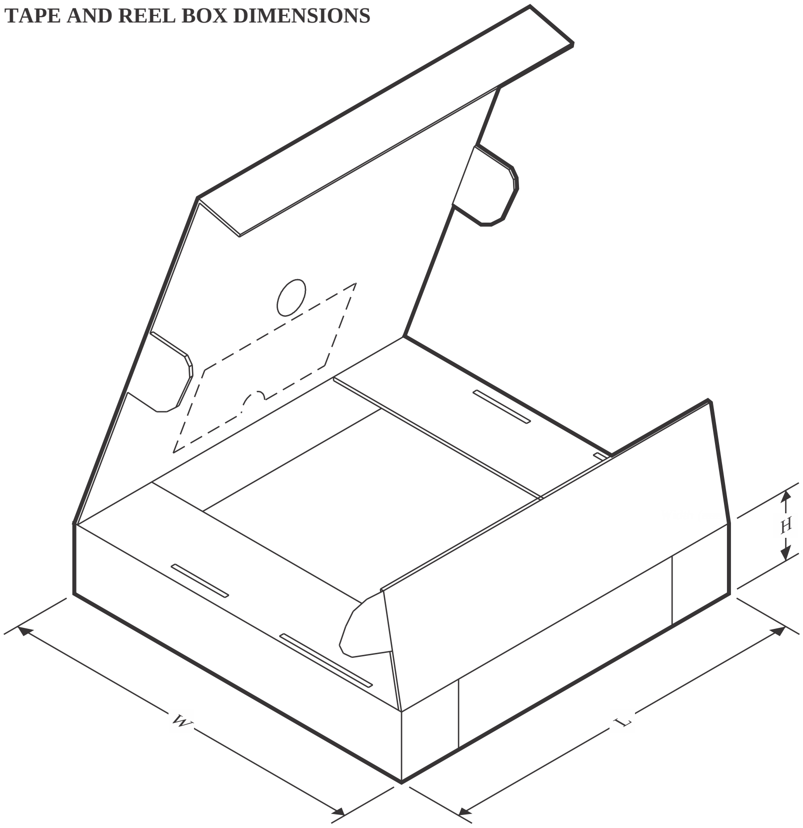
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24314CDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ24314CDSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24314CDSGR	WSON	DSG	8	3000	182.0	182.0	20.0
BQ24314CDSGT	WSON	DSG	8	250	182.0	182.0	20.0

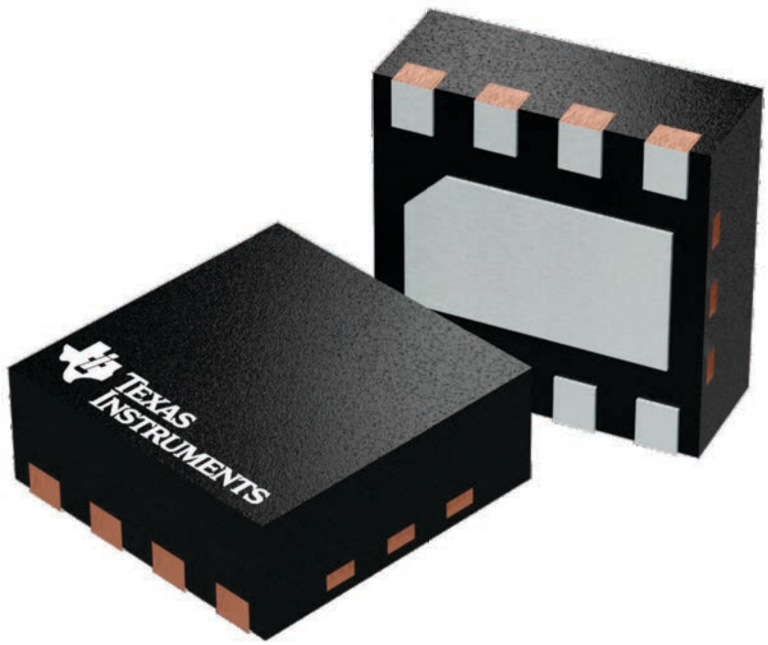
DSG 8

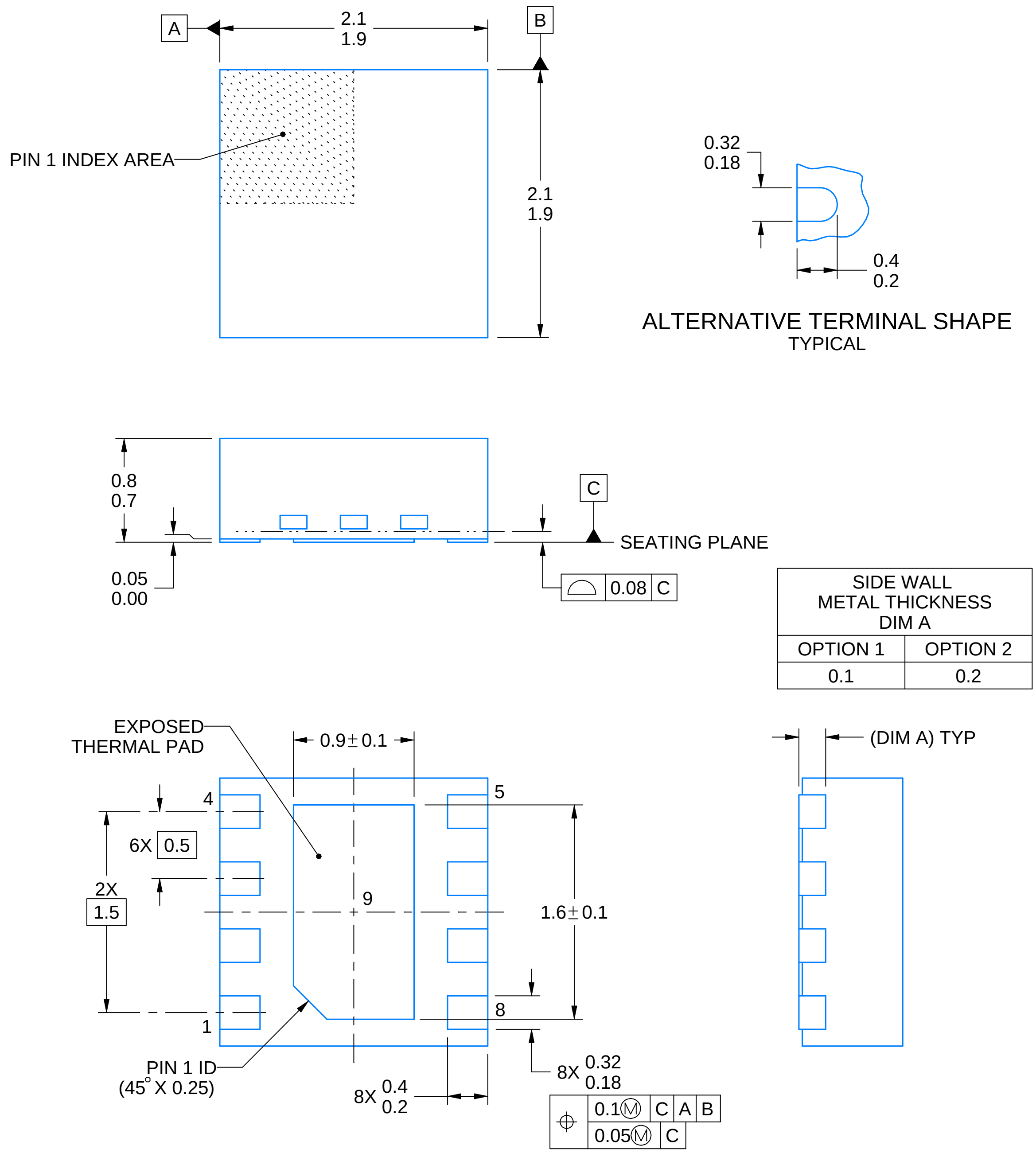
WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

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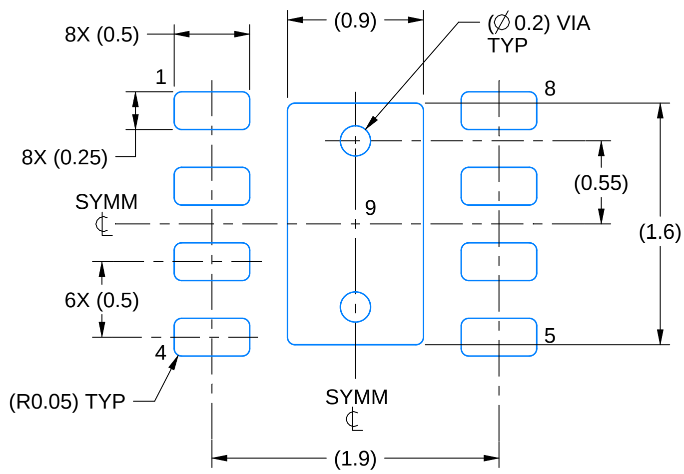
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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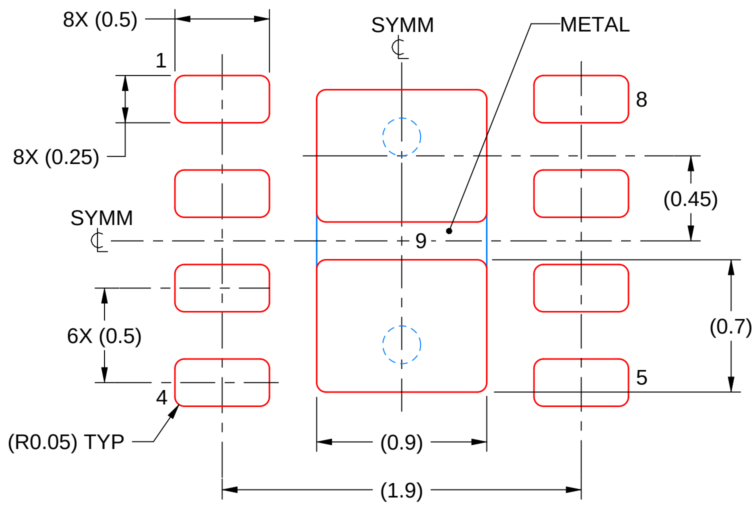
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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