OVERVOLTAGE AND OVERCURRENT PROTECTION IC AND Li+ CHARGER FRONT-END PROTECTION IC

Check for Samples: bq24300 bq24304 bq24305

FEATURES

- **Provides Protection for Three Variables:**
  - **Input Overvoltage**
  - **Input Overcurrent with Current Limiting**
  - **Battery Overvoltage**
- **30V Maximum Input Voltage**
- **Optional Input Reverse Polarity Protection**
- **High Immunity Against False Triggering Due to Voltage Spikes**
- **Robust Against False Triggering Due to Current Transients**
- **Thermal Shutdown**
- **Enable Function**
- **Small 2 mm × 2 mm 8-Pin SON Package**
- **LDO Mode Voltage Regulation Options:**
  - **5.5V on bq24300**
  - **4.5V on bq24304**
  - **5.0V on bq24305**

APPLICATIONS

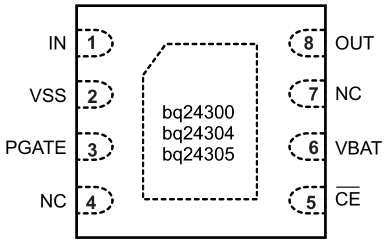
- **Bluetooth Headsets**
- **Low-Power Handheld Devices**

DESCRIPTION

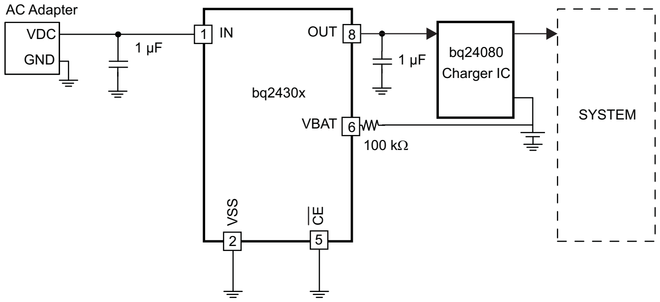
The bq24300 and bq24304 are highly integrated circuits designed to provide protection to Li-ion batteries from failures of the charging circuit. The IC continuously monitors the input voltage, the input current, and the battery voltage. The device operates like a linear regulator: for voltages up to the Input Overvoltage threshold, the output is held at 5.5V (bq24300), 5.0V (bq24305) or 4.5V (bq24304). In case of an input overvoltage condition, if the overvoltage condition persists for more than a few microseconds, the IC removes power from the charging circuit by turning off an internal switch. In the case of an overcurrent condition, it limits the current to a safe value for a blanking duration before turning the switch off. Additionally, the IC also monitors its own die temperature and switches off if it becomes too hot.

The IC also offers optional protection against reverse voltage at the input with an external P-channel MOSFET.

PINOUT



APPLICATION SCHEMATIC



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

DEVICE(2)	OUTPUT REGULATION VOLTAGE	PACKAGE	MARKING
bq24300	5.5V	2mm x 2mm SON	BZA
bq24304	4.5V	2mm x 2mm SON	CBS
bq24305	5.0V	2mm x 2mm SON	DSG

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) To order a 3000 pcs reel add R to the part number, or to order a 250 pcs reel add T to the part number.

PACKAGE DISSIPATION RATINGS

PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$ (1)
DSG	5°C/W	75°C/W

(1) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a Cu pad on the board. The pad is connected to the ground plane by a 2x3 via matrix.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	PIN	VALUE	UNIT
Input voltage	IN, PGATE (with respect to VSS)	–0.3 to 30	V
	OUT (with respect to VSS)	–0.3 to 12	V
	$\overline{CE}$, VBAT (with respect to VSS)	–0.3 to 7	V
ESD Withstand voltage	All (Human Body Model per JESD22-A114-E)	2000	V
	All (Machine Model per JESD22-A115-A)	200	V
	All (Charged Device Model per JESD22-C101-C)	500	V
	IN (IEC 61000-4-2) (with IN pin bypassed to VSS with 1.0-μF low-ESR ceramic capacitor)	15 (Air Discharge) 8 (Contact)	kV
Junction temperature, T_J		–40 to 150	°C
Storage temperature, T_{STG}		–65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Input voltage range		3.3	26	V
T_J	Junction temperature		0	125	°C

ELECTRICAL CHARACTERISTICS

over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-ON-RESET							
UVLO	Under-voltage lock-out, input power detected threshold		$\overline{CE}$ = Low, V_{IN} increasing from 0V to 3V	2.5	2.7	2.8	V
$V_{HYS\text{-}UVLO}$	Hysteresis on UVLO		$\overline{CE}$ = Low, V_{IN} decreasing from 3V to 0V	200	260	300	mV
$t_{DGL(PGOOD)}$	Deglitch time, input power detected status		$\overline{CE}$ = Low, time measured from V_{IN} 0V → 4V 1μs rise time, to output turning ON		8		ms
IN							
I_{DD}	Operating current	bq24300	V_{IN} = 5V, $\overline{CE}$ = Low, no load on OUT pin		340	400	μA
		bq24304, bq24305			410	500	
I_{STDBY}	Standby current		$\overline{CE}$ = High, V_{IN} = 5V		65	95	μA
INPUT TO OUTPUT CHARACTERISTICS							
V_{DO}	Drop-out voltage IN to OUT		$\overline{CE}$ = Low, V_{IN} = 4 V, I_{OUT} = 250 mA		45	75	mV
OUTPUT VOLTAGE REGULATION							
$V_{O(REG)}$	Output voltage	bq24300	$\overline{CE}$ = Low, V_{IN} = 6 V, I_{OUT} = 250 mA	5.30	5.5	5.70	V
		bq24304		4.36	4.5	4.64	
		bq24305		4.85	5.0	5.15	
INPUT OVERVOLTAGE PROTECTION							
V_{OVP}	Input overvoltage protection threshold		$\overline{CE}$ = Low, V_{IN} increasing from 4V to 12V	10.2	10.5	10.8	V
$V_{HYS\text{-}OVP}$	Hysteresis on OVP		$\overline{CE}$ = Low, V_{IN} decreasing from 12V to 4V	60	100	160	mV
$t_{BLANK(OVP)}$	Blanking time, on OVP		$\overline{CE}$ = Low, Time measured from V_{IN} 4V → 12V, 1μs rise time, to output turning OFF		64		μs
$t_{ON(OVP)}$	Recovery time from input overvoltage condition		$\overline{CE}$ = Low, Time measured from V_{IN} 12V → 4V, 1μs fall time, to output turning ON		8		ms
INPUT OVERCURRENT PROTECTION							
I_{OCP}	Input overcurrent protection range		$\overline{CE}$ = Low, V_{IN} = 5 V	250	300	350	mA
$t_{BLANK(OCP)}$	Blanking time, input overcurrent detected		$\overline{CE}$ = Low		5		ms
$t_{REC(OCP)}$	Recovery time from input overcurrent condition		$\overline{CE}$ = Low		64		ms
BATTERY OVERVOLTAGE PROTECTION							
BV_{OVP}	Battery overvoltage protection threshold		$\overline{CE}$ = Low, V_{IN} > 4.4V, V_{VBAT} increasing from 4.2 V to 4.5 V	4.30	4.35	4.40	V
$V_{HYS\text{-}BOVP}$	Hysteresis on BV_{OVP}		$\overline{CE}$ = Low, V_{IN} > 4.4V, V_{VBAT} decreasing from 4.5 V to 3.9 V	200	275	320	mV
I_{VBAT}	Input bias current on the VBAT pin		V_{VBAT} = 4.4 V, T_J = 25°C			10	nA
$t_{DGL(BOVP)}$	Deglitch time, battery overvoltage detected		$\overline{CE}$ = Low, V_{IN} > 4.4V, time measured from V_{VBAT} 4.2V → 4.5V, 1μs rise time to output turning OFF		176		μs
P-FET GATE DRIVER							
V_{GCLMP}	Gate driver clamp voltage		V_{IN} > 17V	13	15	17	V
THERMAL PROTECTION							
$T_{J(OFF)}$	Thermal shutdown temperature				140	150	°C
$T_{J(OFF\text{-}HYS)}$	Thermal shutdown hysteresis				20		°C
LOGIC LEVELS ON $\overline{CE}$							
V_{IL}	Low-level input voltage			0		0.4	V
V_{IH}	High-level input voltage			1.4			V
I_{IL}	Low-level input current					1	μA

ELECTRICAL CHARACTERISTICS (continued)

over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	V_{CE} = 1.8V			15	µA

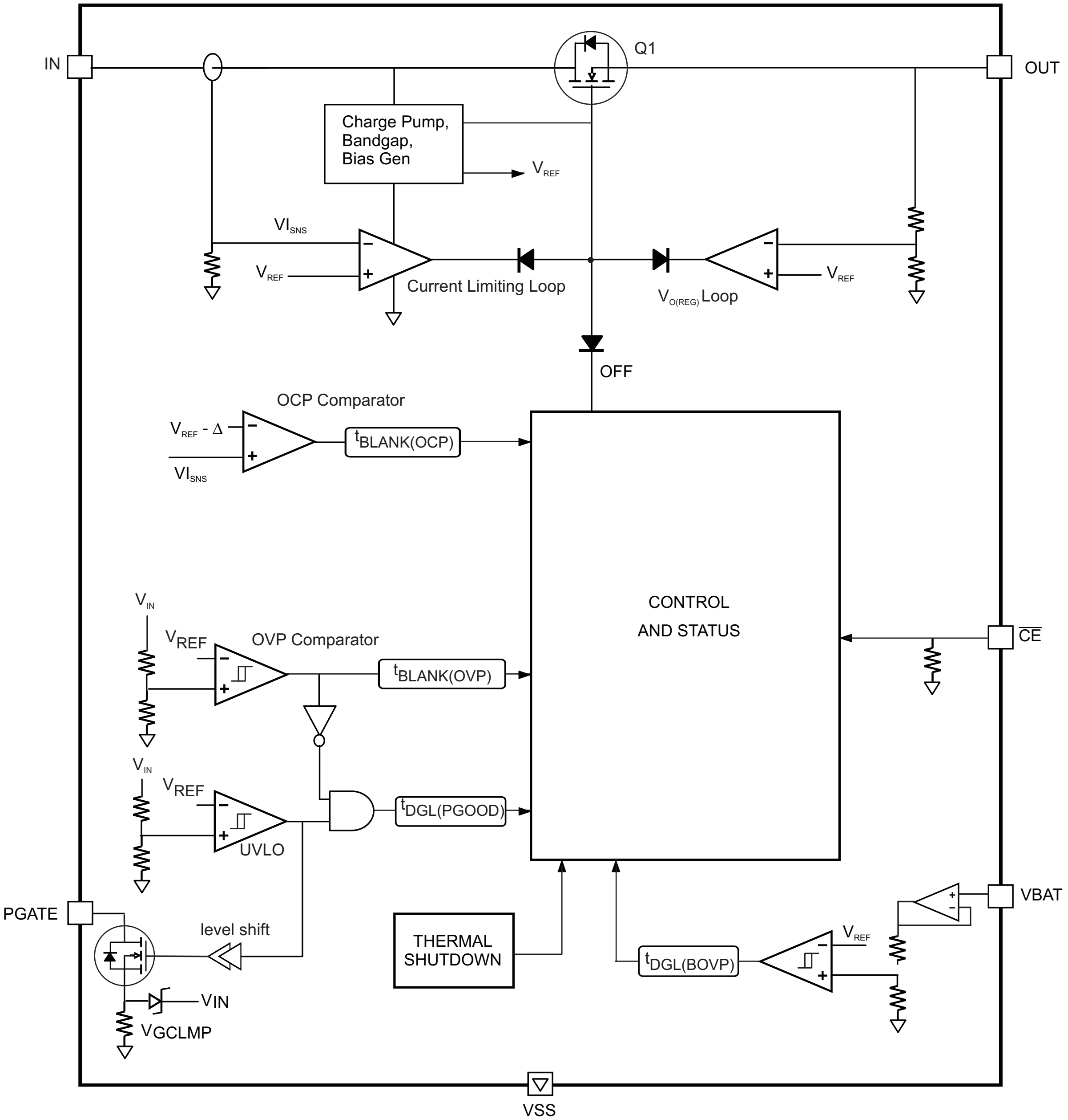
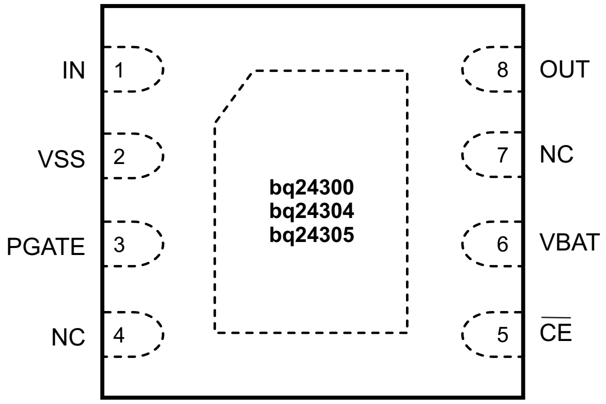


Figure 1. Simplified Block Diagram

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	**NO.**		
IN	1	I	Input power, connect to external DC supply. Connect external 0.1µF (minimum) ceramic capacitor to VSS
VSS	2	–	Ground terminal
PGATE	3	O	Gate drive for optional external P-FET
NC	4, 7		Do not connect to any external circuit. These pins may have internal connections used for test purposes.
$\overline{\text{CE}}$	5	I	Chip enable input. Active low. When $\overline{\text{CE}}$ = Hi, the input FET is off. Internally pulled down.
VBAT	6	I	Battery voltage sense input. Connect to pack positive terminal through a resistor.
OUT	8	O	Output terminal to the charging system. Connect external 1µF capacitor (minimum) ceramic capacitor to VSS
Thermal PAD		–	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.



TYPICAL OPERATING PERFORMANCE

Test conditions (unless otherwise noted) for typical operating performance are: V_{IN} = 5 V, C_{IN} = 1 µF, C_{OUT} = 1µF, R_{BAT} = 100 kΩ, R_{OUT} = 22Ω, T_A = 25°C (see Figure 22 - Typical Application Circuit)

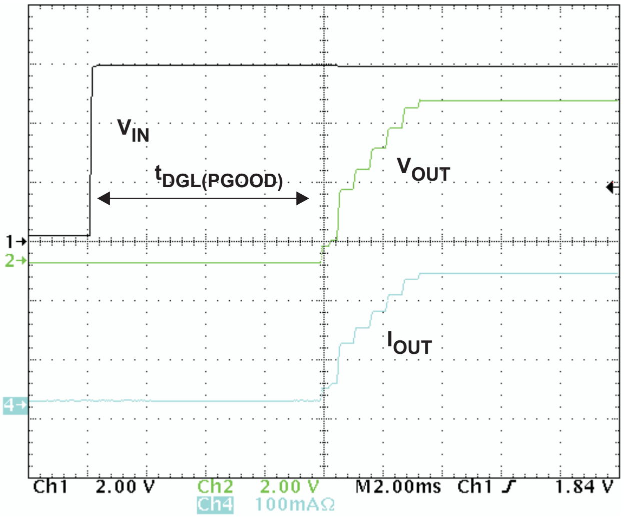


Figure 2. Normal Power-On Showing Soft-Start.
V_{IN} 0 V to 6.0 V, t_R = 20µs

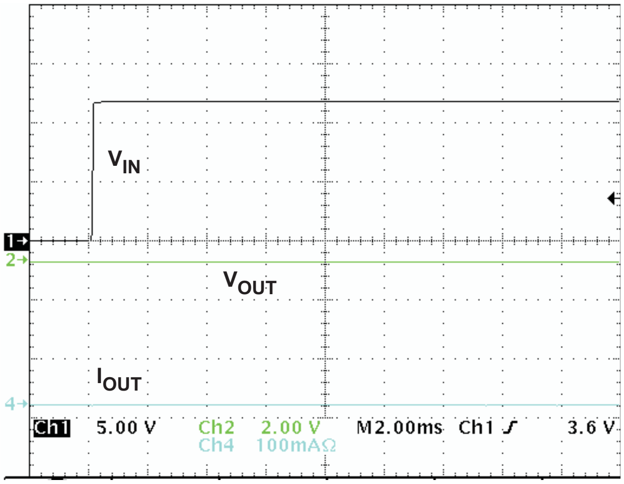


Figure 3. Power-On with Input Overvoltage.
V_{IN} 0 V to 12.0 V, t_R = 50 µs

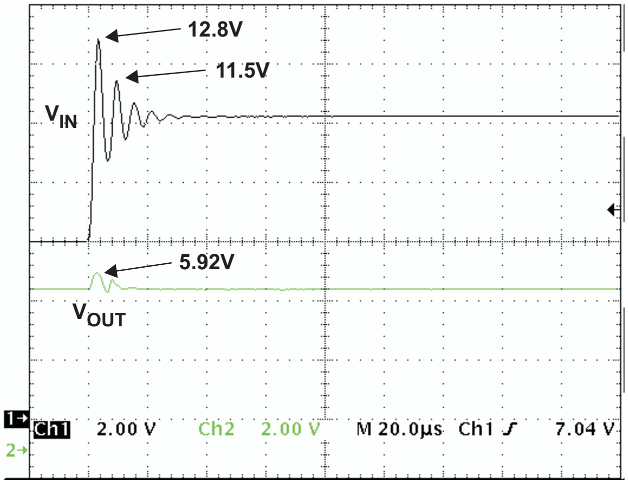


Figure 4. bq24300 OVP Response for Input Step.
V_{IN} 6.0 V to 10.3 V, t_R = 2µs. Shows Immunity to Ringing

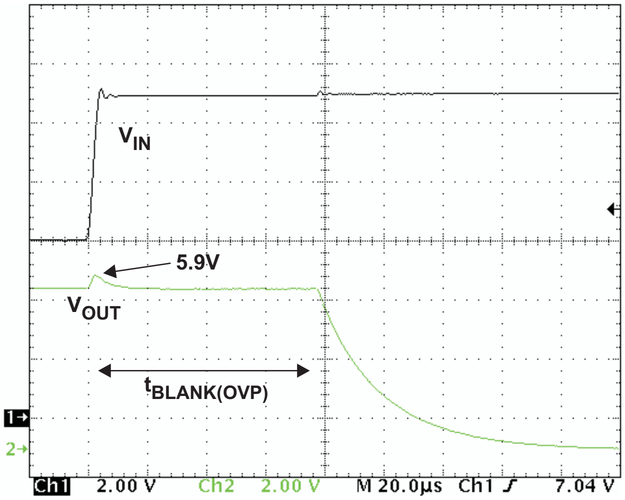


Figure 5. bq24300 OVP Response for Input Step.
V_{IN} 6.0 V to 11.0 V, t_R = 5µs. Shows OVP Blanking Time

TYPICAL OPERATING PERFORMANCE

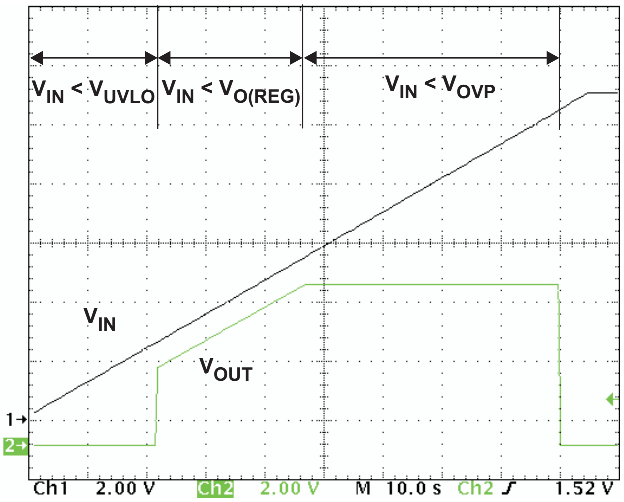


Figure 6. OUT Pin Response to Slow Input Ramp

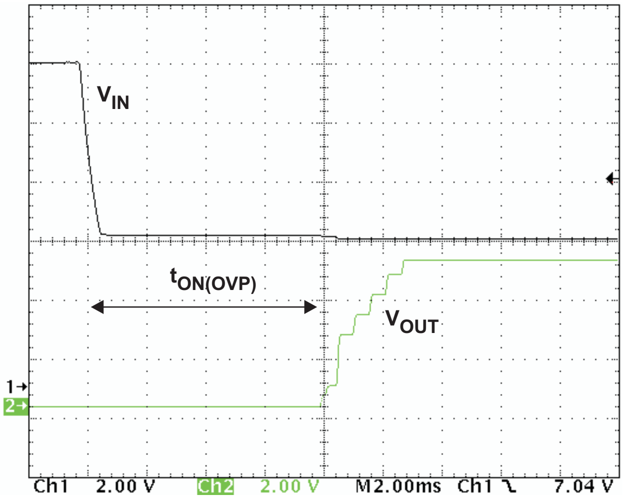


Figure 7. bq24300 Recovery from Input OVP.
V_{IN} 11.0 V to 5.0 V, t_F = 400 µs

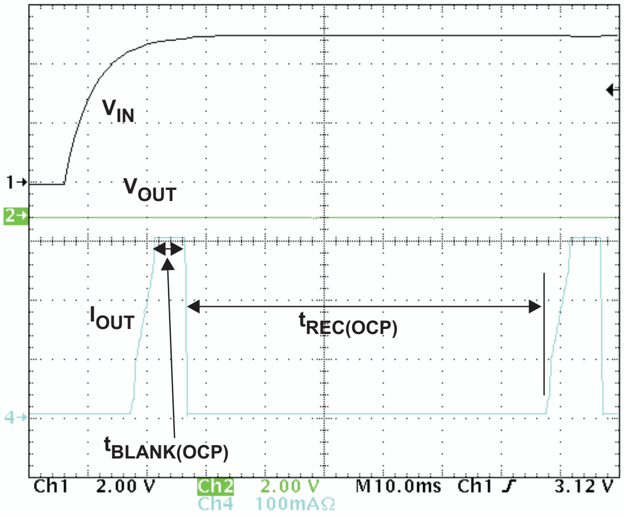


Figure 8. OCP, Powering up with OUT Pin Shorted to VSS

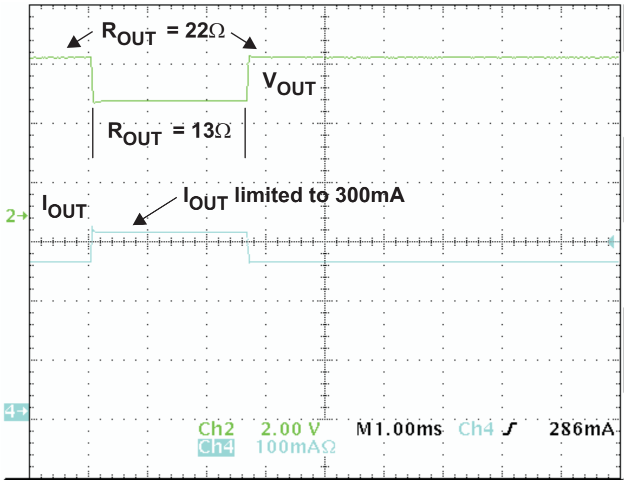


Figure 9. OCP, Showing Current Limiting and
OCP Blanking. R_{OUT} 22Ω to 13Ω for 2.6 ms to 22Ω

TYPICAL OPERATING PERFORMANCE (continued)

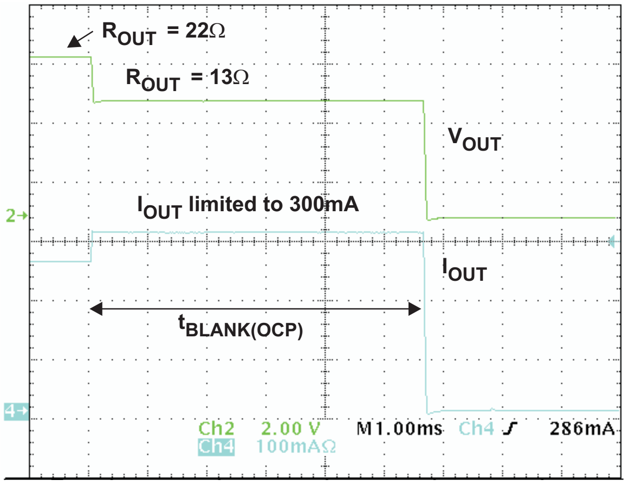


Figure 10. OCP, Showing Current Limiting and OCP Blanking. R_{OUT} 22Ω to 13Ω

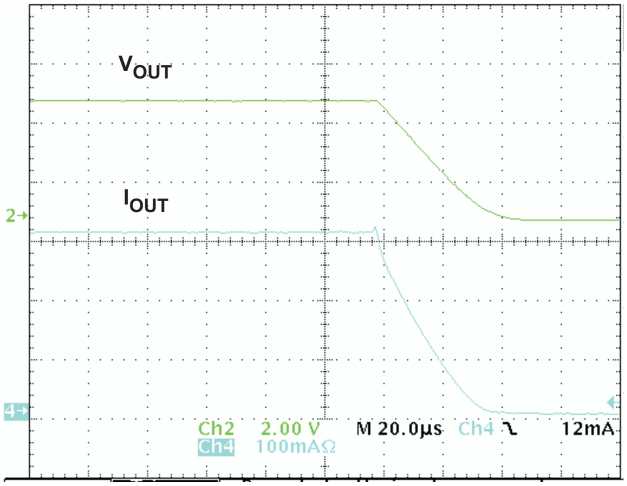


Figure 11. Zoom-in on Turn-off Region of Figure 10, Showing Soft-Stop

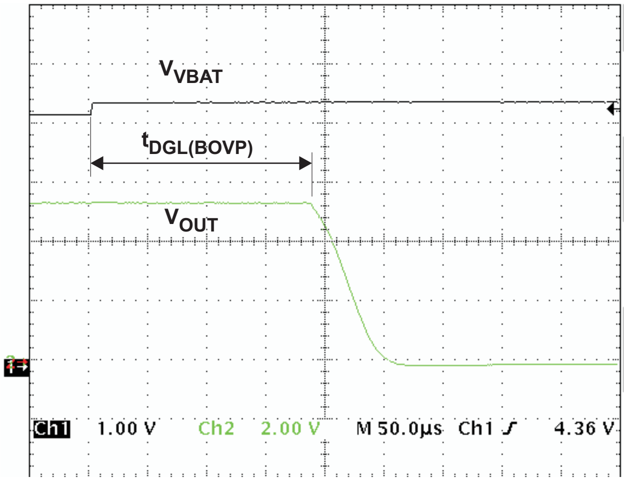


Figure 12. Battery OVP. V_{VBAT} Steps from 4.3 V to 4.5 V. Shows $t_{DGL(BOVP)}$ and Soft-Stop

TYPICAL OPERATING PERFORMANCE (continued)

UNDERVOLTAGE LOCKOUT vs FREE-AIR TEMPERATURE

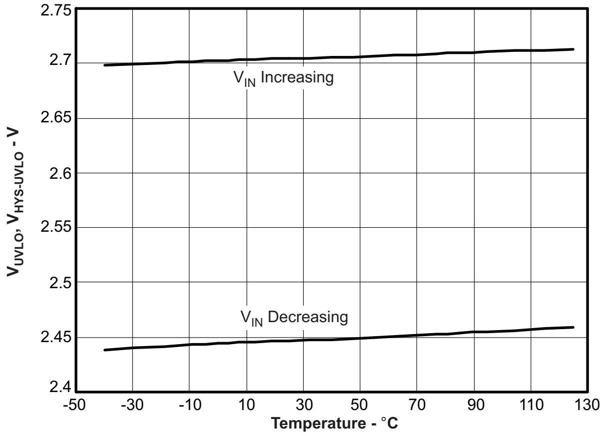


Figure 13.

DROPOUT VOLTAGE (IN to OUT) vs FREE-AIR TEMPERATURE

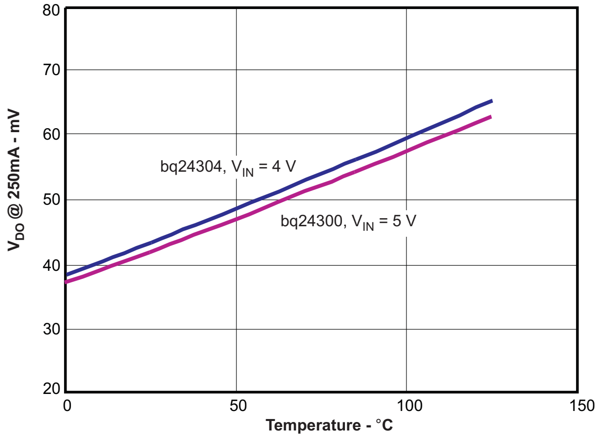


Figure 14.

REGULATION VOLTAGE (OUT pin) vs FREE-AIR TEMPERATURE

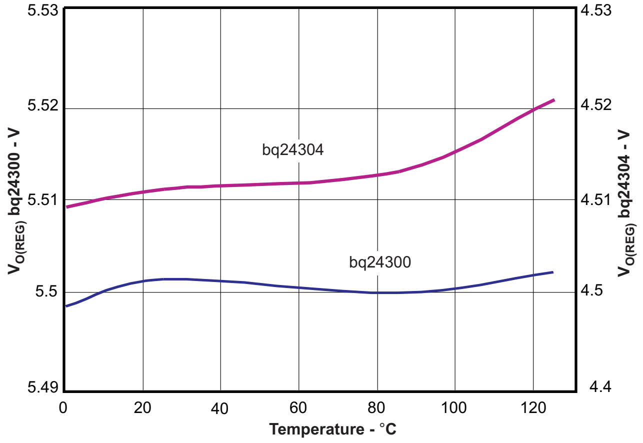


Figure 15.

OVP THRESHOLD vs FREE-AIR TEMPERATURE

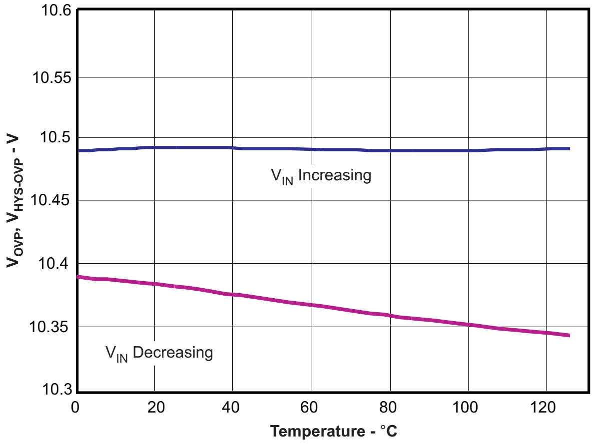


Figure 16.

TYPICAL OPERATING PERFORMANCE (continued)

OCP THRESHOLD vs FREE-AIR TEMPERATURE

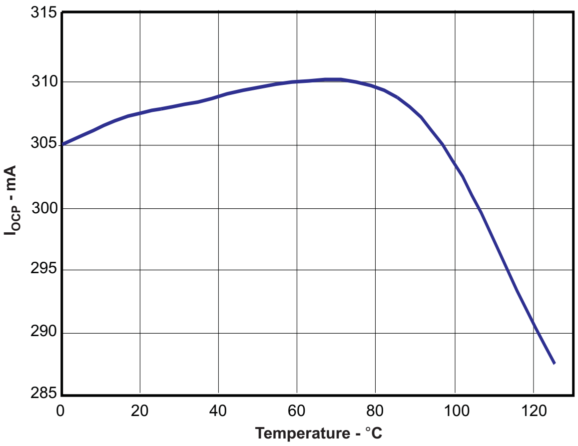


Figure 17.

BATTERY OVP THRESHOLDS vs FREE-AIR TEMPERATURE

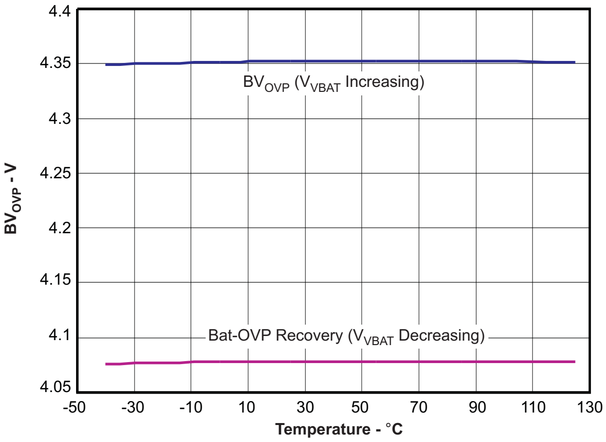


Figure 18.

LEAKAGE CURRENT (BAT pin) vs FREE-AIR TEMPERATURE

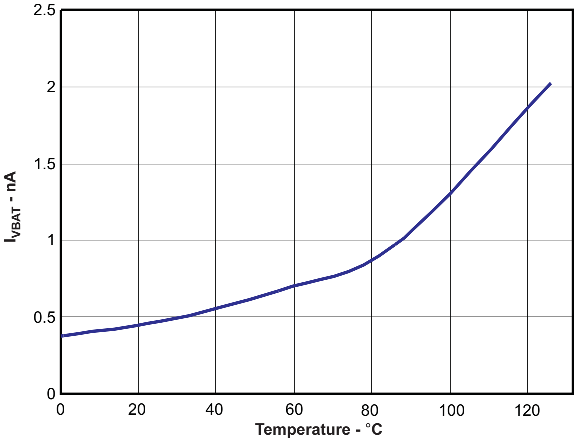


Figure 19.

SUPPLY CURRENT vs INPUT VOLTAGE

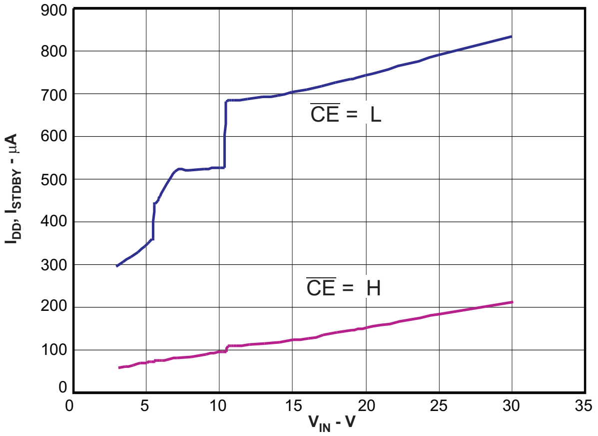


Figure 20.

TYPICAL OPERATING PERFORMANCE (continued)

PGATE VOLTAGE
vs
INPUT VOLTAGE

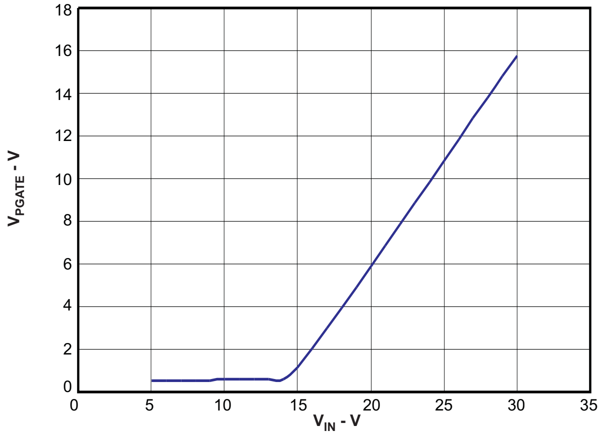


Figure 21.

TYPICAL APPLICATION CIRCUITS

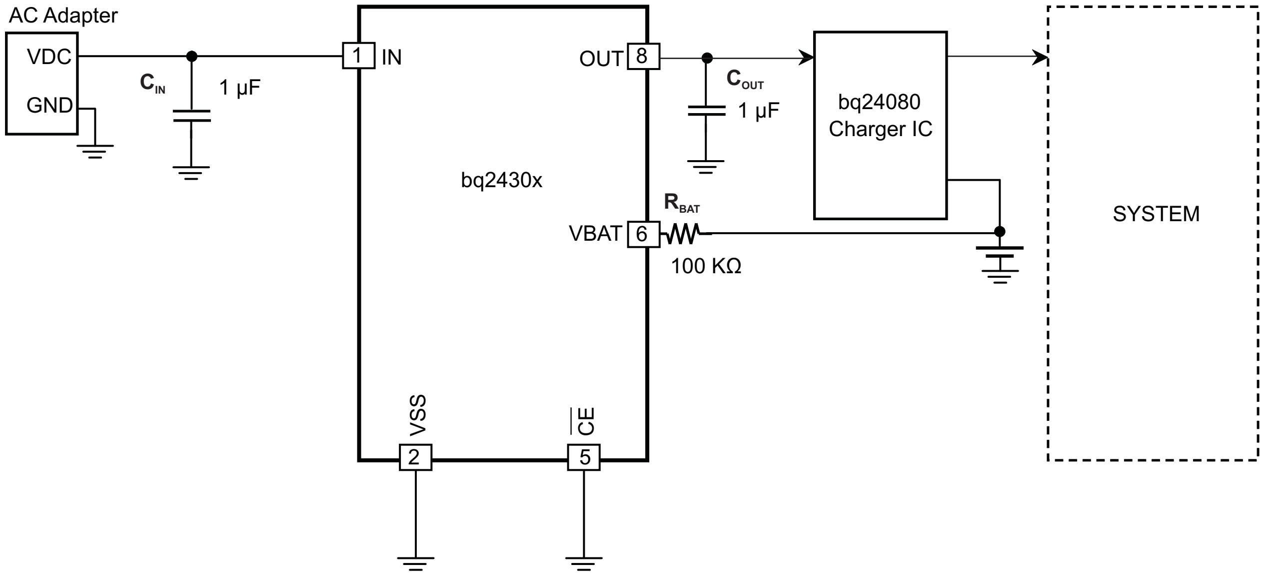


Figure 22. Overvoltage, Overcurrent, and Battery Overvoltage Protection

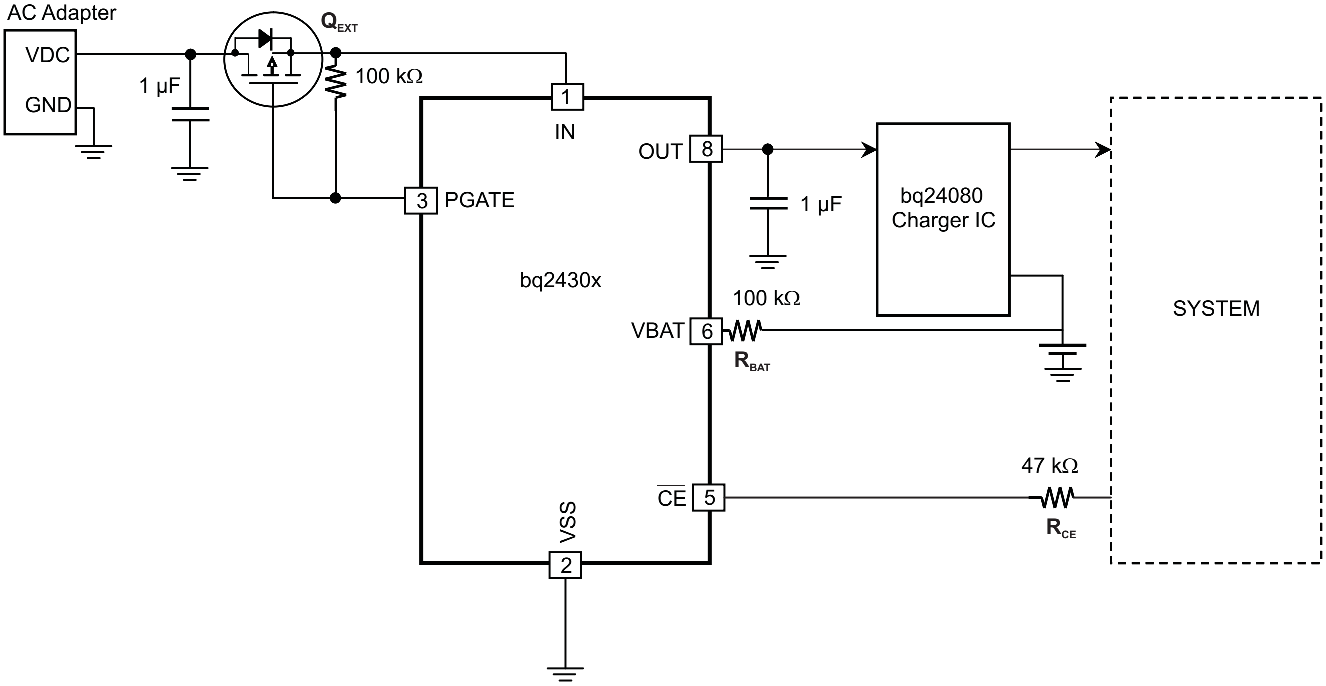


Figure 23. OVP, OCP, BATOVP With Input Reverse-Polarity Protection

DETAILED FUNCTIONAL DESCRIPTION

The bq24300 and bq24304 are highly integrated circuits designed to provide protection to Li-ion batteries from failures of the charging circuit. The IC continuously monitors the input voltage, the input current and the battery voltage, and protects down-stream circuitry from damage if any of these parameters exceeds safe values. The IC also monitors its own die temperature and switches off if it becomes too hot.

The IC also offers optional protection against reverse voltage at the input with an external P-channel MOSFET.

POWER DOWN

The device remains in power down mode when the input voltage at the IN pin is below the under-voltage threshold V_{UVLO}. The FET Q1 (see Figure 1) connected between IN and OUT pins is off.

POWER-ON RESET

The device resets all internal timers when the input voltage at the IN pin exceeds the UVLO threshold. The gate driver for the external P-FET is enabled. The IC then waits for duration $t_{DGL(PGOOD)}$ for the input voltage to stabilize. If, after $t_{DGL(PGOOD)}$, the input voltage and battery voltage are safe, FET Q1 is turned ON. The IC has a soft-start feature to control the inrush current. This soft-start minimizes voltage ringing at the input (the ringing occurs because the parasitic inductance of the adapter cable and the input bypass capacitor form a resonant circuit). Figure 2 shows the power-up behavior of the device. Because of the deglitch time at power-on, if the input voltage rises rapidly to beyond the OVP threshold, the device will not switch on at all, as shown in Figure 3.

OPERATION

The device continuously monitors the input voltage, the input current and the battery voltage as described in detail in the following sections:

Input Overvoltage Protection

As long as the input voltage is less than $V_{O(REG)}$, the output voltage tracks the input voltage (less the drop caused by R_{DS}ON of Q1). If the input voltage is greater than $V_{O(REG)}$ (plus the R_{DS}ON drop) and less than V_{OVP}, the device acts like a series linear regulator, with the output voltage regulated to $V_{O(REG)}$. If the input voltage rises above V_{OVP}, the output voltage is clamped to $V_{O(REG)}$ for a blanking duration $t_{BLANK(OVP)}$. If the input voltage returns below V_{OVP} within $t_{BLANK(OVP)}$, the device continues normal operation (see Figure 4). This provides protection against turning power off due to transient overvoltage spikes while still protecting the system. However, if the input voltage remains above V_{OVP} for more than $t_{BLANK(OVP)}$, the internal FET is turned off, removing power from the circuit (see Figure 5). When the input voltage comes back to a safe value, the device waits for $t_{ON(OVP)}$ then switches on Q1 and goes through the soft-start routine (see Figure 7).

Figure 6 describes graphically the behavior of the OUT pin over the entire range of input voltage variation.

Input Overcurrent Protection

The device can supply load current up to I_{OCP} continuously. If the load current tries to exceed this threshold, the current is limited to I_{OCP} for a maximum duration of $t_{BLANK(OCP)}$. If the load current returns to less than I_{OCP} before $t_{BLANK(OCP)}$ times out, the device continues to operate (see Figure 9). However, if the overcurrent situation persists for $t_{BLANK(OCP)}$, FET Q1 is turned off for a duration of $t_{REC(OCP)}$. It is then turned on again and the current is monitored all over again (see Figure 10 and Figure 8).

To prevent the input voltage from spiking up due to the inductance of the input cable, Q1 is not turned off rapidly in an overcurrent fault condition. Instead, the gate drive of Q1 is reduced slowly, resulting in a “soft-stop”, as shown in Figure 11.

Battery Overvoltage Protection

The battery overvoltage threshold BV_{OVP} is internally set to 4.35V. If the battery voltage exceeds the BV_{OVP} threshold for longer than $t_{DGL(BOVP)}$, FET Q1 is turned off (see Figure 12). This switch-off is also a soft-stop. Q1 is turned ON (soft-start) once the battery voltage drops to $BV_{OVP} – V_{HYS-BOVP}$.

Thermal Protection

If the junction temperature of the device exceeds $T_{J(OFF)}$, FET Q1 is turned off. The FET is turned back on when the junction temperature falls below $T_{J(OFF)} – T_{J(OFF-HYS)}$.

Enable Function

The IC has an enable pin which can be used to enable or disable the device. When the $\overline{CE}$ pin is driven high, the internal FET is turned off. When the $\overline{CE}$ pin is low, the FET is turned on if other conditions are safe. The $\overline{CE}$ pin has an internal pull-down resistor of 200 kΩ (typical) and can be left floating.

PGATE Pin

When used with an external P-Channel MOSFET, in addition to OVP, OCP and Battery-OVP, the device offers protection against input reverse polarity up to –30V. When operating with normal polarity, the IC first turns on due to current flow through the body-diode of the FET Q_{EXT}. The PGATE pin then goes low, turning ON Q_{EXT}. For input voltages larger than V_{GCLMP}, the voltage on the PGATE pin is driven to $V_{IN} – V_{GCLMP}$. This ensures that the gate to source voltage seen by Q_{EXT} does not exceed $–V_{GCLMP}$.

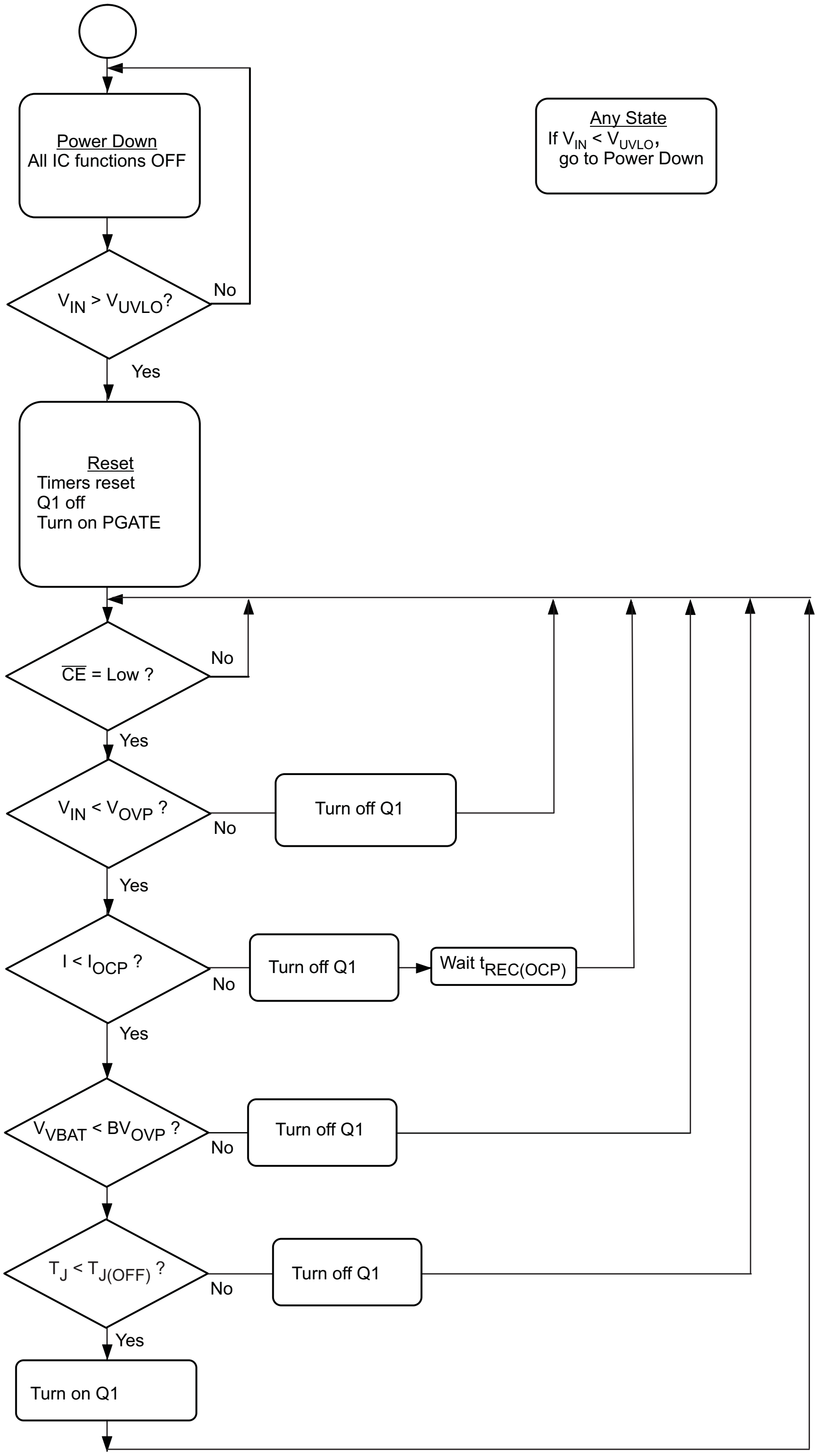


Figure 24. Flow Diagram

APPLICATION INFORMATION

Selection of R_{BAT}:

It is strongly recommended that the battery not be tied directly to the VBAT pin of the device, as under some failure modes of the IC, the voltage at the IN pin may appear on the VBAT pin. This voltage can be as high as 30V, and applying 30V to the battery in case of the failure of the device can be hazardous. Connecting the VBAT pin through R_{BAT} prevents a large current from flowing into the battery in case of failure of the IC. In the interests of safety, R_{BAT} should have a very high value. The problem with a large R_{BAT} is that the voltage drop across this resistor because of the VBAT bias current I_{VBAT} causes an error in the BV_{OVP} threshold. This error is over and above the tolerance on the nominal 4.35V BV_{OVP} threshold.

Choosing R_{BAT} in the range 100KΩ to 470kΩ is a good compromise. In the case of IC failure, with R_{BAT} equal to 100kΩ, the maximum current flowing into the battery would be (30V – 3V) ÷ 100kΩ = 270μA, which is low enough to be absorbed by the bias currents of the system components. R_{BAT} equal to 100kΩ would result in a worst-case voltage drop of $R_{BAT} \times I_{VBAT} \approx 1mV$. This is negligible compared to the internal tolerance of 50mV on the BV_{OVP} threshold.

If the Bat-OVP function is not required, the VBAT pin should be connected to VSS.

Selection of R_{CE}:

The $\overline{CE}$ pin can be used to enable and disable the IC. If host control is not required, the $\overline{CE}$ pin can be tied to ground or left un-connected, permanently enabling the device.

In applications where external control is required, the $\overline{CE}$ pin can be controlled by a host processor. As in the case of the VBAT pin (see above), the $\overline{CE}$ pin should be connected to the host GPIO pin through as large a resistor as possible. The limitation on the resistor value is that the minimum V_{OH} of the host GPIO pin less the drop across the resistor should be greater than V_{IH} of the bq2430x $\overline{CE}$ pin. The drop across the resistor is given by $R_{CE} \times I_{IH}$.

Selection of Input and Output Bypass Capacitors:

The input capacitor C_{IN} in Figure 22 and Figure 23 is for decoupling, and serves an important purpose. Whenever there is a step change downwards in the system load current, the inductance of the input cable causes the input voltage to spike up. C_{IN} prevents the input voltage from overshooting to dangerous levels. It is strongly recommended that a ceramic capacitor of at least 1μF be used at the input of the device. It should be located in close proximity to the IN pin.

C_{OUT} in Figure 23 is also important: If a fast (< 1μs rise-time) overvoltage transient occurs at the input, the current that charges C_{OUT} causes the device's current-limiting loop to kick in, reducing the gate-drive to FET Q1. This results in improved performance for input overvoltage protection. C_{OUT} should also be a ceramic capacitor of at least 1μF, located close to the OUT pin. C_{OUT} also serves as the input decoupling capacitor for the charging circuit downstream of the protection IC.

PCB Layout Guidelines:

1. This device is a protection device, and is meant to protect down-stream circuitry from hazardous voltages. Potentially, high voltages may be applied to this IC. It has to be ensured that the edge-to-edge clearances of PCB traces satisfy the design rules for the maximum voltages expected to be seen in the system.
2. The device uses SON packages with a PowerPAD™. For good thermal performance, the PowerPAD should be thermally coupled with the PCB ground plane. In most applications, this will require a copper pad directly under the IC. This copper pad should be connected to the ground plane with an array of thermal vias.
3. C_{IN} and C_{OUT} should be located close to the IC. Other components like R_{BAT} should also be located close to the IC.

REVISION HISTORY

Changes from Original (August 2007) to Revision A	Page
• Changed the devices from Product Preview status to Production.	1

Changes from Revision A (October 2007) to Revision B	Page
• Added device bq24305 to the data sheet	1
• Changed the bq24305 marking in the Ordering Information table From CHD To: DSG	2
• Changed Figure 22, Overvoltage, Overcurrent, and Battery Overvoltage Protection	12
• Changed Figure 23, OVP, OCP, BATOVP With Input Reverse-Polarity Protection	12

Changes from Revision B (September 2009) to Revision C	Page
• Deleted Lead temperature (soldering, 10 seconds) from the Abs Max table. This is covered in the Package information.	2
• Changed Recommended Operating Conditions, Input voltage range - MAX value From 30V To: 26V	2
• Changed BV_{OVP} test conditions - From: $\overline{CE}$ = Low, V_{IN} > 4.3V, V_{VBAT} increasing To: $\overline{CE}$ = Low, V_{IN} > 4.4V, V_{VBAT} increasing	3
• Changed $V_{HYS\text{-}BOVP}$ test conditions - From: $\overline{CE}$ = Low, V_{IN} > 4.3V, V_{VBAT} decreasing To: $\overline{CE}$ = Low, V_{IN} > 4.4V, V_{VBAT} decreasing	3
• Changed the Gate driver clamp voltage Typ valur From: 14V To: 15V and the Max value From: 15V To: 17V	3
• Changed Figure 23, OVP, OCP, BATOVP With Input Reverse-Polarity Protection	12
• Changed section - Selection of R_{BAT} text From: (30V – 3V) x 100kΩ = 246µA To: battery would be (30V – 3V) ÷ 100kΩ = 270µA	16

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ24300DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	0 to 125	BZA
BQ24300DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	BZA
BQ24300DSGR.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	BZA
BQ24300DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	0 to 125	BZA
BQ24300DSGT.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	BZA
BQ24300DSGT.B	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	BZA
BQ24305DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 125	DSG
BQ24305DSGR.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 125	DSG
BQ24305DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 125	DSG
BQ24305DSGT.B	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 125	DSG

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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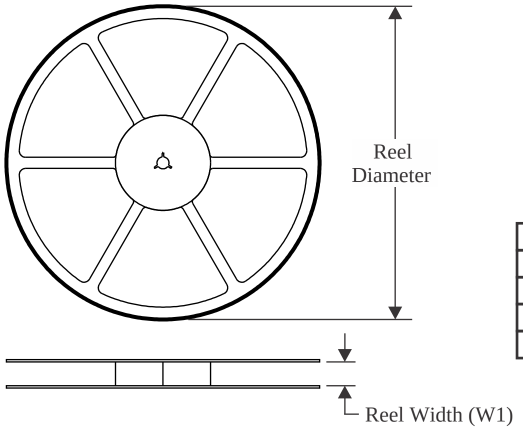
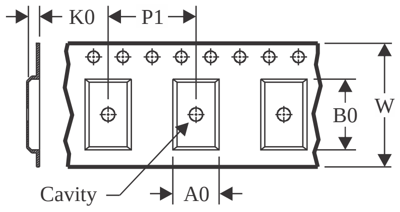
TAPE AND REEL INFORMATION

REEL DIMENSIONS

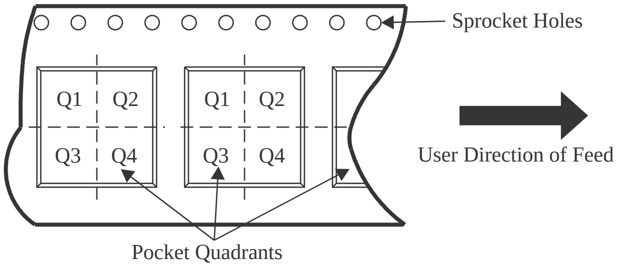


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

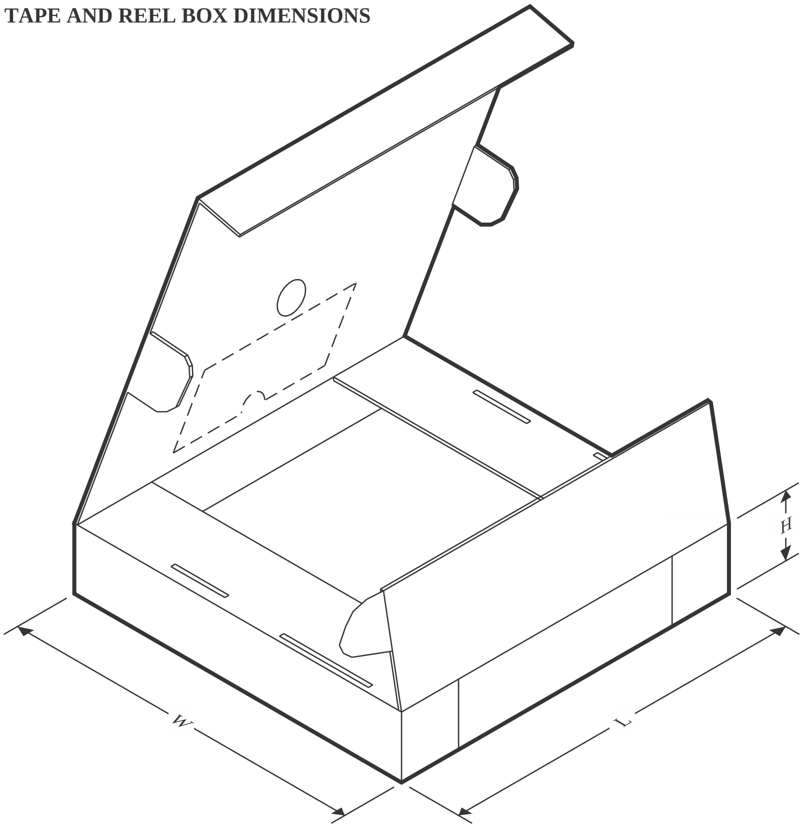
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24300DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ24300DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ24305DSGR	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24305DSGT	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24300DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ24300DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ24305DSGR	WSON	DSG	8	3000	213.0	191.0	35.0
BQ24305DSGT	WSON	DSG	8	250	213.0	191.0	35.0

GENERIC PACKAGE VIEW

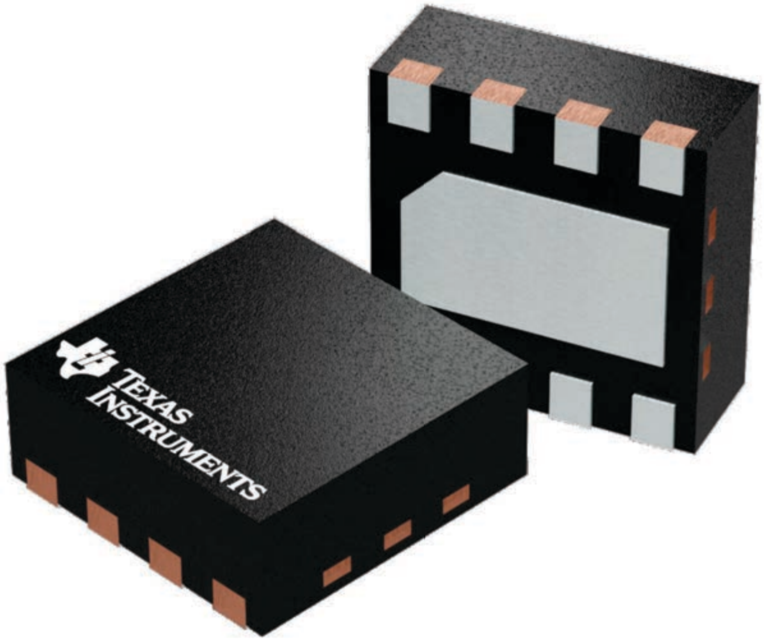
DSG 8

WSON - 0.8 mm max height

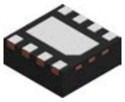
2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



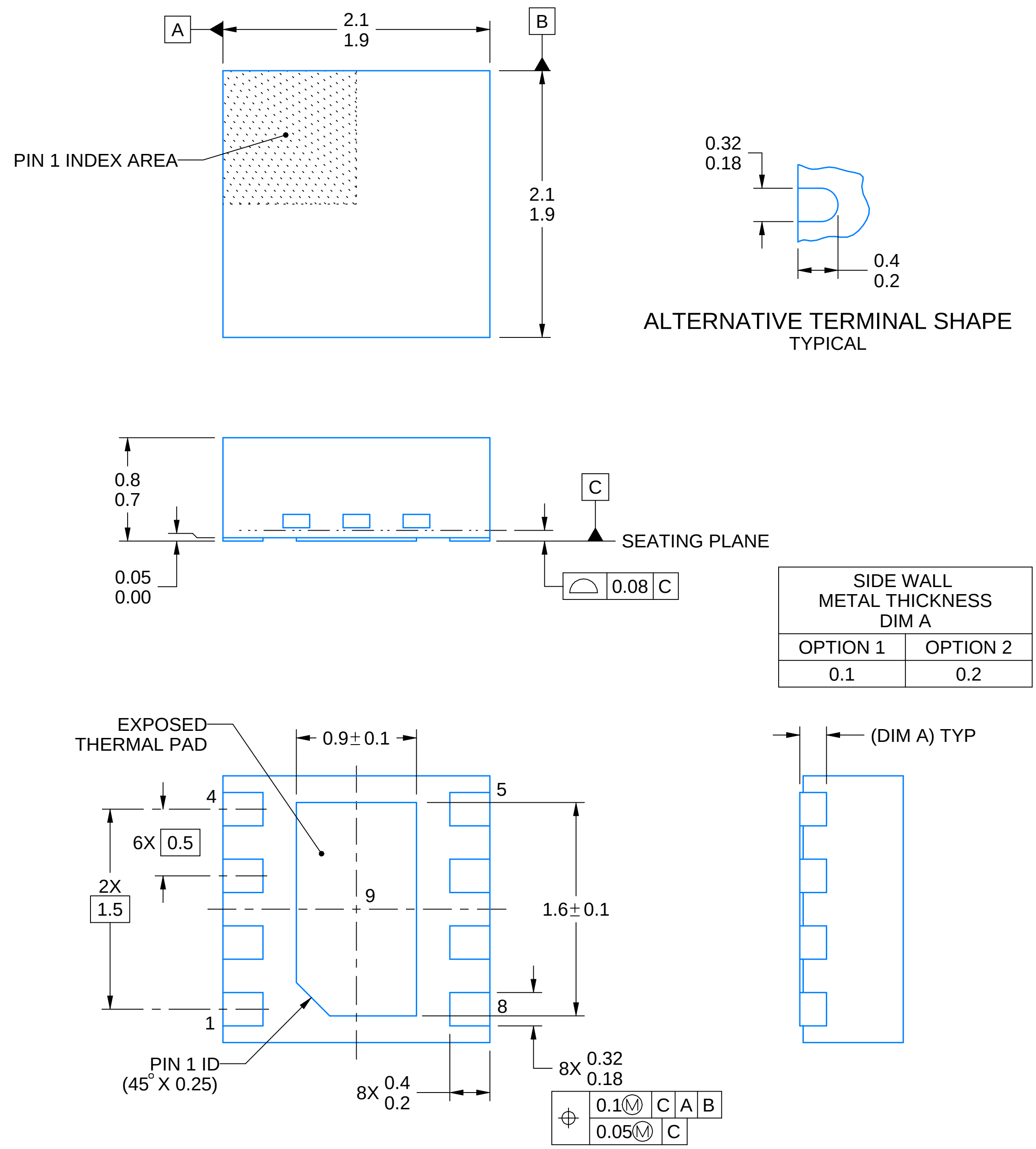
DSG0008A



PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

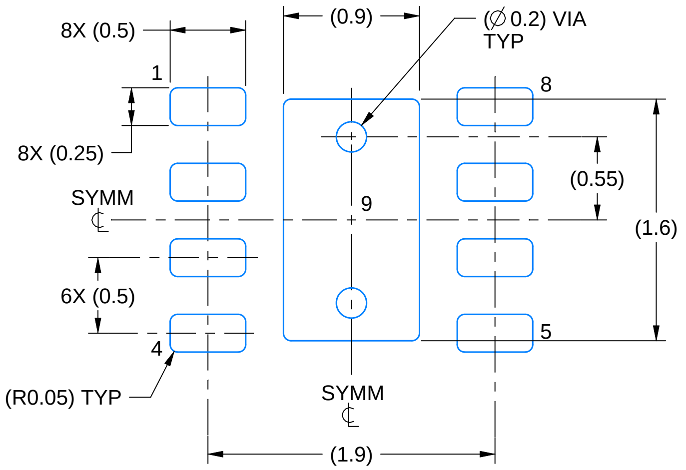


SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

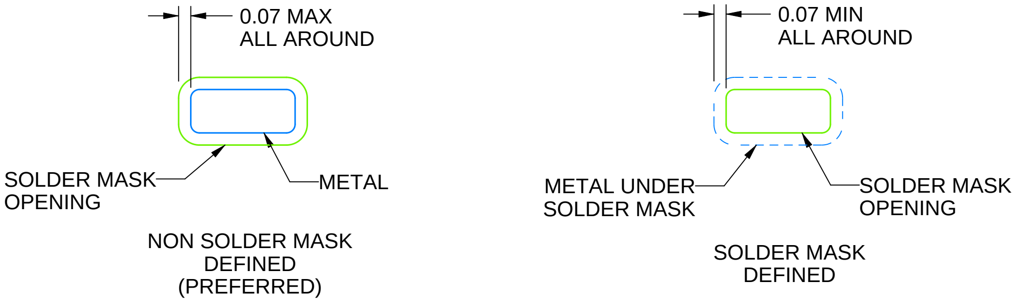
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



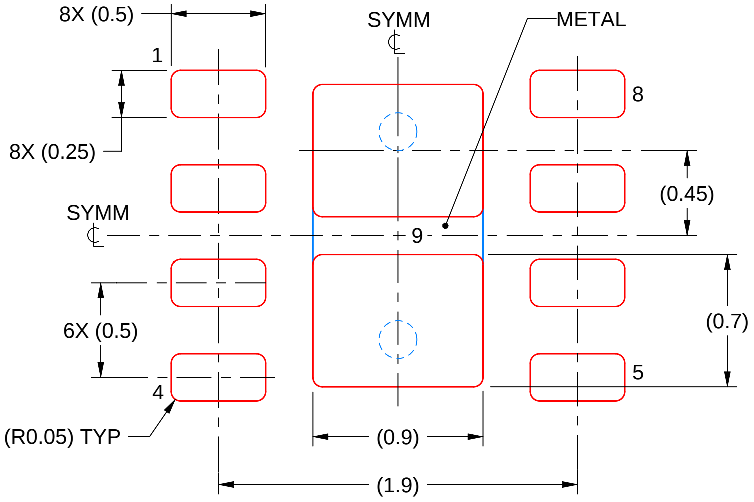
LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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