AMC1306M05-Q1 汽车类高精度 ±50mV 输入增强型隔离式 Δ-Σ 调制器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 温度等级 1：–40°C 至 +125°C，T_A
- 提供功能安全
  - 有助于进行功能安全系统设计的文档
- 线性输入电压范围：±50mV
- 低直流误差：
  - 失调电压误差：±50μV（最大值）
  - 温漂：1μV/°C（最大值）
  - 增益误差：±0.2%（最大值）
  - 增益漂移：±40ppm/°C（最大值）
- 高 CMTI：100kV/μs（最小值）
- 低 EMI：符合 CISPR-11 和 CISPR-25 标准
- 安全相关认证：
  - 符合 DIN VDE V 0884-11 标准的 7070V$_{PEAK}$ 增强型隔离：2017-01
  - 符合 UL1577 标准且长达 1 分钟的 5000V$_{RMS}$ 隔离

2 应用

- 基于分流电阻器的电流感应和隔离式电压测量，包括：
  - 牵引逆变器
  - 车载充电器
  - 直流/直流转换器
  - 混合动力汽车/电动汽车直流充电器

3 说明

AMC1306M05-Q1 是一款精密 Δ-Σ 调制器，此调制器的输出与输入电路由抗电磁干扰性能极强的隔离层隔开。该隔离栅经认证可提供高达 7070V$_{PEAK}$ 的增强型隔离，符合 DIN VDE V 0884-11 和 UL1577 标准，并且可支持最高 1.5kV$_{RMS}$ 的工作电压。该隔离层可将系统中以不同共模电压电平运行的各器件隔开，防止高电压冲击导致低压侧器件电气损坏或对操作员造成伤害。

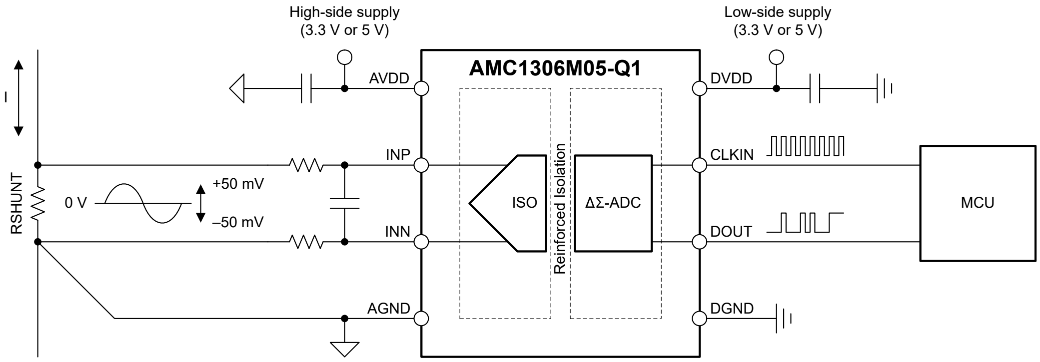
AMC1306M05-Q1 的输入端经过了优化，可直接连接到分流电阻器或其他低电压电平信号源。具有出色的直流精度和低温漂，可支持精确的电流控制，适用于车载充电器 (OBC)、直流/直流转换器、牵引逆变器或其他高压应用。通过使用集成式数字滤波器（如 TMS320F2807x 或 TMS320F2837x 微控制器系列中的滤波器）来抽取位流，该器件可在 78kSPS 数据速率下实现 85dB 动态范围的 16 位分辨率。

AMC1306M05-Q1 采用宽体 8 引脚 SOIC 封装，符合面向汽车应用的 AEC-Q100 标准，并支持 –40°C 至 +125°C 的温度范围。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
AMC1306M05-Q1	SOIC (8)	5.85mm × 7.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型应用

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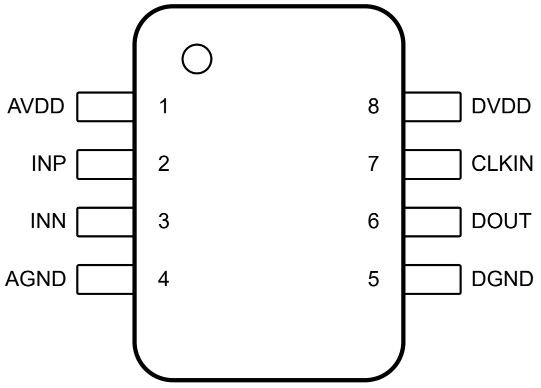
4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
February 2022	*	Initial Release

5 Pin Configuration and Functions



Not to scale

图 5-1. DWV Package, 8-Pin SOIC (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	AVDD	High-side power	Analog (high-side) power supply(1)
2	INP	Analog input	Noninverting analog input
3	INN	Analog input	Inverting analog input
4	AGND	High-side ground	Analog (high-side) ground reference
5	DGND	Low-side ground	Digital (low-side) ground reference
6	DOUT	Digital output	Modulator data output
7	CLKIN	Digital input	Modulator clock input with internal pulldown resistor (typical value: 1.5 MΩ)
8	DVDD	Low-side power	Digital (low-side) power supply(1)

(1) See the *Power Supply Recommendations* section for power-supply decoupling recommendations.

6 Specifications

6.1 Absolute Maximum Ratings

see(1)

PARAMETER		MIN	MAX	UNIT
Power-supply voltage	AVDD to AGND	–0.3	6.5	V
	DVDD to DGND	–0.3	6.5	
Analog input voltage	INP, INN	AGND – 6	AVDD + 0.5V	V
Digital input voltage	CLKIN	DGND – 0.5	DVDD + 0.5	V
Digital output voltage	DOUT	DGND – 0.5	DVDD + 0.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions* . If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1), HBM ESD classification level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011, CDM ESD classification level C6	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
AVDD	Hgh-side power supply	AVDD to AGND	3	5.0	5.5	V
DVDD	Low-side power supply	DVDD to DGND	2.7	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Differential input voltage before clipping output	$V_{IN} = V_{INP} – V_{INN}$		±64		mV
V_{FSR}	Specified linear differential full-scale voltage	$V_{IN} = V_{INP} – V_{INN}$	–50		50	mV
V_{CM}	Operating common-mode input voltage	$(V_{INP} + V_{INN}) / 2$ to AGND	–0.032		AVDD – 2.1	V
DIGITAL I/O						
V_{IO}	Digital input / output voltage		0		VDD	V
f_{CLKIN}	Input clock frequency	4.5 V ≤ AVDD ≤ 5.5 V	5	20	21	MHz
		3.0 V ≤ AVDD ≤ 5.5 V	5	20	20	
t_{HIGH}	Input clock high time		20	25	120	ns
t_{LOW}	Input clock low time		20	25	120	ns
TEMPERATURE RANGE						
T_A	Specified ambient temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		AMC1306M05-Q1 DWV (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	23.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	60.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	AVDD = DVDD = 5.5 V	87	mW
P_{D1}	Maximum power dissipation (high-side supply)	AVDD = 3.6 V	31	mW
		AVDD = 5.5 V	54	
P_{D2}	Maximum power dissipation (low-side supply)	DVDD = 3.6 V	17	mW
		DVDD = 5.5 V	33	

6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance[1]	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External creepage[1]	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 0.021	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN VDE V 0884-11: 2017-01[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	2120	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	1500	V_{RMS}
		At DC voltage	2120	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test)	7070	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test)	8480	
V_{IOSM}	Maximum surge isolation voltage[3]	Test method per IEC 60065, 1.2/50-µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 12800\ V_{PK}$ (qualification)	8000	V_{PK}
q_{pd}	Apparent charge[4]	Method a, after input/output safety test subgroups 2 & 3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output[5]	$V_{IO} = 0.5\ V_{PP}$ at 1 MHz	~1.5	pF
R_{IO}	Insulation resistance, input to output[5]	V_{IO} = 500 V at T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	$> 10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$> 10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5000\ V_{RMS}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6000\ V_{RMS}$, t = 1 s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier are tied together, creating a two-pin device.

6.7 Safety-Related Certifications

VDE	UL
Certified according to DIN VDE V 0884-11 (VDE V 0884-11): 2017-01, DIN EN 60950-1 (VDE 0805 Teil 1): 2014-08, and DIN EN 60065 (VDE 0860): 2005-11	Recognized under 1577 component recognition program
Reinforced insulation	Single protection
Certificate number: pending	File number: pending

Safety Limiting Values

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 112.2°C/W, AVDD = DVDD = 5.5 V, T_J = 150°C, T_A = 25°C			203	mA
		$R_{\theta JA}$ = 112.2°C/W, AVDD = DVDD = 3.6 V, T_J = 150°C, T_A = 25°C			309	mA
P_S	Safety input, output, or total power(1)	$R_{\theta JA}$ = 112.2°C/W, T_J = 150°C, T_A = 25°C			1114	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times AVDD_{max} + I_S \times DVDD_{max}$, where $AVDD_{max}$ is the maximum high-side voltage and $DVDD_{max}$ is the maximum controller-side supply voltage.

6.8 Electrical Characteristics

minimum and maximum specifications are at T_A = –40°C to 125°C, AVDD = 3.0 V to 5.5 V, DVDD = 2.7 V to 5.5 V, INP = –50 mV to 50 mV, INN = 0 V, and sinc^3 filter with OSR = 256 (unless otherwise noted); typical specifications are at T_A = 25°C, CLKIN = 20 MHz, AVDD = 5 V, and DVDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
V_{CMov}	Commonmode overvoltage detection level	(INP + INN) / 2 to AGND	AVDD – 2			V
C_{IN}	Single-ended input capacitance	INN = AGND		4		pF
C_{IND}	Differential input capacitance			2		pF
R_{IN}	Single-ended input resistance	INN = AGND		4.75		kΩ
R_{IND}	Differential input resistance			4.9		kΩ
I_{IB}	Input bias current	INP = INN = AGND, $I_{IB} = I_{BP} + I_{BN}$	–97	–72	–57	µA
I_{IO}	Input offset current			±10		nA
CMTI	Common-mode transient immunity		100	150		kV/µs
CMRR	Common-mode rejection ratio	INP = INN, f_{IN} = 0 Hz, $V_{CM\ min} \le V_{IN} \le V_{CM\ max}$		–99		dB
		INP = INN, f_{IN} from 0.1 Hz to 50 kHz, $V_{CM\ min} \le V_{IN} \le V_{CM\ max}$		–98		
BW	Input bandwidth			800		kHz
DC ACCURACY						
DNL	Differential nonlinearity	Resolution: 16 bits	–0.99		0.99	LSB
INL	Integral nonlinearity(2)	Resolution: 16 bits, 4.5 V ≤ AVDD ≤ 5.5 V	–4	±1	4	LSB
		Resolution: 16 bits, 3.0 V ≤ AVDD ≤ 3.6 V	–5	±1.5	5	LSB
E_O	Offset error(1)	T_A = 25°C, INP = INN = GND1	–50	±2.5	50	µV
TCE_O	Offset error temperatrure drift(3)		–1	±0.25	1	µV/°C
E_G	Gain error	T_A = 25°C	–0.2%	±0.005%	0.2%	
TCE_G	Gain error temperature drift(4)		–40	±20	40	ppm/°C
PSRR	Power-supply rejection ratio	INP = INN = AGND, AVDD from 3.0 V to 5.5 V, at DC		–108		dB
		INP = INN = AGND, AVDD from 3.0 V to 5.5 V, 10 kHz / 100 mV ripple		–107		
AC ACCURACY						
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz	78	82.5		dB
SINAD	Signal-to-noise + distortion	f_{IN} = 1 kHz	77.5	82.3		dB
THD	Total harmonic distortion(5)	4.5 V ≤ AVDD ≤ 5.5 V, f_{IN} = 1 kHz, 5 MHz ≤ f_{CLKIN} ≤ 21 MHz		–98	–84	dB
		3.0 V ≤ AVDD ≤ 3.6 V, f_{IN} = 1 kHz, 5 MHz ≤ f_{CLKIN} ≤ 20 MHz		–93	–83	
SFDR	Spurious-free dynamic range	f_{IN} = 1 kHz	83	100		dB

6.8 Electrical Characteristics (continued)

minimum and maximum specifications are at T_A = –40°C to 125°C, AVDD = 3.0 V to 5.5 V, DVDD = 2.7 V to 5.5 V, INP = –50 mV to 50 mV, INN = 0 V, and sinc^3 filter with OSR = 256 (unless otherwise noted); typical specifications are at T_A = 25°C, CLKIN = 20 MHz, AVDD = 5 V, and DVDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMOS LOGIC WITH SCHMITT-TRIGGER						
I_{IN}	Input current	DGND ≤ V_{IN} ≤ DVDD	0		7	μA
C_{IN}	Input capacitance			4		pF
V_{IH}	High-level input voltage		0.7 × DVDD		DVDD + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 × DVDD	V
C_{LOAD}	Output load capacitance			30		pF
V_{OH}	High-level output voltage	I_{OH} = –4 mA	DVDD – 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA			0.4	V
POWER SUPPLY						
I_{AVDD}	High-side supply current	3.0 V ≤ AVDD ≤ 3.6 V		6.3	8.5	mA
		4.5 V ≤ AVDD ≤ 5.5 V		7.2	9.8	
I_{DVDD}	Low-side supply current	2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		3.3	4.8	mA
		4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 15 pF		3.9	6.0	
$AVDD_{UV}$	High-side undervoltage detection threshold	AVDD rising	2.45	2.7	2.9	V
		AVDD falling	2.4	2.6	2.8	
$DVDD_{UV}$	Low-side undervoltage detection threshold	DVDD rising	2.2	2.45	2.65	V
		DVDD falling	1.75		2.2	

(1) This parameter is input referred.

(2) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified linear full-scale range FSR.

(3) Offset error temperature drift is calculated using the box method, as described by the following equation: $TCE_O = (E_{O,MAX} – E_{O,MIN}) / TempRange$ where $E_{O,MAX}$ and $E_{O,MIN}$ refer to the maximum and minimum E_O values measured within the temperature range (–40 to 125℃).

(4) Gain error temperature drift is calculated using the box method, as described by the following equation: $TCE_G\ (ppm) = ((E_{G,MAX} - E_{G,MIN}) / TempRange) \times 10^4$ where $E_{G,MAX}$ and $E_{G,MIN}$ refer to the maximum and minimum E_G values (in %) measured within the temperature range (–40 to 125℃).

(5) THD is the ratio of the rms sum of the amplitudes of first five higher harmonics to the amplitude of the fundamental.

Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_H	DOUT hold time after rising edge of CLKIN	C_{LOAD} = 15 pF	3.5			ns
t_D	Rising edge of CLKIN to DOUT valid delay	C_{LOAD} = 15 pF			15	ns
t_r	DOUT rise time	10% to 90%, 2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		2.5	6	ns
		10% to 90%, 4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 15 pF		3.2	6	
t_f	DOUT fall time	10% to 90%, 2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		2.2	6	ns
		10% to 90%, 4.5 V ≤ DVDD ≤ 5.5 V,C_{LOAD} = 15 pF		2.9	6	
t_{START}	Device start-up time	AVDD step from 0 to 3.0 V with DVDD ≥ 2.7 V to bitstream valid, 0.1% settling		0.5		ms

6.9 Timing Diagrams

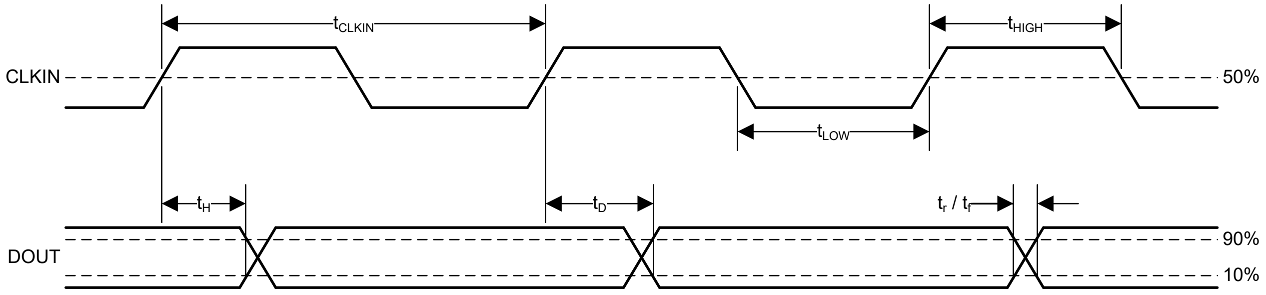


图 6-1. Digital Interface Timing

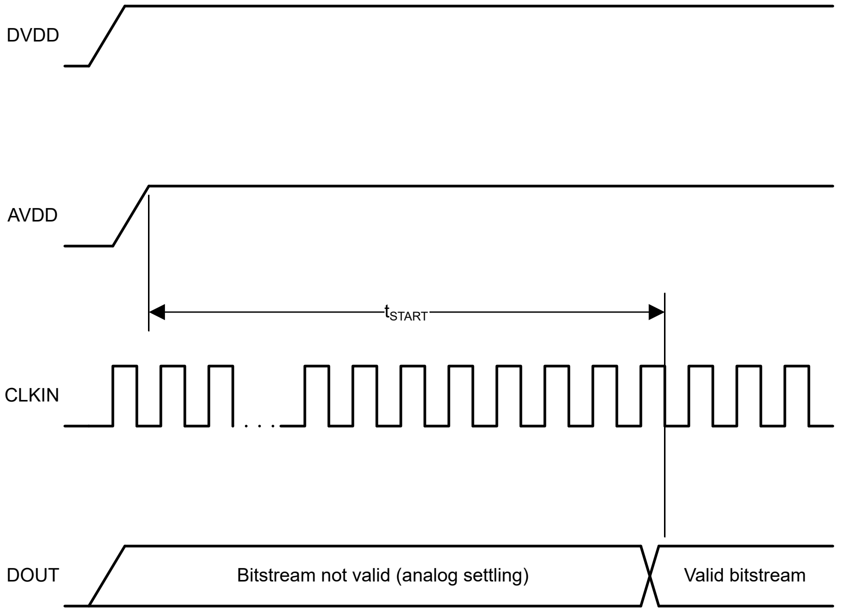


图 6-2. Device Start-Up Timing

6.10 Insulation Characteristics Curves

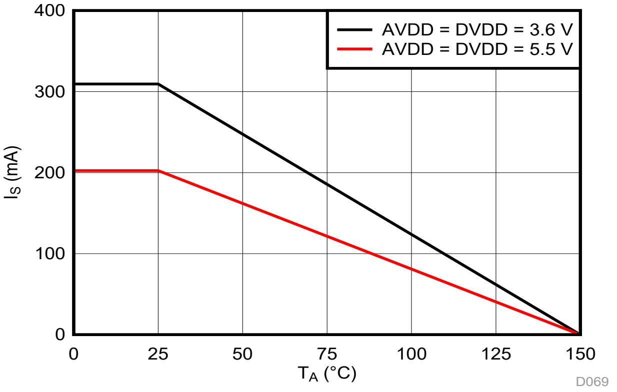


图 6-3. Thermal Derating Curve for Safety-Limiting Current per VDE

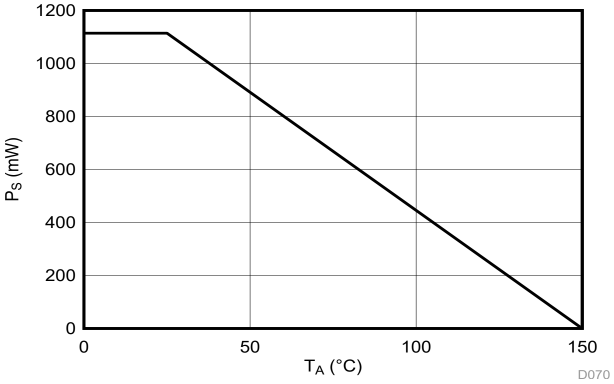
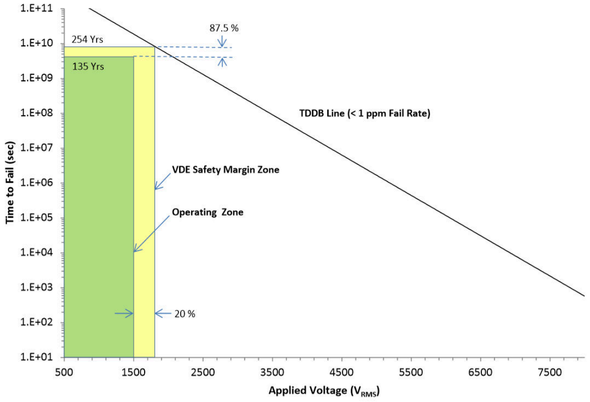


图 6-4. Thermal Derating Curve for Safety-Limiting Power per VDE



T_A up to 150°C, stress-voltage frequency = 60 Hz, isolation working voltage = 1500 V_{RMS}, operating lifetime = 135 years

图 6-5. Reinforced Isolation Capacitor Lifetime Projection

6.11 Typical Characteristics

at AVDD = 5 V, DVDD = 3.3 V, INP = –50 mV to 50 mV , INN = AGND, f_{CLKIN} = 20 MHz, and $sinc^3$ filter with OSR = 256 (unless otherwise noted)

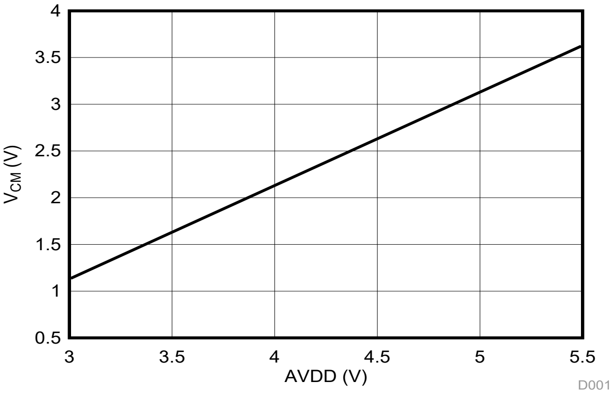


图 6-6. Maximum Operating Common-Mode Input Voltage vs High-Side Supply Voltage

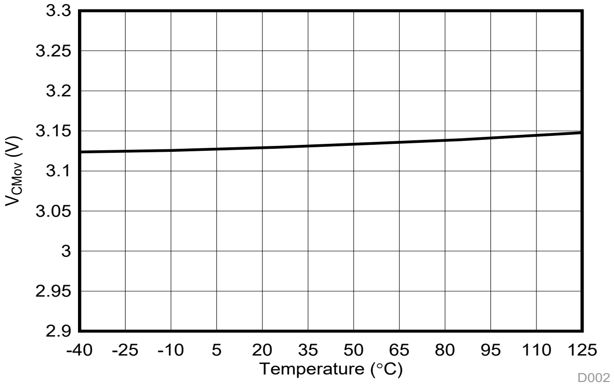


图 6-7. Common-Mode Overvoltage Detection Level vs Temperature

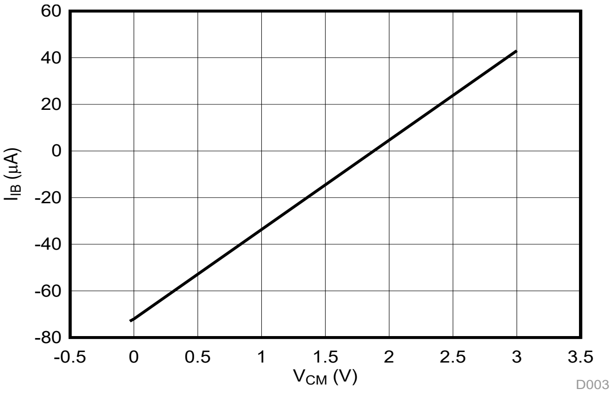


图 6-8. Input Bias Current vs Common-Mode Input Voltage

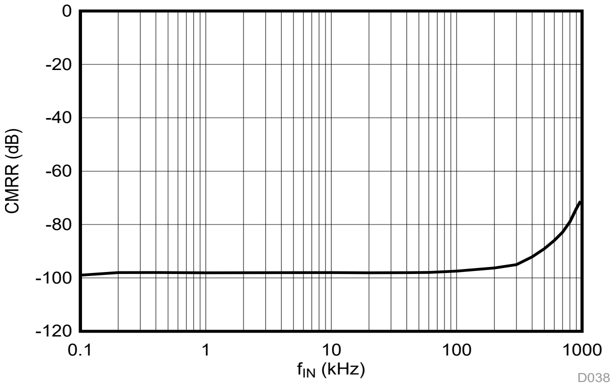


图 6-9. Common-Mode Rejection Ratio vs Input Signal Frequency

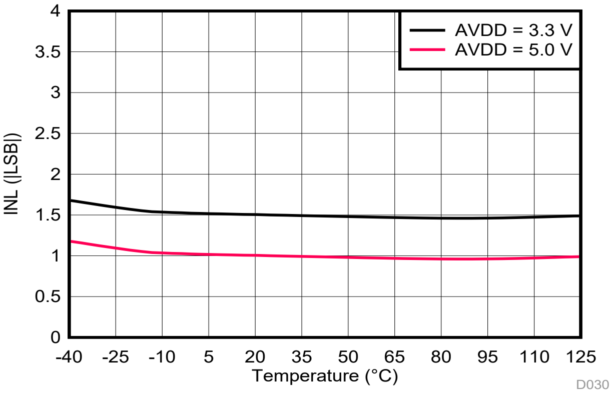


图 6-10. Integral Nonlinearity vs Temperature

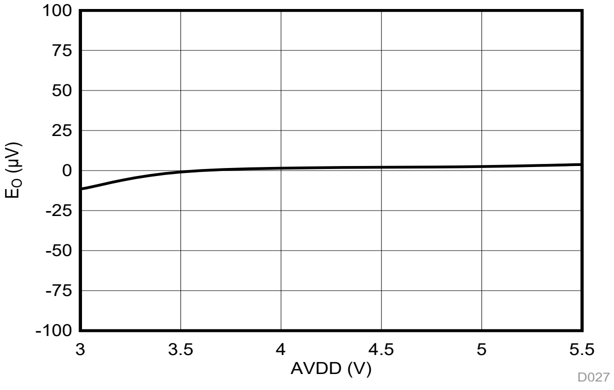


图 6-11. Offset Error vs High-Side Supply Voltage

6.11 Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, INP = –50 mV to 50 mV , INN = AGND, f_{CLKIN} = 20 MHz, and $sinc^3$ filter with OSR = 256 (unless otherwise noted)

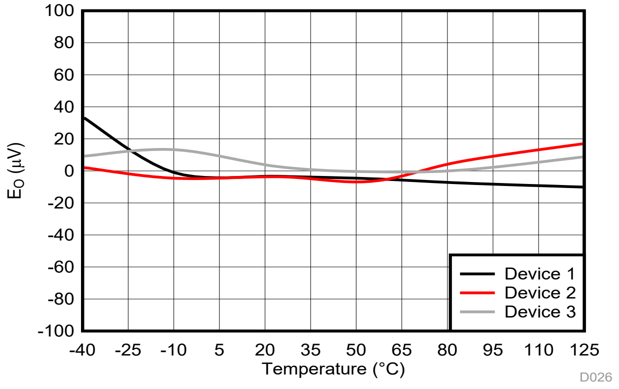


图 6-12. Offset Error vs Temperature

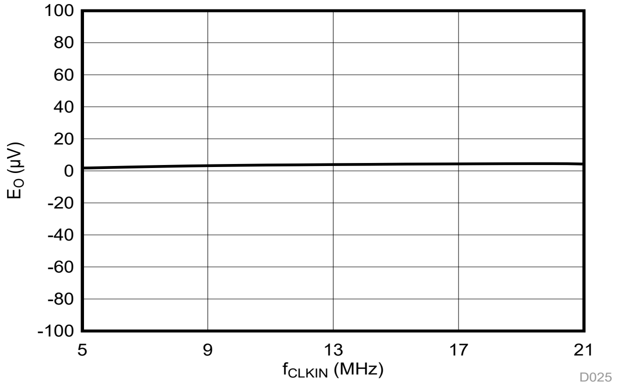


图 6-13. Offset Error vs Clock Frequency

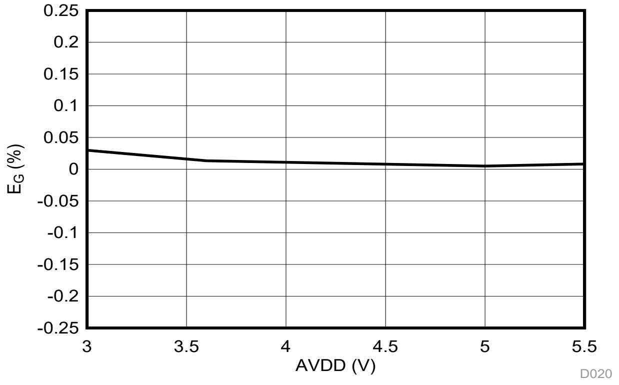


图 6-14. Gain Error vs High-Side Supply Voltage

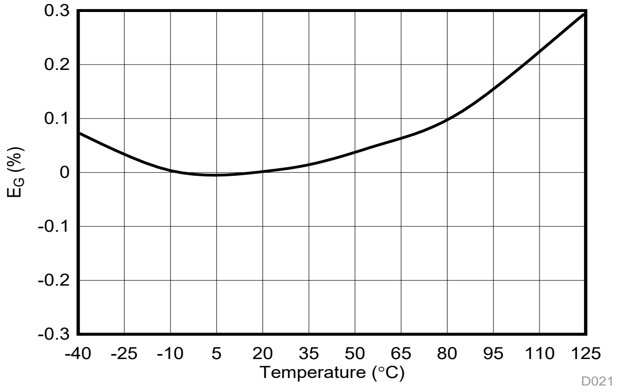


图 6-15. Gain Error vs Temperature

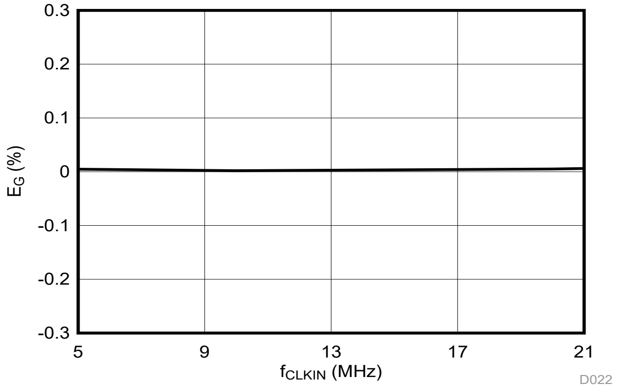


图 6-16. Gain Error vs Clock Frequency

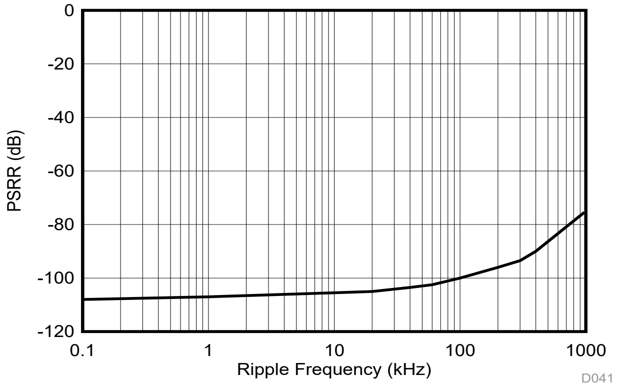


图 6-17. Power-Supply Rejection Ratio vs Ripple Frequency

6.11 Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, INP = –50 mV to 50 mV , INN = AGND, f_{CLKIN} = 20 MHz, and $sinc^3$ filter with OSR = 256 (unless otherwise noted)

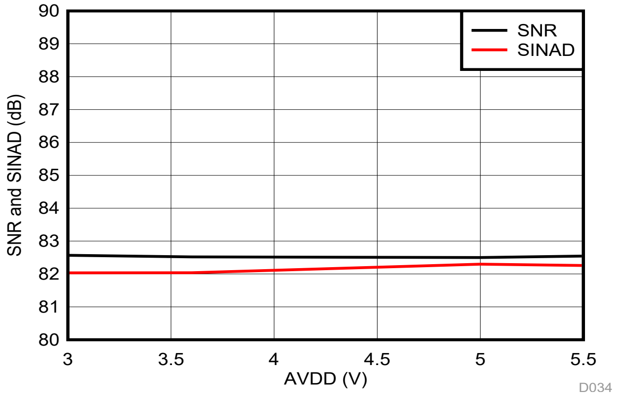


图 6-18. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs High-Side Supply Voltage

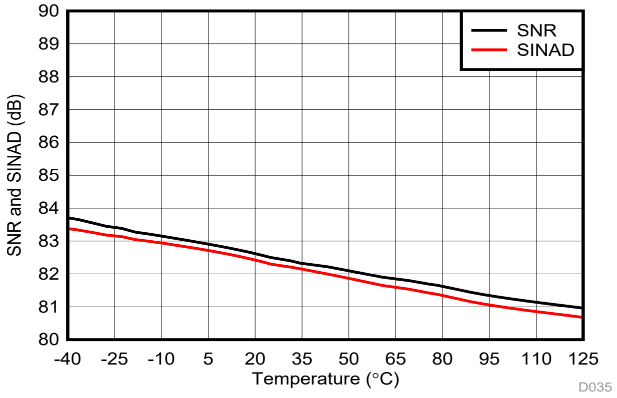


图 6-19. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Temperature

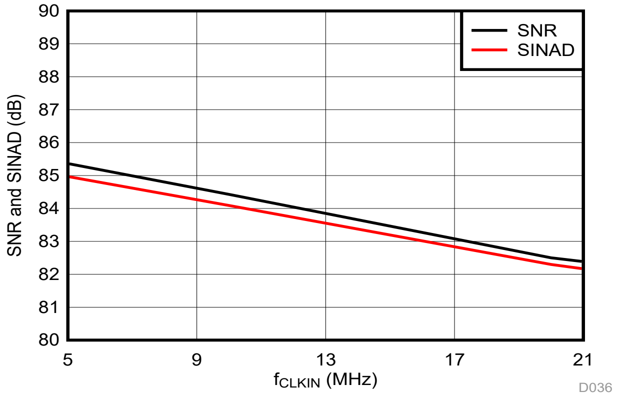


图 6-20. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Clock Frequency

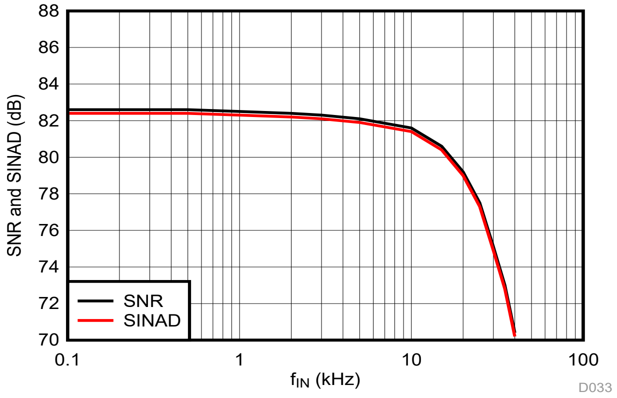


图 6-21. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Frequency

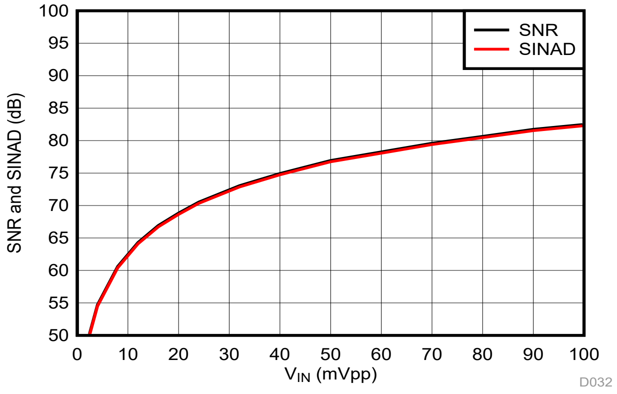
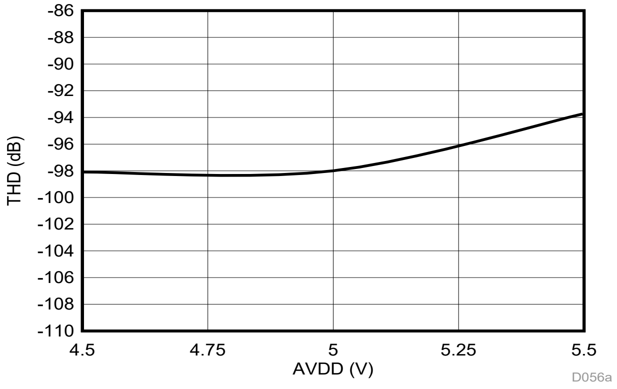


图 6-22. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Amplitude

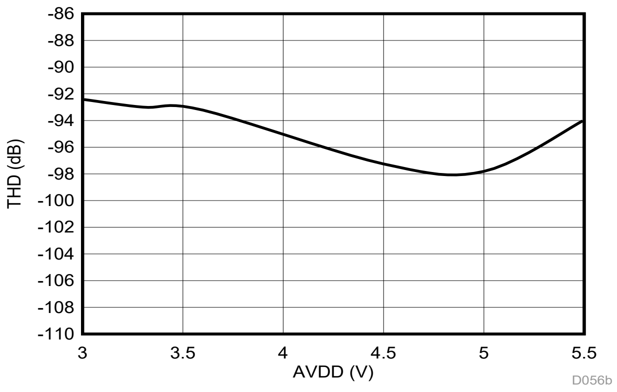


f_{CLKIN} = 21 MHz

图 6-23. Total Harmonic Distortion vs High-Side Supply Voltage (5 V, nom)

6.11 Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, INP = –50 mV to 50 mV , INN = AGND, f_{CLKIN} = 20 MHz, and sinc^3 filter with OSR = 256 (unless otherwise noted)



f_{CLKIN} = 20 MHz

图 6-24. Total Harmonic Distortion vs High-Side Supply Voltage (3.3 V, nom)

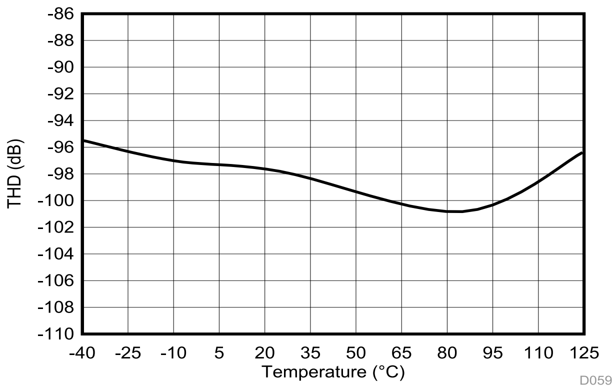


图 6-25. Total Harmonic Distortion vs Temperature

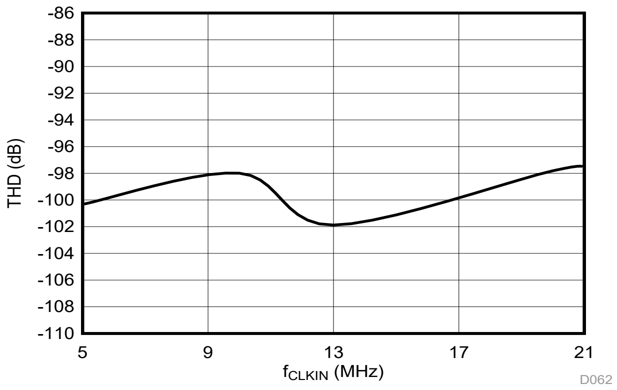


图 6-26. Total Harmonic Distortion vs Clock Frequency

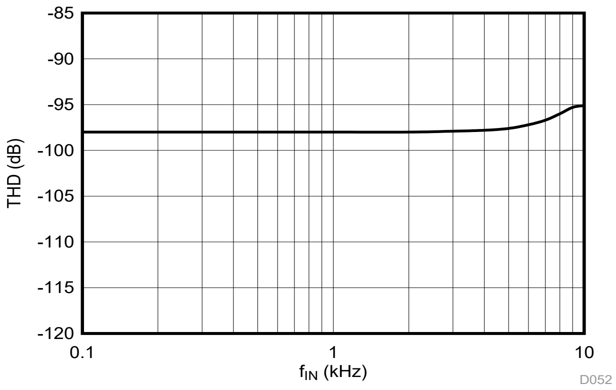


图 6-27. Total Harmonic Distortion vs Input Signal Frequency

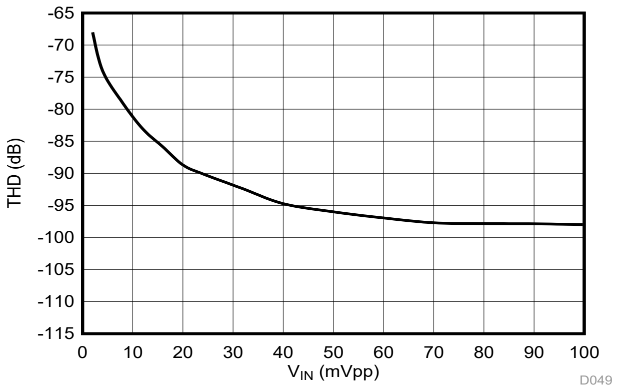


图 6-28. Total Harmonic Distortion vs Input Signal Amplitude

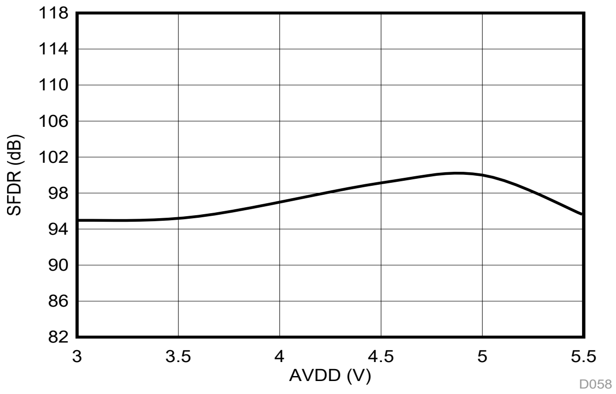


图 6-29. Spurious-Free Dynamic Range vs High-Side Supply Voltage

6.11 Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, INP = –50 mV to 50 mV , INN = AGND, f_{CLKIN} = 20 MHz, and $sinc^3$ filter with OSR = 256 (unless otherwise noted)

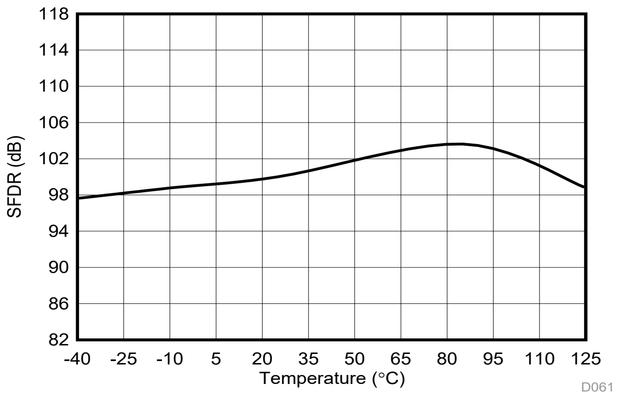


图 6-30. Spurious-Free Dynamic Range vs Temperature

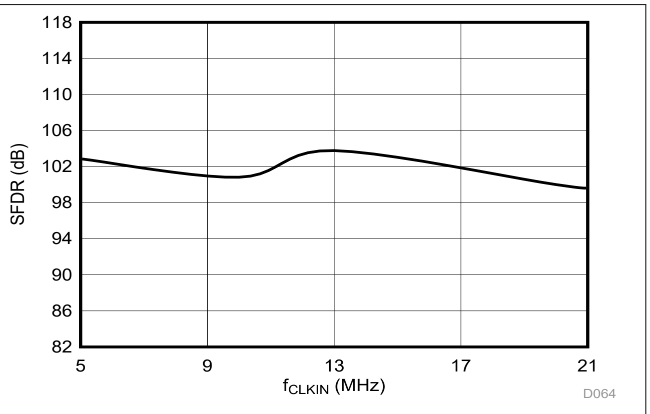


图 6-31. Spurious-Free Dynamic Range vs Clock Frequency

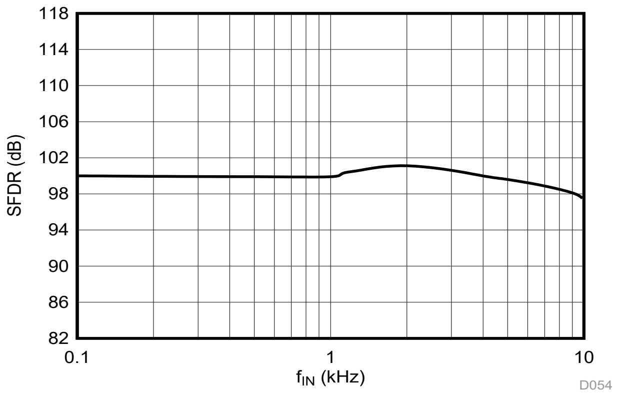


图 6-32. Spurious-Free Dynamic Range vs Input Signal Frequency

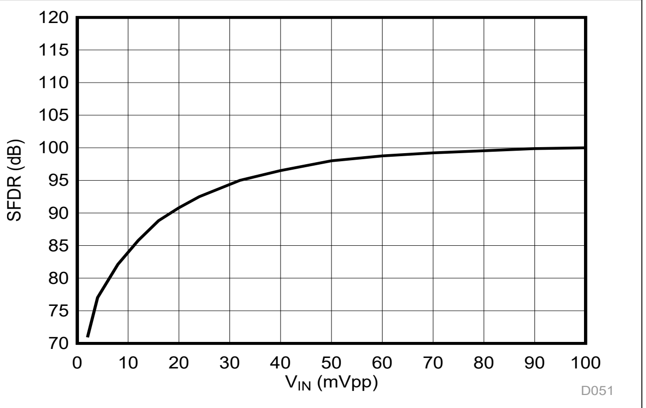
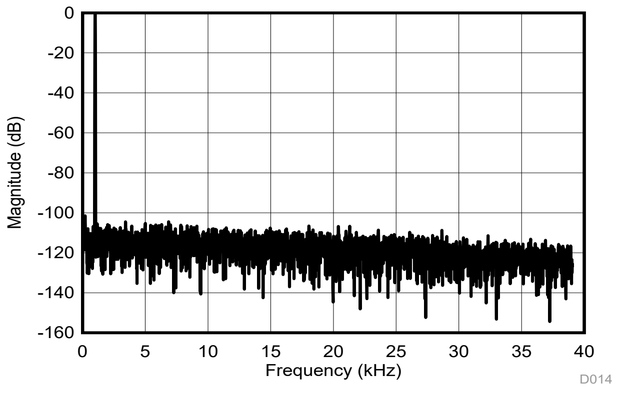
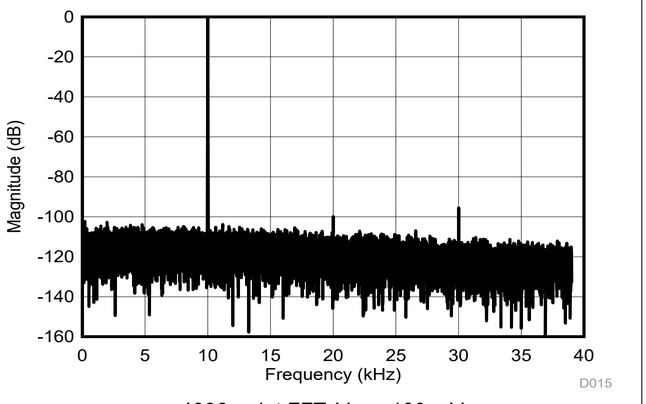


图 6-33. Spurious-Free Dynamic Range vs Input Signal Amplitude



4096-point FFT, V_{IN} = 100 mV_{PP}

图 6-34. Frequency Spectrum With 1-kHz Input Signal



4096-point FFT, V_{IN} = 100 mV_{PP}

图 6-35. Frequency Spectrum With 10-kHz Input Signal

6.11 Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, INP = –50 mV to 50 mV , INN = AGND, f_{CLKIN} = 20 MHz, and sinc^3 filter with OSR = 256 (unless otherwise noted)

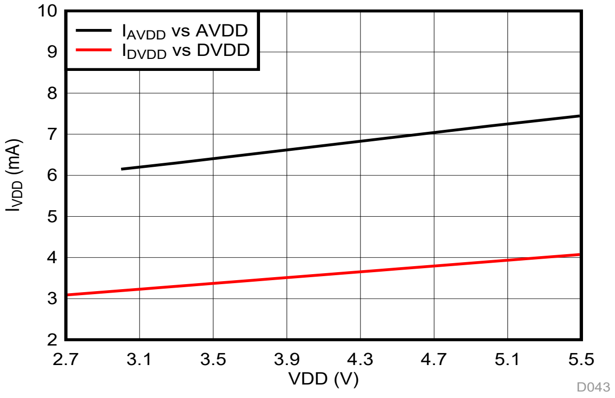


图 6-36. Supply Current vs Supply Voltage

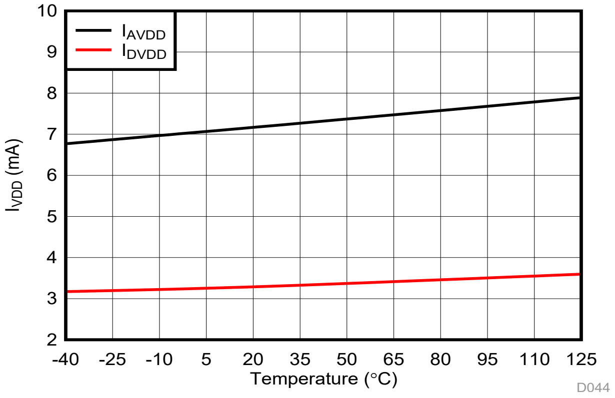


图 6-37. Supply Current vs Temperature

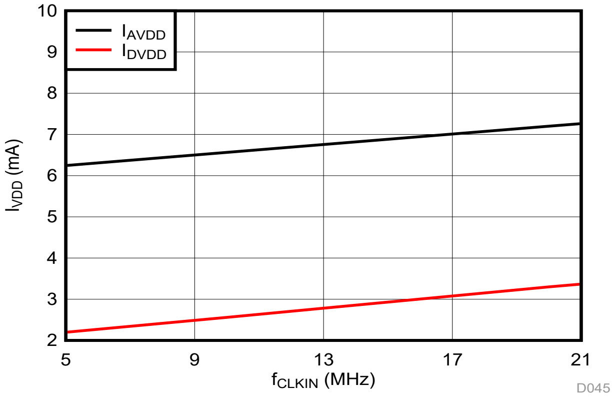


图 6-38. Supply Current vs Clock Frequency

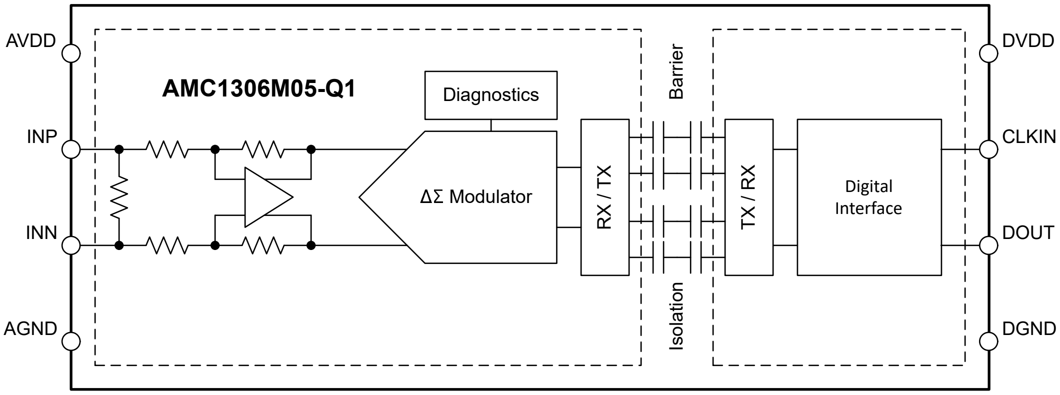
7 Detailed Description

7.1 Overview

The input stage of the AMC1306M05-Q1 consists of a fully differential amplifier that feeds the switched-capacitor input of a second-order, delta-sigma (ΔΣ) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier that separates the high-side from the low-side. The isolated data output DOUT of the converter provides a stream of digital ones and zeros that is synchronous to the externally provided clock source at the CLKIN pin. The time average of this serial bitstream output is proportional to the analog input voltage. The external clock input simplifies the synchronization of multiple current-sensing channels on the system level.

The silicon-dioxide (SiO_2) based capacitive isolation barrier supports a high level of magnetic field immunity as described in the *ISO72x Digital Isolator Magnetic-Field Immunity* application report. The digital modulation used in the AMC1306M05-Q1 to transmit data across the isolation barrier, and the isolation barrier characteristics itself, result in high reliability and common-mode transient immunity.

7.2 Functional Block Diagram

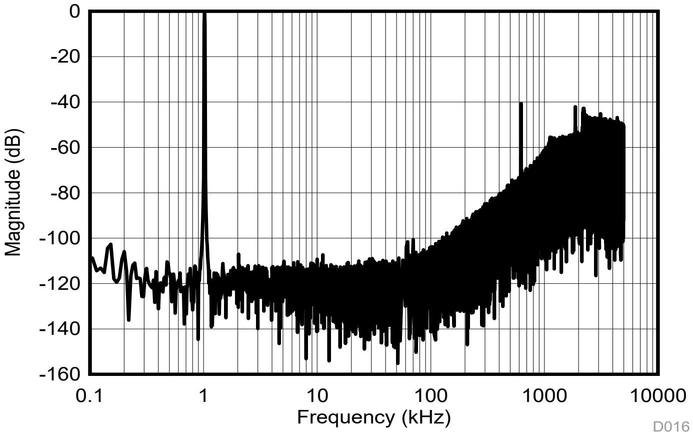


7.3 Feature Description

7.3.1 Analog Input

The differential amplifier input stage of the AMC1306M05-Q1 feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The gain of the differential amplifier is set by internal precision resistors with a differential input impedance of R_{IND}. The modulator converts the analog input signal into a bitstream that is transferred across the isolation barrier, as described in the *Isolation Channel Signal Transmission* section.

For reduced offset and offset drift, the differential amplifier is chopper-stabilized with the switching frequency set at f_{CLKIN} / 32. As shown in 图 7-1, the switching frequency generates a spur at 625 kHz.



sinc^3 filter, OSR = 2, f_{CLKIN} = 20 MHz, f_{IN} = 1 kHz

图 7-1. Quantization Noise Shaping

There are two restrictions on the analog input signals INP and INN. First, if the input voltages V_{INP} or V_{INN} exceed the range specified in the *Absolute Maximum Ratings* table, the input currents must be limited to the absolute maximum value because the electrostatic discharge (ESD) protection turns on. In addition, the linearity and parametric performance of the device are ensured only when the analog input voltage remains within the linear full-scale range (V_{FSR}) and within the common-mode input voltage range (V_{CM}) as specified in the *Recommended Operating Conditions* table.

7.3.2 Modulator

图 7-2 conceptualizes the second-order, switched-capacitor, feed-forward ΔΣ modulator implemented in the AMC1306M05-Q1. The analog input voltage V_{IN} and the output V_5 of the 1-bit digital-to-analog converter (DAC) are differentiated, providing an analog voltage V_1 at the input of the first integrator stage. The output of the first integrator feeds the input of the second integrator stage, resulting in output voltage V_3 that is differentiated with the input signal V_{IN} and the output of the first integrator V_2. Depending on the polarity of the resulting voltage V_4, the output of the comparator is changed. In this case, the 1-bit DAC responds on the next clock pulse by changing the associated analog output voltage V_5, causing the integrators to progress in the opposite direction, and forcing the value of the integrator output to track the average value of the input.

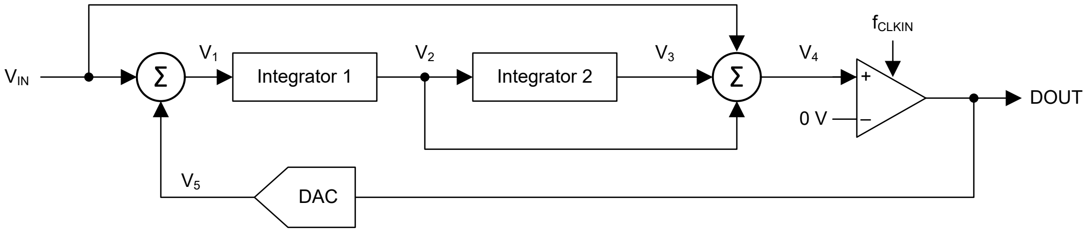


图 7-2. Block Diagram of a Second-Order Modulator

The modulator shifts the quantization noise to high frequencies, as illustrated in 图 7-1. Therefore, use a low-pass digital filter at the output of the device to increase the overall performance. This filter is also used to convert the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). TI's C2000™ and Sitara™ microcontroller families offer a suitable programmable, hardwired filter structure termed a *sigma-delta filter module* (SDFM) optimized for usage with the AMC1306M05-Q1. Alternatively, a field-programmable gate array (FPGA) or complex programmable logic device (CPLD) can be used to implement the filter.

7.3.3 Isolation Channel Signal Transmission

The AMC1306M05-Q1 uses an on-off keying (OOK) modulation scheme, as shown in 图 7-3, to transmit the modulator output bitstream across the SiO_2-based isolation barrier. The transmit driver (TX) shown in the *Functional Block Diagram* transmits an internally generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC1306M05-Q1 is 480 MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and produces the output. The AMC1306M05-Q1 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and lowest level of radiated emissions caused by the high-frequency carrier and RX/TX buffer switching.

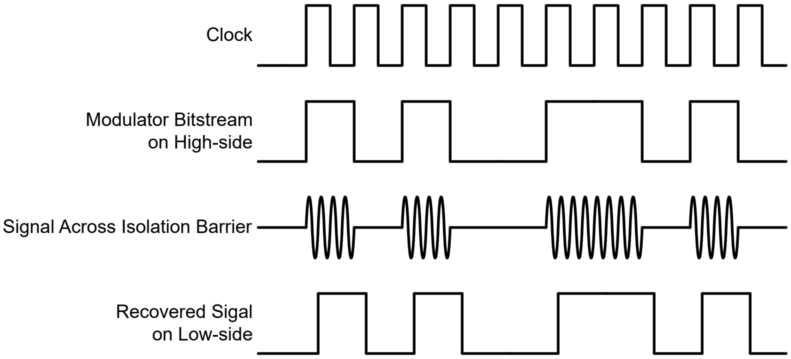


图 7-3. OOK-Based Modulation Scheme

7.3.4 Digital Output

A differential input signal of 0 V ideally produces a stream of ones and zeros that are high 50% of the time. A differential input of 50 mV produces a stream of ones and zeros that are high 89.06% of the time. With 16 bits of resolution, that percentage ideally corresponds to code 58368. A differential input of –50 mV produces a stream of ones and zeros that are high 10.94% of the time and ideally results in code 7168 with 16-bit resolution. These input voltages are also the specified linear range of the AMC1306M05-Q1. If the input voltage value exceeds this range, the output of the modulator shows nonlinear behavior as the quantization noise increases. The output of the modulator clips with a constant stream of zeros with an input less than or equal to –64 mV or with a constant stream of ones with an input greater than or equal to 64 mV. In this case, however, the AMC1306M05-Q1 generates a single 1 (if the input is at negative full-scale) or 0 (if the input is at positive full-scale) every 128 clock cycles to indicate proper device function (see the *Output Behavior in Case of a Full-Scale Input* section for more details). 图 7-4 shows the input voltage versus the output modulator signal.

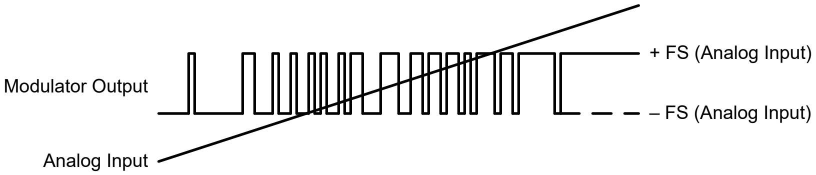


图 7-4. AMC1306M05-Q1 Modulator Output vs Analog Input

The density of ones in the output bitstream can be calculated using 方程式 1 for any input voltage ($V_{IN} = V_{INP} - V_{INN}$) value with the exception of a full-scale input signal, as described in 方程式 1:

$$\rho = \frac{V_{IN} + V_{Clipping}}{2 \times V_{Clipping}} \tag{1}$$

7.3.4.1 Output Behavior in Case of a Full-Scale Input

If a full-scale input signal is applied to the AMC1306M05-Q1 (that is, $|V_{IN}| \geq |V_{Clipping}|$), the device generates a single one or zero every 128 bits at DOUT, as shown in 图 7-5, depending on the actual polarity of the signal being sensed. In this way, differentiating between a missing AVDD and a full-scale input signal is possible on the system level.

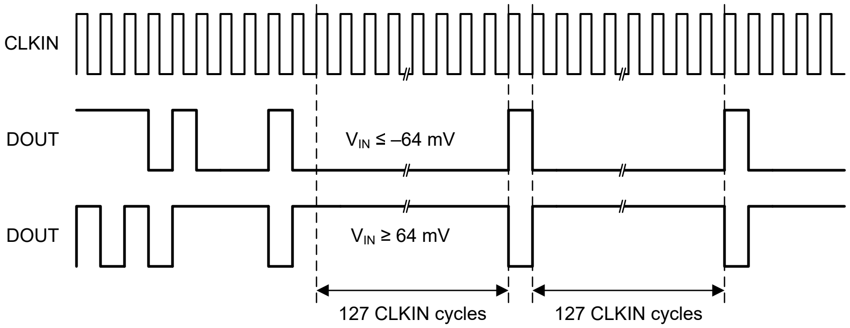


图 7-5. Output of the AMC1306M05-Q1 in Case of an Input Overrange

7.3.4.2 Output Behavior in Case of Input Common-Mode Overrange

If INN or INP is disconnected from the shunt resistor, the input bias current of the AMC1306M05-Q1 drives the disconnected terminal towards the positive supply rail, and the common-mode input voltage increases. A similar effect happens when there is no DC current path between INN, INP, and HGND. If the input common-mode voltage exceeds the common-mode overvoltage detection threshold V_{CMov}, the device provides a constant bitstream of logic 1's at the output, as shown in 图 7-6; that is, DOUT is permanently high. A zero is not generated every 128 clock pulses, which differentiates this condition from a valid positive full-scale input. This feature is useful to identify interconnect problems on the board.

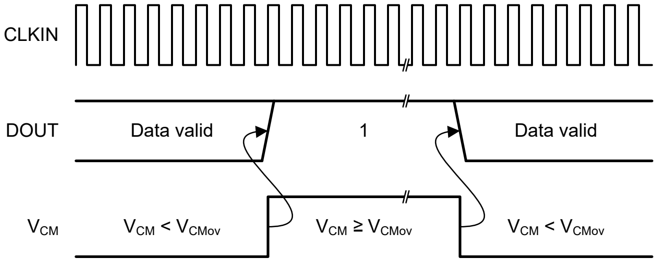


图 7-6. Output of the AMC1306M05-Q1 in Case of a Common-Mode Overvoltage

There is no common-mode overvoltage detection in the negative direction; thus, if the common-mode input voltage is below the minimum V_{CM} value specified in the *Recommended Operating Conditions* table, the bitstream at the DOUT output is not determined.

7.3.4.3 Output Behavior in Case of a Missing High-Side Supply

If the high-side supply is missing, the device provides a constant bitstream of logic 0's at the output, as shown in 图 7-7; that is, DOUT is permanently low. A one is not generated every 128 clock pulses, which differentiates this condition from a valid negative full-scale input. This feature is useful to identify high-side power-supply problems on the board.

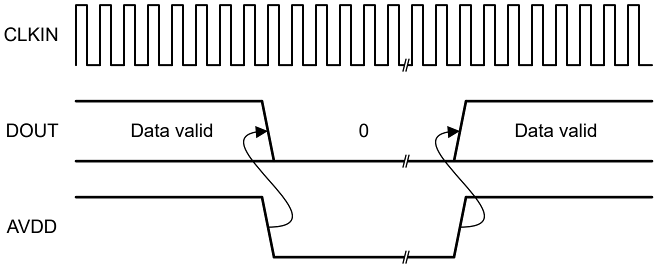


图 7-7. Output of the AMC1306M05-Q1 in Case of a Missing High-Side Supply

7.4 Device Functional Modes

The AMC1306M05-Q1 is operational when the power supplies AVDD and DVDD are applied as specified in the *Recommended Operating Conditions* table.

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The low analog input voltage range, excellent accuracy, and low temperature drift make the AMC1306M05-Q1 a high-performance solution for automotive applications where shunt-based current sensing in the presence of high common-mode voltage levels is required.

8.2 Typical Application

The AMC1306M05-Q1 is ideally suited for shunt-based, current-sensing applications where accurate current monitoring is required in the presence of high common-mode voltages.

图 8-1 shows the AMC1306M05-Q1 in a typical application. The load current flowing through an external shunt resistor RSHUNT produces a voltage drop that is sensed by the AMC1306M05-Q1. The AMC1306M05-Q1 digitizes the analog input signal on the high-side, transfers the data across the isolation barrier to the low-side, and outputs the digital bitstream on the DOUT pin. The 5-V high-side power supply (AVDD) is generated from the floating gate driver supply using a resistor (R4) and a Zener diode (D1).

The differential input, digital output, and the high common-mode transient immunity (CMTI) of the AMC1306M05-Q1 ensure reliable and accurate operation even in high-noise environments.

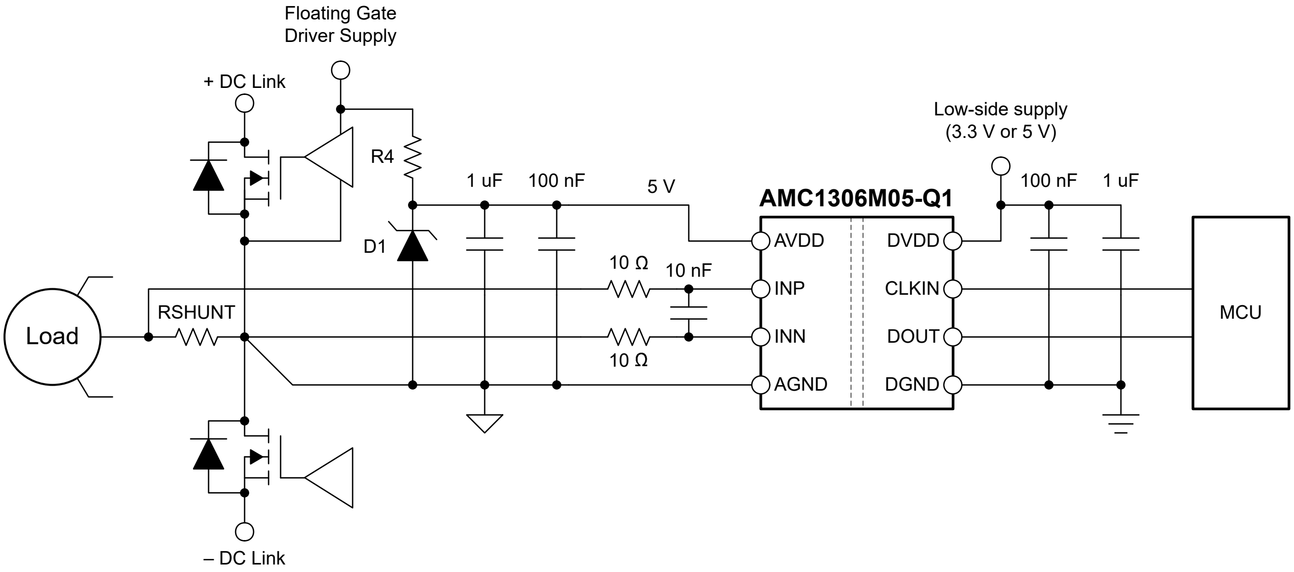


图 8-1. Using the AMC1306M05-Q1 for Current Sensing in a Typical Application

8.2.1 Design Requirements

表 8-1 lists the parameters for this typical application.

表 8-1. Design Requirements

PARAMETER	VALUE
High-side supply voltage	3.3 V or 5 V
Low-side supply voltage	3.3 V or 5 V
Voltage drop across RSHUNT for a linear response	±50 mV (maximum)

8.2.2 Detailed Design Procedure

In 图 8-1, the high-side power supply (AVDD) for the AMC1306M05-Q1 is derived from the floating power supply of the upper gate driver, using a resistor (R4) and a Zener diode (D1).

The floating ground reference (AGND) is derived from the end of the shunt resistor that is connected to the negative input of the AMC1306M05-Q1 (INN). If a four-pin shunt is used, the inputs of the AMC1306M05-Q1 are connected to the inner leads and AGND is connected to the outer lead on the INN-side of the shunt. To minimize offset and improve accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor rather than shorting AGND to INN directly at the input to the device. See the *Layout* section for more details.

8.2.2.1 Shunt Resistor Sizing

Use Ohm's Law to calculate the voltage drop across the shunt resistor (V_{SHUNT}) for the desired measured current: V_{SHUNT} = I × RSHUNT.

Consider the following two restrictions when selecting the value of the shunt resistor, RSHUNT:

- The voltage drop caused by the nominal current range must not exceed the recommended differential input voltage range for a linear response: $|V_{SHUNT}| \le |V_{FSR}|$
- The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $|V_{SHUNT}| \le |V_{Clipping}|$

8.2.2.2 Input Filter Design

Place an RC filter in front of the isolated amplifier to improve signal-to-noise performance of the signal path. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (f_{CLKIN}) of the ΔΣ modulator
- The input bias current does not generate significant voltage drop across the DC impedance of the input filter
- The impedances measured from the analog inputs are equal

For most applications, the structure shown in 图 8-2 achieves excellent performance.

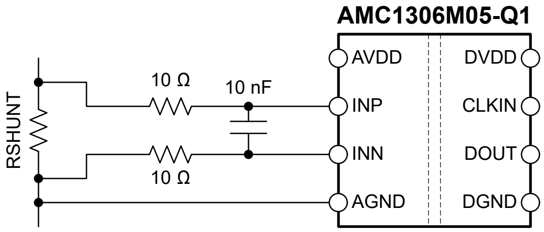


图 8-2. Differential Input Filter

8.2.2.3 Bitstream Filtering

The modulator generates a bitstream that is processed by a digital filter to obtain a digital word similar to a conversion result of a conventional analog-to-digital converter (ADC). As described by 方程式 2, a very simple filter built with minimal effort and hardware, is a sinc^3-type filter:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}}\right)^3 \quad (2)$$

This filter provides the best output performance at the lowest hardware size (count of digital gates) for a second-order modulator. All characterization in this document is also done with a sinc^3 filter with an oversampling ratio (OSR) of 256 and an output word width of 16 bits, unless specified otherwise. The measured effective number of bits (ENOB) as a function of the OSR is illustrated in 图 8-3 of the *Typical Application* section.

A *Delta Sigma Modulator Filter Calculator* is available for download at www.ti.com that aids in the filter design and selecting the right OSR and filter order to achieve the desired output resolution and filter response time.

An example code for implementing a sinc^3 filter in an FPGA is discussed in the *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications* application note, available for download at www.ti.com.

For modulator output bitstream filtering, a device from TI's C2000™ or Sitara™ microcontroller families is recommended. These families support up to eight channels of dedicated hardwired filter structures that significantly simplify system level design by offering two filtering paths per channel: one providing high-accuracy results for the control loop and one fast-response path for overcurrent detection.

A *delta sigma modulator filter calculator* is available for download at www.ti.com that aids in the filter design and selecting the right OSR and filter order to achieve the desired output resolution and filter response time.

8.2.3 Application Curve

The effective number of bits (ENOB) is often used to compare the performance of ADCs and ΔΣ modulators. 图 8-3 shows the ENOB of the AMC1306M05-Q1 with different oversampling ratios. By using 方程式 3, this number can also be calculated from the SINAD:

$$SINAD = 1.76\,dB + 6.02\,dB \times ENOB \quad (3)$$

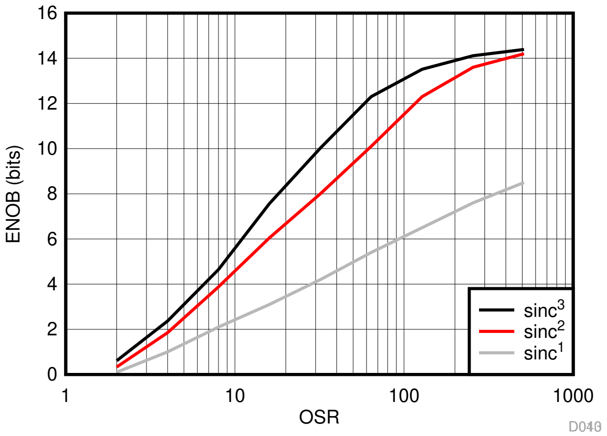


图 8-3. Measured Effective Number of Bits vs Oversampling Ratio

8.3 What to Do and What Not to Do

Do not leave the inputs of the AMC1306M05-Q1 unconnected (floating) when the device is powered up. If the device inputs are left floating, the input bias current may drive the inputs to a positive value that exceeds the operating common-mode input voltage and DOUT is permanently high as described in the *Output Behavior in Case of Input Common-Mode Overrange* section.

Connect the high-side ground (AGND) to INN, either by a hard short or through a resistive path. A DC current path between INN and AGND is required to define the input common-mode voltage. Take care not to exceed the input common-mode range as specified in the *Recommended Operating Conditions* table. For best accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor rather than shorting AGND to INN directly at the input to the device. See the *Layout* section for more details.

9 Power Supply Recommendations

The AMC1306M05-Q1 does not require any specific power-up sequencing. The high-side power supply (AVDD) is decoupled with a low-ESR, 100-nF capacitor (C1) parallel to a low-ESR, 1-µF capacitor (C2). The low-side power supply (DVDD) is equally decoupled with a low-ESR, 100-nF capacitor (C3) parallel to a low-ESR, 1-µF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible.

The ground reference for the high-side (AGND) is derived from the end of the shunt resistor that is connected to the negative input (INN) of the device. For best DC accuracy, use a separate trace to make this connection instead of shorting AGND to INN directly at the device input. If a four-terminal shunt is used, the device inputs are connected to the inner leads and AGND is connected to the outer lead on the INN-side of the shunt. 图 9-1 shows a decoupling diagram of the AMC1306M05-Q1.

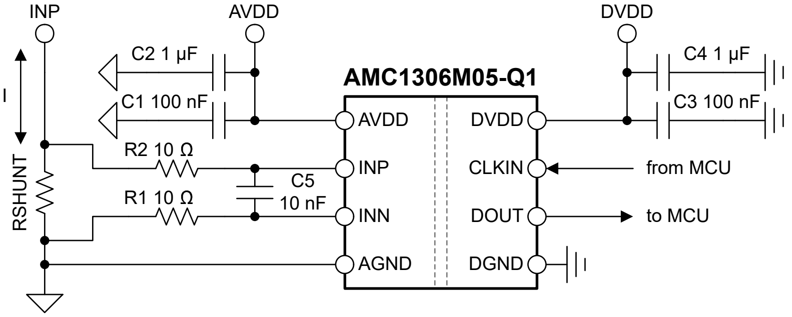


图 9-1. Decoupling of the AMC1306M05-Q1

Capacitors must provide adequate effective capacitance under the applicable DC bias conditions they experience in the application. Multilayer ceramic capacitors (MLCC) typically exhibit only a fraction of their nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

10 Layout

10.1 Layout Guidelines

图 10-1 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC1306M05-Q1 supply pins) and placement of the other components required by the device. For best performance, place the shunt resistor close to the INP and INN inputs of the AMC1306M05-Q1 and keep the layout of both connections symmetrical.

10.2 Layout Example

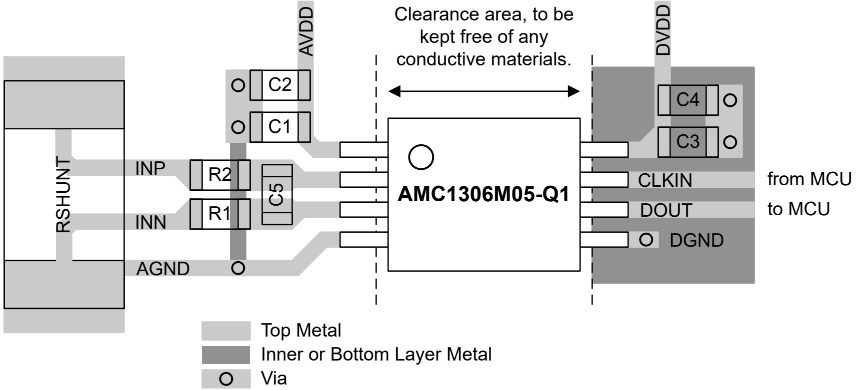


图 10-1. Recommended Layout of the AMC1306M05-Q1

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Isolation Glossary* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application report
- Texas Instruments, *Delta Sigma Modulator Filter Calculator* design tool

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.4 Trademarks

C2000™, Sitara™, and TI E2E™ are trademarks of Texas Instruments.
所有商标均为其各自所有者的财产。

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AMC1306M05QDWVRQ1	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306M05Q
AMC1306M05QDWVRQ1.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306M05Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

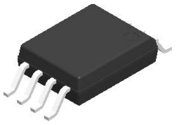
OTHER QUALIFIED VERSIONS OF AMC1306M05-Q1 :

- Catalog : AMC1306M05

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

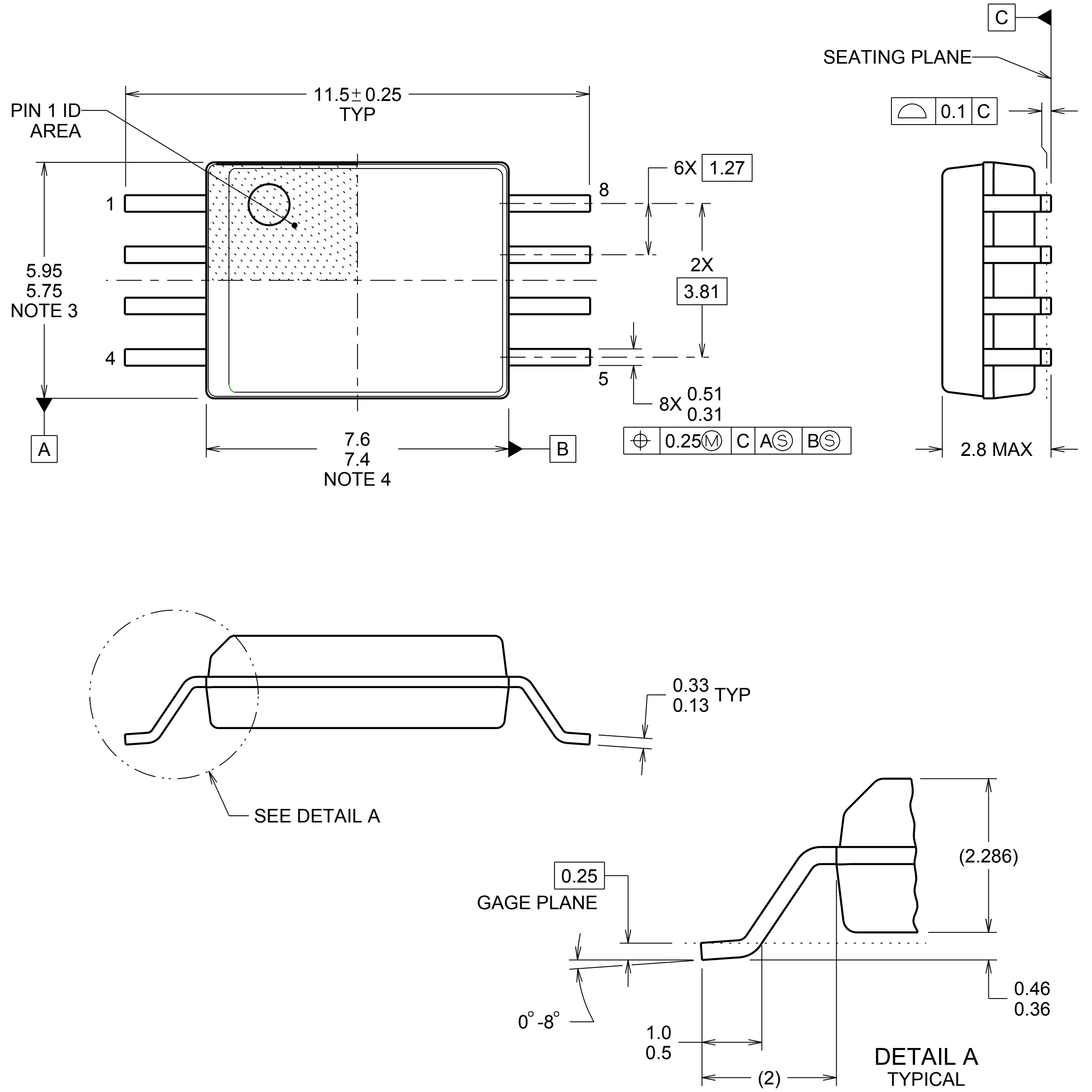
PACKAGE OUTLINE



DWV0008A

SOIC - 2.8 mm max height

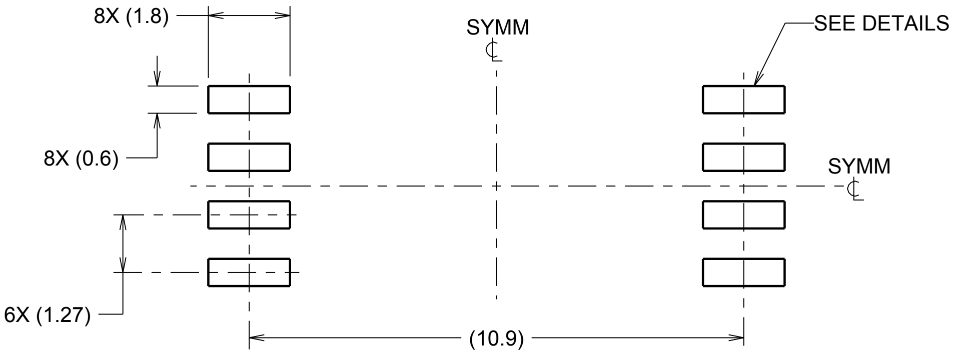
SOIC



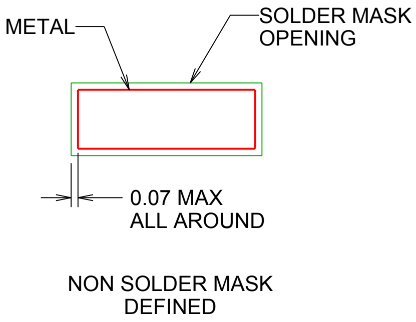
4218796/A 09/2013

NOTES:

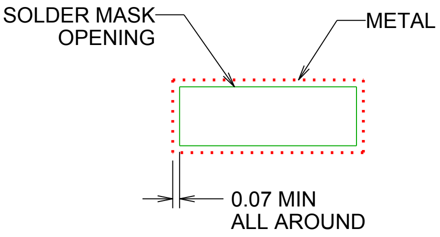
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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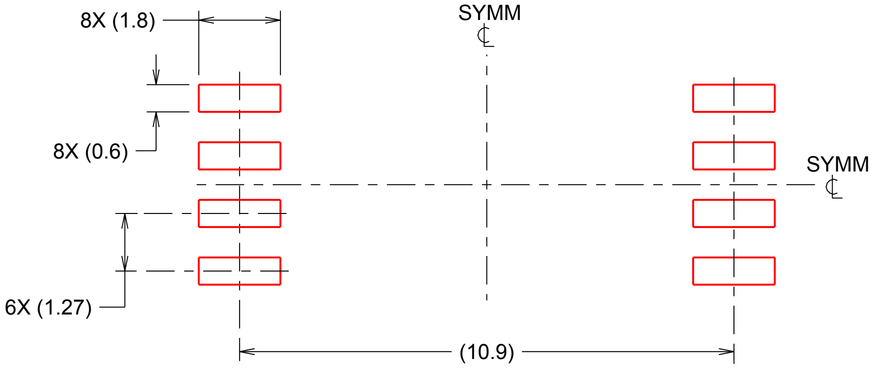
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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