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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

| Changes from Revision A (December 2011) to Revision B | Page |
|--|-------------|
| • 已删除 删除了封装/订购信息 表；请参阅数据表末尾的封装选项附录 | 1 |
| • Deleted <i>ESD specifications</i> from Absolute Maximum Ratings table. Moved to separate ESD Ratings table. | 6 |
| • Moved content from <i>Application and Implementation</i> | 23 |
| • Deleted references to Tx PGA calibration in <i>Calibration Modes</i> | 41 |
| • Deleted reference to Tx PGA calibration in <i>Table 15</i> | 44 |
| • Deleted <i>Packaging/Mechanicals</i> section; information appended to end of data sheet | 52 |

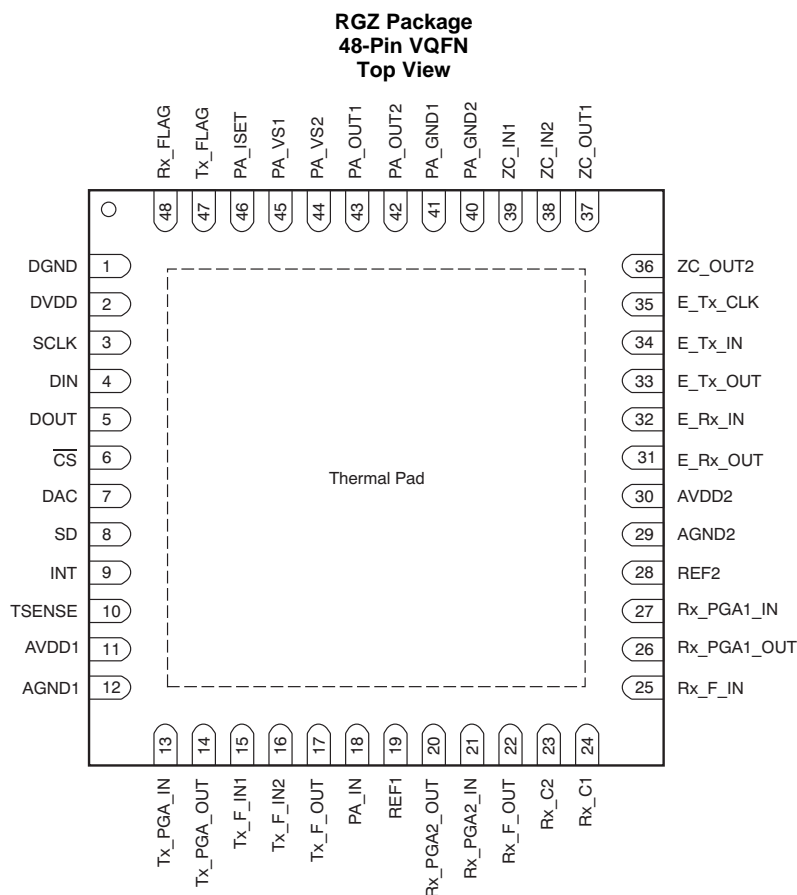
| Changes from Original (December 2011) to Revision A | Page |
|---|-------------|
| • 已更改 将产品状态更改为“生产数据” | 1 |
| • Added cross-reference to footnote 2 to <i>Output short-circuit (PA)</i> parameter in Absolute Maximum Ratings table | 6 |

5 说明（续）

AFE030在过温和短路情况下收到内部保护。它还提供一个可调节电流限值。提供一个中断输出用于标示电流限值和热界限。还有一个关断引脚，此引脚用于快速将此器件置于最低功率的状态下。通过此四线制串行外设接口，或者 SPI™，每一个功能块可以开启或者关闭以优化功率耗散。

AFE030采用耐热增强型，表面贴装PowerPAD封装方式(QFN-48)。额定工作拓展工业结温范围为-40°C至+125°C。

6 Pin Configuration and Functions



Pin Functions

| PIN | | I/O | DESCRIPTION |
|----------|-----|-----|---|
| NAME | NO. | | |
| AGND1 | 12 | — | Analog ground |
| AGND2 | 29 | — | Analog ground |
| AVDD1 | 11 | — | Analog supply |
| AVDD2 | 30 | — | Analog supply |
| CS | 6 | — | SPI digital chip select |
| DAC | 7 | — | DAC mode select |
| DIN | 4 | I | SPI digital input |
| DGND | 1 | — | Digital ground |
| DOUT | 5 | O | SPI digital output |
| DVDD | 2 | — | Digital supply |
| E_Rx_IN | 32 | I | Two-wire receiver input |
| E_Rx_OUT | 31 | O | Two-wire receiver output |
| E_Tx_CLK | 35 | I | Two-wire transmitter clock input |
| E_Tx_IN | 34 | I | Two-wire transmitter input |
| E_Tx_OUT | 33 | O | Two-wire transmitter output |
| INT | 9 | — | Interrupt on overcurrent or thermal limit |
| PA_GND1 | 41 | — | Power amplifier ground |
| PA_GND2 | 40 | — | Power amplifier ground |

Pin Functions (continued)

| PIN | | I/O | DESCRIPTION |
|-------------|-----|-----|--|
| NAME | NO. | | |
| PA_IN | 18 | I | Power amplifier input |
| PA_ISET | 46 | — | Power amplifier current limit set |
| PA_OUT1 | 43 | O | Power amplifier output |
| PA_OUT2 | 42 | O | Power amplifier output |
| PA_VS1 | 45 | — | Power amplifier supply |
| PA_VS2 | 44 | — | Power amplifier supply |
| REF1 | 19 | — | Power amplifier noise reducing capacitor |
| REF2 | 28 | — | Receiver noise reducing capacitor |
| Rx_C1 | 24 | — | Receiver external frequency select |
| Rx_C2 | 23 | — | Receiver external frequency select |
| Rx_F_IN | 25 | I | Receiver filter input |
| Rx_F_OUT | 22 | O | Receiver filter output |
| Rx_FLAG | 48 | — | Receiver ready flag |
| Rx PGA1_IN | 27 | I | Receiver PGA(1) input |
| Rx PGA1_OUT | 26 | O | Receiver PGA(1) output |
| Rx PGA2_IN | 21 | I | Receiver PGA(2) input |
| Rx PGA2_OUT | 20 | O | Receiver PGA(2) output |
| SCLK | 3 | — | SPI serial clock |
| SD | 8 | — | System shutdown |
| TSENSE | 10 | — | Temp sensing diode (anode) |
| Tx_F_IN1 | 15 | I | Transmit filter input 1 |
| Tx_F_IN2 | 16 | I | Transmit filter input 2 |
| Tx_F_OUT | 17 | O | Transmit filter output |
| Tx_FLAG | 47 | — | Transmitter ready flag |
| Tx_PGA_IN | 13 | I | Transmit PGA input |
| Tx_PGA_OUT | 14 | O | Transmit PGA output |
| ZC_IN1 | 39 | I | Zero-crossing detector input |
| ZC_IN2 | 38 | I | Zero-crossing detector input |
| ZC_OUT1 | 37 | O | Zero-crossing detector output |
| ZC_OUT2 | 36 | O | Zero-crossing detector output |

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | | MIN | MAX | UNIT |
|-------------|--|---|--------------|-------------------------|------|
| Voltage | Supply voltage, PA_V _S | | 26 | | V |
| | Signal input terminals | Pins 18,19 ⁽²⁾ | PA_GND – 0.4 | PA_V _S + 0.4 | |
| | | Pins 13, 15, 16, 21, 23-25, 28, 32, 34, 35, 38, 39, 46 ⁽²⁾ | AGND – 0.4 | AV _{DD} + 0.4 | |
| | | Pins 3, 4, 6, 7, 8 ⁽²⁾ | DGND – 0.4 | DV _{DD} + 0.4 | |
| | Voltage limit | Pin 27 | –10 | 10 | |
| | Supply voltage | AV _{DD} | 5.5 | | |
| | | DV _{DD} | 5.5 | | |
| Current | Signal input terminals | Pins 18,19 ⁽²⁾ | –10 | 10 | mA |
| | | Pins 13, 15, 16, 21, 23-25, 28, 32, 34, 35, 38, 39, 46 ⁽²⁾ | –10 | 10 | |
| | | Pins 3, 4, 6, 7, 8 ⁽²⁾ | –10 | 10 | |
| | Signal output terminals | Pins 5, 9, 14, 17, 20, 22, 26, 31, 33, 36, 37, 47, 48 ⁽²⁾ | Continuous | | |
| | Output short circuit (PA) | Pins 42, 43 | Continuous | | |
| | Current limit | Pin 10 ⁽²⁾⁽³⁾⁽⁴⁾ | –10 | 10 | |
| Temperature | Operating, T _A ⁽⁴⁾ | | –40 | 150 | °C |
| | Junction, T _J | | 150 | | |
| | Storage, T _{stg} | | –55 | 125 | |

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.4 V beyond the supply rails should be current limited to 10 mA or less. Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.4 V beyond the supply rails should be current limited to 10 mA or less.
- (3) Short-circuit to ground.
- (4) The AFE030 automatically goes into shutdown at junction temperatures that exceed 165°C.

7.2 ESD Ratings

| | | VALUE | UNIT |
|--|--|-------|------|
| V _(ESD) Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | 3000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | 500 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | AFE030 | UNIT |
|-------------------------------|--|------------|------|
| | | RGZ (VQFN) | |
| | | 48 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 27.8 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 12.1 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 7.5 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 0.4 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 7.4 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 1.7 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.4 Electrical Characteristics: Transmitter (Tx), Tx_DAC

At $T_J = 25^\circ\text{C}$, $PA_V_S = 16\text{ V}$, $V_{AVDD} = V_{DVDD} = 3.3\text{ V}$, and PA_ISET (pin 46) connected to ground, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|--|----------------------------|-----|-----------------|------|
| Output range | | GND + 0.1 | | $AV_{DD} - 0.1$ | V |
| Resolution | 1024 steps, 10-bit DAC | | 3.2 | | mV |
| THD | Total harmonic distortion at 62.5 kHz ⁽¹⁾ | Second-harmonic distortion | –73 | | dB |
| | | Third-harmonic distortion | –56 | | dB |
| | | Fourth-harmonic distortion | –94 | | dB |
| Data rate | | | 1.5 | | MSPS |

(1) Total harmonic distortion measured at output of Tx_PGA configured in a gain of 1 V/V with an amplitude of 3 V_{PP}, at a 1-MHz sample rate.

7.5 Electrical Characteristics: Transmitter (Tx), Tx_PGA

At $T_J = 25^\circ\text{C}$, $PA_V_S = 16\text{ V}$, $V_{AVDD} = V_{DVDD} = 3.3\text{ V}$, and PA_ISET (pin 46) connected to ground, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------|---|---|-------|-----------------|-----------------------|
| INPUT | | | | | |
| Input voltage range | | GND – 0.1 | | $AV_{DD} + 0.1$ | V |
| R_I | Input resistance | $G = 1\text{ V/V}$ | 58 | | k Ω |
| | | $G = 0.707\text{ V/V}$ | 68 | | k Ω |
| | | $G = 0.5\text{ V/V}$ | 77 | | k Ω |
| | | $G = 0.25\text{ V/V}$ | 92 | | k Ω |
| FREQUENCY RESPONSE | | | | | |
| BW | Bandwidth | DAC mode enabled | | | |
| | | $G = 1\text{ V/V}$ | 8 | | MHz |
| | | $G = 0.707\text{ V/V}$ | 9 | | MHz |
| | | $G = 0.5\text{ V/V}$ | 10 | | MHz |
| | | $G = 0.25\text{ V/V}$ | 12 | | MHz |
| OUTPUT | | | | | |
| V_O | Voltage output swing from AGND or AV_{DD} | $R_{LOAD} = 10\text{ k}\Omega$, connected to $AV_{DD}/2$ | 10 | 100 | mV |
| I_O | Maximum continuous current, dc | Sourcing | 25 | | mA |
| | | Sinking | 25 | | mA |
| R_O | Output resistance | $f = 100\text{ kHz}$ | 1 | | Ω |
| GAIN | | | | | |
| Gain error | For all gains | –1% | ±0.1% | +1% | |
| Gain error drift | $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | | 6 | | ppm/ $^\circ\text{C}$ |

7.6 Electrical Characteristics: Transmitter (Tx), Tx_FILTER

At $T_J = 25^\circ\text{C}$, $PA_{VS} = 16\text{ V}$, $V_{AVDD} = V_{DVDD} = 3.3\text{ V}$, and PA_{ISET} (pin 46) connected to ground, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|--|-----------|-----------------|-----|---------------------|
| INPUT | | | | | | |
| Input voltage range | | | GND – 0.1 | $AV_{DD} + 0.1$ | | V |
| R_I | Input resistance (Tx_F_IN1 and Tx_F_IN2) | | | 43 | | k Ω |
| FREQUENCY RESPONSE | | | | | | |
| CENELEC A Mode | | | | | | |
| Passband frequency | | –3 dB | | 95 | | kHz |
| Stop band attenuation | | | –50 | –60 | | dB |
| Stop band frequency | | | | 910 | | kHz |
| Filter gain | | | | 0 | | dB |
| CENELEC B/C/D MODES | | | | | | |
| Passband frequency | | –3 dB | | 145 | | kHz |
| Stop band attenuation | | | –50 | –60 | | dB |
| Stop band frequency | | | | 870 | | kHz |
| Filter gain | | | | 0 | | dB |
| OUTPUT | | | | | | |
| V_O | Voltage output swing from AGND or AV_{DD} | $R_{LOAD} = 10\text{ k}\Omega$, connected to $AV_{DD}/2$ | | 10 | 100 | mV |
| I_O | Maximum continuous current, dc | Sourcing | | 25 | | mA |
| | | Sinking | | 25 | | mA |
| R_O | Output resistance | $f = 100\text{ kHz}$ | | 1 | | Ω |
| TRANSMITTER NOISE | | | | | | |
| Integrated noise at PA output ⁽¹⁾ | CENELEC Band A (40 kHz to 90 kHz) | Noise-reducing capacitor = 1 nF from pin 19 to ground | | 435 | | μV_{RMS} |
| | CENELEC Bands B/C/D (95 kHz to 140 kHz) | Noise-reducing capacitor = 1 nF from pin 19 to ground | | 460 | | μV_{RMS} |

(1) Includes DAC, Tx_PGA, Tx_Filter, PA, and REF1 bias generator.

7.7 Electrical Characteristics: Power Amplifier (PA)

At $T_J = 25^\circ\text{C}$, $PA_V_S = 16\text{ V}$, $V_{AVDD} = V_{DVDD} = 3.3\text{ V}$, and PA_ISET (pin 46) connected to ground, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|----------------------------------|--|---|-------------------------|-----|----------|
| INPUT | | | | | | |
| Input voltage range | | | GND – 0.1 | PA_V _S + 0.1 | | V |
| R _I | Input resistance | | | 20 | | kΩ |
| FREQUENCY RESPONSE | | | | | | |
| BW | Bandwidth | I _{LOAD} = 0 | | 670 | | kHz |
| SR | Slew rate | 10-V step | | 19 | | V/μs |
| Full-power bandwidth | | V _{OUT} = 10 V _{PP} | | 300 | | kHz |
| AC PSRR | | f = 50 kHz | | 14 | | dB |
| OUTPUT | | | | | | |
| V _O | Voltage output swing | From PA_V _S | I _O = 300 mA, sourcing | 0.3 | 1 | V |
| | | | I _O = 1.0 A, sourcing | 1 | 1.5 | V |
| | | From PA_Gnd | I _O = 300 mA, sinking | 0.3 | 1 | V |
| | | | I _O = 1.0 A, sinking | 1 | 1.5 | V |
| I _O | Maximum continuous current, dc | PA_ISET (pin 46) connected to ground | 1.0 | | | A |
| | Maximum peak current, ac | T _J = –40°C to +125°C, f = 50 kHz | | 1.0 | | A |
| R _O | Output resistance | I _O = 1.0 A | | 0.1 | | Ω |
| | PA disabled | Output impedance, f = 100 kHz, REF1 enabled | | 145 120 | | kΩ pF |
| | Output current limit range | | | ±0.4 to ±1.0 | | A |
| | Current limit equation | | I _{LIM} = 20 k × [1.2 V/(R _{SET} + 15 kΩ)] | | | A |
| | | Solved for R _{SET} (current limit) | R _{SET} = [(20 k × 1.2 V/I _{LIM}) – 15 kΩ] | | | Ω |
| GAIN (R _{LOAD} = 1 kΩ) | | | | | | |
| G | Nominal gain | | | 6.5 | | V/V |
| | Gain error | | –1% | 0.1% | +1% | |
| | Gain error drift | T _J = –40°C to +125°C | | ±1 | | ppm/°C |
| TSENSE DIODE | | | | | | |
| η | Diode ideality factor | | | 1.033 | | |
| THERMAL SHUTDOWN | | | | | | |
| | Junction temperature at shutdown | | | +165 | | °C |
| | Hysteresis | | | 20 | | °C |
| | Return to normal operation | | | +145 | | °C |

7.8 Electrical Characteristics: Receiver (Rx), Rx PGA1

At $T_J = 25^\circ\text{C}$, $PA_{VS} = 16\text{ V}$, $V_{AVDD} = V_{DVDD} = 3.3\text{ V}$, and PA_{ISET} (pin 46) connected to ground, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|--|--|-----|-------|-----|-----------------|
| INPUT | | | | | | |
| | Input voltage range | | | 10 | | V _{PP} |
| R _I | Input resistance | G = 2 V/V | | 10 | | kΩ |
| | | G = 1 V/V | | 15 | | kΩ |
| | | G = 0.5 V/V | | 20 | | kΩ |
| | | G = 0.25 V/V | | 24 | | kΩ |
| FREQUENCY RESPONSE | | | | | | |
| BW | Bandwidth | G = 2 V/V | | 6 | | MHz |
| | | G = 1 V/V | | 10 | | MHz |
| | | G = 0.5 V/V | | 13 | | MHz |
| | | G = 0.25 V/V | | 15 | | MHz |
| OUTPUT | | | | | | |
| V _O | Voltage output swing from AGND or AV _{DD} | R _{LOAD} = 6 kΩ, connected to AV _{DD} /2 | | 10 | 100 | mV |
| I _O | Maximum continuous current, dc | Sourcing | | 25 | | mA |
| | | Sinking | | 25 | | mA |
| R _O | Output resistance | G = 1, f = 100 kHz | | 1 | | Ω |
| GAIN | | | | | | |
| | Gain error | G = 0.25 V/V | −1% | ±0.1% | +1% | |
| | | G = 0.5 V/V | −1% | ±0.1% | +1% | |
| | | G = 1 V/V | −1% | ±0.1% | +1% | |
| | | G = 2 V/V | −2% | ±0.2% | +2% | |
| | Gain error drift | T _J = −40°C to +125°C | | 1 | | ppm/°C |

7.9 Electrical Characteristics: Receiver (Rx), Rx Filter

At $T_J = 25^\circ\text{C}$, $PA_V_S = 16\text{ V}$, $V_{AVDD} = V_{DVDD} = 3.3\text{ V}$, and PA_ISET (pin 46) connected to ground, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|-----------|-----------------|-----|------------|
| INPUT | | | | | | |
| | Input voltage range | | GND – 0.1 | $AV_{DD} + 0.1$ | | V |
| R_{IN} | Input resistance | | | 6 | | k Ω |
| FREQUENCY RESPONSE, CENELEC A MODE ($Rx_C1 = 680\text{ pF}$, $Rx_C2 = 680\text{ pF}$) | | | | | | |
| | Passband frequency | –3 dB | | 90 | | kHz |
| | Stop band attenuation | | –25 | –33 | | dB |
| | Stop band frequency | | | 270 | | kHz |
| | Filter gain | | | 0 | | dB |
| FREQUENCY RESPONSE, CENELEC B/C/D MODES ($Rx_C1 = 270\text{ pF}$, $Rx_C2 = 560\text{ pF}$) | | | | | | |
| | Passband frequency | –3 dB | | 145 | | kHz |
| | Stop band attenuation | | –25 | –35 | | dB |
| | Stop band frequency | | | 350 | | kHz |
| | Filter gain | | | 0 | | dB |
| OUTPUT | | | | | | |
| V_O | Voltage output swing from AGND or AV_{DD} | $R_{LOAD} = 10\text{ k}\Omega$, connected to $AV_{DD}/2$ | | 10 | 100 | mV |
| I_O | Maximum continuous current, dc | Sourcing | | 25 | | mA |
| | | Sinking | | 25 | | mA |
| R_O | Output resistance | $f = 100\text{ kHz}$ | | 5 | | Ω |

7.10 Electrical Characteristics: Receiver (Rx), Rx PGA2

At $T_J = 25^\circ\text{C}$, $PA_{VS} = 16\text{ V}$, $V_{AVDD} = V_{DVDD} = 3.3\text{ V}$, and PA_{ISET} (pin 46) connected to ground, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------------|--|---|-----------|------------------------|-----|-------------------|
| INPUT | | | | | | |
| Input voltage range | | | GND – 0.1 | AV _{DD} + 0.1 | | V |
| R _I | Input impedance | G = 64 V/V | | 1.7 | | kΩ |
| | | G = 16 V/V | | 6.3 | | kΩ |
| | | G = 4 V/V | | 21 | | kΩ |
| | | G = 1 V/V | | 53 | | kΩ |
| FREQUENCY RESPONSE | | | | | | |
| BW | Bandwidth | G = 64 V/V | | 300 | | kHz |
| | | G = 16 V/V | | 800 | | kHz |
| | | G = 4 V/V | | 1.4 | | MHz |
| | | G = 1 V/V | | 4 | | MHz |
| OUTPUT | | | | | | |
| V _O | Voltage output swing from AGND or AV _{DD} | R _{LOAD} = 10 kΩ, connected to AV _{DD} /2 | | 10 | 100 | mV |
| I _O | Maximum continuous current, dc | Sourcing | | 25 | | mA |
| | | Sinking | | 25 | | mA |
| R _O | Output impedance | G = 1, f = 100 kHz | | 1 | | Ω |
| GAIN | | | | | | |
| Gain error | | G = 1 V/V | –2% | ±1% | 2% | |
| | | G = 4 V/V | –2% | ±1% | 2% | |
| | | G = 16 V/V | –2% | ±1% | 2% | |
| | | G = 64 V/V | –4% | ±1% | 4% | |
| Gain error drift | | T _J = –40°C to +125°C | | 6 | | ppm/°C |
| Rx SENSITIVITY | | | | | | |
| Integrated noise, RTI ⁽¹⁾ | CENELEC Band A (40 kHz to 90 kHz) | Noise-reducing capacitor = 1 μF from pin 28 to ground | | 14 | | μV _{RMS} |
| | CENELEC Bands B/C/D (95 kHz to 140 kHz) | Noise-reducing capacitor = 1 μF from pin 28 to ground | | 11 | | μV _{RMS} |

(1) Includes Rx PGA1, Rx_Filter, Rx PGA2, and REF2 bias generator.

7.11 Electrical Characteristics: Digital

At $T_J = 25^\circ\text{C}$, $PA_V_S = 16\text{ V}$, $V_{AVDD} = V_{DVDD} = 3.3\text{ V}$, and PA_ISET (pin 46) connected to ground, unless otherwise noted.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|--|------|------------------|---------------|
| DIGITAL INPUTS (SCLK, DIN, \overline{CS} , DAC, SD) | | | | | |
| Leakage input current | $0 \leq V_{IN} \leq DV_{DD}$ | -1 | 0.01 | 1 | μA |
| V _{IH} High-level input voltage | | 0.7 × DV _{DD} | | | V |
| V _{IL} Low-level input voltage | | 0.3 × DV _{DD} | | | V |
| SD pin high | SD > 0.7 × DV _{DD} | AFE030 in shutdown | | | |
| SD pin low | SD < 0.3 × DV _{DD} | AFE030 in normal operation | | | |
| DAC pin high | DAC > 0.7 × DV _{DD} | SPI access to DAC Registers | | | |
| DAC pin low | DAC < 0.3 × DV _{DD} | SPI access to Command and Data Registers | | | |
| DIGITAL OUTPUTS (DO, ZC_OUT) | | | | | |
| V _{OH} High-level output voltage | I _{OH} = 3 mA | DV _{DD} - 0.4 | | DV _{DD} | V |
| V _{OL} Low-level output voltage | I _{OL} = -3 mA | GND | | GND + 0.4 | V |
| DIGITAL OUTPUTS (INT, Tx_Flag, Rx_Flag) | | | | | |
| I _{OH} High-level output current | V _{OH} = 3.3 V | | | 1 | μA |
| V _{OL} Low-level output voltage | I _{OL} = 4 mA | | | 0.4 | V |
| I _{OL} Low-level output current | V _{OL} = 400 mV | 4 | | | mA |
| INT pin high (open drain) | INT sink current < 1 μA | Normal operation | | | μs |
| INT pin low (open drain) ⁽¹⁾ | INT < 0.4 V | Indicates an interrupt has occurred | | | μs |
| Tx_Flag high (open drain) | Tx_Flag sink current < 1 μA | Indicates Tx block is not ready | | | μs |
| Tx_Flag low (open drain) | Tx_Flag < 0.4 V | Indicates Tx block is ready | | | μs |
| Rx_Flag high (open drain) | Rx_Flag sink current < 1 μA | Indicates Rx block is not ready | | | μs |
| Rx_Flag low (open drain) | Rx_Flag < 0.4 V | Indicates Rx block is ready | | | μs |
| DIGITAL TIMING | | | | | |
| Gain select time | | | 0.2 | | μs |
| Shutdown mode, enable time | | | 4.0 | | μs |
| Shutdown mode, disable time | | | 2.0 | | μs |
| Power-on reset (POR) power-up time | DV _{DD} ≥ 2 V | | 50 | | μs |

(1) When an interrupt is detected (INT pin low), the contents of the I_Flag and T_Flag Registers can be read to determine the reason for the interrupt.

7.12 Electrical Characteristics: Two-Wire Interface

At $T_J = 25^\circ\text{C}$, $PA_V_S = 16\text{ V}$, $V_{AVDD} = V_{DVDD} = 3.3\text{ V}$, and PA_ISET (pin 46) connected to ground, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|------------------------------|----------------------|------|----------------------|---------------|
| TWO-WIRE TRANSMITTER | | | | | |
| Frequency range ⁽¹⁾ | | | 50 | | kHz |
| Leakage input current (E_Tx_In , E_Tx_Clk) | $0 \leq V_{IN} \leq DV_{DD}$ | -1 | 0.01 | 1 | μA |
| INPUT LOGIC LEVELS (E_Tx_In, E_Tx_Clk) | | | | | |
| V_{IH} High-level input voltage | | $0.7 \times DV_{DD}$ | | | V |
| V_{IL} Low-level input voltage | | | | $0.3 \times DV_{DD}$ | V |
| OUTPUT LOGIC LEVELS (E_Tx_Out) | | | | | |
| V_{OH} High-level output voltage | $I_{OH} = 3\text{ mA}$ | $AV_{DD} - 0.4$ | | AV_{DD} | V |
| V_{OL} Low-level output voltage | $I_{OL} = -3\text{ mA}$ | GND | | $GND + 0.4$ | V |
| TWO-WIRE RECEIVER | | | | | |
| Gain | | | -4.5 | | dB |
| Frequency range | | | 300 | | kHz |
| Maximum sink current | | | 25 | | mA |
| Maximum source current | | | 25 | | mA |
| Input terminal offset | Referenced to $V_{AVDD}/2$ | -100 | 10 | 100 | mV |
| Input impedance | | | 78 | | k Ω |

(1) The two-wire transmitter circuit is tested at $Tx_CLK = 10\text{ MHz}$.

7.13 Electrical Characteristics: Zero-Crossing Detector

At $T_J = 25^\circ\text{C}$, $PA_V_S = 16\text{ V}$, $V_{AVDD} = V_{DVDD} = 3.3\text{ V}$, and PA_ISET (pin 46) connected to ground, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | AFE030 | | | UNIT |
|---------------------|----------------------|-----------------|-----|-----------------|------|
| | | MIN | TYP | MAX | |
| Input voltage range | | $AV_{DD} - 0.4$ | | $AV_{DD} + 0.4$ | V |
| Input current range | | -10 | | 10 | mA |
| Input capacitance | | | 3 | | pF |
| Rising threshold | | 0.45 | 0.9 | 1.35 | V |
| Falling threshold | | 0.25 | 0.5 | 0.75 | V |
| Hysteresis | | 0.20 | 0.4 | 0.60 | V |
| Jitter | 50 Hz, 240 V_{RMS} | | 10 | | ns |

7.14 Electrical Characteristics: Internal Bias Generator

At $T_J = 25^\circ\text{C}$, $PA_V_S = 16\text{ V}$, $V_{AVDD} = V_{DVDD} = 3.3\text{ V}$, and PA_ISET (pin 46) connected to ground, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|--|-----|--------------|-----|-----------|
| REF1 (Pin 19) | | | | | |
| Bias voltage | | | $PA_V_S/2$ | | V |
| R_I Input resistance | | | 4 | | $k\Omega$ |
| Turn-on time | Noise-reducing capacitor = 1 nF from pin 19 to ground | | 20 | | ms |
| Turn-off time | Noise-reducing capacitor = 1 nF from pin 19 to ground | | 20 | | ms |
| REF2 (Pin 28) | | | | | |
| Bias voltage | | | $V_{AVDD}/2$ | | V |
| R_I Input resistance | | | 4 | | $k\Omega$ |
| Turn-on time | Noise-reducing capacitor = 1 μF from pin 28 to ground | | 20 | | ms |
| Turn-off time | Noise-reducing capacitor = 1 μF from pin 28 to ground | | 20 | | ms |

7.15 Electrical Characteristics: Power Supply

At $T_J = 25^\circ\text{C}$, $PA_V_S = 16\text{ V}$, $V_{AVDD} = V_{DVDD} = 3.3\text{ V}$, and PA_ISET (pin 46) connected to ground, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-----|-----|-----|------------------|
| OPERATING SUPPLY RANGE | | | | | |
| PA_V_S Power amplifier supply voltage | | 7 | | 24 | V |
| DV_{DD} Digital supply voltage | | 3.0 | | 3.6 | V |
| AV_{DD} Analog supply voltage | | 3.0 | | 3.6 | V |
| QUIESCENT CURRENT SD pin low | | | | | |
| I_{QPA_VS} Power amplifier current | $I_O = 0\text{ A}$, $PA = \text{On}^{(1)}$ | | 40 | 55 | mA |
| | $I_O = 0\text{ A}$, $PA = \text{Off}^{(2)}$ | | 10 | | μA |
| I_{QDVDD} Digital supply current | Tx configuration ⁽³⁾ | | 1.2 | | mA |
| | Rx configuration ⁽⁴⁾ | | 5 | | μA |
| | All blocks disabled ⁽⁵⁾ | | 5 | | μA |
| I_{QAVDD} Analog supply current | Tx configuration ⁽³⁾ | | 2.8 | 3.7 | mA |
| | Rx configuration ⁽⁴⁾ | | 3.6 | 5.3 | mA |
| | All blocks disabled ⁽⁵⁾ | | 30 | | μA |
| SHUTDOWN (SD) | | | | | |
| PA_V_S Power amplifier supply voltage | SD pin high | | 75 | 150 | μA |
| DV_{DD} Digital supply voltage | SD pin high | | 5 | 10 | μA |
| AV_{DD} Analog supply voltage | SD pin high | | 15 | 40 | μA |
| TEMPERATURE | | | | | |
| Specified range | | -40 | | 125 | $^\circ\text{C}$ |

(1) Enable1 Register = 00100011, Enable2 Register = 00001110.

(2) Enable1 Register = 00000100, Enable2 Register = 00000110.

(3) In the Tx configuration, the following blocks are enabled: DAC, Tx, PA, REF1, and REF2. All other blocks are disabled. Enable1 Register = 00100011, Enable2 Register = 00001110.

(4) In the Rx configuration, the following blocks are enabled: Rx, REF1, and REF2. All other blocks are disabled. Enable1 Register = 00000100, Enable2 Register = 00000110.

(5) Enable1 Register = 00000000, Enable2 Register = 00000000.

7.16 Typical Characteristics

At $T_J = 25^\circ\text{C}$, $\text{PA_V}_S = 16\text{ V}$, $\text{V}_{\text{AVDD}} = \text{V}_{\text{DVDD}} = 3.3\text{ V}$, and PA_ISET (pin 46) connected to ground, unless otherwise noted.

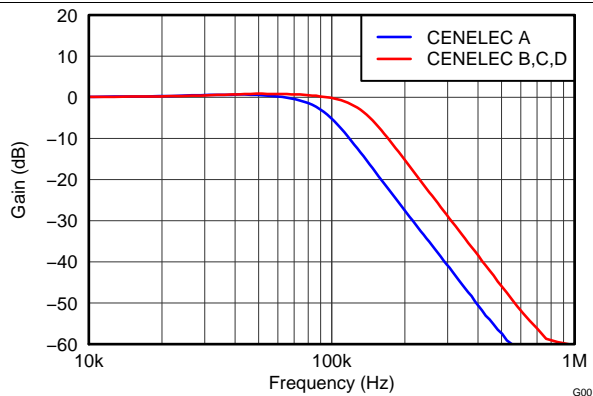


Figure 1. Tx Filter Gain vs Frequency

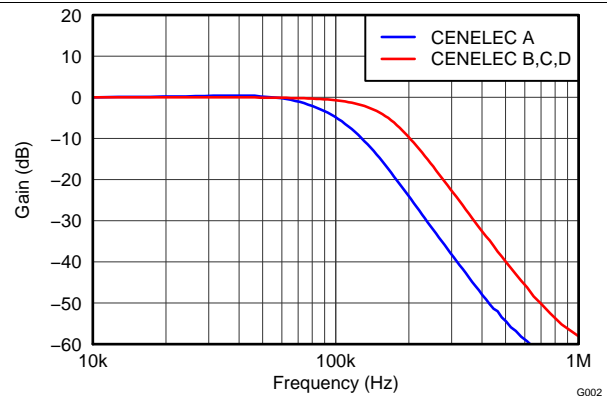


Figure 2. Rx Filter Gain vs Frequency

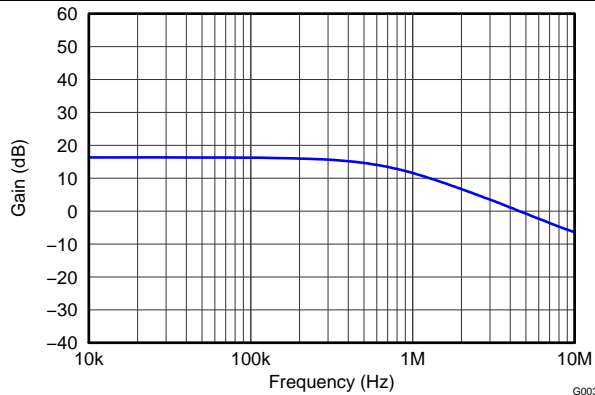


Figure 3. PA Gain vs Frequency

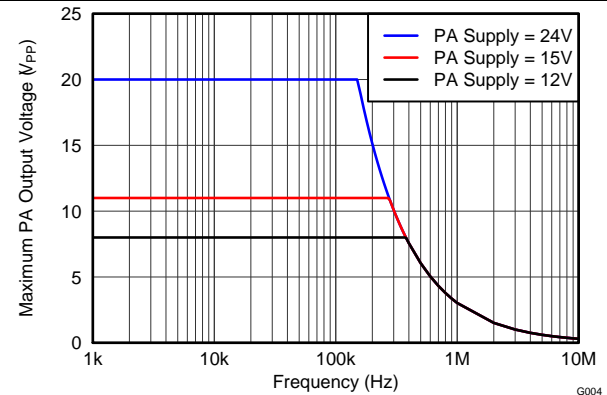


Figure 4. Maximum PA Output Voltage vs Frequency

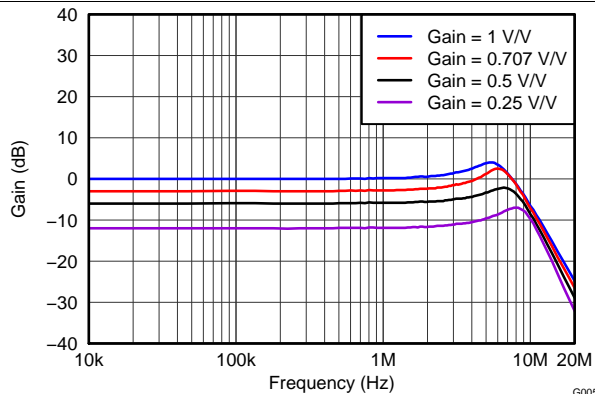


Figure 5. Tx PGA Gain vs Frequency

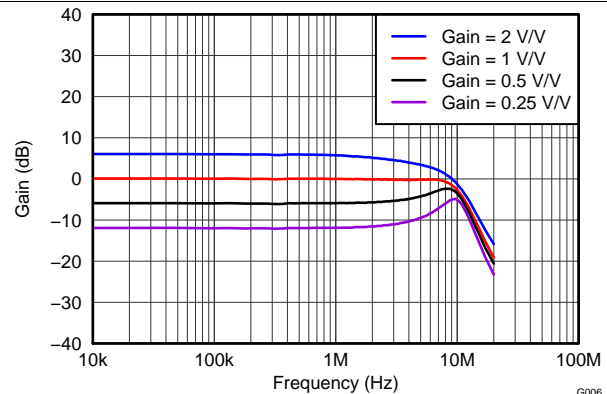


Figure 6. Rx PGA1 Gain vs Frequency

Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$, $PA_V_S = 16\text{ V}$, $V_{AVDD} = V_{DVDD} = 3.3\text{ V}$, and PA_ISET (pin 46) connected to ground, unless otherwise noted.

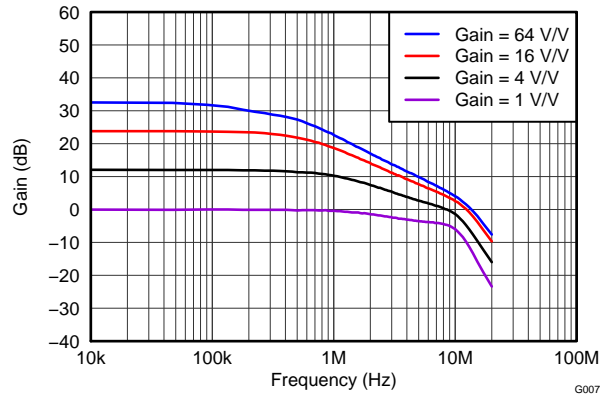


Figure 7. Rx PGA2 Gain vs Frequency

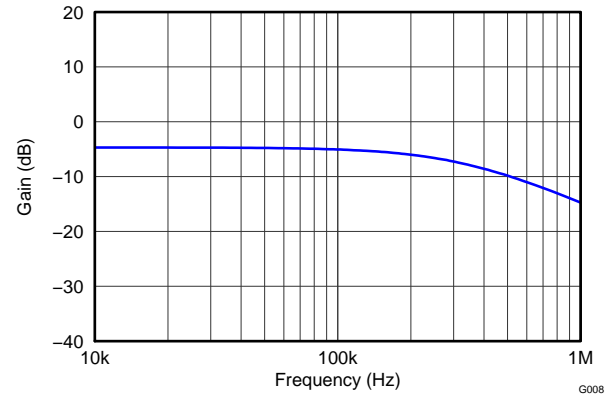


Figure 8. Two-Wire Receiver Gain vs Frequency

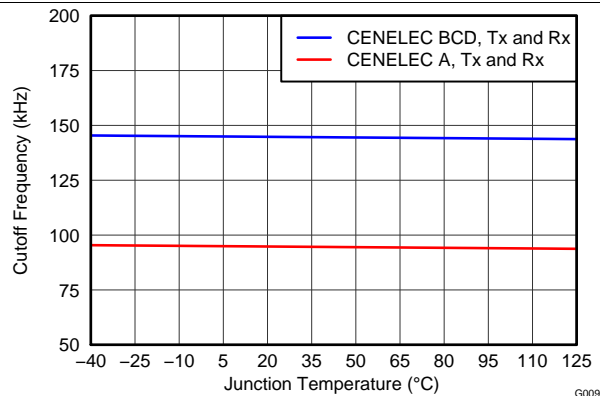


Figure 9. Filter Cutoff vs Temperature

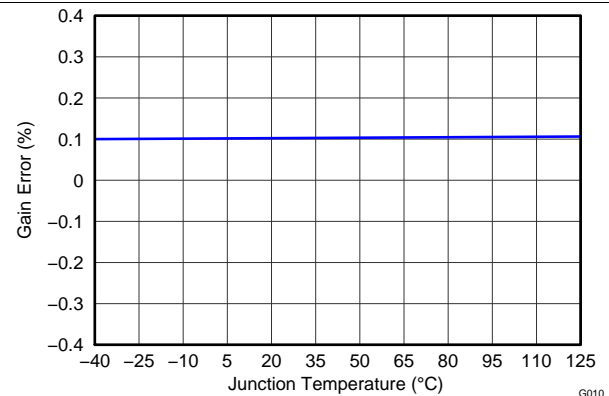


Figure 10. Tx PGA Gain Error vs Temperature

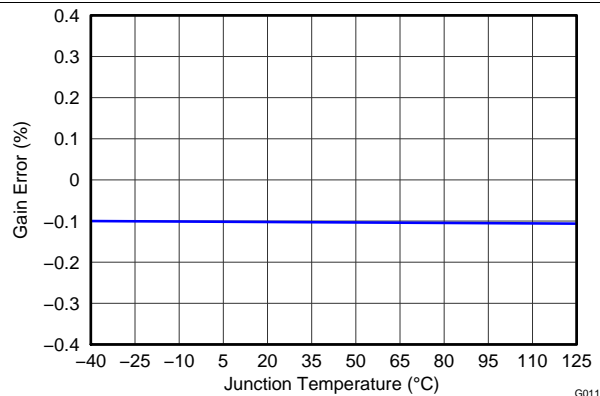


Figure 11. PA Gain Error vs Temperature

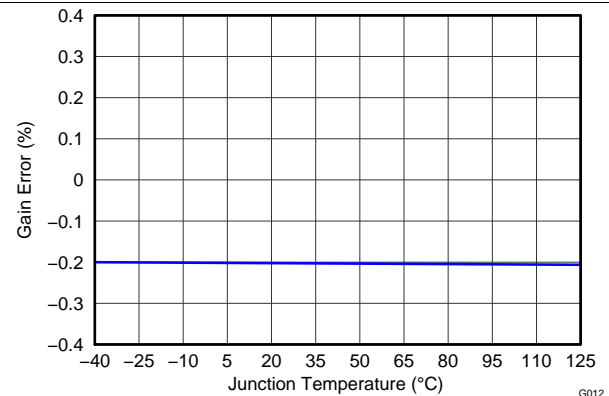


Figure 12. Rx PGA1 Gain Error vs Temperature

Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$, $PA_V_S = 16\text{ V}$, $V_{AVDD} = V_{DVDD} = 3.3\text{ V}$, and PA_ISET (pin 46) connected to ground, unless otherwise noted.

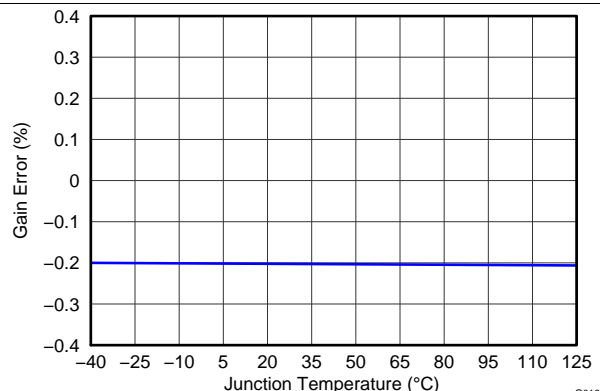


Figure 13. Rx PGA2 Gain Error vs Temperature

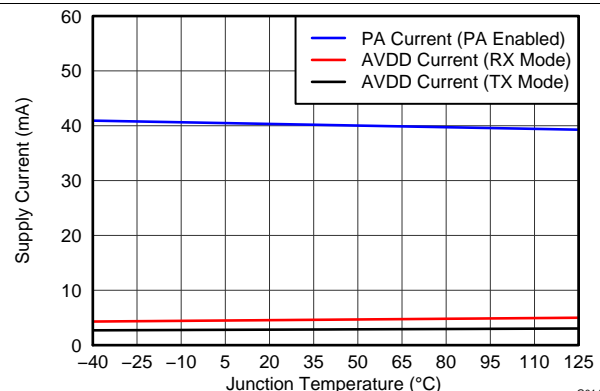


Figure 14. Quiescent Supply Current vs Temperature

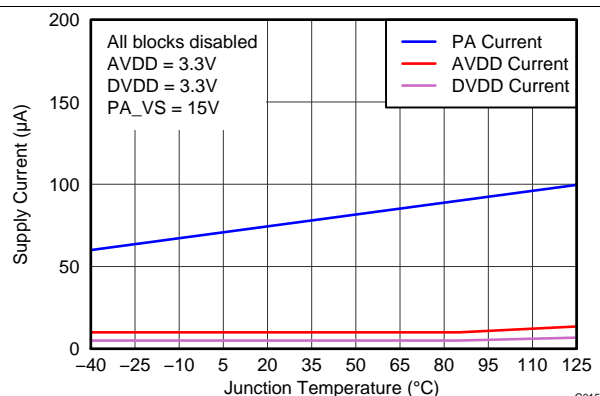


Figure 15. Supply Current (Shutdown) vs Temperature

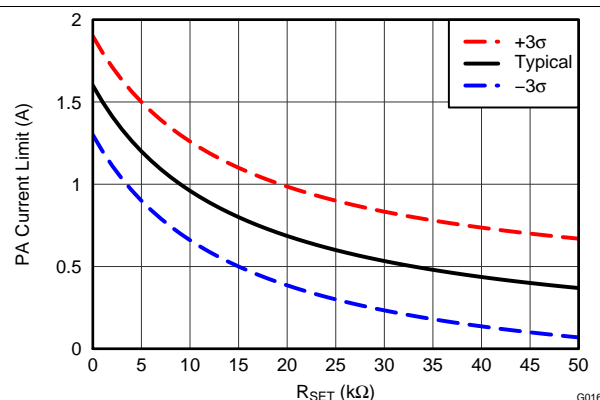


Figure 16. PA Current Limit vs R_{SET}

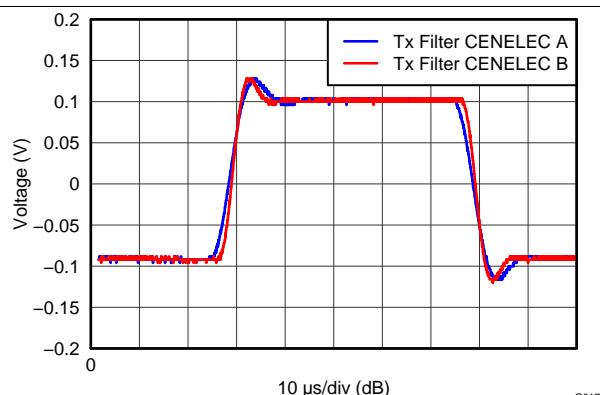


Figure 17. Tx Filter Pulse Response

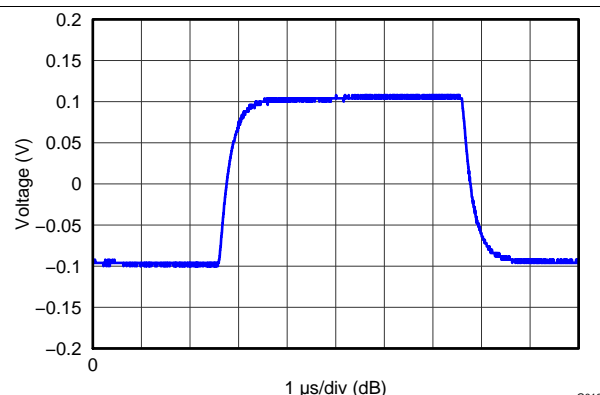


Figure 18. PA Pulse Response

Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$, $PA_V_S = 16\text{ V}$, $V_{AVDD} = V_{DVDD} = 3.3\text{ V}$, and PA_ISET (pin 46) connected to ground, unless otherwise noted.

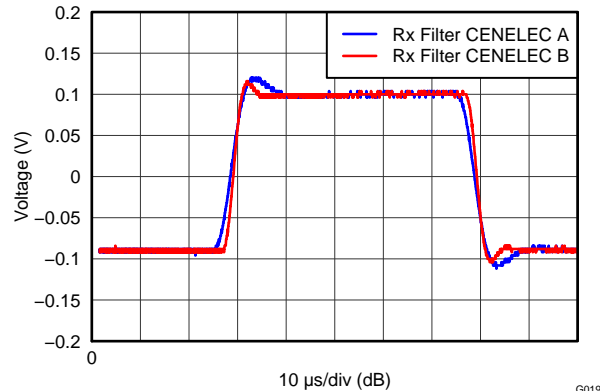


Figure 19. Rx Pulse Response

8 Parameter Measurement Information

8.1 Timing Requirements

Table 1. SPI Timing Requirements

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|--|---------------------------------------|-----|-----|-----|------|
| Input capacitance | | | 1 | | pF |
| Input rise/fall time | t_{RFI} \overline{CS} , DIN, SCLK | | | 2 | ns |
| Output rise/fall time | t_{RFO} DOUT | | | 10 | ns |
| \overline{CS} high time | t_{CSH} \overline{CS} | 20 | | | ns |
| SCLK edge to \overline{CS} fall setup time | t_{CS0} | 10 | | | ns |
| \overline{CS} fall to first SCLK edge setup time | t_{CSSC} | 10 | | | ns |
| SCLK frequency | f_{SCLK} | | | 20 | MHz |
| SCLK high time | t_{HI} | 20 | | | ns |
| SCLK low time | t_{LO} | 20 | | | ns |
| SCLK last edge to \overline{CS} rise setup time | t_{SCCS} | 10 | | | ns |
| \overline{CS} rise to SCLK edge setup time | t_{CS1} | 10 | | | ns |
| DIN setup time | t_{SU} | 10 | | | ns |
| DIN hold time | t_{HD} | 5 | | | ns |
| SCLK to DOUT valid propagation delay | t_{DO} | | | 20 | ns |
| \overline{CS} rise to DOUT forced to Hi-Z | t_{SOZ} | | | 20 | ns |

8.2 Timing Diagrams

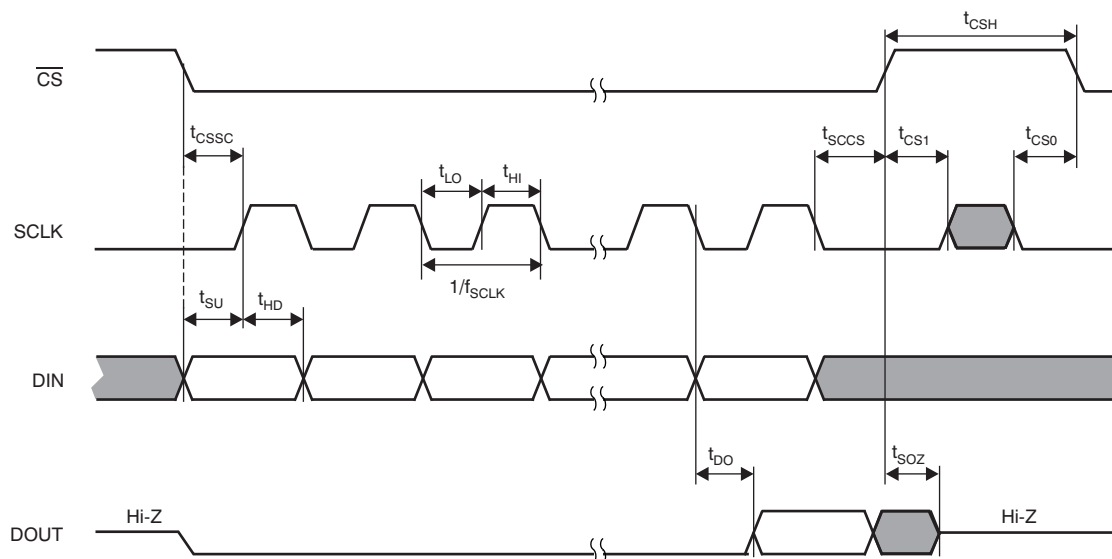


Figure 20. SPI Mode 0,0

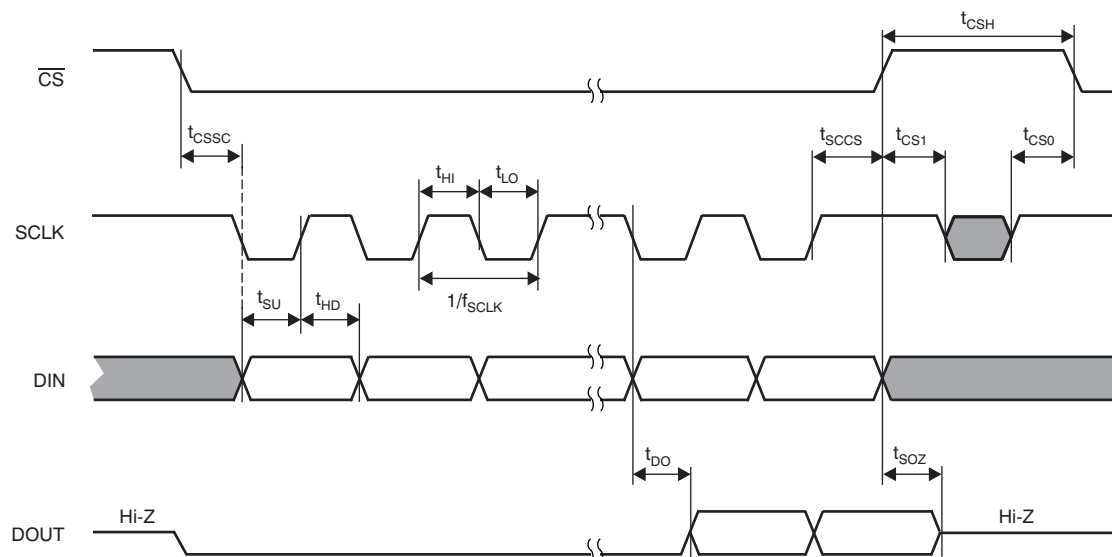
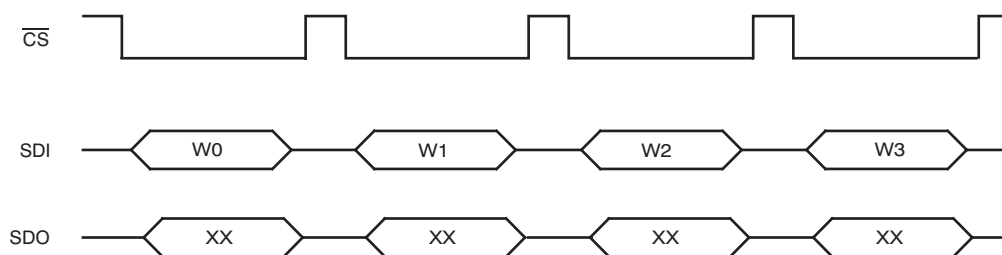


Figure 21. SPI Mode 1,1



W - Command of Write Register *N*
 XX - Don't care; undefined.

Figure 22. Write Operation in Stand-Alone Mode

Timing Diagrams (continued)

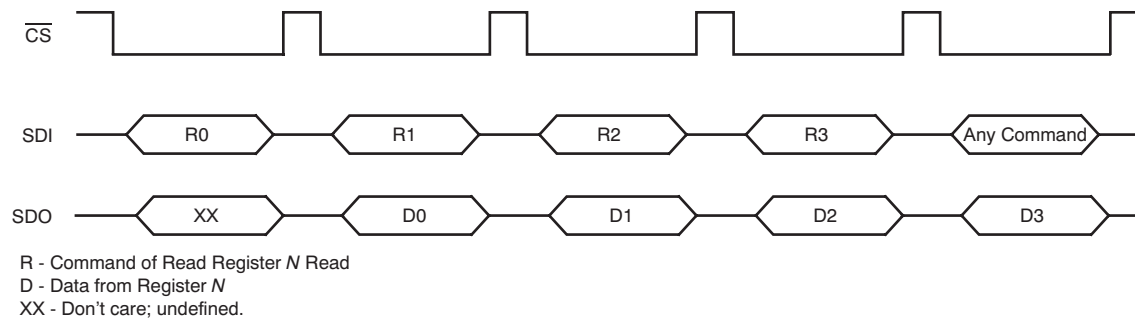


Figure 23. Read Operation in Stand-Alone Mode

9 Detailed Description

9.1 Overview

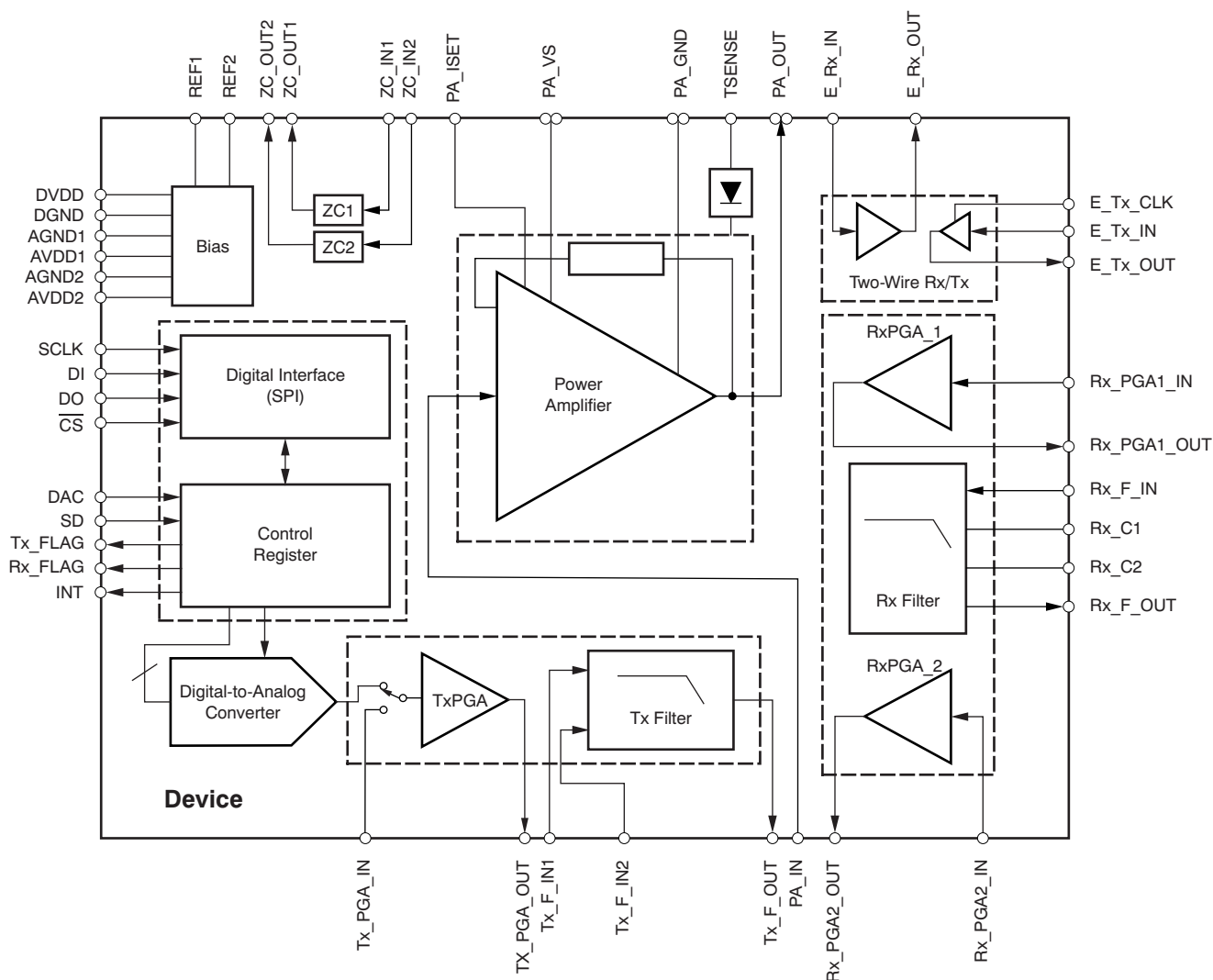
The AFE030 is an integrated powerline communication analog front-end (AFE) device built from a variety of functional blocks that work in conjunction with a microcontroller. The AFE030 provides the interface between the microcontroller and a line coupling circuit. The AFE030 delivers high performance and is designed to work with a minimum number of external components. Consisting of a variety of functional and configurable blocks, the AFE030 simplifies design efforts and reduces the time to market of many applications.

The AFE030 includes three primary functional blocks:

- Power Amplifier (PA)
- Transmitter (Tx)
- Receiver (Rx)

The AFE030 also consists of other support circuitry blocks that provide zero crossing detection, an additional two-wire communications channel, and power-saving biasing blocks (see the [Functional Block Diagram](#)). All of these functional blocks are digitally controlled by the microcontroller through the serial interface (SPI).

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 PA Block

Figure 24 shows a typical powerline communications application system diagram. Table 2 is a complete list of the sections within the AFE030.

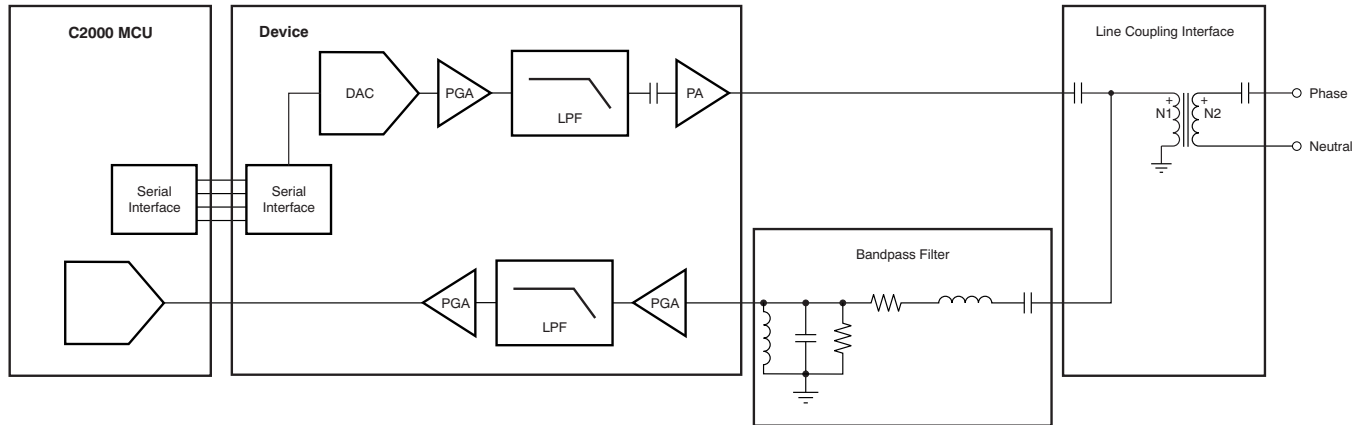


Figure 24. Typical Powerline Communications System Diagram

Table 2. Block Descriptions

| BLOCK | DESCRIPTION |
|-------|--|
| PA | The PA block includes the power amplifier and associated pedestal biasing circuitry |
| Tx | The Tx block includes the Tx_Filter and the Tx_PGA |
| Rx | The Rx block includes the Rx PGA1, the Rx Filter, and the Rx PGA2 |
| ERx | The ER block includes the two-wire receiver |
| ETx | The ER block includes the two-wire transmitter |
| DAC | The DAC block includes a digital-to-analog converter |
| ZC | The ZC block includes both zero crossing detectors |
| REF1 | The REF1 block includes the internal bias generator for the PA block |
| REF2 | The REF2 block includes the internal bias generators for the Tx, Rx, ERx, and ETx blocks |

The power amplifier (PA) block consists of a high slew rate, high-voltage, and high-current operational amplifier. The PA is configured with an inverting gain of 6.5 V/V, has a low-pass filter response, and maintains excellent linearity and low distortion. The PA is specified to operate from 7 V to 26 V and can deliver up to ± 1 A of continuous output current over the specified junction temperature range of -40°C to $+125^{\circ}\text{C}$. Figure 25 illustrates the PA block.

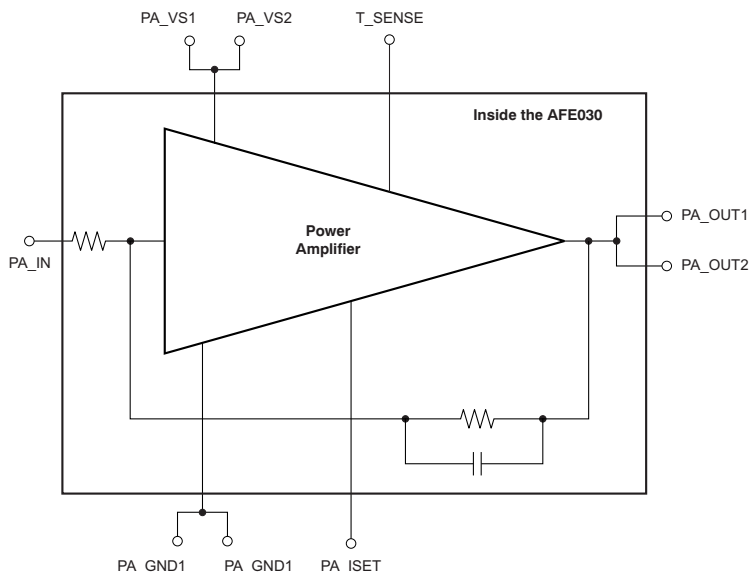


Figure 25. PA Block Equivalent Circuit

Connecting the PA in a typical PLC application requires only two additional components: an ac coupling capacitor, C_{IN} , and the current limit programming resistor, R_{SET} . Figure 26 shows the typical connections to the PA block.

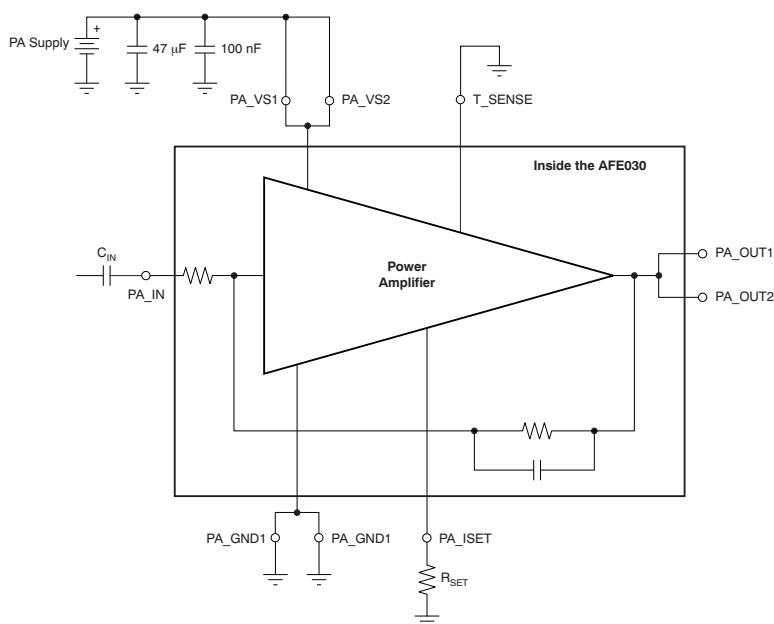


Figure 26. Typical Connections to the PA

The external capacitor, C_{IN} , introduces a single-pole, high-pass characteristic to the PA transfer function; combined with the inherent low-pass transfer function, this characteristic results in a passband response. The value of the high-pass cutoff frequency is determined by C_{IN} reacting with the input resistance of the PA circuit, and can be found from Equation 1:

$$C_{IN} = \frac{1}{(2 \times \pi \times 20 \text{ k}\Omega \times f_{HP})} \quad (1)$$

Where:

- C_{IN} = external input capacitor
- f_{HP} = desired high-pass cutoff frequency

For example, setting C_{IN} to 3.3 nF results in a high-pass cutoff frequency of 2.4 kHz. The voltage rating for C_{IN} should be determined to withstand operation up to the PA power-supply voltage.

When the transmitter is not in use, the output can be disabled and placed into a high-impedance state by writing a '0' to the PA-OUT bit in the [Enable2 Register](#). Additional power savings can be realized by shutting down the PA when not in use. Shutting down the PA for power savings is accomplished by writing a '0' to the PA bit in the [Enable1 Register](#). Shutting down the PA also results in the PA output entering a high-impedance state. When the PA shuts down, it consumes only 2 mW of power.

The PA_ISET pin (pin 46) provides a resistor-programmable output current limit for the PA block. [Equation 2](#) determines the value of the external R_{SET} resistor attached to this pin.

$$R_{SET} = \left(20 \text{ k} \times \frac{1.2 \text{ V}}{I_{LIM}} \right) - 15 \text{ k}\Omega \quad (2)$$

Where:

- R_{SET} = the value of the external resistor connected between pin 46 and ground.
- I_{LIM} = the value of the desired current limit for the PA.

Note that to ensure proper design margin with respect to manufacturing and temperature variations, a 30% increase in the value used in [Equation 2](#) for I_{LIM} over the nominal value of I_{LIM} is recommended. See [Figure 16](#), *PA Current Limit vs R_{SET}* . For maximum output current, PA_ISET (pin 46) may be connected directly to ground.

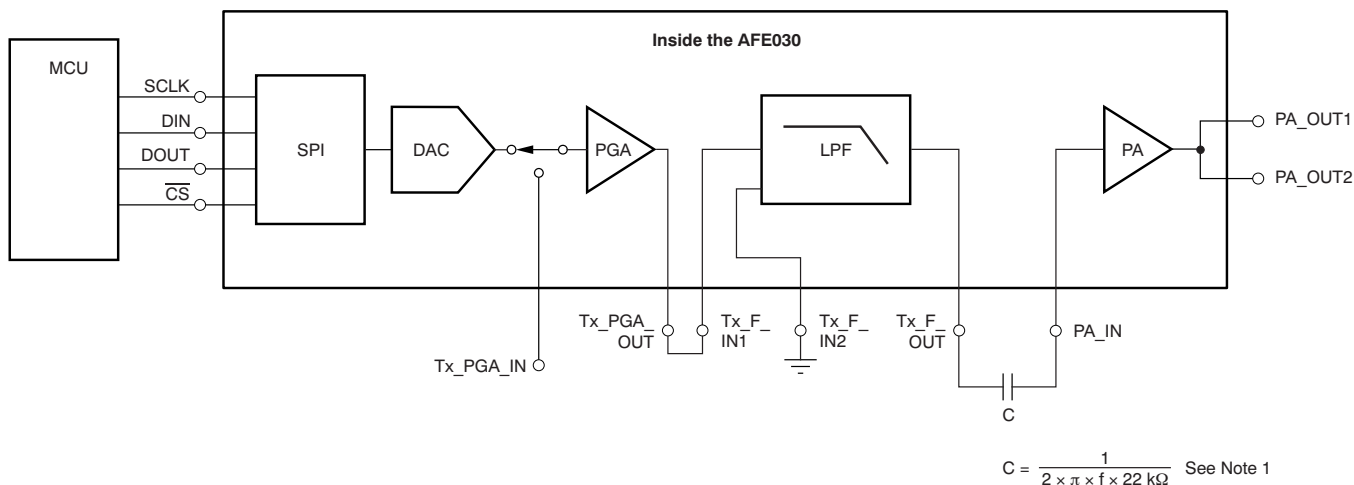
9.3.2 Tx Block

The Tx block consists of the Tx PGA and Tx Filter. The Tx PGA is a low-noise, high-performance, programmable gain amplifier. In DAC mode (where pin 7 is a logical '1' and [Enable1 Register](#) bit location 5 is a logical '1'), the Tx PGA operates as the internal digital-to-analog converter (DAC) output buffer with programmable gain. In PWM mode (where pin 7 is a logical '0' and [Enable1 Register](#) bit location 5 is a logical '0'), the Tx PGA operates as a stand-alone programmable gain amplifier. The Tx PGA gain is programmed through the serial interface. The Tx PGA gain settings are 0.25 V/V, 0.5 V/V, 0.707 V/V, and 1 V/V.

The Tx Filter is a unity-gain, fourth-order low-pass filter. The Tx Filter cutoff frequency is selectable between CENELEC A or CENELEC B, C, and D modes. The [Control1 Register](#) bit location 3 setting (CA CBCD) determines the cutoff frequency. Setting Control1 Register bit location 3 to '0' selects the CENELEC A band; setting Control1 Register bit location 3 to '1' selects CENELEC B, C, and D bands.

The AFE030 supports both DAC inputs or PWM inputs for the Tx signal path. DAC mode is recommended for best performance. In DAC mode, no external components in the Tx signal path are required to meet regulatory signal emissions requirements. When in DAC mode, the AFE030 accepts serial data from the microprocessor and writes that data to the internal DAC registers. When in DAC mode (where pin 7 is a logical '1' and [Enable1 Register](#) bit location 5 is a logical '1'), the Tx PGA output must be directly coupled to the Tx_FIN1 input and the unused Tx_FIN2 input must be grounded.

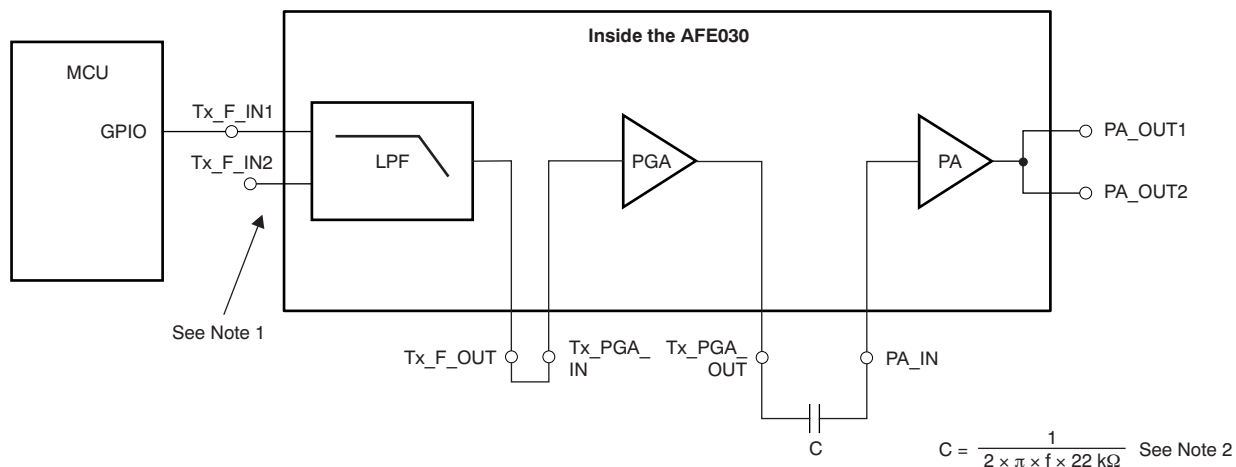
The proper connections for the Tx signal path for DAC mode operation are shown in [Figure 27](#). Operating in DAC mode results in the lowest distortion signal injected onto the ac mains. No additional external filtering components are required to meet CENELEC requirements for A, B, C or D bands when operating in DAC mode.



(1) For capacitor value C, f is the desired lower cutoff frequency and 22 kΩ is the PA input resistance.

Figure 27. Recommended Tx Signal Chain Connections Using DAC Mode

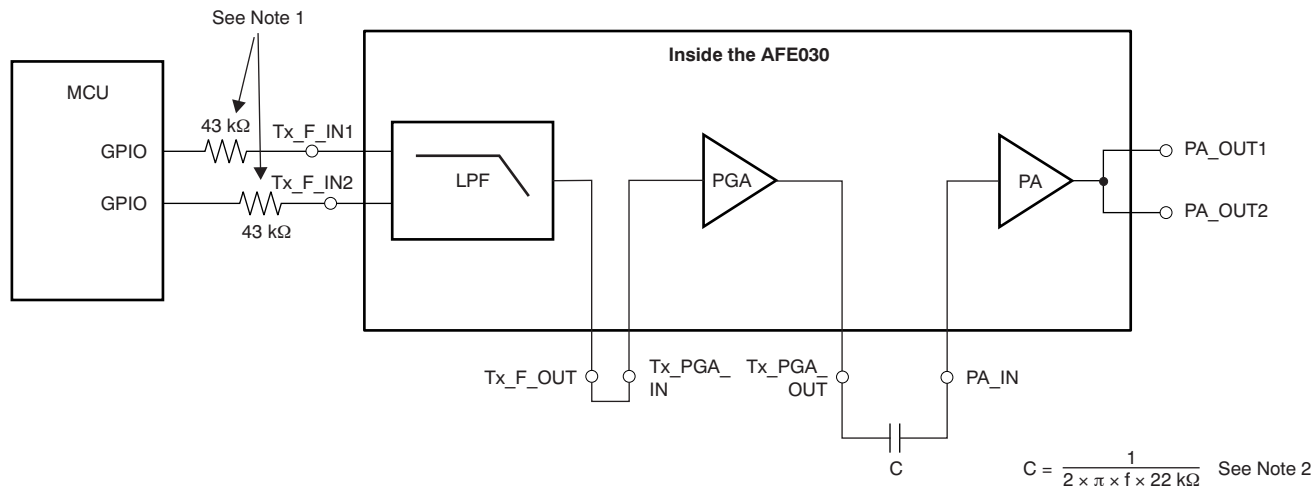
In PWM mode (where pin 7 is a logical '0' and [Enable1 Register](#) bit location 5 is a logical '0'), the microprocessor general-purpose input/output (GPIO) can be connected directly to either one of the Tx Filter inputs; the unused input should remain unconnected. A lower distortion PWM signal generated from two PWM signals shifted in phase by 90 degrees can be also be input to the Tx Filter through the use of both inputs. [Figure 28](#) and [Figure 29](#) show the proper connections for single PWM and dual PWM operating modes, respectively.



(1) Leave unused Tx Filter input unconnected.

(2) For capacitor value C, f is the desired lower cutoff frequency and 22 kΩ is the PA input resistance.

Figure 28. Recommended Tx Signal Chain Connections in PWM Mode Using One PWM Signal

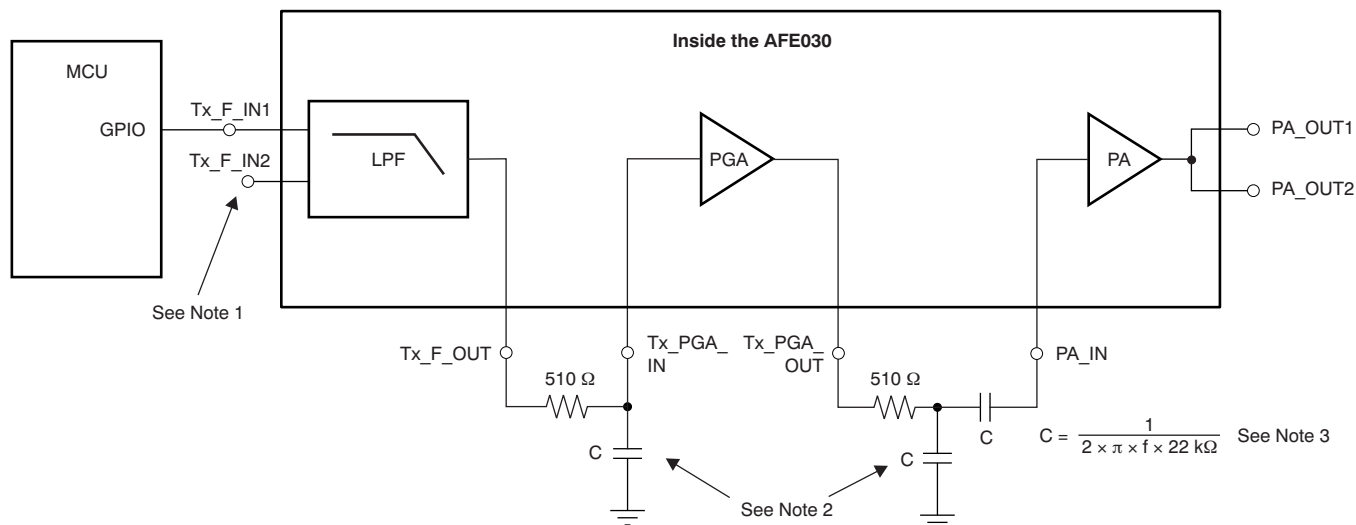


(1) When using both Tx Filter inputs, use 43-kΩ resistors to match the input resistance for best frequency response.

(2) For capacitor value C, f is the desired lower cutoff frequency and 22 kΩ is the PA input resistance.

Figure 29. Recommended Tx Signal Chain Connections in PWM Mode Using Two PWM Signals

In PWM mode, there is inherently more distortion from the PWM signal than from the internal DAC. To achieve the best results in PWM mode, add passive RC filters to increase the low-pass filtering. [Figure 30](#) and [Figure 31](#) illustrate the recommended locations of these RC filters.

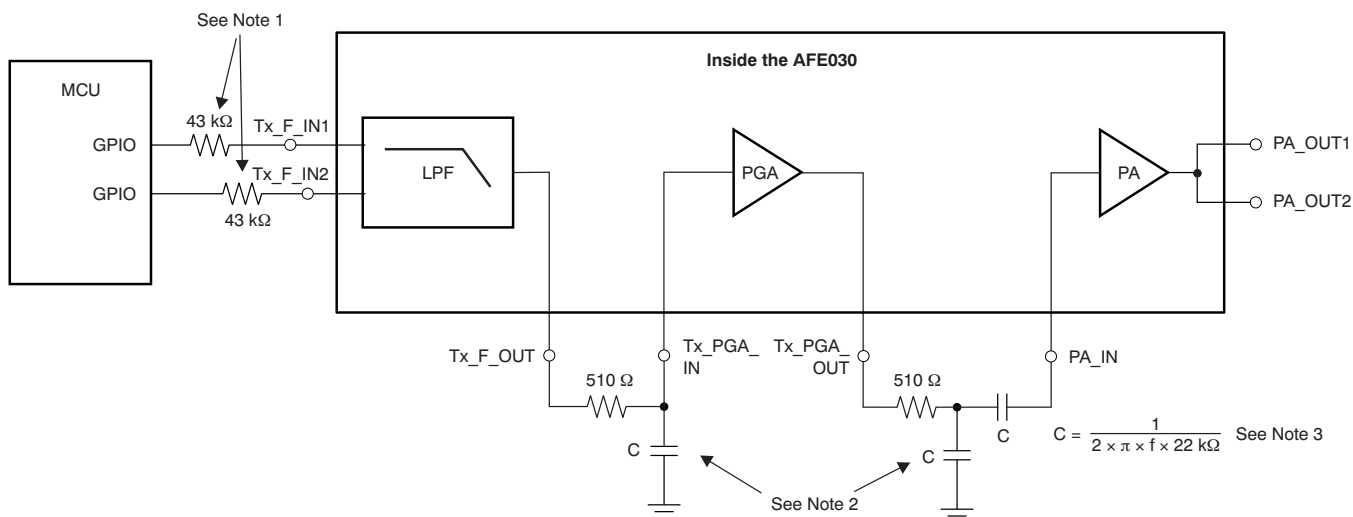


(1) Leave unused Tx Filter input unconnected.

(2) Refer to [Table 3](#).

(3) For capacitor value C, f is the desired lower cutoff frequency and 22 kΩ is the PA input resistance.

Figure 30. Recommended Tx Signal Chain Connections in PWM Mode Using One PWM Signal and Additional RC Filters



(1) When using both Tx Filter inputs, use 43-kΩ resistors to match the input resistance for best frequency response.

(2) Refer to [Table 3](#).

(3) For capacitor value C , f is the desired lower cutoff frequency and 22 kΩ is the PA input resistance.

Figure 31. Recommended Tx Signal Chain Connections in PWM Mode Using Two PWM Signals and Additional RC Filters

For the capacitors listed in [Table 3](#), it is recommended that these components be rated to withstand the full AV_{DD} power-supply voltage.

Table 3. Recommended External R and C Values to Increase Tx Filter Response Order in PWM Applications

| FREQUENCY BAND | R (Ω) | C (nF) |
|----------------------|-------|--------|
| SFSK: 63 kHz, 74 kHz | 510 | 2.7 |
| CENELEC A | 510 | 1.5 |
| CENELEC B, C, D | 510 | 1 |

The Tx PGA and Tx Filter each have the inputs and outputs externally available in order to provide maximum system design flexibility. Care should be taken when laying out the PCB traces from the inputs or outputs to avoid excessive capacitive loading. Keeping the PCB capacitance from the inputs to ground, or from the outputs to ground, less than 100 pF is recommended.

9.3.3 Rx Block

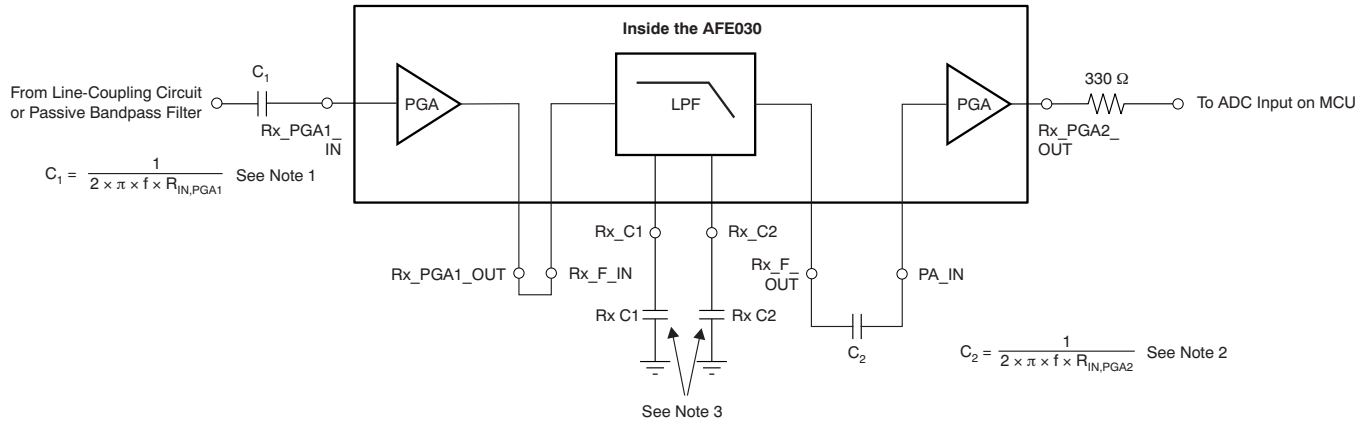
The Rx block consists of Rx PGA1, the Rx Filter, and Rx PGA2. Both Rx PGA1 and Rx PGA2 are high-performance programmable gain amplifiers. Rx PGA1 can be configured through the SPI to operate as either an attenuator or in gain. The gain steps of the Rx PGA1 are 0.25 V/V, 0.5 V/V, 1 V/V, and 2 V/V. The gain steps of the Rx PGA2 are 1 V/V, 4 V/V, 16 V/V, and 64 V/V. Configuring the Rx PGA1 as an attenuator (at gains less than 1 V/V) is useful for applications where the presence of large interference signals are present within the signal band. Attenuating the large interference allows these signals to pass through the analog Rx signal chain without causing an overload; the interference signal can then be processed and removed within the microprocessor as necessary.

The Rx Filter is a very low noise, unity-gain, fourth-order low-pass filter. The Rx Filter cutoff frequency is selectable between CENELEC A or CENELEC B, C, and D modes. The [Control1 Register](#) bit location 3 setting (CA CB CD) determines the cutoff frequency. Setting [Control1 Register](#) bit location 3 to '0' selects the CENELEC A band; setting [Control1 Register](#) bit location 3 to '1' selects the CENELEC B, C, and D bands. Because the Rx Filter is a very low noise analog filter, two external capacitors are required to properly configure the Rx Filter. [Table 4](#) shows the proper capacitance values for CENELEC A, B, C, and D bands. Capacitor Rx C1 is connected between pin 24 and ground, and Rx C2 is connected between pin 23 and ground. For the capacitors shown, it is recommended that these components be rated to withstand the full AV_{DD} power-supply voltage.

Table 4. Recommended External Capacitors Required for Rx Filter

| FREQUENCY BAND | Rx C1, PIN 24 | Rx C2, PIN 23 | CUTOFF FREQUENCY (kHz) |
|-----------------|---------------|---------------|------------------------|
| CENELEC A | 680 pF | 680 pF | 90 |
| CENELEC B, C, D | 270 pF | 560 pF | 145 |

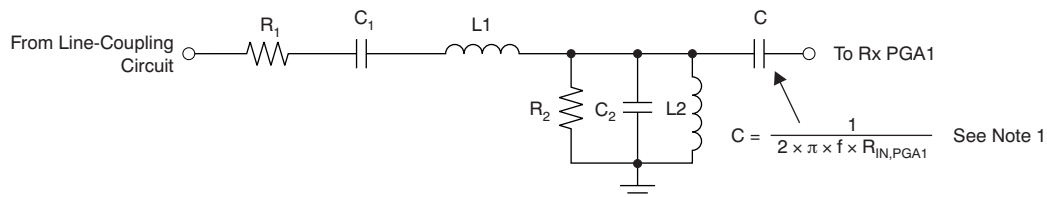
Figure 32 illustrates the recommended connections for the Rx signal chain.



- (1) For capacitor value C_1 , f is the desired lower cutoff frequency and $R_{IN,PGA1}$ is the input resistance of Rx PGA1.
- (2) For capacitor value C_2 , f is the desired lower cutoff frequency and $R_{IN,PGA2}$ is the input resistance of Rx PGA2.
- (3) Refer to Table 4.

Figure 32. Recommended Connections for Rx Signal Chain

As Figure 33 shows, a fourth-order passive passband filter is optional but recommended for applications where high performance is required. The external passive passband filter removes any unwanted, out-of-band signals from the signal path, and prevents them from reaching the active internal filters within the AFE030.



- (1) For capacitor value C , f is the desired lower cutoff frequency and $R_{IN,PGA1}$ is the input resistance of Rx PGA1. Refer to Table 4.

Figure 33. Passive Bandpass Rx Filter

The following steps can be used to quickly design the passive passband filter. (Note that these steps produce an approximate result.)

- Choose the filter characteristic impedance, Z_C :
 - For –6-db passband attenuation: $R_1 = R_2 = Z_C$
 - For 0-db passband attenuation: $R_1 = Z_C$, $R_2 = 10 \times Z_C$
- Calculate values for C_1 , C_2 , L_1 , and L_2 using the following equations:

$$C_1 = \frac{1}{(2 \times \pi \times f_1 \times Z_C)}$$

$$C_2 = \frac{1}{(2 \times \pi \times f_2 \times Z_C)}$$

$$L_1 = \frac{Z_C}{(2 \times \pi \times f_2)}$$

$$L_2 = \frac{Z_C}{(2 \times \pi \times f_1)}$$

Table 5 and Table 6 shows standard values for common applications.

Table 5. Recommended Component Values for Fourth-Order Passive Bandpass Filter (0-db Passband Attenuation)

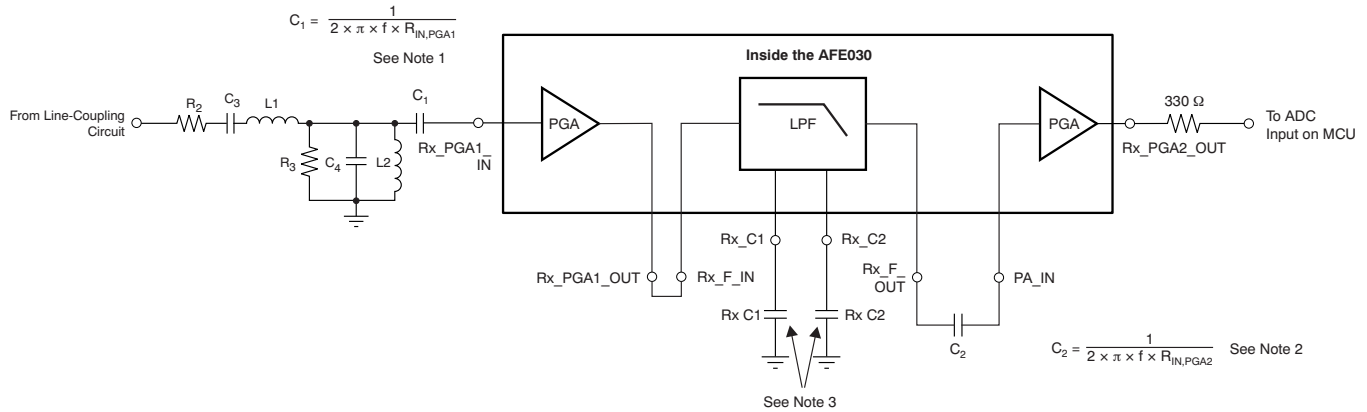
| FREQUENCY BAND | FREQUENCY RANGE (kHz) | CHARACTERISTIC IMPEDANCE (Ω) | R1 (Ω) | R2 (Ω) | C1 (nF) | C2 (nF) | L1 (μ H) | L2 (μ H) |
|-----------------|-----------------------|---------------------------------------|-----------------|-----------------|---------|---------|---------------|---------------|
| CENELEC A | 35 to 95 | 1k | 1k | 10k | 4.7 | 1.5 | 1500 | 4700 |
| CENELEC B, C, D | 95 to 150 | 1k | 1k | 10k | 1.7 | 1 | 1200 | 1500 |
| SFSK | 63 to 74 | 1k | 1k | 10k | 2.7 | 2.2 | 2200 | 2200 |

Table 6. Recommended Component Values for Fourth-Order Passive Bandpass Filter (–6-db Passband Attenuation)

| FREQUENCY BAND | FREQUENCY RANGE (kHz) | CHARACTERISTIC IMPEDANCE (Ω) | R1 (Ω) | R2 (Ω) | C1 (nF) | C2 (nF) | L1 (μ H) | L2 (μ H) |
|-----------------|-----------------------|---------------------------------------|-----------------|-----------------|---------|---------|---------------|---------------|
| CENELEC A | 35 to 95 | 1k | 1k | 1k | 4.7 | 1.5 | 1500 | 4700 |
| CENELEC B, C, D | 95 to 150 | 1k | 1k | 1k | 1.7 | 1 | 1200 | 1500 |
| SFSK | 63 to 74 | 1k | 1k | 1k | 2.7 | 2.2 | 2200 | 2200 |

The Rx PGA1, Rx Filter, and Rx PGA2 components have all inputs and outputs externally available to provide maximum system design flexibility. Care should be taken when laying out the PCB traces from the inputs or outputs to avoid excessive capacitive loading. Keeping the PCB capacitance from the inputs to ground, or outputs to ground, below 100 pF is recommended.

Figure 34 shows the complete Rx signal path, including the optional passive passband filter.



- (1) For capacitor value C_1 , f is the desired lower cutoff frequency and $R_{IN,PGA1}$ is the input resistance of Rx PGA1.
- (2) For capacitor value C_2 , f is the desired lower cutoff frequency and $R_{IN,PGA2}$ is the input resistance of Rx PGA2.
- (3) Refer to Table 4.

Figure 34. Complete Rx Signal Path (with Optional Bandpass Filter)

9.3.4 DAC Block

The DAC block consists only of the 10-bit DAC. The use of the DAC is recommended for best performance. The serial interface is used to write directly to the DAC registers when the DAC pin (pin 7) is driven high. Placing the DAC pin into a high state configures the SPI for direct serial interface to the DAC. Use the following sequence to write to the DAC:

- Set \overline{CS} low.
- Set the DAC pin (pin 7) high.
- Write a 10-bit word to DIN. The DAC register is left-justified and truncates more than 10 bits.
- \overline{CS} high updates the DAC.

Refer to [Figure 35](#) for an illustration of this sequence.

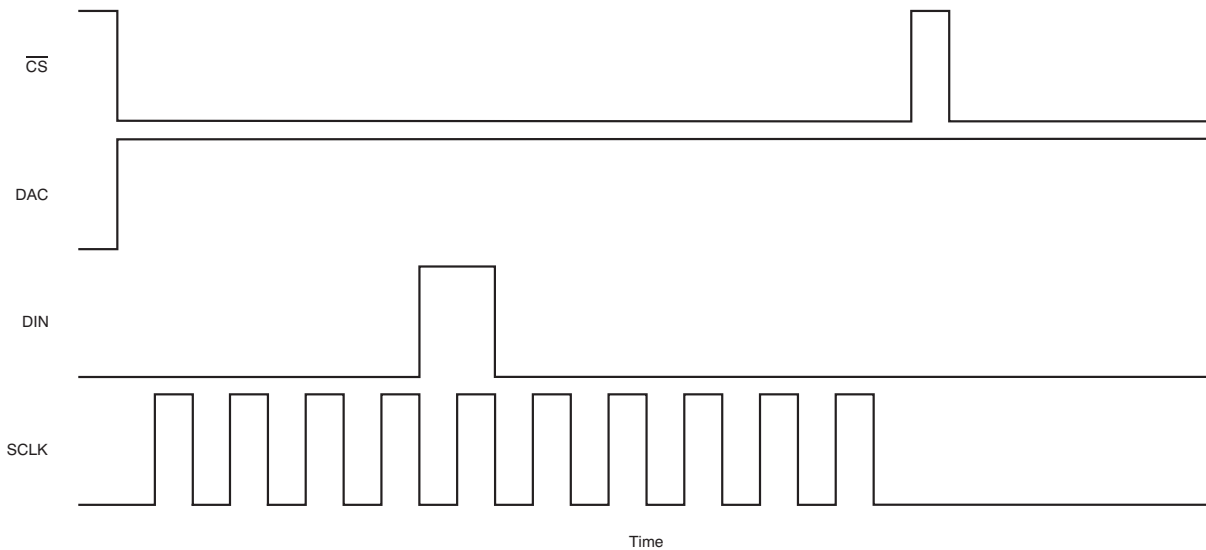


Figure 35. Writing to the DAC Register

[Table 7](#) lists the DAC Register configurations.

Table 7. DAC Registers

| DAC PIN HIGH: DAC REGISTER <15:0> | LOCATION (0 = LSB) | DEFAULT | R/W | FUNCTION |
|--------------------------------------|-----------------------|---------|-----|---------------------|
| BIT NAME | | | | |
| DAC<0> | 0 | — | W | Truncated |
| DAC<1> | 1 | — | W | Truncated |
| DAC<2> | 2 | — | W | Truncated |
| DAC<3> | 3 | — | W | Truncated |
| DAC<4> | 4 | — | W | Truncated |
| DAC<5> | 5 | — | W | Truncated |
| DAC<6> | 6 | — | W | DAC bit 0 = DAC LSB |
| DAC<7> | 7 | — | W | DAC bit 1 |
| DAC<8> | 8 | — | W | DAC bit 2 |
| DAC<9> | 9 | — | W | DAC bit 3 |
| DAC<10> | 10 | — | W | DAC bit 4 |
| DAC<11> | 11 | — | W | DAC bit 5 |
| DAC<12> | 12 | — | W | DAC bit 6 |
| DAC<13> | 13 | — | W | DAC bit 7 |
| DAC<14> | 14 | — | W | DAC bit 8 |
| DAC<15> | 15 | — | W | DAC bit 9 = DAC MSB |

9.3.5 REF1 and REF2 Blocks

The REF1 and REF2 blocks create midscale power-supply biasing points used internally to the AFE030. Each reference divides its respective power-supply voltage in half with a precision resistive voltage divider. REF1 provides a $PA_V_S/2$ voltage at the output of the PA, while REF2 provides an $AV_{DD}/2$ voltage at the outputs of the Tx PGA, Tx Filter, Rx PGA1, Rx Filter, and Rx PGA2. Each REF block has its output brought out to an external pin that can be used for filtering and noise reduction. Figure 36 and Figure 37 show the proper connections of the external noise-reducing capacitors. These capacitors are optional, but are recommended for best performance.

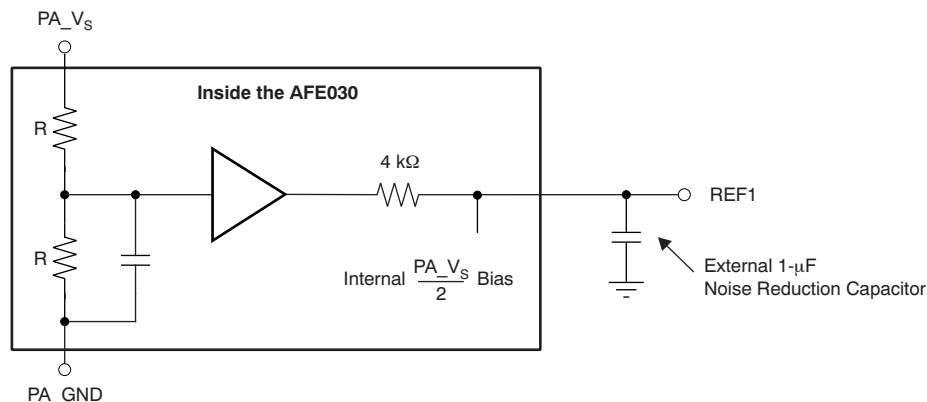


Figure 36. REF1 Functional Diagram

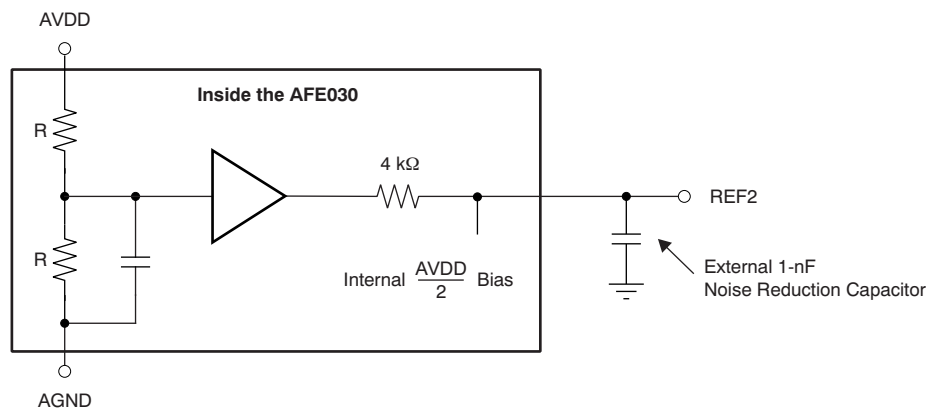


Figure 37. REF2 Functional Diagram

9.3.6 Zero Crossing Detector Block

The AFE030 includes two zero crossing detectors. Zero crossing detectors can be used to synchronize communications signals to the ac line or sources of noise. Typically, in single-phase applications, only a single zero crossing detector is used. In three-phase applications, both zero crossing detectors can be used; one component detects phase A, and one detects phase B. Phase C zero crossings can then be inferred from the data gathered from the other phases. Figure 38 shows the AFE030 configured for non-isolated zero crossing detection.

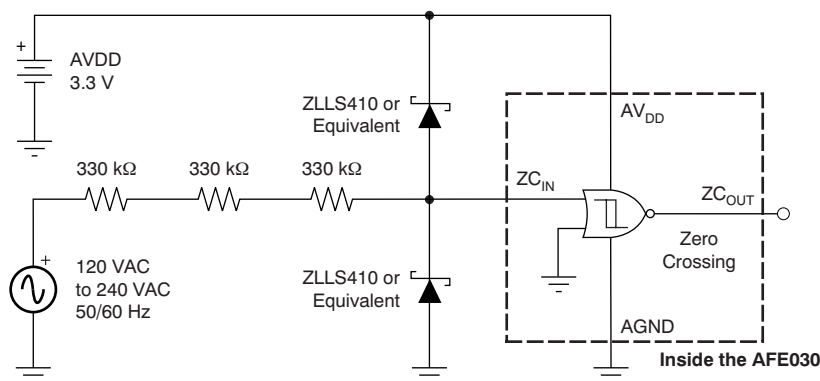


Figure 38. Non-Isolated Zero Crossing Detection Using the AFE030

Non-isolated zero crossing waveforms are shown in Figure 39.

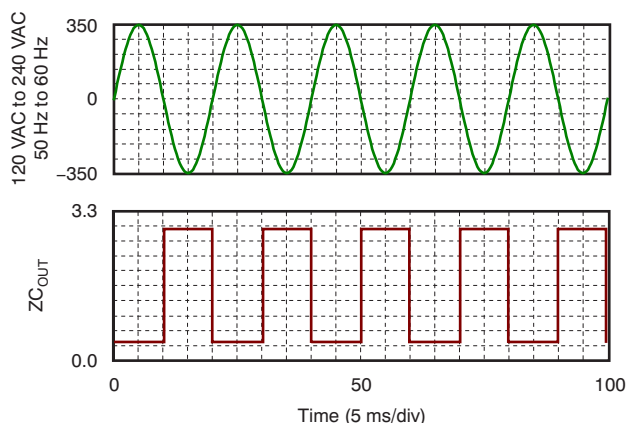


Figure 39. Non-Isolated Zero Crossing Waveforms

For maximum protection of the AFE030 against line transients, it is recommended to use Schottky diodes as indicated in [Figure 38](#). These diodes should limit the ZC_IN pins (pins 38 and 39) to within the maximum rating of ($AV_{DD} + 0.4\text{ V}$) and ($AGND - 0.4\text{ V}$). Some applications may require an isolated zero crossing detection circuit. With a minimal amount of components, the AFE030 can be configured for isolated zero crossing detection, as [Figure 40](#) shows.

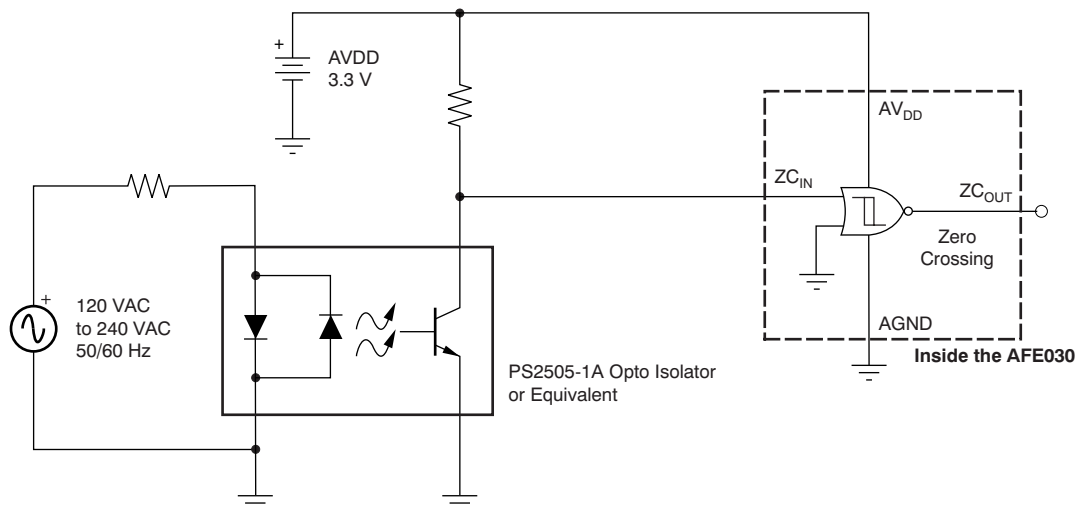


Figure 40. Isolated Zero Crossing Detection Using the AFE030

Isolated zero crossing waveforms are shown in [Figure 41](#).

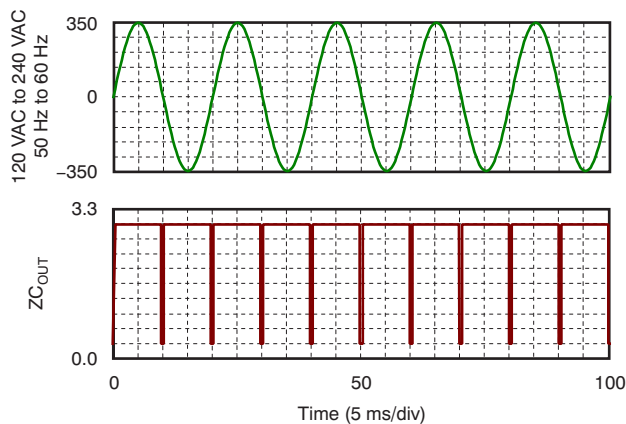


Figure 41. Isolated Zero Crossing Waveforms

9.3.7 ETx and ERx Blocks

The AFE030 contains a two-wire transmitter block, ETx, and a two-wire receiver block, ERx. These blocks support communications that use amplitude shift keying (ASK) with on-off keying (OOK) modulation.

The ETx block is a gated driver that allows for transmission of a carrier input signal and modulating input signal. For typical applications, a 50-kHz square wave carrier signal is applied to E_Tx_Clk while the modulating signal is applied to E_Tx_In. The output (E_Tx_Out) is then in a high-impedance state when E_Tx_In is '1'. [Figure 42](#) shows the relationship between E_Tx_Clk, E_Tx_In, and E_Tx_Out.

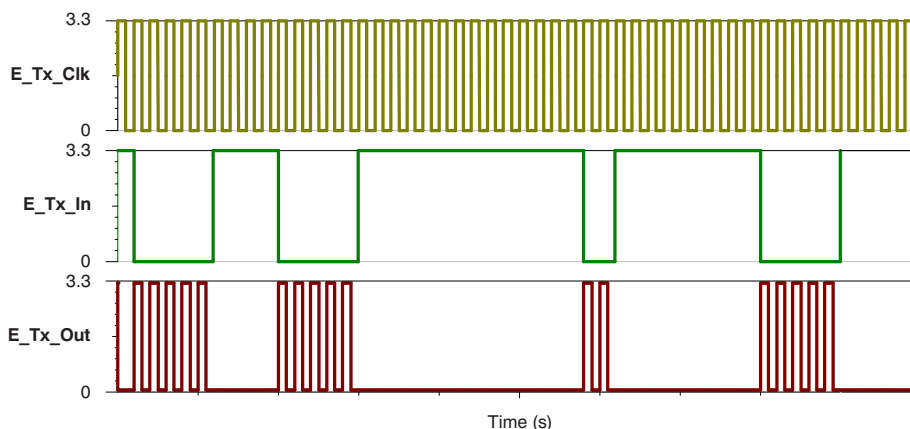


Figure 42. ETx Block Transfer Function

The ERx Block consists of a low-pass analog filter configured in an inverting gain of -4.5 db. This block, along with an external capacitor, can be used to create a passband filter response as shown in [Figure 43](#).

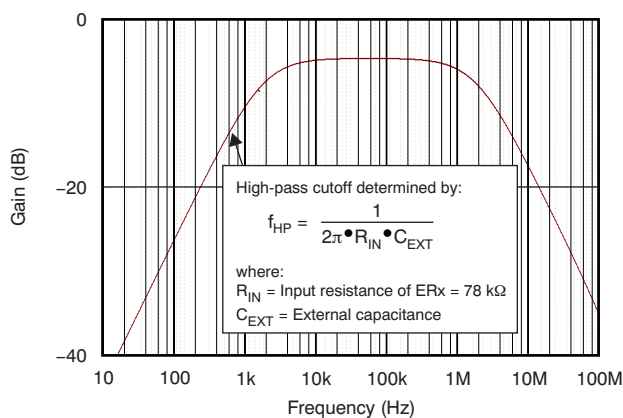


Figure 43. ERx Block Frequency Response

The E_Rx_Out pin can be directly connected to either an available analog-to-digital converter (ADC) input or GPIO on the host microcontroller. [Figure 44](#) illustrates a typical two-wire application for ETx and ERx.

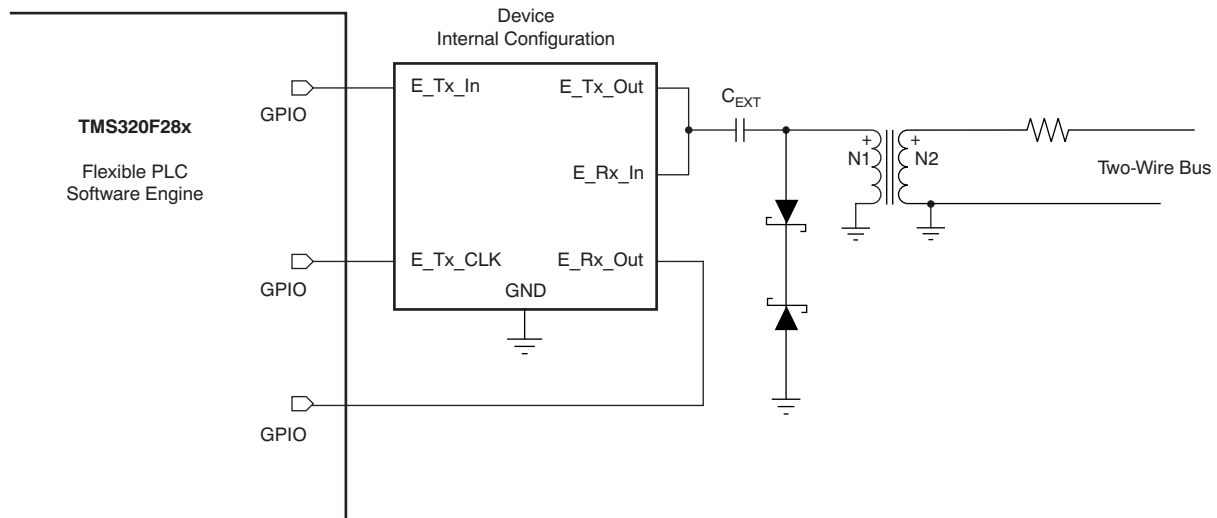


Figure 44. Typical Two-Wire Application for ETx and ERx

9.4 Power Supplies

The AFE030 has two low-voltage analog power-supply pins and one low-voltage digital supply pin. Internally, the two analog supply pins are connected to each other through back-to-back electrostatic discharge (ESD) protection diodes. These pins must be connected to each other on the application printed circuit board (PCB). It is also recommended to connect the digital supply pin and the two analog supply pins together on the PCB. Both low-voltage analog ground pins are also connected internally through back-to-back ESD protection diodes. These ground pins should also be connected to the digital ground pin on the PCB. It is recommended to bypass the low-voltage power supplies with a parallel combination of a 10- μ F and 100-nF capacitor. The PA block is biased separately from a high-voltage, high-current supply.

Two PA power supply pins and two PA ground pins are available to provide a path for the high currents associated with driving the low impedance of the ac mains. Connecting the two PA supply pins together as close as possible to the AFE030 is recommended. It is also recommended to place a bypass capacitor of 47 μ F to 100 μ F in parallel with 100 nF as close as possible to the AFE030. Care must be taken when routing the high current ground lines on the PCB to avoid creating voltage drops in the PCB ground that may vary with changes in load current.

The AFE030 has many options to enable or disable the functional blocks to allow for flexible power-savings modes. [Table 8](#) shows the specific power supply that each functional block draws power from, as well as the typical amount of power drawn from the associated power supplies for both the enabled and disabled states. For additional information on power-supply requirements refer to Application Report [Analog Front-End Design for a Narrowband Power-Line Communications Modem Using the AFE031](#), literature number SBOA130 (available for download at www.ti.com).

Table 8. Power Consumption with Enable and Disable Times (Typical)

| BLOCK | STATUS | ENABLE TIME | DISABLE TIME | AVDD SUPPLY CURRENT | DVDD SUPPLY CURRENT | PA SUPPLY CURRENT |
|-------|--------|-------------|--------------|---------------------|---------------------|-------------------|
| PA | On | 10 μ s | — | — | — | 40 mA |
| | Off | — | 10 μ s | — | — | 70 μ A |
| Tx | On | 10 μ s | — | 3.7 mA | — | — |
| | Off | — | 10 μ s | 1 μ A | — | — |
| Rx | On | 10 μ s | — | 5.3 mA | — | — |
| | Off | — | 10 μ s | 1 μ A | — | — |
| ERx | On | 10 μ s | — | 900 μ A | — | — |
| | Off | — | 10 μ s | 1 μ A | — | — |
| ETx | On | 10 μ s | — | 1.2 mA | — | — |
| | Off | — | 10 μ s | 1 μ A | — | — |
| DAC | On | 10 μ s | — | — | 16 μ A | — |
| | Off | — | 10 μ s | — | 1 μ A | — |
| ZC | On | 10 μ s | — | 25 μ A | — | — |
| | Off | — | 10 μ s | 1 μ A | — | — |
| REF1 | On | 10 μ s | — | — | — | 26 μ A |
| | Off | — | 10 μ s | — | — | 8 μ A |
| REF2 | On | 10 μ s | — | 25 μ A | — | — |
| | Off | — | 10 μ s | 4 μ A | — | — |

9.5 Pin Descriptions

DAC (Pin 7)

The DAC pin is used to configure the SPI to either read or write data to the Command and Data Registers, or to write data to the DAC registers. Setting the DAC pin high allows access to the DAC registers. Setting the DAC pin low allows access to the Command and Data Registers.

SD (Pin 8)

The Shutdown pin (SD) can be used to shut down the entire AFE030 for maximum power savings. When the SD pin is low, normal operation of the AFE030 occurs. When the SD pin is high, all circuit blocks within the AFE030, including the serial interface, are placed into the lowest-power operating modes. In this condition, the entire AFE030 draws only 95 μ A of current. All register contents at the time the AFE030 is placed into shutdown mode are saved; upon re-enabling the AFE030, the register contents retain the respective saved values.

INT (Pin 9)

The Interrupt pin (INT) can be used to signal the microprocessor of an unusual operating condition that results from an anomaly on the ac mains. The INTpin can be triggered by two external circuit conditions, depending upon the Enable Register settings. The AFE030 can be programmed to issue an interrupt on these conditions:

- Current overload
- Thermal overload

9.5.1 Current Overload

The maximum output current allowed from the Power Amplifier can be programmed with the external R_{SET} resistor connected between PA_ISET (pin 46) and ground. If a fault condition should occur and cause an overcurrent event for the PA, the PA goes into current limit and the I_FLAG bit (location 6 in the [RESET Register](#)) is set to a '1' if the I_Flag_EN bit (location 6 in the [Control2 Register](#)) is enabled. This configuration results in an interrupt signal at the INT pin. The I_FLAG bit remains set to '1' even after the device returns to normal operation. The I_FLAG bit remains at '1' until it is reset by the microprocessor.

If the I_FLAG_EN bit (location 6 in the [Control2 Register](#)) is disabled and a current overload condition occurs, the PA goes into current-limit mode to protect the AFE030; however, the contents of the I_FLAG bit (location 6 in the [RESET Register](#)) remain at the respective previous values (presumably '0' for normal operation), and the AFE030 does not issue an interrupt at the INT pin.

9.5.2 Thermal Overload

The AFE030 contains internal protection circuitry that automatically disables the PA output stage if the junction temperature exceeds +165°C. If a fault condition occurs that causes a thermal overload, and if the T_FLAG_EN bit (location 5 in the [Control2 Register](#)) is enabled, the T_FLAG bit (location 5 in the [RESET Register](#)) is set to a '1'. This configuration results in an interrupt signal at the INT pin. The AFE030 includes a thermal hysteresis and allows the PA to resume normal operation when the junction temperature reduces to 145°C. The T_FLAG bit remains set to a '1' even after the device returns to normal operation. The T_FLAG bit remains '1' until it is reset by the microprocessor.

If the T_FLAG_EN bit (location 5 in the [Control2 Register](#)) is disabled and a thermal overload condition occurs, the PA continues to go into thermal limit and protect the AFE030, but the contents of the T_FLAG bit (location 5 in the [RESET Register](#)) remain at the previous value (presumably '0' for normal operation), and the AFE030 does not issue an interrupt at the INT pin.

Once an interrupt is signaled (that is, INT goes low), the contents of the I_FLAG and T_FLAG bits can be read by the microprocessor to determine the type of interrupt that occurred. Using the [Control2 Register](#), each interrupt type (current or thermal) can be individually enabled or disabled, allowing full user customization of the INT function. For proper operation of the interrupt pin it is recommended to configure the interrupt enable registers in the [Control2 Register](#) by writing to bit locations 5, 6, and 7 following the information in [Table 9](#) after each time the AFE030 is powered on. Failure to properly configure bit locations 5, 6, and 7 after power on may result in unexpected interrupt signals.

Pin Descriptions (continued)

Table 9 lists the register contents associated with each interrupt condition.

Table 9. Register Contents to Configure the Interrupt Pin

| FUNCTION | CONTROL2 REGISTER CONTENTS: DETERMINE INTERRUPT PIN FUNCTIONALITY | | |
|--|--|---------------------------------|---------------------------------|
| | D7 | I_FLAG_EN (CURRENT OVERLOAD) | T_FLAG_EN (THERMAL OVERLOAD) |
| | | D6 | D5 |
| POR (default values) | undefined | 0 | 0 |
| No interrupt | 0 | 0 | 0 |
| Interrupt on thermal overload only | 0 | 0 | 1 |
| Interrupt on current overload only | 0 | 1 | 0 |
| Interrupt on thermal or current overload | 0 | 1 | 1 |

TSENSE Pin (10)

The TSENSE pin is internally connected to the anode of a temperature-sensing diode located within the PA output stage. Figure 45 shows a remote junction temperature sensor circuit that can be used to measure the junction temperature of the AFE030. Measuring the junction temperature of the AFE030 is optional and not required.

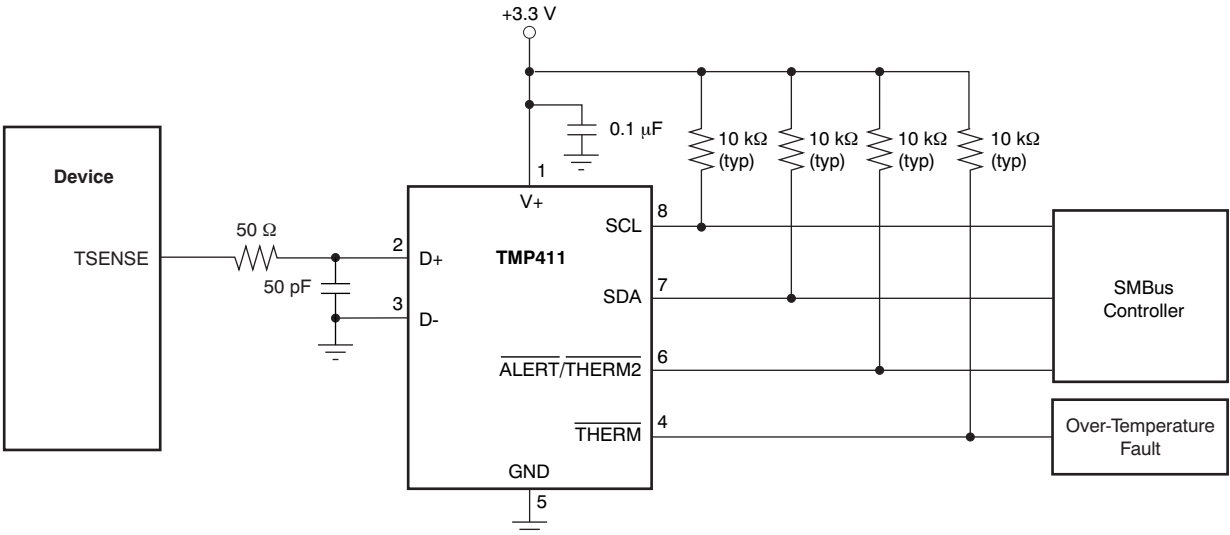


Figure 45. Interfacing the TMP411 to the AFE030

Tx_FLAG (Pin 47)

The Tx_FLAG pin is an open drain output that indicates the readiness of the Tx signal path for transmission. When the Tx_FLAG pin is high, the transmit signal path is enabled and ready for transmission. When the Tx_FLAG pin is low, the transmit path is not ready for transmission.

Rx_FLAG (Pin 48)

The Rx_FLAG pin is an open drain output that indicates the readiness of the Rx signal path for transmission. When the Rx_FLAG pin is high, the transmit signal path is enabled and ready for transmission. When the Rx_FLAG pin is low, the transmit path is not ready for transmission.

9.6 Calibration Modes

The AFE030 can be configured for two different calibration modes: Tx Calibration and Rx Calibration. Calibration values can be determined during the calibration process and stored in system memory. A one-time calibration can be performed the first time that the system powers on; this calibration remains valid over the full temperature range and operating life of the AFE030, independent of the number of power-on/power-off cycles, as long as the calibration factors remain in the system memory. Calibration mode is accessed through the [Control1 Register](#). Note that calibration is not required.

9.6.1 Tx Calibration Mode

The Tx PGA + Tx Filter ac gain can be calibrated in Tx Calibration Mode. [Figure 46](#) shows the signal path during Tx Calibration mode.

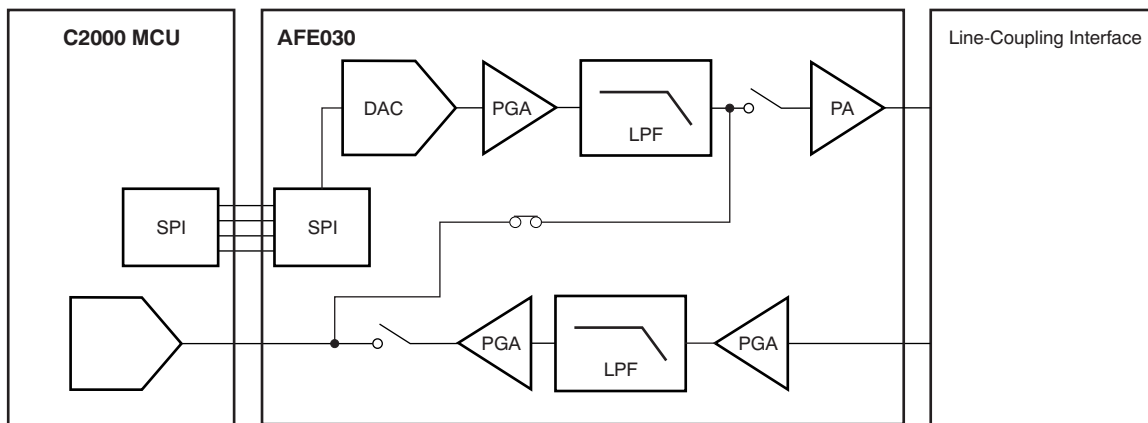


Figure 46. Tx Calibration Mode Configuration

9.6.2 Rx Calibration Mode

The Tx PGA + Rx PGA1 + Rx Filter + Rx PGA2 ac gain can be calibrated in Rx Calibration mode. [Figure 47](#) shows the signal path during Rx Calibration mode.

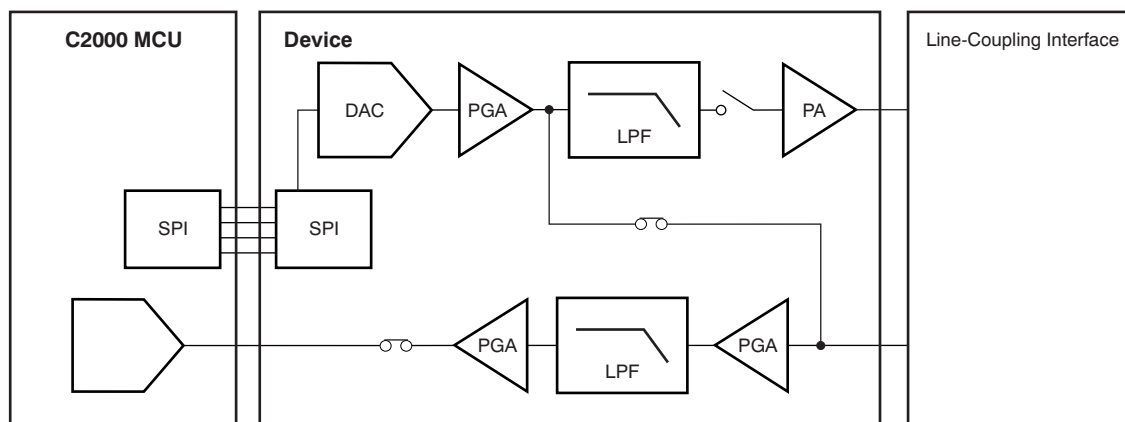


Figure 47. Rx Calibration Mode Configuration

9.7 Serial Interface

The AFE030 is controlled through a serial interface that allows read/write access to the control and data registers. A host SPI frame consists of a R/W bit, a 6-bit register address, and eight data bits. Data are shifted out on the falling edge of SCLK and latched on the rising edge of SCLK. Refer to the [Timing Diagrams](#) for a valid host SPI communications protocol. [Table 10](#) through [Table 19](#) show the complete register information.

Table 10. Data Register

| REGISTER | ADDRESS | DEFAULT | FUNCTION |
|-------------|---------|---------|--|
| ENABLE1 | 01h | 00h | Block enable or disable |
| GAIN SELECT | 02h | 32h | Rx and Tx gain select |
| ENABLE2 | 03h | 00h | Block enable or disable |
| CONTROL1 | 04h | 00h | Frequency select and calibration, Tx and Rx status |
| CONTROL2 | 05h | 01h | Interrupt enable |
| RESET | 09h | 00h | Interrupt status and device reset |
| DIE_ID | 0Ah | 01h | Die name |
| REVISION | 0Bh | 02h | Die revision |

Table 11. Command Register

| BIT NAME | LOCATION (15 = MSB) | R/W | FUNCTION |
|----------|------------------------|-----|---------------------------------|
| ADDR8 | 8 | W | Register address bit |
| ADDR9 | 9 | W | Register address bit |
| ADDR10 | 10 | W | Register address bit |
| ADDR11 | 11 | W | Register address bit |
| ADDR12 | 12 | W | Register address bit |
| ADDR13 | 13 | W | Register address bit |
| ADDR14 | 14 | W | Register address bit |
| R/W | 15 | W | Read/write: read = 1, write = 0 |

**Table 12. Enable1 Register: Address 00h
Default: 00h**

| Enable1 Register <7:0> | | | | |
|------------------------|-----------------------|---------|-----|---|
| BIT NAME | LOCATION (0 = LSB) | DEFAULT | R/W | FUNCTION |
| PA | 0 | 0 | R/W | This bit is used to enable/disable the PA block. 0 = Disabled 1 = Enabled |
| TX | 1 | 0 | R/W | This bit is used to enable/disable the Tx block. 0 = Disabled 1 = Enabled |
| RX | 2 | 0 | R/W | This bit is used to enable/disable the Rx block. 0 = Disabled 1 = Enabled |
| ERX | 3 | 0 | R/W | This bit is used to enable/disable the ERx block. 0 = Disabled 1 = Enabled |
| ETX | 4 | 0 | R/W | This bit is used to enable/disable the ETx block. 0 = Disabled 1 = Enabled |
| DAC | 5 | 0 | R/W | This bit is used to enable/disable the DAC block. 0 = DAC disabled; switch is connected to Tx_PGA_IN pin. 1 = DAC enabled; switch is connected to DAC output. |
| — | 6 | 0 | — | Reserved |
| — | 7 | 0 | — | Reserved |

Table 13. Gain Select Register: Address 02h
Default: 32h

| Gain Select Register <7:0> | | | | |
|----------------------------|-----------------------|---------|-----|--|
| BIT NAME | LOCATION (0 = LSB) | DEFAULT | R/W | FUNCTION |
| RX1G-0, RX1G-1 | 0, 1 | 0, 1 | R/W | This bit is used to set the gain of the Rx PGA1. 00 = 0.25 V/V 01 = 0.5 V/V 10 = 1 V/V 11 = 2 V/V |
| RX2G-0, RX2G-1 | 2, 3 | 0, 0 | R/W | This bit is used to set the gain of the Rx PGA2. 00 = 1 V/V 01 = 4 V/V 10 = 16 V/V 11 = 64 V/V |
| TXG-0, TXG-1 | 4, 5 | 1, 1 | R/W | This bit is used to set the gain of the Tx PGA. 00 = 0.25 V/V 01 = 0.5 V/V 10 = 0.707 V/V 11 = 1 V/V |
| — | 6 | 0 | — | Reserved |
| — | 7 | 0 | — | Reserved |

Table 14. Enable2 Register: Address 03h
Default: 00h

| Enable2 Register <7:0> | | | | |
|------------------------|-----------------------|---------|-----|--|
| BIT NAME | LOCATION (0 = LSB) | DEFAULT | R/W | FUNCTION |
| ZC | 0 | 0 | R/W | This bit is used to enable/disable the ZC block. 0 = Disabled 1 = Enabled |
| REF1 | 1 | 0 | R/W | This bit is used to enable/disable the REF1 block. 0 = Disabled 1 = Enabled |
| REF2 | 2 | 0 | R/W | This bit is used to enable/disable the REF2 block. 0 = Disabled 1 = Enabled |
| PA_OUT | 3 | 0 | R/W | This bit is used to enable/disable the PA output stage. When the PA output stage is enabled it functions normally with a low output impedance, capable of driving heavy loads. When the PA output stage is disabled it is placed into a high impedance state. 0 = Disabled 1 = Enabled |
| — | 4 | 0 | — | Reserved |
| — | 5 | 0 | — | Reserved |
| — | 6 | 0 | — | Reserved |
| — | 7 | 0 | — | Reserved |

Table 15. Control1 Register: Address 04h
Default: 00h

| Control1 Register <7:0> | | | | |
|-------------------------|-----------------------|---------|-----|--|
| BIT NAME | LOCATION (0 = LSB) | DEFAULT | R/W | FUNCTION |
| TX_CAL | 0 | 0 | R/W | This bit is used to enable/disable the TX calibration mode. 0 = Disabled 1 = Enabled |
| RX_CAL | 1 | 0 | R/W | This bit is used to enable/disable the RX calibration mode. 0 = Disabled 1 = Enabled |
| — | 2 | 0 | — | Reserved |
| CA_CBCD | 3 | 0 | R/W | This bit is used to select the frequency response of the Tx filter and Rx filter. 0 = CENELEC A 1 = CENELEC B, C, D |
| — | 4 | 0 | — | Reserved |
| — | 5 | 0 | — | Reserved |
| TX_FLAG | 6 | 0 | R | This bit is used to indicate the status of the Tx block. 0 = Tx block is not ready for transmission 1 = Tx block is ready for transmission |
| RX_FLAG | 7 | 0 | R | This bit is used to indicate the status of the Rx block. 0 = Rx block is not ready for reception 1 = Rx block is ready for reception |

Table 16. Control2 Register: Address 05h
Default: 01h

| Control2 Register <7:0> | | | | |
|-------------------------|-----------------------|---------|-----|---|
| BIT NAME | LOCATION (0 = LSB) | DEFAULT | R/W | FUNCTION |
| — | 0 | 0 | — | Reserved |
| — | 1 | 0 | — | Reserved |
| — | 2 | 0 | — | Reserved |
| — | 3 | 0 | — | Reserved |
| — | 4 | 0 | — | Reserved |
| T_FLAG_EN | 5 | 0 | R/W | This bit is used to enable/disable the T_flag bit in the RESET Register. 0 = Disabled 1 = Enabled |
| I_FLAG_EN | 6 | 0 | R/W | This bit is used to enable/disable the I_flag bit in the RESET Register. 0 = Disabled 1 = Enabled |
| — | 7 | X | — | Reserved |

**Table 17. RESET Register: Address 09h
Default: 00h**

| Reset Register <7:0> | | | | |
|---------------------------------------|-----------------------|---------|-----|--|
| BIT NAME | LOCATION (0 = LSB) | DEFAULT | R/W | FUNCTION |
| -- | 0 | 0 | -- | Reserved |
| -- | 1 | 0 | -- | Reserved |
| SOFTTRST0, SOFTTRST1, SOFTTRST2 | 2, 3, 4 | 0, 0, 0 | W | These bits are used to perform a software reset of the ENABLE1, ENABLE2, CONTROL2, CONTROL3, and GAIN SELECT registers. Writing '101' to these registers performs a software reset. |
| T_FLAG | 5 | 0 | R/W | This bit is used to indicate the status of a PA thermal overload. 0 = On read, indicates that no thermal overload has occurred since the last reset. 0 = On write, resets this bit. 1 = On read, indicates that a thermal overload has occurred since the last reset. Remains latched until reset. |
| I_FLAG | 6 | 0 | R/W | This bit is used to indicate the status of a PA output current overload. 0 = On read indicates that no current overload has occurred since the last reset. 0 = On write, resets this bit. 1 = On read indicates that a current overload has occurred since the last reset. Remains latched until reset. |
| — | 7 | 0 | — | Reserved |

**Table 18. DieID Register: Address 0Ah
Default: 01h**

| DieID Register <7:0> | | | | |
|----------------------|-----------------------|---------|-----|-----------------------------------|
| BIT NAME | LOCATION (0 = LSB) | DEFAULT | R/W | FUNCTION |
| DIE ID<0> | 0 | 1 | R | The DieID Register is hard-wired. |
| DIE ID<1> | 1 | 0 | R | The DieID Register is hard-wired. |
| DIE ID<2> | 2 | 0 | R | The DieID Register is hard-wired. |
| DIE ID<3> | 3 | 0 | R | The DieID Register is hard-wired. |
| DIE ID<4> | 4 | 0 | R | The DieID Register is hard-wired. |
| DIE ID<5> | 5 | 0 | R | The DieID Register is hard-wired. |
| DIE ID<6> | 6 | 0 | R | The DieID Register is hard-wired. |
| DIE ID<7> | 7 | 0 | R | The DieID Register is hard-wired. |

**Table 19. Revision Register: Address 0Bh
Default: 02h**

| Revision Register <7:0> | | | | |
|-------------------------|-----------------------|---------|-----|--------------------------------------|
| BIT NAME | LOCATION (0 = LSB) | DEFAULT | R/W | FUNCTION |
| REVISION ID<0> | 0 | 0 | R | The Revision Register is hard-wired. |
| REVISION ID<1> | 1 | 1 | R | The Revision Register is hard-wired. |
| REVISION ID<2> | 2 | 0 | R | The Revision Register is hard-wired. |
| REVISION ID<3> | 3 | 0 | R | The Revision Register is hard-wired. |
| REVISION ID<4> | 4 | 0 | R | The Revision Register is hard-wired. |
| REVISION ID<5> | 5 | 0 | R | The Revision Register is hard-wired. |
| REVISION ID<6> | 6 | 0 | R | The Revision Register is hard-wired. |
| REVISION ID<7> | 7 | 0 | R | The Revision Register is hard-wired. |

10 Application and Implementation

NOTE

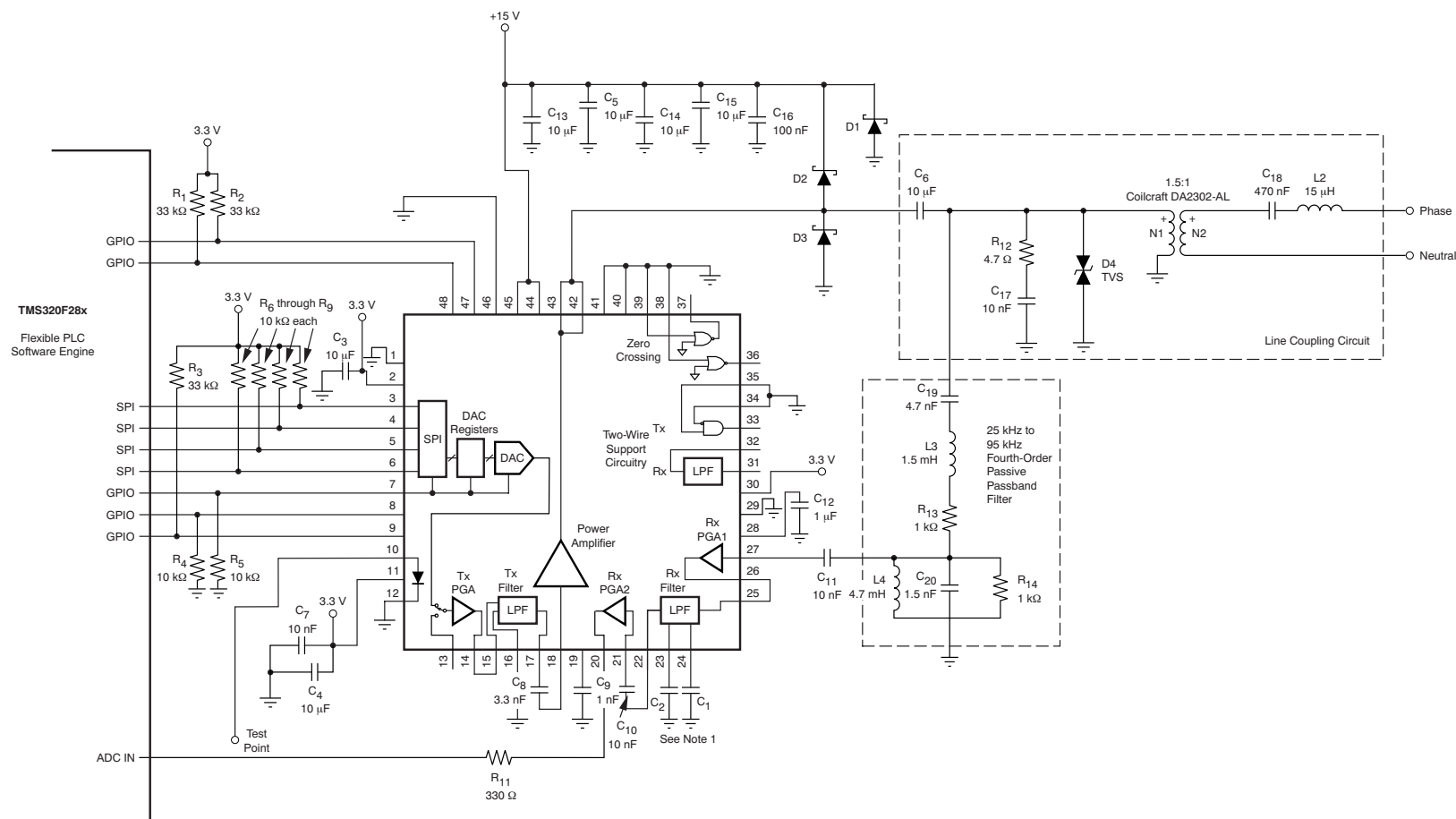
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The AFE030 is an integrated powerline communication analog front-end (AFE) device built from a variety of functional blocks that work in conjunction with a microcontroller. The AFE030 provides the interface between the microcontroller and a line coupling circuit. The AFE030 delivers high performance and is designed to work with a minimum number of external components. Consisting of a variety of functional and configurable blocks, the AFE030 simplifies design efforts and reduces the time to market of many applications.

10.2 Typical Application

[Figure 48](#) shows the AFE030 configured in a typical PLC analog front-end application. The schematic shows the connections to the microprocessor and ac line. The values of the passive components in [Figure 48](#) are suitable for a single-phase powerline communications application in the CENELEC A band, connected to a 120-VAC or 240-VAC, 50-Hz or 60-Hz ac line.



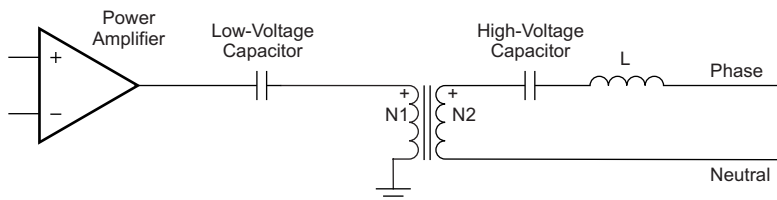
(1) Recommended values for C1 and C2:

1. C1:
 - CENELEC A: 680 pF
 - CENELEC B, C, D: 270 pF
2. C2:
 - CENELEC A: 680 pF
 - CENELEC B, C, D: 560 pF

Figure 48. Typical Powerline Communications Modem Application

10.3 Line-Coupling Circuit

The line-coupling circuit is one of the most critical circuits in a powerline modem. The line-coupling circuit has two primary functions: first, to block the low-frequency signal of the mains (commonly 50 Hz or 60 Hz) from damaging the low-voltage modem circuitry; second, to couple the modem signal to and from the ac mains. A typical line-coupling circuit is shown in Figure 49.



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Figure 49. Simplified Line Coupling Circuit

For additional information on line-coupling interfaces with the AFE030, refer to Application Report SBOA130 *Analog Front-End Design for a Narrowband Power-Line Communications Modem Using the AFE031* (available for download at www.ti.com).

10.4 Circuit Protection

Powerline communications are often located in operating environments that are harsh for electrical components connected to the ac line. Noise or surges from electrical anomalies such as lightning, capacitor bank switching, inductive switching, or other grid fault conditions can damage high-performance integrated circuits if they are not properly protected. The AFE030 can survive even the harshest conditions if several recommendations are followed.

First, dissipate as much of the electrical disturbance before it reaches the AFE030 with a multi-layer approach using metal-oxide varistors (MOVs), transient voltage suppression diodes (TVSs), Schottky diodes, and a Zener diode. Figure 50 shows the recommended strategy for transient overvoltage protection.

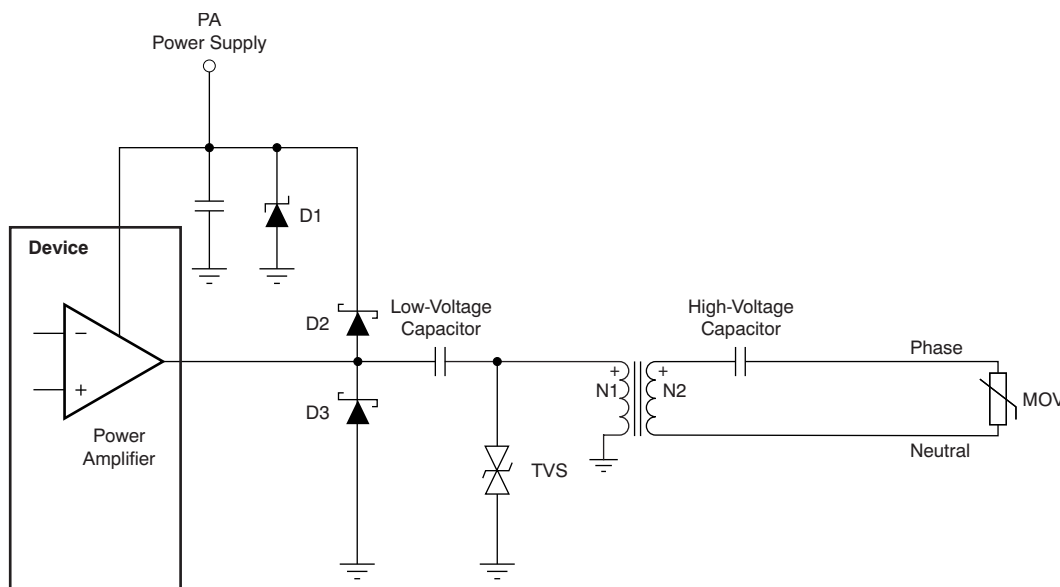


Figure 50. Transient Overvoltage Protection for AFE030

Note that the high-voltage coupling capacitor must be able to withstand pulses up to the clamping protection provided by the MOV. A metallized polypropylene capacitor, such as the 474MKP275KA from Illinois Capacitor, Inc., is rated for 50 Hz to 60 Hz, 250 VAC to 310 VAC, and can withstand 24 impulses of 2.5 kV.

Circuit Protection (continued)

Table 20 lists several recommended transient protection components.

Table 20. Recommended Transient Protection Devices

| COMPONENT | 120 VAC, 60 Hz | | |
|-----------|------------------------------|-------------------------|-----------------------------|
| | DESCRIPTION | MANUFACTURER | MFR PART NO (OR EQUIVALENT) |
| D1 | Zener diode | Diodes, Inc. | 1SMB59xxB ⁽¹⁾ |
| D2, D3 | Schottky diode | Diodes, Inc. | 1N5819HW |
| TVS | Transient voltage suppressor | Diodec Semiconductor | P6SMBJxxC ⁽²⁾ |
| MOV | Varistor | LittleFuse | TMOV20RP140E |
| HV Cap | High-voltage capacitor | Illinois Capacitor, Inc | 474MKP275KA ⁽³⁾ |

| COMPONENT | 240 VAC, 50 Hz | | |
|-----------|------------------------------|-------------------------|-----------------------------|
| | DESCRIPTION | MANUFACTURER | MFR PART NO (OR EQUIVALENT) |
| D1 | Zener diode | Diodes, Inc. | 1SMB59xxB ⁽¹⁾ |
| D2, D3 | Schottky diode | Diodes, Inc. | 1N5819HW |
| TVS | Transient voltage suppressor | Diodec Semiconductor | P6SMBJxxC ⁽²⁾ |
| MOV | Varistor | LittleFuse | TMOV20RP300E |
| HV Cap | High-voltage capacitor | Illinois Capacitor, Inc | 474MKP275KA ⁽³⁾ |

- (1) Select the Zener breakdown voltage at the lowest available rating beyond the normal power-supply operating range.
- (2) Select the TVS breakdown voltage at or slightly greater than $(0.5 \times PA_{VS})$.
- (3) A common value for the high-voltage capacitor is 470 nF. Other values may be substituted depending on the requirements of the application. Note that when making a substitution, it is important in terms of reliability that the capacitor be selected from the same family or equivalent family of capacitors rated to withstand high-voltage surges.

10.5 Thermal Considerations

In a typical powerline communications application, the AFE030 dissipates 1 W of power when transmitting into the low impedance of the ac line. This amount of power dissipation can increase the junction temperature, which in turn can lead to a thermal overload that results in signal transmission interruptions if the proper thermal design of the PCB has not been performed. Proper management of heat flow from the AFE030 as well as good PCB design and construction are required to ensure proper device temperature, maximize performance, and extend device operating life.

The AFE030 is assembled into a 7-mm² x 7-mm², 48-lead, QFN package. As Figure 51 shows, this QFN package has a large area exposed thermal pad on the underside that is used to conduct heat away from the AFE030 and into the underlying PCB.

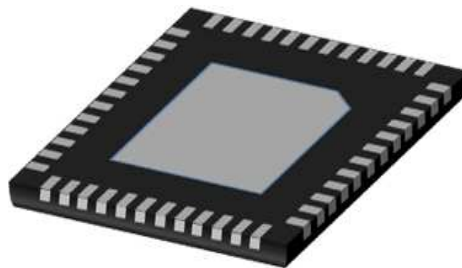


Figure 51. QFN Package with Large Area Exposed Thermal Pad

Thermal Considerations (continued)

Some heat is conducted from the silicon die surface through the plastic packaging material and is transferred into the ambient environment. Because plastic is a relatively poor conductor of heat, however, this route is not the primary thermal path for heat flow. Heat also flows across the silicon die surface to the bond pads, through the wire bonds, into the package leads, and finally into the top layer of the PCB. While both of these paths for heat flow are important, the majority (nearly 80%) of the heat flows downward, through the silicon die, into the thermally-conductive die attach epoxy, and into the exposed thermal pad on the underside of the package (as shown in [Figure 52](#)). Minimizing the thermal resistance of this downward path to the ambient environment maximizes the life and performance of the device.

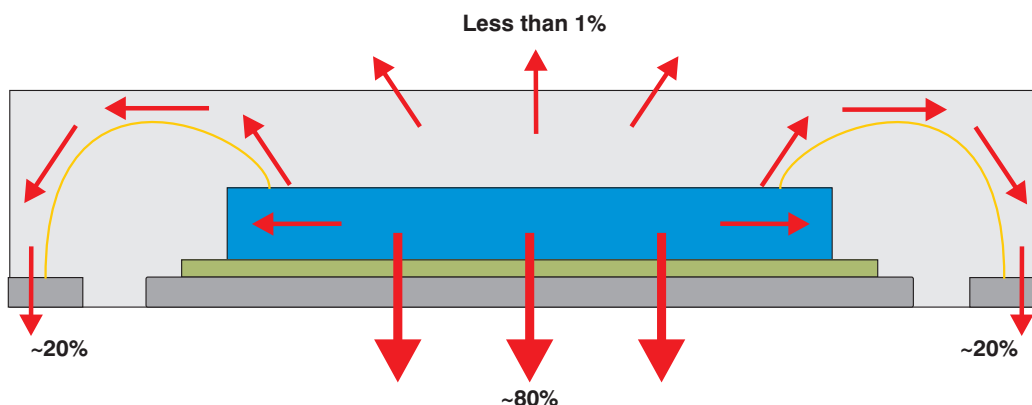


Figure 52. Heat Flow in the QFN Package

The exposed thermal pad must be soldered to the PCB thermal pad. The thermal pad on the PCB should be the same size as the exposed thermal pad on the underside of the QFN package. Refer to Application Report, *QFN/SON PCB Attachment*, literature number [SLUA271A](#), for recommendations on attaching the thermal pad to the PCB. [Figure 53](#) illustrates the direction of heat spreading into the PCB from the device.

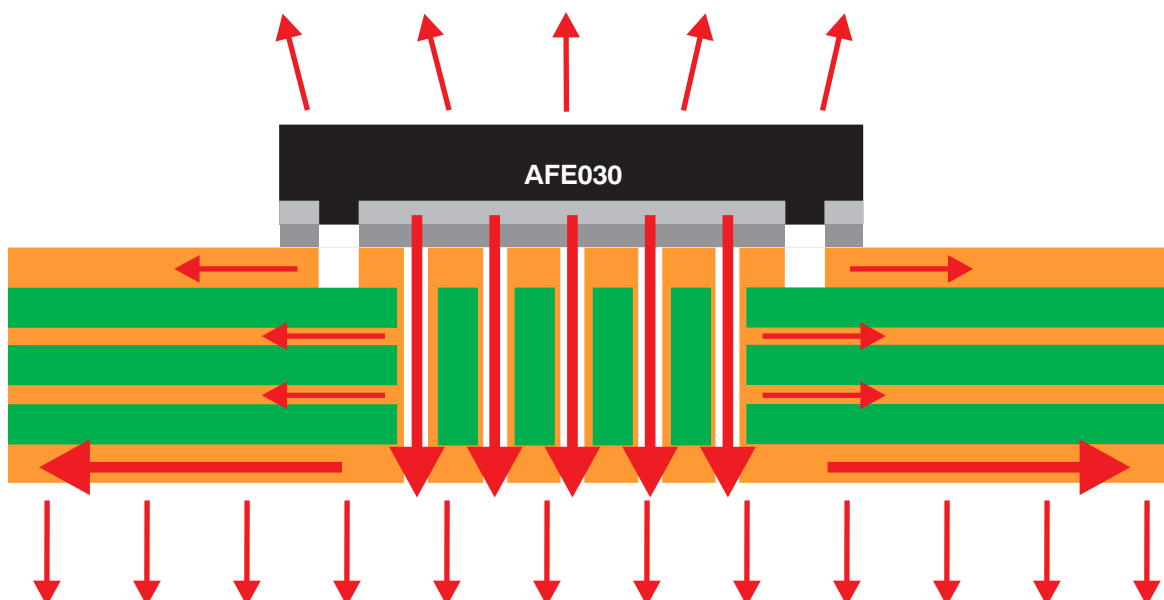


Figure 53. Heat Spreading into PCB

Thermal Considerations (continued)

The heat spreading into the PCB is maximized if the thermal path is uninterrupted. Best results are achieved if the heat-spreading surfaces are filled with copper to the greatest extent possible, maximizing the percent area covered on each layer. As an example, a thermally robust, multilayer PCB design may consist of four layers with copper (Cu) coverage of 60% in the top layer, 85% and 90% in the inner layers, respectively, and 95% on the bottom layer.

Increasing the number of layers in the PCB, using thicker copper, and increasing the PCB area are all factors that improve the spread of heat. Figure 54 through Figure 56, respectively, show thermal resistance performance as a function of each of these factors.

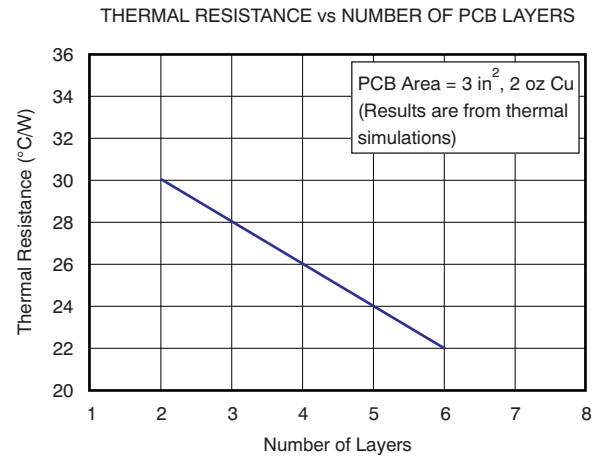


Figure 54. Thermal Resistance as a Function of the Number of Layers in the PCB

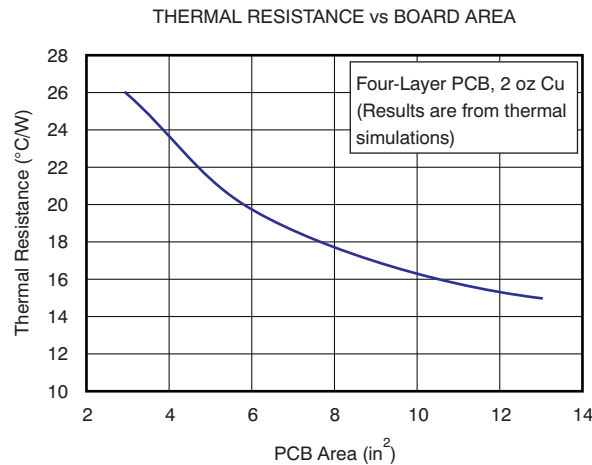


Figure 55. Thermal Resistance as a Function of PCB Area

Thermal Considerations (continued)

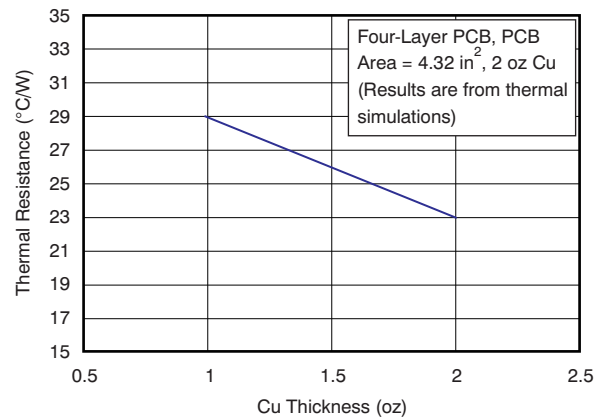


Figure 56. Thermal Resistance as a Function of Copper Thickness

For additional information on thermal PCB design using exposed thermal pad packages, refer to Application Report [SBOA130](#), *Analog Front-End Design for a Narrowband Power-Line Communications Modem Using the AFE031* and Application Report [SLMA002E](#), *PowerPAD™ Thermally-Enhanced Package* (both available for download at www.ti.com).

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 TINA-TI™ (免费下载)

TINA™是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。TINA-TI™ 是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 提供所有传统的 SPICE 直流、瞬态和频域分析以及其他设计功能。

TINA-TI 可通过模拟电子实验室设计中心[免费下载](#)，该软件提供了丰富的后处理能力，允许用户以各种方式设置结果的格式。虚拟仪器提供选择输入波形和探测电路节点、电压以及波形的功能，从而构建一个动态的快速入门工具。

注

这些文件需要安装 TINA 软件（由 DesignSoft™提供）或者 TINA-TI 软件。请从 [TINA-TI 文件夹](#) 中下载免费的 TINA-TI 软件。

11.1.1.2 TI 高精度设计

TI 高精度设计的模拟设计方案是由 TI 公司高精度模拟实验室设计应用专家创建的模拟解决方案，提供了许多实用电路的工作原理、组件选择、仿真、完整印刷电路板 (PCB) 电路原理图和布局布线、物料清单以及性能测量结果。欲获取 TI 高精度设计，请访问 <http://www.ti.com.cn/www/analog/precision-designs/>。

11.1.1.3 WEBENCH®滤波器设计器

[WEBENCH® 滤波器设计器](#)是一款简单、功能强大且便于使用的有源滤波器设计程序。借助 WEBENCH 滤波器设计器，用户可使用精选 TI 运算放大器和 TI 供应商合作伙伴提供的无源组件来构建最佳滤波器设计方案。

WEBENCH® 设计中心以基于网络的工具形式提供 [WEBENCH® 滤波器设计器](#)。用户通过该工具可在数分钟内完成多级有源滤波器解决方案的设计、优化和仿真。

11.1.2 电力线通信开发者套件

PLC 开发者套件 (TMDSPLOCKIT-V3) 可在 www.ti.com/plc 上订购。此套件提供了完整的硬件和软件解决方案，可为各种应用提供灵活、高效和可靠的网络功能。借助独特的模块化硬件架构和灵活的软件框架，TI 的 PLC 解决方案是唯一一种基于 PLC 且能够通过单一平台支持多协议标准和模块方案的技术。此技术使设计人员能够利用整个全球市场的产品线。该平台的灵活性还使开发人员能够优化特定环境工作条件下的硬件和软件性能，同时可简化端到端产品设计。基于 TI 的强大 C2000™微控制器架构和 AFE031，开发人员可以选择正确的处理能力和外设组合将电力线通信添加到现有设计中或借助 PLC 通信实施完整应用。

借助 C2000 电力线调制解调器开发者套件，可以轻松开发基于软件的 PLC 调制解调器。该套件包含两个基于 C2000 TMS320F28069 controlCARD 和 AFE031 的 PLC 调制解调器。附带的 PLC 套件软件支持多种通信技术，包括 OFDM (PRIME/G3 和 FlexOFDM) 和 SFSK。该套件还包含板载 USB JTAG 仿真和 Code Composer Studio。

11.2 文档支持

11.2.1 相关文档

如需相关文档，请参阅以下应用报告和出版物（在 www.ti.com.cn 上提供下载）：

- 《双节点、电力线通信系统的 TINA 仿真原理图》(SBOU133)
- 《数据集中器中的微控制器》(SLAT142)
- 《信号：有关运算放大器设计主题的博客文章汇编》电子版 (SLYT701)

11.3 接收文档更新通知

要接收文档更新通知，请导航至 Ti.com.cn 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 商标

PowerPAD, TINA-TI, C2000, E2E are trademarks of Texas Instruments.

WEBENCH is a registered trademark of Texas Instruments.

TINA, DesignSoft are trademarks of DesignSoft, Inc.

SPI is a trademark of Motorola, Inc.

All other trademarks are the property of their respective owners.

11.6 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| AFE030AIRGZR | Active | Production | VQFN (RGZ) 48 | 2500 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | AFE030AI |
| AFE030AIRGZR.A | Active | Production | VQFN (RGZ) 48 | 2500 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | AFE030AI |
| AFE030AIRGZT | Active | Production | VQFN (RGZ) 48 | 250 SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | AFE030AI |
| AFE030AIRGZT.A | Active | Production | VQFN (RGZ) 48 | 250 SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | AFE030AI |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| AFE030AIRGZR | VQFN | RGZ | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| AFE030AIRGZT | VQFN | RGZ | 48 | 250 | 180.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| AFE030AIRGZR | VQFN | RGZ | 48 | 2500 | 367.0 | 367.0 | 38.0 |
| AFE030AIRGZT | VQFN | RGZ | 48 | 250 | 210.0 | 185.0 | 35.0 |

GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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