ADS7128 小型 8 通道 12 位 ADC，具有 I²C 接口、GPIO 和 CRC

1 特性

- 小封装尺寸：
  - 3mm × 3mm WQFN
- 8 通道，可配置为以下任意组合：
  - 最多 8 个模拟输入、数字输入或数字输出
- 用于 I/O 扩展的 GPIO：
  - 开漏、推挽数字输出
- 模拟监控：
  - 每个通道的可编程阈值
  - 用于瞬态抑制的事件计数器
- 宽工作范围：
  - AVDD：2.35V 至 5.5V
  - DVDD：1.65V 至 5.5V
  - 温度范围：–40°C 至 +85°C
- 用于读取/写入操作的 CRC：
  - 数据读取/写入 CRC
  - 上电配置 CRC
- I²C 接口：
  - 高达 3.4MHz（高速）
  - 8 个可配置 I²C 地址
- 可编程均值滤波器
- 均方根模块：
  - 16 位真正 RMS 输出
  - 可编程 RMS 时间窗口
- 过零检测模块：
  - 对应于任何模拟输入的 ZCD 输出
  - 内置瞬态抑制和迟滞
  - 数字可调节检测阈值

2 应用

- 监控功能
- 便携式仪表
- 电器
- 电信基础设施
- 电源监控

3 说明

ADS7128 是一款易于使用的 8 通道多路复用 12 位逐次逼近寄存器模数转换器 (SAR ADC)。8 个通道可独立配置为模拟输入、数字输入或数字输出。该器件具有一个用于执行 ADC 转换过程的内部振荡器。

ADS7128 通过兼容 I²C 的接口进行通信，可以在自主或单冲转换模式下运行。ADS7128 使用具有可编程高低阈值、迟滞和事件计数器的数字窗口比较器，通过每通道事件触发的中断来实施模拟监控功能。ADS7128 具有用于数据读取/写入操作和上电配置的内置循环冗余校验 (CRC) 功能。ADS7128 具有 一个均方根 (RMS) 模块，可以为任何模拟输入通道计算 16 位真正 RMS 结果。集成式过零检测 (ZCD) 模块可以在接近越过可配置阈值时触发瞬态抑制和迟滞。

器件信息(1)

部件名称	封装	封装尺寸（标称值）
ADS7128	WQFN (16)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

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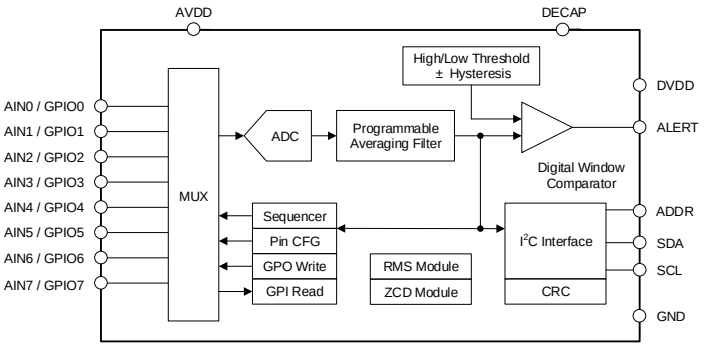
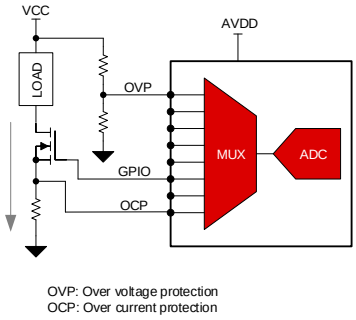
ADS7128 方框图和 应用

Device Block Diagram



Example System Architecture



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2019 年 5 月	*	初始发行版。

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5 Device Comparison Table

PART NUMBER	DESCRIPTION	CRC MODULE	ZERO-CROSSING-DETECT (ZCD) MODULE	ROOT-MEAN-SQUARE (RMS) MODULE
ADS7128	8-channel, 12-bit ADC with I^2C interface and GPIOs	Yes	Yes	Yes
ADS7138		Yes	No	No
ADS7138-Q1		Yes	No	No

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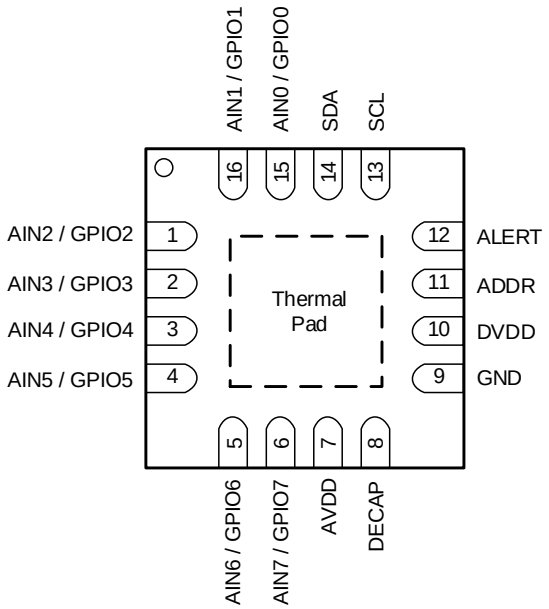
6 Pin Configuration and Functions

RTE Package
16-Pin WQFN
Top View



Pin Functions

PIN		FUNCTION(1)	DESCRIPTION
NAME	NO.		
AIN0/GPIO0	15	AI, DI, DO	Channel 0; configurable as either an analog input (default) or a general-purpose input/output (GPIO)
AIN1/GPIO1	16	AI, DI, DO	Channel 1; configurable as either an analog input (default) or a GPIO
AIN2/GPIO2	1	AI, DI, DO	Channel 2; configurable as either an analog input (default) or a GPIO
AIN3/GPIO3	2	AI, DI, DO	Channel 3; configurable as either an analog input (default) or a GPIO
AIN4/GPIO4	3	AI, DI, DO	Channel 4; configurable as either an analog input (default) or a GPIO
AIN5/GPIO5	4	AI, DI, DO	Channel 5; configurable as either an analog input (default) or a GPIO
AIN6/GPIO6	5	AI, DI, DO	Channel 6; configurable as either an analog input (default) or a GPIO
AIN7/GPIO7	6	AI, DI, DO	Channel 7; configurable as either an analog input (default) or a GPIO
ADDR	11	AI	Input for selecting the device I^2C address. Connect a resistor to this pin from DECAP pin or GND to select one of the eight addresses.
ALERT	12	Digital output	Open-drain (default) or push-pull output for the digital comparator
AVDD	7	Supply	Analog supply input, also used as the reference voltage to the ADC; connect a 1-µF decoupling capacitor to GND
DECAP	8	Supply	Connect a decoupling capacitor to this pin for the internal power supply
DVDD	10	Supply	Digital I/O supply voltage; connect a 1-µF decoupling capacitor to GND
GND	9	Supply	Ground for the power supply; all analog and digital signals are referred to this pin voltage
SDA	14	DI, DO	Serial data input or output for the I^2C interface
SCL	13	DI	Serial clock for the I^2C interface

(1) AI = analog input, DI = digital input, and DO = digital output.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
DVDD to GND	–0.3	5.5	V
AVDD to GND	–0.3	5.5	V
AINx/GPOx[2]	GND – 0.3	AVDD + 0.3	V
ADDR	GND – 0.3	2.1	V
Digital inputs	GND – 0.3	5.5	V
Current through any pin except supply pins[3]	–10	10	mA
Junction temperature, T_J	–40	125	°C
Storage temperature, T_{stg}	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) AINx/GPIOx refers to pins 1, 2, 3, 4, 5, 6, 15, and 16.
(3) Pin current must be limited to 10mA or less.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
AVDD	Analog supply voltage		2.35	3.3	5.5	V
DVDD	Digital supply voltage		1.65	3.3	5.5	V
ANALOG INPUTS						
FSR	Full-scale input range	AIN_X[1] - GND	0		AVDD	V
V_{IN}	Absolute input voltage	AIN_X - GND	–0.1		AVDD + 0.1	V
TEMPERATURE RANGE						
T_A	Ambient temperature		–40	25	85	℃

(1) AINx refers to AIN0, AIN1, AIN2, AIN3, AIN4, AIN5, AIN6, and AIN7.

7.4 Thermal Information

THERMAL METRIC[1]		ADS7128 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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7.5 Electrical Characteristics

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +85°C; typical values at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
C_{SH}	Sampling capacitance			12		pF
DC PERFORMANCE						
	Resolution	No missing codes		12		bits
DNL	Differential nonlinearity		–0.9	±0.2	0.9	LSB
INL	Integral nonlinearity		–2	±0.5	2	LSB
$V_{(OS)}$	Input offset error	Post offset calibration	–2	±0.3	2	LSB
	Input offset thermal drift	Post offset calibration		±5		ppm/°C
G_E	Gain error		–0.1	±0.05	0.1	%FSR
	Gain error thermal drift			±5		ppm/°C
AC PERFORMANCE						
SINAD	Signal-to-noise + distortion ratio	AVDD = 5 V, f_{IN} = 2 kHz	68.5	71.5		dB
		AVDD = 3 V, f_{IN} = 2 kHz	67.5	70.5		
SNR	Signal-to-noise ratio	AVDD = 5 V, f_{IN} = 2 kHz	69	72		dB
		AVDD = 3 V, f_{IN} = 2 kHz	68	71		
	Crosstalk	100-kHz signal applied on any OFF channel and measured on the ON channel		–100		dB
DECAP Pin						
	Decoupling capacitor on DECAP pin		0.22	1		µF
DIGITAL INPUT/OUTPUT (SCL, SDA)						
V_{IH}	Input high logic level	All I^2C modes	0.7 x DVDD		5.5	V
V_{IL}	Input low logic level	All I^2C modes	–0.3		0.3 x DVDD	V
V_{OL}	Output low logic level	Sink current = 2 mA, DVDD > 2 V	0		0.4	V
		Sink current = 2 mA, DVDD ≤ 2 V	0		0.2 x DVDD	
I_{OL}	Low-level output current (sink)	V_{OL} = 0.4 V, standard and fast mode			3	mA
		V_{OL} = 0.6 V, fast mode			6	
		V_{OL} = 0.4 V, fast mode plus			20	
GPIOs						
V_{IH}	Input high logic level		0.7 x AVDD		AVDD + 0.3	V
V_{IL}	Input low logic level		–0.3		0.3 x AVDD	V
	Input leakge current	GPIO configured as input		10	100	nA
V_{OH}	Output high logic level	GPO_DRIVE_CFG = push-pull, I_{SOURCE} = 2 mA	0.8 x AVDD		AVDD	V
V_{OL}	Output low logic level	I_{SINK} = 2 mA	0		0.2 x AVDD	V
I_{OH}	Output high source current	V_{OH} > 0.7 x AVDD			5	mA
I_{OL}	Output low sink current	V_{OL} < 0.3 x AVDD			5	mA
DIGITAL OUTPUT (ALERT)						
V_{OH}	Output high logic level	GPO_DRIVE_CFG = push-pull, I_{SOURCE} = 2 mA	0.8 x DVDD		DVDD	V
V_{OL}	Output low logic level	I_{SINK} = 2 mA	0		0.2 x DVDD	V
I_{OH}	Output high sink current	V_{OH} > 0.7 x DVDD			5	mA
I_{OL}	Output low sink current	V_{OL} < 0.3 x DVDD			5	mA
POWER SUPPLY CURRENTS						

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Electrical Characteristics (continued)

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +85°C; typical values at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{AVDD}	Analog supply current	I^2C high-speed mode, AVDD = 5 V		260	430	µA
		I^2C fast mode plus, AVDD = 5 V		83	140	
		I^2C fast mode, AVDD = 5 V		35	57	
		I^2C standard mode, AVDD = 5 V		10	20	
		No conversion, AVDD = 5 V		5	15	

7.6 I^2C Timing Requirements

		MODE				UNIT
		FAST MODE		HIGH-SPEED MODE		
		MIN	MAX	MIN	MAX	
f_{SCL}	SCL clock frequency(1)		1		3.4	MHz
t_{SUSTA}	START condition setup time for repeated start	260		160		ns
t_{HDSTA}	Start condition hold time	260		160		ns
t_{LOW}	Clock low period	500		160		ns
t_{HIGH}	Clock high period	260		60		ns
t_{SUDAT}	Data in setup time	50		10		ns
t_{HDDAT}	Data in hold time	0		0		ns
t_R	SCL rise time		120		80	ns
t_F	SCL fall time		120		80	ns
t_{SUSTO}	STOP condition hold time	260		60		ns
t_{BUF}	Bus free time before new transmission	500		300		ns

(1) Bus load (C_B) consideration; $C_B \leq 400$ pF for $f_{SCL} \leq 1$ MHz; $C_B < 100$ pF for $f_{SCL} = 3.4$ MHz.

7.7 Timing Requirements

at AVDD = 2.35 V to 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +85°C; typical values at T_A = 25°C.

		MIN	MAX	UNIT
t_{ACQ}	Acquisition time	300		ns

7.8 I^2C Switching Characteristics

		MODE				UNIT
		FAST MODE		HIGH-SPEED MODE		
		MIN	MAX	MIN	MAX	
t_{VDDATA}	SCL low to SDA data out valid		450		200	ns
t_{VDACK}	SCL low to SDA acknowledge time		450		200	ns
$t_{STRETCH}$	Clock stretch time in one-shot conversion mode; during ADC conversion		1200		950	ns
t_{SP}	Noise supression time constant on SDA and SCL		50		10	ns

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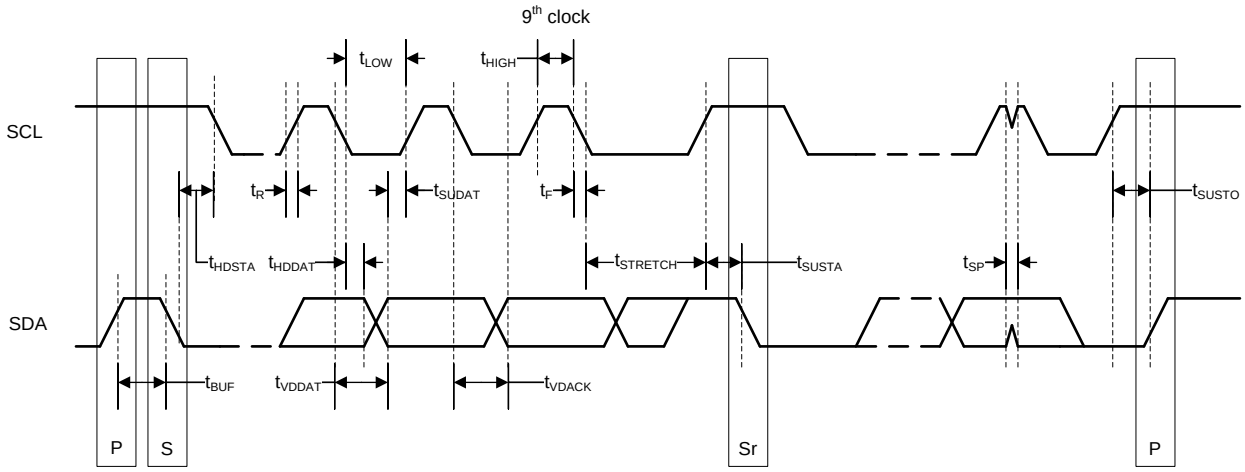
7.9 Switching Characteristics

at AVDD = 2.35 V to 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +85°C; typical values at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
CONVERSION CYCLE					
t_{CONV}	ADC conversion time	Manual and auto sequence modes		$t_{STRETCH}$	ns
		Autonomous mode		550	ns
RESET AND ALERT					
t_{PU}	Power-up time for device	AVDD ≥ 2.35 V		5	ms
t_{RST}	Delay time; RST bit = 1b to device reset complete (1)			5	ms
t_{ALERT_HI}	ALERT high period	ALERT_LOGIC[1:0] = 1x	85	105	ns
t_{ALERT_LO}	ALERT low period	ALERT_LOGIC[1:0] = 1x	85	105	ns

(1) RST bit is automatically reset to 0b after t_{RST}.



NOTE: S = start, Sr = repeated start, and P = stop.

图 1. I²C Timing Diagram

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8 Detailed Description

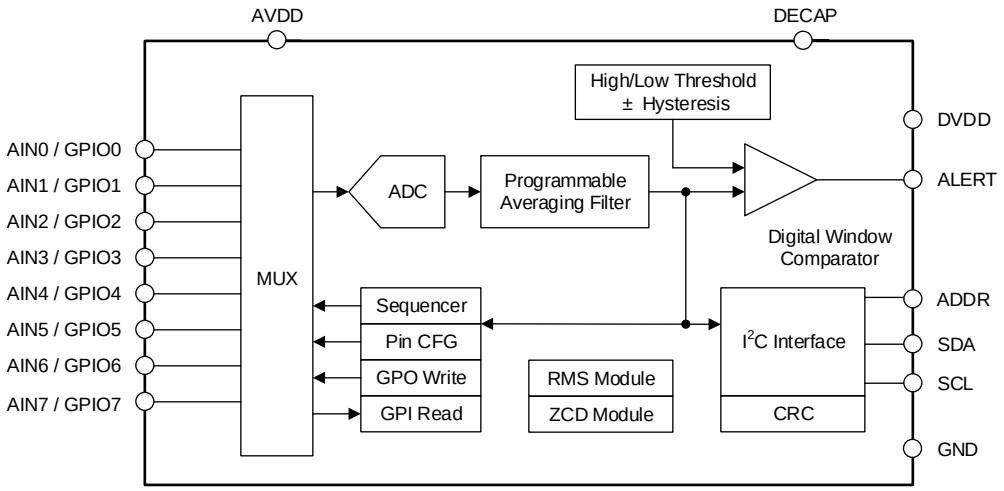
8.1 Overview

The ADS7128 is a small, eight-channel, multiplexed, 12-bit, analog-to-digital converter (ADC) with an I^{2}C-compatible serial interface. The eight channels of the ADS7128 can be individually configured as either analog inputs, digital inputs, or digital outputs. The device includes a digital comparator with a dedicated alert pin that can be used to interrupt the host when a programmed high or low threshold is crossed on any input channel. The device uses an internal oscillator for conversion. The ADC can be used in the manual mode for reading ADC data over the I^{2}C interface or in autonomous mode for monitoring the analog inputs without an active I^{2}C interface.

The device features a programmable averaging filter that outputs a 16-bit result for enhanced resolution. The root-mean-square (RMS) module computes a 16-bit true RMS result of any analog input channel over a configurable time window. The zero-crossing-detect (ZCD) module can be used to generate a digital output corresponding to the programmable threshold crossings of any analog input channel.

The I^{2}C serial interface supports standard-mode, fast-mode, fast-mode plus, and high-speed mode. The device also features an 8-bit cyclic redundancy check (CRC) for the serial communication interface.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Multiplexer and ADC

The eight channels of the multiplexer can be independently configured as ADC inputs or general-purpose inputs/outputs (GPIOs). 图 2 shows that each input pin has electrostatic discharge (ESD) protection diodes to AVDD and GND. On power-up or after device reset, all eight multiplexer channels are configured as analog inputs.

图 2 shows an equivalent circuit for pins configured as analog inputs. The ADC sampling switch is represented by an ideal switch (SW) in series with the resistor, R_{SW} (typically 150 Ω), and the sampling capacitor, C_{SH} (typically 12 pF).

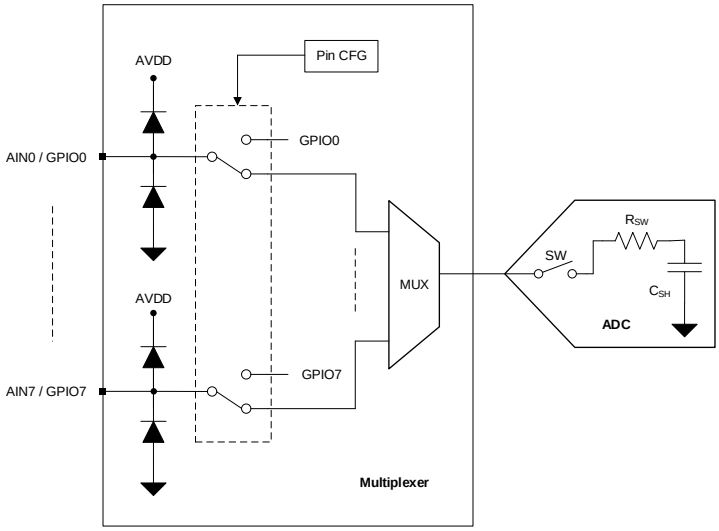

图 2. Analog Inputs, GPIOs, and ADC Connections

During acquisition, the SW switch is closed to allow the signal on the selected analog input channel to charge the internal sampling capacitor. During conversion, the SW switch is opened to disconnect the analog input channel from the sampling capacitor.

The multiplexer channels can be configured as GPIOs in the PIN_CFG register. The direction of a GPIO (either as an input or an output) can be set in the GPIO_CFG register. The logic level on the channels configured as digital inputs can be read from the GPI_VALUE register. The digital outputs can be accessed by writing to the GPO_OUTPUT_VALUE register. The digital outputs can be configured as either open-drain or push-pull in the GPO_DRIVE_CFG register.

8.3.2 Reference

The device uses the analog supply voltage (AVDD) as a reference for the analog-to-digital conversion process. TI recommends connecting a 1-µF, low-equivalent series resistance (ESR) ceramic decoupling capacitor between the AVDD and GND pins.

8.3.3 ADC Transfer Function

The ADC output is in straight binary format. 公式 1 computes the ADC resolution:

$$1\ \text{LSB} = V_{REF} / 2^N \tag{1}$$

where:

- V_{REF} = AVDD
- N = 12

图 3 and 表 1 detail the transfer characteristics for the device.

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Feature Description (接下页)

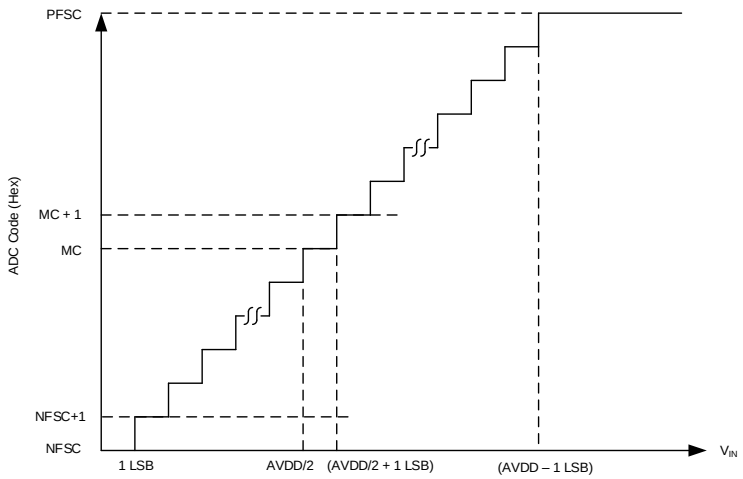

图 3. Ideal Transfer Characteristics

表 1. Transfer Characteristics

INPUT VOLTAGE	CODE	DESCRIPTION	IDEAL OUTPUT CODE
≤1 LSB	NFSC	Negative full-scale code	000
1 LSB to 2 LSBs	NFSC + 1	—	001
(AVDD / 2) to (AVDD / 2) + 1 LSB	MC	Mid code	800
(AVDD / 2) + 1 LSB to (AVDD / 2) + 2 LSB	MC + 1	—	801
≥ AVDD – 1 LSB	PFSC	Positive full-scale code	FFF

8.3.4 ADC Offset Calibration

The variation in ADC offset error resulting from changes in temperature or AVDD can be calibrated by setting the CAL bit in the GENERAL_CFG register. The CAL bit is reset to 0 after calibration. The host can poll the CAL bit to check the ADC offset calibration completion status.

8.3.5 I²C Address Selector

The I²C address for the device is determined by connecting external resistors on the ADDR pin. The device address is determined at power-up based on the resistor values. The device retains this address until the next power-up event, until the next device reset, or until the device receives a command to program its own address. 图 4 shows a connection diagram for the ADDR pin and 表 2 lists the resistor values for selecting different addresses of the device.

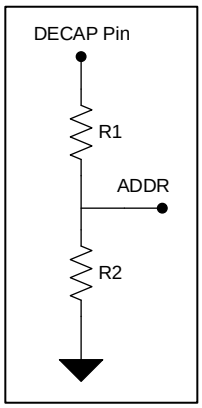

图 4. External Resistor Connection Diagram for the ADDR Pin

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ADVANCE INFORMATION

表 2. I²C Address Selection

RESISTORS		ADDRESS
R1 (1)	R2 (1)	
0 Ω	DNP (2)	001 0111b (17h)
11 kΩ	DNP (2)	001 0110b (16h)
33 kΩ	DNP (2)	001 0101b (15h)
100 kΩ	DNP (2)	001 0100b (14h)
DNP (2)	0 Ω or DNP (2)	001 0000b (10h)
DNP (2)	11 kΩ	001 0001b (11h)
DNP (2)	33 kΩ	001 0010b (12h)
DNP (2)	100 kΩ	001 0011b (13h)

(1) Tolerance for R1, R2 ≤ ±5%.
(2) DNP = Do not populate.

8.3.6 Programmable Averaging Filter

The ADS7128 features a built-in oversampling (OSR) function that can be used to average several samples. The averaging filter can be enabled by programming the OSR[2:0] bits in the OSR_CFG register. The averaging filter configuration is common to all analog input channels. 图 5 shows that the averaging filter module output is 16 bits long. In the manual conversion mode and auto-sequence mode, only the first conversion for the selected analog input channel must be initiated by the host; see the *Manual Mode* and *Auto-Sequence Mode* sections. As shown in 图 5, any remaining conversions for the selected averaging factor are generated internally. The time required to complete the averaging operation is determined by the sampling speed and number of samples to be averaged. As shown in 图 5, the 16-bit result can be read out after the averaging operation completes.

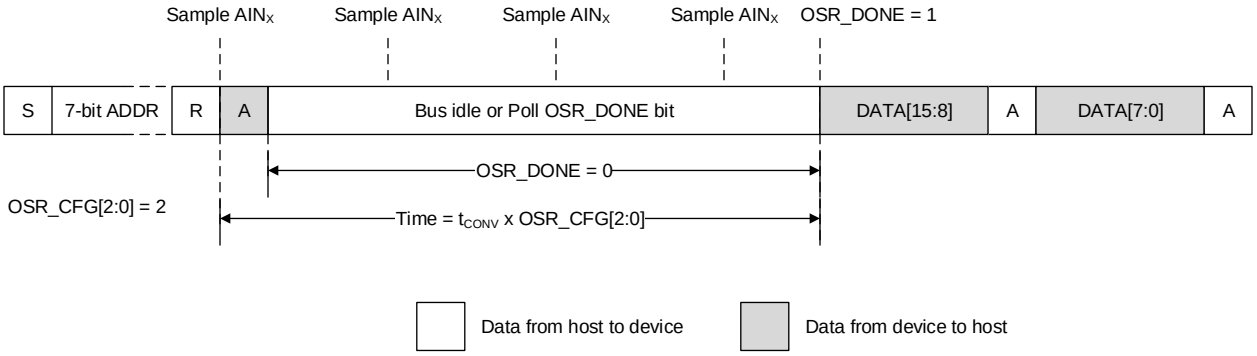

图 5. Averaging Example

In 图 5, SCL is stretched by the device after the start of conversions until the averaging operation is complete.

If SCL stretching is not required during averaging, enable the statistics registers by setting STATS_EN to 1b and initiate conversions by writing 1b to the CNVST bit. The OSR_DONE bit in the SYSTEM_STATUS register can be polled to check the averaging completion status. When using the CNVST bit to initiate conversion, the result can be read in the RECENT_CHx_LSB and RECENT_CHx_MSB registers.

In the autonomous mode of operation, samples from the analog input channels that are enabled in the AUTO_SEQ_CH_SEL register are averaged sequentially; see the *Autonomous Mode* section. The digital window comparator compares the top 12 bits of the 16-bit average result with the thresholds.

公式 2 provides the LSB value of the 16-bit average result.

$$1\ LSB = \frac{AVDD}{2^{16}} \tag{2}$$

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8.3.7 CRC on Data Interface

The ADS7128 features a cyclic redundancy check (CRC) module for checking the integrity of the data bits exchanged over the I^2C interface. The CRC module is bidirectional and appends an 8-bit CRC to every byte read from the device while also evaluating the CRC of every incoming byte over the I^2C interface. The CRC module uses the CRC-8-CCITT polynomial ($x^8 + x^2 + x + 1$) for CRC computation.

To enable the CRC module, set the CRC_EN bit in the GENERAL_CFG register. 表 3 shows how a CRC error can be detected when configuring the ADS7128.

表 3. Configuration Notifications When a CRC Error is Detected

CRC ERROR NOTIFICATION	CONFIGURATION	DESCRIPTION
ALERT pin	ALERT_CRCIN = 1b	ALERT pin is asserted if a CRC error is detected by the device.
Status flags	APPEND_STATUS = 10b	4-bit status flags are appended to the ADC data; see the *Output Data Format* section for details.
Register read	—	Read the CRC_ERR_IN bit to check if a CRC error is detected.

When the ADS7128 detects a CRC error, the erroneous data are ignored and the CRC_ERR_IN bit is set. 表 3 describes the additional notifications that can be enabled. Further register writes are disabled until the CRC_ERR_IN bit is cleared by writing 1b to it. When using autonomous mode, further conversions can be disabled on the CRC error by setting CONV_ON_ERR to 1b; see the *Autonomous Mode* section.

8.3.8 General-Purpose I/Os (GPIOs)

The eight channels of the ADS7128 can be independently configured as analog inputs, digital inputs, or digital outputs. 表 4 describes how the PIN_CFG and GPIO_CFG registers can be used to configure the channels.

表 4. Configuring Channels as Analog Inputs or GPIOs

PIN_CFG[7:0]	GPIO_CFG[7:0]		GPO_DRIVE_CFG[7:0]	CHANNEL CONFIGURATION
0	x		x	Analog input (default)
1	0		x	Digital input
1	1		0	Digital output; open-drain driver
1	1		1	Digital output; push-pull driver

The digital outputs can be configured to logic 1 or 0 by writing to the GPO_OUTPUT_VALUE register. Reading the GPI_VALUE register returns the logic level for all channels configured as digital inputs.

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8.3.9 Oscillator and Timing Control

The device uses an internal oscillator for conversions. When using the averaging module or the RMS module, the host initiates the first conversion and all subsequent conversions are generated internally by the device. However, in the autonomous mode of operation, the start of the conversion signal is generated by the device. 表 5 shows that when the device generates the start of the conversion, the sampling rate is controlled by the OSC_SEL and CLK_DIV[3:0] register fields.

表 5. Configuring Sampling Rate for Internal Conversion Start Control

CLK_DIV[3:0]	OSC_SEL = 0		OSC_SEL = 1	
	SAMPLING FREQUENCY, f_{CYCLE} (kSPS)	CYCLE TIME, t_{CYCLE} (µs)	SAMPLING FREQUENCY, f_{CYCLE} (kSPS)	CYCLE TIME, t_{CYCLE} (µs)
0000b	1000	1	31.25	32
0001b	666.7	1.5	20.83	48
0010b	500	2	15.63	64
0011b	333.3	3	10.42	96
0100b	250	4	7.81	128
0101b	166.7	6	5.21	192
0110b	125	8	3.91	256
0111b	83	12	2.60	384
1000b	62.5	16	1.95	512
1001b	41.7	24	1.3	768
1010b	31.3	32	0.98	1024
1011b	20.8	48	0.65	1536
1100b	15.6	64	0.49	2048
1101b	10.4	96	0.33	3072

The conversion time of the device (see t_{CONV} in the *Switching Characteristics* table) is independent of the OSC_SEL and CLK_DIV[3:0] configuration.

8.3.10 Output Data Format

图 6 illustrates various I^2C frames for reading data.

- Read the ADC conversion result: Two 8-bit I^2C packets are required (frame A).
- Read the averaged conversion result: Two 8-bit I^2C packets are required (frame B).
- Read data with the channel ID or status flags appended: The 4-bit channel ID or status flags can be appended to the 12-bit ADC result by configuring the APPEND_STATUS field in the GENERAL_CFG register. The status flags can be used to detect if a CRC error is detected and if an alert condition is detected by the digital window comparator. When the channel ID or status flags are appended to the 12-bit ADC data, two I^2C packets are required (frame C). If the channel ID or status flags are appended to the 16-bit average result, three I^2C frames are required (frame D).

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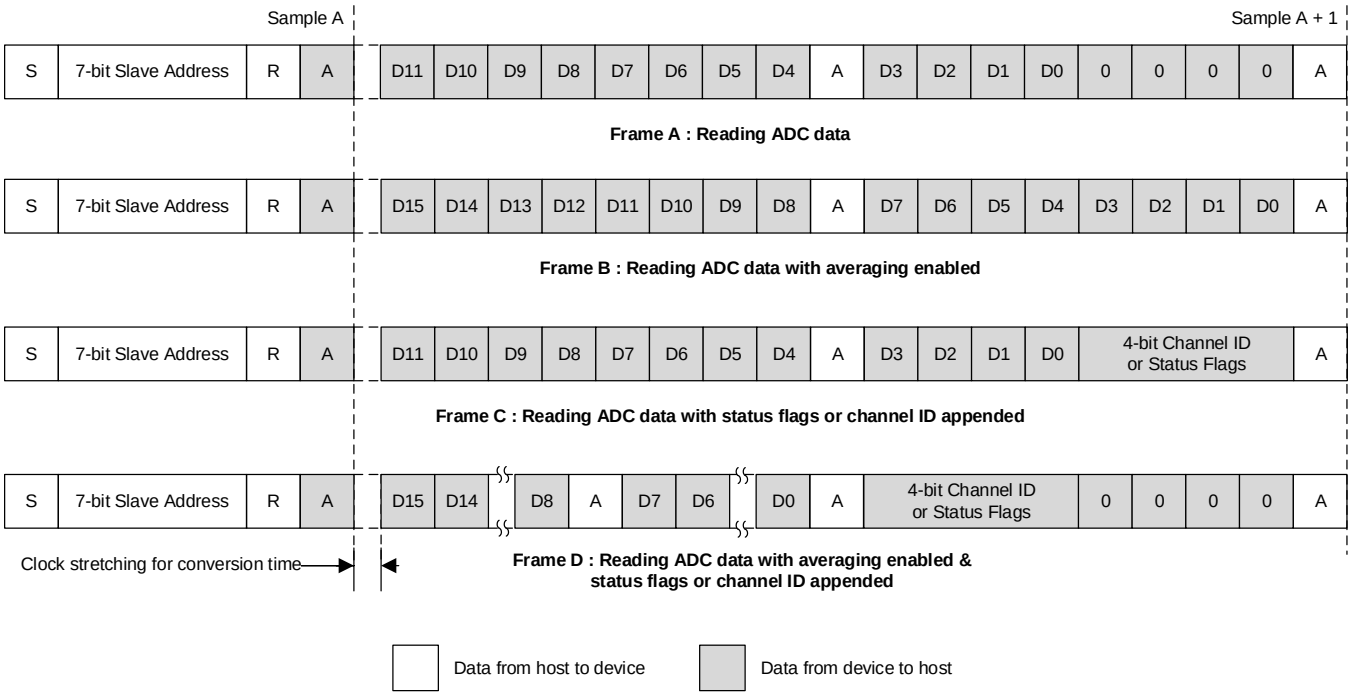

图 6. Data Frames for Reading Data

When status flags are enabled, APPEND_STATUS is set to 10b and four bits are appended to the ADC output. The device outputs status flags in this order: {1b, 0b, CRCERR_IN, ALERT}. The level transitions on the digital interface, resulting from the fixed 1b and 0b in the status flags, can be used to detect if the digital outputs are shorted to a fixed voltage in the system. The CRCERR_IN flag reflects the corresponding bit in the GENERAL_CFG register. The ALERT flag is the output of the logical OR of the bits in the EVENT_FLAG register.

8.3.11 Digital Window Comparator

The internal digital window comparator (DWC) is available in all functional modes of the device (see the *Device Functional Modes* section for details). The digital window comparator controls output of the ALERT pin buffer. The ALERT pin can be configured as open-drain (default) or push-pull output using the ALERT_DRIVE bit in the ALERT_PIN_CFG register. 图 7 shows a block diagram for the digital window comparator.

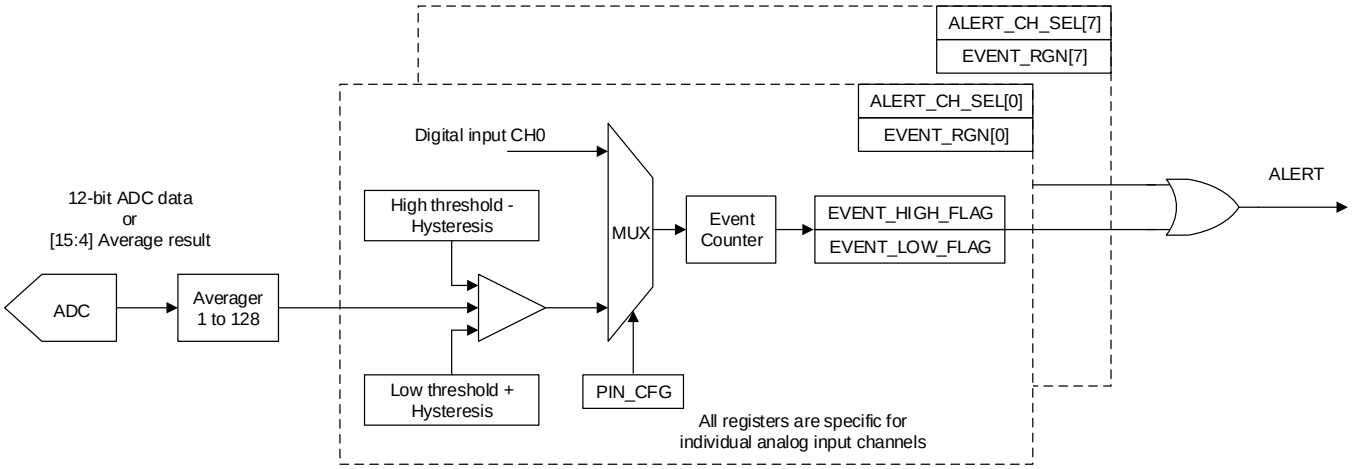

图 7. Digital Window Comparator Block Diagram

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The low-side threshold, high-side threshold, event counter, and hysteresis parameters are independently programmable for each input channel. 图 8 shows the events that can be monitored for every analog input channel by the window comparator.

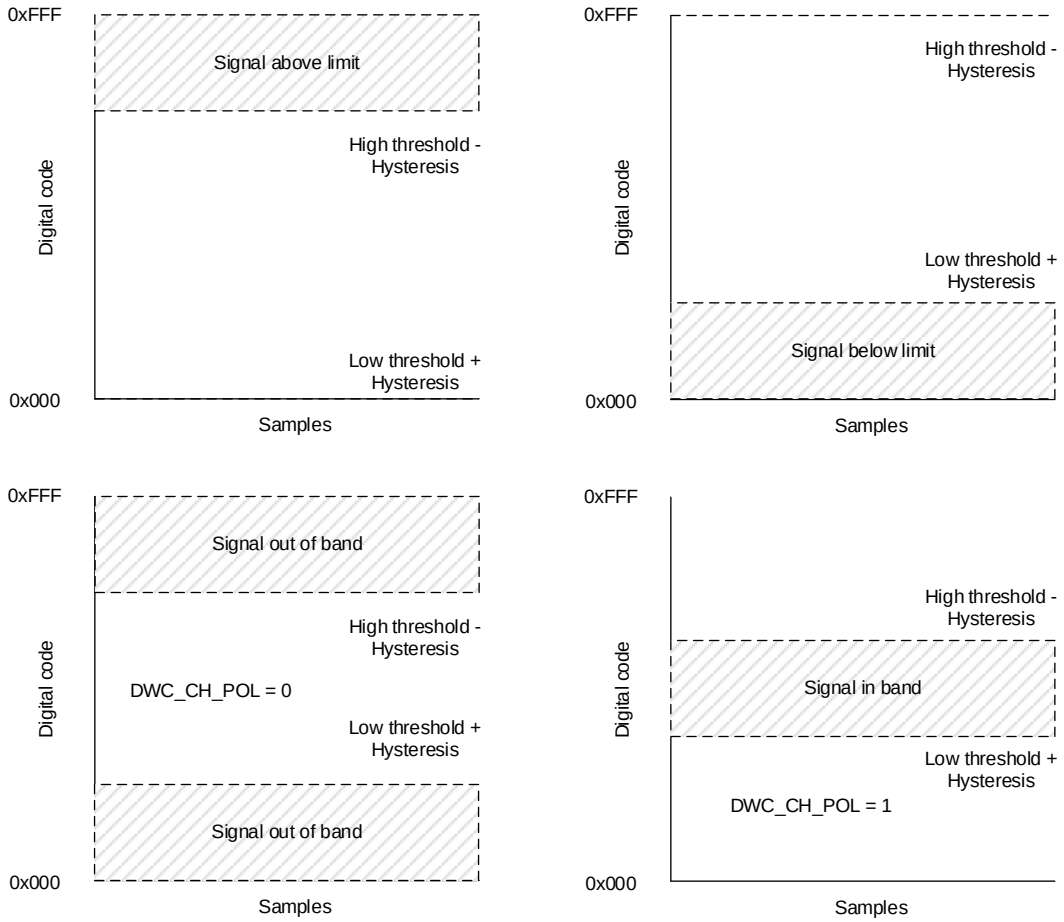

图 8. Event Monitoring With the Window Comparator

To enable the digital window comparator, set the DWC_EN bit in the GENERAL_CFG register. By default, hysteresis is 0, the high threshold is 0xFFF, and the low threshold is 0x000. A 12-bit straight binary code cannot be higher than 0xFFF or lower than 0x000, thus the thresholds have no effect unless set to different values. 图 8 shows the various types of event that can be detected by adjusting the thresholds. For detecting when a signal is in-band, the EVENT_RGN register must be configured. In each of the cases shown in 图 8, either or both EVENT_HIGH_FLAG and EVENT_LOW_FLAG can be set.

The programmable event counter counts consecutive thresholds violations before alert flags can be set. The event count can be set to a higher value to avoid transients in the input signal setting the alert flags.

In order to assert the ALERT pin when the alert flag is set for a particular analog input channel, set the corresponding bit in the ALERT_CH_SEL register. Alert flags are set regardless of the ALERT_CH_SEL configuration if DWC_EN is 1 and the high or low thresholds are exceeded.

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8.3.11.1 Interrupts From Digital Inputs

Logic 1 or logic 0 events can detected on channels configured as digital inputs, as shown in 表 6, by enabling the corresponding ALERT_CH_SEL bit.

表 6. Configuring Interrupts From Digital Inputs

PIN_CFG[7:0]	GPIO_CFG[7:0]	ALERT_CH_SEL[7:0]	EVENT_RGN [7:0]	EVENT DESCRIPTION
1	0	1	0	EVENT_HIGH_FLAG is set when digital input channel is at logic 1.
1	0	1	1	EVENT_LOW_FLAG is set when digital input channel is at logic 0.

8.3.11.2 Changing Digital Outputs on Alert and ZCD

图 9 shows how digital outputs can be updated in response to alerts from individual channels or synchronized to the zero-crossing-detect signal.

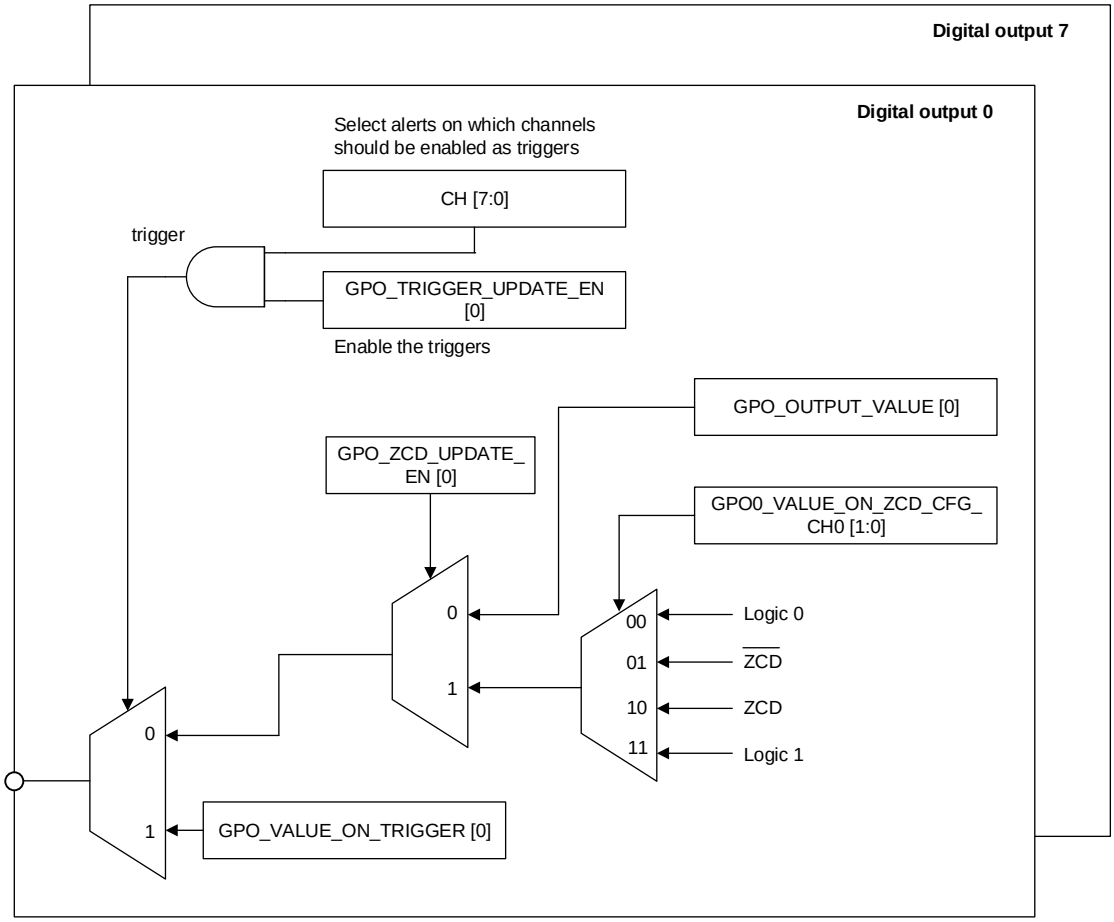

图 9. Block Diagram for the Digital Output Logic

8.3.11.2.1 Changing Digital Outputs on Alerts

Any given digital output can be updated in response to an alert condition on one or more analog inputs and digital inputs. To update the digital output in response to alert conditions, the trigger must be configured and the value must be launched on the trigger.

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8.3.11.2.1.1 Trigger

The following events can act as triggers for updating the value on the digital output:

- An alert occurs on one or more analog input channels. The digital window comparator must be enabled for these channels.
- An alert occurs on one or more digital input channels. The digital window comparator must be enabled for these channels.

Configure the GPOx_TRIG_EVENT_SEL register to select which channels, analog inputs, or digital inputs can trigger an update on the digital output pin. After configuring the triggers for updating a digital output, the logic can be enabled by configuring the corresponding bit in the GPO_TRIGGER_UPDATE_EN register.

8.3.11.2.1.2 Output Value

The digital outputs can be set to logic 1 or logic 0 in response to the triggers. The value to be updated on the digital output when a trigger event occurs can be configured in the GPO_VALUE_ON_TRIGGER register.

8.3.11.2.2 Changing Digital Outputs Synchronous to the Zero-Crossing Detect

Individual digital outputs can be set to either logic 0, logic 1, ZCD, or $\overline{ZCD}$ synchronous to the zero-crossing-detect signal. This function can be enabled for individual digital outputs by configuring the GPO_VALUE_ON_ZCD_CFG_CHx field and setting the corresponding bit in the GPO_ZCD_UPDATE_EN [7:0] register.

8.3.12 Root-Mean-Square Module

The ADS7128 features an RMS computation module. Any one analog input channel can be selected for computing the RMS result. The RMS result is computed over a block of samples from the selected channel and the result can be read from the RMS_RESULT_LSB and RMS_RESULT_MSB registers. 公式 3 shows how the RMS result is computed by calculating the 16-bit square root of the mean of the accumulated result of the squares of the ADC conversion data.

$$RMS = \sqrt{\underbrace{\left(\frac{{D_1}^2 + {D_2}^2 + {D_3}^2 + \cdots + {D_N}^2}{N}\right)}_{\text{AC component}} - b \times \underbrace{\left(\frac{D_1 + D_2 + D_3 + \cdots + D_N}{N}\right)^2}_{\text{DC component}}}\ LSB$$

where

- D is the data corresponding to the analog input channel selected for RMS measurement
- N is the number of samples over which the RMS is computed (3)

The DC offset must be subtracted from the AC component because the analog input signal to the ADC is unipolar. DC subtraction can be enabled or disabled, as given by b in 公式 3, by configuring the DC_SUB field. The RMS result is 16 bits long and 公式 4 gives the size of the 1 LSB of RMS result.

$$1\ LSB = AVDD / 2^{16} \quad (4)$$

The procedure for using the RMS module is outlined in the steps below:

1. Select the channel for the RMS computation using the RMS_CHID field in the RMS_CFG register.
2. Define the time over which the RMS is to be computed by configuring the RMS_SAMPLES field.
3. Start the RMS computation by setting RMS_EN to 1 in the GENERAL_CFG register.
4. The device starts computing the RMS result when the sample size defined by RMS_SAMPLES is converted on the analog input selected for RMS computation. An additional 40 samples must be converted to complete the RMS computation.
5. To monitor for when the RMS computation completes, poll the RMS_DONE bit in the SYSTEM_STATUS register. The ALERT pin can also be used for requesting an interrupt by configuring the ALERT_RMS bit in the ALERT_MAP register.
6. For starting a new RMS measurement, write 1 to the RMS_EN bit in the GENERAL_CFG register.

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8.3.13 Zero-Crossing-Detect Module

图 10 shows the zero-crossing-detection (ZCD) module that generates a digital output corresponding to the threshold crossings of an analog input. In order to detect threshold crossings on a particular analog input, configure the 4-bit channel ID in the ZCD_CHID register field. The threshold crossing to be detected can be configured in the HIGH_TH register. The output of the ZCD module can be mapped to any digital output by configuring the GPO_ZCD_UPDATE_EN, GPO_VALUE_ZCD_CFG_CH0_CH3, and GPO_VALUE_ZCD_CFG_CH4_CH7 registers.

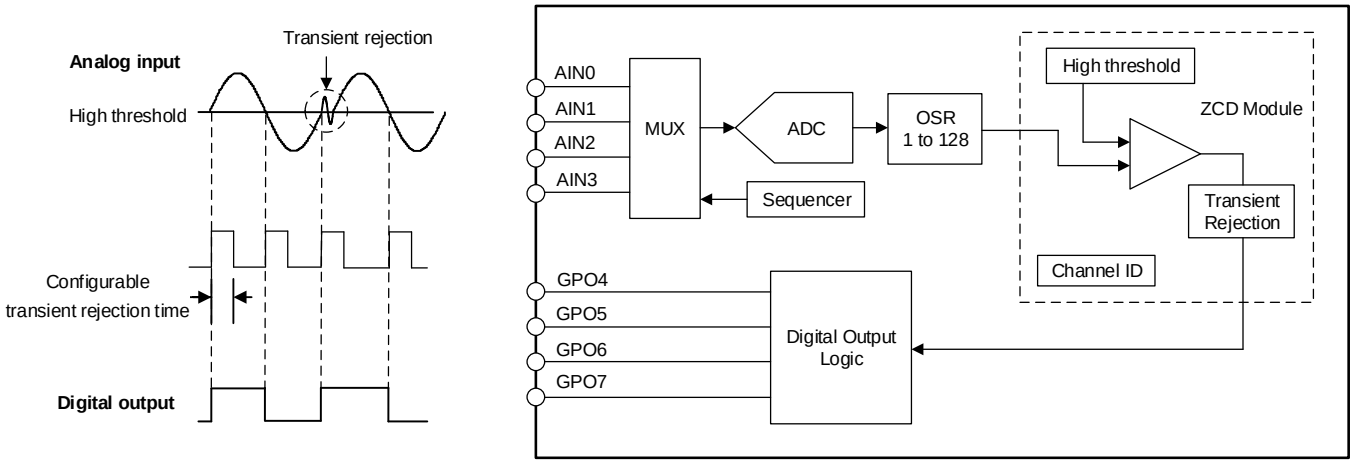

图 10. ZCD Module Operation Block Diagram

The ADC conversion result of the selected analog input channel is compared with the digital threshold and the digital output is set accordingly. 公式 5 shows how transients near zero crossings can be rejected by configuring the ZCD_BLANKING register.

$$\text{transient rejection time} = \text{MULT_EN} \times \text{ZCD_BLANKING}[6:0] \times \frac{1}{\text{sampling rate for ZCD channel}} \text{seconds} \quad (5)$$

8.3.14 Minimum, Maximum, and Latest Data Registers

The ADS7128 can record the minimum, maximum, and latest code (statistics registers) for every analog input channel. To enable or re-enable recording statistics, set the STATS_EN bit in the GENERAL_CFG register. Writing 1 to the STATS_EN bit reinitializes the statistics module, after which results from new conversions are recorded in the statistics registers. Until a new conversion result is available, previous values can be read from the statistics registers. Before reading the statistics registers, set STATS_EN to 0 to prevent any updates to this register block.

8.3.15 I²C Protocol Features

8.3.15.1 General Call

On receiving a general call (00h), the device provides an acknowledge (ACK).

8.3.15.2 General Call With Software Reset

On receiving a general call (00h) followed by a software reset (06h), the device resets itself.

8.3.15.3 General Call With a Software Write to the Programmable Part of the Slave Address

On receiving a general call (00h) followed by 04h, the device reevaluates its own I²C address configured by the ADDR pin. During this operation, the device does not respond to other I²C commands except the general-call command.

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8.3.15.4 Configuring the Device for High-Speed I²C Mode

The device can be configured in high-speed I²C mode by providing an I²C frame with one of these codes: 0x09, 0x0B, 0x0D, or 0x0F.

After receiving one of these codes, the device sets the I2C_HIGH_SPEED bit in the SYSTEM_STATUS register and remains in high-speed I²C mode until a STOP condition is received in an I²C frame.

8.4 Device Functional Modes

表 7 lists the functional modes supported by the ADS7128.

表 7. Functional Modes

FUNCTIONAL MODE	CONVERSION CONTROL	MUX CONTROL	CONV_MODE[1:0]	SEQ_MODE[1:0]
Manual	9th falling edge of SCL (ACK)	Register write to MANUAL_CHID	00b	00b
Auto-sequence	9th falling edge of SCL (ACK)	Channel sequencer	00b	01b
Autonomous	Internal to the device	Channel sequencer	01b	01b

The device powers up in manual mode (see the *Manual Mode* section) and can be configured into any mode listed in 表 7 by writing the configuration registers for the desired mode.

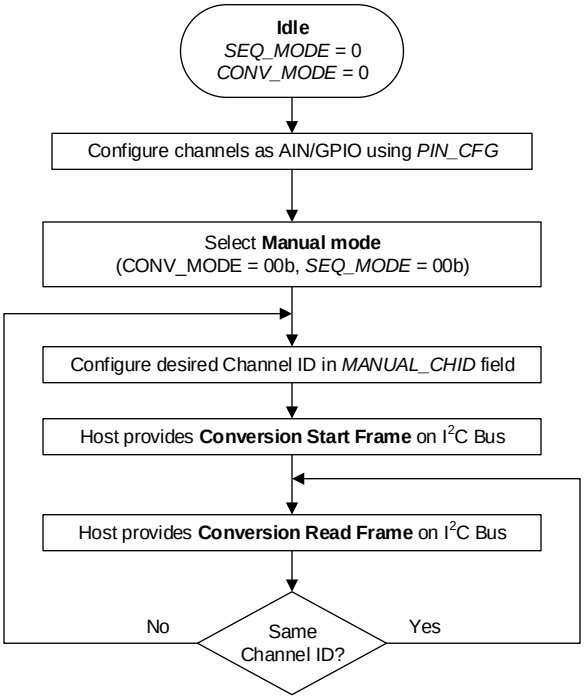
8.4.1 Device Power-Up and Reset

On power-up, the device calculates the address from the resistors connected on the ADDR pin and the BOR bit is set, thus indicating a power-cycle or reset event.

The device can be reset by an I²C general call (00h) followed by a software reset (06h), by setting the RST bit, or by recycling the power on the AVDD pin.

8.4.2 Manual Mode

Manual mode allows the external host processor to directly select the analog input channel. 图 11 lists the steps for operating the device in manual mode.



Manual mode with channel selection using register write

图 11. Device Operation in Manual Mode

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Provide an I²C start or restart frame to initiate a conversion, as shown in the conversion start frame of 图 12, after configuring the device registers. ADC data can be read in subsequent I²C frames. The number of I²C frames required to read conversion data depends on the output data frame size; see the *Output Data Format* section for more details. A new conversion is initiated on the ninth falling edge of SCL (ACK bit) when the last byte of output data is read.

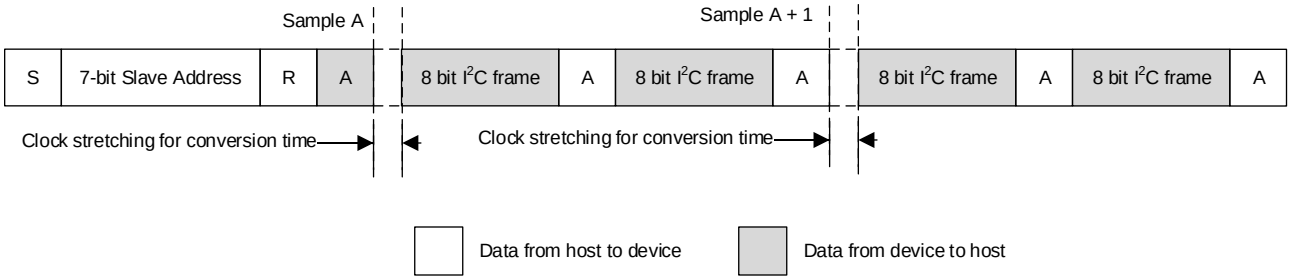

图 12. Starting a Conversion and Reading Data in Manual Mode

8.4.3 Auto-Sequence Mode

In auto-sequence mode, the internal channel sequencer switches the multiplexer to the next analog input channel after every conversion. The desired analog input channels can be configured for sequencing in the AUTO_SEQ_CHSEL register. To enable the channel sequencer, set SEQ_START to 1b. After every conversion, the channel sequencer switches the multiplexer to the next analog input in ascending order. To stop the channel sequencer from selecting channels, set SEQ_START to 0b. 图 13 lists the conversion start and read frames for auto-sequence mode.

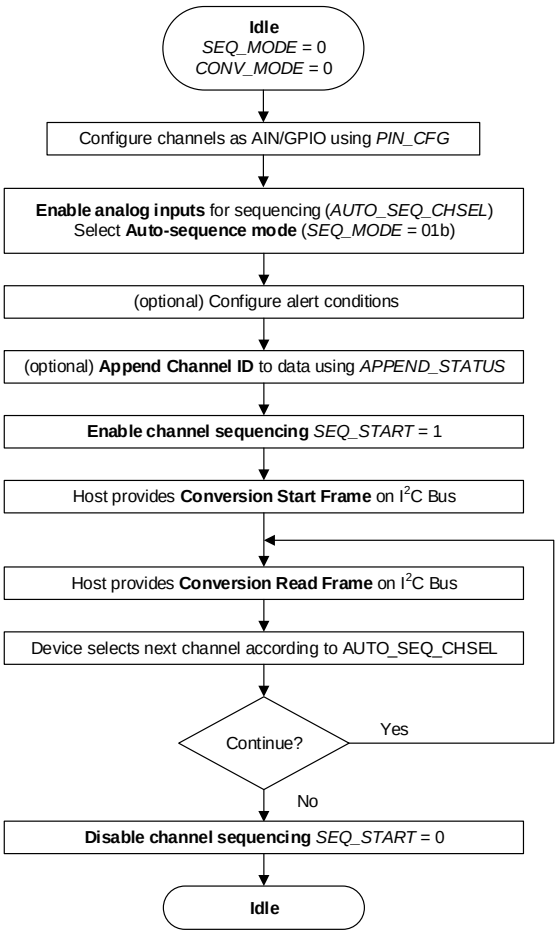

图 13. Device Operation in Auto-Sequence Mode

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8.4.4 Autonomous Mode

In autonomous mode, the device can be programmed to monitor the voltage applied on the analog input pins of the device and generate a signal on the ALERT pin when the programmable high or low threshold values are crossed. In this mode, the device generates the start of conversion using the internal oscillator. The first start of conversion must be provided by the host and the device then generates the subsequent start of conversions.

图 14 shows the steps for configuring the operation mode to autonomous mode. Abort the ongoing sequence by setting SEQ_START to 0b before changing the functional mode or device configuration.

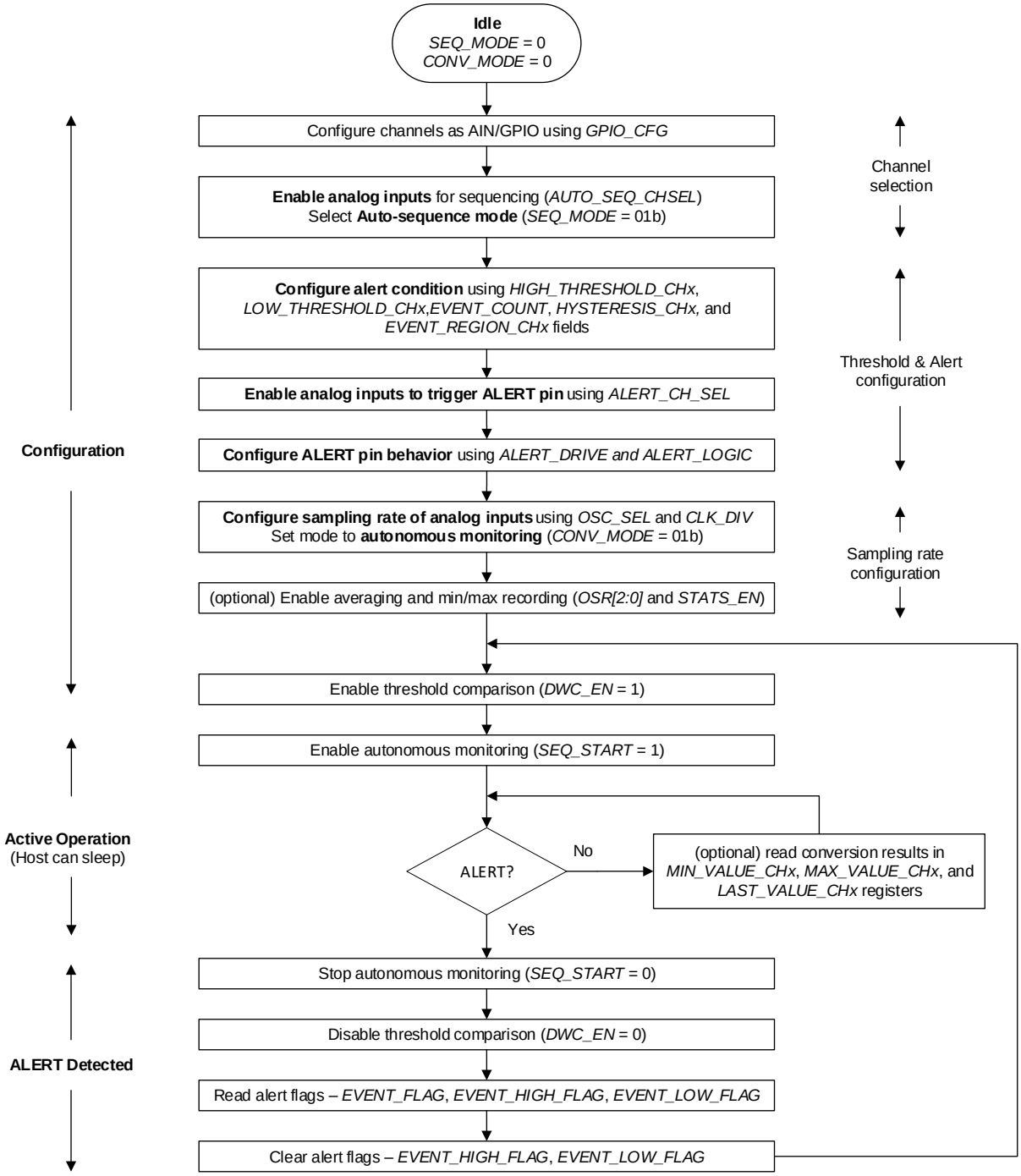

图 14. Configuring the Device in Autonomous Mode

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8.5 Programming

表 8 provides the acronyms for different conditions in an I²C frame. 表 9 lists the various command opcodes.

表 8. I²C Frame Acronyms

SYMBOL	DESCRIPTION
S	Start condition for the I²C frame
Sr	Restart condition for the I²C frame
P	Stop condition for the I²C frame
A	ACK (low)
N	NACK (high)
R	Read bit (high)
W	Write bit (low)

表 9. Opcodes for Commands

OPCODE	COMMAND DESCRIPTION
0001 0000b	Single register read
0000 1000b	Single register write
0001 1000b	Set bit
0010 0000b	Clear bit
0011 0000b	Reading a continuous block of registers
0010 1000b	Writing a continuous block of registers

8.5.1 Reading Registers

The I²C master can either read a single register or a continuous block registers from the device, as described in the *Single Register Read* and *Reading a Continuous Block of Registers* sections.

8.5.1.1 Single Register Read

To read a single register from the device, the I²C master must provide an I²C command with three frames to set the register address for reading data. 表 9 lists the opcodes for different commands. After this command is provided, the I²C master must provide another I²C frame (as shown in 图 15) containing the device address and the read bit. After this frame, the device provides the register data. The device provides the same register data even if the host provides more clocks. To end the register read command, the master must provide a STOP or a RESTART condition in the I²C frame.

S	7-bit Slave Address	W	A	0001 0000b	A	Register Address	A	P/Sr	S	7-bit Slave Address	R	A	Register Data	A	P/Sr

Data from host to device Data from device to host

NOTE: S = start, Sr = repeated start, and P = stop.

图 15. Reading Register Data

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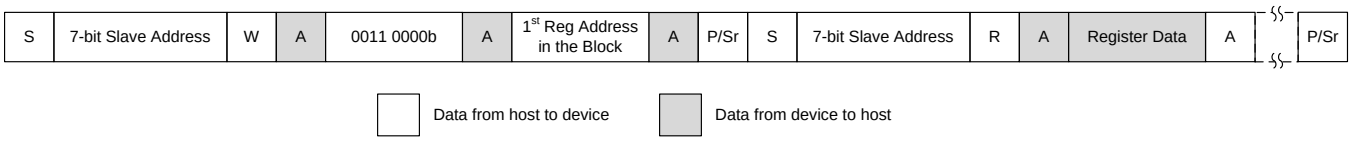
8.5.1.2 Reading a Continuous Block of Registers

To read a continuous block of registers, the I²C master must provide an I²C command to set the register address. The register address is the address of the first register in the block that must be read. After this command is provided, the I²C master must provide another I²C frame, as shown in 图 16, containing the device address and the read bit. After this frame, the device provides the register data. The device provides data for the next register when more clocks are provided. When data are read from addresses that do not exist in the register map of the device, the device returns zeros. If the device does not have any further registers to provide data on, the device provide zeros. To end the register read command, the master must provide a STOP or a RESTART condition in the I²C frame.



NOTE: S = start, Sr = repeated start, and P = stop.

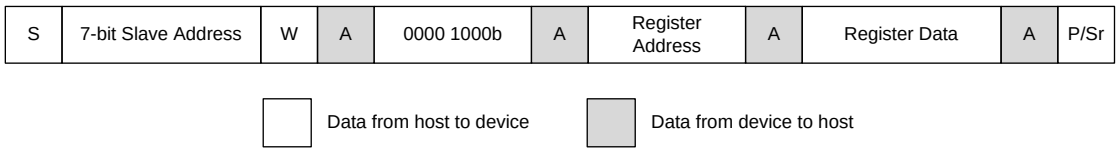
图 16. Reading a Continuous Block of Registers

8.5.2 Writing Registers

The I²C master can either write a single register or a continuous block of registers to the device, set a few bits in a register, or clear a few bits in a register.

8.5.2.1 Single Register Write

To write a single register from the device, as shown in 图 17, the I²C master must provide an I²C command with four frames. The register address is the address of the register that must be written and the register data is the value that must be written. 表 9 lists the opcodes for different commands. To end the register write command, the master must provide a STOP or a RESTART condition in the I²C frame.



NOTE: S = start, Sr = repeated start, and P = stop.

图 17. Writing a Single Register

8.5.2.2 Set Bit

The I²C master must provide an I²C command with four frames, as shown in 图 17, to set bits in a register without changing the other bits. The register address is the address of the register that the bits must set and the register data is the value representing the bits that must be set. Bits with a value of 1 in the register data are set and bits with a value of 0 in the register data are not changed. 表 9 lists the opcodes for different commands. To end this command, the master must provide a STOP or RESTART condition in the I²C frame.

8.5.2.3 Clear Bit

The I²C master must provide an I²C command with four frames, as shown in 图 17, to clear bits in a register without changing the other bits. The register address is the address of the register that the bits must clear and the register data is the value representing the bits that must be cleared. Bits with a value of 1 in the register data are cleared and bits with a value of 0 in the register data are not changed. 表 9 lists the opcodes for different commands. To end this command, the master must provide a STOP or a RESTART condition in the I²C frame.

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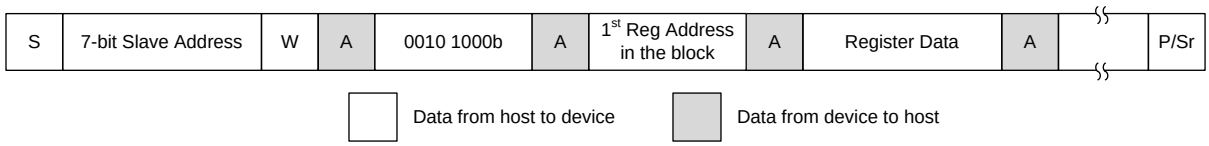
8.5.2.4 Writing a Continuous Block of Registers

The I²C master must provide an I²C command, as shown in 图 18, to write a continuous block of registers. The register address is the address of the first register in the block that must be written. The I²C master must provide data for registers in subsequent I²C frames in an ascending order of register addresses. Writing data to addresses that do not exist in the register map of the device have no effect. 表 9 lists the opcodes for different commands. If the data provided by the I²C master exceeds the address space of the device, the device ignores the data beyond the address space. To end the register write command, the master must provide a STOP or a RESTART condition in the I²C frame.



NOTE: S = start, Sr = repeated start, and P = stop.

图 18. Writing a Continuous Block of Registers

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8.6 ADS7128 Registers

Table 10 lists the ADS7128 registers. All register offset addresses not listed in Table 10 should be considered as reserved locations and the register contents should not be modified.

Table 10. ADS7128 Registers

Address	Acronym	Register Name	Section
0x0	SYSTEM_STATUS		SYSTEM_STATUS Register (Address = 0x0) [reset = 0x81]
0x1	GENERAL_CFG		GENERAL_CFG Register (Address = 0x1) [reset = 0x0]
0x2	DATA_CFG		DATA_CFG Register (Address = 0x2) [reset = 0x0]
0x3	OSR_CFG		OSR_CFG Register (Address = 0x3) [reset = 0x0]
0x4	OPMODE_CFG		OPMODE_CFG Register (Address = 0x4) [reset = 0x0]
0x5	PIN_CFG		PIN_CFG Register (Address = 0x5) [reset = 0x0]
0x7	GPIO_CFG		GPIO_CFG Register (Address = 0x7) [reset = 0x0]
0x9	GPO_DRIVE_CFG		GPO_DRIVE_CFG Register (Address = 0x9) [reset = 0x0]
0xB	GPO_OUTPUT_VALUE		GPO_OUTPUT_VALUE Register (Address = 0xB) [reset = 0x0]
0xD	GPI_VALUE		GPI_VALUE Register (Address = 0xD) [reset = 0x0]
0xF	ZCD_BLANKING_CFG		ZCD_BLANKING_CFG Register (Address = 0xF) [reset = 0x0]
0x10	SEQUENCE_CFG		SEQUENCE_CFG Register (Address = 0x10) [reset = 0x0]
0x11	CHANNEL_SEL		CHANNEL_SEL Register (Address = 0x11) [reset = 0x0]
0x12	AUTO_SEQ_CH_SEL		AUTO_SEQ_CH_SEL Register (Address = 0x12) [reset = 0x0]
0x14	ALERT_CH_SEL		ALERT_CH_SEL Register (Address = 0x14) [reset = 0x0]
0x16	ALERT_MAP		ALERT_MAP Register (Address = 0x16) [reset = 0x0]
0x17	ALERT_PIN_CFG		ALERT_PIN_CFG Register (Address = 0x17) [reset = 0x0]
0x18	EVENT_FLAG		EVENT_FLAG Register (Address = 0x18) [reset = 0x0]
0x1A	EVENT_HIGH_FLAG		EVENT_HIGH_FLAG Register (Address = 0x1A) [reset = 0x0]
0x1C	EVENT_LOW_FLAG		EVENT_LOW_FLAG Register (Address = 0x1C) [reset = 0x0]
0x1E	EVENT_RGN		EVENT_RGN Register (Address = 0x1E) [reset = 0x0]
0x20	HYSTERESIS_CH0		HYSTERESIS_CH0 Register (Address = 0x20) [reset = 0xF0]
0x21	HIGH_TH_CH0		HIGH_TH_CH0 Register (Address = 0x21) [reset = 0xFF]
0x22	EVENT_COUNT_CH0		EVENT_COUNT_CH0 Register (Address = 0x22) [reset = 0x0]
0x23	LOW_TH_CH0		LOW_TH_CH0 Register (Address = 0x23) [reset = 0x0]
0x24	HYSTERESIS_CH1		HYSTERESIS_CH1 Register (Address = 0x24) [reset = 0xF0]
0x25	HIGH_TH_CH1		HIGH_TH_CH1 Register (Address = 0x25) [reset = 0xFF]
0x26	EVENT_COUNT_CH1		EVENT_COUNT_CH1 Register (Address = 0x26) [reset = 0x0]
0x27	LOW_TH_CH1		LOW_TH_CH1 Register (Address = 0x27) [reset = 0x0]
0x28	HYSTERESIS_CH2		HYSTERESIS_CH2 Register (Address = 0x28) [reset = 0xF0]
0x29	HIGH_TH_CH2		HIGH_TH_CH2 Register (Address = 0x29) [reset = 0xFF]
0x2A	EVENT_COUNT_CH2		EVENT_COUNT_CH2 Register (Address = 0x2A) [reset = 0x0]
0x2B	LOW_TH_CH2		LOW_TH_CH2 Register (Address = 0x2B) [reset = 0x0]
0x2C	HYSTERESIS_CH3		HYSTERESIS_CH3 Register (Address = 0x2C) [reset = 0xF0]
0x2D	HIGH_TH_CH3		HIGH_TH_CH3 Register (Address = 0x2D) [reset = 0xFF]
0x2E	EVENT_COUNT_CH3		EVENT_COUNT_CH3 Register (Address = 0x2E) [reset = 0x0]
0x2F	LOW_TH_CH3		LOW_TH_CH3 Register (Address = 0x2F) [reset = 0x0]
0x30	HYSTERESIS_CH4		HYSTERESIS_CH4 Register (Address = 0x30) [reset = 0xF0]
0x31	HIGH_TH_CH4		HIGH_TH_CH4 Register (Address = 0x31) [reset = 0xFF]
0x32	EVENT_COUNT_CH4		EVENT_COUNT_CH4 Register (Address = 0x32) [reset = 0x0]
0x33	LOW_TH_CH4		LOW_TH_CH4 Register (Address = 0x33) [reset = 0x0]
0x34	HYSTERESIS_CH5		HYSTERESIS_CH5 Register (Address = 0x34) [reset = 0xF0]
0x35	HIGH_TH_CH5		HIGH_TH_CH5 Register (Address = 0x35) [reset = 0xFF]

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Table 10. ADS7128 Registers (continued)

Address	Acronym	Register Name	Section
0x36	EVENT_COUNT_CH5		EVENT_COUNT_CH5 Register (Address = 0x36) [reset = 0x0]
0x37	LOW_TH_CH5		LOW_TH_CH5 Register (Address = 0x37) [reset = 0x0]
0x38	HYSTERESIS_CH6		HYSTERESIS_CH6 Register (Address = 0x38) [reset = 0xF0]
0x39	HIGH_TH_CH6		HIGH_TH_CH6 Register (Address = 0x39) [reset = 0xFF]
0x3A	EVENT_COUNT_CH6		EVENT_COUNT_CH6 Register (Address = 0x3A) [reset = 0x0]
0x3B	LOW_TH_CH6		LOW_TH_CH6 Register (Address = 0x3B) [reset = 0x0]
0x3C	HYSTERESIS_CH7		HYSTERESIS_CH7 Register (Address = 0x3C) [reset = 0xF0]
0x3D	HIGH_TH_CH7		HIGH_TH_CH7 Register (Address = 0x3D) [reset = 0xFF]
0x3E	EVENT_COUNT_CH7		EVENT_COUNT_CH7 Register (Address = 0x3E) [reset = 0x0]
0x3F	LOW_TH_CH7		LOW_TH_CH7 Register (Address = 0x3F) [reset = 0x0]
0x60	MAX_CH0_LSB		MAX_CH0_LSB Register (Address = 0x60) [reset = 0x0]
0x61	MAX_CH0_MSB		MAX_CH0_MSB Register (Address = 0x61) [reset = 0x0]
0x62	MAX_CH1_LSB		MAX_CH1_LSB Register (Address = 0x62) [reset = 0x0]
0x63	MAX_CH1_MSB		MAX_CH1_MSB Register (Address = 0x63) [reset = 0x0]
0x64	MAX_CH2_LSB		MAX_CH2_LSB Register (Address = 0x64) [reset = 0x0]
0x65	MAX_CH2_MSB		MAX_CH2_MSB Register (Address = 0x65) [reset = 0x0]
0x66	MAX_CH3_LSB		MAX_CH3_LSB Register (Address = 0x66) [reset = 0x0]
0x67	MAX_CH3_MSB		MAX_CH3_MSB Register (Address = 0x67) [reset = 0x0]
0x68	MAX_CH4_LSB		MAX_CH4_LSB Register (Address = 0x68) [reset = 0x0]
0x69	MAX_CH4_MSB		MAX_CH4_MSB Register (Address = 0x69) [reset = 0x0]
0x6A	MAX_CH5_LSB		MAX_CH5_LSB Register (Address = 0x6A) [reset = 0x0]
0x6B	MAX_CH5_MSB		MAX_CH5_MSB Register (Address = 0x6B) [reset = 0x0]
0x6C	MAX_CH6_LSB		MAX_CH6_LSB Register (Address = 0x6C) [reset = 0x0]
0x6D	MAX_CH6_MSB		MAX_CH6_MSB Register (Address = 0x6D) [reset = 0x0]
0x6E	MAX_CH7_LSB		MAX_CH7_LSB Register (Address = 0x6E) [reset = 0x0]
0x6F	MAX_CH7_MSB		MAX_CH7_MSB Register (Address = 0x6F) [reset = 0x0]
0x80	MIN_CH0_LSB		MIN_CH0_LSB Register (Address = 0x80) [reset = 0xFF]
0x81	MIN_CH0_MSB		MIN_CH0_MSB Register (Address = 0x81) [reset = 0xFF]
0x82	MIN_CH1_LSB		MIN_CH1_LSB Register (Address = 0x82) [reset = 0xFF]
0x83	MIN_CH1_MSB		MIN_CH1_MSB Register (Address = 0x83) [reset = 0xFF]
0x84	MIN_CH2_LSB		MIN_CH2_LSB Register (Address = 0x84) [reset = 0xFF]
0x85	MIN_CH2_MSB		MIN_CH2_MSB Register (Address = 0x85) [reset = 0xFF]
0x86	MIN_CH3_LSB		MIN_CH3_LSB Register (Address = 0x86) [reset = 0xFF]
0x87	MIN_CH3_MSB		MIN_CH3_MSB Register (Address = 0x87) [reset = 0xFF]
0x88	MIN_CH4_LSB		MIN_CH4_LSB Register (Address = 0x88) [reset = 0xFF]
0x89	MIN_CH4_MSB		MIN_CH4_MSB Register (Address = 0x89) [reset = 0xFF]
0x8A	MIN_CH5_LSB		MIN_CH5_LSB Register (Address = 0x8A) [reset = 0xFF]
0x8B	MIN_CH5_MSB		MIN_CH5_MSB Register (Address = 0x8B) [reset = 0xFF]
0x8C	MIN_CH6_LSB		MIN_CH6_LSB Register (Address = 0x8C) [reset = 0xFF]
0x8D	MIN_CH6_MSB		MIN_CH6_MSB Register (Address = 0x8D) [reset = 0xFF]
0x8E	MIN_CH7_LSB		MIN_CH7_LSB Register (Address = 0x8E) [reset = 0xFF]
0x8F	MIN_CH7_MSB		MIN_CH7_MSB Register (Address = 0x8F) [reset = 0xFF]
0xA0	RECENT_CH0_LSB		RECENT_CH0_LSB Register (Address = 0xA0) [reset = 0x0]
0xA1	RECENT_CH0_MSB		RECENT_CH0_MSB Register (Address = 0xA1) [reset = 0x0]
0xA2	RECENT_CH1_LSB		RECENT_CH1_LSB Register (Address = 0xA2) [reset = 0x0]
0xA3	RECENT_CH1_MSB		RECENT_CH1_MSB Register (Address = 0xA3) [reset = 0x0]
0xA4	RECENT_CH2_LSB		RECENT_CH2_LSB Register (Address = 0xA4) [reset = 0x0]

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Table 10. ADS7128 Registers (continued)

Address	Acronym	Register Name	Section
0xA5	RECENT_CH2_MSB		RECENT_CH2_MSB Register (Address = 0xA5) [reset = 0x0]
0xA6	RECENT_CH3_LSB		RECENT_CH3_LSB Register (Address = 0xA6) [reset = 0x0]
0xA7	RECENT_CH3_MSB		RECENT_CH3_MSB Register (Address = 0xA7) [reset = 0x0]
0xA8	RECENT_CH4_LSB		RECENT_CH4_LSB Register (Address = 0xA8) [reset = 0x0]
0xA9	RECENT_CH4_MSB		RECENT_CH4_MSB Register (Address = 0xA9) [reset = 0x0]
0xAA	RECENT_CH5_LSB		RECENT_CH5_LSB Register (Address = 0xAA) [reset = 0x0]
0xAB	RECENT_CH5_MSB		RECENT_CH5_MSB Register (Address = 0xAB) [reset = 0x0]
0xAC	RECENT_CH6_LSB		RECENT_CH6_LSB Register (Address = 0xAC) [reset = 0x0]
0xAD	RECENT_CH6_MSB		RECENT_CH6_MSB Register (Address = 0xAD) [reset = 0x0]
0xAE	RECENT_CH7_LSB		RECENT_CH7_LSB Register (Address = 0xAE) [reset = 0x0]
0xAF	RECENT_CH7_MSB		RECENT_CH7_MSB Register (Address = 0xAF) [reset = 0x0]
0xC0	RMS_CFG		RMS_CFG Register (Address = 0xC0) [reset = 0x0]
0xC1	RMS_LSB		RMS_LSB Register (Address = 0xC1) [reset = 0x0]
0xC2	RMS_MSB		RMS_MSB Register (Address = 0xC2) [reset = 0x0]
0xC3	GPO0_TRIG_EVENT_SEL		GPO0_TRIG_EVENT_SEL Register (Address = 0xC3) [reset = 0x2]
0xC5	GPO1_TRIG_EVENT_SEL		GPO1_TRIG_EVENT_SEL Register (Address = 0xC5) [reset = 0x2]
0xC7	GPO2_TRIG_EVENT_SEL		GPO2_TRIG_EVENT_SEL Register (Address = 0xC7) [reset = 0x2]
0xC9	GPO3_TRIG_EVENT_SEL		GPO3_TRIG_EVENT_SEL Register (Address = 0xC9) [reset = 0x2]
0xCB	GPO4_TRIG_EVENT_SEL		GPO4_TRIG_EVENT_SEL Register (Address = 0xCB) [reset = 0x2]
0xCD	GPO5_TRIG_EVENT_SEL		GPO5_TRIG_EVENT_SEL Register (Address = 0xCD) [reset = 0x2]
0xCF	GPO6_TRIG_EVENT_SEL		GPO6_TRIG_EVENT_SEL Register (Address = 0xCF) [reset = 0x2]
0xD1	GPO7_TRIG_EVENT_SEL		GPO7_TRIG_EVENT_SEL Register (Address = 0xD1) [reset = 0x2]
0xE3	GPO_VALUE_ZCD_CFG_CH0_CH3		GPO_VALUE_ZCD_CFG_CH0_CH3 Register (Address = 0xE3) [reset = 0x0]
0xE4	GPO_VALUE_ZCD_CFG_CH4_CH7		GPO_VALUE_ZCD_CFG_CH4_CH7 Register (Address = 0xE4) [reset = 0x0]
0xE7	GPO_ZCD_UPDATE_EN		GPO_ZCD_UPDATE_EN Register (Address = 0xE7) [reset = 0x0]
0xE9	GPO_TRIGGER_CFG		GPO_TRIGGER_CFG Register (Address = 0xE9) [reset = 0x0]
0xEB	GPO_VALUE_TRIG		GPO_VALUE_TRIG Register (Address = 0xEB) [reset = 0x0]

Complex bit access types are encoded to fit into small table cells. Table 11 shows the codes that are used for access types in this section.

Table 11. ADS7128 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		

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Table 11. ADS7128 Access Type Codes (continued)

Access Type	Code	Description
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

8.6.1 SYSTEM_STATUS Register (Address = 0x0) [reset = 0x81]

SYSTEM_STATUS is shown in Figure 19 and described in Table 12.

Return to the Summary Table.

Figure 19. SYSTEM_STATUS Register

7	6	5	4	3	2	1	0
RSVD	SEQ_STATUS	I^2C_SPEED	RMS_DONE	OSR_DONE	CRC_ERR_FUSE	CRC_ERR_IN	BOR
R-1b	R-0b	R-0b	R/W-0b	R/W-0b	R-0b	R/W-0b	R/W-1b

Table 12. SYSTEM_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	1b	Reads return 1b.
6	SEQ_STATUS	R	0b	Status of the channel sequencer. 0b = Sequence stopped 1b = Sequence in progress
5	I^2C_SPEED	R	0b	I^2C high-speed status. 0b = I^2C bus is not in high speed mode. 1b = I^2C bus is in high speed mode.
4	RMS_DONE	R/W	0b	RMS computation status. Clear this bit by writing 1b to this bit. 0b = RMS operation in progress or not started; RMS result not ready. 1b = RMS computation complete; RMS result ready.
3	OSR_DONE	R/W	0b	Averaging status. Clear this bit by writing 1b to this bit. 0b = Averaging in progress or not started; average result is not ready. 1b = Averaging complete; average result is ready.
2	CRC_ERR_FUSE	R	0b	Device power-up configuration CRC check status. To re-evaluate this bit, software reset the device or power cycle AVDD. 0b = No problems detected in power-up configuration. 1b = Device configuration not loaded correctly.
1	CRC_ERR_IN	R/W	0b	Status of CRC check on incoming data. Write 1b to clear this error flag. 0b = No CRC error. 1b = CRC error detected. All register writes, except to addresses 0x00 and 0x01, are blocked.
0	BOR	R/W	1b	Brown out reset indicator. This bit is set if brown out condition occurs or device is power cycled. Write 1b to this bit to clear the flag. 0b = No brown out since last time this bit was cleared. 1b = Brown out condition detected or device power cycled.

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8.6.2 GENERAL_CFG Register (Address = 0x1) [reset = 0x0]

GENERAL_CFG is shown in Figure 20 and described in Table 13.

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Figure 20. GENERAL_CFG Register

7	6	5	4	3	2	1	0
RMS_EN	CRC_EN	STATS_EN	DWC_EN	CNVST	CH_RST	CAL	RST
R/W-0b	R/W-0b	R/W-0b	R/W-0b	W-0b	R/W-0b	R/W-0b	W-0b

Table 13. GENERAL_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RMS_EN	R/W	0b	Enableor disable the RMS module. 0b = RMS module disabled. 1b = RMS module enabled; writing 1b to this bit clears RMS_RESULT resgiters and initiates new RMS computation.
6	CRC_EN	R/W	0b	Enable or disable the CRC on device interface. 0b = CRC module disabled. 1b = CRC appended to data output. CRC check is enabled on incoming data.
5	STATS_EN	R/W	0b	Enable or disable the statistics module to update minimum, maximum, and latest output code registers. 0b = Statistics registers are not updated. 1b = Clear statistics registers and conitnue updating with new conversion results.
4	DWC_EN	R/W	0b	Enable or disable the digital window comparator. 0b = Reset or disable the digital window comparator. 1b = Enable the digital window comparator.
3	CNVST	W	0b	Control start conversion on selected analog input. Readback of this bit returns 0b. 0b = Normal operation; conversions start on the 9th falling edge of I^2C frame. Device stretches SCL until end of conversion or completion of averaging. 1b = Initiate start of conversion. Device does not stretch SCL until end of conversion or completion of averaging.
2	CH_RST	R/W	0b	Force all channels to be analog inputs. 0b = Normal operation. 1b = All channels are configured as analog inputs irrespective of configuration in other registers.
1	CAL	R/W	0b	Calibrate ADC offset. 0b = Normal operation. 1b = ADC offset is calibrated. After calibration is complete, this bit is set to 0b.
0	RST	W	0b	Software reset all registers to default values. 0b = Normal operation. 1b = Device is reset. After reset is complete, this bit is set to 0b and BOR bit is set to 1b.

8.6.3 DATA_CFG Register (Address = 0x2) [reset = 0x0]

DATA_CFG is shown in Figure 21 and described in Table 14.

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Figure 21. DATA_CFG Register

7	6	5	4	3	2	1	0
FIX_PAT	RESERVED	APPEND_STATUS[1:0]		RESERVED			
R/W-0b	R-0b	R/W-0b		R-0b			

Table 14. DATA_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FIX_PAT	R/W	0b	Device will output fixed data bits which can be helpful for debugging communication with the device. 0b = Normal operation. 1b = Device will output fixed code 0xA5A repeatitively when reading ADC data.
6	RESERVED	R	0b	Reserved. Reads return 0.
5-4	APPEND_STATUS[1:0]	R/W	0b	Append 4-bit channel ID or status flags to output data. 0b = Channel ID and status flags are not appended to ADC data. 1b = 4-bit channel ID is appended to ADC data. 10b = 4-bit status flags are appended to ADC data. 11b = Reserved.
3-0	RESERVED	R	0b	Reserved. Reads return 0.

8.6.4 OSR_CFG Register (Address = 0x3) [reset = 0x0]

OSR_CFG is shown in Figure 22 and described in Table 15.

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Figure 22. OSR_CFG Register

7	6	5	4	3	2	1	0
RESERVED					OSR[2:0]		
R-0b					R/W-0b		

Table 15. OSR_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0b	Reserved. Reads return 0.
2-0	OSR[2:0]	R/W	0b	Selects the oversampling ratio for ADC conversion result. 0b = No averaging 1b = 2 samples 10b = 4 samples 11b = 8 samples 100b = 16 samples 101b = 32 samples 110b = 64 samples 111b = 128 samples

8.6.5 OPMODE_CFG Register (Address = 0x4) [reset = 0x0]

OPMODE_CFG is shown in Figure 23 and described in Table 16.

Return to the Summary Table.

Figure 23. OPMODE_CFG Register

7	6	5	4	3	2	1	0
CONV_ON_ERR	CONV_MODE[1:0]		OSC_SEL	CLK_DIV[3:0]			
R/W-0b	R/W-0b		R/W-0b	R/W-0b			

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Table 16. OPMODE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CONV_ON_ERR	R/W	0b	Control continuation of autonomous modes if CRC error is detected on communication interface. 0b = If CRC error is detected, device continues channel sequencing and pin configuration is retained. See the CRC_ERR_IN bit for more details. 1b = If CRC error is detected, device changes all channels to analog inputs and channel sequencing is paused until CRC_ERR_IN bit is set to 0b. After clearing CRC_ERR_IN flag, device resumes channel sequencing and pin confguration is restored.
6-5	CONV_MODE[1:0]	R/W	0b	These bits set the mode of conversion of the ADC. 0b = Manual mode; conversions are initiated by the host. 1b = Autonomous mode; conversions are initiated by the internal state machine.
4	OSC_SEL	R/W	0b	Selects the oscillator for internal timing generation. 0b = High-speed oscillator. 1b = Low-power oscillator.
3-0	CLK_DIV[3:0]	R/W	0b	Sampling speed control in autonomous monitoring mode (CONV_MODE = 01b). See the section on oscillator and timing control for details.

8.6.6 PIN_CFG Register (Address = 0x5) [reset = 0x0]

PIN_CFG is shown in Figure 24 and described in Table 17.

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Figure 24. PIN_CFG Register

7	6	5	4	3	2	1	0
PIN_CFG[7:0]							
R/W-0b							

Table 17. PIN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PIN_CFG[7:0]	R/W	0b	Configure device channels AIN/GPIO[7:0] as analog inputs or GPIOs. 0b = Channel is configured as analog input. 1b = Channel is configured as GPIO.

8.6.7 GPIO_CFG Register (Address = 0x7) [reset = 0x0]

GPIO_CFG is shown in Figure 25 and described in Table 18.

Return to the Summary Table.

Figure 25. GPIO_CFG Register

7	6	5	4	3	2	1	0
GPIO_CFG[7:0]							
R/W-0b							

Table 18. GPIO_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPIO_CFG[7:0]	R/W	0b	Configure GPIO[7:0] as either digital inputs or digital outputs. 0b = GPIO is configured as digital input. 1b = GPIO is configured as digital output.

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8.6.8 GPO_DRIVE_CFG Register (Address = 0x9) [reset = 0x0]

GPO_DRIVE_CFG is shown in Figure 26 and described in Table 19.

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Figure 26. GPO_DRIVE_CFG Register

7	6	5	4	3	2	1	0
GPO_DRIVE_CFG[7:0]							
R/W-0b							

Table 19. GPO_DRIVE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO_DRIVE_CFG[7:0]	R/W	0b	Configure digital outputs GPO[7:0] as either open-drain or push-pull outputs. 0b = Digital output is open-drain; connect external pullup resistor. 1b = Pushpull driver is used for digital output.

8.6.9 GPO_OUTPUT_VALUE Register (Address = 0xB) [reset = 0x0]

GPO_OUTPUT_VALUE is shown in Figure 27 and described in Table 20.

Return to the Summary Table.

Figure 27. GPO_OUTPUT_VALUE Register

7	6	5	4	3	2	1	0
GPO_OUTPUT_VALUE[7:0]							
R/W-0b							

Table 20. GPO_OUTPUT_VALUE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO_OUTPUT_VALUE[7:0]	R/W	0b	Logic level to be set on digital outputs GPO[7:0]. 0b = Digital output set to logic 0. 1b = Digital output set to logic 1.

8.6.10 GPI_VALUE Register (Address = 0xD) [reset = 0x0]

GPI_VALUE is shown in Figure 28 and described in Table 21.

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Figure 28. GPI_VALUE Register

7	6	5	4	3	2	1	0
GPI_VALUE[7:0]							
R-0b							

Table 21. GPI_VALUE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPI_VALUE[7:0]	R	0b	Readback the logic level on GPIO[7:0]. 0b = GPIO is at logic 0. 1b = GPIO is at logic 1.

8.6.11 ZCD_BLANKING_CFG Register (Address = 0xF) [reset = 0x0]

ZCD_BLANKING_CFG is shown in Figure 29 and described in Table 22.

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Figure 29. ZCD_BLANKING_CFG Register

7	6	5	4	3	2	1	0
MULT_EN	ZCD_BLANKING[6:0]						
R/W-0b	R/W-0b						

Table 22. ZCD_BLANKING_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MULT_EN	R/W	0b	Multiplier enable bit for the ZCD_BLANKING field. 0b = Blanking count = ZCD_BLANKING 1b = Blanking count = ZCD_BLANKING x 8
6-0	ZCD_BLANKING[6:0]	R/W	0b	This field defines the number of analog conversions, of the ZCD channel, which must be ignored for generating next ZCD event. The counting starts from ZCD event detection.

8.6.12 SEQUENCE_CFG Register (Address = 0x10) [reset = 0x0]

SEQUENCE_CFG is shown in Figure 30 and described in Table 23.

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Figure 30. SEQUENCE_CFG Register

7	6	5	4	3	2	1	0
RESERVED			SEQ_START	RESERVED		SEQ_MODE[1:0]	
R-0b			R/W-0b	R-0b		R/W-0b	

Table 23. SEQUENCE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0b	Reserved. Reads return 0.
4	SEQ_START	R/W	0b	Control for start of channel sequence when using auto sequence mode (SEQ_MODE = 01b). 0b = Stop channel sequencing. 1b = Start channel sequencing in ascending order for channels enabled in AUTO_SEQ_CH_SEL register.
3-2	RESERVED	R	0b	Reserved. Reads return 0.
1-0	SEQ_MODE[1:0]	R/W	0b	Selects the mode of scanning of analog input channels. 0b = Manual sequence mode; channel selected by MANUAL_CHID field. 1b = Auto sequence mode; channel selected by internal channel sequencer. 10b = Reserved. 11b = Reserved.

8.6.13 CHANNEL_SEL Register (Address = 0x11) [reset = 0x0]

CHANNEL_SEL is shown in Figure 31 and described in Table 24.

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Figure 31. CHANNEL_SEL Register

7	6	5	4	3	2	1	0
ZCD_CHID[3:0]				MANUAL_CHID[3:0]			
R/W-0b				R/W-0b			

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Table 24. CHANNEL_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	ZCD_CHID[3:0]	R/W	0b	Input channel to treat as ZCD input. If the selected channel is configured as an analog input, internally generated ZCD signal is used (setup thresholds accordingly). If the selected channel is a digital input, the digital signal on this channel is directly used as ZCD signal.
3-0	MANUAL_CHID[3:0]	R/W	0b	In manual mode (SEQ_MODE = 00b), this field contains the 4-bit channel ID of the analog input channel for next ADC conversion. For valid ADC data, the selected channel must not be configured as GPIO in PIN_CFG register. 0b = AIN0 1b = AIN1 10b = AIN2 11b = AIN3 100b = AIN4 101b = AIN5 110b = AIN6 111b = AIN7 1000b = Reserved.

8.6.14 AUTO_SEQ_CH_SEL Register (Address = 0x12) [reset = 0x0]

AUTO_SEQ_CH_SEL is shown in Figure 32 and described in Table 25.

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Figure 32. AUTO_SEQ_CH_SEL Register

7	6	5	4	3	2	1	0
AUTO_SEQ_CH_SEL[7:0]							
R/W-0b							

Table 25. AUTO_SEQ_CH_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	AUTO_SEQ_CH_SEL[7:0]	R/W	0b	Select analog input channels AIN[7:0] in for auto sequencing mode. 0b = Analog input channel is not enabled in scanning sequence. 1b = Analog input channel is enabled in scanning sequence.

8.6.15 ALERT_CH_SEL Register (Address = 0x14) [reset = 0x0]

ALERT_CH_SEL is shown in Figure 33 and described in Table 26.

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Figure 33. ALERT_CH_SEL Register

7	6	5	4	3	2	1	0
ALERT_CH_SEL[7:0]							
R/W-0b							

Table 26. ALERT_CH_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ALERT_CH_SEL[7:0]	R/W	0b	Select channels for which the alert flags can assert the ALERT pin. 0b = Alert flags for this channel do not assert the ALERT pin. 1b = Alert flags for this channel assert the ALERT pin.

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8.6.16 ALERT_MAP Register (Address = 0x16) [reset = 0x0]

ALERT_MAP is shown in Figure 34 and described in Table 27.

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Figure 34. ALERT_MAP Register

7	6	5	4	3	2	1	0
RESERVED						ALERT_RMS	ALERT_CRCIN
R-0b						R/W-0b	R/W-0b

Table 27. ALERT_MAP Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0b	Reserved. Reads return 0.
1	ALERT_RMS	R/W	0b	Enable or disable the notification on the ALERT pin based on the status of RMS computation (RMS_DONE = 1b). 0b = ALERT pin is not asserted when RMS_DONE =1b. 1b = ALERT pin is asserted when RMS_DONE = 1b. Clear RMS_DONE flag to deassert the ALERT pin.
0	ALERT_CRCIN	R/W	0b	Enable or disable the notification on the ALERT pin for CRC error on input data (CRCERR_IN = 1b). 0b = ALERT pin is not asserted when CRCERR_IN = 1b. 1b = ALERT pin is asserted when CRCERR_IN = 1b. Clear CRCERR_IN for deasserting the ALERT pin.

8.6.17 ALERT_PIN_CFG Register (Address = 0x17) [reset = 0x0]

ALERT_PIN_CFG is shown in Figure 35 and described in Table 28.

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Figure 35. ALERT_PIN_CFG Register

7	6	5	4	3	2	1	0
RESERVED					ALERT_DRIVE	ALERT_LOGIC[1:0]	
R-0b					R/W-0b	R/W-0b	

Table 28. ALERT_PIN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0b	Reserved. Reads return 0.
2	ALERT_DRIVE	R/W	0b	Configure output drive of the ALERT pin. 0b = Open-drain output. Connect external pullup resistor. 1b = Push-pull output.
1-0	ALERT_LOGIC[1:0]	R/W	0b	Configure how the ALERT pin is asserted. 0b = Pulsed high (one logic high pulse one time per alert flag). 1b = Active high.

8.6.18 EVENT_FLAG Register (Address = 0x18) [reset = 0x0]

EVENT_FLAG is shown in Figure 36 and described in Table 29.

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Figure 36. EVENT_FLAG Register

7	6	5	4	3	2	1	0
EVENT_FLAG[7:0]							
R-0b							

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Table 29. EVENT_FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EVENT_FLAG[7:0]	R	0b	Alert flags indicating digital window comparator status for CH[7:0]. Write 0b to individual bits of high/low register to clear alert flag. 0b = Event condition not detected. 1b = Event condition detected.

8.6.19 EVENT_HIGH_FLAG Register (Address = 0x1A) [reset = 0x0]

EVENT_HIGH_FLAG is shown in Figure 37 and described in Table 30.

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Figure 37. EVENT_HIGH_FLAG Register

7	6	5	4	3	2	1	0
EVENT_HIGH_FLAG[7:0]							
R/W-0b							

Table 30. EVENT_HIGH_FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EVENT_HIGH_FLAG[7:0]	R/W	0b	Alert flag corresponding to high threshold of analog input or logic 1 on digital input on CH[7:0]. Write 1b to clear this flag. 0b = No alert condition detected. 1b = Either high threshold was exceeded (analog input) or logic 1 was detected (digital input).

8.6.20 EVENT_LOW_FLAG Register (Address = 0x1C) [reset = 0x0]

EVENT_LOW_FLAG is shown in Figure 38 and described in Table 31.

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Figure 38. EVENT_LOW_FLAG Register

7	6	5	4	3	2	1	0
EVENT_LOW_FLAG[7:0]							
R/W-0b							

Table 31. EVENT_LOW_FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EVENT_LOW_FLAG[7:0]	R/W	0b	Alert flag corresponding to low threshold of analog input or logic 0 on digital input on CH[7:0]. Write 1b to clear this flag. 0b = No Event condition detected. 1b = Either low threshold was exceeded (analog input) or logic 0 was detected (digital input).

8.6.21 EVENT_RGN Register (Address = 0x1E) [reset = 0x0]

EVENT_RGN is shown in Figure 39 and described in Table 32.

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Figure 39. EVENT_RGN Register

7	6	5	4	3	2	1	0
EVENT_RGN[7:0]							
R/W-0b							

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Table 32. EVENT_RGN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EVENT_RGN[7:0]	R/W	0b	Choice of region used in monitoring analog/digital inputs CH[7:0]. 0b = Alert flag is set if: (conversion result < low threshold) or (conversion result > high threshold). For digital inputs, logic 1 sets the alert flag. 1b = Alert flag is set if: (low threshold > conversion result < high threshold). For digital inputs, logic 0 sets the alert flag.

8.6.22 HYSTERESIS_CH0 Register (Address = 0x20) [reset = 0xF0]

HYSTERESIS_CH0 is shown in Figure 40 and described in Table 33.

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Figure 40. HYSTERESIS_CH0 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH0_LSB[3:0]				HYSTERESIS_CH0[3:0]			
R/W-1111b				R/W-0b			

Table 33. HYSTERESIS_CH0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH0_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH0[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteris is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

8.6.23 HIGH_TH_CH0 Register (Address = 0x21) [reset = 0xFF]

HIGH_TH_CH0 is shown in Figure 41 and described in Table 34.

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Figure 41. HIGH_TH_CH0 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH0_MSB[7:0]							
R/W-11111111b							

Table 34. HIGH_TH_CH0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH0_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.24 EVENT_COUNT_CH0 Register (Address = 0x22) [reset = 0x0]

EVENT_COUNT_CH0 is shown in Figure 42 and described in Table 35.

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Figure 42. EVENT_COUNT_CH0 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH0_LSB[3:0]				EVENT_COUNT_CH0[3:0]			
R/W-0b				R/W-0b			

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Table 35. EVENT_COUNT_CH0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH0_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH0[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting event flag.

8.6.25 LOW_TH_CH0 Register (Address = 0x23) [reset = 0x0]

LOW_TH_CH0 is shown in Figure 43 and described in Table 36.

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Figure 43. LOW_TH_CH0 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH0_MSB[7:0]							
R/W-0b							

Table 36. LOW_TH_CH0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH0_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.26 HYSTERESIS_CH1 Register (Address = 0x24) [reset = 0xF0]

HYSTERESIS_CH1 is shown in Figure 44 and described in Table 37.

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Figure 44. HYSTERESIS_CH1 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH1_LSB[3:0]				HYSTERESIS_CH1[3:0]			
R/W-1111b				R/W-0b			

Table 37. HYSTERESIS_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH1_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH1[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteris is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

8.6.27 HIGH_TH_CH1 Register (Address = 0x25) [reset = 0xFF]

HIGH_TH_CH1 is shown in Figure 45 and described in Table 38.

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Figure 45. HIGH_TH_CH1 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH1_MSB[7:0]							
R/W-11111111b							

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Table 38. HIGH_TH_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH1_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.28 EVENT_COUNT_CH1 Register (Address = 0x26) [reset = 0x0]

EVENT_COUNT_CH1 is shown in Figure 46 and described in Table 39.

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Figure 46. EVENT_COUNT_CH1 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH1_LSB[3:0]				EVENT_COUNT_CH1[3:0]			
R/W-0b				R/W-0b			

Table 39. EVENT_COUNT_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH1_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH1[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting event flag.

8.6.29 LOW_TH_CH1 Register (Address = 0x27) [reset = 0x0]

LOW_TH_CH1 is shown in Figure 47 and described in Table 40.

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Figure 47. LOW_TH_CH1 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH1_MSB[7:0]							
R/W-0b							

Table 40. LOW_TH_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH1_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.30 HYSTERESIS_CH2 Register (Address = 0x28) [reset = 0xF0]

HYSTERESIS_CH2 is shown in Figure 48 and described in Table 41.

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Figure 48. HYSTERESIS_CH2 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH2_LSB[3:0]				HYSTERESIS_CH2[3:0]			
R/W-1111b				R/W-0b			

Table 41. HYSTERESIS_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH2_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.

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Table 41. HYSTERESIS_CH2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	HYSTERESIS_CH2[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteris is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

8.6.31 HIGH_TH_CH2 Register (Address = 0x29) [reset = 0xFF]

HIGH_TH_CH2 is shown in Figure 49 and described in Table 42.

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Figure 49. HIGH_TH_CH2 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH2_MSB[7:0]							
R/W-11111111b							

Table 42. HIGH_TH_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH2_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.32 EVENT_COUNT_CH2 Register (Address = 0x2A) [reset = 0x0]

EVENT_COUNT_CH2 is shown in Figure 50 and described in Table 43.

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Figure 50. EVENT_COUNT_CH2 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH2_LSB[3:0]				EVENT_COUNT_CH2[3:0]			
R/W-0b				R/W-0b			

Table 43. EVENT_COUNT_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH2_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH2[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting event flag.

8.6.33 LOW_TH_CH2 Register (Address = 0x2B) [reset = 0x0]

LOW_TH_CH2 is shown in Figure 51 and described in Table 44.

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Figure 51. LOW_TH_CH2 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH2_MSB[7:0]							
R/W-0b							

Table 44. LOW_TH_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH2_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

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8.6.34 HYSTERESIS_CH3 Register (Address = 0x2C) [reset = 0xF0]

HYSTERESIS_CH3 is shown in Figure 52 and described in Table 45.

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Figure 52. HYSTERESIS_CH3 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH3_LSB[3:0]				HYSTERESIS_CH3[3:0]			
R/W-1111b				R/W-0b			

Table 45. HYSTERESIS_CH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH3_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH3[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteris is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

8.6.35 HIGH_TH_CH3 Register (Address = 0x2D) [reset = 0xFF]

HIGH_TH_CH3 is shown in Figure 53 and described in Table 46.

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Figure 53. HIGH_TH_CH3 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH3_MSB[7:0]							
R/W-11111111b							

Table 46. HIGH_TH_CH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH3_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.36 EVENT_COUNT_CH3 Register (Address = 0x2E) [reset = 0x0]

EVENT_COUNT_CH3 is shown in Figure 54 and described in Table 47.

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Figure 54. EVENT_COUNT_CH3 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH3_LSB[3:0]				EVENT_COUNT_CH3[3:0]			
R/W-0b				R/W-0b			

Table 47. EVENT_COUNT_CH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH3_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH3[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting event flag.

8.6.37 LOW_TH_CH3 Register (Address = 0x2F) [reset = 0x0]

LOW_TH_CH3 is shown in Figure 55 and described in Table 48.

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Figure 55. LOW_TH_CH3 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH3_MSB[7:0]							
R/W-0b							

Table 48. LOW_TH_CH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH3_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.38 HYSTERESIS_CH4 Register (Address = 0x30) [reset = 0xF0]

HYSTERESIS_CH4 is shown in Figure 56 and described in Table 49.

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Figure 56. HYSTERESIS_CH4 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH4_LSB[3:0]				HYSTERESIS_CH4[3:0]			
R/W-1111b				R/W-0b			

Table 49. HYSTERESIS_CH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH4_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH4[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteris is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

8.6.39 HIGH_TH_CH4 Register (Address = 0x31) [reset = 0xFF]

HIGH_TH_CH4 is shown in Figure 57 and described in Table 50.

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Figure 57. HIGH_TH_CH4 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH4_MSB[7:0]							
R/W-11111111b							

Table 50. HIGH_TH_CH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH4_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.40 EVENT_COUNT_CH4 Register (Address = 0x32) [reset = 0x0]

EVENT_COUNT_CH4 is shown in Figure 58 and described in Table 51.

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Figure 58. EVENT_COUNT_CH4 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH4_LSB[3:0]				EVENT_COUNT_CH4[3:0]			
R/W-0b				R/W-0b			

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Table 51. EVENT_COUNT_CH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH4_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH4[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting event flag.

8.6.41 LOW_TH_CH4 Register (Address = 0x33) [reset = 0x0]

LOW_TH_CH4 is shown in Figure 59 and described in Table 52.

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Figure 59. LOW_TH_CH4 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH4_MSB[7:0]							
R/W-0b							

Table 52. LOW_TH_CH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH4_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.42 HYSTERESIS_CH5 Register (Address = 0x34) [reset = 0xF0]

HYSTERESIS_CH5 is shown in Figure 60 and described in Table 53.

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Figure 60. HYSTERESIS_CH5 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH5_LSB[3:0]				HYSTERESIS_CH5[3:0]			
R/W-1111b				R/W-0b			

Table 53. HYSTERESIS_CH5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH5_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH5[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteris is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

8.6.43 HIGH_TH_CH5 Register (Address = 0x35) [reset = 0xFF]

HIGH_TH_CH5 is shown in Figure 61 and described in Table 54.

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Figure 61. HIGH_TH_CH5 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH5_MSB[7:0]							
R/W-11111111b							

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Table 54. HIGH_TH_CH5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH5_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.44 EVENT_COUNT_CH5 Register (Address = 0x36) [reset = 0x0]

EVENT_COUNT_CH5 is shown in Figure 62 and described in Table 55.

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Figure 62. EVENT_COUNT_CH5 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH5_LSB[3:0]				EVENT_COUNT_CH5[3:0]			
R/W-0b				R/W-0b			

Table 55. EVENT_COUNT_CH5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH5_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH5[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting event flag.

8.6.45 LOW_TH_CH5 Register (Address = 0x37) [reset = 0x0]

LOW_TH_CH5 is shown in Figure 63 and described in Table 56.

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Figure 63. LOW_TH_CH5 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH5_MSB[7:0]							
R/W-0b							

Table 56. LOW_TH_CH5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH5_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.46 HYSTERESIS_CH6 Register (Address = 0x38) [reset = 0xF0]

HYSTERESIS_CH6 is shown in Figure 64 and described in Table 57.

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Figure 64. HYSTERESIS_CH6 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH6_LSB[3:0]				HYSTERESIS_CH6[3:0]			
R/W-1111b				R/W-0b			

Table 57. HYSTERESIS_CH6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH6_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.

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Table 57. HYSTERESIS_CH6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	HYSTERESIS_CH6[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteris is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

8.6.47 HIGH_TH_CH6 Register (Address = 0x39) [reset = 0xFF]

HIGH_TH_CH6 is shown in Figure 65 and described in Table 58.

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Figure 65. HIGH_TH_CH6 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH6_MSB[7:0]							
R/W-11111111b							

Table 58. HIGH_TH_CH6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH6_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.48 EVENT_COUNT_CH6 Register (Address = 0x3A) [reset = 0x0]

EVENT_COUNT_CH6 is shown in Figure 66 and described in Table 59.

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Figure 66. EVENT_COUNT_CH6 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH6_LSB[3:0]				EVENT_COUNT_CH6[3:0]			
R/W-0b				R/W-0b			

Table 59. EVENT_COUNT_CH6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH6_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH6[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting event flag.

8.6.49 LOW_TH_CH6 Register (Address = 0x3B) [reset = 0x0]

LOW_TH_CH6 is shown in Figure 67 and described in Table 60.

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Figure 67. LOW_TH_CH6 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH6_MSB[7:0]							
R/W-0b							

Table 60. LOW_TH_CH6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH6_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

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8.6.50 HYSTERESIS_CH7 Register (Address = 0x3C) [reset = 0xF0]

HYSTERESIS_CH7 is shown in Figure 68 and described in Table 61.

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Figure 68. HYSTERESIS_CH7 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH7_LSB[3:0]				HYSTERESIS_CH7[3:0]			
R/W-1111b				R/W-0b			

Table 61. HYSTERESIS_CH7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH7_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH7[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteris is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

8.6.51 HIGH_TH_CH7 Register (Address = 0x3D) [reset = 0xFF]

HIGH_TH_CH7 is shown in Figure 69 and described in Table 62.

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Figure 69. HIGH_TH_CH7 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH7_MSB[7:0]							
R/W-11111111b							

Table 62. HIGH_TH_CH7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH7_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.52 EVENT_COUNT_CH7 Register (Address = 0x3E) [reset = 0x0]

EVENT_COUNT_CH7 is shown in Figure 70 and described in Table 63.

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Figure 70. EVENT_COUNT_CH7 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH7_LSB[3:0]				EVENT_COUNT_CH7[3:0]			
R/W-0b				R/W-0b			

Table 63. EVENT_COUNT_CH7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH7_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH7[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting event flag.

8.6.53 LOW_TH_CH7 Register (Address = 0x3F) [reset = 0x0]

LOW_TH_CH7 is shown in Figure 71 and described in Table 64.

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Figure 71. LOW_TH_CH7 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH7_MSB[7:0]							
R/W-0b							

Table 64. LOW_TH_CH7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH7_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.54 MAX_CH0_LSB Register (Address = 0x60) [reset = 0x0]

MAX_CH0_LSB is shown in Figure 72 and described in Table 65.

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Figure 72. MAX_CH0_LSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH0_LSB[7:0]							
R-0b							

Table 65. MAX_CH0_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH0_LSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.6.55 MAX_CH0_MSB Register (Address = 0x61) [reset = 0x0]

MAX_CH0_MSB is shown in Figure 73 and described in Table 66.

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Figure 73. MAX_CH0_MSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH0_MSB[7:0]							
R-0b							

Table 66. MAX_CH0_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH0_MSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.6.56 MAX_CH1_LSB Register (Address = 0x62) [reset = 0x0]

MAX_CH1_LSB is shown in Figure 74 and described in Table 67.

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Figure 74. MAX_CH1_LSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH1_LSB[7:0]							
R-0b							

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Table 67. MAX_CH1_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH1_LSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.6.57 MAX_CH1_MSB Register (Address = 0x63) [reset = 0x0]

MAX_CH1_MSB is shown in Figure 75 and described in Table 68.

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Figure 75. MAX_CH1_MSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH1_MSB[7:0]							
R-0b							

Table 68. MAX_CH1_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH1_MSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.6.58 MAX_CH2_LSB Register (Address = 0x64) [reset = 0x0]

MAX_CH2_LSB is shown in Figure 76 and described in Table 69.

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Figure 76. MAX_CH2_LSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH2_LSB[7:0]							
R-0b							

Table 69. MAX_CH2_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH2_LSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.6.59 MAX_CH2_MSB Register (Address = 0x65) [reset = 0x0]

MAX_CH2_MSB is shown in Figure 77 and described in Table 70.

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Figure 77. MAX_CH2_MSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH2_MSB[7:0]							
R-0b							

Table 70. MAX_CH2_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH2_MSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

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8.6.60 MAX_CH3_LSB Register (Address = 0x66) [reset = 0x0]

MAX_CH3_LSB is shown in Figure 78 and described in Table 71.

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Figure 78. MAX_CH3_LSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH3_LSB[7:0]							
R-0b							

Table 71. MAX_CH3_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH3_LSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.6.61 MAX_CH3_MSB Register (Address = 0x67) [reset = 0x0]

MAX_CH3_MSB is shown in Figure 79 and described in Table 72.

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Figure 79. MAX_CH3_MSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH3_MSB[7:0]							
R-0b							

Table 72. MAX_CH3_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH3_MSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.6.62 MAX_CH4_LSB Register (Address = 0x68) [reset = 0x0]

MAX_CH4_LSB is shown in Figure 80 and described in Table 73.

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Figure 80. MAX_CH4_LSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH4_LSB[7:0]							
R-0b							

Table 73. MAX_CH4_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH4_LSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.6.63 MAX_CH4_MSB Register (Address = 0x69) [reset = 0x0]

MAX_CH4_MSB is shown in Figure 81 and described in Table 74.

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Figure 81. MAX_CH4_MSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH4_MSB[7:0]							
R-0b							

Table 74. MAX_CH4_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH4_MSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.6.64 MAX_CH5_LSB Register (Address = 0x6A) [reset = 0x0]

MAX_CH5_LSB is shown in Figure 82 and described in Table 75.

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Figure 82. MAX_CH5_LSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH5_LSB[7:0]							
R-0b							

Table 75. MAX_CH5_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH5_LSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.6.65 MAX_CH5_MSB Register (Address = 0x6B) [reset = 0x0]

MAX_CH5_MSB is shown in Figure 83 and described in Table 76.

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Figure 83. MAX_CH5_MSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH5_MSB[7:0]							
R-0b							

Table 76. MAX_CH5_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH5_MSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.6.66 MAX_CH6_LSB Register (Address = 0x6C) [reset = 0x0]

MAX_CH6_LSB is shown in Figure 84 and described in Table 77.

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Figure 84. MAX_CH6_LSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH6_LSB[7:0]							
R-0b							

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Table 77. MAX_CH6_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH6_LSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.6.67 MAX_CH6_MSB Register (Address = 0x6D) [reset = 0x0]

MAX_CH6_MSB is shown in Figure 85 and described in Table 78.

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Figure 85. MAX_CH6_MSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH6_MSB[7:0]							
R-0b							

Table 78. MAX_CH6_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH6_MSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.6.68 MAX_CH7_LSB Register (Address = 0x6E) [reset = 0x0]

MAX_CH7_LSB is shown in Figure 86 and described in Table 79.

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Figure 86. MAX_CH7_LSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH7_LSB[7:0]							
R-0b							

Table 79. MAX_CH7_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH7_LSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.6.69 MAX_CH7_MSB Register (Address = 0x6F) [reset = 0x0]

MAX_CH7_MSB is shown in Figure 87 and described in Table 80.

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Figure 87. MAX_CH7_MSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH7_MSB[7:0]							
R-0b							

Table 80. MAX_CH7_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH7_MSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

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8.6.70 MIN_CH0_LSB Register (Address = 0x80) [reset = 0xFF]

MIN_CH0_LSB is shown in Figure 88 and described in Table 81.

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Figure 88. MIN_CH0_LSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH0_LSB[7:0]							
R-11111111b							

Table 81. MIN_CH0_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH0_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.6.71 MIN_CH0_MSB Register (Address = 0x81) [reset = 0xFF]

MIN_CH0_MSB is shown in Figure 89 and described in Table 82.

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Figure 89. MIN_CH0_MSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH0_MSB[7:0]							
R-11111111b							

Table 82. MIN_CH0_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH0_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.6.72 MIN_CH1_LSB Register (Address = 0x82) [reset = 0xFF]

MIN_CH1_LSB is shown in Figure 90 and described in Table 83.

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Figure 90. MIN_CH1_LSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH1_LSB[7:0]							
R-11111111b							

Table 83. MIN_CH1_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH1_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.6.73 MIN_CH1_MSB Register (Address = 0x83) [reset = 0xFF]

MIN_CH1_MSB is shown in Figure 91 and described in Table 84.

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Figure 91. MIN_CH1_MSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH1_MSB[7:0]							
R-11111111b							

Table 84. MIN_CH1_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH1_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.6.74 MIN_CH2_LSB Register (Address = 0x84) [reset = 0xFF]

MIN_CH2_LSB is shown in Figure 92 and described in Table 85.

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Figure 92. MIN_CH2_LSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH2_LSB[7:0]							
R-11111111b							

Table 85. MIN_CH2_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH2_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.6.75 MIN_CH2_MSB Register (Address = 0x85) [reset = 0xFF]

MIN_CH2_MSB is shown in Figure 93 and described in Table 86.

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Figure 93. MIN_CH2_MSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH2_MSB[7:0]							
R-11111111b							

Table 86. MIN_CH2_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH2_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.6.76 MIN_CH3_LSB Register (Address = 0x86) [reset = 0xFF]

MIN_CH3_LSB is shown in Figure 94 and described in Table 87.

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Figure 94. MIN_CH3_LSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH3_LSB[7:0]							
R-11111111b							

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Table 87. MIN_CH3_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH3_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.6.77 MIN_CH3_MSB Register (Address = 0x87) [reset = 0xFF]

MIN_CH3_MSB is shown in Figure 95 and described in Table 88.

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Figure 95. MIN_CH3_MSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH3_MSB[7:0]							
R-11111111b							

Table 88. MIN_CH3_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH3_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.6.78 MIN_CH4_LSB Register (Address = 0x88) [reset = 0xFF]

MIN_CH4_LSB is shown in Figure 96 and described in Table 89.

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Figure 96. MIN_CH4_LSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH4_LSB[7:0]							
R-11111111b							

Table 89. MIN_CH4_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH4_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.6.79 MIN_CH4_MSB Register (Address = 0x89) [reset = 0xFF]

MIN_CH4_MSB is shown in Figure 97 and described in Table 90.

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Figure 97. MIN_CH4_MSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH4_MSB[7:0]							
R-11111111b							

Table 90. MIN_CH4_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH4_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

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8.6.80 MIN_CH5_LSB Register (Address = 0x8A) [reset = 0xFF]

MIN_CH5_LSB is shown in Figure 98 and described in Table 91.

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Figure 98. MIN_CH5_LSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH5_LSB[7:0]							
R-11111111b							

Table 91. MIN_CH5_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH5_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.6.81 MIN_CH5_MSB Register (Address = 0x8B) [reset = 0xFF]

MIN_CH5_MSB is shown in Figure 99 and described in Table 92.

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Figure 99. MIN_CH5_MSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH5_MSB[7:0]							
R-11111111b							

Table 92. MIN_CH5_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH5_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.6.82 MIN_CH6_LSB Register (Address = 0x8C) [reset = 0xFF]

MIN_CH6_LSB is shown in Figure 100 and described in Table 93.

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Figure 100. MIN_CH6_LSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH6_LSB[7:0]							
R-11111111b							

Table 93. MIN_CH6_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH6_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.6.83 MIN_CH6_MSB Register (Address = 0x8D) [reset = 0xFF]

MIN_CH6_MSB is shown in Figure 101 and described in Table 94.

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Figure 101. MIN_CH6_MSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH6_MSB[7:0]							
R-11111111b							

Table 94. MIN_CH6_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH6_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.6.84 MIN_CH7_LSB Register (Address = 0x8E) [reset = 0xFF]

MIN_CH7_LSB is shown in Figure 102 and described in Table 95.

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Figure 102. MIN_CH7_LSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH7_LSB[7:0]							
R-11111111b							

Table 95. MIN_CH7_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH7_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.6.85 MIN_CH7_MSB Register (Address = 0x8F) [reset = 0xFF]

MIN_CH7_MSB is shown in Figure 103 and described in Table 96.

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Figure 103. MIN_CH7_MSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH7_MSB[7:0]							
R-11111111b							

Table 96. MIN_CH7_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH7_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.6.86 RECENT_CH0_LSB Register (Address = 0xA0) [reset = 0x0]

RECENT_CH0_LSB is shown in Figure 104 and described in Table 97.

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Figure 104. RECENT_CH0_LSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH0_LSB[7:0]							
R-0b							

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Table 97. RECENT_CH0_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH0_LSB[7:0]	R	0b	Lower 8 bits of the last conversion result for this analog input channel.

8.6.87 RECENT_CH0_MSB Register (Address = 0xA1) [reset = 0x0]

RECENT_CH0_MSB is shown in Figure 105 and described in Table 98.

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Figure 105. RECENT_CH0_MSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH0_MSB[7:0]							
R-0b							

Table 98. RECENT_CH0_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH0_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last conversion result for this analog input channel.

8.6.88 RECENT_CH1_LSB Register (Address = 0xA2) [reset = 0x0]

RECENT_CH1_LSB is shown in Figure 106 and described in Table 99.

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Figure 106. RECENT_CH1_LSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH1_LSB[7:0]							
R-0b							

Table 99. RECENT_CH1_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH1_LSB[7:0]	R	0b	Lower 8 bits of the last conversion result for this analog input channel.

8.6.89 RECENT_CH1_MSB Register (Address = 0xA3) [reset = 0x0]

RECENT_CH1_MSB is shown in Figure 107 and described in Table 100.

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Figure 107. RECENT_CH1_MSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH1_MSB[7:0]							
R-0b							

Table 100. RECENT_CH1_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH1_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last conversion result for this analog input channel.

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8.6.90 RECENT_CH2_LSB Register (Address = 0xA4) [reset = 0x0]

RECENT_CH2_LSB is shown in Figure 108 and described in Table 101.

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Figure 108. RECENT_CH2_LSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH2_LSB[7:0]							
R-0b							

Table 101. RECENT_CH2_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH2_LSB[7:0]	R	0b	Lower 8 bits of the last conversion result for this analog input channel.

8.6.91 RECENT_CH2_MSB Register (Address = 0xA5) [reset = 0x0]

RECENT_CH2_MSB is shown in Figure 109 and described in Table 102.

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Figure 109. RECENT_CH2_MSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH2_MSB[7:0]							
R-0b							

Table 102. RECENT_CH2_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH2_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last conversion result for this analog input channel.

8.6.92 RECENT_CH3_LSB Register (Address = 0xA6) [reset = 0x0]

RECENT_CH3_LSB is shown in Figure 110 and described in Table 103.

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Figure 110. RECENT_CH3_LSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH3_LSB[7:0]							
R-0b							

Table 103. RECENT_CH3_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH3_LSB[7:0]	R	0b	Lower 8 bits of the last conversion result for this analog input channel.

8.6.93 RECENT_CH3_MSB Register (Address = 0xA7) [reset = 0x0]

RECENT_CH3_MSB is shown in Figure 111 and described in Table 104.

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Figure 111. RECENT_CH3_MSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH3_MSB[7:0]							
R-0b							

Table 104. RECENT_CH3_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH3_MSB [7:0]	R	0b	MSB aligned first 8 bits of the last conversion result for this analog input channel.

8.6.94 RECENT_CH4_LSB Register (Address = 0xA8) [reset = 0x0]

RECENT_CH4_LSB is shown in Figure 112 and described in Table 105.

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Figure 112. RECENT_CH4_LSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH4_LSB[7:0]							
R-0b							

Table 105. RECENT_CH4_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH4_LSB[7:0]	R	0b	Lower 8 bits of the last conversion result for this analog input channel.

8.6.95 RECENT_CH4_MSB Register (Address = 0xA9) [reset = 0x0]

RECENT_CH4_MSB is shown in Figure 113 and described in Table 106.

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Figure 113. RECENT_CH4_MSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH4_MSB[7:0]							
R-0b							

Table 106. RECENT_CH4_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH4_MSB [7:0]	R	0b	MSB aligned first 8 bits of the last conversion result for this analog input channel.

8.6.96 RECENT_CH5_LSB Register (Address = 0xAA) [reset = 0x0]

RECENT_CH5_LSB is shown in Figure 114 and described in Table 107.

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Figure 114. RECENT_CH5_LSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH5_LSB[7:0]							
R-0b							

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Table 107. RECENT_CH5_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH5_LSB[7:0]	R	0b	Lower 8 bits of the last conversion result for this analog input channel.

8.6.97 RECENT_CH5_MSB Register (Address = 0xAB) [reset = 0x0]

RECENT_CH5_MSB is shown in Figure 115 and described in Table 108.

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Figure 115. RECENT_CH5_MSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH5_MSB[7:0]							
R-0b							

Table 108. RECENT_CH5_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH5_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last conversion result for this analog input channel.

8.6.98 RECENT_CH6_LSB Register (Address = 0xAC) [reset = 0x0]

RECENT_CH6_LSB is shown in Figure 116 and described in Table 109.

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Figure 116. RECENT_CH6_LSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH6_LSB[7:0]							
R-0b							

Table 109. RECENT_CH6_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH6_LSB[7:0]	R	0b	Lower 8 bits of the last conversion result for this analog input channel.

8.6.99 RECENT_CH6_MSB Register (Address = 0xAD) [reset = 0x0]

RECENT_CH6_MSB is shown in Figure 117 and described in Table 110.

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Figure 117. RECENT_CH6_MSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH6_MSB[7:0]							
R-0b							

Table 110. RECENT_CH6_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH6_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last conversion result for this analog input channel.

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8.6.100 RECENT_CH7_LSB Register (Address = 0xAE) [reset = 0x0]

RECENT_CH7_LSB is shown in Figure 118 and described in Table 111.

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Figure 118. RECENT_CH7_LSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH7_LSB[7:0]							
R-0b							

Table 111. RECENT_CH7_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH7_LSB[7:0]	R	0b	Lower 8 bits of the last conversion result for this analog input channel.

8.6.101 RECENT_CH7_MSB Register (Address = 0xAF) [reset = 0x0]

RECENT_CH7_MSB is shown in Figure 119 and described in Table 112.

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Figure 119. RECENT_CH7_MSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH7_MSB[7:0]							
R-0b							

Table 112. RECENT_CH7_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH7_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last conversion result for this analog input channel.

8.6.102 RMS_CFG Register (Address = 0xC0) [reset = 0x0]

RMS_CFG is shown in Figure 120 and described in Table 113.

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Figure 120. RMS_CFG Register

7	6	5	4	3	2	1	0
RMS_CHID[3:0]				RESERVED	RMS_DC_SUB	RMS_SAMPLES[1:0]	
R/W-0b				R-0b	R/W-0b	R/W-0b	

Table 113. RMS_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RMS_CHID[3:0]	R/W	0b	Select analog input channel for RMS computation.
3	RESERVED	R	0b	Reserved. Reads return 0b.
2	RMS_DC_SUB	R/W	0b	Subtract DC component from the RMS result. 0b = Do not subtract DC component. 1b = Subtract DC component.
1-0	RMS_SAMPLES[1:0]	R/W	0b	Number of samples for computing RMS result. Additional 40 samples are required for completing RMS computation. 0b = 1024 1b = 4096 10b = 16384 11b = 65536

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8.6.103 RMS_LSB Register (Address = 0xC1) [reset = 0x0]

RMS_LSB is shown in Figure 121 and described in Table 114.

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Figure 121. RMS_LSB Register

7	6	5	4	3	2	1	0
RMS_RESULT_LSB[7:0]							
R-0b							

Table 114. RMS_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RMS_RESULT_LSB[7:0]	R	0b	Lower 8-bits of RMS computation result.

8.6.104 RMS_MSB Register (Address = 0xC2) [reset = 0x0]

RMS_MSB is shown in Figure 122 and described in Table 115.

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Figure 122. RMS_MSB Register

7	6	5	4	3	2	1	0
RMS_RESULT_MSB[7:0]							
R-0b							

Table 115. RMS_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RMS_RESULT_MSB[7:0]	R	0b	Upper 8-bits of RMS result.

8.6.105 GPO0_TRIG_EVENT_SEL Register (Address = 0xC3) [reset = 0x2]

GPO0_TRIG_EVENT_SEL is shown in Figure 123 and described in Table 116.

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Figure 123. GPO0_TRIG_EVENT_SEL Register

7	6	5	4	3	2	1	0
GPO0_TRIG_EVENT_SEL[7:0]							
R/W-10b							

Table 116. GPO0_TRIG_EVENT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO0_TRIG_EVENT_SEL[7:0]	R/W	10b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO0. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO0 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit do trigger GPO0 output.

8.6.106 GPO1_TRIG_EVENT_SEL Register (Address = 0xC5) [reset = 0x2]

GPO1_TRIG_EVENT_SEL is shown in Figure 124 and described in Table 117.

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Figure 124. GPO1_TRIG_EVENT_SEL Register

7	6	5	4	3	2	1	0
GPO1_TRIG_EVENT_SEL[7:0]							
R/W-10b							

Table 117. GPO1_TRIG_EVENT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO1_TRIG_EVENT_SEL[7:0]	R/W	10b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO1. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO1 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit do trigger GPO1 output.

8.6.107 GPO2_TRIG_EVENT_SEL Register (Address = 0xC7) [reset = 0x2]

GPO2_TRIG_EVENT_SEL is shown in Figure 125 and described in Table 118.

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Figure 125. GPO2_TRIG_EVENT_SEL Register

7	6	5	4	3	2	1	0
GPO2_TRIG_EVENT_SEL[7:0]							
R/W-10b							

Table 118. GPO2_TRIG_EVENT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO2_TRIG_EVENT_SEL[7:0]	R/W	10b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO2. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO2 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit do trigger GPO2 output.

8.6.108 GPO3_TRIG_EVENT_SEL Register (Address = 0xC9) [reset = 0x2]

GPO3_TRIG_EVENT_SEL is shown in Figure 126 and described in Table 119.

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Figure 126. GPO3_TRIG_EVENT_SEL Register

7	6	5	4	3	2	1	0
GPO3_TRIG_EVENT_SEL[7:0]							
R/W-10b							

Table 119. GPO3_TRIG_EVENT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO3_TRIG_EVENT_SEL[7:0]	R/W	10b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO3. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO3 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit do trigger GPO3 output.

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8.6.109 GPO4_TRIG_EVENT_SEL Register (Address = 0xCB) [reset = 0x2]

GPO4_TRIG_EVENT_SEL is shown in Figure 127 and described in Table 120.

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Figure 127. GPO4_TRIG_EVENT_SEL Register

7	6	5	4	3	2	1	0
GPO4_TRIG_EVENT_SEL[7:0]							
R/W-10b							

Table 120. GPO4_TRIG_EVENT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO4_TRIG_EVENT_SEL[7:0]	R/W	10b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO4. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO4 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit do trigger GPO4 output.

8.6.110 GPO5_TRIG_EVENT_SEL Register (Address = 0xCD) [reset = 0x2]

GPO5_TRIG_EVENT_SEL is shown in Figure 128 and described in Table 121.

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Figure 128. GPO5_TRIG_EVENT_SEL Register

7	6	5	4	3	2	1	0
GPO0_TRIG_EVENT_SEL[7:0]							
R/W-10b							

Table 121. GPO5_TRIG_EVENT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO0_TRIG_EVENT_SEL[7:0]	R/W	10b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO5. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO5 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit do trigger GPO5 output.

8.6.111 GPO6_TRIG_EVENT_SEL Register (Address = 0xCF) [reset = 0x2]

GPO6_TRIG_EVENT_SEL is shown in Figure 129 and described in Table 122.

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Figure 129. GPO6_TRIG_EVENT_SEL Register

7	6	5	4	3	2	1	0
GPO6_TRIG_EVENT_SEL[7:0]							
R/W-10b							

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Table 122. GPO6_TRIG_EVENT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO6_TRIG_EVENT_SEL[7:0]	R/W	10b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO6. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO6 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit do trigger GPO6 output.

8.6.112 GPO7_TRIG_EVENT_SEL Register (Address = 0xD1) [reset = 0x2]

GPO7_TRIG_EVENT_SEL is shown in Figure 130 and described in Table 123.

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Figure 130. GPO7_TRIG_EVENT_SEL Register

7	6	5	4	3	2	1	0
GPO7_TRIG_EVENT_SEL[7:0]							
R/W-10b							

Table 123. GPO7_TRIG_EVENT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO7_TRIG_EVENT_SEL[7:0]	R/W	10b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO7. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO7 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit do trigger GPO7 output.

8.6.113 GPO_VALUE_ZCD_CFG_CH0_CH3 Register (Address = 0xE3) [reset = 0x0]

GPO_VALUE_ZCD_CFG_CH0_CH3 is shown in Figure 131 and described in Table 124.

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Figure 131. GPO_VALUE_ZCD_CFG_CH0_CH3 Register

7	6	5	4	3	2	1	0
GPO_VALUE_ZCD_CFG_CH3[1:0]		GPO_VALUE_ZCD_CFG_CH2[1:0]		GPO_VALUE_ZCD_CFG_CH1[1:0]		GPO_VALUE_ZCD_CFG_CH0[1:0]	
R/W-0b		R/W-0b		R/W-0b		R/W-0b	

Table 124. GPO_VALUE_ZCD_CFG_CH0_CH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	GPO_VALUE_ZCD_CFG_CH3[1:0]	R/W	0b	Define the GPO value to be launched on ZCD rising and falling edges. 0b = Rising (0) and falling (0) -> logic 0 on both edges 1b = Rising (0) and falling (1) -> $\overline{ZCD}$ 10b = Rising (1) and falling (0) -> ZCD 11b = Rising (1) and falling (1) -> logic 1 on both edges
5-4	GPO_VALUE_ZCD_CFG_CH2[1:0]	R/W	0b	Define the GPO value to be launched on ZCD rising and falling edges. 0b = Rising (0) and falling (0) -> logic 0 on both edges 1b = Rising (0) and falling (1) -> $\overline{ZCD}$ 10b = Rising (1) and falling (0) -> ZCD 11b = Rising (1) and falling (1) -> logic 1 on both edges

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Table 124. GPO_VALUE_ZCD_CFG_CH0_CH3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	GPO_VALUE_ZCD_CFG_CH1[1:0]	R/W	0b	Define the GPO value to be launched on ZCD rising and falling edges. 0b = Rising (0) and falling (0) -> logic 0 on both edges 1b = Rising (0) and falling (1) -> $\overline{ZCD}$ 10b = Rising (1) and falling (0) -> ZCD 11b = Rising (1) and falling (1) -> logic 1 on both edges
1-0	GPO_VALUE_ZCD_CFG_CH0[1:0]	R/W	0b	Define the GPO value to be launched on ZCD rising and falling edges. 0b = Rising (0) and falling (0) -> logic 0 on both edges 1b = Rising (0) and falling (1) -> $\overline{ZCD}$ 10b = Rising (1) and falling (0) -> ZCD 11b = Rising (1) and falling (1) -> logic 1 on both edges

8.6.114 GPO_VALUE_ZCD_CFG_CH4_CH7 Register (Address = 0xE4) [reset = 0x0]

GPO_VALUE_ZCD_CFG_CH4_CH7 is shown in Figure 132 and described in Table 125.

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Figure 132. GPO_VALUE_ZCD_CFG_CH4_CH7 Register

7	6	5	4	3	2	1	0
GPO_VALUE_ZCD_CFG_CH7[1:0]		GPO_VALUE_ZCD_CFG_CH6[1:0]		GPO_VALUE_ZCD_CFG_CH5[1:0]		GPO_VALUE_ZCD_CFG_CH4[1:0]	
R/W-0b		R/W-0b		R/W-0b		R/W-0b	

Table 125. GPO_VALUE_ZCD_CFG_CH4_CH7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	GPO_VALUE_ZCD_CFG_CH7[1:0]	R/W	0b	Define the GPO value to be launched on ZCD rising and falling edges. 0b = Rising (0) and falling (0) -> logic 0 on both edges 1b = Rising (0) and falling (1) -> $\overline{ZCD}$ 10b = Rising (1) and falling (0) -> ZCD 11b = Rising (1) and falling (1) -> logic 1 on both edges
5-4	GPO_VALUE_ZCD_CFG_CH6[1:0]	R/W	0b	Define the GPO value to be launched on ZCD rising and falling edges. 0b = Rising (0) and falling (0) -> logic 0 on both edges 1b = Rising (0) and falling (1) -> $\overline{ZCD}$ 10b = Rising (1) and falling (0) -> ZCD 11b = Rising (1) and falling (1) -> logic 1 on both edges
3-2	GPO_VALUE_ZCD_CFG_CH5[1:0]	R/W	0b	Define the GPO value to be launched on ZCD rising and falling edges. 0b = Rising (0) and falling (0) -> logic 0 on both edges 1b = Rising (0) and falling (1) -> $\overline{ZCD}$ 10b = Rising (1) and falling (0) -> ZCD 11b = Rising (1) and falling (1) -> logic 1 on both edges
1-0	GPO_VALUE_ZCD_CFG_CH4[1:0]	R/W	0b	Define the GPO value to be launched on ZCD rising and falling edges. 0b = Rising (0) and falling (0) -> logic 0 on both edges 1b = Rising (0) and falling (1) -> $\overline{ZCD}$ 10b = Rising (1) and falling (0) -> ZCD 11b = Rising (1) and falling (1) -> logic 1 on both edges

ADVANCE INFORMATION

8.6.115 GPO_ZCD_UPDATE_EN Register (Address = 0xE7) [reset = 0x0]

GPO_ZCD_UPDATE_EN is shown in Figure 133 and described in Table 126.

Return to the Summary Table.

Figure 133. GPO_ZCD_UPDATE_EN Register

7	6	5	4	3	2	1	0
GPO_ZCD_UPDATE_EN[7:0]							
R/W-0b							

Table 126. GPO_ZCD_UPDATE_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO_ZCD_UPDATE_EN[7:0]	R/W	0b	Update digital outputs GPO[7:0] synchronous to ZCD. 0b = Digital output is not updated synchronous to the ZCD event. 1b = Digital output is updated synchronous to ZCD event. Configure the GPO_VALUE_ON_ZCD_CFG register.

8.6.116 GPO_TRIGGER_CFG Register (Address = 0xE9) [reset = 0x0]

GPO_TRIGGER_CFG is shown in Figure 134 and described in Table 127.

Return to the Summary Table.

Figure 134. GPO_TRIGGER_CFG Register

7	6	5	4	3	2	1	0
GPO_TRIGGER_UPDATE_EN[7:0]							
R/W-0b							

Table 127. GPO_TRIGGER_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO_TRIGGER_UPDATE_EN[7:0]	R/W	0b	Update digital outputs GPO[7:0] when the corresponding trigger is set. 0b = Digital output is not updated in response to the alert flags. 1b = Digital output is updated when the corresponding alert flags are set. Configure GPOx_TRIG_EVENT_SEL register to select which alert flags can trigger an update on the desired GPO.

8.6.117 GPO_VALUE_TRIG Register (Address = 0xEB) [reset = 0x0]

GPO_VALUE_TRIG is shown in Figure 135 and described in Table 128.

Return to the Summary Table.

Figure 135. GPO_VALUE_TRIG Register

7	6	5	4	3	2	1	0
GPO_VALUE_ON_TRIGGER[7:0]							
R/W-0b							

Table 128. GPO_VALUE_TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO_VALUE_ON_TRIGGER[7:0]	R/W	0b	Value to be set on digital outputs GPO[7:0] when the corresponding trigger occurs. GPO update on alert flags must be enabled in the corresponding bit in the GPO_TRIGGER_CFG register. 0b = Digital output is set to logic 0. 1b = Digital output is set to logic 1.

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9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The two primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR), analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section details some general principles for designing the input driver circuit, reference driver circuit, and provides some application circuits designed for the ADS7128.

9.2 Typical Applications

9.2.1 Mixed-Channel Configuration

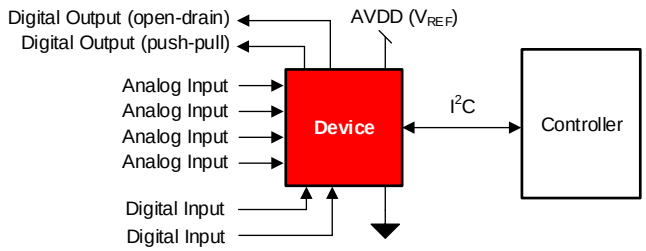

图 136. DAQ Circuit: Single-Supply DAQ

9.2.1.1 Design Requirements

The goal of this application is to configure some channels of the ADS7128 as digital inputs, open-drain digital outputs, and push-pull digital outputs.

9.2.1.2 Detailed Design Procedure

The ADS7128 can support GPIO functionality at each input pin. Any analog input pin can be independently configured as a digital input, a digital open-drain output, or a digital push-pull output though the PIN_CFG and GPIO_CFG registers; see 表 4.

9.2.1.2.1 Digital Input

The digital input functionality can be used to monitor a signal within the system. 图 137 illustrates that the state of the digital input can be read from the GPI_VALUE register.

ADVANCE INFORMATION

Typical Applications (接下页)

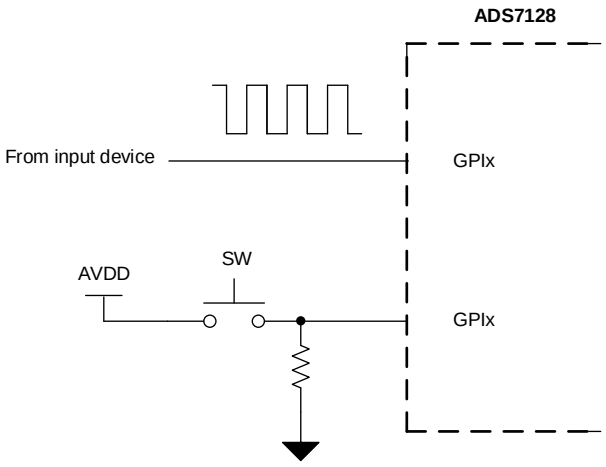

图 137. Digital Input

9.2.1.2.2 Digital Open-Drain Output

The channels of the ADS7128 can be configured as digital open-drain outputs supporting an output voltage up to 5.5 V. An open-drain output, as shown in 图 138, consists of an internal FET (Q) connected to ground. The output is idle when not driven by the device, which means Q is off and the pull-up resistor, R_{PULL_UP}, connects the GPOx node to the desired output voltage. The output voltage can range anywhere up to 5.5 V, depending on the external voltage that the GPIOx is pulled up to. When the device is driving the output, Q turns on, thus connecting the pull-up resistor to ground and bringing the node voltage at GPOx low.

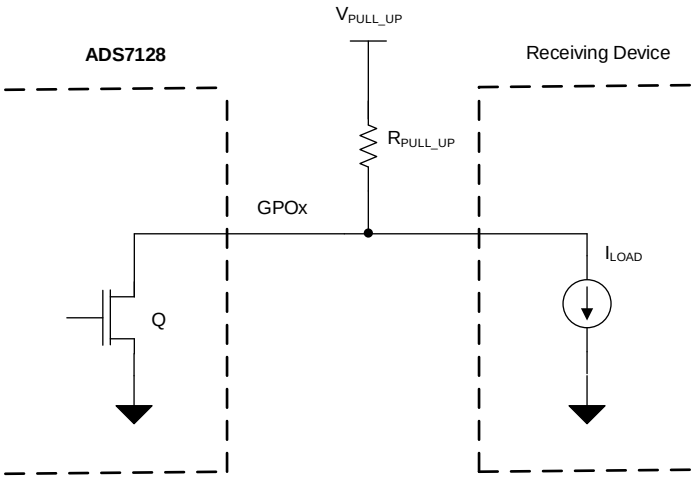

图 138. Digital Open-Drain Output

The minimum value of the pullup resistor, as calculated in 公式 6, is given by the ratio of V_{PULL_UP} and the maximum current supported by the device digital output (5 mA).

$$R_{MIN} = (V_{PULL_UP} / 5\ mA) \quad (6)$$

The maximum value of the pullup resistor, as calculated in 公式 7, depends on the minimum input current requirement, I_{LOAD}, of the receiving device driven by this GPIO.

$$R_{MAX} = (V_{PULL_UP} / I_{LOAD}) \quad (7)$$

Select R_{PULL_UP} such that $R_{MIN} < R_{PULL_UP} < R_{MAX}$.

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Typical Applications (接下页)

9.2.1.3 Digital Push-Pull Output

The channels of the ADS7128 can be configured as digital push-pull outputs supporting an output voltage up to AVDD. As shown in 图 139, a push-pull output consists of two mirrored opposite bipolar transistors, Q1 and Q2. The device can both source and sink current because only one transistor is on at a time (either Q2 is on and pulls the output low, or Q1 is on and sets the output high). A push-pull configuration always drives the line opposed to an open-drain output where the line is left floating.

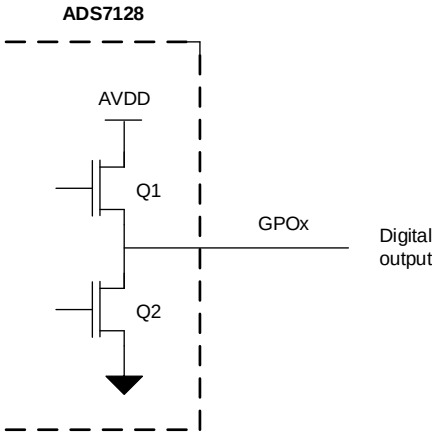

图 139. Digital Push-Pull Output

10 Power Supply Recommendations

10.1 AVDD and DVDD Supply Recommendations

The ADS7128 has two separate power supplies: AVDD and DVDD. The device operates on AVDD; DVDD is used for the interface circuits. For supplies greater than 2.35 V, AVDD and DVDD can be shorted externally if single-supply operation is desired. The AVDD supply also defines the full-scale input range of the device. Decouple the AVDD and DVDD pins individually, as shown in 图 140, with 1-µF ceramic decoupling capacitors. The minimum capacitor value required for AVDD and DVDD is 200 nF and 20 nF, respectively. If both supplies are powered from the same source, a minimum capacitor value of 220 nF is required for decoupling.

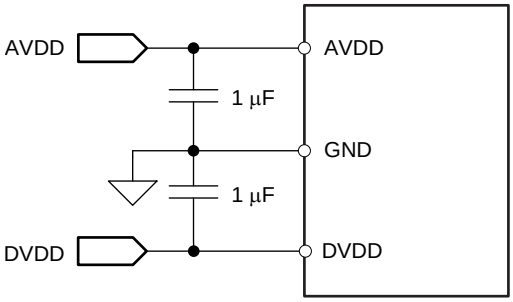

图 140. Power-Supply Decoupling

ADVANCE INFORMATION

11 Layout

11.1 Layout Guidelines

图 141 shows a board layout example for the ADS7128. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the AVDD supply away from noise sources.

Use 1-µF ceramic bypass capacitors in close proximity to the analog (AVDD) and digital (DVDD) power-supply pins. Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors. Connect the GND pin to the ground plane using short, low-impedance paths. The AVDD supply voltage also functions as the reference voltage for the ADS7128. Place the decoupling capacitor (C_{REF}) for AVDD close to the device AVDD and GND pins and connect C_{REF} to the device pins with thick copper tracks.

11.2 Layout Example

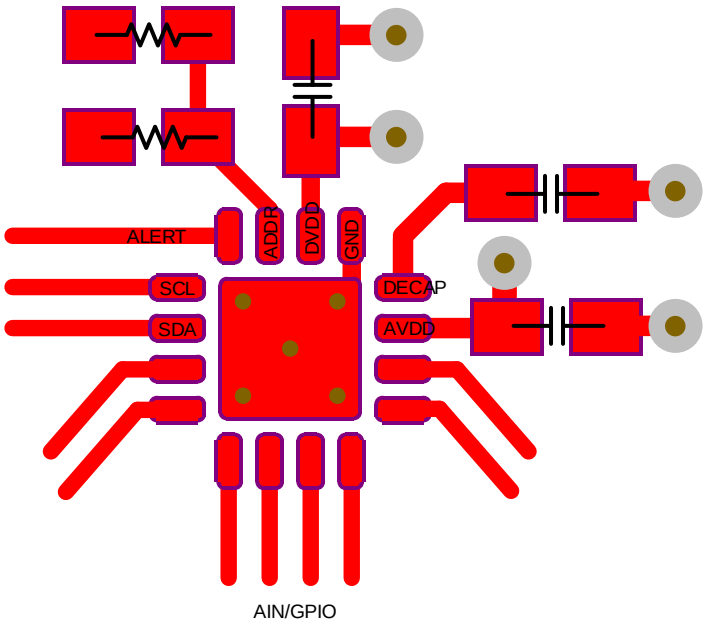

图 141. Example Layout

ADVANCE INFORMATION

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12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS7128IRTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	X71X8
ADS7128IRTER.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	X71X8
ADS7128IRTET	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X71X8
ADS7128IRTET.A	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X71X8

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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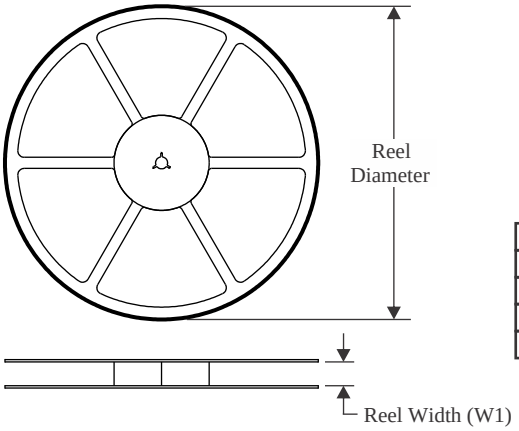
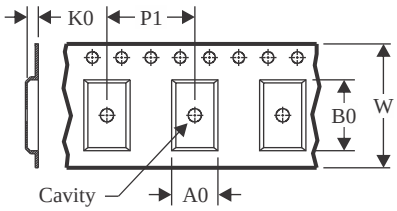
TAPE AND REEL INFORMATION

REEL DIMENSIONS

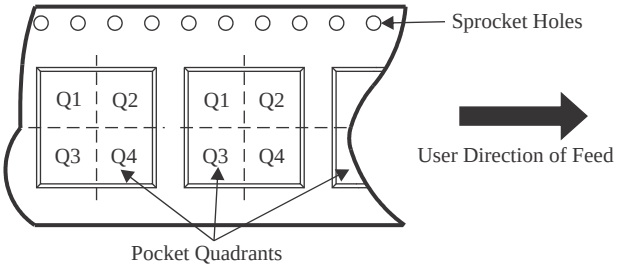


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

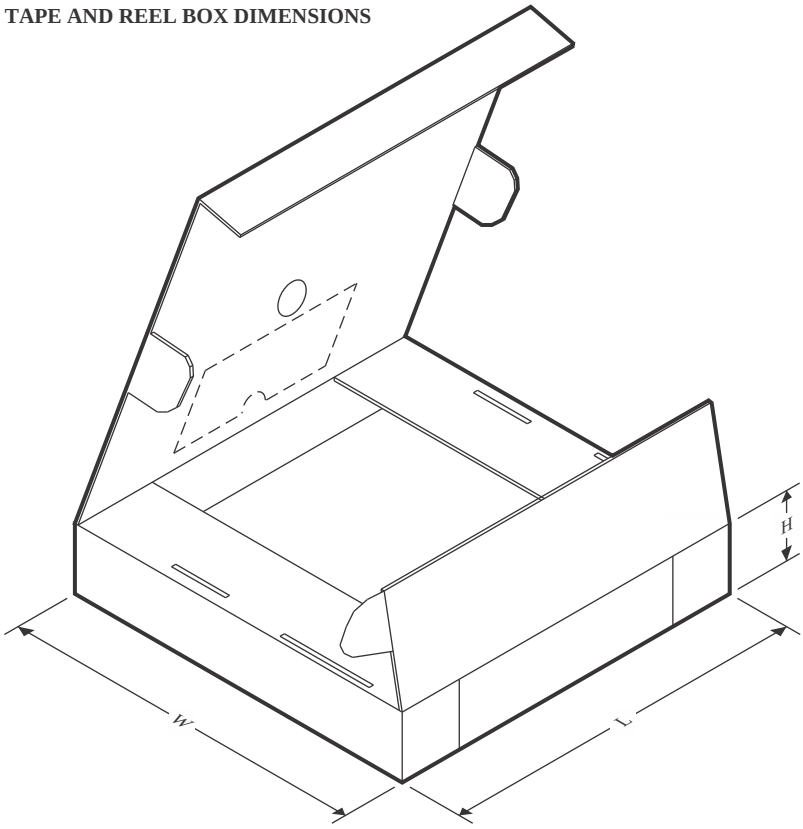
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7128IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7128IRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7128IRTER	WQFN	RTE	16	3000	360.0	360.0	36.0
ADS7128IRTET	WQFN	RTE	16	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

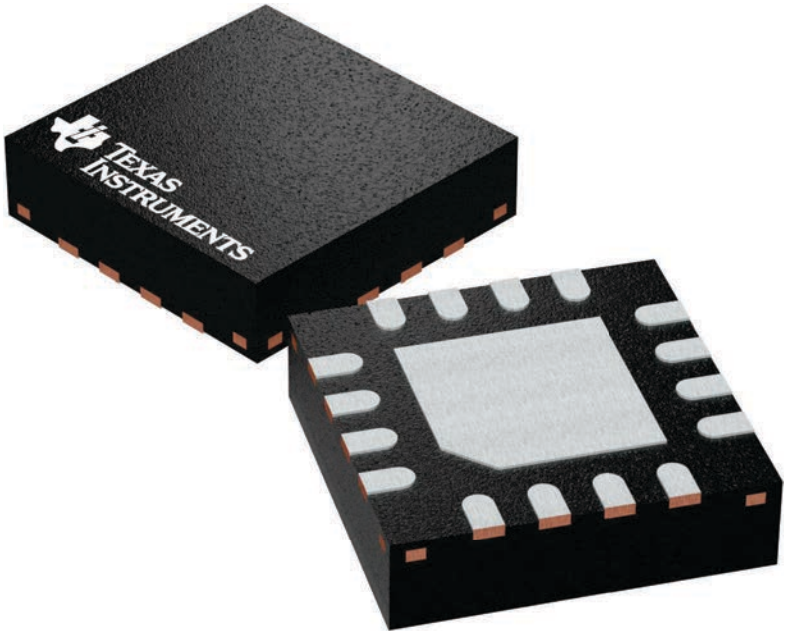
RTE 16

WQFN - 0.8 mm max height

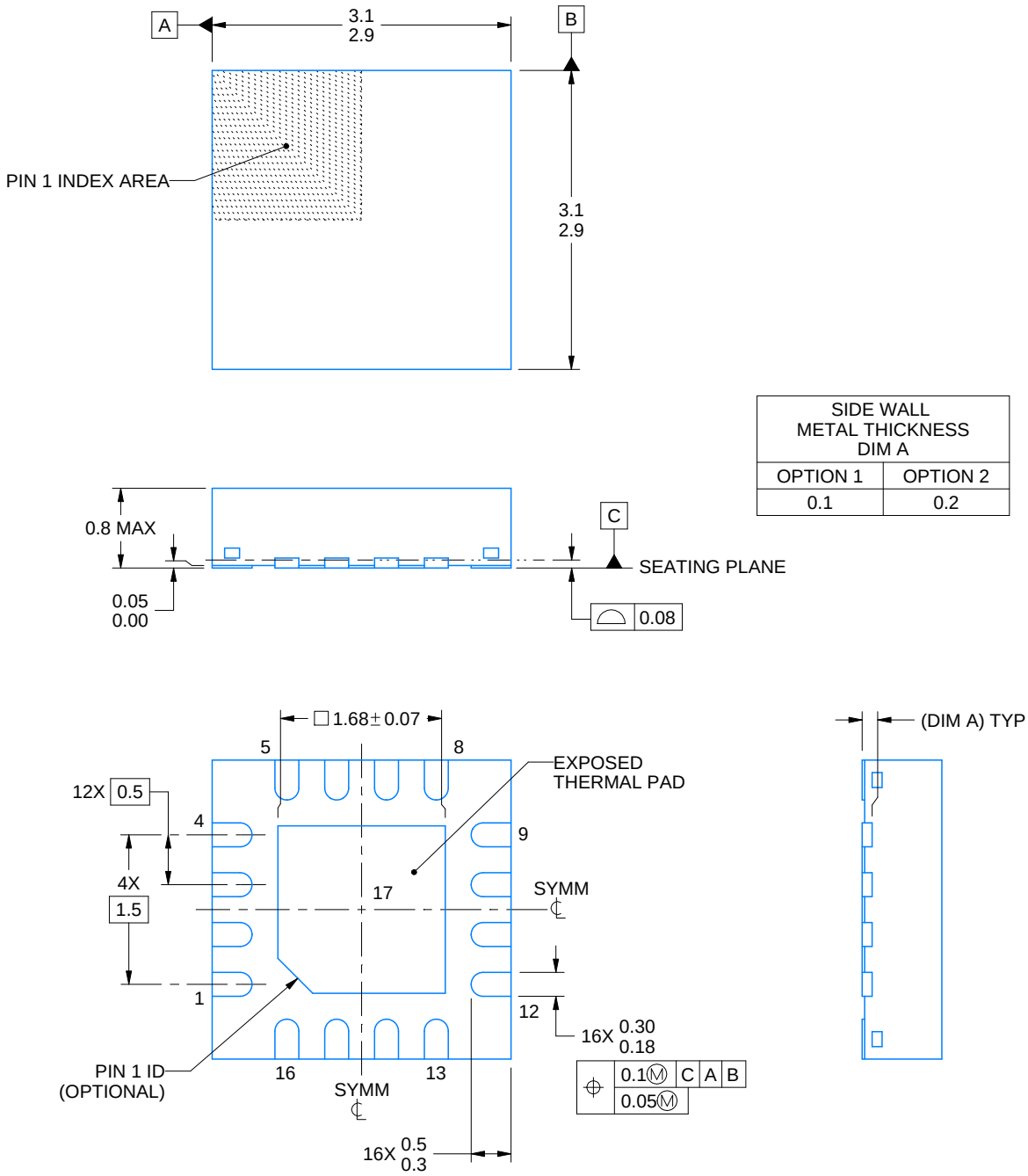
3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



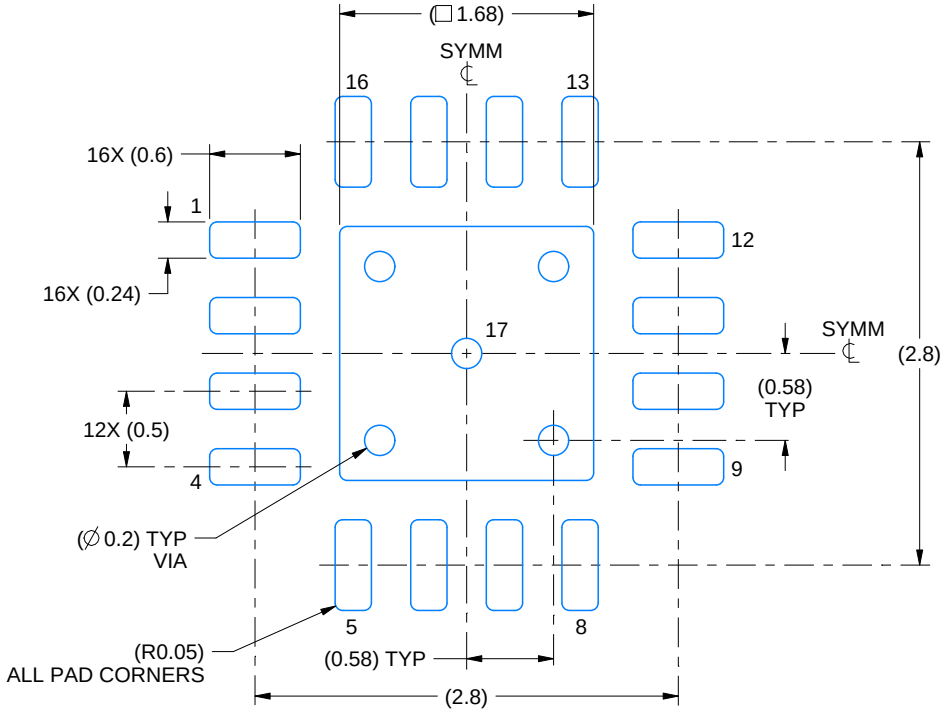
4225944/A



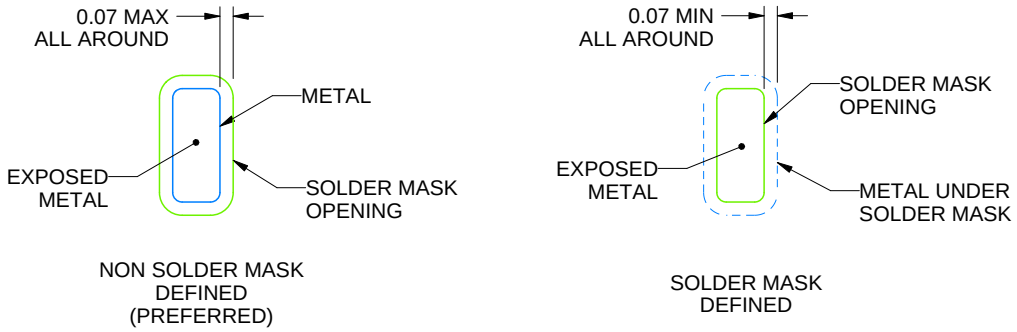
SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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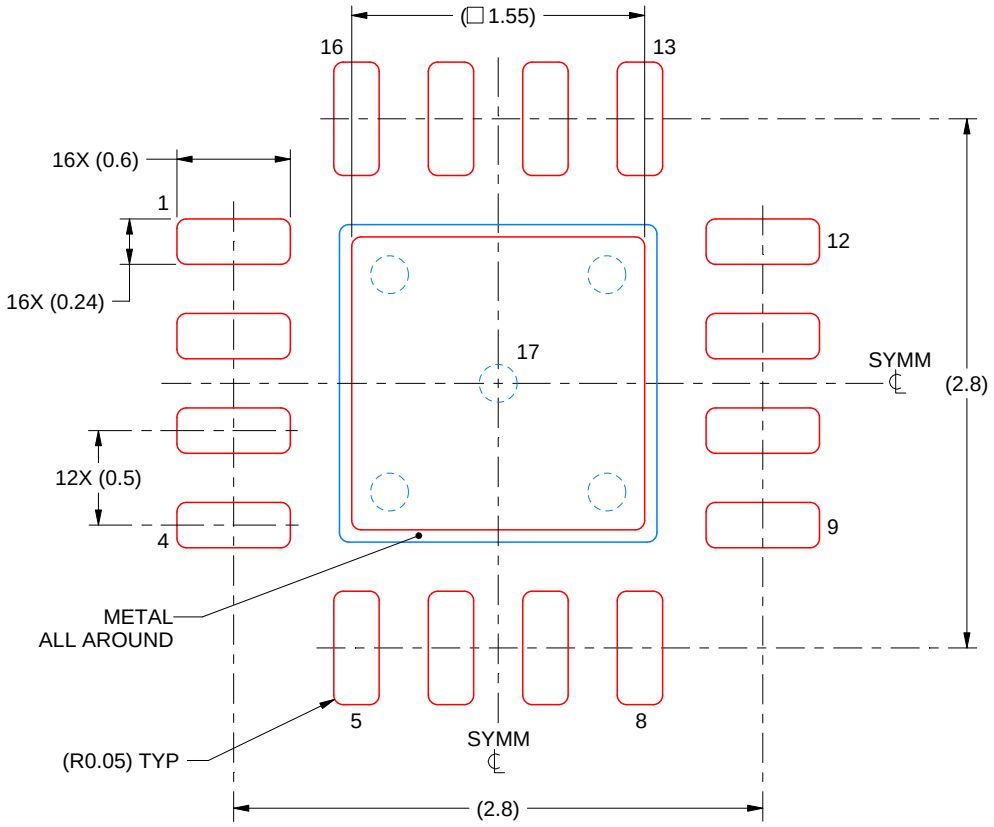
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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