# Dual Channel 11 Bit, 200 MSPS ADC With *SNRBoost*

## FEATURES

- **Maximum Sample Rate: 200 MSPS**
- **11-bit Resolution with No Missing Codes**
- **90 dBc SFDR at Fin = 10 MHz**
- **79.8 dBFS SNR at 125 MHz IF, 20 MHz BW using TI proprietary SNRBoost technology**
- **Total Power 1.1 W at 200 MSPS**
- **90 dB Cross-talk**
- **Double Data Rate (DDR) LVDS and Parallel CMOS Output Options**
- **Programmable Gain up to 6dB for SNR/SFDR Trade-off**
- **DC Offset Correction**
- **Gain Tuning Capability in Fine Steps (0.001 dB) Allows Channel-to-channel Gain Matching**
- **Supports Input Clock Amplitude Down to 400 mV p-p Differential**
- **Internal and External Reference Support**
- **64-QFN Package (9 mm × 9 mm)**

## DESCRIPTION

ADS62C17 is a dual channel 11-bit, 200 MSPS A/D converter that combines high dynamic performance and low power consumption in a compact 64 QFN package. This makes it well-suited for multi-carrier, wide band-width communications applications.

ADS62C17 uses TI-proprietary *SNRBoost* technology that can be used to overcome SNR limitation due to quantization noise for bandwidths less than Nyquist (Fs/2). It includes several useful and commonly used digital functions such as ADC offset correction, gain (0 to 6 dB in steps of 0.5 dB) and gain tuning (in fine steps of 0.001 dB).

The gain option can be used to improve SFDR performance at lower full-scale input ranges. Using the gain tuning capability, each channel's gain can be set independently to improve channel-to-channel gain matching. The device also includes a dc offset correction loop that can be used to cancel the ADC offset.

Both DDR LVDS (Double Data Rate) and parallel CMOS digital output interfaces are available. It includes internal references while the traditional reference pins and associated decoupling capacitors have been eliminated. Nevertheless, the device can also be driven with an external reference.

The device is specified over the industrial temperature range (–40°C to 85°C).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

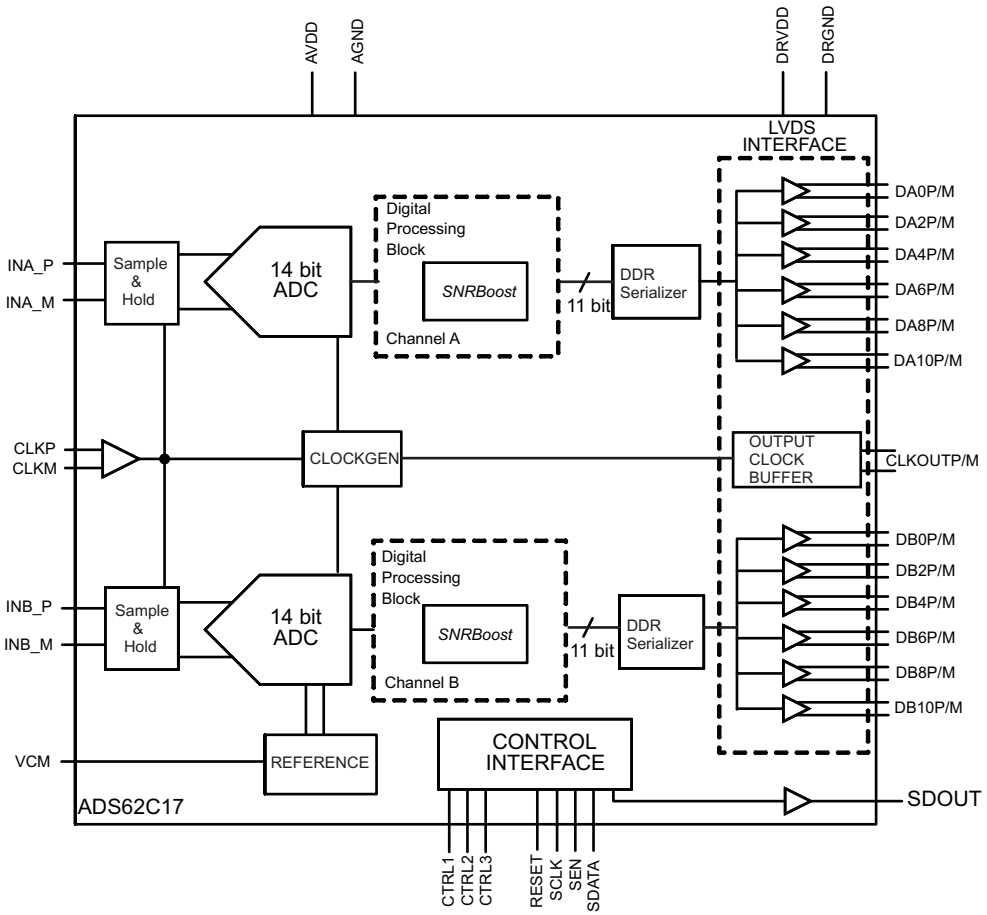



**Figure 1. ADS62C17 Block Diagram**

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|---|---|---|---|---|---|---|
| ADS62C17 | QFN-64 | RGC | –40°C to 85°C | AZ62C17 | ADS62C17IRGCR<br>ADS62C17IRGCT | Tape and Reel |

## THERMAL CHARACTERISTICS(1)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|
| $R_{\theta JA}$(2) | Soldered thermal pad, no airflow | 22 | ° C/W |
| | Soldered thermal pad, 200 LFM | 15 | |
| $R_{\theta JT}$(3) | Bottom of package (thermal pad) | 0.57 | |

(1) With a JEDEC standard high K board and 5x5 via array. See Exposed Pad in the Application Information.
(2) $R_{\theta JA}$ is the thermal resistance from the junction to ambient.
(3) $R_{\theta JT}$ is the thermal resistance from the junction to the thermal pads.

## ABSOLUTE MAXIMUM RATINGS(1)

| | | VALUE | UNIT |
|---|---|---|---|
| | Supply voltage range AVDD | -0.3 to 3.9 | V |
| | Supply voltage range DRVDD | –0.3 to 2.2 | |
| | Voltage between AGND and DRGND | –0.3 to 0.3 | V |
| | Voltage between AVDD to DRVDD (when AVDD leads DRVDD) | 0 to 3.3 | |
| | Voltage between DRVDD to AVDD (when DRVDD leads AVDD) | –1.5 to 1.8 | |
| | Voltage applied to external pin, VCM (in external refersnce mode) | –0.3 to 2.0 | V |
| | Voltage applied to analog input pins – INP_A, INM_A, INP_B, INM_B | –0.3V to minimum (3.6, AVDD + 0.3V) | |
| | Voltage applied to input pins – CLKP, CLKM(2), RESET, SCLK, SDATA, SEN, CTRL1, CTRL2, CTRL3 | –0.3V to ADD + 0.3V | |
| $T_A$ | Operating free-air temperature range | –40 to 85 | °C |
| $T_J$ | Operating junction temperature range | 125 | °C |
| $T_{stg}$ | Storage temperature range | –54 to 150 | °C |
| | ESD, human body model | 2 | kV |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) When AVDD is turned off, it is recommended to switch off the input clock (or ensure the voltage on CLKP, CLKM is < |0.3V|. This prevents the ESD protection diodes at the clock input pins from turning on.

## RECOMMENDED OPERATING CONDITIONS(1)

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **SUPPLIES** | | | | | |
| AVDD | Analog supply voltage | 3.15 | 3.3 | 3.8 | V |
| DRVDD | Digital supply voltage | 1.7 | 1.8 | 1.9 | V |
| **ANALOG INPUTS** | | | | | |
| | Differential input voltage range | | 2 | | $V_{PP}$ |
| | Input common-mode voltage | | 1.5 ± 0.1 | | V |
| | Voltage applied on CM in external reference mode | | 1.5 ± 0.05 | | V |
| | Maximum analog input frequency with 2V pp input amplitude (1) | | 500 | | MHz |
| | Maximum analog input frequency with 1V pp input amplitude (1) | | 800 | | MHz |
| **CLOCK INPUT** | | | | | |
| | Input clock sample rate | 1 | | 200 | MSPS |
| | Input Clock amplitude differential ($V_{CLKP}$– $V_{CLKM}$) | | | | |
| | Sine wave, ac-coupled | 0.2 | 3.0 | | $V_{PP}$ |
| | LVPECL, ac-coupled | | 1.6 | | $V_{PP}$ |
| | LVDS, ac-coupled | | 0.7 | | $V_{PP}$ |
| | LVCMOS, single-ended, ac-coupled | | 3.3 | | V |
| | Input clock duty cycle | 40% | 50% | 60% | |
| **DIGITAL OUTPUTS** | | | | | |
| $C_L$ | Maximum external load capacitance from each output pin to DRGND | | 5 | | pF |
| $R_L$ | Differential external load resistance between the LVDS output (LVDS interface) | | 100 | | Ω |
| $T_A$ | Operating free-air temperature | –40 | | 85 | °C |

(1) See Theory of Operation in the application section.

## ELECTRICAL CHARACTERISTICS[1]

Typical values are at 25°C, AVDD = 3.3V, DRVDD = 1.8V, sampling frequency = 200 MSPS, 50% clock duty cycle, –1dBFS differential analog input, internal reference mode, LVDS and CMOS interfaces unless otherwise noted.
Min and max values are across the full temperature range $T_{MIN}$ = –40°C to $T_{MAX}$ = 85°C, AVDD = 3.3V, DRVDD = 1.8V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Resolution | | | | 11 | bits |
| **ANALOG INPUTS** | | | | | | |
| | Differential input voltage range | | | 2.0 | | $V_{PP}$ |
| | Differential input resistance (at dc) | See Figure 44 | | > 1 | | MΩ |
| | Differential input capacitance | See Figure 45 | | 3.5 | | pF |
| | Analog input bandwidth | | | 700 | | MHz |
| | Analog input common mode current (per channel) | | | 3.6 | | µA/MSPS |
| | VCM common mode voltage output | | | 1.5 | | V |
| | VCM output current capability | | | ±4 | | mA |
| **POWER SUPPLY** | | | | | | |
| IAVDD | Analog supply current | | | 262 | | mA |
| IDRVDD | Output buffer supply current LVDS interface | With 100 Ω external termination | | 120 | | mA |
| IDRVDD | Output buffer supply current CMOS interface | No external load capacitance | | 87 | | mA |
| | Analog power | | | 865 | 1025 | mW |
| | Digital power LVDS interface | | | 216 | 306 | mW |
| | Global power down | | | 45 | 75 | mW |
| | No missing codes | | | Assured | | |
| **DC ACCURACY** | | | | | | |
| DNL | Differential Non-Linearity | Fin = 170 MHz | -0.6 | ±0.2 | 0.6 | LSB |
| INL | Integral Non-Linearity | Fin = 170 MHz | -2.5 | ±0.75 | 2.5 | LSB |
| | Offset Error | | -20 | ±2 | 20 | mV |
| | Offset error temperature coefficient | | | 0.02 | | mV/C |
| | Offset error variation with supply | | | 0.5 | | mV/V |
| There are two sources of gain error – internal reference inaccuracy and channel gain error | | | | | | |
| | Gain error due to internal reference inaccuracy alone | | -1 | ±0.2 | 1 | % FS |
| | Gain error of channel alone[2] | | -1 | +0.2 | 1 | % FS |
| | Channel gain error temperature coefficient | | | 0.002 | | Δ%/°C |
| | Gain matching[3] | Difference in gain errors between two channels within the same device | -2 | | 2 | % FS |
| | | Difference in gain errors between two channels across two devices | -4 | | 4 | |

(1) In CMOS interface, the DRVDD current scales with the sampling frequency and the load capacitance on output pins.
(2) This is specified by design and characterization; it is not tested in production.
(3) For two channels within the same device, only the channel gain error matters, as the reference is common for both channels.

## ELECTRICAL CHARACTERISTICS

Typical values are at 25°C, AVDD = 3.3V, DRVDD = 1.8V, sampling frequency = 200 MSPS, 50% clock duty cycle, –1dBFS differential analog input, internal reference mode, *SNRBoost* disabled, LVDS and CMOS interfaces unless otherwise noted. Min and max values are across the full temperature range $T_{MIN}$ = –40°C to $T_{MAX}$ = 85°C, AVDD = 3.3V, DRVDD = 1.8V

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| SNR<br>Signal to noise ratio<br>LVDS | Fin = 20 MHz | | | 67 | | dBFS |
| | Fin = 70 MHz | | | 66.8 | | |
| | Fin = 170 MHz | 0 dB gain | 64.5 | 66.3 | | |
| | | 6 dB gain | | 64.4 | | |

**Table 1. SNR Enhancement With SNRBoost Enabled**

| ***SNRBoost* bath-tub centered at Fsx0.25, –1 dBFS input applied at Fin = 125MHz, Sampling frequency = 200MSPS** | | | | | | |
|---|---|---|---|---|---|---|
| **Bandwidth, MHz** | **SNR Within Specified bandwidth, dBFS** | | | | | |
| | **In Default Mode (*SNRBoost* Disabled)** | | | **With *SNRBoost* Enabled(1)** | | |
| | **MIN** | **TYP** | **MAX** | **MIN** | **TYP** | **MAX** |
| 5 | 78.8 | 79.6 | | 83 | 85.6 | |
| 10 | 75.8 | 76.6 | | 80 | 82.6 | |
| 15 | 74 | 74.9 | | 78.2 | 80.9 | |
| 20 | 72.7 | 73.6 | | 77 | 79.6 | |
| 30 | 71 | 71.9 | | 74.4 | 76.4 | |
| 40 | 69.8 | 70.6 | | 72.7 | 74.5 | |

(1) Using recommended *SNRBoost* coefficients. See note on *SNRBoost* in application section.

## ELECTRICAL CHARACTERISTICS

Typical values are at 25°C, AVDD = 3.3V, DRVDD = 1.8V, sampling frequency = 200 MSPS, 50% clock duty cycle, –1dBFS differential analog input, internal reference mode, *SNRBoost* disabled, 0dB gain, LVDS and CMOS interfaces unless otherwise noted.

Min and max values are across the full temperature range $T_{MIN}$ = –40°C to $T_{MAX}$ = 85°C, AVDD = 3.3V, DRVDD = 1.8V

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SINAD** Signal to Noise and Distortion Ratio | Fin= 20 MHz | | | 66.9 | | dBFS |
| | Fin = 70 MHz | | | 66.6 | | |
| | Fin = 170 MHz | 0 dB gain | 63.5 | 65.7 | | |
| | | 6 dB gain | | 64.2 | | |
| **SFDR** Spurious Free Dynamic Range | Fin= 20 MHz | | | 85 | | dBc |
| | Fin = 70 MHz | | | 83 | | |
| | Fin = 170 MHz | 0 dB gain | 73 | 78 | | |
| | | 6 dB gain | | 81 | | |
| **THD** Total Harmonic Distortion | Fin= 20 MHz | | | 83 | | dBc |
| | Fin = 70 MHz | | | 81 | | |
| | Fin = 170 MHz | 0 dB gain | 71.5 | 75.5 | | |
| | | 6 dB gain | | 79 | | |
| **HD2** Second Harmonic Distortion | Fin= 20 MHz | | | 94 | | dBc |
| | Fin = 70 MHz | | | 90 | | |
| | Fin = 170 MHz | 0 dB gain | 73 | 83 | | |
| | | 6 dB gain | | 92 | | |
| **HD3** Third Harmonic Distortion | Fin= 20 MHz | | | 85 | | dBc |
| | Fin = 70 MHz | | | 83 | | |
| | Fin = 170 MHz | 0 dB gain | 73 | 78 | | |
| | | 6 dB gain | | 81 | | |
| **Worst Spur** Other than second, third harmonics | Fin= 20 MHz | | | 94 | | dBc |
| | Fin = 70 MHz | | | 92 | | |
| | Fin = 170 MHz | | 80 | 90 | | |
| **IMD** 2-Tone Inter-modulation Distortion | F1 = 185 MHz, F2 = 190 MHz, Each tone at –7 dBFS | | | 87 | | dBFS |
| Input Overload recovery | Recovery to within 1% (of final value) for 6-dB overload with sine wave input at Fclk/4 | | | 1 | | clock cycles |
| Cross-talk | Up to 200 MHz cross-talk frequency | | | 90 | | dB |
| **PSRR** AC Power Supply Rejection Ratio | For 100 mV pp signal on AVDD supply | | | 25 | | dB |

## DIGITAL CHARACTERISTICS — ADS62C17

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD = 3.3V, DRVDD = 1.8V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DIGITAL INPUTS – CTRL1, CTRL2, CTRL3, RESET, SCLK, SDATA, SEN (1)** | | | | | | |
| High-level input voltage | | All digital inputs support 1.8 V and 3.3 V CMOS logic levels. | 1.3 | | | V |
| Low-level input voltage | | | | | 0.4 | V |
| High-level input current | SDATA, SCLK(2) | $V_{HIGH}$ = 3.3 V | | 16 | | µA |
| | SEN(3) | $V_{HIGH}$ = 3.3 V | | 10 | | µA |
| Low-level input current | SDATA, SCLK | $V_{LOW}$ = 0 V | | 0 | | µA |
| | SEN | $V_{LOW}$ = 0 V | | –20 | | µA |
| Input capacitance | | | | 4 | | pF |
| **DIGITAL OUTPUTS – CMOS INTERFACE (DA0-DA10, DB0-DB10, CLKOUT, SDOUT)** | | | | | | |
| High-level output voltage | Ioh = 1mA | | DRVDD – 0.1 | DRVDD | | V |
| Low-level output voltage | Iol = 1mA | | | 0 | 0.1 | V |
| Output capacitance (internal to device) | | | | 2 | | pF |
| **DIGITAL OUTPUTS – LVDS INTERFACE (DA0P/M TO DA10P/M, DB0P/M TO DB10P/M, CLKOUTP/M)** | | | | | | |
| VODH, High-level output differential voltage | | With external 100 Ω termination | +275 | +350 | +425 | mV |
| VODL, Low-level output differential voltage | | With external 100 Ω termination. | –425 | –350 | –275 | mV |
| VOCM, Output common-mode voltage | | | 1.0 | 1.15 | 1.40 | V |
| Output Capacitance | | Capacitance inside the device from each output to ground | | 2 | | pF |

(1) SCLK, SDATA, SEN function as digital input pins in serial configuration mode.
(2) SDATA, SCLK have internal 200 kΩ pull-down resistor
(3) SEN has internal 100 kΩ pull-up resistor to AVDD.

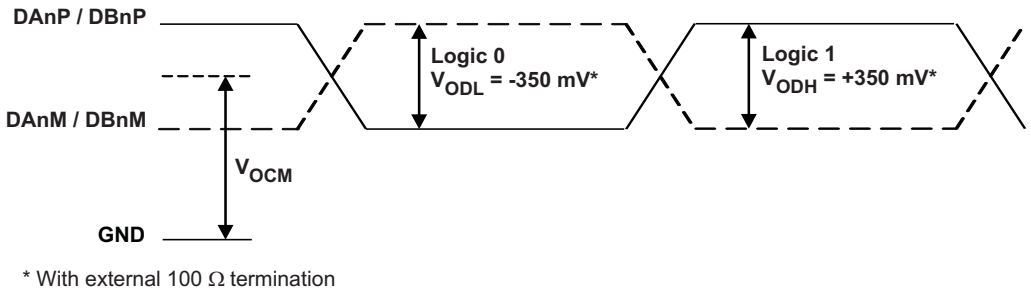



**Figure 2. LVDS Output Voltage Levels**

## TIMING CHARACTERISTICS — LVDS AND CMOS MODES(1)

Typical values are at 25°C, AVDD = 3.3V, DRVDD = 1.8V, sampling frequency = 200 MSPS, sine wave input clock, $C_{LOAD}$ = 5pF(2), $R_{LOAD}$ = 100 Ω(3), no internal termination, LOW SPEED mode disabled, unless otherwise noted.
Min and max values are across the full temperature range $T_{MIN}$ = –40°C to $T_{MAX}$ = 85°C, AVDD = 3.3V, DRVDD = 1.7V to 1.9V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_a$ | Aperture delay | | 0.7 | 1.2 | 1.7 | ns |
| | Aperture delay matching | between two channels of the same device | | ±50 | | ps |
| $t_j$ | Aperture jitter | | | 145 | | fs rms |
| | Wake-up time | Time to valid data after coming out of STANDBY mode | | 1 | 3 | µs |
| | | Time to valid data after coming out of global powerdown | | 20 | 50 | µs |
| | | Time to valid data after stopping and restarting the input clock | | 10 | | Clock cycles |
| | ADC Latency(4) | Default, after reset | | 22 | | Clock cycles |
| **DDR LVDS MODE(5)** | | | | | | |
| $t_{su}$ | Data setup time(6) | Data valid(7) to zero-crossing of CLKOUTP | 0.8 | 1.15 | | ns |
| $t_h$ | Data hold time(7) | Zero-crossing of CLKOUTP to data becoming invalid(7) | 0.8 | 1.15 | | ns |
| $t_{PDI}$ | Clock propagation delay | Input clock falling edge cross-over to output clock rising edge cross-over | $t_{PDI}$ = 0.69×Ts + $t_{delay}$ | | | |
| | $t_{delay}$ | *100 MSPS ≤ Sampling frequency ≤ 200 MSPS*<br>*Ts = 1/Sampling frequency* | 4.2 | 5.7 | 7.2 | ns |
| | $t_{delay}$ skew | Difference in $t_{delay}$ between two devices operating at same temperature & SVDD supply voltage. | | ±500 | | ps |
| | LVDS bit clock duty cycle | Duty cycle of differential clock, (CLKOUTP-CLKOUTM)<br>*100 MSPS ≤ Sampling frequency ≤ 200 MSPS* | | 52% | | |
| $t_{RISE}$, $t_{FALL}$ | Data rise time, Data fall time | Rise time measured from –100 mV to +100 mV<br>Fall time measured from +100 mV to –100 mV<br>*1MSPS ≤ Sampling frequency ≤ 200 MSPS* | | 0.14 | | ns |
| $t_{CLKRISE}$, $t_{CLKFALL}$ | Output clock rise time, Output clock fall time | Rise time measured from –100 mV to +100 mV<br>Fall time measured from +100 mV to –100 mV<br>*1 MSPS ≤ Sampling frequency ≤ 200 MSPS* | | 0.14 | | ns |
| $t_{OE}$ | Output buffer enable to data delay | Time to valid data after output buffer becomes active | | 100 | | ns |
| **PARALLEL CMOS MODE at Fs=200 MSPS(8)** | | | | | | |
| $t_{START}$ | Input clock to data delay | Input clock falling edge cross-over to start of data valid(7) | | | 2.5 | ns |
| $t_{DV}$ | Data valid time | Time interval of valid data(7) | 1.7 | 2.7 | | ns |
| $t_{PDI}$ | Clock propagation delay | Input clock falling edge cross-over to output clock rising edge cross-over | $t_{PDI}$ = 0.28×Ts + $t_{delay}$ | | | |
| | $t_{delay}$ | *100 MSPS ≤ Sampling frequency ≤ 150 MSPS*<br>*Ts = 1/Sampling frequency* | 5.5 | 7.5 | 8.5 | ns |
| | Output clock duty cycle | Duty cycle of output clock, CLKOUT<br>*100 MSPS ≤ Sampling frequency ≤ 150 MSPS* | | 43 | | |
| $t_{RISE}$, $t_{FALL}$ | Data rise time, Data fall time | Rise time measured from 20% to 80% of DRVDD<br>Fall time measured from 80% to 20% of DRVDD<br>*1 ≤ Sampling frequency ≤ 200 MSPS* | | 1.2 | | ns |
| $t_{CLKRISE}$, $t_{CLKFALL}$ | Output clock rise time, Output clock fall time | Rise time measured from 20% to 80% of DRVDD<br>Fall time measured from 80% to 20% of DRVDD<br>*1 ≤ Sampling frequency ≤ 150 MSPS* | | 0.8 | | ns |
| $t_{OE}$ | Output buffer enable (OE) to data delay | Time to valid data after output buffer becomes active | | 100 | | ns |

(1) Timing parameters are ensured by design and characterization and not tested in production.
(2) $C_{LOAD}$ is the effective external single-ended load capacitance between each output pin and ground
(3) $R_{LOAD}$ is the differential load resistance between the LVDS output pair.
(4) At higher frequencies, $t_{PDI}$ is greater than one clock period and overall latency = ADC latency + 1.
(5) Measurements are done with a transmission line of 100Ω characteristic impedance between the device and the load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(6) Data valid refers to LOGIC HIGH of +100.0mV and LOGIC LOW of -100.0mV.
(7) Data valid refers to LOGIC HIGH of 1.26V and LOGIC LOW of 0.54V.
(8) For Fs> 150 MSPS, it is recommended to use external clock for data capture and NOT the device output clock signal (CLKOUT).

**Table 2. LVDS Timings at Lower Sampling Frequencies**

| Sampling Frequency, MSPS | Setup Time, ns | | | Hold Time, ns | | |
|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | TYP | MAX |
| 185 | 0.9 | 1.25 | | 0.85 | 1.25 | |
| 150 | 1.15 | 1.6 | | 1.1 | 1.5 | |
| 125 | 1.6 | 2 | | 1.45 | 1.85 | |
| <100 *Enable LOW SPEED mode* | 2 | | | 2 | | |
| 1 ≤ Fs ≤ 100 *Enable LOW SPEED mode* | | | | $t_{PDI}$, ns | | |
| | | | | MIN | TYP | MAX |
| | | | | | 12.6 | |

**Table 3. CMOS Timings at Lower Sampling Frequencies**

| Sampling Frequency, MSPS | Timings Specified With Respect to Input Clock | | | | | |
|---|---|---|---|---|---|---|
| | $t_{START}$, ns | | | Data Valid Time, ns | | |
| | MIN | TYP | MAX | MIN | TYP | MAX |
| 190 | | | 1.9 | 2 | 3 | |
| 170 | | | 0.9 | 2.7 | 3.7 | |
| 150 | | | 6 | 3.6 | 4.6 | |
| **Sampling Frequency, MSPS** | **Timings Specified With Respect to CLKOUT** | | | | | |
| | **Setup Time, ns** | | | **Hold Time, ns** | | |
| | **MIN** | **TYP** | **MAX** | **MIN** | **TYP** | **MAX** |
| 150 | 2.8 | 4.4 | | 0.5 | 1.2 | |
| 125 | 3.8 | 5.4 | | 0.8 | 1.5 | |
| *<100 Enable LOW SPEED mode* | 5 | | | 1.2 | | |
| 1 ≤ Fs ≤ 100 *Enable LOW SPEED mode* | | | | $t_{PDI}$, ns | | |
| | | | | MIN | TYP | MAX |
| | | | | | 9 | |

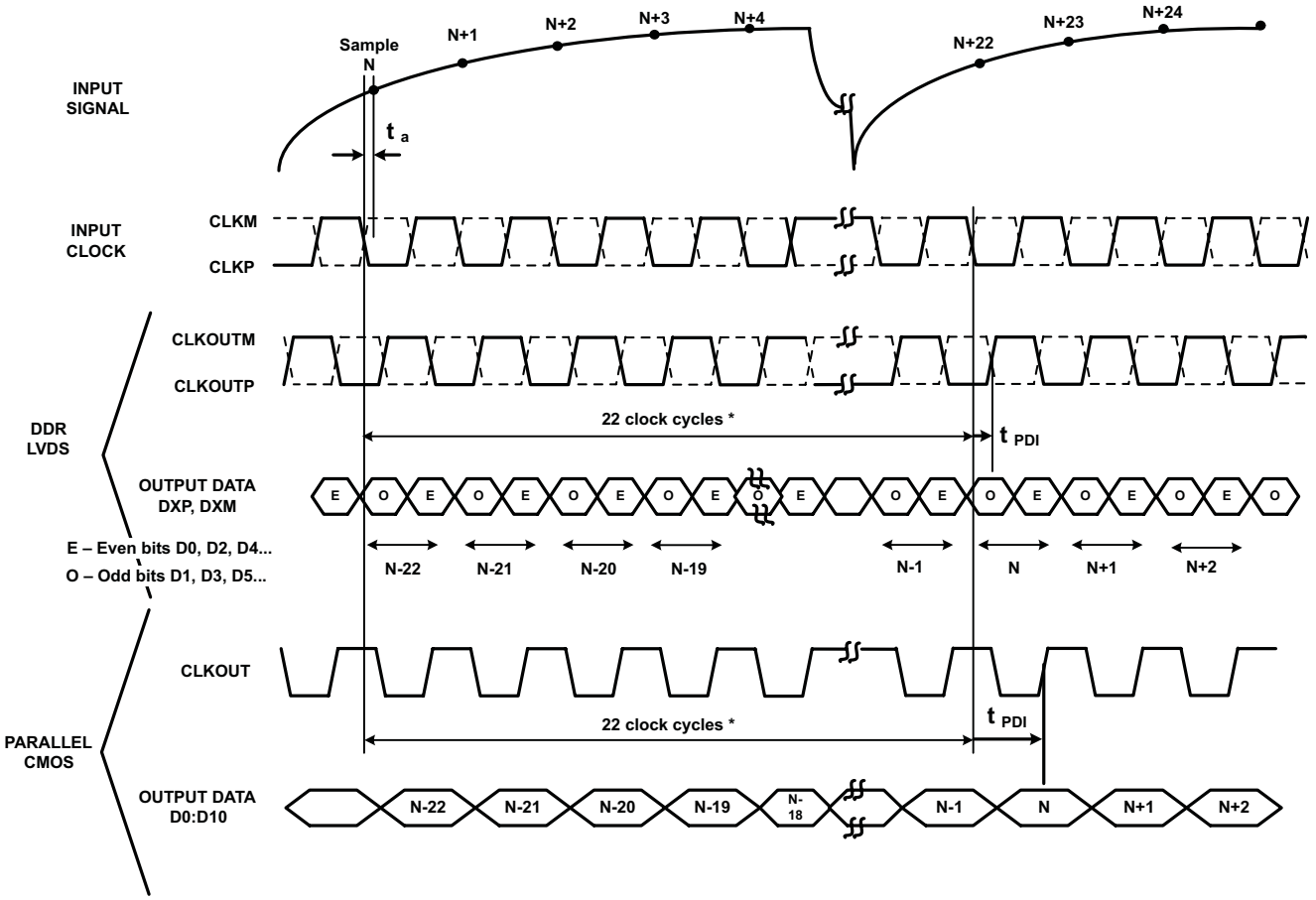
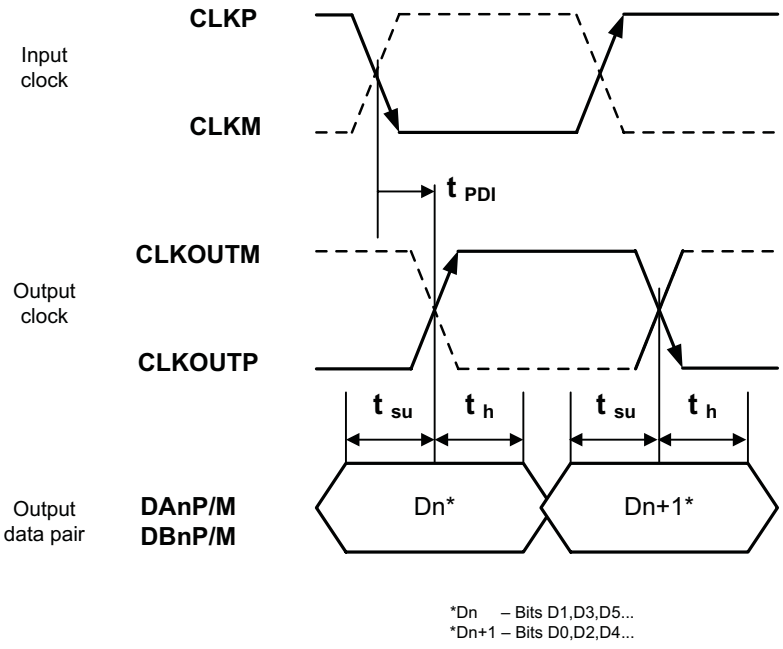
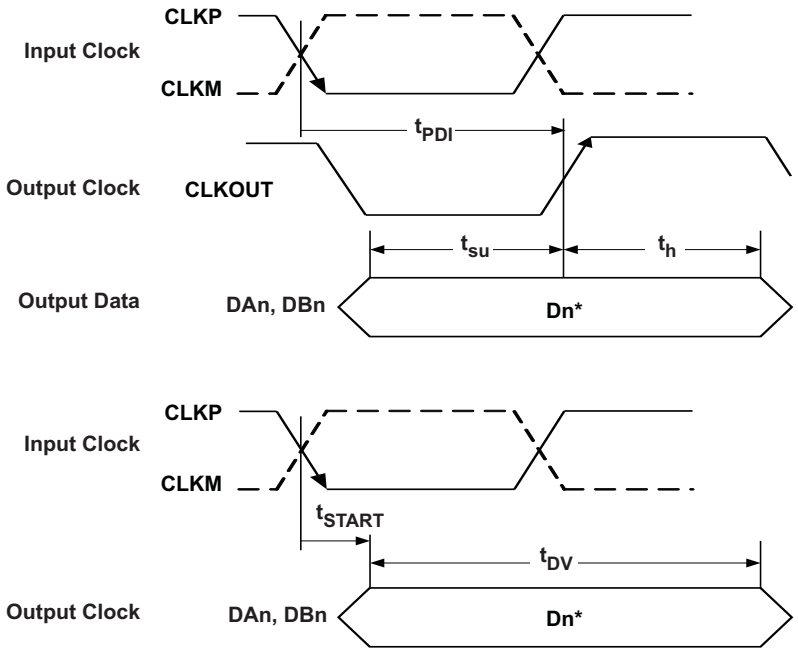



**Figure 3. Latency Diagram**




*Dn – Bits D1,D3,D5...
*Dn+1 – Bits D0,D2,D4...

**Figure 4. LVDS Interface Timing**




*Dn - Bits D0, D1, D2....of channel A and B

**Figure 5. CMOS Interface Timing**

## DEVICE CONFIGURATION

ADS62C17 can be configured independently using either parallel interface control or serial interface programming.

## PARALLEL CONFIGURATION ONLY

To put the device in parallel configuration mode, keep RESET tied to ***high*** (AVDD).

Now, pins SEN, SCLK, CTRL1, CTRL2 and CTRL3 can be used to directly control certain modes of the ADC. The device can be easily configured by connecting the parallel pins to the correct voltage levels (as described in Table 3 to Table 6. There is no need to apply reset and SDATA can be kept low.

In this mode, SEN and SCLK function as parallel interface control pins. Frequently used functions can be controlled in this mode – Power down modes, internal/external reference, selection between LVDS/CMOS interface and output data format.

Table 4 has a brief description of the modes controlled by the four parallel pins.

**Table 4. PARALLEL PIN DEFINITION**

| PIN | | CONTROLS MODES |
|---|---|---|
| SCLK | Analog control pins (controlled by analog voltage level, see Figure 5 | Internal or External reference |
| SEN | | LVDS/CMOS interface and Output Data Format |
| CTRL1 | Digital control pints (controlled by digital logic levels) | Control SNRBoost, Standby and MUX mode. |
| CTRL2 | | |
| CTRL3 | | |

## SERIAL INTERFACE CONFIGURATION ONLY

To exercise this mode, first the serial registers have to be reset to their default values and RESET pin has to be kept ***low***.

SEN, SDATA and SCLK function as serial interface pins in this mode and can be used to access the internal registers of the ADC.

The registers can be reset either by applying a pulse on RESET pin or by setting the **<RESET>** bit ***high***. The serial interface section describes the register programming and register reset in more detail.

## USING BOTH SERIAL INTERFACE and PARALLEL CONTROLLS

For increased flexibility, a combination of serial interface registers and parallel pin controls (CTRL1 to CTRL3) can also be used to configure the device. To allow this, keep RESET low. The parallel interface control pins CTRL1 to CTRL3 are available. After power-up, the device will automatically get configured as per the voltage settings on these pins (Table 6). SEN, SDATA, and SCLK function as serial interface digital pins and are used to access the internal registers of ADC. The registers must first be reset to their default values either by applying a pulse on RESET pin or by setting bit <RST> = 1. After reset, the RESET pin must be kept low. The serial interface section describes the register programming and register reset in more detail.

## DETAILS OF PARALLEL CONFIGURATION ONLY

The functions controlled by each parallel pin are described below. A simple way of configuring the parallel pins is shown in Figure 6.

**Table 5. SCLK Control Pin**

| SCLK | DESCRIPTION |
|---|---|
| 0<br>+200mV/-0mV | Internal reference |
| (3/8)AVDD<br>±200mV | External reference |
| (5/8)2AVDD<br>±200mV | External reference |
| AVDD<br>+0mV/-200mV | Internal reference |

**Table 6. SEN Control Pin**

| SEN | DESCRIPTION |
|---|---|
| 0<br>+200mV/-0mV | Offset binary and DDR LVDS output |
| (3/8)AVDD<br>±200mV | 2's complement format and DDR LVDS output |
| (5/8)2AVDD<br>±200mV | 2's complement format and parallel CMOS output |
| AVDD<br>+0mV/-200mV | Offset binary and parallel CMOS output |

**Table 7. CTRL1, CTRL2 and CTRL3 Pins**

| CTRL1 | CTRL2 | CTRL3 | DESCRIPTION |
|---|---|---|---|
| LOW | LOW | LOW | Normal operation |
| LOW | LOW | HIGH | SNRBoost enabled for Channel B(1) |
| LOW | HIGH | LOW | SNRBoost enabled for Channel A(1) |
| LOW | HIGH | HIGH | SNRBoost enabled for Channel A and B(1) |
| HIGH | LOW | LOW | Global power down |
| HIGH | LOW | HIGH | Channel B standby |

(1) To enable & disable SNRBoost mode using the CTRL pins, reset the register bits <SNRBoost Enable - CHA> = 0 & <SNRBoost Enable - CHB> = 0.

**Table 7. CTRL1, CTRL2 and CTRL3 Pins (continued)**

| CTRL1 | CTRL2 | CTRL3 | DESCRIPTION |
|---|---|---|---|
| HIGH | HIGH | LOW | Channel A standby |
| HIGH | HIGH | HIGH | MUX mode of operation, Channel A and B data is multiplexed and output on DA10 to DA0 pins. |

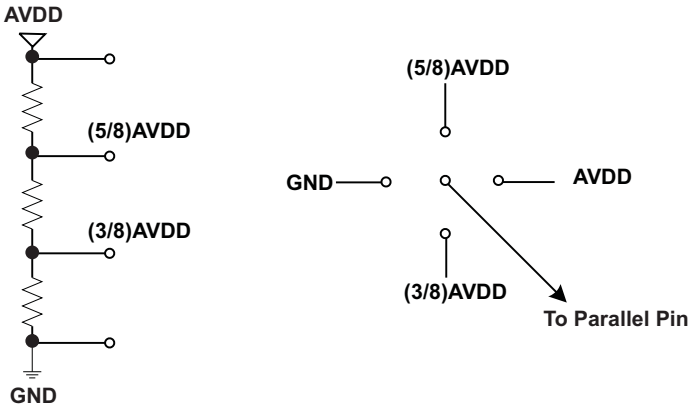



**Figure 6. Simple Scheme to Configure Parallel Pins**

## SERIAL INTERFACE

The ADC has a set of internal registers, which can be accessed by the serial interface formed by pins SEN (Serial interface Enable), SCLK (Serial Interface Clock) and SDATA (Serial Interface Data).

Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA is latched at every falling edge of SCLK when SEN is active (low). The serial data is loaded into the register at every 16$^{th}$ SCLK falling edge when SEN is low. In case the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiple of 16-bit words within a single active SEN pulse.

The first 8 bits form the register address and the remaining 8 bits are the register data. The interface can work with SCLK frequency from 20 MHz down to very low speeds (few Hertz) and also with non-50% SCLK duty cycle.

### Register Initialization (when using serial interface only)

After power-up, the internal registers MUST be initialized to their default values. This can be done in one of two ways:

1. Either through hardware reset by applying a high-going pulse on RESET pin (of width greater than 10 ns) as shown in Figure 7

   OR

2. By applying software reset. Using the serial interface, set the **<RESET>** bit (D7 in register 0x00) to HIGH. This initializes internal registers to their default values and then self-resets the **<RESET>** bit to ***low***. In this case the RESET pin is kept ***low***.

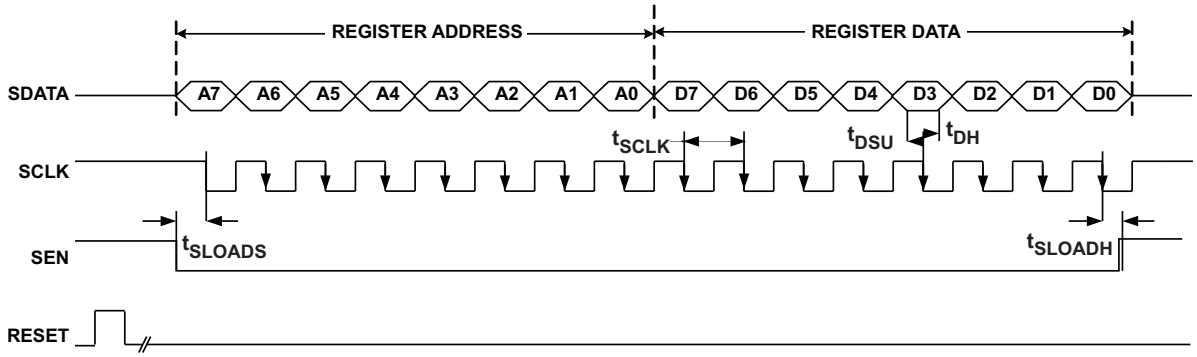



**Figure 7. Serial Interface Timing**

## SERIAL INTERFACE TIMING CHARACTERISTICS

Typical values at 25°C, min and max values across the full temperature range $T_{MIN}$ = –40C to $T_{MAX}$ = 85°C, AVDD = 3.3V, DRVDD = 1.8V, unless otherwise noted.

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{SCLK}$ | SCLK frequency (= 1/ $t_{SCLK}$) | >DC | | 20 | MHz |
| $t_{SLOADS}$ | SEN to SCLK setup time | 25 | | | ns |
| $t_{SLOADH}$ | SCLK to SEN hold time | 25 | | | ns |
| $t_{DS}$ | SDATA setup time | 25 | | | ns |
| $t_{DH}$ | SDATA hold time | 25 | | | ns |

### Serial Register Readout

The device includes an option where the contents of the internal registers can be read back. This may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

a. First, set register bit <SERIAL READOUT> = 1 to put the device in serial readout mode. This disables any further writes into the registers, EXCEPT the register at address 0. Note that the <SERIAL READOUT> bit is also located in register 0. The device can exit readout mode by writing <SERIAL READOUT> to 0. Also, only contents of register at adress 0 cannot be read in the register readout mode.

b. Initiate a serial interface cycle specifying the address of the register (A7–A0) whose content has to be read.

c. The device outputs the contents (D7–D0) of the selected register on the SDOUT pin.

d. The external controller can latch the contents at the falling edge of SCLK.

e. To exit the serial readout mode, reset register bit <SERIAL READOUT> = 0, which enables writes into all registers of the device.

The serial register readout works with both CMOS and LVDS interfaces.

When <SERIAL READOUT> is disabled, SDOUT pin is forced low by the device (and not put in high-impedance). If serial readout is not used, SDOUT pin has to be floated.

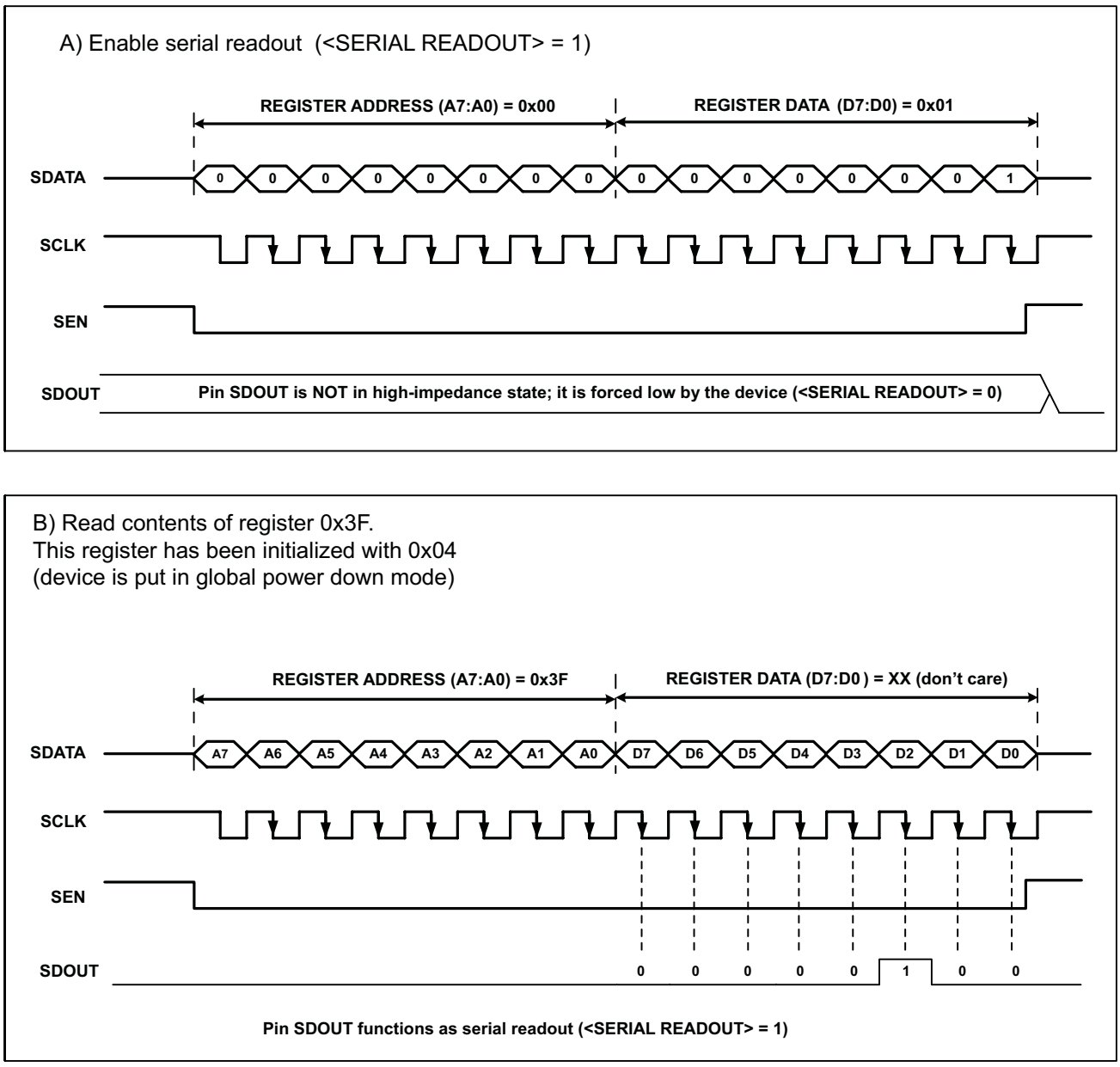


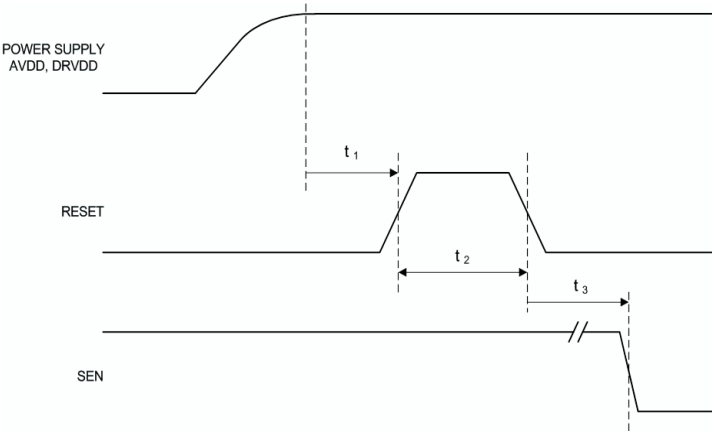

**Figure 8. Serial Readout**

## RESET TIMING (WHEN USING SERIAL INTERFACE ONLY)

Typical values at 25°C, min and max values across the full temperature range $T_{MIN}$ = –40°C to $T_{MAX}$ = 85°C, unless otherwise noted.

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_1$ | Power-on delay | Delay from power-up of AVDD and DRVDD to RESET pulse active | 1 | | | ns |
| $t_2$ | Reset pulse width | Pulse width of active RESET signal | 10 | | | ns |
| | | | | | 1 (1) | µs |
| $t_3$ | Register write delay | Delay from RESET disable to SEN active | 100 | | | ns |

(1) The reset pulse is needed only when using the serial interface configuration. If the pulse width is greater than 1usec, the device could enter the parallel configuration mode briefly and then return back to serial interface mode.




NOTE: A high-going pulse on RESET pin is required in serial interface mode in case of initialization through hardware reset. For parallel interface operation, RESET has to be tied permanently HIGH.

**Figure 9. Reset Timing Diagram**

## SERIAL REGISTER MAP

**Table 8. Summary of Functions Supported by Serial Interface(1)**

| REGISTER ADDRESS | REGISTER FUNCTIONS | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **A7 - A0 IN HEX** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| 00 | **<RESET>** *Software Reset* | 0 | 0 | 0 | 0 | 0 | 0 | **<SERIAL READOUT>** |
| 20 | 0 | 0 | 0 | 0 | 0 | **<ENABLE LOW SPEED mode>** | 0 | 0 |
| 3F | 0 | **<REF>** *Internal or external reference* | | 0 | 0 | 0 | **<STAND BY>** | 0 |
| 40 | 0 | 0 | 0 | 0 | **<POWER DOWN MODES>** | | | |
| 41 | **<LVDS CMOS>** *Output interface* | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 44 | **<CLKOUT EDGE CONTROL>** | | | | | | 0 | 0 |
| 50 | 0 | **<ENABLE INDEPENDENT CHANNEL CONTROL>** | 0 | 0 | 0 | **<DATA FORMAT>** *2s comp or offset binary* | | 0 |
| 51 | **<CUSTOM PATTERN LOW>** | | | | | 0 | 0 | 0 |
| 52 | 0 | 0 | **<CUSTOM PATTERN HIGH>** | | | | | |
| 53 | 0 | **<OFFSET CORRECTION ENABLE – Common/Ch A>** | 0 | | | | | |
| 55 | **<GAIN PROGRAMMABILITY – Common/Ch A>** *0 to 6 dB in 0.5 dB steps* | | | | **<OFFSET CORRECTION TIME CONSTANT – Common/ Ch A >** | | | |
| 56 | **<*SNRBoost Coeff 1* – Common/ Ch A >** | | | | **<*SNRBoost Coeff 2* – Common/ Ch A >** | | | |
| 57 | 0 | **<FINE GAIN ADJUST – Common/ Ch A >** *+0.001 dB to +0.134 dB, in 128 steps* | | | | | | |
| 59 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **<*SNRBoost Enable* – Common/ Ch A >** |
| 62 | 0 | 0 | 0 | 0 | 0 | **<TEST PATTERNS - Common/ Ch A >** | | |
| 63 | 0 | 0 | **<OFFSET PEDESTAL – Common/ Ch A >** | | | | | |
| 66 | 0 | **<OFFSET CORRECTION ENABLE– Ch B>** | 0 | 0 | 0 | 0 | 0 | 0 |
| 68 | **<GAIN PROGRAMMABILITY – Ch B>** *0 to 6 dB in 0.5 dB steps* | | | | **<OFFSET CORRECTION TIME CONSTANT – Ch B>** | | | |
| 69 | **<*SNRBoost Coeff 1 – Ch B*>** | | | | **<*SNRBoost Coeff 2 – Ch B*>** | | | |
| 6A | 0 | **<FINE GAIN ADJUST – Ch B>** *+0.001 dB to +0.134 dB, in 128 steps* | | | | | | |
| 6C | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **<*SNRBoost Enable – Ch B*>** |
| 75 | 0 | 0 | 0 | 0 | 0 | **<TEST PATTERNS - Ch B>** | | |
| 76 | 0 | 0 | **<OFFSET PEDESTAL – Ch B>** | | | | | |

(1) Multiple functions in a register can be programmed in a single write operation.

## DESCRIPTION OF SERIAL REGISTERS

| A7 – A0 IN HEX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 00 | <RESET> *Software Reset* | 0 | 0 | 0 | 0 | 0 | 0 | <SERIAL READOUT> |

**D7 <RESET>**

1 Software reset applied – resets all internal registers and self-clears to 0.

**D0 <SERIAL READOUT>**

0 Serial readout disabled. SDOUT is forced high or low by the device (and not out in high impedance state).

1 Serial readout enabled, Pin SDOUT functions as serial data readout. This mode is available only with CMOS output interface. With LVDS interface, pin 56 becomes CLKOUTM.

| A7 – A0 IN HEX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 20 | 0 | 0 | 0 | 0 | 0 | <ENABLE LOW SPEED MODE> | 0 | 0 |

**D2 <ENABLE LOW SPEED MODE>**

0 LOW SPEED mode disabled. Use for sampling frequency > 100 MSPS.

1 Enable LOW SPEED mode for sampling frequencies <= 100 MSPS.

| A7 – A0 IN HEX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 3F | 0 | <REF> | | 0 | 0 | 0 | <STANDBY> | 0 |

**D6-D5 <REF> Internal or external reference selection**

01 Internal reference enabled

11 External reference enabled

**D1 <STANDBY>**

0 Normal operation

1 ADC is powered down for both channels. Internal references, output buffers are active. This results in quick wake-up time from standby.

| A7 – A0 IN HEX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 40 | 0 | 0 | 0 | 0 | POWER DOWN MODES | | | |

**D3-D0 <POWER DOWN MODES>**

0000 Pins CTRL1, CTRL2 & CTRL3 determine power down modes.

1000 Normal operation

1001 Output buffer disabled for channel B

1010 Output buffer disabled for channel A

1011 Output buffer disabled for channel A and B

1100 Global power down

1101 Channel B standby

1110 Channel A standby

1111 Multiplexed mode, **MUX–** (only with CMOS interface)
Channel A and B data is multiplexed and output on DA10 to DA0 pins.

| A7 – A0 IN HEX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 41 | <LVDS CMOS> | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**D7 <LVDS CMOS>**

0 Parallel CMOS interface

1 DDR LVDS interface

| A7 – A0 IN HEX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 44 | <CLKOUT EDGE CONTROL><br>*Output clock edge control* | | | | | | 0 | 0 |

**LVDS Interface**

**D7-D5 <CLKOUT POSN> Output clock rising edge position**

000, 100 Default output clock position (refer to timing specification table)

101 Rising edge shifted by + (4/26)Ts

110 Rising edge aligned with data transition

111 Rising edge shifted by – (4/26)Ts

**D4-D2 <CLKOUT POSN> Output clock falling edge position**

000, 100 Default output clock position (refer to timing specification table)

101 Falling edge shifted by + (4/26)Ts

110 Falling edge aligned with data transition

111 Falling edge shifted by – (4/26)Ts

**CMOS INterface**

**D7-D5 <CLKOUT POSN> Output clock rising edge position**

000, 100 Default output clock position (refer to timing specification table)

101 Rising edge shifted by + (4/26)Ts

110 Rising edge shifted by – (6/26)Ts

111 Rising edge shifted by – (4/26)Ts

**D4-D2 <CLKOUT POSN> Output clock falling edge position**

000, 100 Default output clock position (refer to timing specification table)

101 Falling edge shifted by + (4/26)Ts

110 Falling edge shifted by – (6/26)Ts

111 Falling edge shifted by – (4/26)Ts

| A7 – A0 IN HEX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 50 | 0 | <ENABLE INDEPENDENT CHANNEL CONTROL> | 0 | 0 | 0 | <DATA FORMAT><br>*2s complement or offset binary* 0 | | 0 |

**D6 <ENABLE INDEPENDENT CHANNEL CONTROL>**

0 ***Common control*** – both channels use common control settings for test patterns, offset correction, gain, gain correction and SNRBoost functions. These settings can be specified in a single set of registers.

1 ***Independent control*** – both channels can be programmed with independent control settings for test patterns, offset correction and SNRBoost functions. Separate registers are available for each channel.

**D2-D1 <DATA FORMAT>**

10 2s complement

11 Offset binary

| A7 – A0 IN HEX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 51 | <Custom Pattern Low> | | | | | 0 | 0 | 0 |
| 52 | 0 | 0 | <Custom Pattern High> | | | | | |

**D7-D3 <CUSTOM LOW>**

5 lower bits of custom pattern available at the output instead of ADC data

**D5-D0 <CUSTOM HIGH>**

6 upper bits of custom pattern available at the output instead of ADC data

| A7 – A0 IN HEX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 53 | 0 | <OFFSET CORRECTION ENABLE – Common/Ch A><br>*Offset correction enable* | 0 | 0 | 0 | 0 | 0 | 0 |

**D6 <OFFSET CORRECTION ENABLE – Common/Ch A>**

Offset correction enable control for both channels (*with common control*) or for channel A only (*with independent control*).

0 Offset correction disabled

1 Offset correction enabled

See Offset Correction

| A7 – A0 IN HEX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 55 | <GAIN PROGRAMMABILITY – Common/Ch A> | | | | <OFFSET CORR TIME CONSTANT – Common/Ch A><br>*Offset correction time constant* | | | |

**D7-D4 <GAIN PROGRAMMABILITY – Common/Ch A>**

Gain control for both channels (with common control) or for channel A only (with independent control).

0000 0 dB gain, default after reset
0001 0.5 dB gain
0010 1.0 dB gain
0011 1.5 dB gain
0100 2.0 dB gain
0101 2.5 dB gain
0110 3.0 dB gain
0111 3.5 dB gain
1000 4.0 dB gain
1001 4.5 dB gain
1010 5.0 dB gain
1011 5.5 dB gain
1100 6.0 dB gain

**D3-D0 <OFFSET CORR TIME CONSTANT – Common/Ch A>**

Correction loop time constant in number of clock cycles.

Applies to both channels (with common control) or for channel A only (with independent control).

0000 256 k
0001 512 k
0010 1 M
0011 2 M
0100 4 M
0101 8 M
0110 16 M
0111 32 M
1000 64 M
1001 128 M
1010 256 M
1011 512 M

| A7 – A0 IN HEX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 56 | *<SNRBoost Coeff 1 – Common/CH A>* | | | | *<SNRBoost Coeff 2 – Common/CH A>* | | | |

See SNR enhancement using SNRBoost

| A7 – A0 IN HEX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 57 | 0 | **<FINE GAIN ADJUST – Common/Ch A>** *+0.001 dB to +0.134 dB, in 128 steps* | | | | | | |

Using the FINE GAIN ADJUST register bits, the channel gain can be trimmed in fine steps. The trim is only additive, has 128 steps & a range of 0.134dB. The relation between the FINE GAIN ADJUST bits & the trimmed channel gain is:

Δ Channel Gain = 20 × log10[1 + (FINE GAIN ADJUST/8192)]

Note that the total device gain = ADC gain + Δ Channel gain. The ADC gain is determined by register bits <**GAIN PROGRAMMABILITY**>

| A7 – A0 IN HEX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 59 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ***<SNRBoost Enable – CH A>*** |

**D0** ***<SNRBoost Enable – CH A>***

SNRBoost control for both channels (*with common control*) or for channel A only (*with independent control*).

0 SNRBoost disabled

1 SNRBoost enabled

| A7 – A0 IN HEX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 62 | 0 | 0 | 0 | 0 | 0 | **<TEST PATTERNS>** | | |

**D2-D0** **<TEST PATTERNS>** Test Patterns to verify data capture.

Applies to both channels (*with common control*) for channel A only (*with independent control*)

000 Normal operation

001 Outputs all zeros

010 Outputs all ones

011 Outputs toggle pattern
Output data <D10:D0> alternates between 01010101010 and 10101010101 every clock cycle.

100 Outputs digital ramp
Output data increments by one LSB (12-bit) every 8th clock cycle from code 0 to code 2047.

101 Outputs custom pattern (use registers 0x51, 0x52 for setting the custom pattern)

110 Unused

111 Unused

| A7 – A0 IN HEX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 63 | 0 | 0 | <OFFSET PEDESTAL – Common/Ch A> | | | | | |

**D5-D0 <OFFSET PEDESTAL – Common/Ch A>**

When the offset correction is enabled, the final converged value after the offset is corrected will be the ADC mid-code value. A pedestal can be added to the final converged value by programming these bits. See "Offset Correction" in application section.

Applies to both channels (*with common control*) or for channel A only (*with independent control*).

011111 PEDESTAL = 31 LSB

011110 PEDESTAL = 30 LSB

011101 PEDESTAL = 29 LSB

....

000000 PEDESTAL = 0 LSB

....

111111 PEDESTAL = –1 LSB

111110 PEDESTAL = –2 LSB

....

100000 PEDESTAL = –32LSB

| A7 – A0 IN HEX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 66 | 0 | <OFFSET CORRECTION ENABLE – CH B><br>*Offset correction enable* | 0 | 0 | 0 | 0 | 0 | 0 |

**D6 <OFFSET CORRECTION ENABLE – CH B>**

Offset correction enable control for channel B (*only with independent control*).

0 offset correction disabled

1 offset correction enabled

| A7 – A0 IN HEX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 68 | <GAIN PROGRAMMABILITY – CH B> | | | | <OFFSET CORR TIME CONSTANT – CH B><br>*Offset correction time constant* | | | |

**D7-D4** **<GAIN – CH B>** Gain programmability in 0.5 dB steps

Applies to channel B (*only with independent control*).

0000 0 dB gain, default after reset

0001 0.5 dB gain

0010 1.0 dB gain

0011 1.5 dB gain

0100 2.0 dB gain

0101 2.5 dB gain

0110 3.0 dB gain

0111 3.5 dB gain

1000 4.0 dB gain

1001 4.5 dB gain

1010 5.0 dB gain

1011 5.5 dB gain

1100 6.0 dB gain

**D3-D0** **<OFFSET CORR TIME CONSTANT – CH B>** Time constant of correction loop in number of clock cycles.

Applies to channel B (*only with independent control*)

0000 256 k

0001 512 k

0010 1 M

0011 2 M

0100 4 M

0101 8 M

0110 16 M

0111 32 M

1000 64 M

1001 128 M

1010 256 M

1011 512 M

| A7 – A0 IN HEX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 69 | *<SNRBoost Coeff 1 – CH B>* | | | | *<SNRBoost Coeff 2 – CH B>* | | | |

See SNR enhancement using SNRBoost

| A7 – A0 IN HEX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 6A | | **<GAIN CORRECTION – CH B>** *+0.001 dB to +0.134 dB, in 128 steps* | | | | | | |

Using the FINE GAIN ADJUST register bits, the channel gain can be trimmed in fine steps. The trim is only additive, has 128 steps & a range of 0.134dB. The relation between the FINE GAIN ADJUST bits & the trimmed channel gain is:

$$\Delta \text{ Channel Gain} = 20 \times \log10[1 + (\text{FINE GAIN ADJUST}/8192)]$$

Note that the total device gain = ADC gain + Δ Channel gain. The ADC gain is determined by register bits <**GAIN PROGRAMMABILITY**>

| A7 – A0 IN HEX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 6C | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ***<SNRBoost Enable – CH B>*** |

**D0** ***<SNRBoost Enable – CH B>***

SNRBoost control for channel B (*only with independent control)*.

0 SNRBoost disabled

1 SNRBoost enabled

| A7 – A0 IN HEX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 75 | | | 0 | 0 | 0 | **<TEST PATTERNS – CH B>** | | |

**D2-D0** **<TEST PATTERNS>** Test Patterns to verify data capture

Applies to both channels (*with common control*) for channel A only (*with independent control*)

000 Normal operation

001 Outputs all zeros

010 Outputs all ones

011 Outputs toggle pattern
Output data <D10:D0> alternates between 01010101010 and 10101010101 every clock cycle.

100 Outputs digital ramp
Output data increments by one LSB (12-bit) every 8th clock cycle from code 0 to code 2047.

101 Outputs custom pattern (use registers 0x51, 0x52 for setting the custom pattern)

110 Unused

111 Unused

| A7 – A0 IN HEX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 76 | 0 | 0 | <OFFSET PEDESTAL – Common/Ch A> | | | | | |

**D5-D0 <OFFSET PEDESTAL – Ch B>**

When the offset correction is enabled, the final converged value after the offset is corrected will be the ADC mid-code value. A pedestal can be added to the final converged value by programming these bits. See "Offset Correction" in application section.

Applies to both channels (*with common control*) or for channel A only (*with independent control*).

011111 PEDESTAL = 31 LSB

011110 PEDESTAL = 30 LSB

011101 PEDESTAL = 29 LSB

....

000000 PEDESTAL = 0 LSB

....

111111 PEDESTAL = –1 LSB

111110 PEDESTAL = –2 LSB

....

100000 PEDESTAL = –32LSB

## PIN CONFIGURATION (LVDS INTERFACE) – ADS62C17

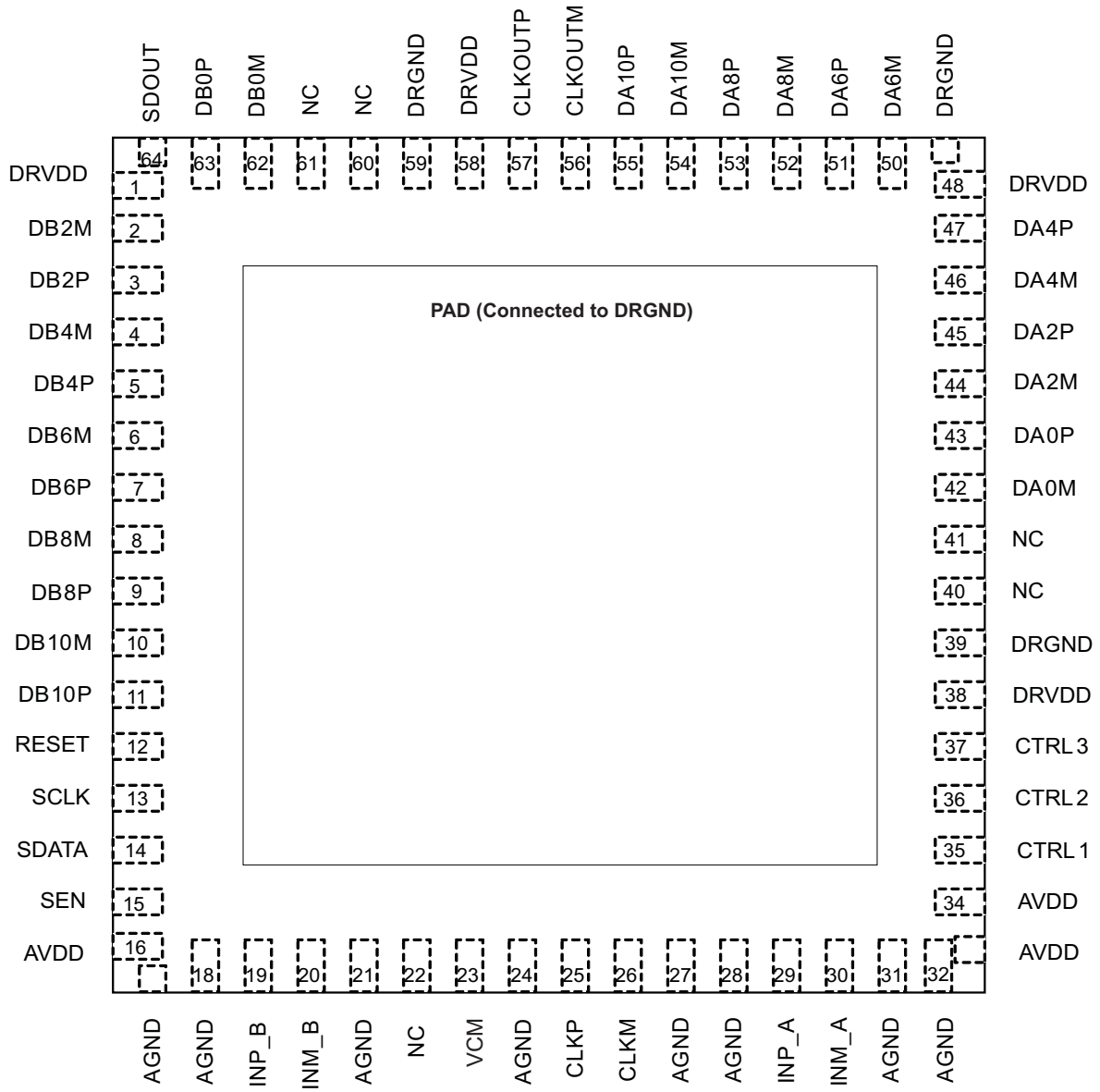



**Figure 10. Pin Configuration**

## PIN ASSIGNMENTS (LVDS INTERFACE) – ADS62C17

| PIN | | NO. OF PINS | PIN TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | NUMBER | | | |
| AVDD | 16, 33, 34 | 3 | I | Analog power supply |
| AGND | 17,18,21,24, 27,28,31,32 | 8 | I | Analog ground |
| CLKP, CLKM | 25, 26 | 2 | I | Differential clock input |
| INP_A, INM_A | 29, 30 | 2 | I | Differential analog input, Channel A |
| INP_B, INM_B | 19, 20 | 2 | I | Differential analog input, Channel B |
| VCM | 23 | 1 | IO | Internal reference mode – Common-mode voltage output.<br>External reference mode – Reference input. The voltage forced on this pin sets the internal references. |
| RESET | 12 | 1 | I | Serial interface RESET input.<br>When using the serial interface mode, the user **must** initialize internal registers through hardware RESET by applying a high-going pulse on this pin or by using software reset option. Refer to **Serial Interface** section.<br>In parallel interface mode, the user has to tie RESET pin permanently **high**. (SCLK and SEN are used as parallel control pins in this mode)<br>The pin has an internal 100 kΩ pull-down resistor. |
| SCLK | 13 | 1 | I | This pin functions as serial interface clock input when RESET is **low.**<br>It controls selection of internal or external reference when RESET is tied high. See Table 5 for detailed information.<br>The pin has an internal 100 kΩ pull-down resistor. |
| SDATA | 14 | 1 | I | Serial interface data input.<br>The pin has an internal 100 kΩ pull-down resistor.<br>The pin has no function in parallel interface mode and can be tired to ground. |
| SEN | 15 | 1 | I | This pin functions as serial interface enable input when RESET is **low**.<br>It controls selection of data format and interface type when RESET is tied high. See Table 6 for detailed information.<br>The pin has an internal 100 kΩ pull-up resistor to AVDD |
| SDOUT | 64 | 1 | O | This pin functions as serial interface register readout, when the <SERIAL READOUT> bit is enabled.<br>When <SERIAL READOUT> = 0, this pin forces logic LOW & is not tri-stated. |
| CTRL1 | 35 | 1 | I | Digital control input pins. Together, they control SNRBoost control and power down modes. |
| CTRL2 | 36 | 1 | I | |
| CTRL3 | 37 | 1 | I | |
| CLKOUTP | 57 | 1 | O | Differential output clock, true |
| CLKOUTM | 56 | 1 | O | Differential output clock, complement |
| DA0P, DA0M | Refer to Figure 10 | 2 | O | Differential output data pair, D0 and 0 multiplexed – Channel A |
| DA2P, DA2M | | 2 | O | Differential output data D1 and D2 multiplexed, true – Channel A |
| DA4P, DA4M | | 2 | O | Differential output data D3 and D4 multiplexed, true – Channel A |
| DA6P, DA6M | | 2 | O | Differential output data D5 and D6 multiplexed, true – Channel A |
| DA8P, DA8M | | 2 | O | Differential output data D7 and D8 multiplexed, true – Channel A |
| DA10P, DA10M | | 2 | O | Differential output data D9 and D10 multiplexed, true – Channel A |
| DB0P, DB0M | | 2 | O | Differential output data pair, D0 and 0 multiplexed – Channel B |
| DB2P, DB2M | | 2 | O | Differential output data D1 and D2 multiplexed, true – Channel B |
| DB4P, DB4M | | 2 | O | Differential output data D3 and D4 multiplexed, true – Channel B |
| DB6P, DB6M | | 2 | O | Differential output data D5 and D6 multiplexed, true – Channel B |
| DB8P, DB8M | | 2 | O | Differential output data D7 and D8 multiplexed, true – Channel B |
| DB10P, DB10M | | 2 | O | Differential output data D9 and D10 multiplexed, true – Channel B |
| DRVDD | 1,38,48,58 | 4 | I | Output buffer supply |

| PIN | | NO. OF PINS | PIN TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | NUMBER | | | |
| DRGND | 39,49,59,PAD | 4 | I | Output buffer ground |
| NC | Refer to Figure 10 | | | Do not connect |

## PIN CONFIGURATION (CMOS INTERFACE) – ADS62C17

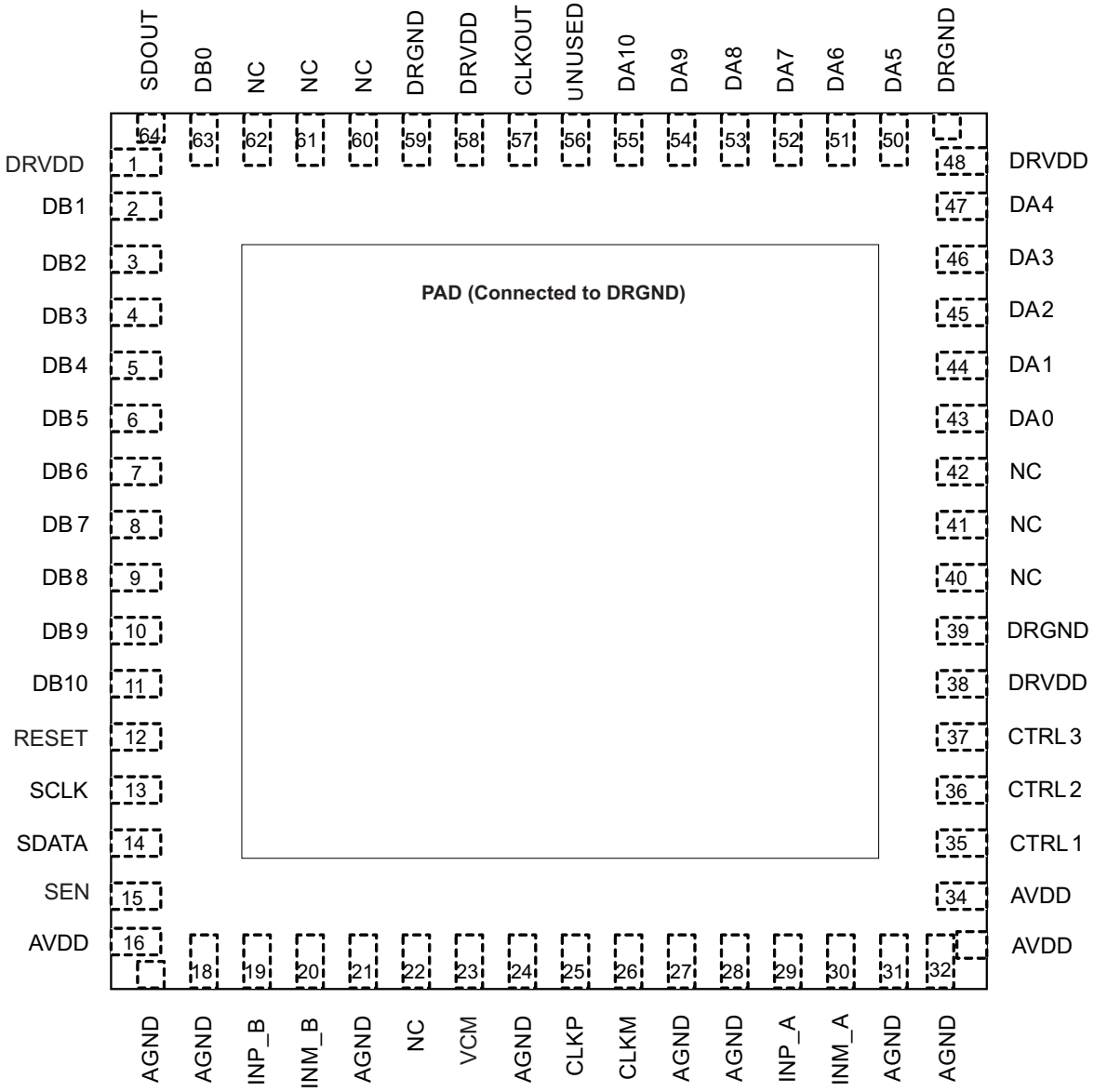



**Figure 11. Pin Configuration**

## PIN ASSIGNMENTS (CMOS INTERFACE) – ADS62C17

| PIN | | NO. OF PINS | PIN TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | NUMBER | | | |
| AVDD | 16, 33, 34 | 3 | I | Analog power supply |
| AGND | 17,18,21,24, 27,28,31, 32 | 8 | I | Analog ground |
| CLKP, CLKM | 25, 26 | 2 | I | Differential clock input |
| INP_A, INM_A | 29, 30 | 2 | I | Differential analog input, Channel A |
| INP_B, INM_B | 19, 20 | 2 | I | Differential analog input, Channel B |
| VCM | 23 | 1 | IO | Internal reference mode – Common-mode voltage output.<br>External reference mode – Reference input. The voltage forced on this pin sets the internal references. |
| RESET | 12 | 1 | I | Serial interface RESET input.<br>When using the serial interface mode, the user MUST initialize internal registers through hardware RESET by applying a high-going pulse on this pin or by using software reset option. Refer to SERIAL INTERFACE section.<br>In parallel interface mode, the user has to tie RESET pin permanently **high**. (SDATA and SEN are used as parallel control pins in this mode)<br>The pin has an internal 100 kΩ pull-down resistor. |
| SCLK | 13 | 1 | I | This pin functions as serial interface clock input when RESET is **low.**<br>It controls selection of internal or external reference when RESET is tied **high**. See Table 5 for detailed information.<br>The pin has an internal 100 kΩ pull-down resistor. |
| SDATA | 14 | 1 | I | Serial interface data input.<br>The pin has an internal 100 kΩ pull-down resistor.<br>The pin has no function in parallel interface mode and can be tired to ground. |
| SEN | 15 | 1 | I | This pin functions as serial interface enable input when RESET is **low**.<br>It controls selection of data format and interface type when RESET is tied **high**. See Table 6 for detailed information.<br>The pin has an internal 100 kΩ pull-up resistor to AVDD |
| SDOUT | 64 | 1 | O | This pin functions as serial interface register readout, when the <SERIAL READOUT> bit is enabled.<br>When <SERIAL READOUT> = 0, this pin forces logic LOW & is not tri-stated. |
| CTRL1 | 35 | 1 | I | Digital control input pins. Together, they control SNRBoost control & power down modes. |
| CTRL2 | 36 | 1 | I | |
| CTRL3 | 37 | 1 | I | |
| CLKOUT | 57 | 1 | O | CMOS output clock |
| DA0, DA10 | Refer to Figure 11 | 11 | O | Channel A 11-bit ADC output data bits, CMOS levels |
| DB0-DB10 | | 11 | O | Channel B 11-bit ADC output data bits, CMOS levels |
| DRVDD | 1,38,48,58 | 4 | I | Output buffer supply |
| DRGND | 39,49,59,PAD | 3 | I | Output buffer ground |
| NC | Refer to Figure 11 | | | Do not connect |

## TYPICAL CHARACTERISTICS

All plots are at 25 °C, AVDD = 3.3 V, DRVDD = 1.8 V, sampling frequency = 200 MSPS, sine wave input clock. 1.5 VPP differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, SNRBoost disabled, internal reference mode, 0 dB gain, LVDS output interface (unless otherwise noted)

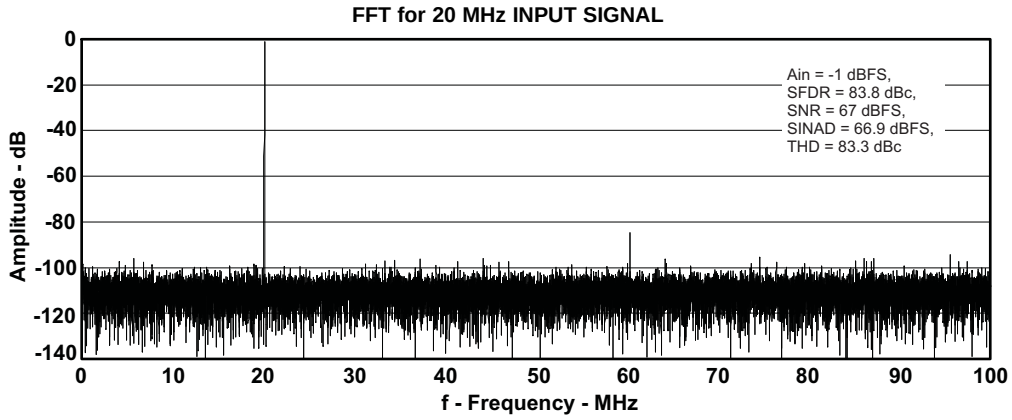



Figure 12.

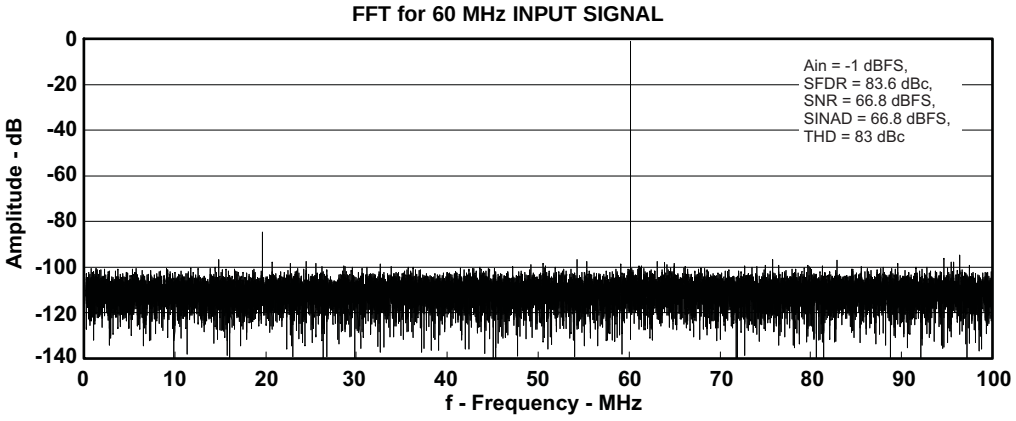



Figure 13.

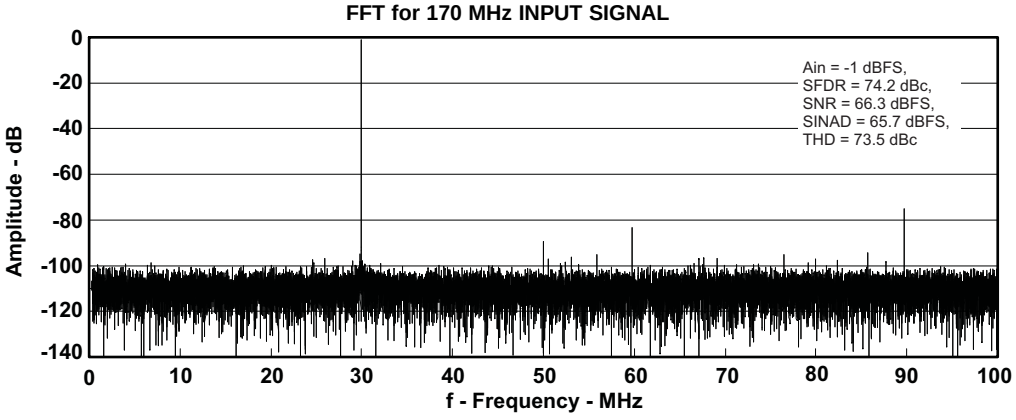



Figure 14.

## TYPICAL CHARACTERISTICS (continued)

All plots are at 25 °C, AVDD = 3.3 V, DRVDD = 1.8 V, sampling frequency = 200 MSPS, sine wave input clock. 1.5 VPP differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, SNRBoost disabled, internal reference mode, 0 dB gain, LVDS output interface (unless otherwise noted)

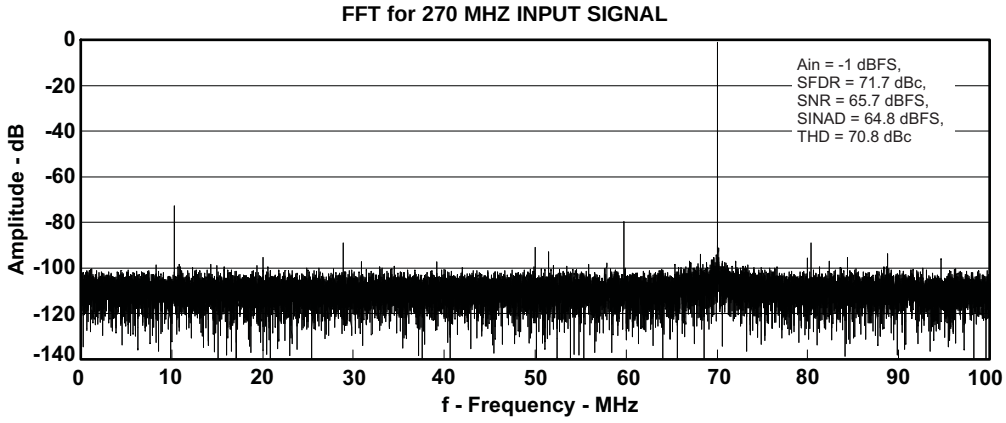



Figure 15.

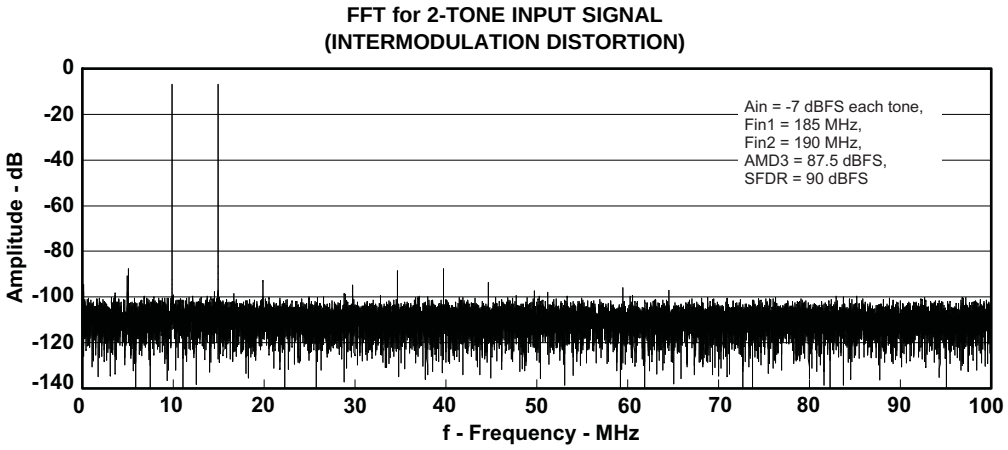



Figure 16.

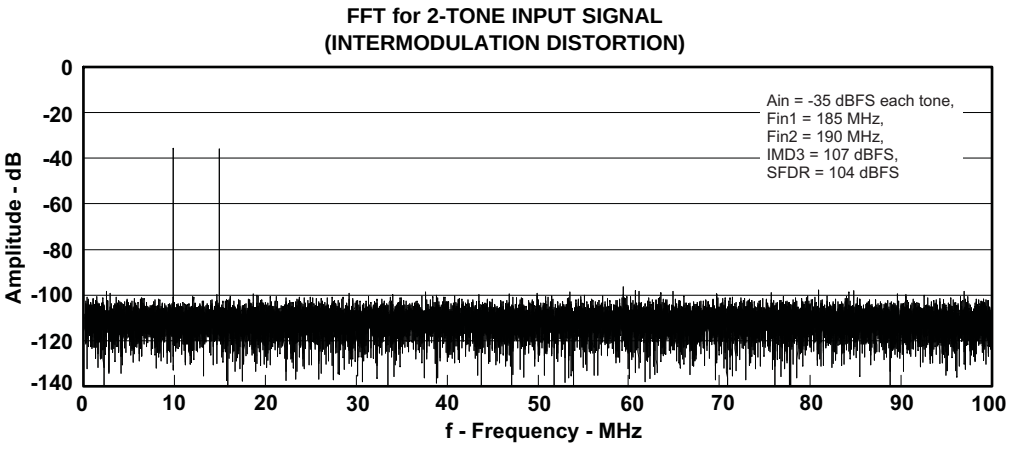



Figure 17.

## TYPICAL CHARACTERISTICS (continued)

All plots are at 25 °C, AVDD = 3.3 V, DRVDD = 1.8 V, sampling frequency = 200 MSPS, sine wave input clock. 1.5 VPP differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, SNRBoost disabled, internal reference mode, 0 dB gain, LVDS output interface (unless otherwise noted)

**FFT with SNRBOOST ENABLED for 5MHz, 10MHZ, and 15 MHz BANDWIDTHS, Fin = 150 MHz, Fcenter = Fs/4**

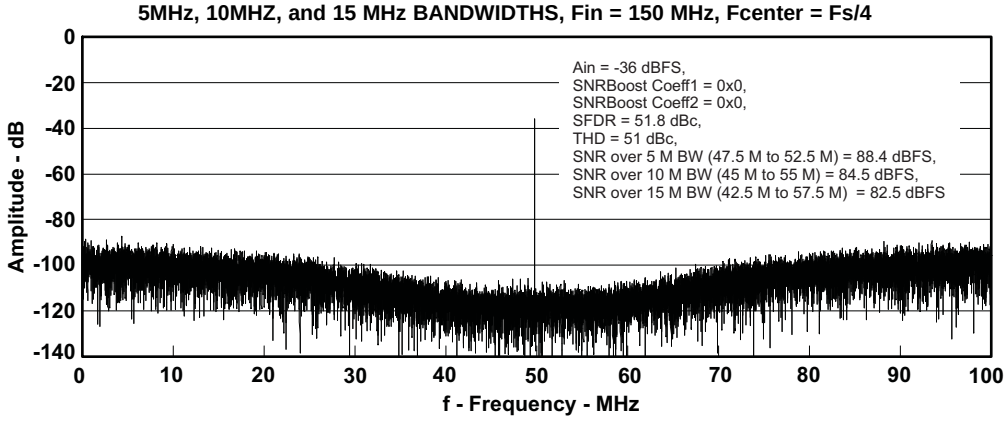



Figure 18.

**FFT with SNRBOOST ENABLED for 20 MHz BANDWIDTH, Fin = 150 MHz, Fcenter = Fs/4**

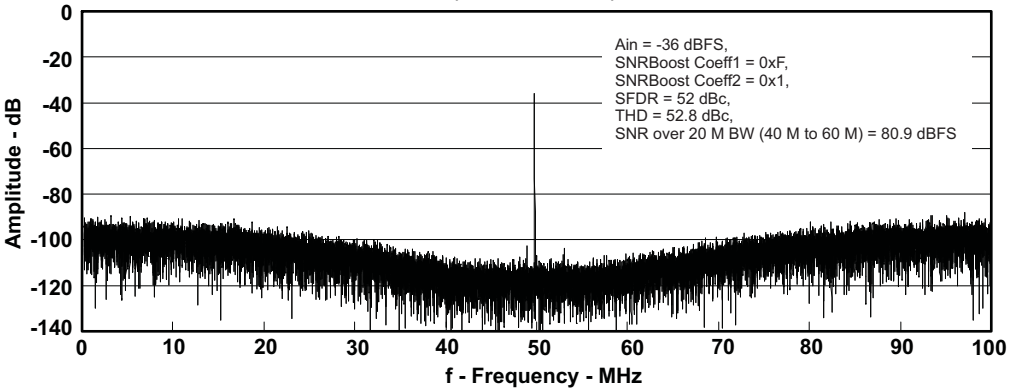



Figure 19.

**FFT with SNRBOOST ENABLED for 30MHz, BANDWIDTH, Fin = 150 MHz, Fcenter = Fs/4**

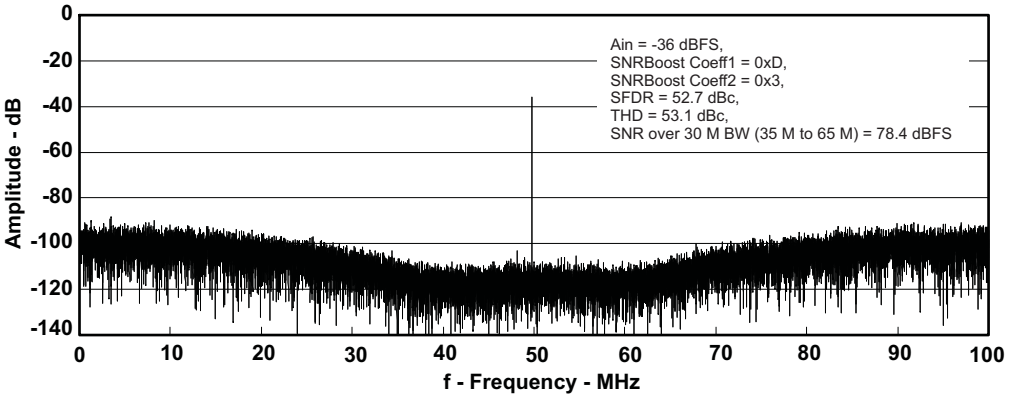



Figure 20.

## TYPICAL CHARACTERISTICS (continued)

All plots are at 25 °C, AVDD = 3.3 V, DRVDD = 1.8 V, sampling frequency = 200 MSPS, sine wave input clock. 1.5 VPP differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, SNRBoost disabled, internal reference mode, 0 dB gain, LVDS output interface (unless otherwise noted)

**FFT with SNRBOOST ENABLED for 40MHz, BANDWIDTH, Fin = 150 MHz, Fcenter = Fs/4**

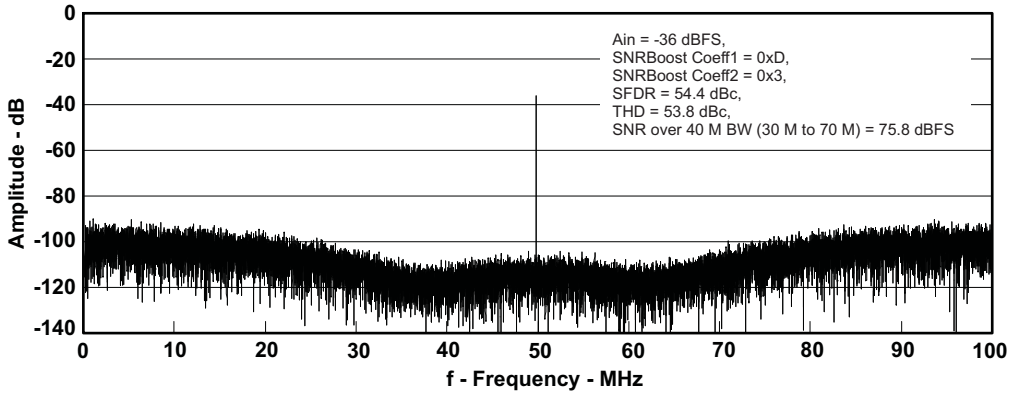



**Figure 21.**

**SNR with SNRBOOST ENABLE and DISABLED**

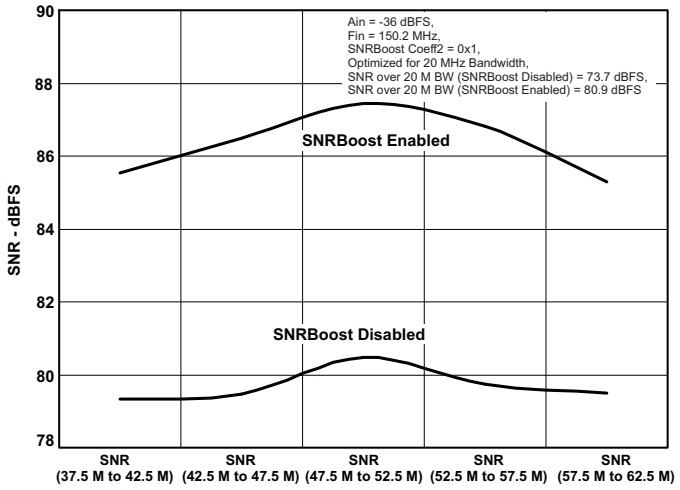



**Figure 22.**

**SFDR ACROSS INPUT FREQUENCY**

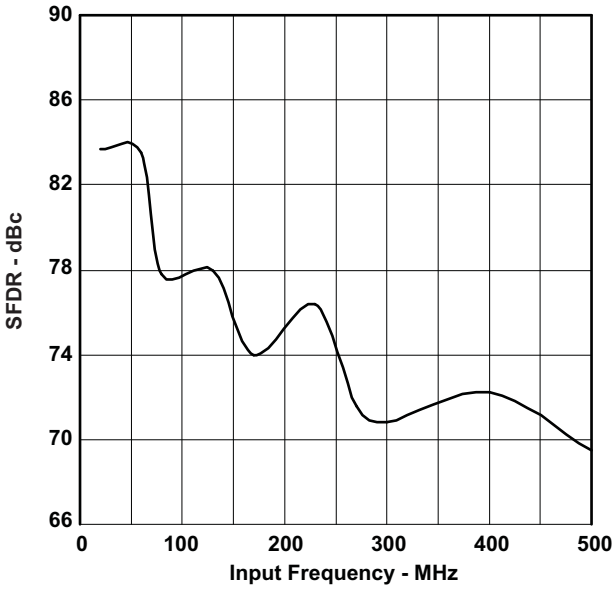



**Figure 23.**

## TYPICAL CHARACTERISTICS (continued)

All plots are at 25 °C, AVDD = 3.3 V, DRVDD = 1.8 V, sampling frequency = 200 MSPS, sine wave input clock. 1.5 VPP differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, SNRBoost disabled, internal reference mode, 0 dB gain, LVDS output interface (unless otherwise noted)

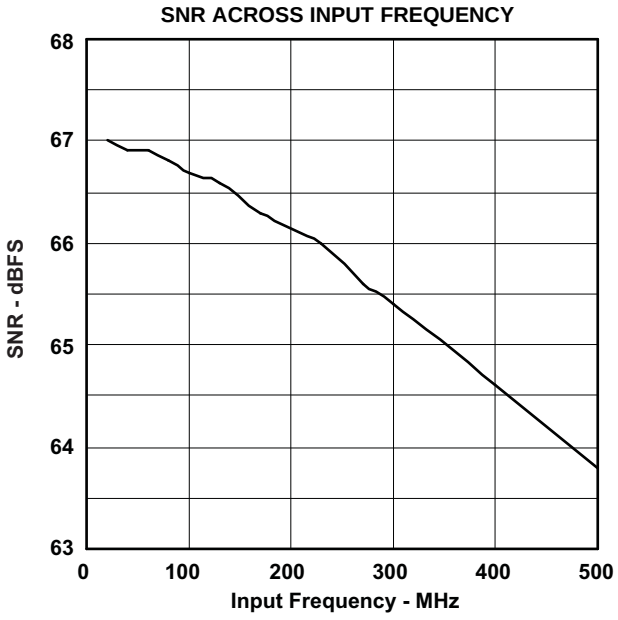



Figure 24.

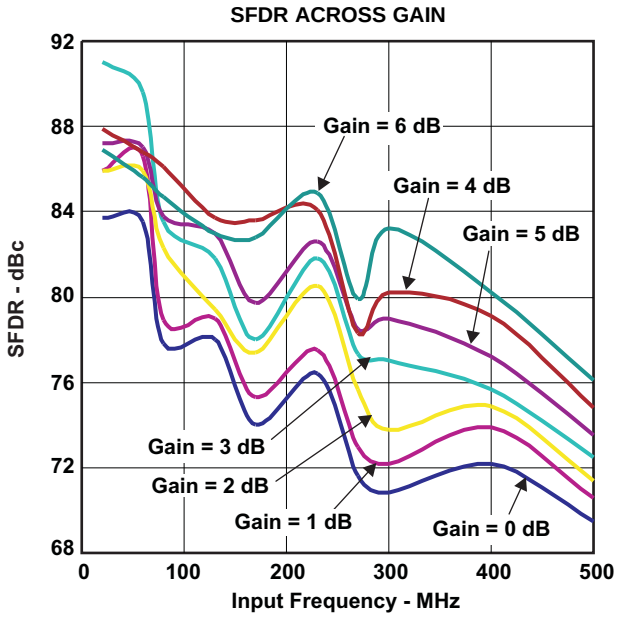



Figure 25.

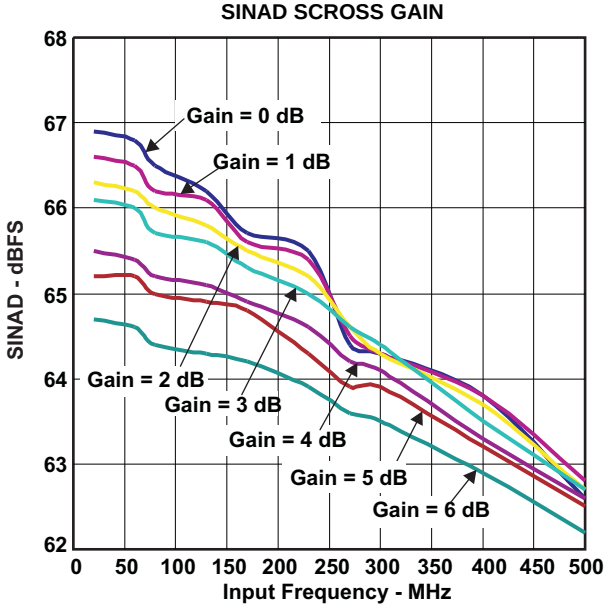



Figure 26.

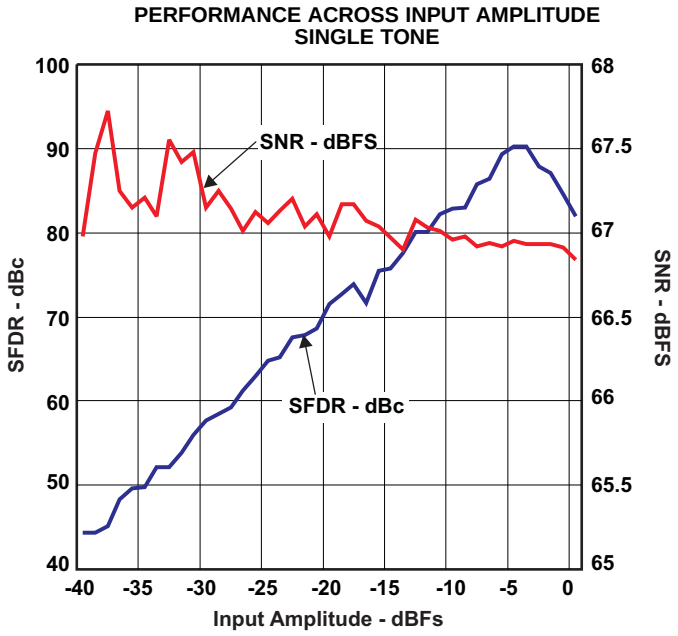



Figure 27.

## TYPICAL CHARACTERISTICS (continued)

All plots are at 25 °C, AVDD = 3.3 V, DRVDD = 1.8 V, sampling frequency = 200 MSPS, sine wave input clock. 1.5 VPP differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, SNRBoost disabled, internal reference mode, 0 dB gain, LVDS output interface (unless otherwise noted)

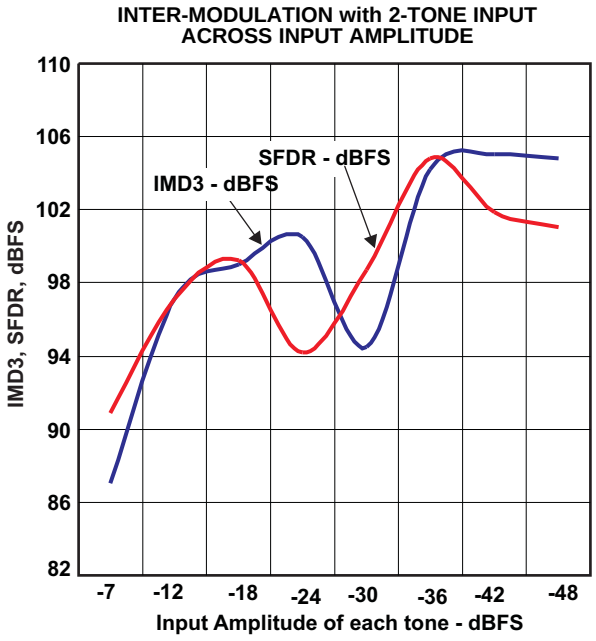



Figure 28.

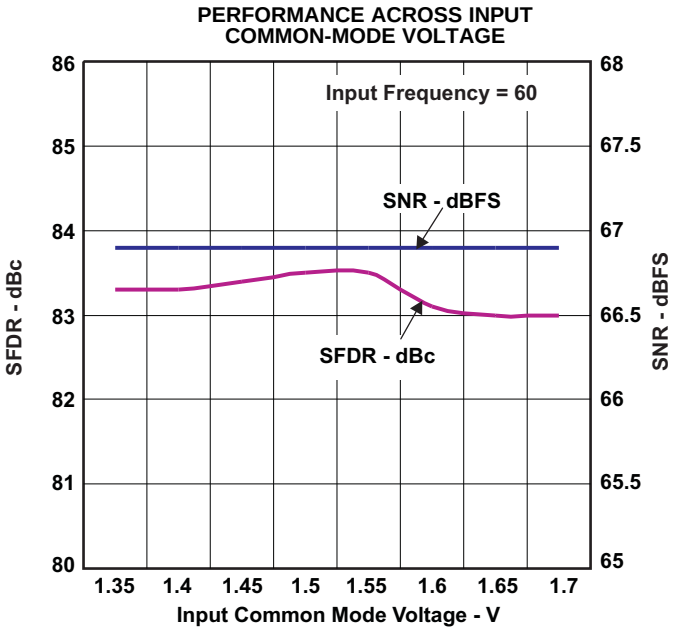



Figure 29.

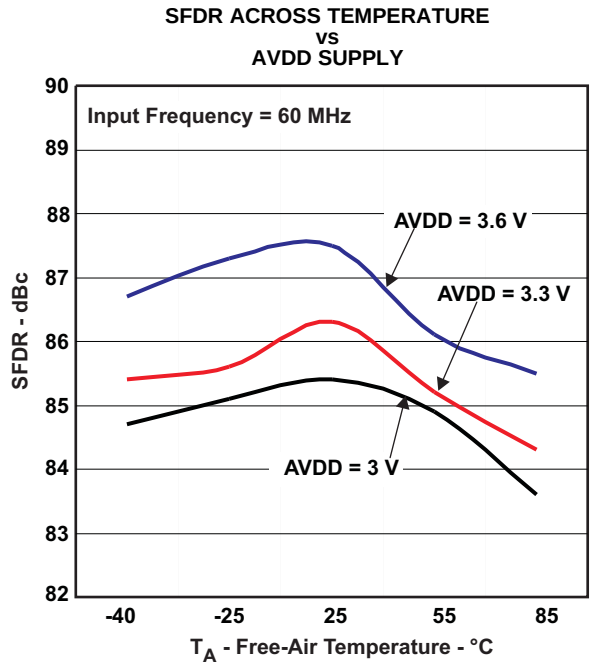



Figure 30.

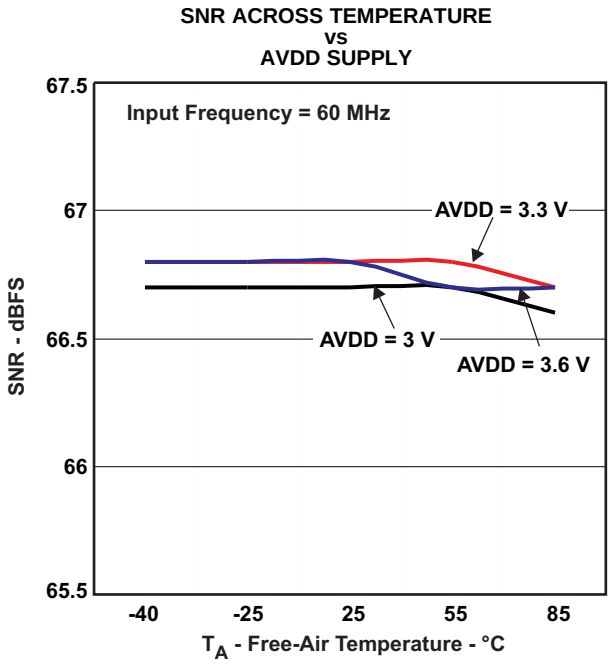



Figure 31.

## TYPICAL CHARACTERISTICS (continued)

All plots are at 25 °C, AVDD = 3.3 V, DRVDD = 1.8 V, sampling frequency = 200 MSPS, sine wave input clock. 1.5 VPP differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, SNRBoost disabled, internal reference mode, 0 dB gain, LVDS output interface (unless otherwise noted)

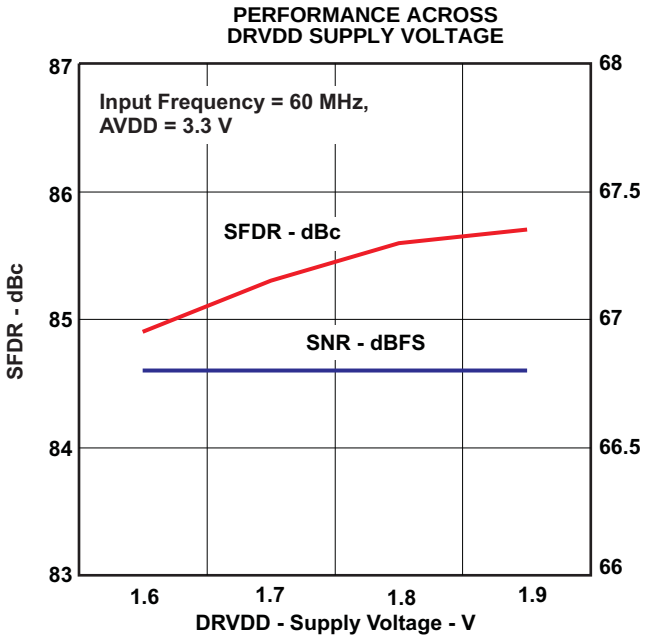



Figure 32.

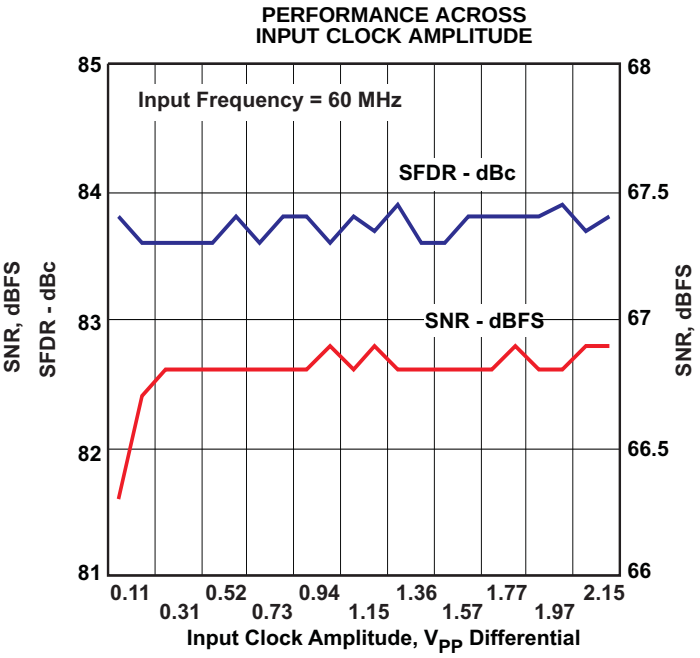



Figure 33.

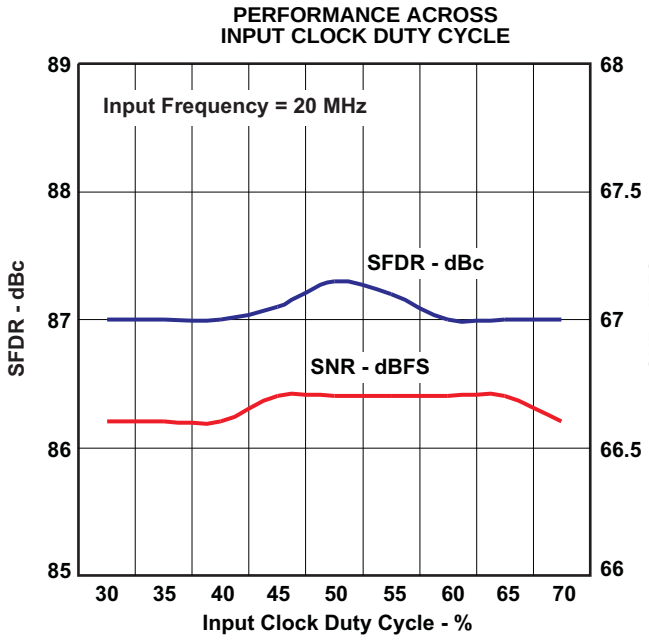



Figure 34.

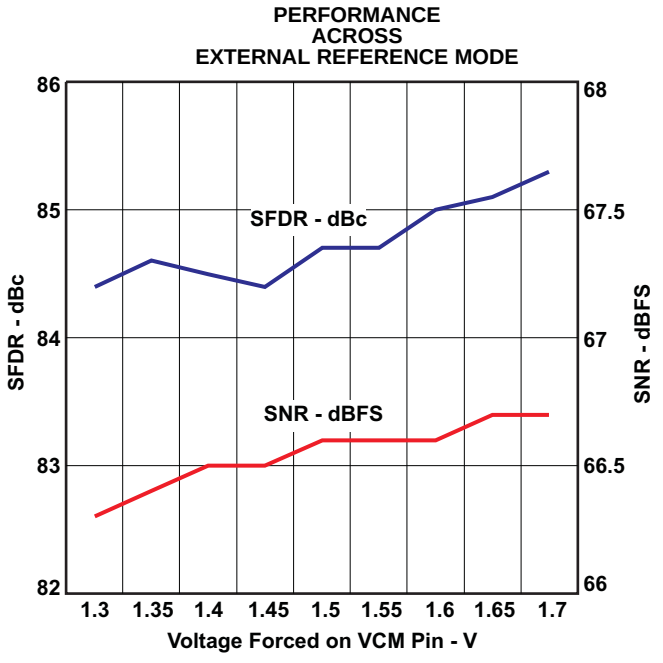



Figure 35.

## TYPICAL CHARACTERISTICS (continued)

All plots are at 25 °C, AVDD = 3.3 V, DRVDD = 1.8 V, sampling frequency = 200 MSPS, sine wave input clock. 1.5 VPP differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, SNRBoost disabled, internal reference mode, 0 dB gain, LVDS output interface (unless otherwise noted)

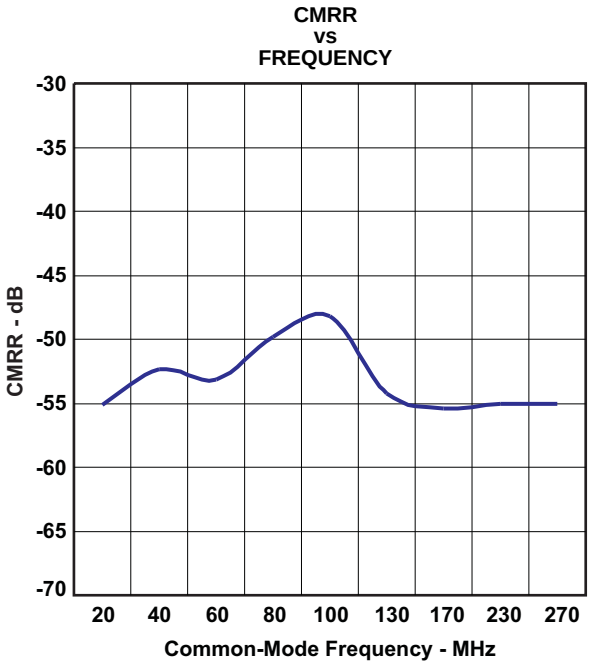



Figure 36.

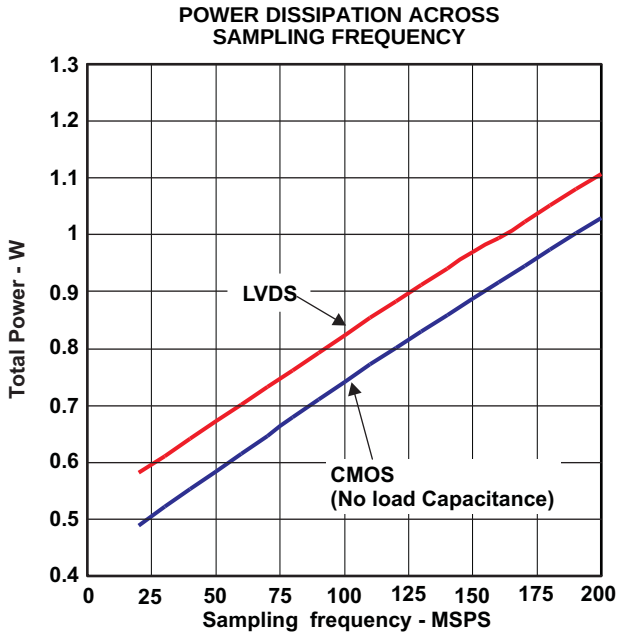



Figure 37.

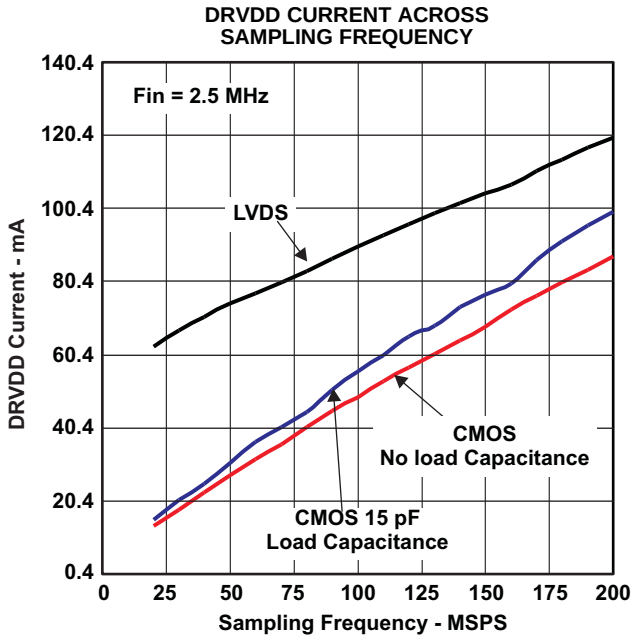



Figure 38.

## TYPICAL CHARACTERISTICS (continued)

All plots are at 25 °C, AVDD = 3.3 V, DRVDD = 1.8 V, sampling frequency = 200 MSPS, sine wave input clock. 1.5 VPP differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, SNRBoost disabled, internal reference mode, 0 dB gain, LVDS output interface (unless otherwise noted)

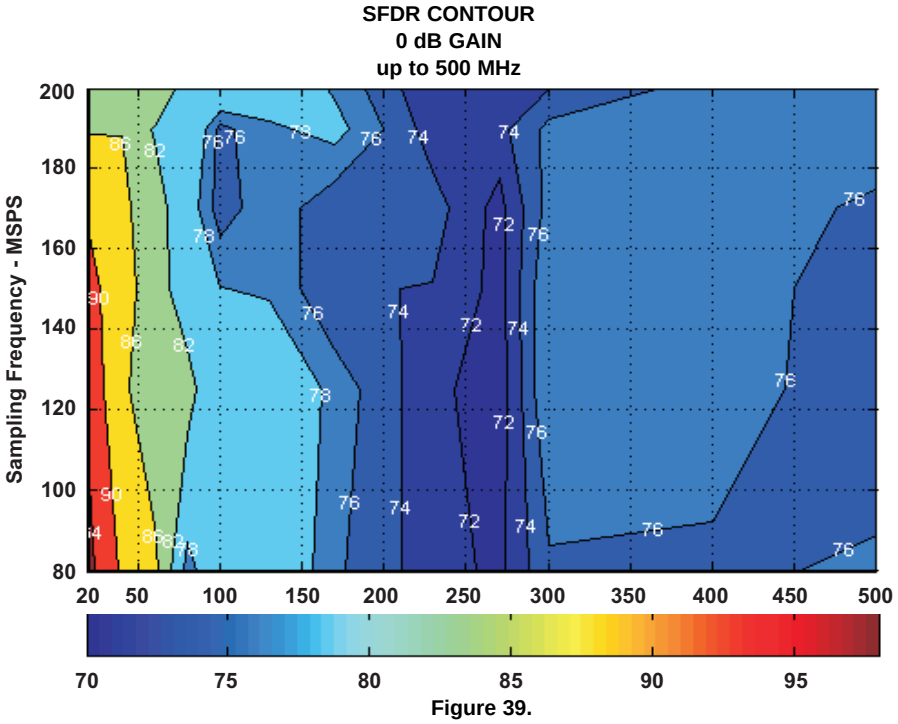



Figure 39.

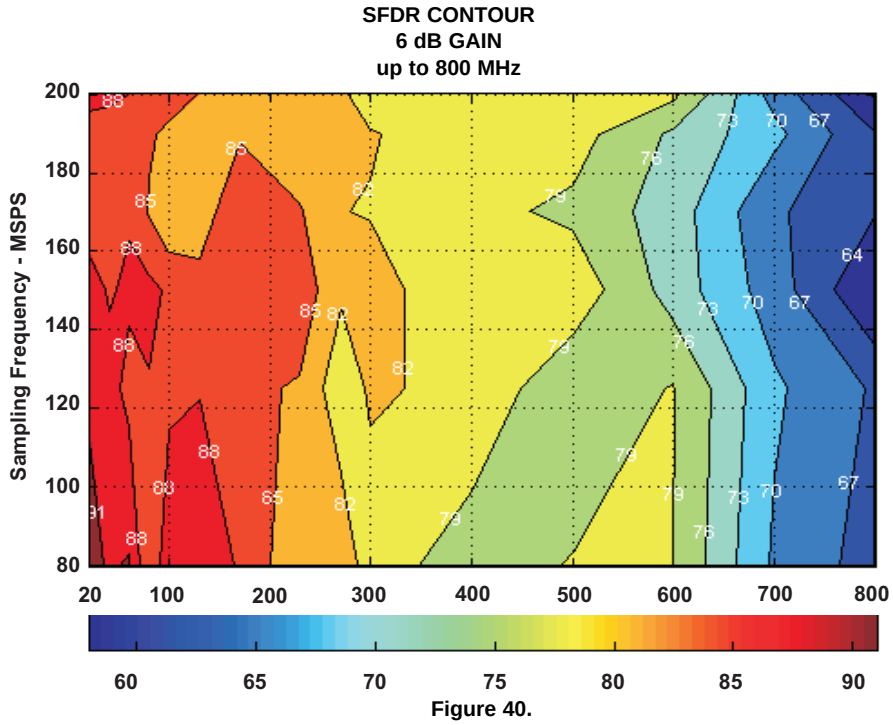



Figure 40.

## TYPICAL CHARACTERISTICS (continued)

All plots are at 25 °C, AVDD = 3.3 V, DRVDD = 1.8 V, sampling frequency = 200 MSPS, sine wave input clock. 1.5 VPP differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, SNRBoost disabled, internal reference mode, 0 dB gain, LVDS output interface (unless otherwise noted)

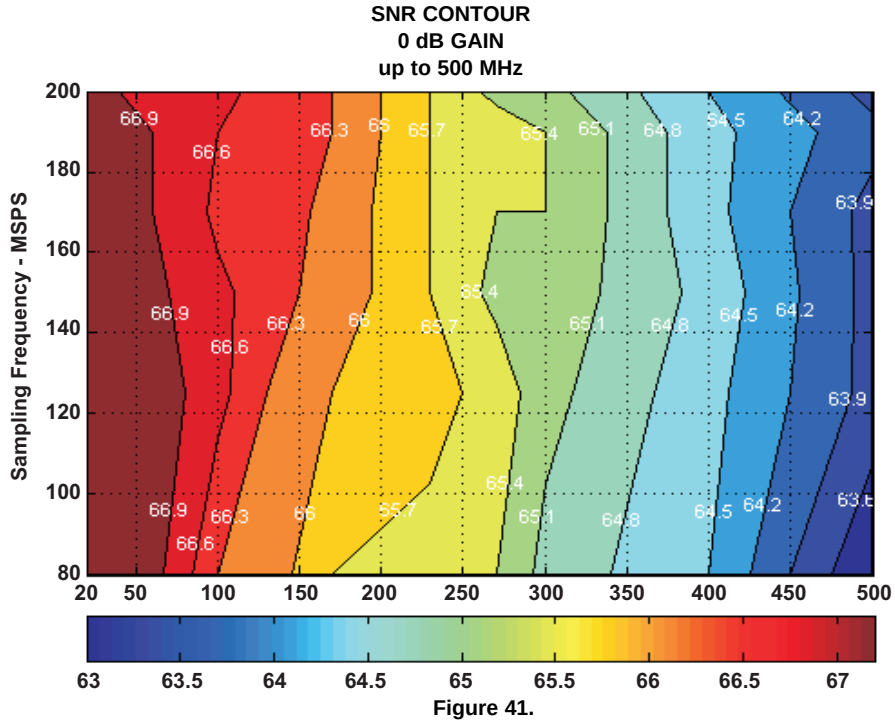



Figure 41.

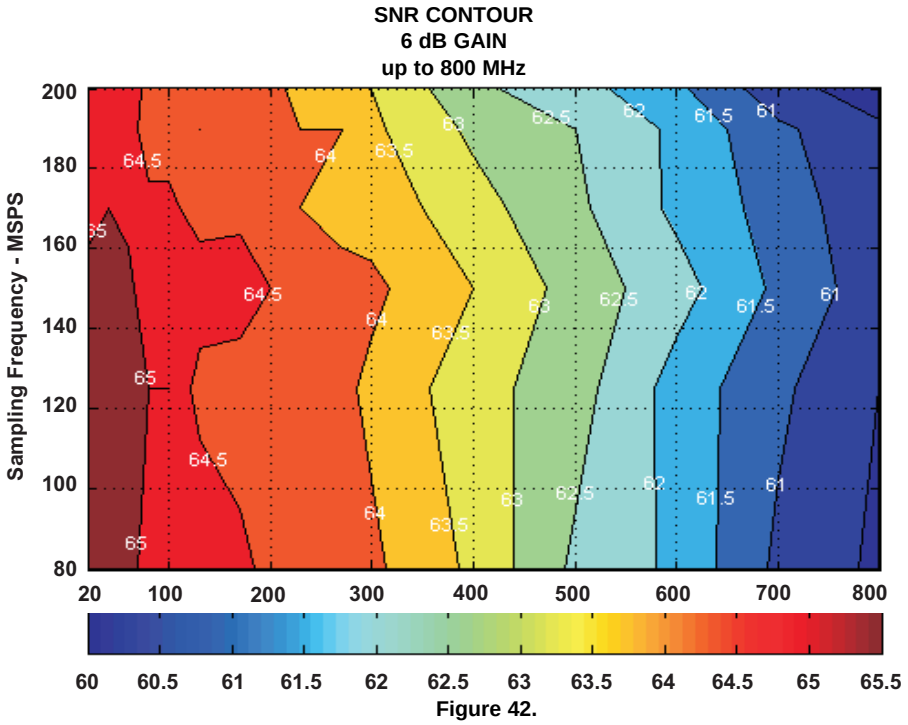



Figure 42.

# APPLICATION INFORMATION

## THEORY OF OPERATION

ADS62C17 is a low power 11-bit pipeline A/D converters with maximum sampling rate up to 200 MSPS.

At every falling edge of the input clock, the analog input signal of each channel is sampled simultaneously. The sampled signal in each channel is converted by a pipeline of low resolution stages. In each stage, the sampled and held signal is converted by a high speed, low resolution flash sub-ADC. The difference (residue) between the stage input and its quantized equivalent is gained and propagates to the next stage. At every clock, each succeeding stage resolves the sampled input with greater accuracy. The digital outputs from all stages are combined in a digital correction logic block and processed digitally to create the final 11 bit code, after a data latency of 22 clock cycles.

The digital output is available as either DDR LVDS or parallel CMOS and coded in either straight offset binary or binary 2s complement format.

The dynamic offset of the first stage sub-ADC limits the maximum analog input frequency to about 500MHz (with 2V pp amplitude) and about 800MHz (with 1V pp amplitude).

## ANALOG INPUT

The analog input consists of a switched-capacitor based differential sample and hold architecture.

This differential topology results in very good AC performance even for high input frequencies at high sampling rates. The INP and INM pins have to be externally biased around a common-mode voltage of 1.5V, available on VCM pin. For a full-scale differential input, each input pin INP, INM has to swing symmetrically between VCM + 0.5V and VCM – 0.5V, resulting in a 2Vpp differential input swing.

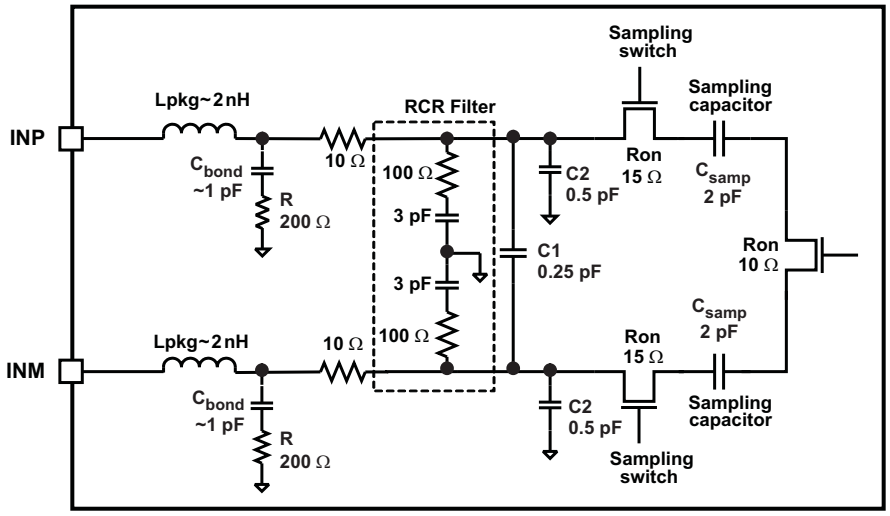



**Figure 43. Analog Input Circuit**

### Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This improves the common-mode noise immunity and even order harmonic rejection. A 5 Ω to 15 Ω resistor in series with each input pin is recommended to damp out ringing caused by package parasitic.

SFDR performance can be limited due to several reasons - the effect of sampling glitches (described below), non-linearity of the sampling circuit & non-linearity of the quantizer that follows the sampling circuit.

Depending on the input frequency, sample rate & input amplitude, one of these plays a dominant part in limiting performance.

At very high input frequencies (> about 300 MHz), SFDR is determined largely by the device's sampling circuit non-linearity. At low input amplitudes, the quantizer non-linearity usually limits performance.

Glitches are caused by the opening & closing of the sampling switches. The driving circuit should present a low source impedance to absorb these glitches. Otherwise, this could limit performance, mainly at low input frequencies (up to about 200 MHz). It is also necessary to present low impedance (< 50 Ω) for the common mode switching currents. This can be achieved by using two resistors from each input terminated to the common mode voltage (VCM).

The device includes an internal R-C filter from each input to ground. The purpose of this filter is to absorb the sampling glitches inside the device itself. The cut-off frequency of the R-C filter involves a trade-off.

A lower cut-off frequency (larger C) absorbs glitches better, but it reduces the input bandwidth. On the other hand, with a higher cut-off frequency (smaller C), bandwidth support is maximized. But now, the sampling glitches need to be supplied by the external drive circuit. This has limitations due to the presence of the package bond-wire inductance.

In ADS62C17, the R-C component values have been optimized while supporting high input bandwidth (up to 700 MHz). However, in applications with input frequencies up to 200-300MHz, the filtering of the glitches can be improved further using an external R-C-R filter (as shown in Figure 46 and Figure 47).

In addition to the above, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched impedance to the source. While doing this, the ADC input impedance must be considered. Figure 44 and Figure 45 show the impedance (Zin = Rin || Cin) looking into the ADC input pins.

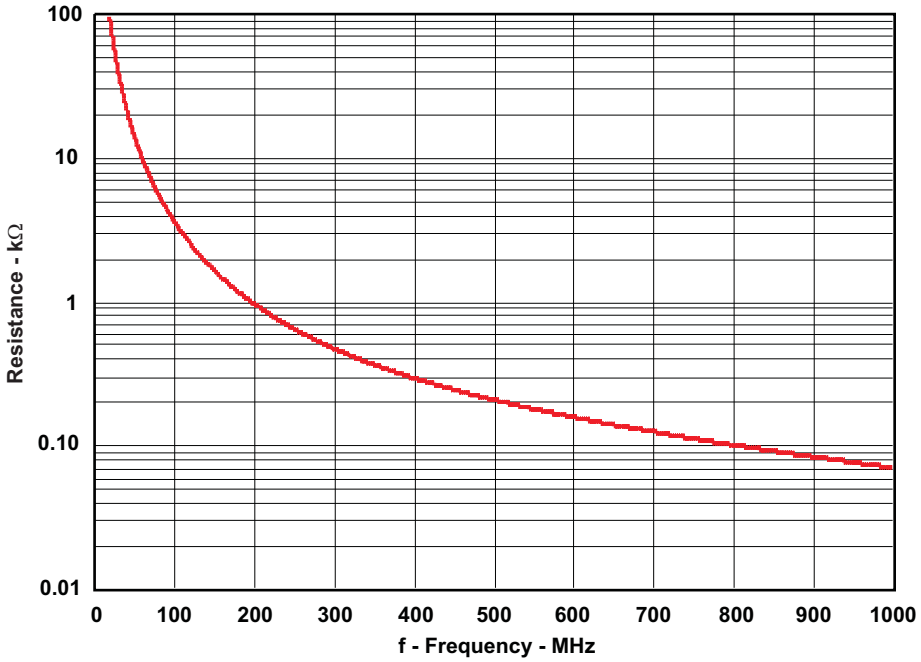



**Figure 44. ADC Analog Input Resistance (Rin) Across Frequency**

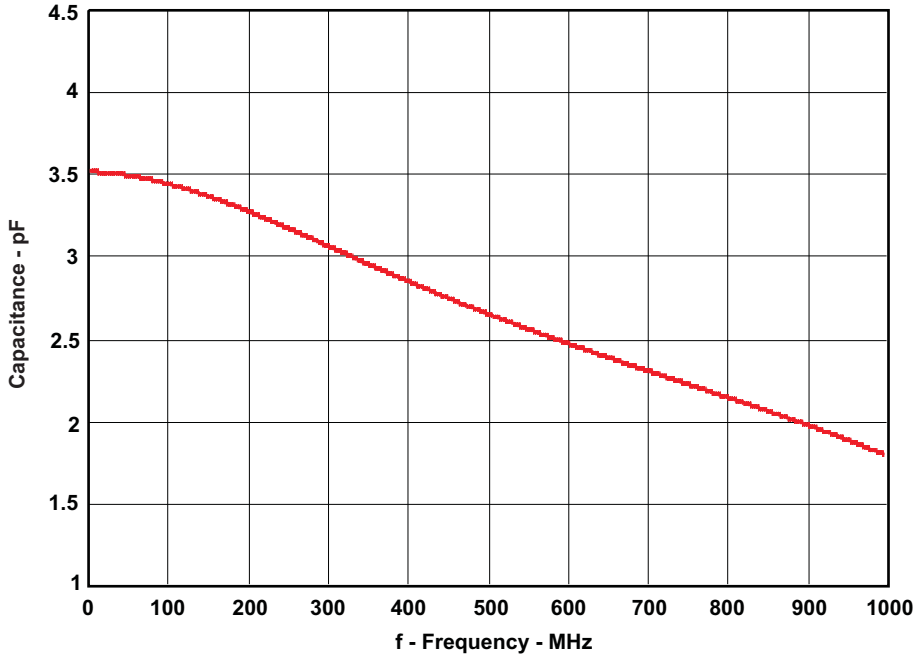



**Figure 45. ADC Analog Input Capacitance (Cin) Across Frequency**

## Driving Circuit

Two example driving circuit configurations are shown in Figure 46 and Figure 47 – one optimized for low bandwidth (low input frequencies) and the other one for high bandwidth to support higher input frequencies.

In Figure 46, an external R-C-R filter using 22pF has been used. Together with the series inductor (39nH), this combination forms a filter and absorbs the sampling glitches. Due to the large capacitor (22pF) in the R-C-R and the 15Ω resistors in series with each input pin, the drive circuit has low bandwidth and supports low input frequencies (<100MHz).

To support high input frequencies (up to about 300MHz, see Figure 47), the capacitance used in the R-C-R is reduced to 3.3pF and the series inductors are shorted out. Together with the lower series resistors (5Ω), this drive circuit provides high bandwidth and supports high input frequencies.

Transformers such as ADT1-1WT or ETC1-1-13 can be used up to 300MHz.

Without the external R-C-R filter, the drive circuit has very high bandwidth & can support very high input frequencies (> 300MHz). For example, a transmission line transformer such as ADTL2-18 can be used (Figure 48).

Note that both the drive circuits have been terminated by 50 ohms near the ADC side. The termination is accomplished by a 25 ohms resistor from each input to the 1.5V common-mode (VCM) from the device. This allows the analog inputs to be biased around the required common-mode voltage.

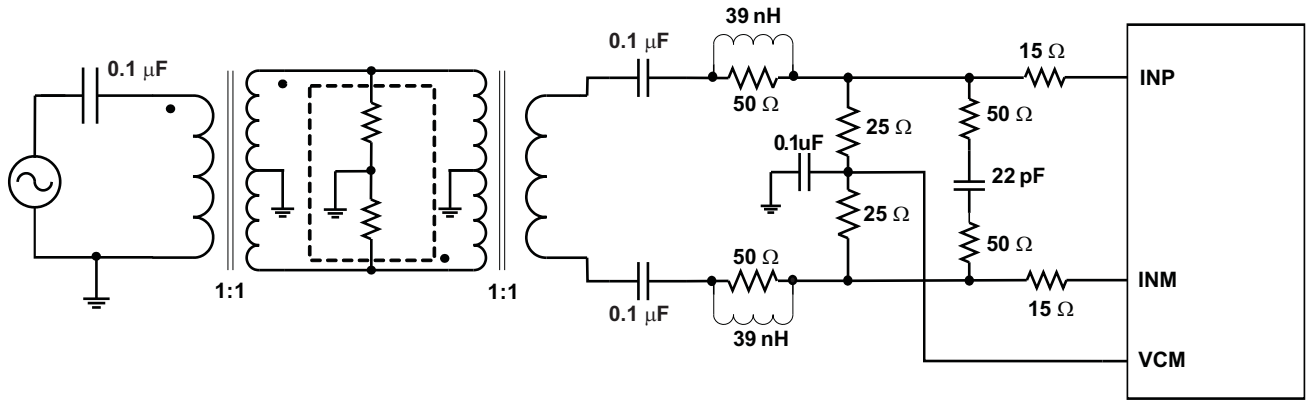



**Figure 46. Drive Circuit With Low Bandwidth (for low input frequencies)**

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back to back helps minimize this mismatch and good performance is obtained for high frequency input signals. An additional termination resistor pair may be required between the two transformers as shown in the figures. The center point of this termination is connected to ground to improve the balance between the P and M sides. The values of the terminations between the transformers and on the secondary side have to be chosen to get an effective 50Ω (in the case of 50Ω source impedance).

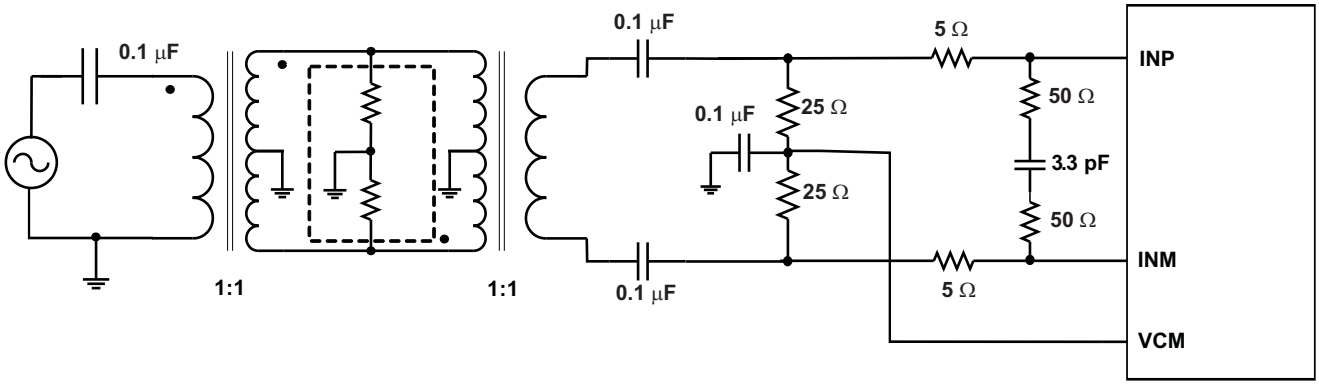



**Figure 47. Drive Circuit With High Bandwidth (for high input frequencies)**

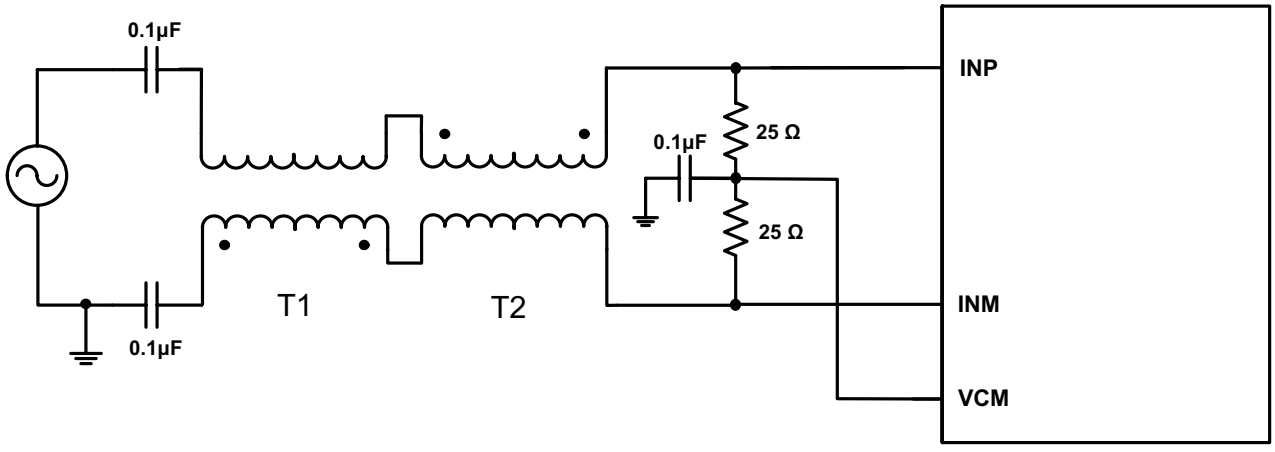



**Figure 48. Drive circuit with very high bandwidth (> 300 MHz)**

All these examples show 1:1 transformers being used with a 50 ohms source. As explained in the "Drive Circuit Requirements", this helps to present a low source impedance to absorb the sampling glitches. With a 1:4 transformer, the source impedance will be 200 ohms. The higher impedance can lead to degradation in performance, compared to the case with 1:1 transformers. For applications where only a band of frequencies are used, the drive circuit can be tuned to present a low impedance for the sampling glitches. Figure 49 shows an example with 1:4 transformer, tuned for a band around 150MHz.

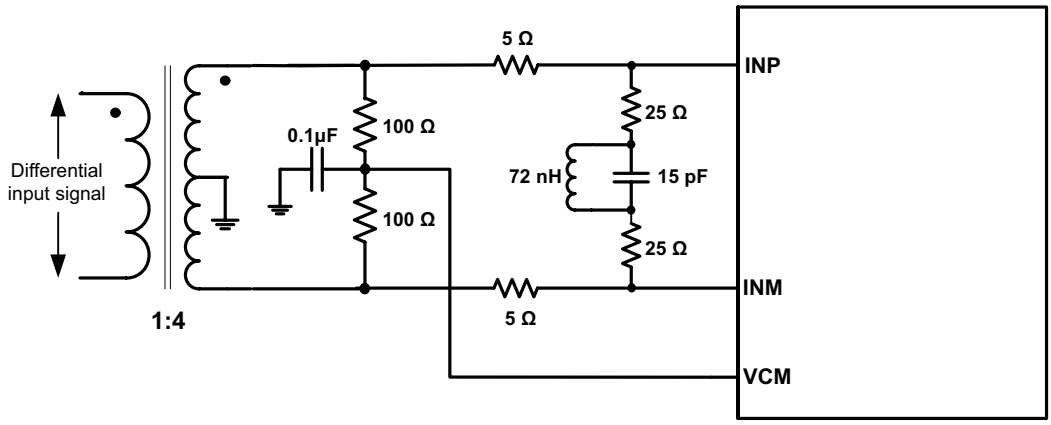



**Figure 49. Drive circuit with 1:4 transformer**

## Input common-mode

To ensure a low-noise common-mode reference, the VCM pin is filtered with a 0.1µF low-inductance capacitor connected to ground. The VCM pin is designed to directly drive the ADC inputs. The input stage of the ADC sinks a common-mode current in the order of 3.6 µA / MSPS (about 720 µA at 200 MSPS).

## REFERENCE

ADS62C17 has built-in internal references REFP and REFM, requiring no external components. Design schemes are used to linearize the converter load seen by the references; this and the on-chip integration of the requisite reference capacitors eliminates the need for external decoupling. The full-scale input range of the converter can be controlled in the external reference mode as explained below. The internal or external reference modes can be selected by programming the serial interface register bit **<REF>**.

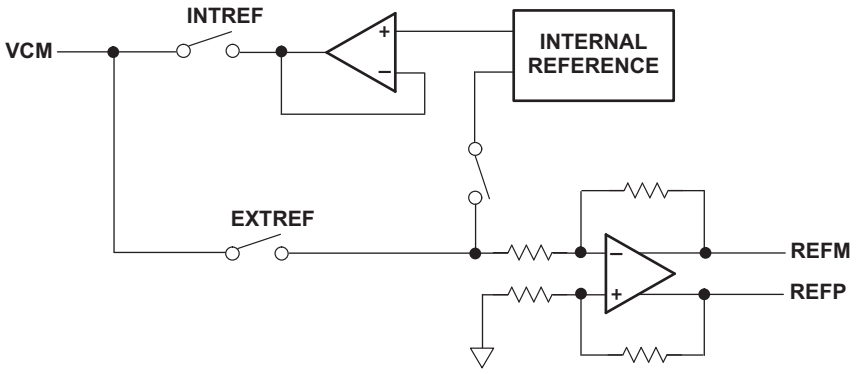



**Figure 50. Reference Section**

### Internal reference

When the device is in internal reference mode, the REFP and REFM voltages are generated internally. Common-mode voltage (1.5V nominal) is output on VCM pin, which can be used to externally bias the analog input pins

### External reference

When the device is in external reference mode, the VCM acts as a reference input pin. The voltage forced on the VCM pin is buffered and gained by 1.33 internally, generating the REFP and REFM voltages. The differential input voltage corresponding to full-scale is given by the following:

Full-scale differential input pp = (Voltage forced on VCM) × 1.33

In this mode, the 1.5V common-mode voltage to bias the input pins has to be generated externally.

## SNR ENHANCEMENT USING SNRBOOST

SNRBoost technology makes it possible to overcome SNR limitations due to quantization noise. With SNRBoost, enhanced SNR can be obtained for any bandwidth (less than Nyquist or Fs/2, see Table 1). The SNR improvement is achieved without affecting the default harmonic performance. SNRBoost *is disabled after reset*; it can be enabled using register bit **<SNRBoost Enable>** or using the control pins CTRL1, 2, 3.

(While using the register bits to control SNRBoost, keep CTRL1, CTRL2, CTRL3 low. To use the CTRL pins as SNRBoost control, reset the <SNRBoost Enable> register bits).

When it is enabled, the noise floor in the spectrum acquires a typical bath-tub shape as shown in Figure 51. The bath-tub is centered around a specific frequency (called *center frequency*). The center frequency is located mid-way between two corner frequencies, which are specified by the SNRBoost coefficients (Register bits <SNRBoost Coeff1> and SNRBoost Coeff2>).

Table 9 shows the relation between each coefficient and its corner frequency. By choosing appropriate coefficients, the bath-tub can be positioned over the frequency range 0 to Fs/2 (Table 10 shows some examples). By positioning the bath-tub within the desired signal band, SNR improvement can be achieved (see Table 1). Note that as the bandwidth is increased, the amount of SNR improvement reduces.

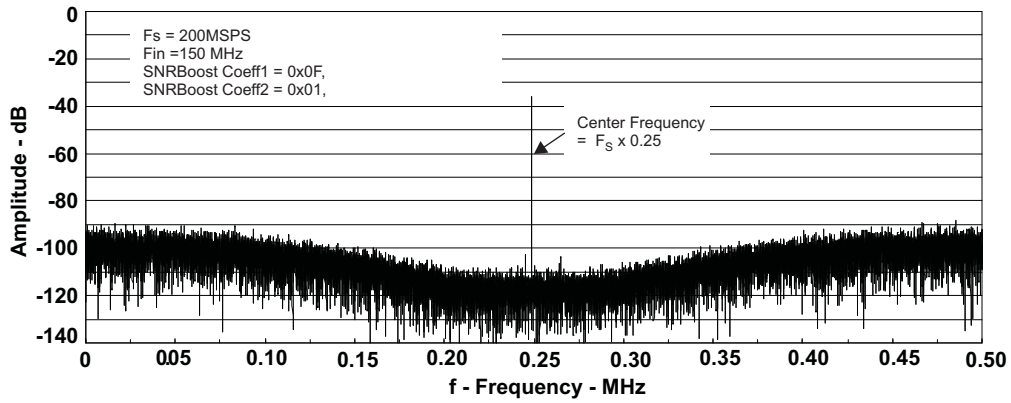



**Figure 51. Specturm with SNRBoost Enabled**

**Table 9. Setting the Corner Frequency**

| SNRBoost Coefficient Value | Normalized Corner Frequency (f/fs) | SNRBoost Coefficient value | Normalized Corner Frequency (f/fs) |
|---|---|---|---|
| 7 | 0.420 | F | 0.230 |
| 6 | 0.385 | E | 0.210 |
| 5 | 0.357 | D | 0.189 |
| 4 | 0.333 | C | 0.167 |
| 3 | 0.311 | B | 0.143 |
| 2 | 0.290 | A | 0.115 |
| 1 | 0.270 | 9 | 0.080 |
| 0 | 0.250 | 8 | 0.000 |

**Table 10. Positioning the Corner Frequency (Some Examples)**

| SNRBoost Coefficient1, <SNRBoost Coeff1> | Normalized Corner Frequency1 (f/fs) | SNRBoost Coefficient1, <SNRBoost Coeff2> | Normalized Corner Frequency2 (f/fs) | Center Frequency |
|---|---|---|---|---|
| 0 | 0.250 | 0 | 0.250 | Fs × 0.25 |
| F | 0.230 | 1 | 0.270 | Fs × 0.25 |
| 6 | 0.385 | 2 | 0.290 | Fs × 0.3375 |
| D | 0.189 | B | 0.143 | Fs × 0.166 |
| 9 | 0.080 | 7 | 0.420 | Fs × 0.25 |

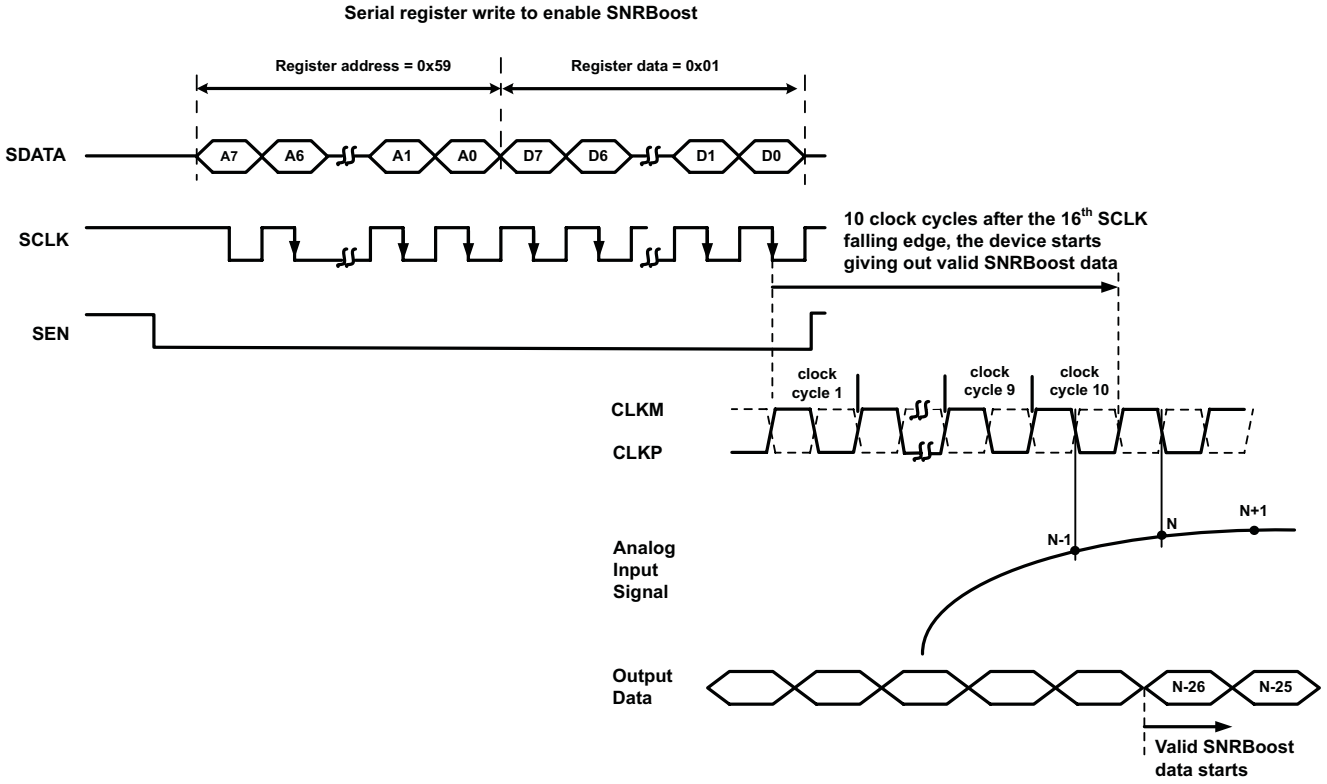



**Figure 52. SNRBoost Active Delay**

*SNRBoost* does not introduce any group delay in the input signal path. The ADC latency increases by four clock cycle (to 26 clock cycles). When it is enabled using the serial interface, the mode becomes fully active 10 input clock cycles after the 16th SCLK falling edge. When it is disabled, normal data (without SNRBoost) resumes after 6 clock cycle.

## CLOCK INPUT

ADS62C17 clock inputs can be driven differentially (sine, LVPECL or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to VCM using internal 5-kΩ resistors as shown in Figure 53. This allows using transformer-coupled drive circuits for sine wave clock or ac-coupling for LVPECL, LVDS clock sources (Figure 54 and Figure 55).

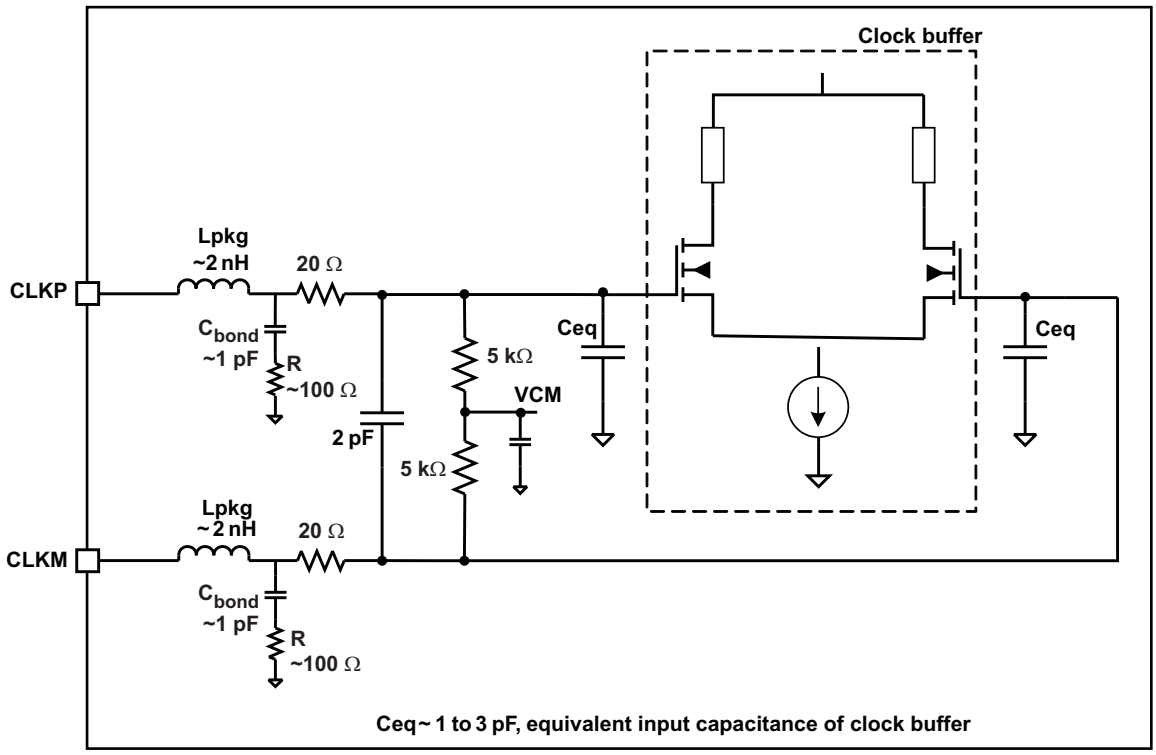



**Figure 53. Internal Clock Buffer**

For best performance, the clock inputs have to be driven differentially, reducing susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effect of jitter. There is no change in performance with a non-50% duty cycle clock input.

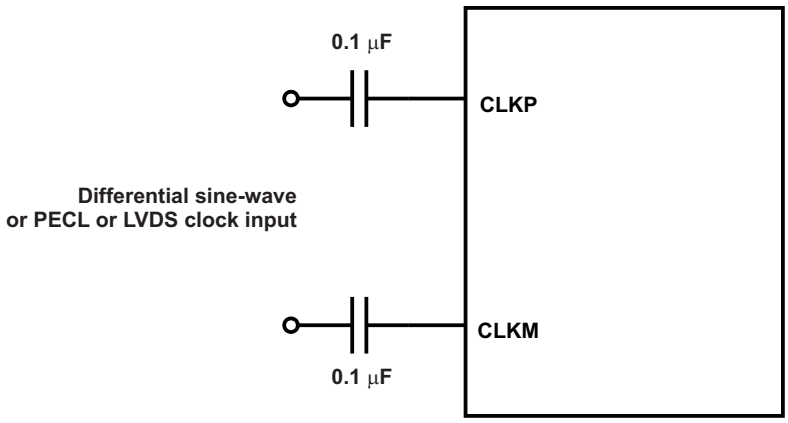



**Figure 54. Differential Clock Driving Circuit**

Single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM tied to 1.5V common-mode voltage. As shown in Figure 55, CLKM can be tied to VCM pin.

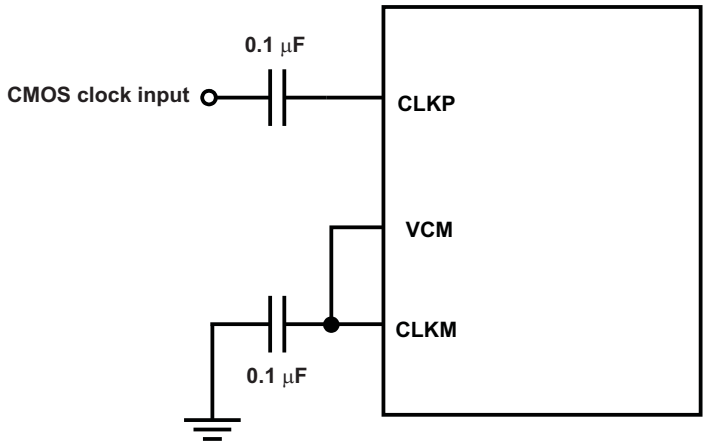



**Figure 55. Single-Ended Clock Driving Circuit**

## GAIN PROGRAMMABILITY

ADS62C17 includes gain settings that can be used to get improved SFDR performance (compared to 0dB gain). The gain is programmable from 0dB to 6dB (in 0.5 dB steps). For each gain setting, the analog input full-scale range scales proportionally, as shown in Table 11.

The SFDR improvement is achieved at the expense of SNR; for each 1dB gain step, the SNR degrades about 1dB. The SNR degradation is less at high input frequencies. As a result, the gain is very useful at high input frequencies as the SFDR improvement is significant with marginal degradation in SNR.

So, the gain can be used to trade-off between SFDR and SNR. Note that the default gain after reset is 0 dB.

**Table 11. Full-Scale Range Across Gains**

| Gain, dB | Full-Scale, Vpp |
|---|---|
| 0 | 2V |
| 1 | 1.78 |
| 2 | 1.59 |
| 3 | 1.42 |
| 4 | 1.26 |
| 5 | 1.12 |
| 6 | 1.00 |

## OFFSET CORRECTION

ADS62C17 has an internal offset correction algorithm that estimates and corrects dc offset up to +/-10mV. The correction can be enabled using the serial register bit **<OFFSET CORRECTION ENABLE>**. Once enabled, the algorithm estimates the channel offset and applies the correction every clock cycle. The time constant of the correction loop is a function of the sampling clock frequency. The time constant can be controlled using register bits **<OFFSET CORR TIME CONSTANT>** as described in Table 12.

After the offset is estimated, the correction can be frozen by setting **<OFFSET CORRECTION ENABLE> = 0**.

Once frozen, the last estimated value is used for offset correction every clock cycle. The correction does not affect the phase of the signal. Note that offset correction is disabled by default after reset.

Figure 56 shows the time response of the offset correction algorithm, after it is enabled.

**Table 12. Time Constant of Offset Correction Algorithm**

| <OFFSET CORR TIME CONSTANT> D3-D0 | Time Constant (TCCLK), Number of Clock Cycles | Time Constant, sec (=$TC_{CLK}$ x 1/Fs)(1) |
|---|---|---|
| 0000 | 256 k | 1.2 ms |
| 0001 | 512 k | 2.5 ms |
| 0010 | 1 M | 5 ms |
| 0011 | 2 M | 10 ms |
| 0100 | 4 M | 20 ms |
| 0101 | 8 M | 40 ms |
| 0110 | 16 M | 80 ms |
| 0111 | 32 M | 0.16 s |
| 1000 | 64 M | 0.32 s |
| 1001 | 128 M | 0.64 s |
| 1010 | 256 M | 1.28 s |
| 1011 | 512 M | 2.5 s |
| 1100 | RESERVED | |
| 1101 | RESERVED | |
| 1110 | RESERVED | |
| 1111 | RESERVED | |

(1) Sampling frequency, Fs = 200 MSPS

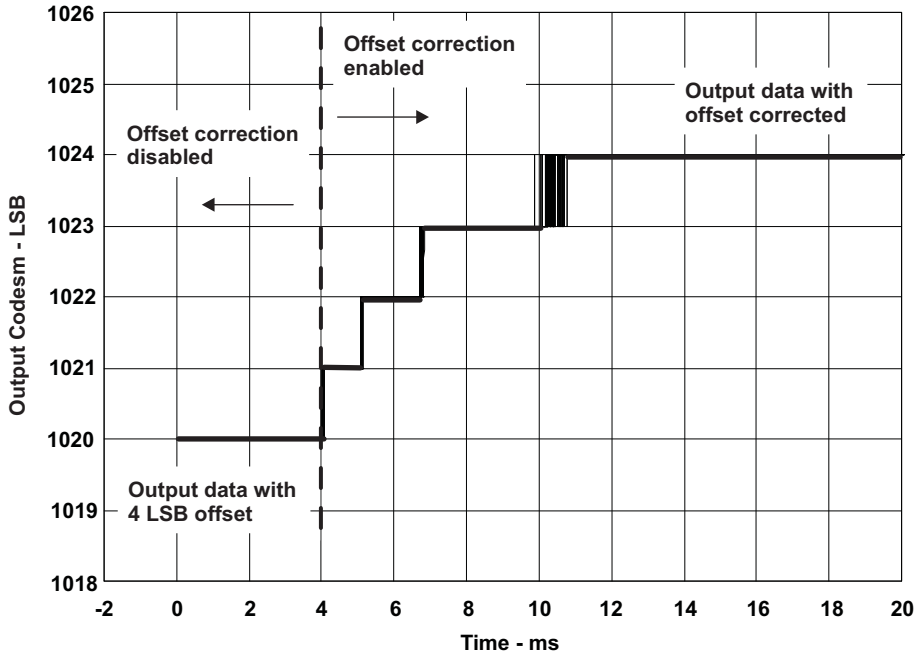



**Figure 56. Time Response of Offset Correction**

## POWER DOWN

ADS62C17 has three power down modes – power down global, individual channel standby and individual channel output buffer disable. These can be set using either the serial register bits or using the control pins CTRL1 to CTRL3.

**Table 13. Power Down Controls**

| POWER DOWN MODES | CONFIGURE USING | | | | WAKE-UP TIME |
|---|---|---|---|---|---|
| | SERIAL INTERFACE | PARALLEL CONTROL PINS | | | |
| Normal operation | **<POWER DOWN MODES>**=0000 | *low* | *low* | *low* | – |
| Output buffer disabled for channel B | **<POWER DOWN MODES>**=1001 | The pins do not support output buffer disable | | | – |
| Output buffer disabled for channel A | **<POWER DOWN MODES>**=1010 | | | | – |
| Output buffer disabled for channel A and B | **<POWER DOWN MODES>**=1011 | | | | Fast (100 ns) |
| Global power down | **<POWER DOWN MODES>**=1100 | *high* | *low* | *low* | Slow (20 µs) |
| Channel B standby | **<POWER DOWN MODES>**=1101 | *high* | *low* | *high* | Fast (1 µs) |
| Channel A standby | **<POWER DOWN MODES>**=1110 | *high* | *high* | *low* | Fast (1 µs) |
| Multiplexed (MUX) mode – Output data of channel A and B is multiplexed & available on DA10 to DA0 pins. | **<POWER DOWN MODES>**=1111 | *high* | *high* | *high* | – |

### Power Down Global

In this mode, the entire chip including both the A/D converters, internal reference and the output buffers are powered down resulting in reduced total power dissipation of about 45mW. The output buffers are in high impedance state. The wake-up time from the global power down to data becoming valid in normal mode is typically 20 µs.

### Channel Power Down (individual or both channels)

Here, each channel's A/D converter can be powered down. The internal references are active, resulting in quick wake-up time of 1 µs. The total power dissipation in standby is about 450 mW.

### Output Buffer Disable (individual or both channels)

Each channel's output buffer can be disabled and put in high impedance state – wakeup time from this mode is fast, about 100 ns.

### Input Clock Stop

In addition to the above, the converter enters a low-power mode when the input clock frequency falls below 1MSPS. The power dissipation is about 275 mW.

## POWER SUPPLY SEQUENCE

During power-up, the AVDD and DRVDD supplies can come up in any sequence. The two supplies are separated in the device.

## DIGITAL OUTPUT INTERFACE

ADS62C17 provides 11-bit data and an output clock synchronized with the data.

Two output interface options are available – Double Data Rate (DDR) LVDS and parallel CMOS. They can be selected using the serial interface register bit **<LVDS_CMOS>** or using DFS pin in parallel configuration mode.

### DDR LVDS Interface

In this mode, the data bits and clock are output using LVDS (Low Voltage Differential Signal) levels. Two data bits are multiplexed and output on each LVDS differential pair.

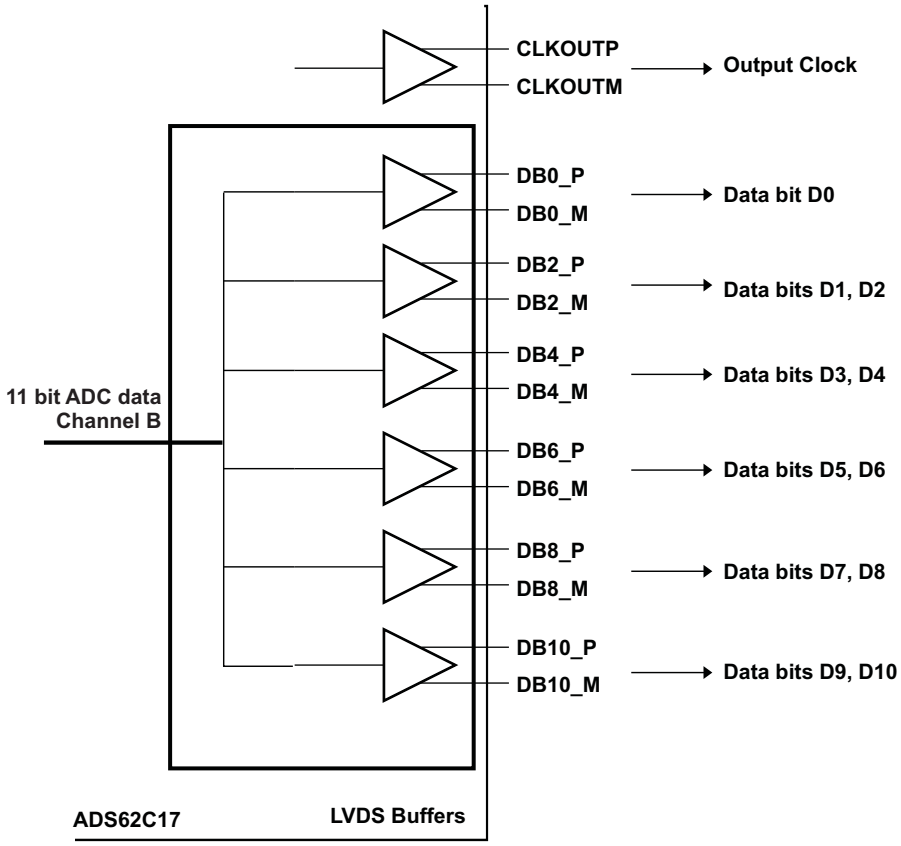



**Figure 57. DDR LVDS Outputs**

Even data bits D0, D2, D4… are output at the falling edge of CLKOUTP and the odd data bits D1, D3, D5… are output at the rising edge of CLKOUTP. Both the rising and falling edges of CLKOUTP have to be used to capture all the data bits (Figure 58).

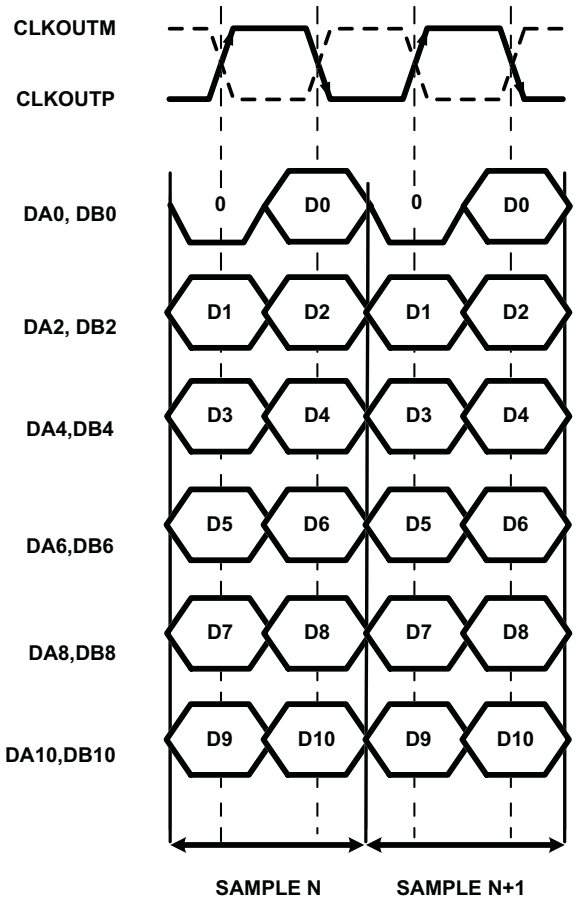



**Figure 58. DDR LVDS Interface**

### LVDS Buffer

The equivalent circuit of each LVDS output buffer is shown in Figure 59. The buffer is designed to present an output impedance of 100Ω (Rout). The differential outputs can be terminated at the receive end by a 100Ω termination.

The buffer output impedance behaves like a source-side series termination. By absorbing reflections from the receiver end, it helps to improve signal integrity. Note that this internal termination cannot be disabled and its value cannot be changed.

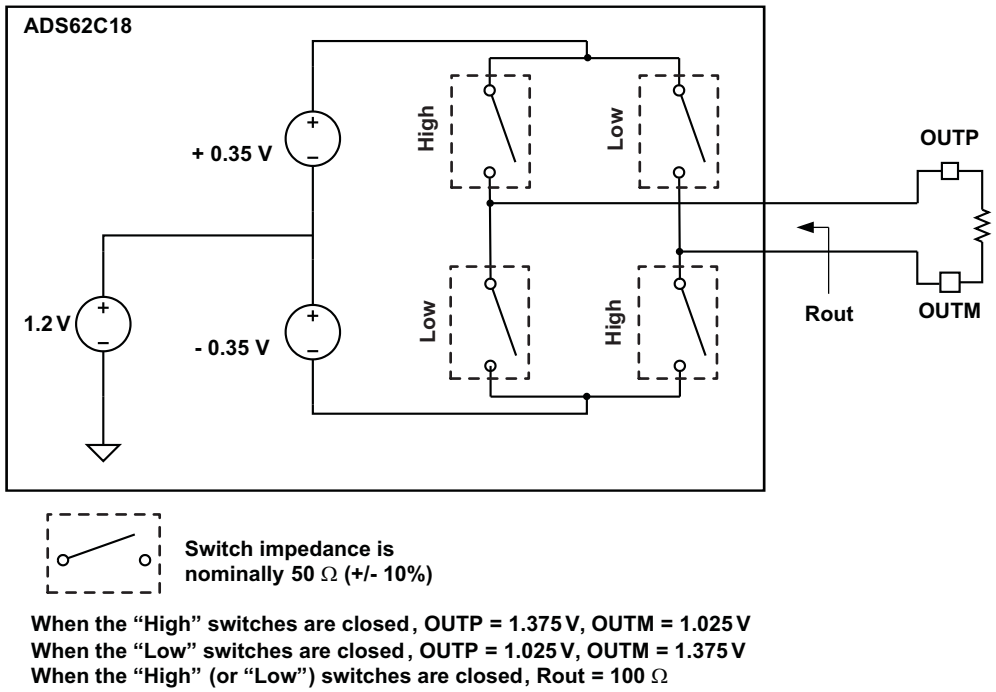



**Figure 59. LVDS Buffer Equivalent Circuit**

### Parallel CMOS Interface

In the CMOS mode, each data bit is output on separate pin as CMOS voltage level, every clock cycle. The rising edge of the output clock CLKOUT can be used to latch data in the receiver ***(for sampling frequencies up to 150 MSPS)***.

Up to 150MSPS, the setup and hold timings of the output data with respect to CLKOUT are specified. It is recommended to minimize the load capacitance seen by data and clock output pins by using short traces to the receiver. Also, match the output data and clock traces to minimize the skew between them.

***For sampling frequencies above 150 MSPS,*** it is recommended to use an external clock to capture data. The delay from input clock to output data and the data valid times are specified for the higher sampling frequencies. These timings can be used to delay the input clock appropriately and use it to capture the data.

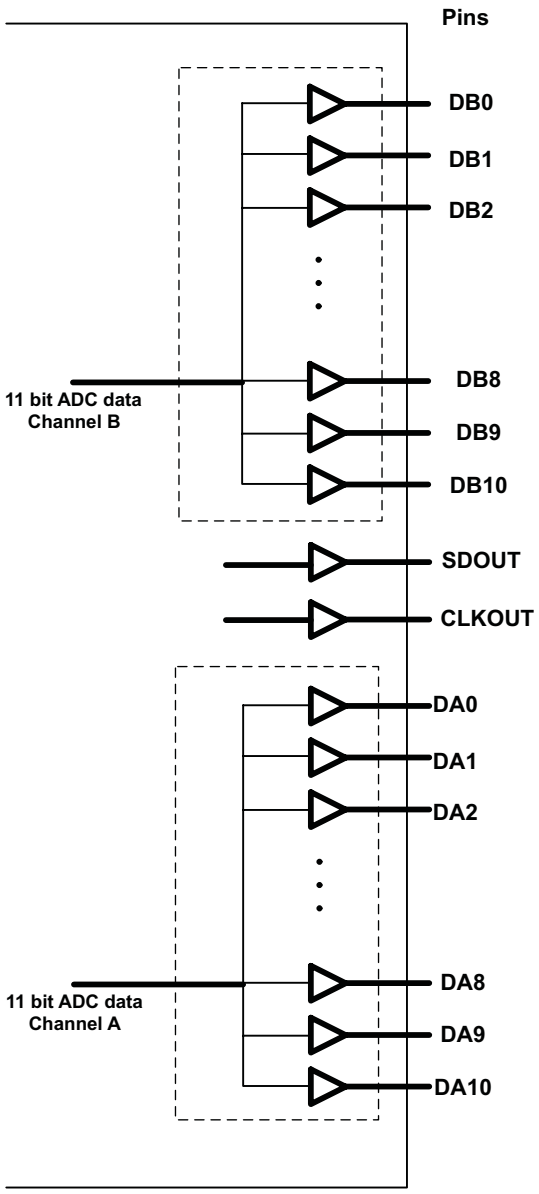



**Figure 60. Parallel CMOS Outputs**

### CMOS Interface Power Dissipation

With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output pin. The maximum DRVDD current occurs when each output bit toggles between 0 and 1 every clock cycle. In actual applications, this condition is unlikely to occur. The actual DRVDD current would be determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal.

Digital current due to CMOS output switching = $C_L \times DRVDD \times (N \times F_{AVG})$,

where $C_L$ = load capacitance, $N \times F_{AVG}$ = average number of output bits switching.

Figure 38 shows the current with various load capacitances across sampling frequencies at 2 MHz analog input frequency.

### Output Data Format

Two output data formats are supported – 2s complement and offset binary. They can be selected using the serial interface register bit **<DATA FORMAT>** or controlling the DFS pin in parallel configuration mode.

In the event of an input voltage overdrive, the digital outputs go to the appropriate full scale level. For a positive overdrive, the output code is 0x7FF in offset binary output format, and 0x3FF in 2s complement output format. For a negative input overdrive, the output code is 0x000 in offset binary output format and 0x400 in 2s complement output format.

## BOARD DESIGN CONSIDERATIONS

### Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See the EVM User Guide (SLAU237A) for details on layout and grounding.

### Supply Decoupling

As ADS62C17 already includes internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help filter external power supply noise, so the optimum number of capacitors would depend on the actual application. The decoupling capacitors should be placed very close to the converter supply pins.

### Exposed Pad

In addition to providing a path for heat dissipation, the pad is also electrically connected to digital ground internally. So, it is necessary to solder the exposed pad to the ground plane for best thermal and electrical performance. For detailed information, see application notes *QFN Layout Guidelines* (SLOA122) and **QFN/SON**.

**PCB Attachment** (SLUA271).

## MIGRATION FROM ADS62C15 TO ADS62C17

While migrating from the C15 to C17, note the following differences between the two devices.

| ADS62C15 | ADS62C17 |
|---|---|
| **Pinout** | |
| Pin 22 is AGND | Pin 22 is NC |
| Pin 64 is DRGND | Pin 64 is SDOUT (Serial readout pin) |
| **Supply** | |
| AVDD is 3.3V | No change |
| DRVDD is 1.8V to 3.3V (for CMOS interface) and is 3.3V (for LVDS interface) | DRVDD is 1.8V (for both CMOS and LVDS interfaces) |
| **Serial Interface** | |
| Protocol: 8 bit register address & 8 bit register data | No change in protocol |
| | Serial register map is completely different |

## DEFINITION OF SPECIFICATIONS

**Analog Bandwidth –** The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

**Aperture Delay –** The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay will be different across channels. The maximum variation is specified as aperture delay variation (channel-channel).

**Aperture Uncertainty (Jitter) –** The sample-to-sample variation in aperture delay.

**Clock Pulse Width/Duty Cycle –** The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

**Maximum Conversion Rate –** The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

**Minimum Conversion Rate –** The minimum sampling rate at which the ADC functions.

**Differential Nonlinearity (DNL) –** An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

**Integral Nonlinearity (INL) –** The INL is the deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

**Gain Error –** Gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error due to reference inaccuracy and error due to the channel. Both these errors are specified independently as $E_{GREF}$ and $E_{GCHAN}$.

To a first order approximation, the total gain error will be $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$.

For example, if $E_{TOTAL} = \pm 0.5\%$, the full-scale input varies from $(1\text{-}0.5/100) \times FS_{ideal}$ to $(1 + 0.5/100) \times FS_{ideal}$.

**Offset Error –** The offset error is the difference, given in number of LSBs, between the ADC's actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into mV.

**Temperature Drift –** The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from $T_{MIN}$ to $T_{MAX}$. It is calculated by dividing the maximum deviation of the parameter across the $T_{MIN}$ to $T_{MAX}$ range by the difference $T_{MAX}–T_{MIN}$.

**Signal-to-Noise Ratio –** SNR is the ratio of the power of the fundamental (PS) to the noise floor power (PN), excluding the power at DC and the first nine harmonics.

$$SNR = 10Log^{10} \frac{P_S}{P_N} \quad (3)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

**Signal-to-Noise and Distortion (SINAD) –** SINAD is the ratio of the power of the fundamental ($P_S$) to the power of all the other spectral components including noise ($P_N$) and distortion ($P_D$), but excluding dc.

$$SINAD = 10Log^{10} \frac{P_S}{P_N + P_D} \quad (4)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

**Effective Number of Bits (ENOB) –** The ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (5)$$

**Total Harmonic Distortion (THD) –** THD is the ratio of the power of the fundamental ($P_S$) to the power of the first nine harmonics (PD).

$$THD = 10Log^{10} \frac{P_S}{P_N} \quad (6)$$

THD is typically given in units of dBc (dB to carrier).

**Spurious-Free Dynamic Range (SFDR) –** The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

**Two-Tone Intermodulation Distortion –** IMD3 is the ratio of the power of the fundamental (at frequencies f1 and f2) to the power of the worst spectral component at either frequency 2f1–f2 or 2f2–f1. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

**DC Power Supply Rejection Ratio (DC PSRR) –** The DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The DC PSRR is typically given in units of mV/V.

**AC Power Supply Rejection Ratio (AC PSRR) –** AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If $\Delta V_{SUP}$ is the change in supply voltage and ΔVout is the resultant change of the ADC output code (referred to the input), then

$$PSRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \text{ (Expressed in dBc)} \quad (7)$$

**Voltage Overload Recovery –** The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This is tested by separately applying a sine wave signal with 6dB positive and negative overload. The deviation of the first few samples after the overload (from their expected values) is noted.

**Common Mode Rejection Ratio (CMRR) –** CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If ΔVcm_in is the change in the common-mode voltage of the input pins and $\Delta V_{OUT}$ is the resultant change of the ADC output code (referred to the input), then

$$CMRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{CM}} \text{ (Expressed in dBc)} \quad (8)$$

**Cross-Talk (only for multi-channel ADC)–** This is a measure of the internal coupling of a signal from adjacent channel into the channel of interest. It is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from channel across the package (far-channel). It is usually measured by applying a full-scale signal in the adjacent channel. Cross-talk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. It is typically expressed in dBc.

## Revision History

**Changes from Original (April 2009) to Revision A** **Page**

- Added missing Value ..... 9
- Added paragraph - This disables any further writes into the registers, EXCEPT the register at address 0. Note that the <SERIAL READOUT> bit is also located in register 0. The device can exit readout mode by writing <SERIAL READOUT> to 0. Also, only the ..... 15
- Changed To - To exit the serial readout mode, reset register bit <SERIAL READOUT> =0, which enables writes into all registers of the device. ..... 15
- Changed Normalized Corner Frequencies changed to fix error with respect to the mapping between the SNRBoost coefficient value and normalized corner frequency (f/fs). ..... 48
- Changed values for Normalized Corner Frequency1, 2, and center frequency ..... 49

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS62C17IRGCR | ACTIVE | VQFN | RGC | 64 | 2000 | RoHS & Green | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ62C17 | Samples |
| ADS62C17IRGCT | ACTIVE | VQFN | RGC | 64 | 250 | RoHS & Green | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ62C17 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

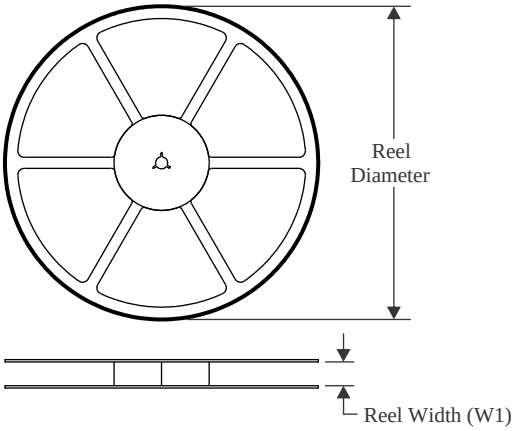
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

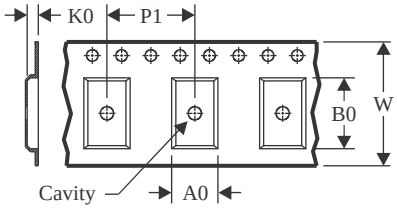
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

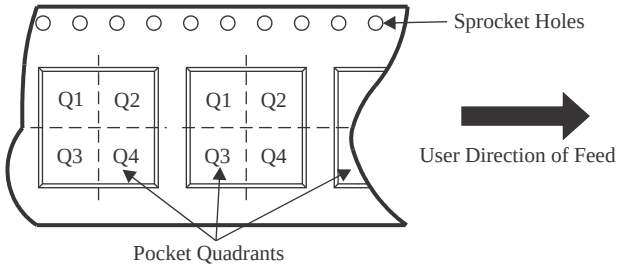



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

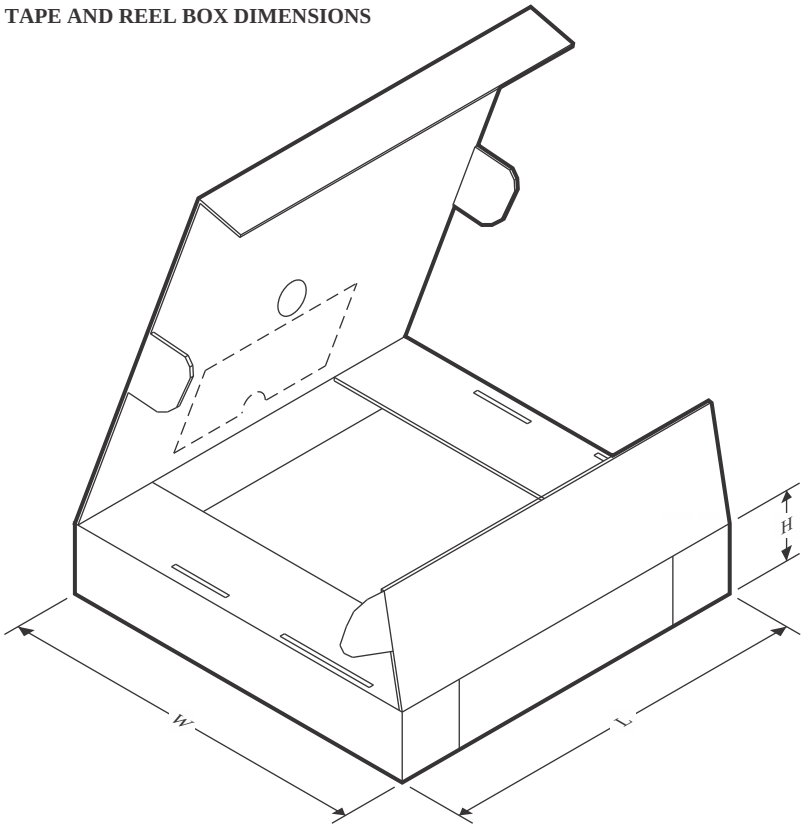
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS62C17IRGCR | VQFN | RGC | 64 | 2000 | 330.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ADS62C17IRGCR | VQFN | RGC | 64 | 2000 | 350.0 | 350.0 | 43.0 |

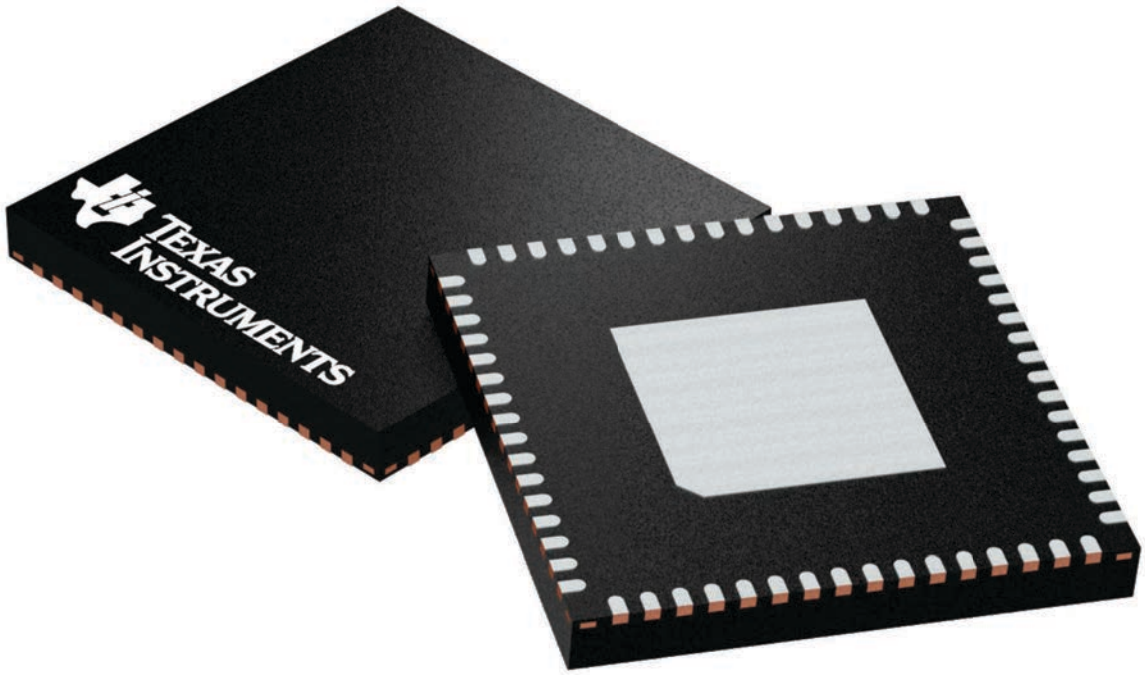
# GENERIC PACKAGE VIEW

## RGC 64

## VQFN - 1 mm max height

**9 x 9, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

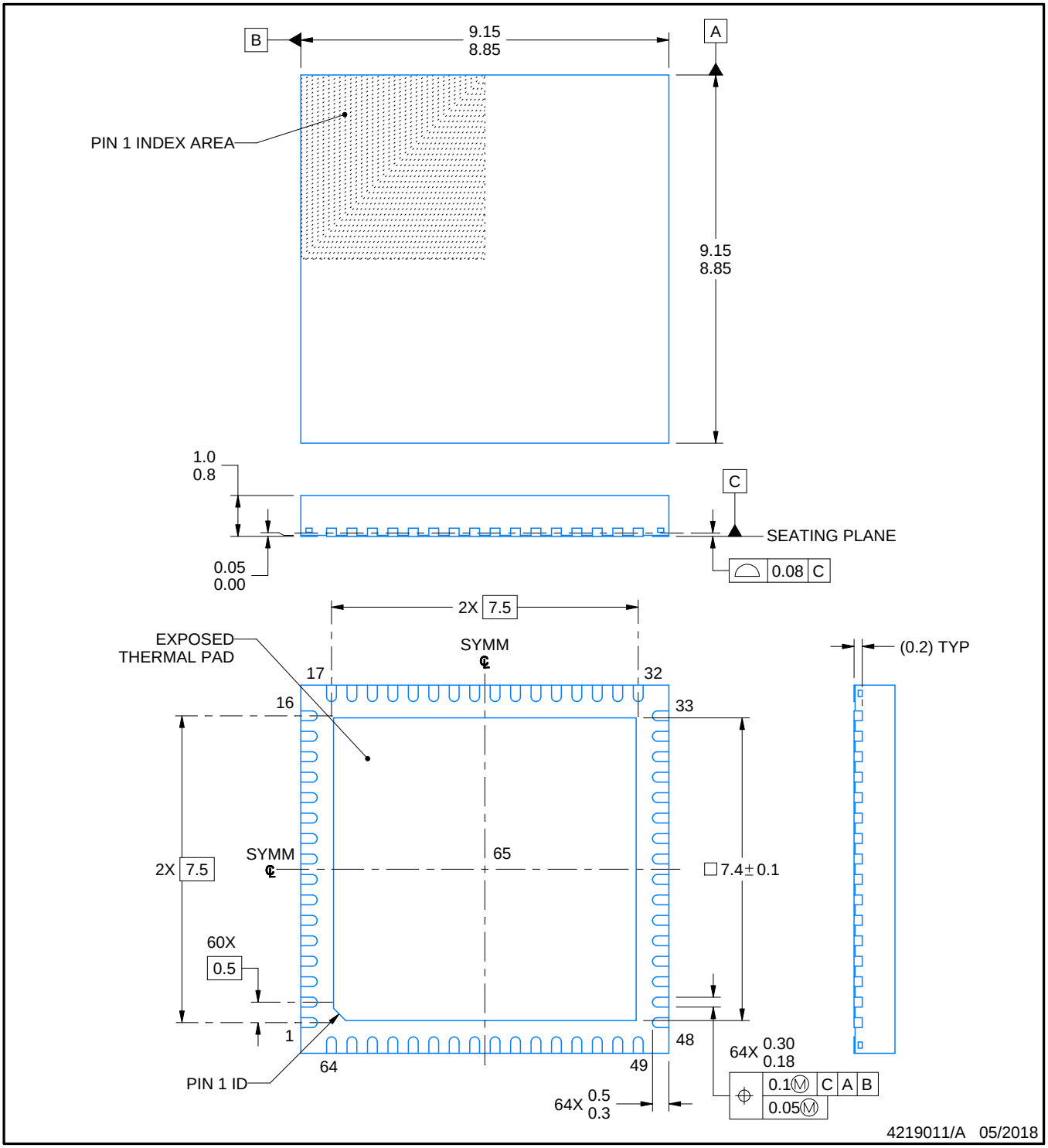
4224597/A

# RGC0064H

# PACKAGE OUTLINE

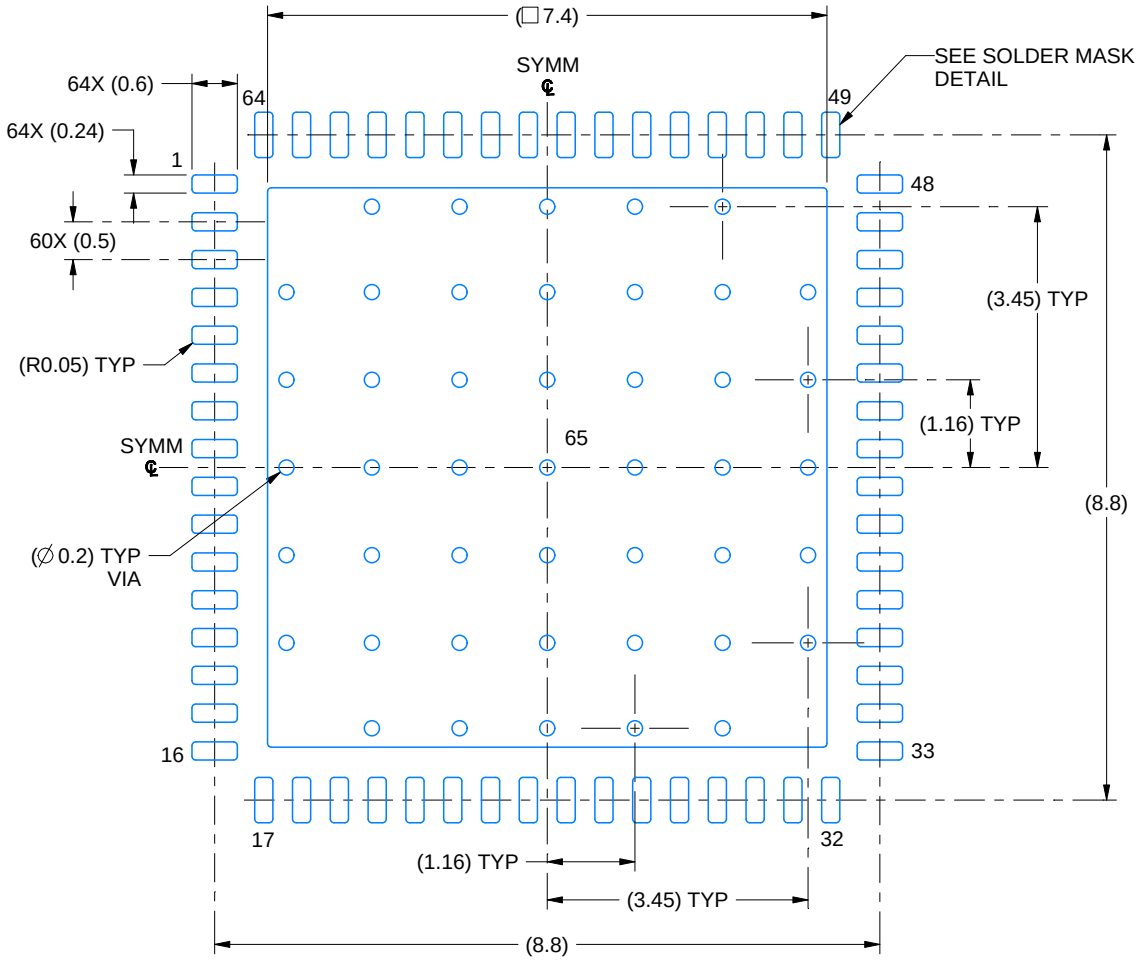
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

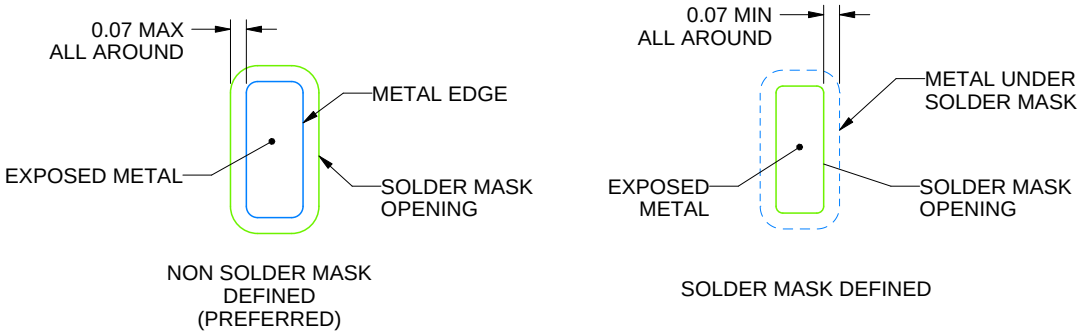



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

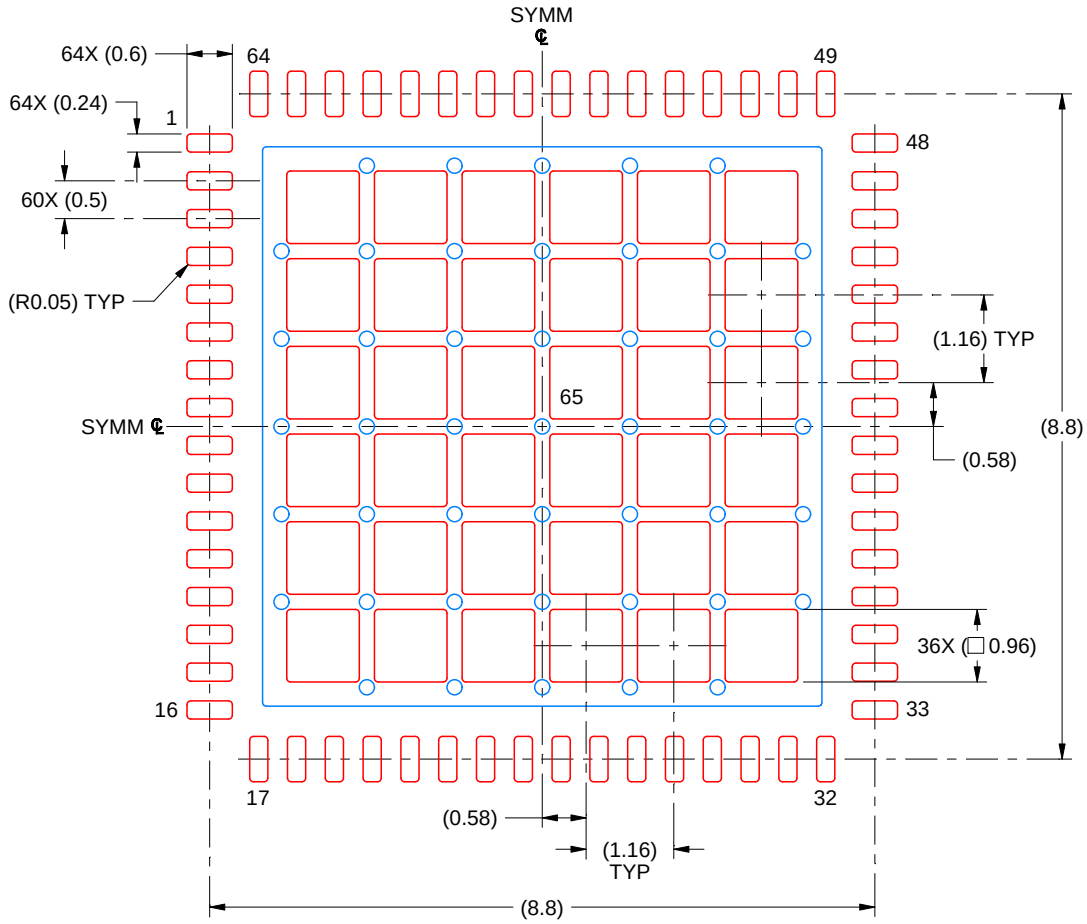



SOLDER MASK DETAILS

4219011/A 05/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
61% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219011/A 05/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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