

ADS52J91 具有 LVDS、JESD 输出的 10 位、12 位、14 位多通道低功耗高速 ADC

1 特性

- 16 通道 ADC，可配置为对 8、16 或 32 路输入进行转换
- 最大 ADC 转换速率：
 - 10 位模式下为 125MSPS
 - 12 位模式下为 100MSPS
 - 14 位模式下为 65MSPS
- 电源：1.2 V/1.8 V
- 差分或单端输入时钟
- 信噪比 (SNR)：
 - 10 位模式下为 61dBFS
 - 12 位模式下为 69dBFS
 - 14 位模式下为 73.5dBFS
- 125MSPS 时的功耗：48.6mW/通道
- 16 个 ADC 经配置可进行下列转换：
 - 8 路输入，采样率为 ADC 转换速率的 2 倍
 - 16 路输入，采样率与 ADC 转换速率相同
 - 32 路输入，采样率为 ADC 转换速率的一半
- 支持 10/12/14/16 倍串行化的 1Gbps LVDS 接口
- 5Gbps JESD 接口：
 - JESD204B 子类 0、1 和 2
 - 每个 JESD 信道包含 2、4 或 8 个通道
- 封装：NFBGA-198 (9mm × 15mm)

2 应用

- 超声波成像
- 便携式仪表
- 声纳和雷达
- 高速多通道数据采集

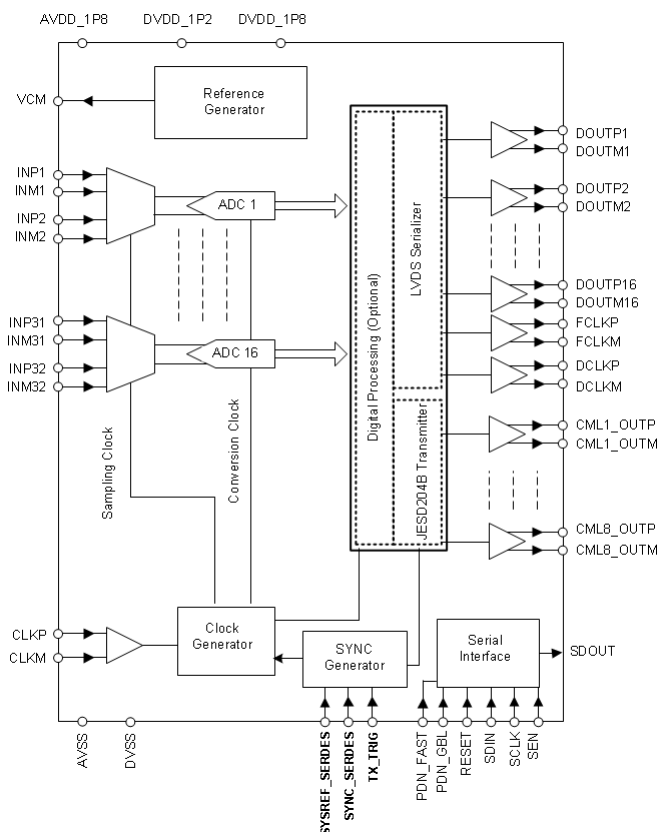
3 说明

ADS52J91 是一款低功耗、高性能、16 通道的模数转换器 (ADC)。每个 ADC 在 10 位模式下的转换速率可高达 125MSPS。ADC 分辨率越高，最高转换速率越低。

该器件可配置为接受 8、16 或 32 个输入。在 32 位模式下，每个 ADC 以值为 ADC 转换速率一半的有效采样率对两个不同输入交替进行采样并转换。在 8 位输入模式下，两个 ADC 以交错方式对同一输入进行转换，这种情况下的有效采样率为 ADC 转换速率的 2 倍。ADC 设计为根据转换速率调整其功耗。

器件信息

器件型号	封装	封装尺寸 (标称值)
ADS52J91	NFBGA (198)	9.00mm × 15.00mm



简化版原理图



4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
September 2021	*	Initial Release

5 说明 (续)

ADC 输出会进行串行化，并与帧时钟和高速位时钟一起通过低压差分信令 (LVDS) 接口输出。

该器件还具有一个可选的 JESD204B 接口，同时可在 16 输入和 32 输入模式下工作。该接口的运行速率最高可达 5Gbps

该器件采用间距为 0.8mm 的 9mm × 15mm NFBGA-198 封装

6 Device and Documentation Support

6.1 Documentation Support

6.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6.4 Trademarks

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6.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS52J91ZZE	Active	Production	NFBGA (ZZE) 198	160 JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	0 to 70	ADS52J91
ADS52J91ZZE.A	Active	Production	NFBGA (ZZE) 198	160 JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	0 to 70	ADS52J91

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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