ADS1204 4 个 1 位、10MHz、2 阶、Δ-Σ 调制器

1 特性

- 16 位分辨率
- 14 位线性
- 分辨率与速度之间的折衷：
  10 位有效分辨率，信号延迟为 10µs（12 位时为 19µs）
- 2.5V 时输入范围为 ±2.5V
- 内部基准电压：2%
- 增益误差：0.5%
- 4 个独立的 Δ-Σ 调制器
- 4 个输入基准缓冲器
- 板载 20MHz 振荡器
- 可选择的内部或外部时钟
- 工作温度范围：
  –40°C 至 +105°C
- 封装：VQFN-32 (5mm × 5mm)

2 应用

- 电机控制
- 电流测量
- 工业过程控制
- 智能发送器
- 称重秤
- 压力传感器
- 便携式仪器
- 仪表

3 说明

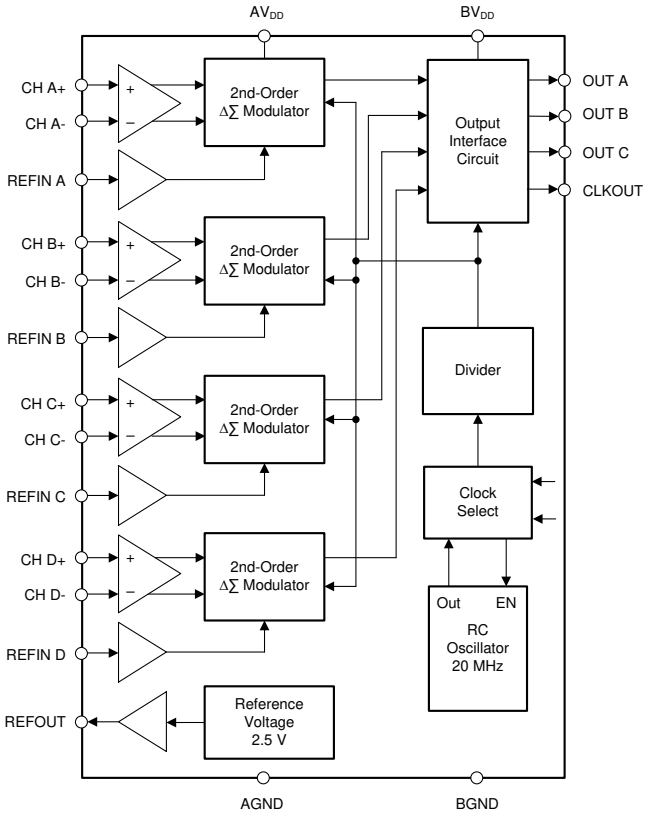
ADS1204 是一款四通道高性能器件，具有四个动态范围为 100dB 的 ΔΣ 调制器，由 5V 单电源供电。差分输入非常适合直接连接到工业环境中的传感器。借助适当的数字滤波器和调制器速率，该器件可用于在无丢码的情况下实现 16 位模数 (A/D) 转换。在 10MHz 的调制器速率下，使用 160kHz 的数字滤波器数据速率可以获得 12 位的有效分辨率。ADS1204 专为中高分辨率测量应用而设计，这些 应用 包括电流测量、智能变送器、工业过程控制、称重秤、色谱分析和便携式仪器。该器件采用 VQFN-32 (5×5) 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ADS1204	VQFN (32)	5.00mm × 5.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

功能方框图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (February 2009) to Revision D **Page**

- 已添加 添加了*器件信息* 表、第 1 页的图、*ESD 额定值* 表、*热性能信息* 表、*概述* 部分、*功能方框图* 部分、*特性 说明* 部分、*器件功能模式* 部分、*应用和实施* 部分、*电源建议* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1
- 已更改 通篇将 QFN 更改为 VQFN ... 1
- 已更改 更改了*应用* 部分 ... 1
- Deleted *Ordering Information* table ... 5
- Changed *Power dissipation* to point to *Thermal Information* table instead, added unit ... 5
- Changed *External clock* maximum specification from 24 MHz to 32 MHz in *Recommended Operating Conditions* table ... 6
- Changed footnote in *Recommended Operating Conditions* table ... 6
- Deleted *Dissipation Ratings* table ... 6
- Changed *External clock frequency* maximum specification from 24 MHz to 32 MHz in *Electrical Characteristics* table ... 7
- Changed *CLKIN period* minimum specification from 41.6 ns to 31.25 ns in *Timing Requirements: 5.0 V* table ... 9
- Changed NOM column to MAX column in *Timing Requirements: 5.0 V* table ... 9
- Changed BV_{DD} from 5 V to 3 V in *Timing Requirements: 3.0 V* test conditions ... 9
- Changed *CLKIN period* minimum specification from 41.6 ns to 31.25 ns in *Timing Requirements: 3.0 V* table ... 9
- Changed *Layout* section ... 22

Changes from Revision B (August 2007) to Revision C **Page**

- 更新了文档格式 ... 1
- 通篇将工作温度范围从 +85°C 扩展为 +105°C ... 1
- Deleted operating free-air temperature range row from *Absolute Maximum Ratings* table ... 5
- Added free-air temperature range ratings to *Recommended Operating Conditions* table ... 6
- Changed *Dissipation Ratings* table ... 6
- Changed typical specification in *Input capacitance* row of *Analog Input* section of *Electrical Characteristics* table ... 6
- Added additional specification for Total Harmonic Distortion in *AC Accuracy* section of *Electrical Characteristics* table ... 6
- Deleted test condition of V_{OUT} row in *Voltage Reference Output* section of *Electrical Characteristics* table ... 6

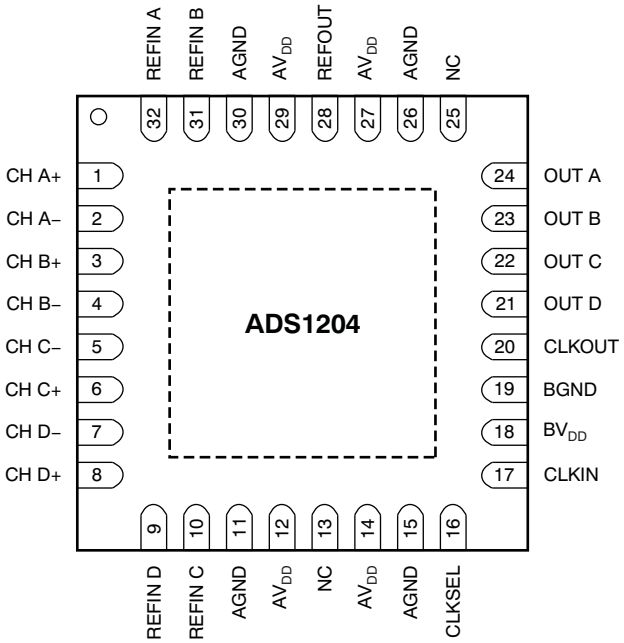
- Updated typical characteristic graphs to reflect extended temperature range 10

Changes from Revision A (June 2004) to Revision B **Page**

- Added note to QFN package 4

5 Pin Configuration and Functions

RHB Package
32-Pin VQFN
Top View



NOTE: The thermal pad is internally connected to the substrate. This pad can be connected to the analog ground or left floating. Keep the thermal pad separate from the digital ground, if possible.

Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
CH A+	1	AI	Analog input of channel A: noninverting input
CH A–	2	AI	Analog input of channel A: inverting input
CH B+	3	AI	Analog input of channel B: noninverting input
CH B–	4	AI	Analog input of channel B: inverting input
CH C–	5	AI	Analog input of channel C: inverting input
CH C+	6	AI	Analog input of channel C: noninverting input
CH D–	7	AI	Analog input of channel D: inverting input
CH D+	8	AI	Analog input of channel D: noninverting input
REFIN D	9	AI	Reference voltage input of channel D: pin for external reference voltage
REFIN C	10	AI	Reference voltage input of channel C: pin for external reference voltage
AGND	11	—	Analog ground
AVDD	12	P	Analog power supply; nominal 5 V
NC	13	—	No connection; this pin is left unconnected
AV_{DD}	14	P	Analog power supply; nominal 5 V
AGND	15	—	Analog ground
CLKSEL	16	I	Clock select between internal clock (CLKSEL = 1) or external clock (CLKSEL = 0)
CLKIN	17	I	External clock input
BV_{DD}	18	P	Digital interface power supply; from 2.7 V to 5.5 V
BGND	19	—	Interface ground
CLKOUT	20	O	System clock output

(1) AI = analog input; AO = analog output; I = input; O = output; P = power supply.

Pin Functions (continued)

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
OUT D	21	O	Bit stream from channel D modulator
OUT C	22	O	Bit stream from channel C modulator
OUT B	23	O	Bit stream from channel B modulator
OUT A	24	O	Bit stream from channel A modulator
NC	25	—	No connection; this pin is left unconnected
AGND	26	—	Analog ground
AV_{DD}	27	P	Analog power supply; nominal 5 V
REFOUT	28	AO	Reference voltage output: output pin of the internal reference source; nominal 2.5 V
AV_{DD}	29	P	Analog power supply; nominal 5 V
AGND	30	—	Analog ground
REFIN B	31	AI	Reference voltage input of channel B: pin for external reference voltage
REFIN A	32	AI	Reference voltage input of channel A: pin for external reference voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage	AV_{DD} to AGND	–0.3	6	V
	BV_{DD} to BGND	–0.3	6	
Analog input voltage with respect to AGND		AGND – 0.3	AV_{DD} + 0.3	V
Reference input voltage with respect to AGND		AGND – 0.3	AV_{DD} + 0.3	V
Digital input voltage with respect to BGND		BGND – 0.3	BV_{DD} + 0.3	V
Ground voltage difference, AGND to BGND			±0.3	V
Voltage differences, BV_{DD} to AGND		–0.3	6	V
Input current to any pin except supply			±10	mA
Power dissipation		See the *Thermal Information*		A
Temperature	Operating virtual junction, T_J	–40	+150	°C
	Storage, T_{stg}	–65	+150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, AVDD to AGND		4.75	5	5.25	V
Supply voltage, BVDD to BGND	Low-voltage levels	2.7		3.6	V
	5V logic levels	4.5	5	5.5	V
Reference input voltage		0.5	2.5	2.6	V
Operating common-mode signal		0		AV_{DD}	V
Analog inputs	+IN – (–IN)	0		±REFIN	V
External clock(1)		16	20	32	MHz
Operating free-air temperature range, T_A		–40		+125	°C
Specified free-air temperature range, T_A		–40		+105	°C

(1) Analog performance is degraded at clock frequencies > 20 MHz; see the *Typical Characteristics* section for details.

6.4 Thermal Information

THERMAL METRIC(1)		ADS1204 RHB (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	28.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range at –40°C to +105°C, AV_{DD} = 5 V, BV_{DD} = 3 V, CH x+ = 0.5 V to 4.5 V, CH x– = 2.5 V, REFIN = REFOUT = internal 2.5 V, CLKIN = 20 MHz, and 16-bit $sinc^3$ filter with decimation by 256 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
RESOLUTION						
	Resolution		16			Bits
DC ACCURACY						
INL	Integral linearity error(2)			±1	±3	LSB
				±0.001	±0.005	% FSR
	Integral linearity match				±6	LSB
					±0.009	% FSR
DNL	Differential nonlinearity(3)				±1	LSB
V_{OS}	Input offset error			–1.4	±3	mV
	Input offset error match				±2	mV
TCV_{OS}	Input offset error drift			±2	±8	µV/°C
G_{ERR}	Gain error(4)	Referenced to V_{REF}		±0.08	±0.5	% FSR
	Gain error match			±0.185	±0.5	% FSR
TCG_{ERR}	Gain error drift			±2		ppm/°C
PSRR	Power-supply rejection ratio	4.75 V < AV_{DD} < 5.25 V		78		dB

(1) All typical values are at T_A = +25°C.
(2) Integral nonlinearity is defined as the maximum deviation of the line through the end points of the specified input range of the transfer curve for CH x+ = –2 V to +2 V at 2.5 V, expressed either as the number of LSBs or as a percent of measured input range (4 V).
(3) Specified by design.
(4) Maximum values, including temperature drift, are specified over the full specified temperature range.

Electrical Characteristics (continued)

over recommended operating free-air temperature range at –40°C to +105°C, AV_{DD} = 5 V, BV_{DD} = 3 V, CH x+ = 0.5 V to 4.5 V, CH x– = 2.5 V, REFIN = REFOUT = internal 2.5 V, CLKIN = 20 MHz, and 16-bit $sinc^3$ filter with decimation by 256 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
ANALOG INPUT						
FSR	Full-scale differential range	(CH x+) – (CH x–); CH x– = 2.5 V			±2.5	V
	Specified differential range	(CH x+) – (CH x–); CH x– = 2.5 V			±2	V
	Maximum operating input range(3)		0		AV_{DD}	V
	Input capacitance	Common-mode		1.5		pF
	Input leakage current	CLK turned off			±1	nA
	Differential input resistance			100		kΩ
	Differential input capacitance			2.5		pF
CMRR	Common-mode rejection ratio	At DC		100		dB
		V_{IN} = ±1.25 V_{PP} at 40 kHz		110		
BW	Bandwidth	FS sine wave, –3 dB		50		MHz
SAMPLING DYNAMICS						
	Internal clock frequency	CLKSEL = 1	8	10	12	MHz
CLKIN	External clock frequency	CLKSEL = 0	1	20	32	MHz
AC ACCURACY						
THD	Total harmonic distortion	V_{IN} = ±2 V_{PP} at 5 kHz; –40°C ≤ T_A ≤ +85°C		–96	–88	dB
		V_{IN} = ±2 V_{PP} at 5 kHz; –40°C ≤ T_A ≤ +105°C		–96	–87	
SFDR	Spurious-free dynamic range	V_{IN} = ±2 V_{PP} at 5 kHz	92	100		dB
SNR	Signal-to-noise ratio	V_{IN} = ±2 V_{PP} at 5 kHz	86	89		dB
SINAD	Signal-to-noise + distortion	V_{IN} = ±2 V_{PP} at 5 kHz	85	89		dB
	Channel-to-channel isolation(3)	V_{IN} = ±2 V_{PP} at 50 kHz		85		dB
ENOB	Effective number of bits		14	14.5		Bits
VOLTAGE REFERENCE OUTPUT						
V_{OUT}	Reference voltage output		2.450	2.5	2.550	V
dV_{OUT}/dT	Output voltage temperature drift			±20		ppm/°C
	Output voltage noise	f = 0.1 Hz to 10 Hz, C_L = 10 µF		10		µVrms
		f = 10 Hz to 10 kHz, C_L = 10 µF		12		
PSRR	Power-supply rejection ratio			60		dB
I_{OUT}	Output current			10		µA
I_{SC}	Short-circuit current			0.5		mA
	Turn-on settling time	To 0.1% at C_L = 0		100		µs
VOLTAGE REFERENCE INPUT						
V_{IN}	Reference voltage input		0.5	2.5	2.6	V
	Reference input resistance			100		MΩ
	Reference input capacitance			5		pF
	Reference input current				1	µA
DIGITAL INPUTS(5)						
	Logic family		CMOS with Schmitt Trigger			
V_{IH}	High-level input voltage		0.7 × BV_{DD}		BV_{DD} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 × BV_{DD}	V
I_{IN}	Input current	V_I = BV_{DD} or GND			±50	nA
C_I	Input capacitance			5		pF

(5) Applicable for 5.0-V nominal supply: BV_{DD} (min) = 4.5 V and BV_{DD} (max) = 5.5 V.

Electrical Characteristics (continued)

over recommended operating free-air temperature range at –40°C to +105°C, AV_{DD} = 5 V, BV_{DD} = 3 V, CH x+ = 0.5 V to 4.5 V, CH x– = 2.5 V, REFIN = REFOUT = internal 2.5 V, CLKIN = 20 MHz, and 16-bit $sinc^3$ filter with decimation by 256 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
DIGITAL OUTPUTS(5)						
	Logic family			CMOS		
V_{OH}	High-level output voltage	BV_{DD} = 4.5 V, I_{OH} = –100 µA	4.44			V
V_{OL}	Low-level output voltage	BV_{DD} = 4.5 V, I_{OL} = 100 µA			0.5	V
C_O	Output capacitance			5		pF
C_L	Load capacitance				30	pF
	Data format			Bit stream		
DIGITAL INPUTS(6)						
	Logic family			LVCMOS		
V_{IH}	High-level input voltage	BV_{DD} = 3.6 V	2		BV_{DD} + 0.3	V
V_{IL}	Low-level input voltage	BV_{DD} = 2.7 V	–0.3		0.8	V
I_{IN}	Input current	V_I = BV_{DD} or GND			±50	nA
C_I	Input capacitance			5		pF
DIGITAL OUTPUTS(6)						
	Logic family			LVCMOS		
V_{OH}	High-level output voltage	BV_{DD} = 2.7V, I_{OH} = –100 µA	BV_{DD} – 0.2			V
V_{OL}	Low-level output voltage	BV_{DD} = 2.7 V, I_{OL} = 100 µA			0.2	V
C_O	Output capacitance			5		pF
C_L	Load capacitance				30	pF
	Data format			Bit stream		
POWER SUPPLY						
AV_{DD}	Analog supply voltage		4.5		5.5	V
BV_{DD}	Buffer I/O supply voltage	Low-voltage levels	2.7		3.6	V
		5-V logic levels	4.5		5.5	
AI_{DD}	Analog operating supply current	CLKSEL = 1		22.5	30	mA
		CLKSEL = 0		22.4	29	
BI_{DD}	Buffer I/O operating supply current	BV_{DD} = 3 V, CLKOUT = 10 MHz			4	mA
		BV_{DD} = 5 V, CLKOUT = 10 MHz			4	
	Power dissipation	CLKSEL = 0		122	145	mW
		CLKSEL = 1		112.5	150	

(6) Applicable for 3.0-V nominal supply: BV_{DD} (min) = 2.7 V and BV_{DD} (max) = 3.6 V.

6.6 Timing Requirements: 5.0 V(1)

over recommended operating free-air temperature range at –40°C to +105°C, AV_{DD} = 5 V, and BV_{DD} = 5 V (unless otherwise noted)

		MIN	MAX	UNIT
t_{C1}	CLKIN period	31.25	1000	ns
t_{W1}	CLKIN high time	10	t_{C1} – 10	ns
t_{C2}	CLKOUT period using internal oscillator (CLKSEL = 1)	83	125	ns
	CLKOUT period using external clock (CLKSEL = 0)	2 × t_{C1}		ns
t_{W2}	CLKOUT high time	(t_{C2} / 2) – 5	(t_{C2} / 2) + 5	ns
t_{D1}	CLKOUT rising edge delay after CLKIN rising edge	0	10	ns
t_{D2}	CLKOUT falling edge delay after CLKIN rising edge	0	10	ns
t_{D3}	Data valid delay after rising edge of CLKOUT (CLKSEL = 1)	(t_{C2} / 4) – 8	(t_{C2} / 4) + 8	ns
t_{D4}	Data valid delay after rising edge of CLKOUT (CLKSEL = 0)	t_{W1} – 3	t_{W1} + 7	ns

(1) Applicable for 5.0-V nominal supply: BV_{DD} (min) = 4.5 V and BV_{DD} (max) = 5.5 V. All input signals are specified with t_R = t_F = 5 ns (10% to 90% of BV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH}) / 2. See Figure 1.

6.7 Timing Requirements: 3.0 V(1)

over recommended operating free-air temperature range at –40°C to +105°C, AV_{DD} = 5 V, and BV_{DD} = 3 V (unless otherwise noted)

		MIN	MAX	UNIT
t_{C1}	CLKIN period	31.25	1000	ns
t_{W1}	CLKIN high time	10	t_{C1} – 10	ns
t_{C2}	CLKOUT period using internal oscillator (CLKSEL = 1)	83	125	ns
	CLKOUT period using external clock (CLKSEL = 0)	2 × t_{C1}		ns
t_{W2}	CLKOUT high time	(t_{C2} / 2) – 5	(t_{C2} / 2) + 5	ns
t_{D1}	CLKOUT rising edge delay after CLKIN rising edge	0	10	ns
t_{D2}	CLKOUT falling edge delay after CLKIN rising edge	0	10	ns
t_{D3}	Data valid delay after rising edge of CLKOUT (CLKSEL = 1)	(t_{C2} / 4) – 8	(t_{C2} / 4) + 8	ns
t_{D4}	Data valid delay after rising edge of CLKOUT (CLKSEL = 0)	t_{W1} – 3	t_{W1} + 7	ns

(1) Applicable for 3.0V nominal supply: BV_{DD} (min) = 2.7V and BV_{DD} (max) = 3.6V. All input signals are specified with t_R = t_F = 5ns (10% to 90% of BV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2. See Figure 1.

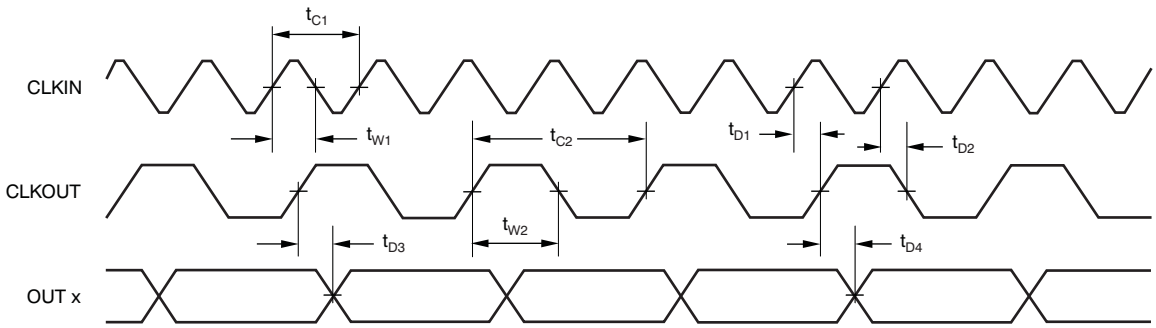


Figure 1. ADS1204 Timing Diagram

6.8 Typical Characteristics

AV_{DD} = 5 V, BV_{DD} = 3 V, CH x+ = 0.5 V to 4.5 V, CH x– = 2.5 V, REFIN = external, CLKSEL = 0, and 16-bit sinc^3 filter, with OSR = 256 (unless otherwise noted)

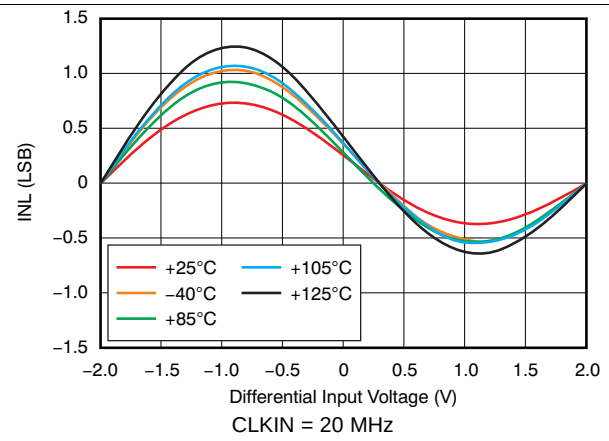


Figure 2. Integral Nonlinearity vs Input Signal

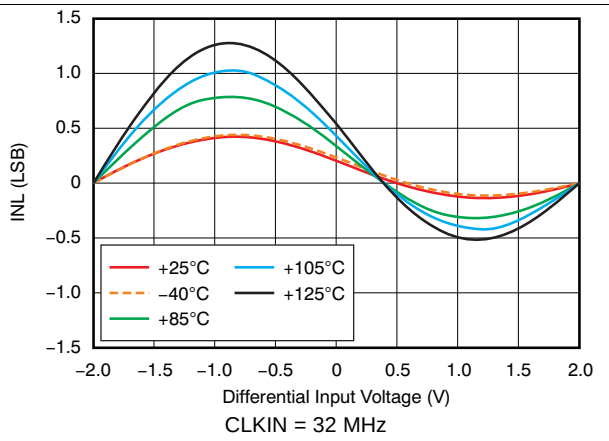


Figure 3. Integral Nonlinearity vs Input Signal

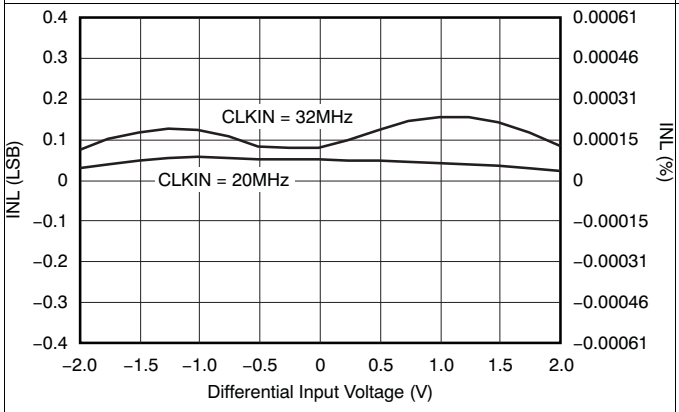


Figure 4. Integral Linearity Match of Channels vs Input Signal

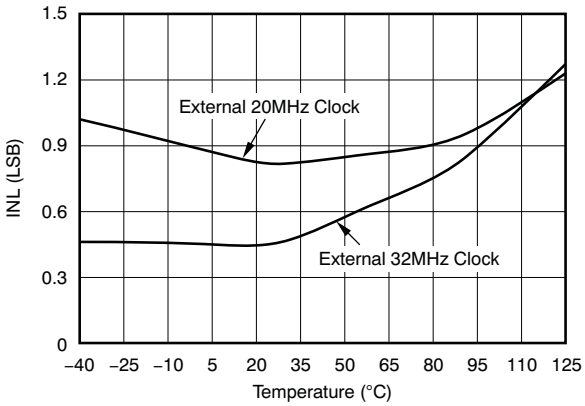


Figure 5. Maximum Integral Nonlinearity vs Temperature

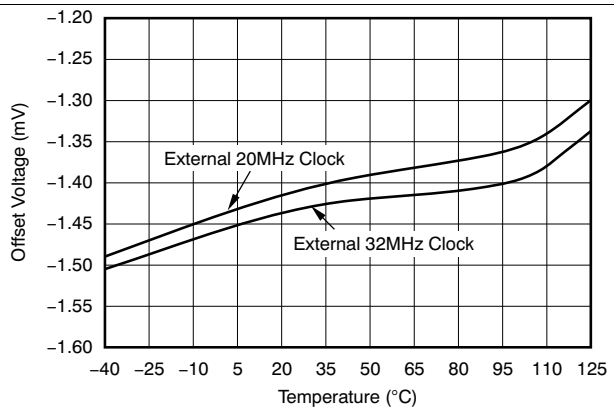


Figure 6. Offset vs Temperature

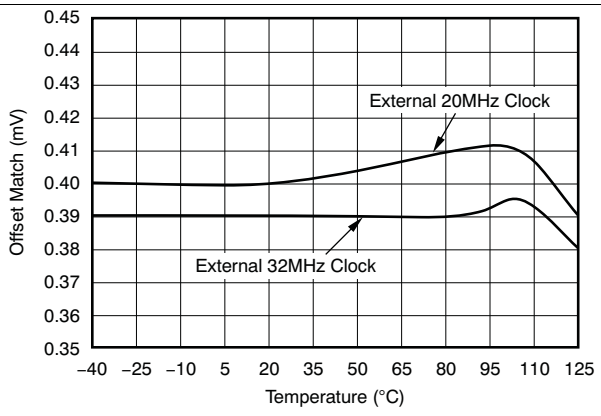


Figure 7. Offset Match vs Temperature

Typical Characteristics (continued)

AV_{DD} = 5 V, BV_{DD} = 3 V, CH x+ = 0.5 V to 4.5 V, CH x– = 2.5 V, REFIN = external, CLKSEL = 0, and 16-bit $sinc^3$ filter, with OSR = 256 (unless otherwise noted)

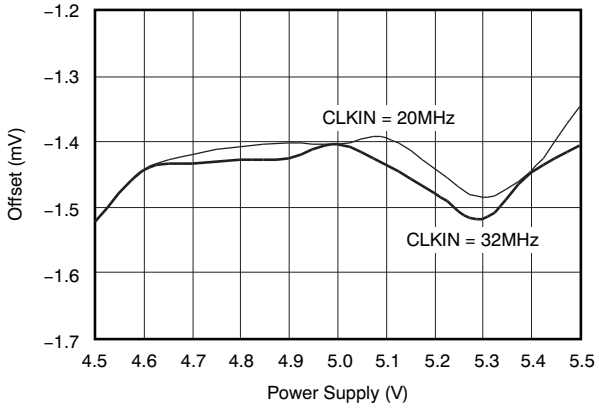


Figure 8. Offset vs Power Supply

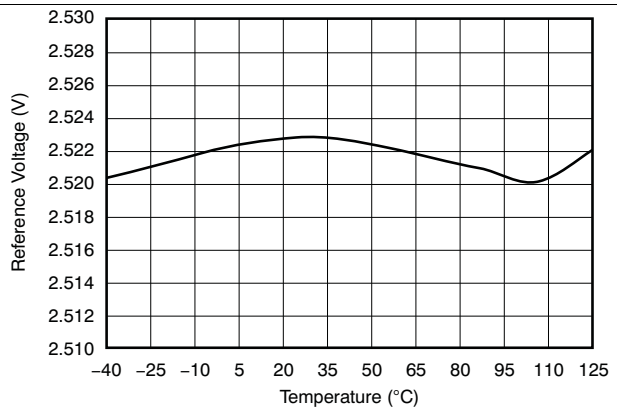


Figure 9. Internal Reference vs Temperature

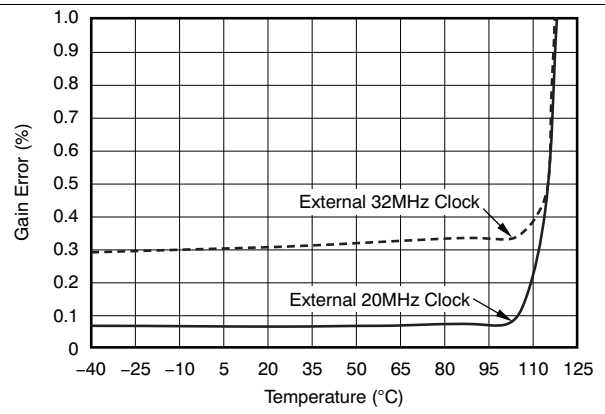


Figure 10. Gain Error vs Temperature

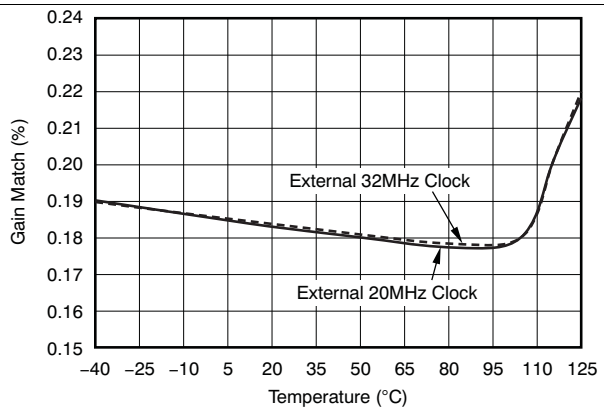


Figure 11. Gain Match vs Temperature

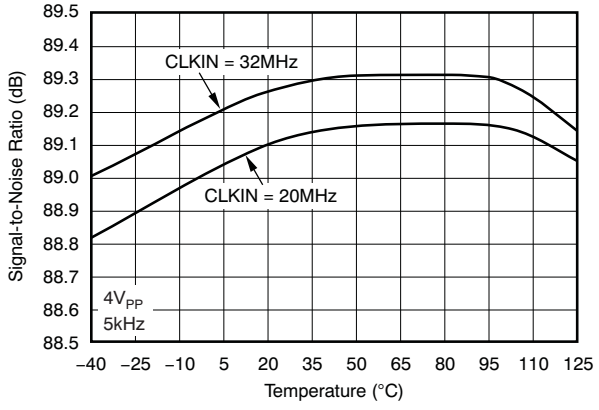


Figure 12. SNR vs Temperature

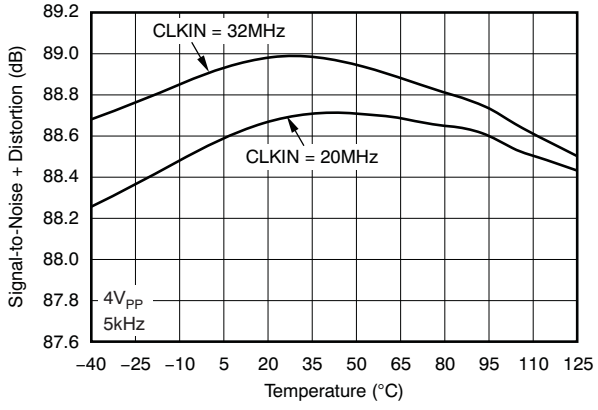


Figure 13. SINAD vs Temperature

Typical Characteristics (continued)

AV_{DD} = 5 V, BV_{DD} = 3 V, CH x+ = 0.5 V to 4.5 V, CH x– = 2.5 V, REFIN = external, CLKSEL = 0, and 16-bit $sinc^3$ filter, with OSR = 256 (unless otherwise noted)

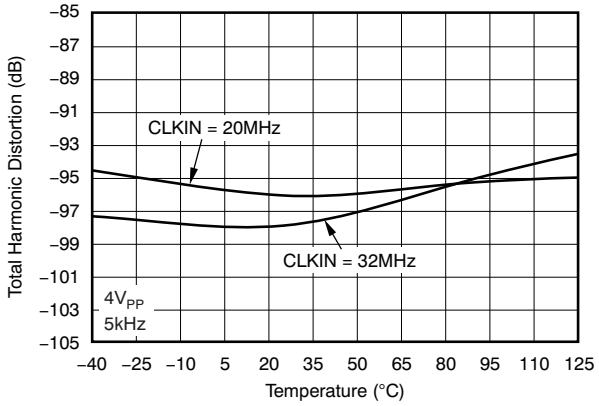


Figure 14. THD vs Temperature

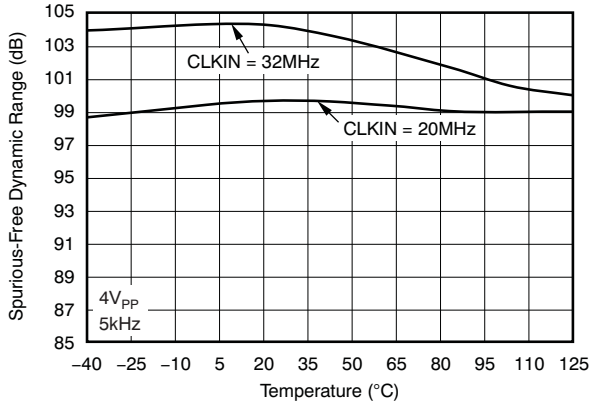
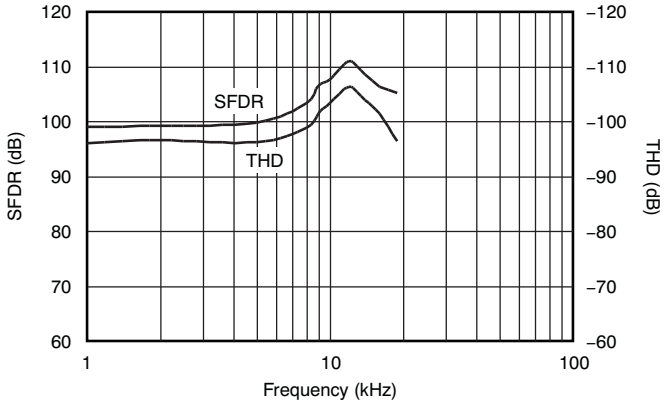
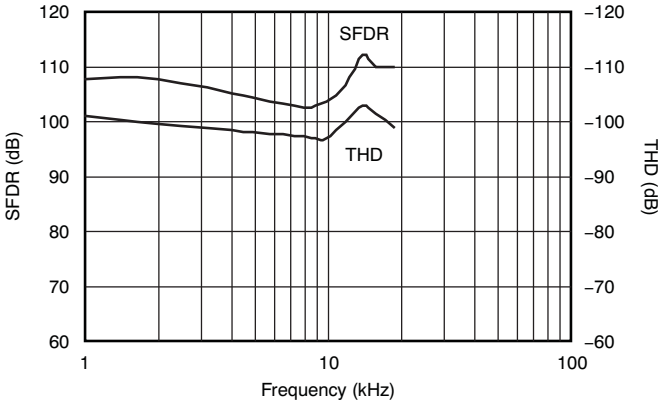


Figure 15. SFDR vs Temperature



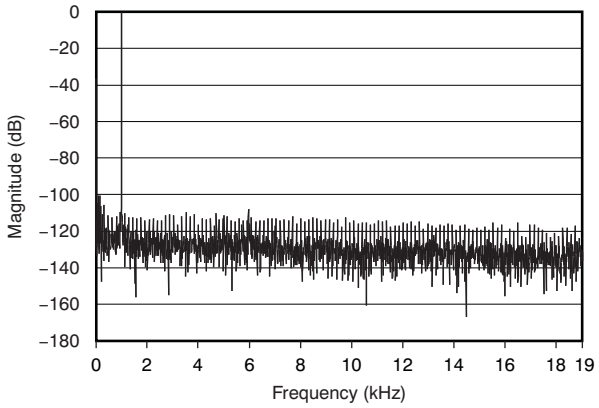
CLKIN = 20 MHz

Figure 16. SFDR and THD vs Input Frequency



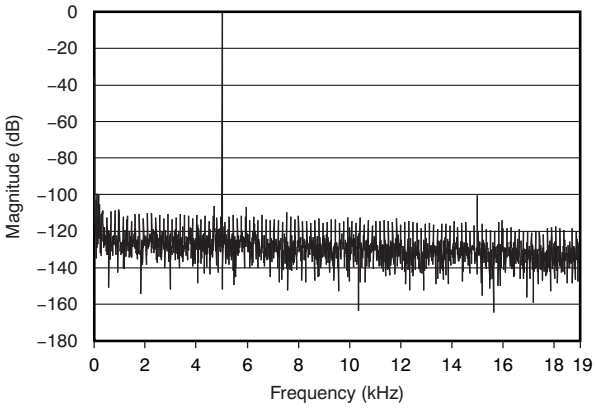
CLKIN = 32 MHz

Figure 17. SFDR and THD vs Input Frequency



4096-Point FFT, f_{IN} = 1 kHz, 4 V_{PP}

Figure 18. Frequency Spectrum



4096-Point FFT, f_{IN} = 5 kHz, 4 V_{PP}

Figure 19. Frequency Spectrum

Typical Characteristics (continued)

AV_{DD} = 5 V, BV_{DD} = 3 V, CH x+ = 0.5 V to 4.5 V, CH x– = 2.5 V, REFIN = external, CLKSEL = 0, and 16-bit $sinc^3$ filter, with OSR = 256 (unless otherwise noted)

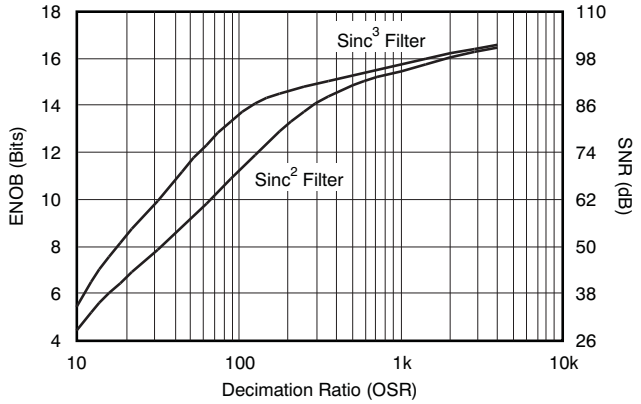


Figure 20. ENOB vs Decimation Ratio

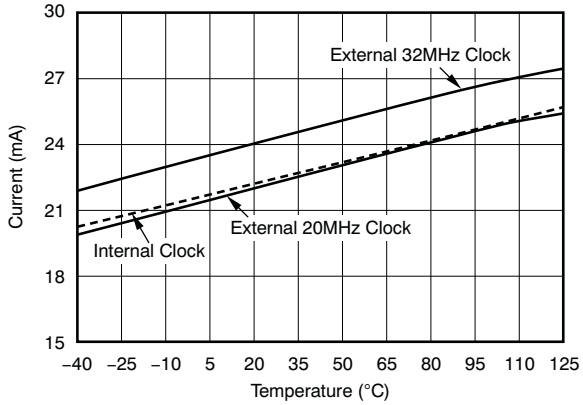


Figure 21. Analog Power-Supply Current vs Temperature

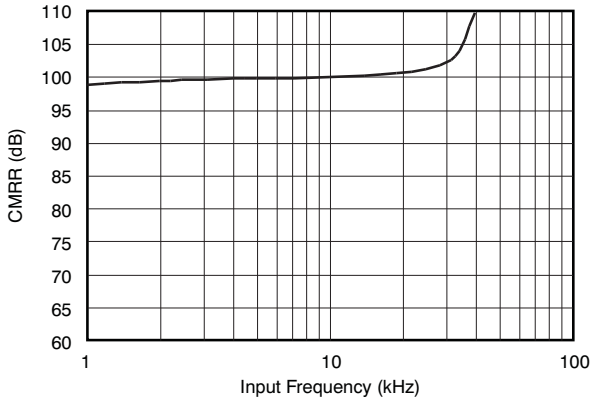


Figure 22. CMRR vs Frequency

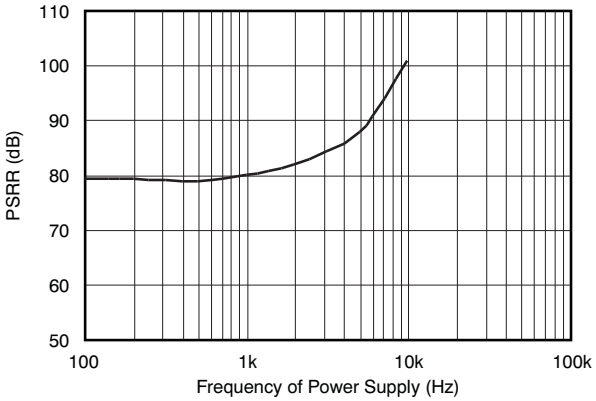


Figure 23. PSRR vs Frequency

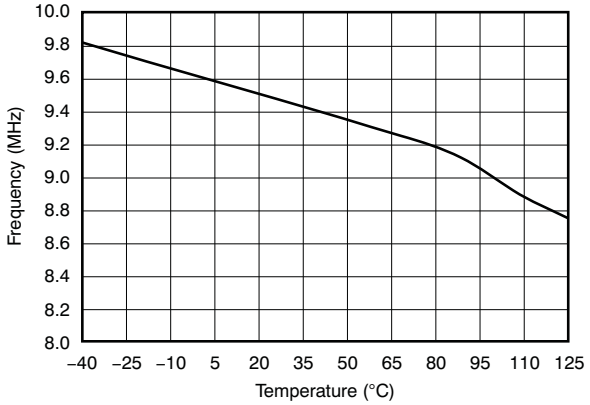


Figure 24. Clock Frequency vs Temperature

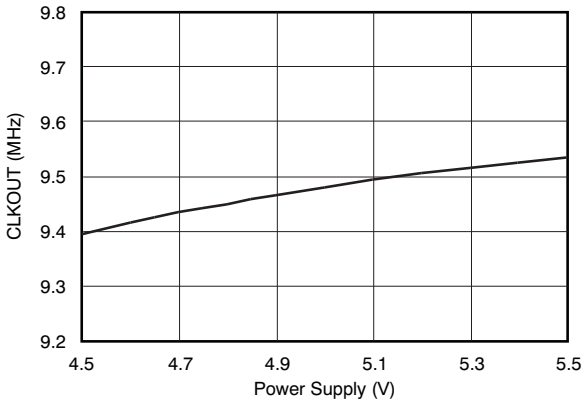


Figure 25. Clock Frequency vs Power Supply

7 Detailed Description

7.1 Overview

The ADS1204 is a four-channel, second-order, CMOS device with four delta-sigma (ΔΣ) modulators, designed for medium- to high-resolution A/D signal conversions from dc to 39 kHz (filter response –3 dB) if an oversampling ratio (OSR) of 64 is chosen. The output of the converter (OUTX) provides a stream of digital ones and zeros. The time average of this serial output is proportional to the analog input voltage.

The modulator shifts the quantization noise to high frequencies. A low-pass digital filter should be used at the output of the ΔΣ modulator. The filter serves two functions. First, it filters out high-frequency noise. Second, the filter converts the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation).

An application-specific integrated circuit (ASIC) or field-programmable gate array (FPGA) could be used to implement the digital filter. Figure 26 and Figure 27 illustrate typical application circuits with the ADS1204 connected to an FPGA.

The overall performance (that is, speed and accuracy) depends on the selection of an appropriate OSR and filter type. A higher OSR produces greater output accuracy while operating at a lower refresh rate. Alternatively, a lower OSR produces lower output accuracy, but operates at a higher refresh rate. This system allows flexibility with the digital filter design and is capable of A/D conversion results that have a dynamic range exceeding 100 dB with an OSR equal to 256.

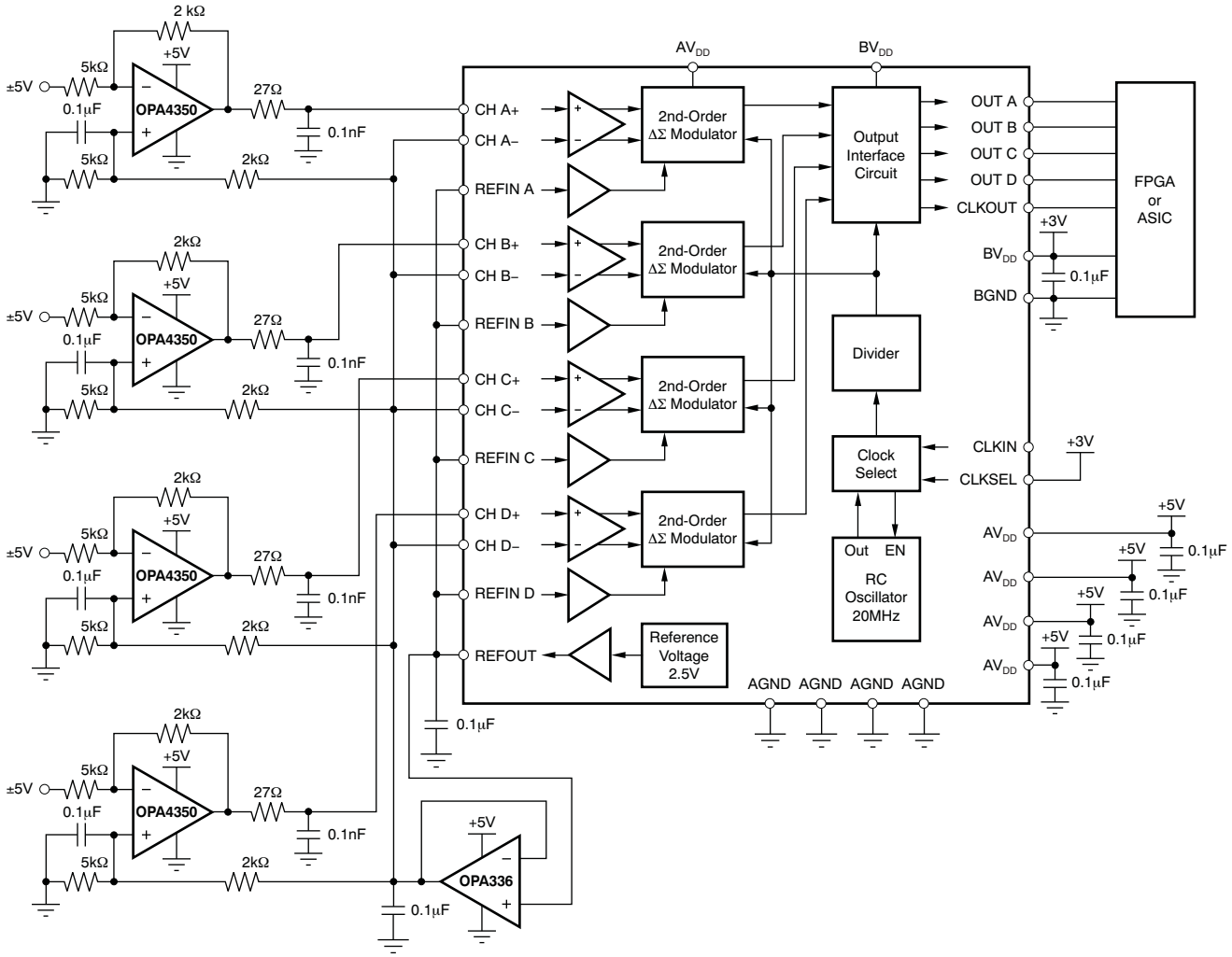


Figure 26. Single-Ended Connection Diagram for the ADS1204 ΔΣ Modulator

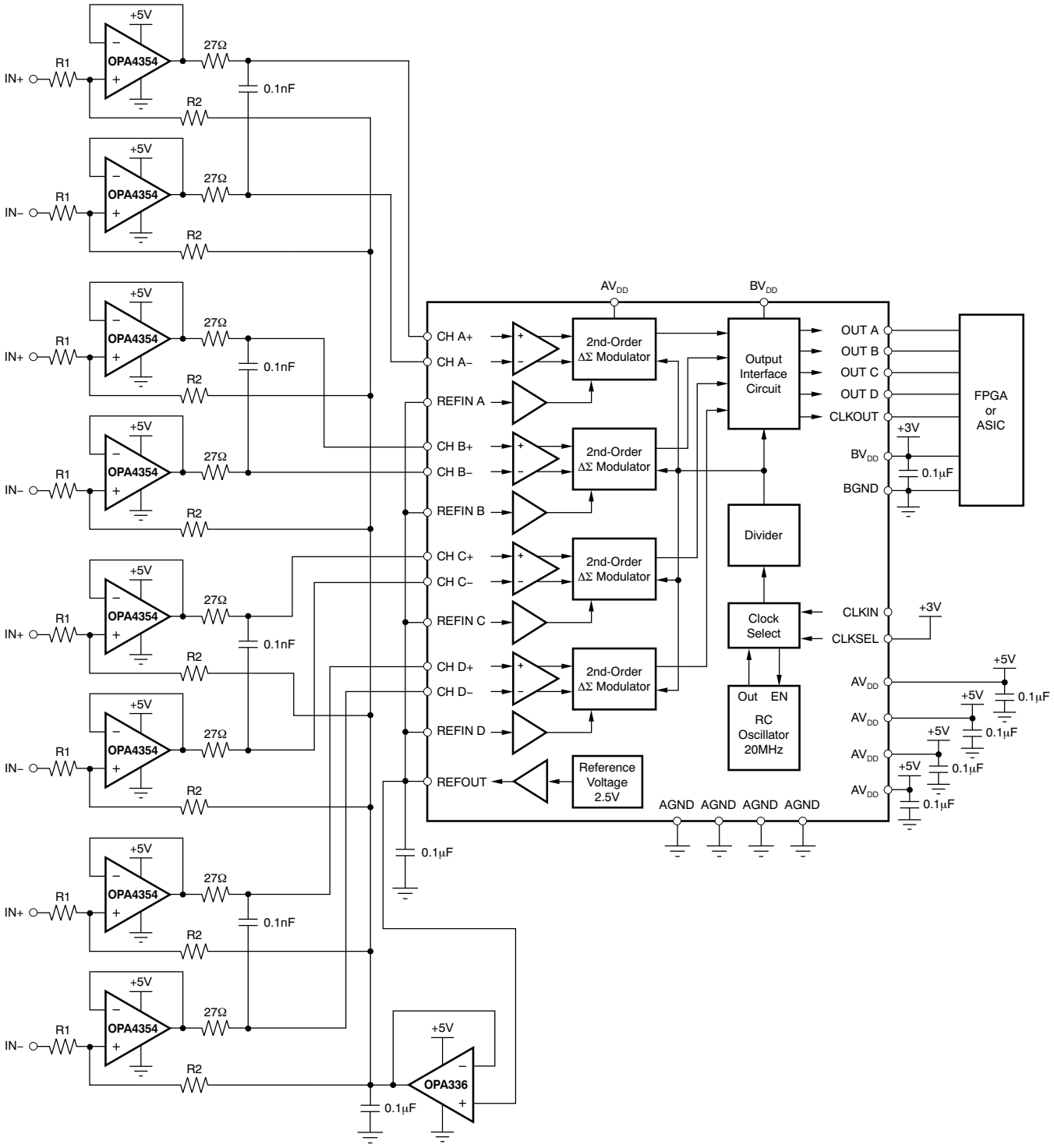
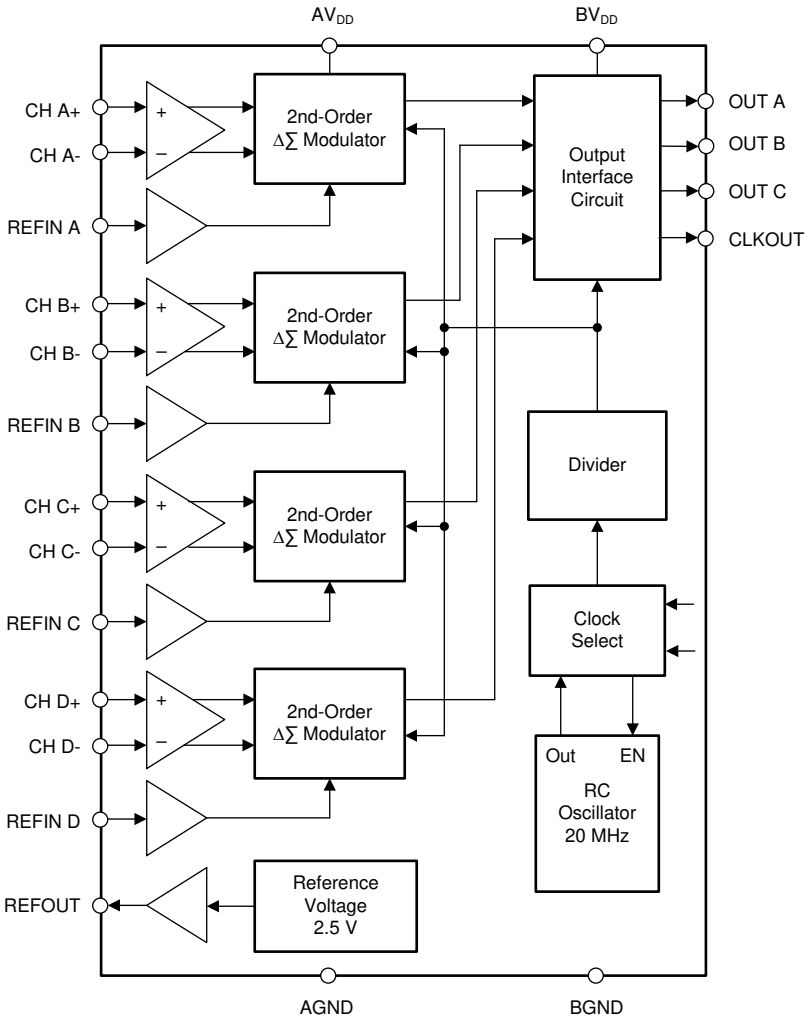


Figure 27. Differential Connection Diagram for the ADS1204 ΔΣ Modulator

7.2 Functional Block Diagram



7.3 Feature Description

The differential analog input of the ADS1204 is implemented with a switched-capacitor circuit. This circuit implements a second-order modulator stage, which digitizes the analog input signal into a 1-bit output stream. The clock source can be internal as well as external. Different frequencies for this clock allow for a variety of solutions and signal bandwidths. Every analog input signal is continuously sampled by the modulator and compared to a reference voltage that is applied to the REFINx pin. A digital stream, which accurately represents the analog input voltage over time, appears at the output of the corresponding converter.

Feature Description (continued)

7.3.1 Analog Input Stage

7.3.1.1 Analog Input

The topology of the analog inputs of ADS1204 is based on fully differential switched-capacitor architecture. This input stage provides the mechanism to achieve low system noise, high common-mode rejection (100 dB), and excellent power-supply rejection.

The input impedance of the analog input is dependent on the modulator clock frequency (f_{CLK}), which is also the sampling frequency of the modulator. Figure 28 shows the basic input structure of one channel of the ADS1204. The relationship between the input impedance of the ADS1204 and the modulator clock frequency is shown in Equation 1:

$$Z_{IN} = \frac{100k\Omega}{f_{MOD}/10MHz} \quad (1)$$

The input impedance becomes a consideration in designs where the source impedance of the input signal is high. This high impedance may cause degradation in gain, linearity, and THD. The importance of this effect depends on the desired system performance. There are two restrictions on the analog input signals, CH x+ and CH x–. If the input voltage exceeds the range (GND – 0.3 V) to (V_{DD} + 0.3 V), the input current must be limited to 10 mA because the input protection diodes on the front end of the converter will begin to turn on. In addition, the linearity and the noise performance of the device are ensured only when the differential analog voltage resides within ±2 V (with V_{REF} as a midpoint); however, the FSR input voltage is ±2.5 V.

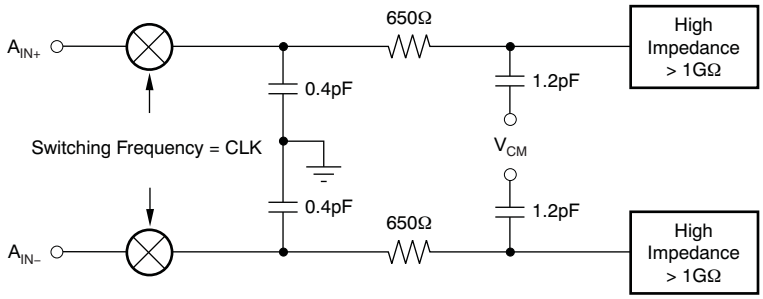


Figure 28. Input Impedance of the ADS1204

7.3.1.2 Modulator

The ADS1204 can be operated in two modes. When CKLSEL = 1, the four modulators operate using the internal clock, which is fixed at 20 MHz. When CKLSEL = 0, the modulators operate using an external clock . In both modes, the clock is divided by two internally and functions as the modulator clock. The frequency of the external clock can vary from 1 MHz to 32 MHz to adjust for the clock requirements of the application.

The modulator topology is fundamentally a second-order, switched-capacitor, ΔΣ modulator, such as the one conceptualized in Figure 29. The analog input voltage and the output of the 1-bit digital-to-analog converter (DAC) are differentiated, providing analog voltages at X2 and X3. The voltages at X2 and X3 are presented to their individual integrators. The output of these integrators progresses in a negative or positive direction. When the value of the signal at X4 equals the comparator reference voltage, the output of the comparator switches from negative to positive, or positive to negative, depending on its original state. When the output value of the comparator switches from high to low or vice versa, the 1-bit DAC responds on the next clock pulse by changing its analog output voltage at X6, causing the integrators to progress in the opposite direction. The feedback of the modulator to the front end of the integrators forces the value of the integrator output to track the average of the input.

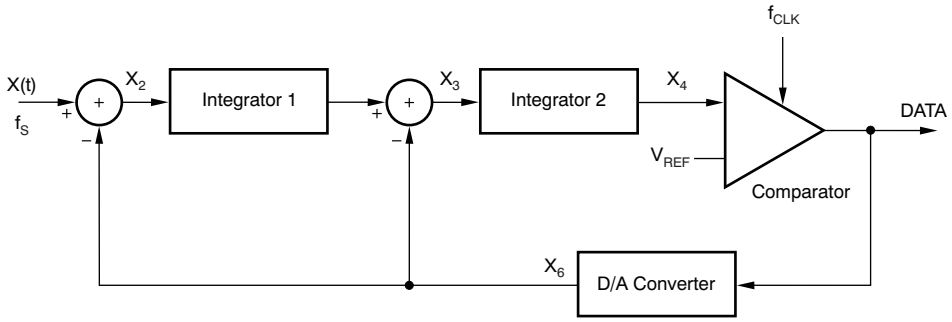


Figure 29. Block Diagram of the Second-Order Modulator

7.3.2 Digital Output

A differential input signal of 0 V will ideally produce a stream of ones and zeros that are high 50% of the time and low 50% of the time. A differential input of 2 V produces a stream of ones and zeros that are high 80% of the time. A differential input of –2 V produces a stream of ones and zeros that are high 20% of the time. The input voltage versus the output modulator signal is shown in Figure 30.

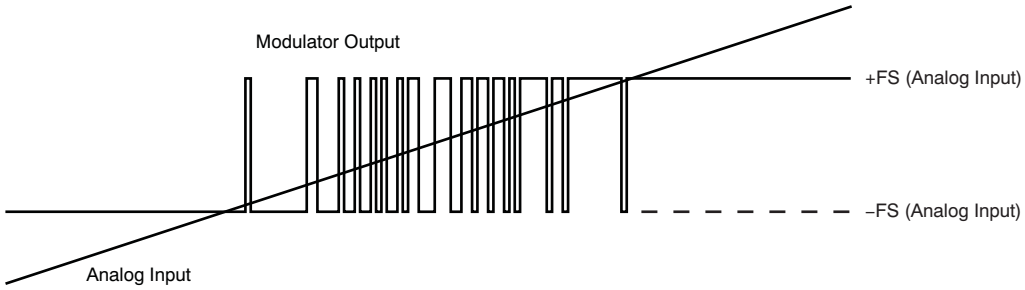
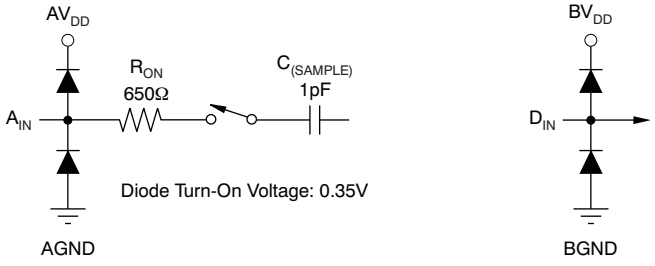


Figure 30. Analog Input versus Modulator Output of the ADS1204

7.3.3 Equivalent Input Circuits

Figure 31 shows equivalent circuits for the analog input and digital outputs.



NOTE: The thermal pad is internally connected to the substrate. This pad can be connected to the analog ground or left floating. Keep the thermal pad separate from the digital ground, if possible.

Figure 31. Equivalent Input Circuits

7.4 Device Functional Modes

The system clock of the ADS1204 is 20 MHz by default. The system clock can be provided either from the internal 20MHz RC oscillator or from an external clock source. For this purpose, the CLKIN pin is provided; it is controlled by the mode setting, CLKSEL.

The system clock is divided by two for the modulator clock. Therefore, the default clock frequency of the modulator is 10MHz. With a possible external clock range of 1MHz to 32MHz, the modulator operates between 500 kHz and 16 MHz.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The analog signal connected to the input of the ΔΣ modulator is converted using the clock signal applied to the modulator. The result of the conversion, or modulation, is generated and sent to the OUTx pin from the ΔΣ modulator. In most applications where a direct connection is realized between the ΔΣ modulator and an ASIC or FPGA (each with an implemented filter), the two standard signals per modulator (CLKOUT and OUTx) are provided from the modulator. The output clock signal is equal for all four modulators. If CLKSEL = 1, CLKIN must always be set either high or low.

8.1.1 Filter Usage

The modulator generates only a bitstream, which does not output a digital word like an A/D converter. In order to output a digital word equivalent to the analog input voltage, the bitstream must be processed by a digital filter.

A very simple filter, built with minimal effort and hardware, is the $sinc^3$ filter shown in Equation 2:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^2 \tag{2}$$

This filter provides the best output performance at the lowest hardware size (for example, a count of digital gates). For oversampling ratios in the range of 16 to 256, this is a good choice. All the characterizations in the data sheet are also done using a $sinc^3$ filter with an oversampling ratio of OSR = 256 and an output word width of 16 bits.

In a $sinc^3$ filter response (see Figure 32 and Figure 33), the location of the first notch occurs at the frequency of output data rate $f_{DATA} = f_{CLK} / OSR$. The –3-dB point is located at half the Nyquist frequency or $f_{DATA} / 4$. For some applications, it may be necessary to use another filter type for better frequency response.

Application Information (continued)

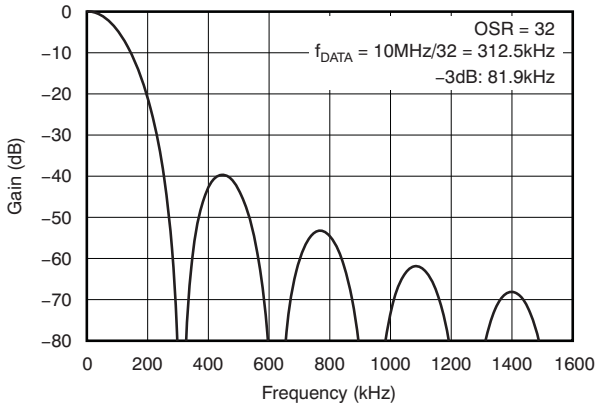


Figure 32. Frequency Response of Sinc^3 Filter

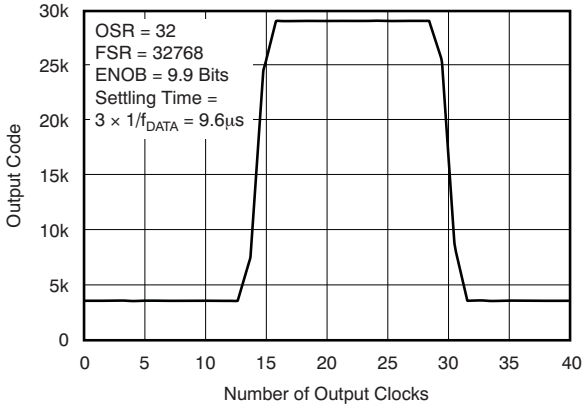


Figure 33. Pulse Response of Sinc^3 Filter (f_{MOD} = 10 MHz)

This performance can be improved, for example, by a cascaded filter structure. The first decimation stage can be a sinc^3 filter with a low OSR and the second stage a high-order filter.

For more information, see the *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications* application note, available for download at www.ti.com.

The effective number of bits (ENOB) can be used to compare the performance of A/D converters and ΔΣ modulators. Figure 34 shows the ENOB of the ADS1204 with different filter types. In this data sheet, the ENOB is calculated from the SNR as shown in Equation 3:

$$SNR = 1.76dB + 6.02dB \times ENOB \quad (3)$$

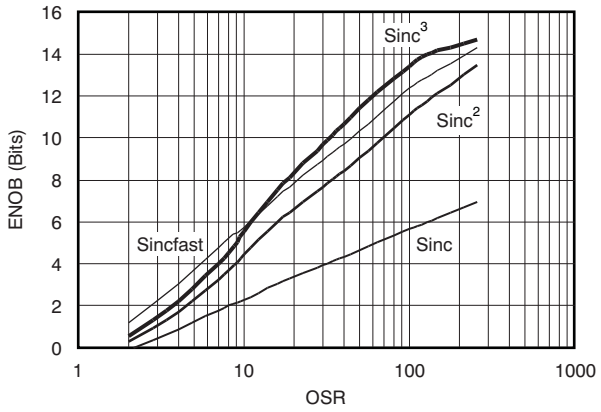


Figure 34. Measured ENOB vs OSR

In motor control applications, a very fast response time for overcurrent detection is required. There is a constraint between 1 µs and 5 µs with 3 bits to 7 bits resolution. The time for full settling is dependent on the filter order. Therefore, the full settling of the sinc^3 filter needs three data clocks and the sinc^2 filter needs two data clocks. The data clock is equal to the modulator clock divided by the OSR. For overcurrent protection, filter types other than sinc^3 might be a better choice. A simple example is a sinc^2 filter. Figure 35 compares the settling time of different filter types. The Sincfast is a modified sinc^2 filter as Equation 4 shows:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^2 (1 + z^{-2 \times OSR}) \quad (4)$$

Application Information (continued)

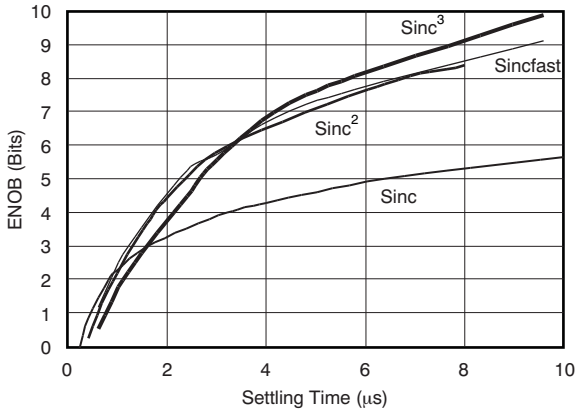


Figure 35. Measured ENOB versus Settling Time

For more information, see the *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications* application note, available for download at www.ti.com.

9 Power Supply Recommendations

The ADS1204 requires two power supplies, AV_{DD} for analog, and BV_{DD} for digital. The analog supply is a fixed voltage of 5 V ± 5%, whereas the digital supply can be set within a range of 2.7 V to 5.5 V. BV_{DD} determines the I/O voltage for the interface. If AV_{DD} equals BV_{DD}, the two supplies can be tied together.

9.1 Power-Supply Sequencing

The supplies can be sequenced in any order, but in no case must any analog or digital input exceed the respective analog or digital power-supply voltage and current limits. In particular, inputs to the ADS1204, such as CH x+, CH x–, and CLKIN, should not be present before the power supply is on. Violating this condition could cause latch-up. If these signals are present before the supply is on, series resistors should be used to limit the input current to a maximum of 10 mA.

Wait approximately 600 µs after all power supplies are stabilized before communicating with the device to allow the power-on reset process to complete.

9.2 Power-Supply Decoupling

Good decoupling practices must be used for the ADS1204 and for all components in the design. All decoupling capacitors, specifically the 0.1-µF ceramic capacitors, must be placed as close as possible to the pin being decoupled. A 1-µF and 10-µF capacitor, in parallel with the 0.1-µF ceramic capacitor, can be used to decouple AV_{DD} to AGND as well as BV_{DD} to BGND. At least one 0.1-µF ceramic capacitor must be used to decouple every AV_{DD} to AGND and BV_{DD} to BGND, as well as for the digital supply on each digital component.

In cases where both the analog and digital I/O supplies share the same supply source, an RC filter of 10 Ω and 0.1 µF can be used to help reduce the noise in the analog supply.

10 Layout

10.1 Layout Guidelines

Employing best design practices is recommended when laying out a printed-circuit board (PCB) for both analog and digital components. This recommendation generally means that the layout separates analog components [such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog MUXs] from digital components [such as microcontrollers, complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators]. Figure 36 shows an example of good component placement. Although Figure 36 provides a good example of component placement, the best placement for each application is unique to the geometries, components, and PCB fabrication capabilities employed. That is, there is no single layout that is perfect for every design and careful consideration must always be used when designing with any analog component.

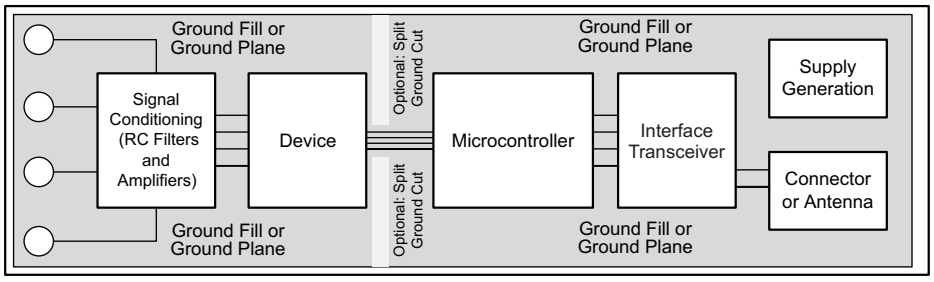


Figure 36. System Component Placement

The following basic recommendations for layout of the ADS1204 help achieve the best possible performance of the ADC.

- Separate analog and digital signals. To start, partition the board into analog and digital sections where the layout permits. Routing digital lines away from analog lines prevents digital noise from coupling back into analog signals.
- The ground plane can be split into an analog plane (AGND) and digital plane (DGND), but is not necessary. Place digital signals over the digital plane, and analog signals over the analog plane. As a final step in the layout, the split between the analog and digital grounds must be connected to together at the ADC.
- Fill void areas on signal layers with ground fill.
- Provide good ground return paths. Signal return currents flow on the path of least impedance. If the ground plane is cut or has other traces that block the current from flowing right next to the signal trace, another path must be found to return to the source and complete the circuit. If forced into a larger path, the chance that the signal radiates increases. Sensitive signals are more susceptible to EMI interference.
- Use bypass capacitors on supplies to reduce high-frequency noise. Do not place vias between bypass capacitors and the active device. Placing the bypass capacitors on the same layer as close to the active device yields the best results.
- Consider the resistance and inductance of the routing. Often, traces for the inputs have resistances that react with the input bias current and cause an added error voltage. Reducing the loop area enclosed by the source signal and the return current reduces the inductance in the path. Reducing the inductance reduces the EMI pickup and reduces the high-frequency impedance at the input of the device.
- Watch for parasitic thermocouples in the layout. Dissimilar metals going from each analog input to the sensor can create a parasitic thermocouple that can add an offset to the measurement. Differential inputs must be matched for both the inputs going to the measurement source.
- Analog inputs with differential connections must have a capacitor placed differentially across the inputs. Best input combinations for differential measurements use adjacent analog input lines (such as CH A+, CH A– through CH D+ and CH D–). The differential capacitors must be of high quality. The best ceramic chip capacitors are C0G (NPO) that have stable properties and low noise characteristics.

10.2 Layout Example

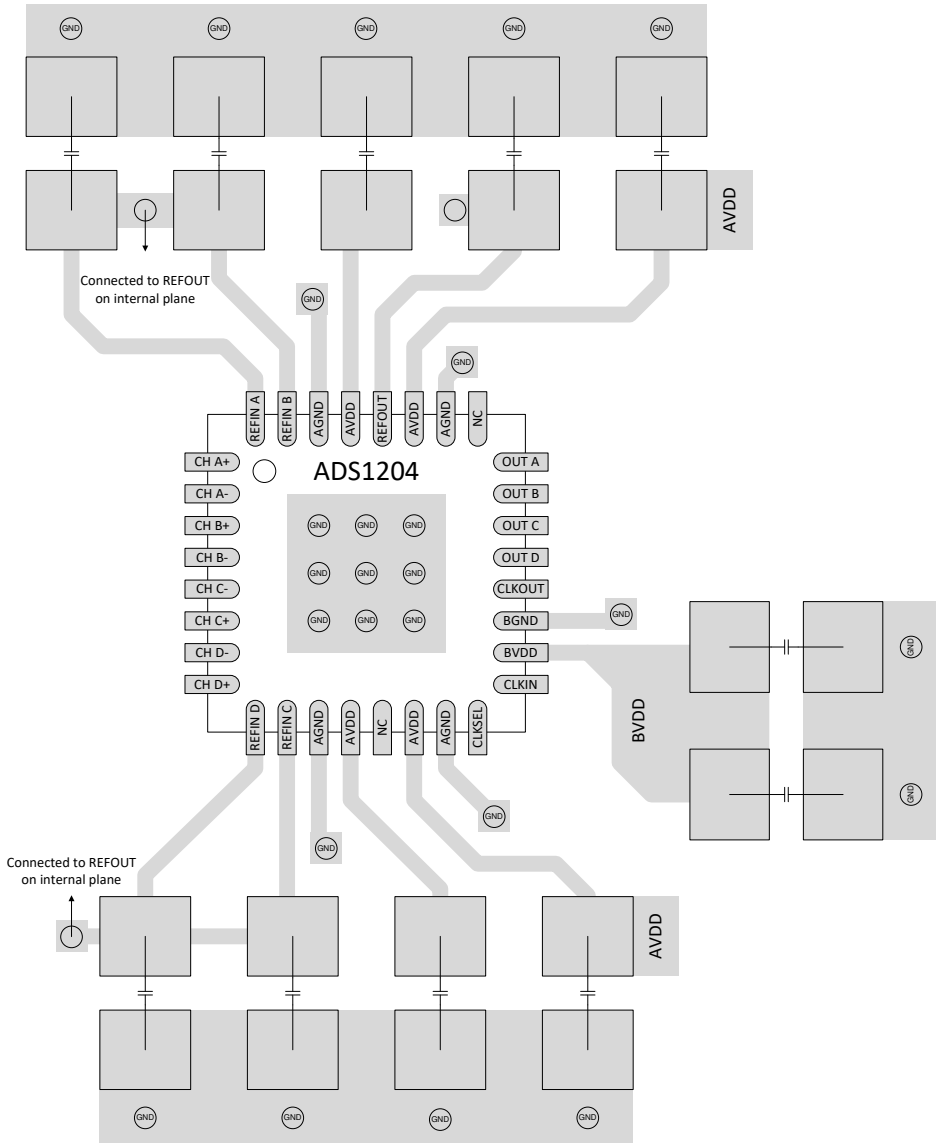


Figure 37. ADS1204 Layout Example

11 器件和文档支持

11.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS1204IRHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS 1204I
ADS1204IRHBR.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS 1204I
ADS1204IRHBT	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS 1204I
ADS1204IRHBT.B	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS 1204I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

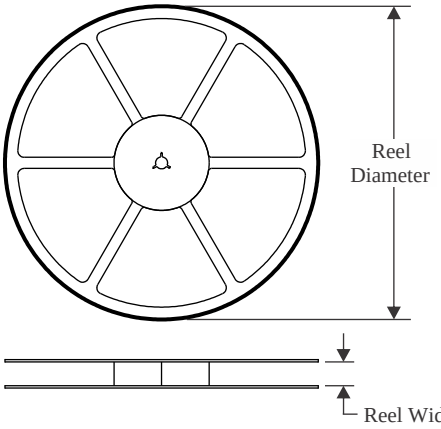
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

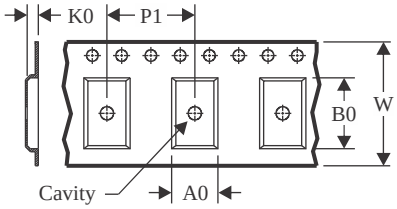
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

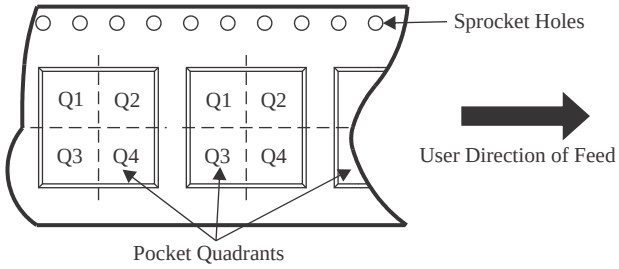


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

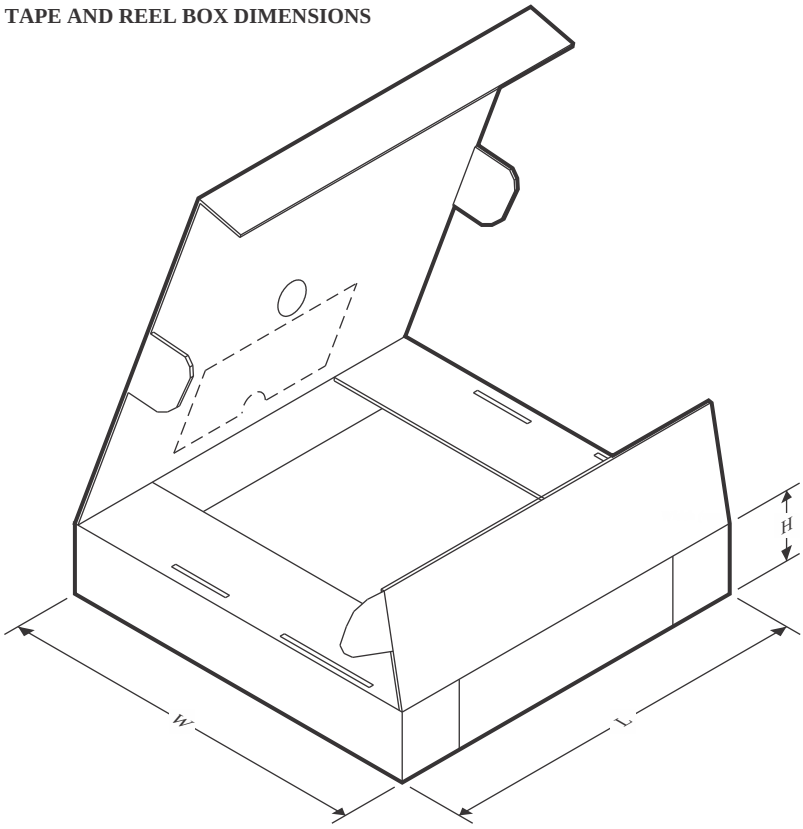
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1204IRHBRG4	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1204IRHBRG4	VQFN	RHB	32	3000	350.0	350.0	43.0

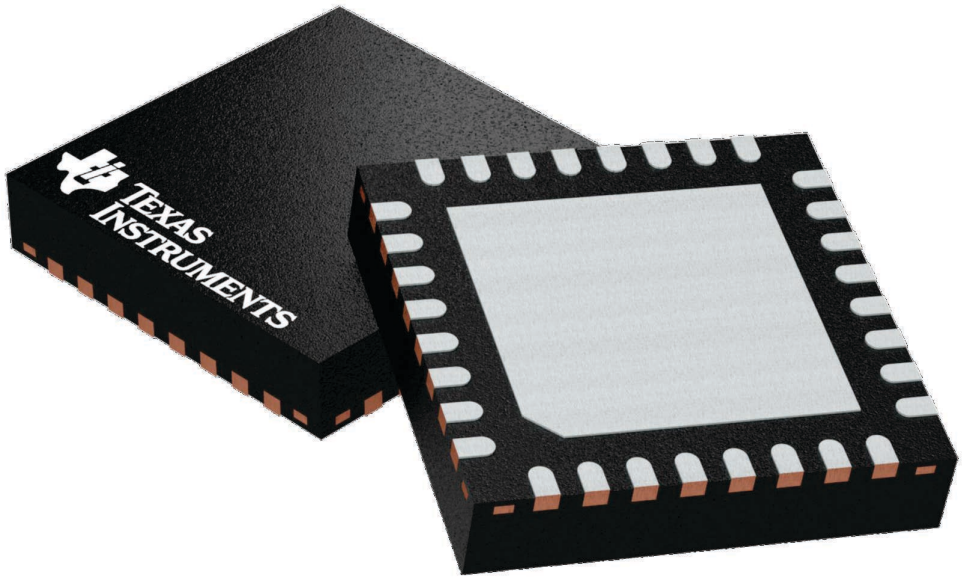
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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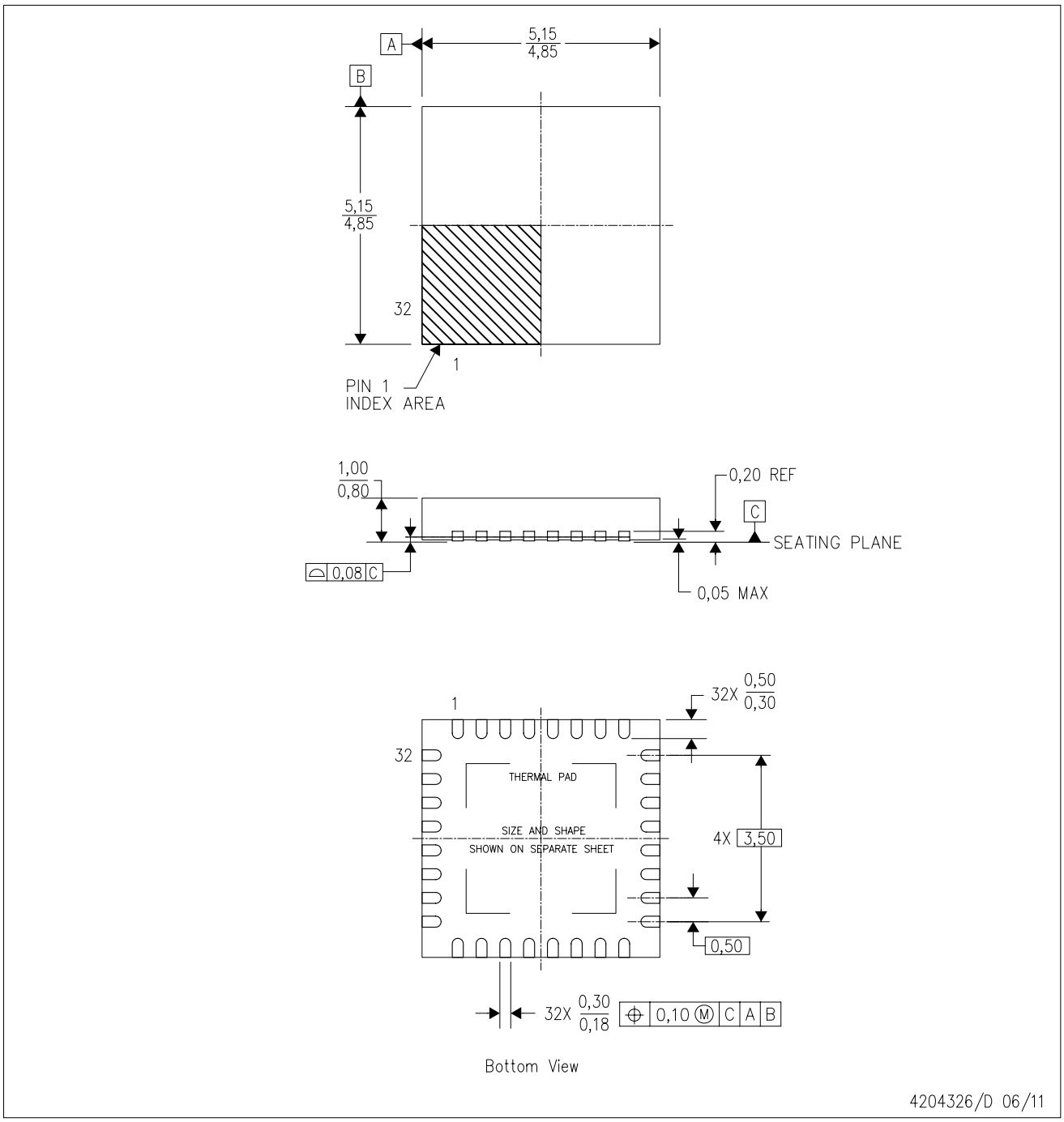
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

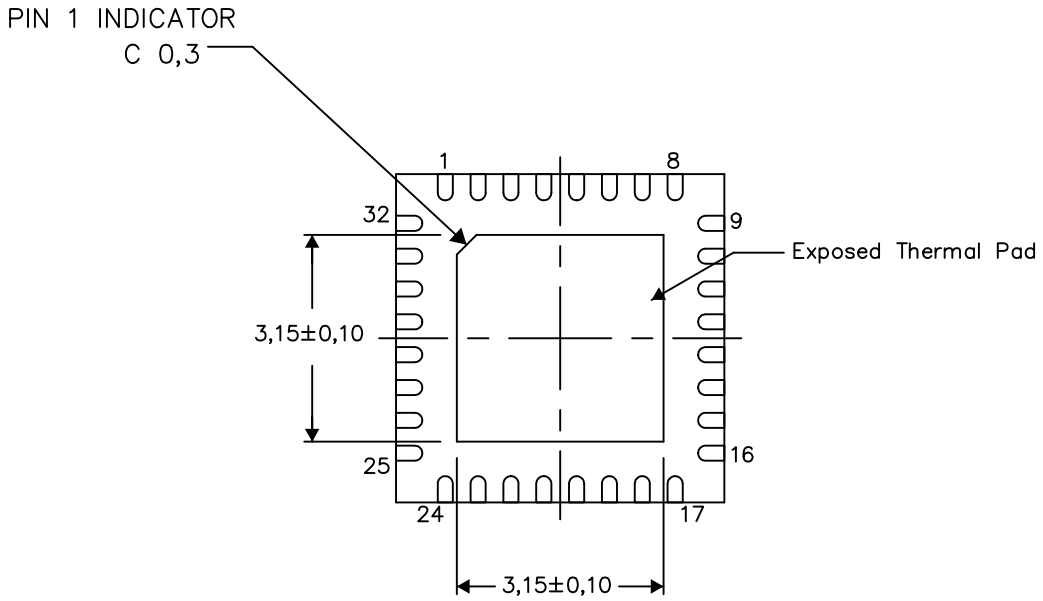
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



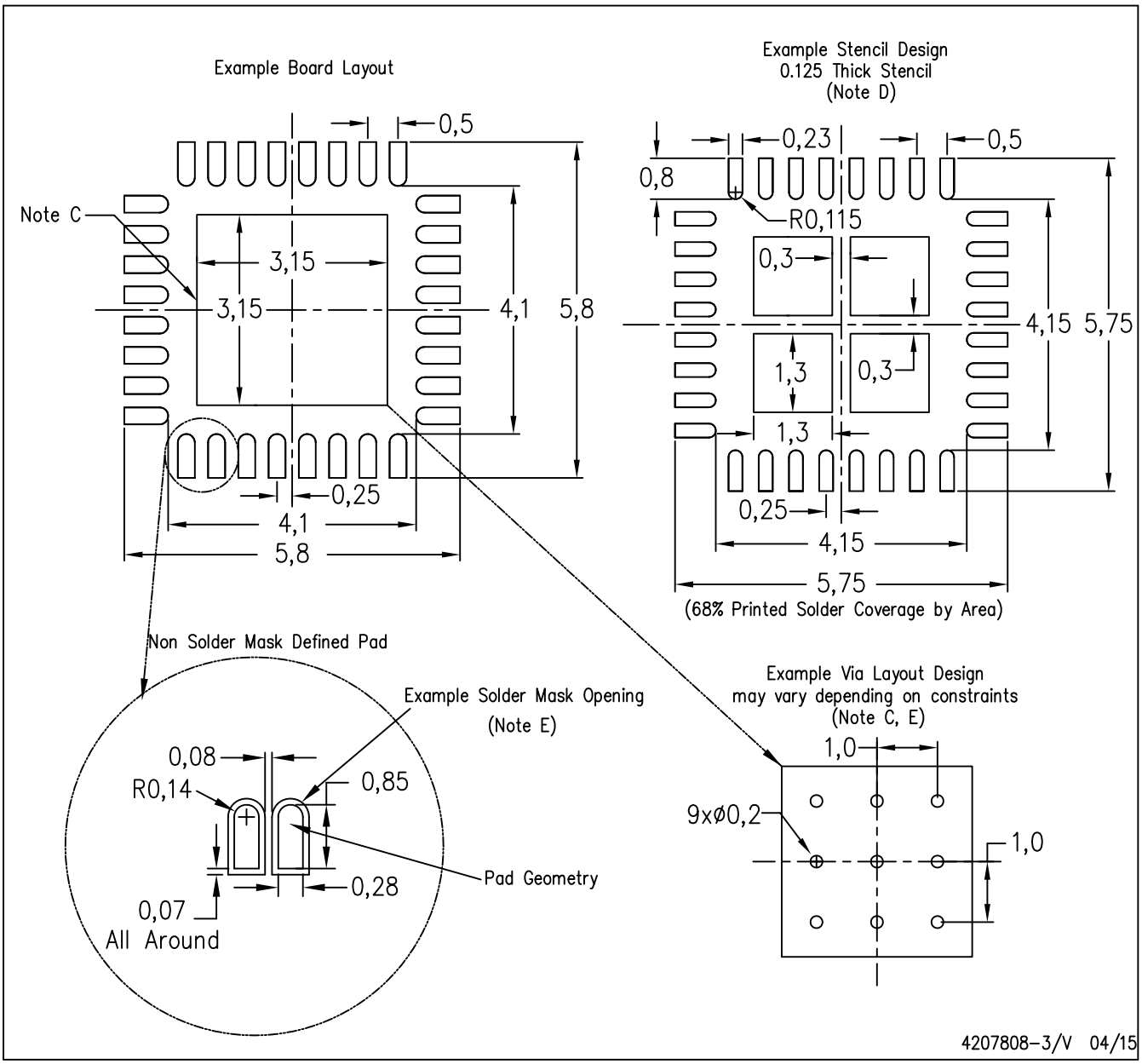
Bottom View

Exposed Thermal Pad Dimensions

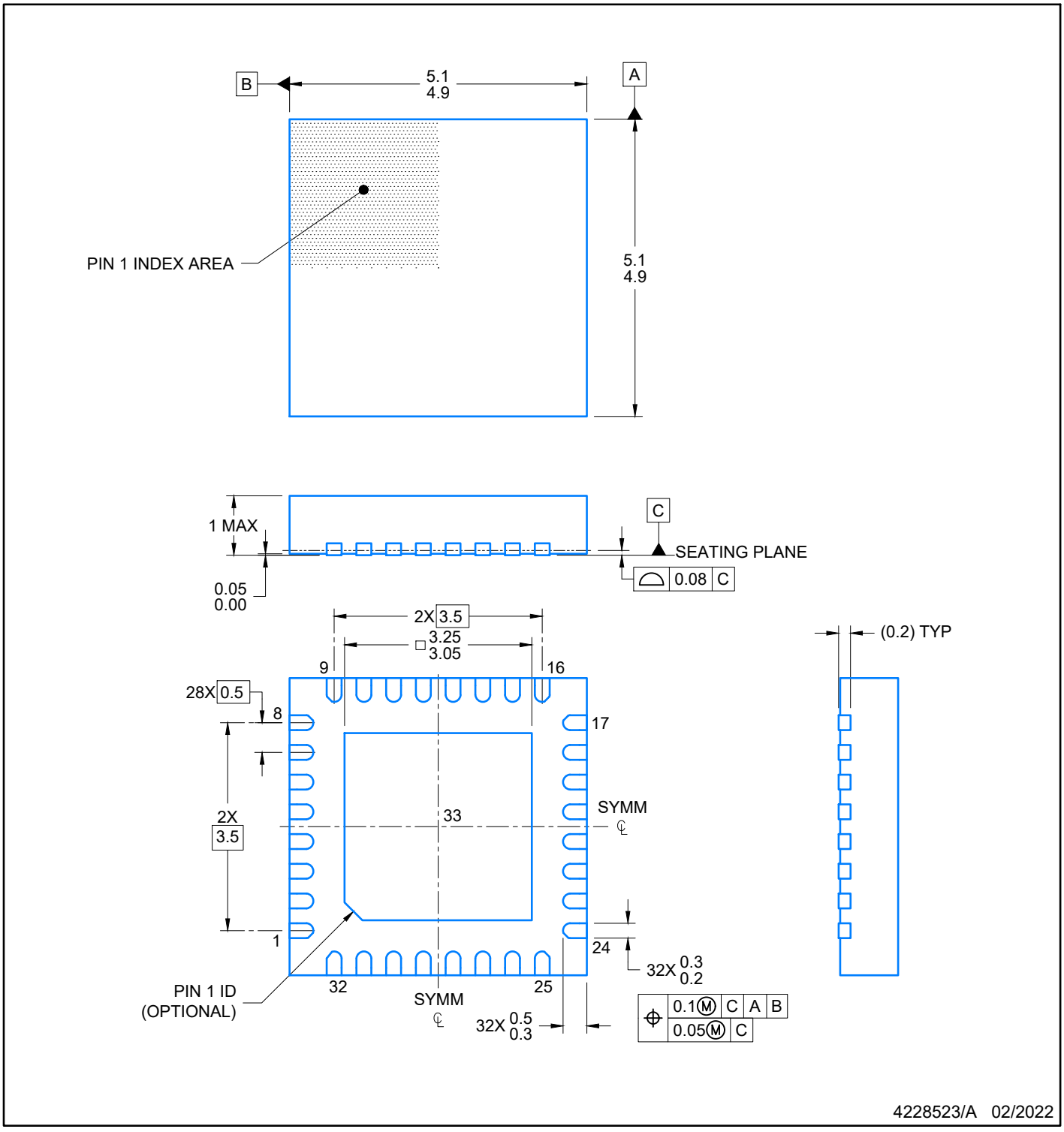
4206356–3/AC 05/15

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

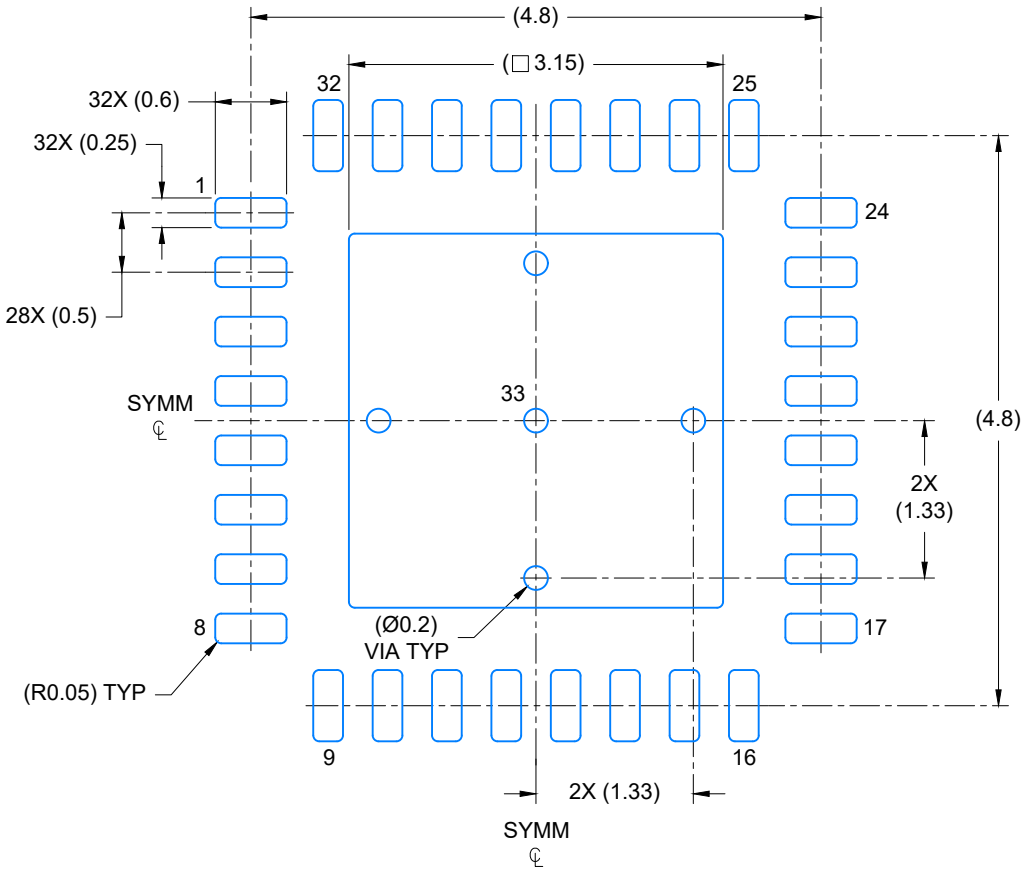


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

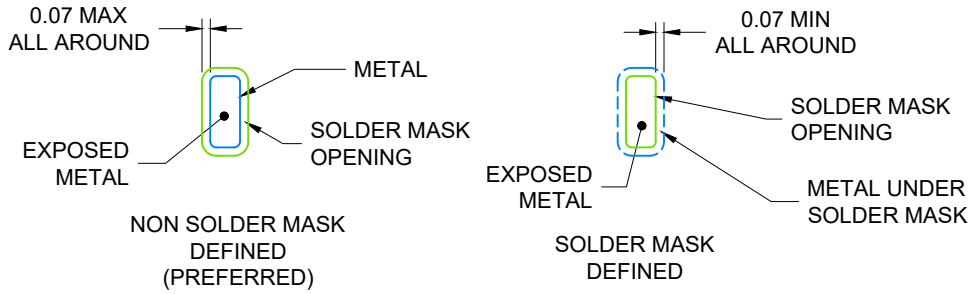


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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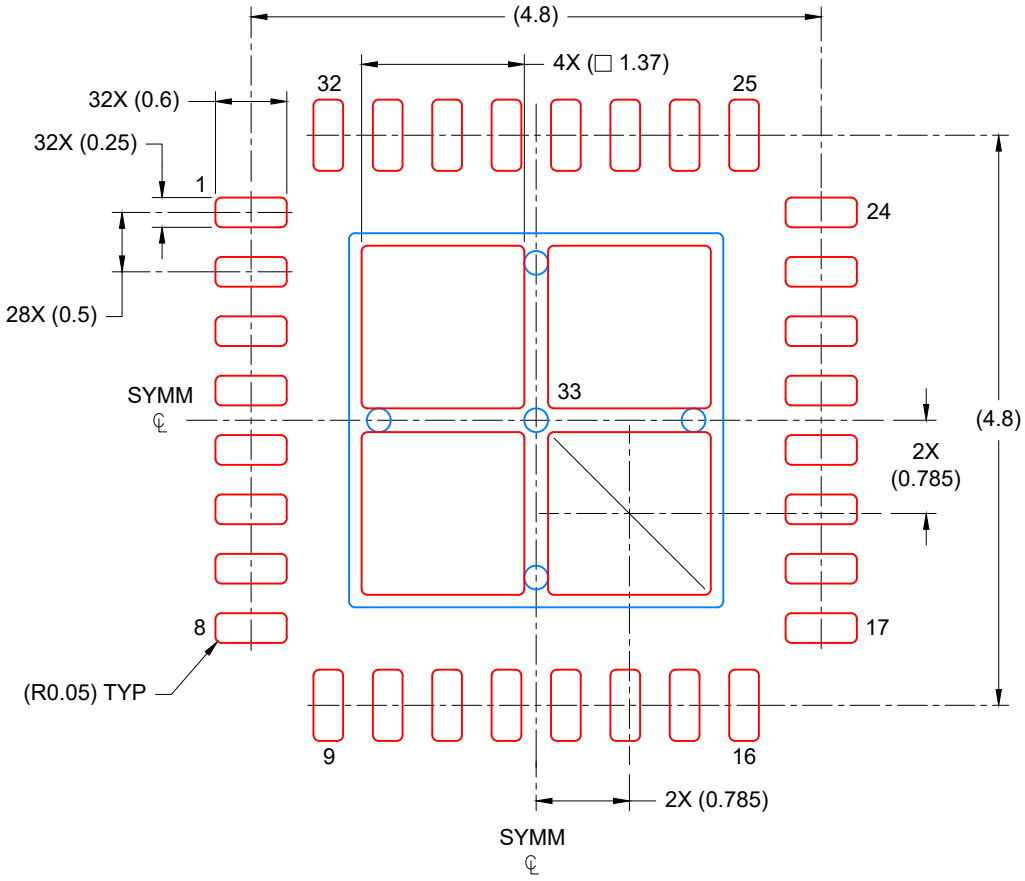
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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