ADC12DLx500 0.5, 1.5, 2.5GSPS Dual-Channel or 1, 3, 5GSPS Single-Channel,12-Bit Analog-to-Digital Converters (ADC) With LVDS Interface

1 Features

- ADC core:
  - 12-Bit resolution
  - Up to 1GSPS, 3GSPS, 5GSPS in single-channel mode
  - Up to 500MSPS, 1.5GSPS, 2.5GSPS in dual-channel mode
- Internal dither for low-magnitude, high-order harmonics
- Low-latency LVDS interface:
  - Total latency: < 10ns
  - Up to 48 data pairs at 1.6Gbps
  - Four DDR data clocks
  - Strobe signals simplify synchronization
- Noise floor (no input, V_{FS} = $1V_{PP\text{-}DIFF}$):
  - Dual-channel mode: -143.5, -148, -149.8dBFS/Hz
  - Single-channel mode: -146.2, -150.3, -152.2dBFS/Hz
- Buffered analog inputs with V_{CMI} of 0V:
  - Analog input bandwidth (–3dB): 8GHz
  - Full-scale input voltage (V_{FS}, default): $0.8V_{PP}$
- Noiseless aperture delay (T_{AD}) adjustment:
  - Precise sampling control: 19fs step
  - Simplifies synchronization and interleaving
  - Temperature and voltage invariant delays
- Easy-to-use synchronization features:
  - Automatic SYSREF timing calibration
  - Timestamp for sample marking
- Power consumption: 2.6, 2.8, 3W

2 Applications

- Oscilloscopes and digitizers
- Electronic Warfare (SIGINT, ELINT)
- Time-of-flight and LIDAR distance measurement
- Microwave backhaul
- Automotive radar testers
- Spectrometry

3 Description

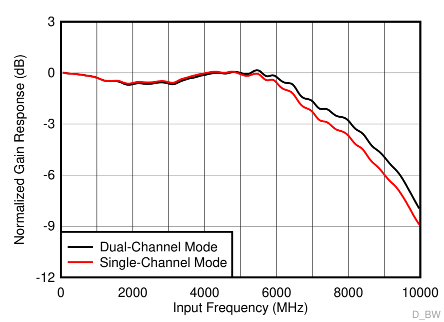
The ADC12DL500, ADC12DL1500 and ADC12DL2500 are a family of analog-to-digital converters (ADC) that can sample up to 500MSPS, 1.5GSPS, and 2.5GSPS in dual-channel mode and up to 1GSPS, 3GSPS, and 5GSPS in single-channel mode. Programmable tradeoffs in channel count (dual-channel mode) and sample rate (single-channel mode) allow development of flexible hardware that meets the needs of both high-channel count or wide instantaneous signal bandwidth applications.

The devices uses a low-latency, low-voltage differential signaling (LVDS) interface for latency sensitive applications or when the simplicity of LVDS is preferred. The interface uses up to 48 data pairs, four double data rate (DDR) clocks, and four strobe signals arranged in four 12-bit data buses. The interface supports signaling rates of up to 1.6Gbps. Strobe signals simplify synchronization across buses and between multiple devices. The strobe is generated internally and can be reset at a deterministic time by the SYSREF input. Multi-device synchronization is further eased by innovative synchronization features such as noiseless aperture delay (T_{AD}) adjustment and SYSREF windowing.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ADC12DL500 ADC12DL1500 ADC12DL2500	FCBGA (256)	17mm × 17mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



ADC12DLx500 Frequency Response

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4 Pin Configuration and Functions

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	AGND	AGND	AGND	INA+	INA–	AGND	AGND	ORA1	DA0+	DA0–	DA6+	DA6–	DC0+	DC0–	DGND	DGND
B	CALSTAT	CALTRIG	AGND	AGND	AGND	AGND	AGND	ORA0	DA1+	DA1–	DA7+	DA7–	DC1+	DC1–	DC7+	DC7–
C	AGND	AGND	AGND	AGND	AGND	AGND	AGND	ORB1	DA2+	DA2–	DA8+	DA8–	DC2+	DC2–	DC8+	DC8–
D	TMSTP+	BG	AGND	AGND	AGND	AGND	DGND	ORB0	DA3+	DA3–	DA9+	DA9–	DC3+	DC3–	DC9+	DC9–
E	TMSTP–	SYNCSE	AGND	VA11	VA11	VA11	DGND	VD11	DA4+	DA4–	DA10+	DA10–	DC4+	DC4–	DC10+	DC10–
F	AGND	AGND	VA11	VA11	VA11	VA11	DGND	VD11	DA5+	DA5–	DA11+	DA11–	DC5+	DC5–	DC11+	DC11–
G	AGND	AGND	VA19	VA19	VA19	VA19	DGND	VD11	DACLK+	DACLK–	VLVDS	VLVDS	DC6+	DC6–	DCCLK+	DCCLK–
H	CLK+	AGND	VA19	VA19	VA19	VA19	DGND	DGND	DASTR+	DASTR–	VLVDS	VLVDS	VLVDS	DGND	DCSTR+	DCSTR–
J	CLK–	AGND	VA19	VA19	VA19	VA19	DGND	DGND	DBSTR+	DBSTR–	VLVDS	VLVDS	VLVDS	DGND	DDSTR+	DDSTR–
K	AGND	AGND	VA19	VA19	VA19	VA19	DGND	VD11	DBCLK+	DBCLK–	VLVDS	VLVDS	DD6+	DD6–	DDCLK+	DDCLK–
L	AGND	AGND	VA11	VA11	VA11	VA11	DGND	VD11	DB5+	DB5–	DB11+	DB11–	DD5+	DD5–	DD11+	DD11–
M	SYSREF+	TDIODE+	AGND	VA11	VA11	VA11	DGND	VD11	DB4+	DB4–	DB10+	DB10–	DD4+	DD4–	DD10+	DD10–
N	SYSREF–	TDIODE–	AGND	AGND	AGND	AGND	DGND	SDO	DB3+	DB3–	DB9+	DB9–	DD3+	DD3–	DD9+	DD9–
P	AGND	AGND	AGND	AGND	AGND	AGND	AGND	SDI	DB2+	DB2–	DB8+	DB8–	DD2+	DD2–	DD8+	DD8–
R	PD	AGND	AGND	AGND	AGND	AGND	AGND	SCS	DB1+	DB1–	DB7+	DB7–	DD1+	DD1–	DD7+	DD7–
T	AGND	AGND	AGND	INB+	INB–	AGND	AGND	SCLK	DB0+	DB0–	DB6+	DB6–	DD0+	DD0–	DGND	DGND

Not to scale

Figure 4-1. ACF Package, 256-Ball Flip Chip BGA (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
A2	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
A3	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
A4	INA+	I	Channel A analog input positive connection. The differential full-scale input range is determined by the FS_RANGE_A register; see the *Full-Scale Voltage (VFS) Adjustment* section. This input is terminated to AGND through a 50-Ω termination resistor. The input common-mode voltage must typically be set to 0 V (GND) and must follow the recommendations in the *Recommended Operating Conditions* table. This pin can be left disconnected if not used.
A5	INA–	I	Channel A analog input negative connection. See INA+ (pin A4) for detailed description. This input is terminated to ground through a 50Ω termination resistor. This pin can be left disconnected if not used.
A6	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
A7	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
A8	ORA1	O	Fast overrange detection status for channel A for the OVR_T1 threshold. When the analog input exceeds the threshold programmed into OVR_T1, this status indicator goes high. The minimum pulse duration is set by OVR_N. See the *ADC Overrange Detection* section for more information. Leave this pin disconnected if not used.
A9	DA0+	O	LVDS output for bit 0 of LVDS bus A. Positive connection. This pin can be left disconnected if not used.
A10	DA0–	O	LVDS output for bit 0 of LVDS bus A. Negative connection. This pin can be left disconnected if not used.
A11	DA6+	O	LVDS output for bit 6 of LVDS bus A. Positive connection. This pin can be left disconnected if not used.
A12	DA6–	O	LVDS output for bit 6 of LVDS bus A. Negative connection. This pin can be left disconnected if not used.
A13	DC0+	O	LVDS output for bit 0 of LVDS bus C. Positive connection. This pin can be left disconnected if not used.
A14	DC0–	O	LVDS output for bit 0 of LVDS bus C. Negative connection. This pin can be left disconnected if not used.
A15	DGND	—	Digital supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
A16	DGND	—	Digital supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
B1	CALSTAT	O	Foreground calibration status output or device alarm output. Functionality is programmed through CAL_STATUS_SEL. This pin can be left disconnected if not used.
B2	CALTRIG	I	Foreground calibration trigger input. This pin is only used if hardware calibration triggering is selected in CAL_TRIG_EN, otherwise software triggering is performed using CAL_SOFT_TRIG. Tie this pin to GND if not used.
B3	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
B4	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
B5	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
B6	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
B7	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
B8	ORA0	O	Fast overrange detection status for channel A for the OVR_T0 threshold. When the analog input exceeds the threshold programmed into OVR_T0, this status indicator goes high. The minimum pulse duration is set by OVR_N. See the *ADC Overrange Detection* section for more information. Leave this pin disconnected if not used.
B9	DA1+	O	LVDS output for bit 1 of LVDS bus A. Positive connection. This pin can be left disconnected if not used.
B10	DA1–	O	LVDS output for bit 1 of LVDS bus A. Negative connection. This pin can be left disconnected if not used.
B11	DA7+	O	LVDS output for bit 7 of LVDS bus A. Positive connection. This pin can be left disconnected if not used.
B12	DA7–	O	LVDS output for bit 7 of LVDS bus A. Negative connection. This pin can be left disconnected if not used.
B13	DC1+	O	LVDS output for bit 1 of LVDS bus C. Positive connection. This pin can be left disconnected if not used.
B14	DC1–	O	LVDS output for bit 1 of LVDS bus C. Negative connection. This pin can be left disconnected if not used.
B15	DC7+	O	LVDS output for bit 7 of LVDS bus C. Positive connection. This pin can be left disconnected if not used.
B16	DC7–	O	LVDS output for bit 7 of LVDS bus C. Negative connection. This pin can be left disconnected if not used.
C1	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
C2	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
C3	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.

Table 4-1. Pin Functions (continued)

PIN NO.	PIN NAME	TYPE	DESCRIPTION
C4	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
C5	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
C6	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
C7	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
C8	ORB1	O	Fast overrange detection status for channel B for the OVR_T1 threshold. When the analog input exceeds the threshold programmed into OVR_T1, this status indicator goes high. The minimum pulse duration is set by OVR_N. See the *ADC Overrange Detection* section for more information. Leave this pin disconnected if not used.
C9	DA2+	O	LVDS output for bit 2 of LVDS bus A. Positive connection. This pin can be left disconnected if not used.
C10	DA2–	O	LVDS output for bit 2 of LVDS bus A. Negative connection. This pin can be left disconnected if not used.
C11	DA8+	O	LVDS output for bit 8 of LVDS bus A. Positive connection. This pin can be left disconnected if not used.
C12	DA8–	O	LVDS output for bit 8 of LVDS bus A. Negative connection. This pin can be left disconnected if not used.
C13	DC2+	O	LVDS output for bit 2 of LVDS bus C. Positive connection. This pin can be left disconnected if not used.
C14	DC2–	O	LVDS output for bit 2 of LVDS bus C. Negative connection. This pin can be left disconnected if not used.
C15	DC8+	O	LVDS output for bit 8 of LVDS bus C. Positive connection. This pin can be left disconnected if not used.
C16	DC8–	O	LVDS output for bit 8 of LVDS bus C. Negative connection. This pin can be left disconnected if not used.
D1	TMSTP+	I	Timestamp input positive connection or differential LVDS SYNC positive connection. This input is used as the timestamp input, used to mark a specific sample, when TIMESTAMP_EN is set 1. This differential input is used as the SYNC signal input when SYNC_SEL is set to 1. This input can be used as both a timestamp and differential SYNC input at the same time, allowing feedback of the SYNC signal using the timestamp mechanism. TMSTP± uses active low signaling when used as the LVDS SYNC signal. For additional usage information, see the *Timestamp* section. TMSTP_RECV_EN must be set to 1 to use this input. This differential input (TMSTP+ to TMSTP–) has an internal untrimmed 100Ω differential termination and can be AC-coupled when TMSTP_LVPECL_EN is set to 0. The termination changes to 50Ω to ground on each input pin (TMSTP+ and TMSTP–) and can be DC-coupled when TMSTP_LVPECL_EN is set to 1. This pin is not self-biased and therefore must be externally biased for both AC-coupled and DC-coupled configurations. The common-mode voltage must be within the range provided in the *Recommended Operating Conditions* table when both AC-coupled and DC-coupled. This pin can be left disconnected and disabled (TMSTP_RECV_EN = 0) if $\overline{\text{SYNCSE}}$ is used for the LVDS SYNC signal and timestamp is not required.
D2	BG	O	Band-gap voltage output. This pin is capable of sourcing only small currents and driving limited capacitive loads, as specified in the *Recommended Operating Conditions* table. See the *Analog Reference Voltage* section for more details. This pin can be left disconnected if not used.
D3	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
D4	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
D5	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
D6	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
D7	DGND	—	Digital supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
D8	ORB0	O	Fast overrange detection status for channel B for the OVR_T0 threshold. When the analog input exceeds the threshold programmed into OVR_T0, this status indicator goes high. The minimum pulse duration is set by OVR_N. See the *ADC Overrange Detection* section for more information. Leave this pin disconnected if not used.
D9	DA3+	O	LVDS output for bit 3 of LVDS bus A. Positive connection. This pin can be left disconnected if not used.
D10	DA3–	O	LVDS output for bit 3 of LVDS bus A. Negative connection. This pin can be left disconnected if not used.
D11	DA9+	O	LVDS output for bit 9 of LVDS bus A. Positive connection. This pin can be left disconnected if not used.
D12	DA9–	O	LVDS output for bit 9 of LVDS bus A. Negative connection. This pin can be left disconnected if not used.
D13	DC3+	O	LVDS output for bit 3 of LVDS bus C. Positive connection. This pin can be left disconnected if not used.
D14	DC3–	O	LVDS output for bit 3 of LVDS bus C. Negative connection. This pin can be left disconnected if not used.
D15	DC9+	O	LVDS output for bit 9 of LVDS bus C. Positive connection. This pin can be left disconnected if not used.
D16	DC9–	O	LVDS output for bit 9 of LVDS bus C. Negative connection. This pin can be left disconnected if not used.

Table 4-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
E1	TMSTP–	I	Timestamp input negative connection or differential LVDS SYNC negative connection. This pin can be left disconnected and disabled (TMSTP_RECV_EN = 0) if $\overline{\text{SYNCSE}}$ is used for the LVDS SYNC signal and timestamp is not required.
E2	$\overline{\text{SYNCSE}}$	I	LVDS interface SYNC signal, single-ended active low input used to control sending strobe signals for synchronization or digital interface test patterns. The *Digital Interface Test Patterns* section describes using the SYNC signal in more detail. The choice of single-ended or differential SYNC (using the TMSTP+ and TMSTP– pins) is selected by programming SYNC_SEL. Tie this pin to ground if differential SYNC (TMSTP±) is used as the SYNC signal.
E3	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
E4	VA11	I	1.1V analog supply
E5	VA11	I	1.1V analog supply
E6	VA11	I	1.1V analog supply
E7	DGND	—	Digital supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
E8	VD11	I	1.1V digital supply
E9	DA4+	O	LVDS output for bit 4 of LVDS bus A. Positive connection. This pin can be left disconnected if not used.
E10	DA4–	O	LVDS output for bit 4 of LVDS bus A. Negative connection. This pin can be left disconnected if not used.
E11	DA10+	O	LVDS output for bit 10 of LVDS bus A. Positive connection. This pin can be left disconnected if not used.
E12	DA10–	O	LVDS output for bit 10 of LVDS bus A. Negative connection. This pin can be left disconnected if not used.
E13	DC4+	O	LVDS output for bit 4 of LVDS bus C. Positive connection. This pin can be left disconnected if not used.
E14	DC4–	O	LVDS output for bit 4 of LVDS bus C. Negative connection. This pin can be left disconnected if not used.
E15	DC10+	O	LVDS output for bit 10 of LVDS bus C. Positive connection. This pin can be left disconnected if not used.
E16	DC10–	O	LVDS output for bit 10 of LVDS bus C. Negative connection. This pin can be left disconnected if not used.
F1	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
F2	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
F3	VA11	I	1.1V analog supply
F4	VA11	I	1.1V analog supply
F5	VA11	I	1.1V analog supply
F6	VA11	I	1.1V analog supply
F7	DGND	—	Digital supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
F8	VD11	I	1.1-V digital supply
F9	DA5+	O	LVDS output for bit 5 of LVDS bus A. Positive connection. This pin can be left disconnected if not used.
F10	DA5–	O	LVDS output for bit 5 of LVDS bus A. Negative connection. This pin can be left disconnected if not used.
F11	DA11+	O	LVDS output for bit 11 of LVDS bus A. Positive connection. This pin can be left disconnected if not used.
F12	DA11–	O	LVDS output for bit 11 of LVDS bus A. Negative connection. This pin can be left disconnected if not used.
F13	DC5+	O	LVDS output for bit 5 of LVDS bus C. Positive connection. This pin can be left disconnected if not used.
F14	DC5–	O	LVDS output for bit 5 of LVDS bus C. Negative connection. This pin can be left disconnected if not used.
F15	DC11+	O	LVDS output for bit 11 of LVDS bus C. Positive connection. This pin can be left disconnected if not used.
F16	DC11–	O	LVDS output for bit 11 of LVDS bus C. Negative connection. This pin can be left disconnected if not used.
G1	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
G2	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
G3	VA19	I	1.9V analog supply
G4	VA19	I	1.9V analog supply
G5	VA19	I	1.9V analog supply

Table 4-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
G6	VA19	I	1.9V analog supply
G7	DGND	—	Digital supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
G8	VD11	I	1.1-V digital supply
G9	DACLK+	O	LVDS output for data clock of LVDS bus A. Positive connection. This pin can be left disconnected if not used.
G10	DACLK–	O	LVDS output for data clock of LVDS bus A. Negative connection. This pin can be left disconnected if not used.
G11	VLVDS	I	1.1V to 1.9V LVDS digital interface supply
G12	VLVDS	I	1.1V to 1.9V LVDS digital interface supply
G13	DC6+	O	LVDS output for bit 6 of LVDS bus C. Positive connection. This pin can be left disconnected if not used.
G14	DC6–	O	LVDS output for bit 6 of LVDS bus C. Negative connection. This pin can be left disconnected if not used.
G15	DCCLK+	O	LVDS output for data clock of LVDS bus C. Positive connection. This pin can be left disconnected if not used.
G16	DCCLK–	O	LVDS output for data clock of LVDS bus C. Negative connection. This pin can be left disconnected if not used.
H1	CLK+	I	Device (sampling) clock positive input. TI strongly recommends that the clock signal be AC-coupled to this input for best performance. In single-channel mode, the analog input signal is sampled on both rising and falling edges. In-dual channel mode, the analog signal is sampled on the rising edge. This differential input has an internal untrimmed 100Ω differential termination and is self-biased to the optimal input common-mode voltage as long as DEVCLK_LVPECL_EN is set to 0.
H2	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
H3	VA19	I	1.9V analog supply
H4	VA19	I	1.9V analog supply
H5	VA19	I	1.9V analog supply
H6	VA19	I	1.9V analog supply
H7	DGND	—	Digital supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
H8	DGND	—	Digital supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
H9	DASTR+	O	LVDS output for data strobe of LVDS bus A. Positive connection. This pin can be left disconnected if not used.
H10	DASTR–	O	LVDS output for data strobe of LVDS bus A. Negative connection. This pin can be left disconnected if not used.
H11	VLVDS	I	1.1V to 1.9V LVDS digital interface supply
H12	VLVDS	I	1.1V to 1.9V LVDS digital interface supply
H13	VLVDS	I	1.1V to 1.9V LVDS digital interface supply
H14	DGND	—	Digital supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
H15	DCSTR+	O	LVDS output for data strobe of LVDS bus C. Positive connection. This pin can be left disconnected if not used.
H16	DCSTR–	O	LVDS output for data strobe of LVDS bus C. Negative connection. This pin can be left disconnected if not used.
J1	CLK–	I	Device (sampling) clock negative input. TI strongly recommends that the clock signal be AC-coupled to this input for best performance.
J2	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
J3	VA19	I	1.9V analog supply
J4	VA19	I	1.9V analog supply
J5	VA19	I	1.9V analog supply
J6	VA19	I	1.9V analog supply
J7	DGND	—	Digital supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
J8	DGND	—	Digital supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.

Table 4-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
J9	DBSTR+	O	LVDS output for data strobe of LVDS bus B. Positive connection. This pin can be left disconnected if not used.
J10	DBSTR–	O	LVDS output for data strobe of LVDS bus B. Negative connection. This pin can be left disconnected if not used.
J11	VLVDS	I	1.1V to 1.9V LVDS digital interface supply
J12	VLVDS	I	1.1V to 1.9V LVDS digital interface supply
J13	VLVDS	I	1.1V to 1.9V LVDS digital interface supply
J14	DGND	—	Digital supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
J15	DDSTR+	O	LVDS output for data strobe of LVDS bus D. Positive connection. This pin can be left disconnected if not used.
J16	DDSTR–	O	LVDS output for data strobe of LVDS bus D. Negative connection. This pin can be left disconnected if not used.
K1	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
K2	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
K3	VA19	I	1.9V analog supply
K4	VA19	I	1.9V analog supply
K5	VA19	I	1.9V analog supply
K6	VA19	I	1.9V analog supply
K7	DGND	—	Digital supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
K8	VD11	I	1.1V digital supply
K9	DBCLK+	O	LVDS output for data clock of LVDS bus B. Positive connection. This pin can be left disconnected if not used.
K10	DBCLK–	O	LVDS output for data clock of LVDS bus B. Negative connection. This pin can be left disconnected if not used.
K11	VLVDS	I	1.1V to 1.9V LVDS digital interface supply
K12	VLVDS	I	1.1V to 1.9V LVDS digital interface supply
K13	DD6+	O	LVDS output for bit 6 of LVDS bus D. Positive connection. This pin can be left disconnected if not used.
K14	DD6–	O	LVDS output for bit 6 of LVDS bus D. Negative connection. This pin can be left disconnected if not used.
K15	DDCLK+	O	LVDS output for data clock of LVDS bus D. Positive connection. This pin can be left disconnected if not used.
K16	DDCLK–	O	LVDS output for data clock of LVDS bus D. Negative connection. This pin can be left disconnected if not used.
L1	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
L2	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
L3	VA11	I	1.1V analog supply
L4	VA11	I	1.1V analog supply
L5	VA11	I	1.1V analog supply
L6	VA11	I	1.1V analog supply
L7	DGND	—	Digital supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
L8	VD11	I	1.1-V digital supply
L9	DB5+	O	LVDS output for bit 5 of LVDS bus B. Positive connection. This pin can be left disconnected if not used.
L10	DB5–	O	LVDS output for bit 5 of LVDS bus B. Negative connection. This pin can be left disconnected if not used.
L11	DB11+	O	LVDS output for bit 11 of LVDS bus B. Positive connection. This pin can be left disconnected if not used.
L12	DB11–	O	LVDS output for bit 11 of LVDS bus B. Negative connection. This pin can be left disconnected if not used.
L13	DD5+	O	LVDS output for bit 5 of LVDS bus D. Positive connection. This pin can be left disconnected if not used.
L14	DD5–	O	LVDS output for bit 5 of LVDS bus D. Negative connection. This pin can be left disconnected if not used.

Table 4-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
L15	DD11+	O	LVDS output for bit 11 of LVDS bus D. Positive connection. This pin can be left disconnected if not used.
L16	DD11–	O	LVDS output for bit 11 of LVDS bus D. Negative connection. This pin can be left disconnected if not used.
M1	SYSREF+	I	SYSREF input positive connection. The SYSREF input is used to achieve synchronization between multiple ADC12DLx500 devices and deterministic latency across the LVDS data interface. This differential input (SYSREF+ to SYSREF–) has an internal untrimmed 100Ω differential termination and can be AC-coupled when SYSREF_LVPECL_EN is set to 0. This input is self-biased when SYSREF_LVPECL_EN is set to 0. The termination changes to 50Ω to ground on each input pin (SYSREF+ and SYSREF–) and can be DC-coupled when SYSERF_LVPECL_EN is set to 1. This input is not self-biased when SYSERF_LVPECL is set to 1 and must be biased externally to the input common-mode voltage range provided in the *Recommended Operating Conditions* table.
M2	TDIODE+	I	Temperature diode positive (anode) connection. An external temperature sensor can be connected to TDIODE+ and TDIODE– to monitor the junction temperature of the device. This pin can be left disconnected if not used.
M3	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
M4	VA11	I	1.1V analog supply
M5	VA11	I	1.1V analog supply
M6	VA11	I	1.1V analog supply
M7	DGND	—	Digital supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
M8	VD11	I	1.1V digital supply
M9	DB4+	O	LVDS output for bit 4 of LVDS bus B. Positive connection. This pin can be left disconnected if not used.
M10	DB4–	O	LVDS output for bit 4 of LVDS bus B. Negative connection. This pin can be left disconnected if not used.
M11	DB10+	O	LVDS output for bit 10 of LVDS bus B. Positive connection. This pin can be left disconnected if not used.
M12	DB10–	O	LVDS output for bit 10 of LVDS bus B. Negative connection. This pin can be left disconnected if not used.
M13	DD4+	O	LVDS output for bit 4 of LVDS bus D. Positive connection. This pin can be left disconnected if not used.
M14	DD4–	O	LVDS output for bit 4 of LVDS bus D. Negative connection. This pin can be left disconnected if not used.
M15	DD10+	O	LVDS output for bit 10 of LVDS bus D. Positive connection. This pin can be left disconnected if not used.
M16	DD10–	O	LVDS output for bit 10 of LVDS bus D. Negative connection. This pin can be left disconnected if not used.
N1	SYSREF–	I	SYSREF input negative connection. See SYSREF+ (pin M1) for detailed description.
N2	TDIODE–	I	Temperature diode negative (cathode) connection. This pin can be left disconnected if not used.
N3	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
N4	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
N5	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
N6	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
N7	DGND	—	Digital supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
N8	SDO	O	Serial programming interface (SPI) data output. The *Using the Serial Interface* section describes the serial interface in more detail. This pin is high impedance during normal device operation. This pin outputs 1.9V CMOS levels during serial interface read operations. This pin can be left disconnected if not used.
N9	DB3+	O	LVDS output for bit 3 of LVDS bus B. Positive connection. This pin can be left disconnected if not used.
N10	DB3–	O	LVDS output for bit 3 of LVDS bus B. Negative connection. This pin can be left disconnected if not used.
N11	DB9+	O	LVDS output for bit 9 of LVDS bus B. Positive connection. This pin can be left disconnected if not used.
N12	DB9–	O	LVDS output for bit 9 of LVDS bus B. Negative connection. This pin can be left disconnected if not used.
N13	DD3+	O	LVDS output for bit 3 of LVDS bus D. Positive connection. This pin can be left disconnected if not used.
N14	DD3–	O	LVDS output for bit 3 of LVDS bus D. Negative connection. This pin can be left disconnected if not used.
N15	DD9+	O	LVDS output for bit 9 of LVDS bus D. Positive connection. This pin can be left disconnected if not used.
N16	DD9–	O	LVDS output for bit 9 of LVDS bus D. Negative connection. This pin can be left disconnected if not used.

Table 4-1. Pin Functions (continued)

PIN NO.	PIN NAME	TYPE	DESCRIPTION
P1	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
P2	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
P3	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
P4	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
P5	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
P6	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
P7	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
P8	SDI	I	Serial programming interface (SPI) data input. The *Using the Serial Interface* section describes the serial interface in more detail. Supports 1.1V and 1.8V CMOS levels.
P9	DB2+	O	LVDS output for bit 2 of LVDS bus B. Positive connection. This pin can be left disconnected if not used.
P10	DB2–	O	LVDS output for bit 2 of LVDS bus B. Negative connection. This pin can be left disconnected if not used.
P11	DB8+	O	LVDS output for bit 8 of LVDS bus B. Positive connection. This pin can be left disconnected if not used.
P12	DB8–	O	LVDS output for bit 8 of LVDS bus B. Negative connection. This pin can be left disconnected if not used.
P13	DD2+	O	LVDS output for bit 2 of LVDS bus D. Positive connection. This pin can be left disconnected if not used.
P14	DD2–	O	LVDS output for bit 2 of LVDS bus D. Negative connection. This pin can be left disconnected if not used.
P15	DD8+	O	LVDS output for bit 8 of LVDS bus D. Positive connection. This pin can be left disconnected if not used.
P16	DD8–	O	LVDS output for bit 8 of LVDS bus D. Negative connection. This pin can be left disconnected if not used.
R1	PD	I	This pin disables all analog circuits and LVDS outputs when set high to save power or for temperature diode calibration. Tie this pin to ground during normal operation.
R2	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
R3	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
R4	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
R5	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
R6	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
R7	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
R8	$\overline{\text{SCS}}$	I	Serial programming interface (SPI) chip-select active low input. The *Using the Serial Interface* section describes the serial interface in more detail. Supports 1.1-V and 1.8-V CMOS levels. This pin has an 82-kΩ pullup resistor to VD11.
R9	DB1+	O	LVDS output for bit 1 of LVDS bus B. Positive connection. This pin can be left disconnected if not used.
R10	DB1–	O	LVDS output for bit 1 of LVDS bus B. Negative connection. This pin can be left disconnected if not used.
R11	DB7+	O	LVDS output for bit 7 of LVDS bus B. Positive connection. This pin can be left disconnected if not used.
R12	DB7–	O	LVDS output for bit 7 of LVDS bus B. Negative connection. This pin can be left disconnected if not used.
R13	DD1+	O	LVDS output for bit 1 of LVDS bus D. Positive connection. This pin can be left disconnected if not used.
R14	DD1–	O	LVDS output for bit 1 of LVDS bus D. Negative connection. This pin can be left disconnected if not used.
R15	DD7+	O	LVDS output for bit 7 of LVDS bus D. Positive connection. This pin can be left disconnected if not used.
R16	DD7–	O	LVDS output for bit 7 of LVDS bus D. Negative connection. This pin can be left disconnected if not used.
T1	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
T2	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
T3	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
T4	INB+	I	Channel B analog input positive connection. The differential full-scale input range is determined by the FS_RANGE_B register; see the *Full-Scale Voltage (VFS) Adjustment* section. This input is terminated to AGND through a 50-Ω termination resistor. The input common-mode voltage must typically be set to 0 V (GND) and must follow the recommendations in the *Recommended Operating Conditions* table. This pin can be left disconnected if not used.
T5	INB–	I	Channel B analog input negative connection. See INB+ (pin T4) for detailed description. This input is terminated to ground through a 50Ω termination resistor. This pin can be left disconnected if not used.
T6	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.

Table 4-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
T7	AGND	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
T8	SCLK	I	Serial programming interface (SPI) clock. This pin functions as the serial-interface clock input that clocks the serial programming data in and out. The *Using the Serial Interface* section describes the serial interface in more detail. Supports 1.1V and 1.8V CMOS levels.
T9	DB0+	O	LVDS output for bit 0 of LVDS bus B. Positive connection. This pin can be left disconnected if not used.
T10	DB0–	O	LVDS output for bit 0 of LVDS bus B. Negative connection. This pin can be left disconnected if not used.
T11	DB6+	O	LVDS output for bit 6 of LVDS bus B. Positive connection. This pin can be left disconnected if not used.
T12	DB6–	O	LVDS output for bit 6 of LVDS bus B. Negative connection. This pin can be left disconnected if not used.
T13	DD0+	O	LVDS output for bit 0 of LVDS bus D. Positive connection. This pin can be left disconnected if not used.
T14	DD0–	O	LVDS output for bit 0 of LVDS bus D. Negative connection. This pin can be left disconnected if not used.
T15	DGND	—	Digital supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
T16	DGND	—	Digital supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage range	VA19[2]	–0.3	2.35	V
	VA11[2]	–0.3	1.32	
	VD11[3]	–0.3	1.32	
	VLVDS[3]	–0.3	2.35	
	Voltage between VD11 and VA11	–1.32	1.32	
Voltage between AGND and DGND		–0.1	0.1	V
Pin voltage range	DACLK+, DACLK–, DASTR+, DASTR–, DA[11:0]+, DA[11:0]–, DBCLK+, DBCLK–, DBSTR+, DBSTR–, DB[11:0]+, DB[11:0]–, DCCLK+, DCCLK–, DCSTR+, DCSTR–, DC[11:0]+, DC[11:0]–, DDCLK+, DDCLK–, DDSTR+, DDSTR–, DD[11:0]+, DD[11:0]–[3]	–0.5	VLVDS + 0.5[7]	V
	CLK+, CLK–, SYSREF+, SYSREF–[2]	–0.5	VA11 + 0.5[5]	
	TMSTP+, TMSTP–[3]	–0.5	VD11 + 0.5[6]	
	BG, TDIODE+, TDIODE–[2]	–0.5	VA19 + 0.5[4]	
	INA+, INA–, INB+, INB–[2]	–1	1	
	CALSTAT, CALTRIG, ORA0, ORA1, ORB0, ORB1, PD, SCLK, $\overline{\text{SCS}}$, SDI, SDO, $\overline{\text{SYNCSE}}$ [2]	–0.5	VA19 + 0.5[4]	
Peak input current (any input except INA+, INA–, INB+, INB–)		–25	25	mA
Peak input current (INA+, INA–, INB+, INB–)		–50	50	mA
Peak RF input power (INA+, INA–, INB+, INB–)	Single-ended with $Z_{S\text{-}SE}$ = 50 Ω or differential with $Z_{S\text{-}DIFF}$ = 100 Ω		16.4	dBm
Peak total input current (sum of absolute value of all currents forced in or out, not including power supply current)			100	mA
Operating junction temperature, T_j			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured to AGND.
(3) Measured to DGND.
(4) Maximum voltage not to exceed VA19 absolute maximum rating.
(5) Maximum voltage not to exceed VA11 absolute maximum rating.
(6) Maximum voltage not to exceed VD11 absolute maximum rating.
(7) Maximum voltage not to exceed VLVDS absolute maximum rating.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage range	VA19, analog 1.9-V supply[(2)]	1.8	1.9	2.0	V
		VA11, analog 1.1-V supply[(2)]	1.05	1.1	1.15	
		VD11, digital 1.1-V supply[(3)]	1.05	1.1	1.15	
		VLVDS, LVDS interface supply[(3)]	1.05	1.9	2.0	
V_{CMI}	Input common-mode voltage	INA+, INA–, INB+, INB–[(2)]	-50	0	110	mV
		CLK+, CLK–, SYSREF+, SYSREF–[(2) (4)]	0	0.3	0.55	V
		TMSTP+, TMSTP–[(3) (5)]	0	0.3	0.55	
V_{ID}	Input voltage, peak-to-peak differential	CLK+ to CLK–, SYSREF+ to SYSREF–, TMSTP+ to TMSTP–	0.4	1.0	2.0	$V_{PP\text{-}DIFF}$
		INA+ to INA–, INB+ to INB–			1.0[(6)]	
V_{IH}	High-level input voltage	CALTRIG, PD, SCLK, $\overline{SCS}$, SDI, $\overline{SYNCSE}$ [(2)]	0.7			V
V_{IL}	Low-level input voltage	CALTRIG, PD, SCLK, $\overline{SCS}$, SDI, $\overline{SYNCSE}$ [(2)]			0.45	V
I_{C_TD}	Temperature diode input current	TDIODE+ to TDIODE–		100		µA
C_L	BG maximum load capacitance				100	pF
I_O	BG maximum output current				100	µA
DC	Input clock duty cycle		30%	50%	70%	
T_A	Operating free-air temperature	ADC12DL500 ADC12DL1500, ADC12DL2500	0[(7)] -40[(8)]		85	ºC
T_j	Operating junction temperature				105[(1)]	ºC

(1) Prolonged use above this junction temperature may increase the device failure-in-time (FIT) rate.
(2) Measured to AGND.
(3) Measured to DGND.
(4) It is strongly recommended that CLK± be AC coupled with DEVCLK_LVPECL_EN set to 0 to allow CLK± to self bias to the optimal input common mode voltage for best performance. TI recommends AC coupling for SYSREF± unless DC coupling is required, in which case LVPECL input mode must be used (SYSREF_LVPECL_EN = 1).
(5) TMSTP± does not have internal biasing which requires TMSTP± to be biased externally whether AC coupled with TMSTP_LVPECL_EN = 0 or DC coupled with TMSTP_LVPECL_EN = 1.
(6) ADC output code will saturate when VID for INA+/– or INB+/– exceeds the programmed full-scale voltage (V_{FS}) set by FS_RANGE_A for INA± or FS_RANGE_B for INB±.
(7) ADC12DL500 min. operating free-air temperature
(8) ADC12DL1500/2500 min. operating free-air temperature

5.4 Thermal Information

THERMAL METRIC[(1)]		ACF (FCBGA)	UNIT
		256 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	16.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.94	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	5.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the spra953 application report.

5.5 Electrical Characteristics: DC Specifications

Typical values at T_A = +25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-$V_{PP-DIFF}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM), foreground calibration; minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in the *Recommended Operating Conditions* table.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC ACCURACY						
	Resolution	Resolution with no missing codes		12		Bits
ADC12DL500						
DNL	Differential nonlinearity	Maximum positive excursion from ideal step size		0.17		LSB
		Maximum negative excursion from ideal step size		-0.14		
INL	Integral nonlinearity	Maximum positive excursion from ideal transfer function		1		LSB
		Maximum negative excursion from ideal transfer function		-1.5		
ADC12DL1500						
DNL	Differential nonlinearity	Maximum positive excursion from ideal step size		0.14		LSB
		Maximum negative excursion from ideal step size		-0.14		
INL	Integral nonlinearity	Maximum positive excursion from ideal transfer function		1		LSB
		Maximum negative excursion from ideal transfer function		-1		
ADC12DL2500						
DNL	Differential nonlinearity	Maximum positive excursion from ideal step size		0.17		LSB
		Maximum negative excursion from ideal step size		-0.19		
INL	Integral nonlinearity	Maximum positive excursion from ideal transfer function		2.3		LSB
		Maximum negative excursion from ideal transfer function		-1		
ANALOG INPUTS (INA±, INB±)						
V_{OFF}	Offset Error	CAL_OS = 0		±2.0		mV
		CAL_OS = 1		±0.3		mV
V_{OFF_ADJ}	Input offset voltage adjustment range	Available offset correction range (see CAL_OS bit in the CAL_CFGO register or the OADJ_A_FG0_VINA register)		±55		mV
V_{OFF_DRIFT}	Offset drift	Foreground calibration at nominal temperature only		14		µV/°C
		Foreground calibration at each temperature		4		
V_{IN_FSR}	Analog differential input full-scale range	Default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000)		800		mV_{PP}
		Maximum full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xFFFF)		1040		
		Minimum full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0x2000)		480		
$V_{IN\_FSR\_DRIFT}$	Analog differential input full-scale range drift	Default FS_RANGE_A and FS_RANGE_B setting, foreground calibration at nominal temperature only, inputs driven by 50-Ω source, includes effect of R_{IN} drift		0.037		%/°C
		Default FS_RANGE_A and FS_RANGE_B setting, foreground calibration at each temperature, inputs driven by 50-Ω source, includes effect of R_{IN} drift		0.006		
$V_{IN\_FSR\_MATCH}$	Analog differential input full-scale range matching	Matching between INA± and INB±, default setting, dual channel mode		0.53		%
R_{IN}	Single-ended input resistance to AGND	Each input terminal is terminated to AGND, measured at T_A = 25°C		50		Ω
R_{IN_TEMPCO}	Input termination linear temperature coefficient			11.6		mΩ/°C
C_{IN}	Single-ended input capacitance	Single-channel mode measured at DC		0.45		pF
		Dual-channel mode measured at DC		0.45		
TEMPERATURE DIODE CHARACTERISTICS (TDIODE±)						
ΔV_{BE}	Temperature diode voltage slope	Forced forward current of 100 µA. Offset voltage (approximately 0.792 V at 0°C) varies with process and must be measured for each part. Perform offset measurements with the device unpowered or with the PD pin asserted to minimize device self-heating.		-1.5		mV/°C

5.5 Electrical Characteristics: DC Specifications (continued)

Typical values at T_A = +25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-$V_{PP-DIFF}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM), foreground calibration; minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in the *Recommended Operating Conditions* table.

<table>
<tr><th colspan="2">PARAMETER</th><th>TEST CONDITIONS</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr>
<tr><td colspan="7">BANDGAP VOLTAGE OUTPUT (BG)</td></tr>
<tr><td>V_{BG}</td><td>Reference output voltage</td><td>I_L ≤ 100 µA</td><td></td><td>1.1</td><td></td><td>V</td></tr>
<tr><td>V_{BG_DRIFT}</td><td>Reference output temperature drift</td><td>I_L ≤ 100 µA</td><td></td><td>-125</td><td></td><td>µV/°C</td></tr>
<tr><td colspan="7">CLOCK INPUTS (CLK±, SYSREF±, TMSTP±)</td></tr>
<tr><td rowspan="2">Z_T</td><td rowspan="2">Internal termination</td><td>Differential termination with DEVCLK_LVPECL_EN = 0, SYSREF_LVPECL_EN = 0 and TMSTP_LVPECL_EN = 0</td><td></td><td>100</td><td></td><td rowspan="2">Ω</td></tr>
<tr><td>Single ended termination to GND (per pin) with DEVCLK_LVPECL_EN = 0, SYSREF_LVPECL_EN = 0 and TMSTP_LVPECL_EN = 0</td><td></td><td>50</td><td></td></tr>
<tr><td rowspan="3">V_{CM}</td><td rowspan="3">Input common-mode voltage, self-biased</td><td>Self-biasing common-mode voltage for CLK± when AC coupled (DEVCLK_LVPECL_EN must be set to 0)</td><td></td><td>0.3</td><td></td><td rowspan="3">V</td></tr>
<tr><td>Self-biasing common-mode voltage for SYSREF± when AC coupled (SYSREF_LVPECL_EN must be set to 0) and with receiver enabled (SYSREF_RECV_EN = 1).</td><td></td><td>0.3</td><td></td></tr>
<tr><td>Self-biasing common-mode voltage for SYSREF± when AC coupled (SYSREF_LVPECL_EN must be set to 0) and with receiver disabled (SYSREF_RECV_EN = 0).</td><td></td><td>VA11</td><td></td></tr>
<tr><td>C_{L_DIFF}</td><td>Differential input capacitance</td><td>Between positive and negative differential input pins</td><td></td><td>0.1</td><td></td><td>pF</td></tr>
<tr><td>C_{L_SE}</td><td>Single-ended input capacitance</td><td>Each input to ground</td><td></td><td>0.5</td><td></td><td>pF</td></tr>
<tr><td colspan="7">LVDS OUTPUTS (DACLK±, DASTR±, DA[11:0]±, DBCLK±, DBSTR±, DB[11:0]±, DCCLK±, DCSTR±, DC[11:0]±, DDCLK±, DDSTR±, DD[11:0]±)</td></tr>
<tr><td rowspan="3">V_{DIFF}</td><td rowspan="3">Differential output peak-to-peak voltage, DC measurement</td><td>Default swing (HSM), 100-Ω load</td><td></td><td>720</td><td></td><td rowspan="3">$mV_{PP-DIFF}$</td></tr>
<tr><td>Low swing (LSM), 100-Ω load</td><td></td><td>350</td><td></td></tr>
<tr><td>Low swing high-Z mode (HZM), high-impedance load</td><td></td><td>380</td><td></td></tr>
<tr><td rowspan="2">V_{CM}</td><td rowspan="2">Output common-mode voltage, tracks with VLVDS</td><td>VLVDS = 1.9 V</td><td></td><td>1.3</td><td></td><td rowspan="2">V</td></tr>
<tr><td>VLVDS = 1.1 V</td><td></td><td>0.5</td><td></td></tr>
<tr><td>I_{OS_DIFF}</td><td>Differential short-circuit current</td><td>Positive and negative outputs shorted together</td><td></td><td>5</td><td></td><td>mA</td></tr>
<tr><td>I_{OS_GND}</td><td>Short-circuit current to ground</td><td>Either positive or negative output tied to ground</td><td></td><td>20</td><td></td><td>mA</td></tr>
<tr><td>Z_{DIFF}</td><td>Differential output impedance</td><td>Measured at DC</td><td></td><td>300</td><td></td><td>Ω</td></tr>
</table>

5.5 Electrical Characteristics: DC Specifications (continued)

Typical values at T_A = +25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-$V_{PP\text{-}DIFF}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM), foreground calibration; minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in the *Recommended Operating Conditions* table.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMOS INTERFACE: SCLK, SDI, SDO, $\overline{\text{SCS}}$, PD, CALSTAT, CALTRIG, ORA0, ORA1, ORB0, ORB1, $\overline{\text{SYNCSE}}$						
I_{IH}	High-level input current				40	µA
I_{IL}	Low-level input current		–40			µA
C_I	Input capacitance			2		pF
V_{OH}	High-level output voltage	I_{LOAD} = –400 µA	1.65			V
V_{OL}	Low-level output voltage	I_{LOAD} = 400 µA			150	mV

5.6 Electrical Characteristics: Power Consumption

Typical values at T_A = +25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-$V_{PP-DIFF}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM), foreground calibration.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC12DL500						
I_{VA19}	1.9-V analog supply current	Power mode 1: single-channel mode, demux-by-2, foreground calibration, V_{LVDS} = 1.9 V		835		mA
I_{VA11}	1.1-V analog supply current			185		mA
I_{VD11}	1.1-V digital supply current			40		mA
I_{VLVDS}	LVDS interface supply current			389		mA
P_{DIS}	Power dissipation			2.58		W
I_{VA19}	1.9-V analog supply current	Power mode 2: dual-channel mode, demux-by-2, foreground calibration, V_{LVDS} = 1.9 V		913		mA
I_{VA11}	1.1-V analog supply current			185		mA
I_{VD11}	1.1-V digital supply current			35		mA
I_{VLVDS}	LVDS interface supply current			389		mA
P_{DIS}	Power dissipation			2.72		W
I_{VA19}	1.9-V analog supply current	Power mode 3: PD pin held high, no clock, V_{LVDS} = 1.9 V		33		mA
I_{VA11}	1.1-V analog supply current			23		mA
I_{VD11}	1.1-V digital supply current			3		mA
I_{VLVDS}	LVDS interface supply current			0		mA
P_{DIS}	Power dissipation			0.1		W
ADC12DL1500						
I_{VA19}	1.9-V analog supply current	Power mode 1: single-channel mode, demux-by-2, foreground calibration, V_{LVDS} = 1.9 V		834		mA
I_{VA11}	1.1-V analog supply current			300		mA
I_{VD11}	1.1-V digital supply current			113		mA
I_{VLVDS}	LVDS interface supply current			389		mA
P_{DIS}	Power dissipation			2.78		W
I_{VA19}	1.9-V analog supply current	Power mode 2: dual-channel mode, demux-by-2, foreground calibration, V_{LVDS} = 1.9 V		912		mA
I_{VA11}	1.1-V analog supply current			299		mA
I_{VD11}	1.1-V digital supply current			98		mA
I_{VLVDS}	LVDS interface supply current			389		mA
P_{DIS}	Power dissipation			2.91		W
I_{VA19}	1.9-V analog supply current	Power mode 3: PD pin held high, no clock, V_{LVDS} = 1.9 V		33		mA
I_{VA11}	1.1-V analog supply current			23		mA
I_{VD11}	1.1-V digital supply current			3		mA
I_{VLVDS}	LVDS interface supply current			0		mA
P_{DIS}	Power dissipation			0.1		W
ADC12DL2500						
I_{VA19}	1.9-V analog supply current	Power mode 1: single-channel mode, demux-by-2, foreground calibration, V_{LVDS} = 1.9 V		833		mA
I_{VA11}	1.1-V analog supply current			419		mA
I_{VD11}	1.1-V digital supply current			188		mA
I_{VLVDS}	LVDS interface supply current			388		mA
P_{DIS}	Power dissipation			2.99		W
I_{VA19}	1.9-V analog supply current	Power mode 2: dual-channel mode, demux-by-2, foreground calibration, V_{LVDS} = 1.9 V		911		mA
I_{VA11}	1.1-V analog supply current			419		mA
I_{VD11}	1.1-V digital supply current			169		mA
I_{VLVDS}	LVDS interface supply current			389		mA
P_{DIS}	Power dissipation			3.12		W

5.6 Electrical Characteristics: Power Consumption (continued)

Typical values at T_A = +25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-$V_{PP\text{-}DIFF}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM), foreground calibration.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VA19}	1.9-V analog supply current	Power mode 3: PD pin held high, no clock, V_{LVDS} = 1.9 V		33		mA
I_{VA11}	1.1-V analog supply current			23		mA
I_{VD11}	1.1-V digital supply current			3		mA
I_{VLVDS}	LVDS interface supply current			0		mA
P_{DIS}	Power dissipation			0.1		W

5.7 Electrical Characteristics: AC Specifications (Dual-Channel Mode)

Typical values at T_A = +25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-$V_{PP-DIFF}$ sine-wave clock, DES_EN = 0, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM), foreground calibration; minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in the Recommending Operating Conditions table.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC12DL500						
FPBW	Full-power input bandwidth (–3 dB)[1]	Foreground calibration		8.0		GHz
XTALK	Channel-to-channel crosstalk	Aggressor = 400 MHz, –1 dBFS		-94		dB
CER	Code error rate	Maximum CER		10^{-18}		errors/ sample
NSD	Noise spectral density, no input signal	Maximum full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xFFFF) setting		-143.5		dBFS/Hz
		Default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000) setting		-142.3		
NF	Noise figure	Maximum full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xFFFF) setting, no input, Z_S = 100 Ω		31.5		dB
		Default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000) setting, no input, Z_S = 100 Ω		30.7		
$NOISE_{DC}$	DC input noise standard deviation	No input, excludes DC offset, includes fixed interleaving spur (F_S/2 spur)		1.8		LSB
SNR	Signal-to-noise ratio, large signal, excluding DC, HD2 to HD9 and interleaving spurs	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		56.8		dBFS
		f_{IN} = 97 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting		57.6		
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		56.7		
SNR	Signal-to-noise ratio, small signal, excluding DC, HD2 to HD9 and interleaving spurs	f_{IN} = 97 MHz, AIN = –16 dBFS		57.3		dBFS
		f_{IN} = 347 MHz, A_{IN} = –16 dBFS		57.4		
SINAD	Signal-to-noise and distortion ratio, large signal, excluding DC and F_S/2 fixed spurs	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		56		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		55.9		
ENOB	Effective number of bits, large signal, excluding DC and F_S/2 fixed spurs	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		9.0		bits
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		9.0		
SFDR	Spurious-free dynamic range, large signal, excluding DC and F_S/2 fixed spurs	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		69		dBFS
		f_{IN} = 97 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting		65		
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		67		
SFDR	Spurious-free dynamic range, small signal, excluding DC and F_S/2 fixed spurs	f_{IN} = 97 MHz, A_{IN} = –16 dBFS		75		dBFS
		f_{IN} = 347 MHz, A_{IN} = –16 dBFS		72		
F_S/2	F_S/2 fixed interleaving spur, independent of input signal	No input		-71		dBFS
HD2	2nd-order harmonic	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-75		dBFS
		f_{IN} = 97 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting		-72		
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-67		
HD3	3rd-order harmonic	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-71		dBFS
		f_{IN} = 97 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting		-67		
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-69		
F_S/2-F_{IN}	F_S/2-F_{IN} interleaving spur, signal dependent	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-77		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-71		
SPUR	Worst harmonic 4th-order or higher	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-72		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-71		

5.7 Electrical Characteristics: AC Specifications (Dual-Channel Mode) (continued)

Typical values at T_A = +25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-$V_{PP-DIFF}$ sine-wave clock, DES_EN = 0, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM), foreground calibration; minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in the Recommending Operating Conditions table.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IMD3	3rd-order intermodulation	f_{IN} = 97 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		-82		dBFS
		f_{IN} = 347 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		-80		
ADC12DL1500						
FPBW	Full-power input bandwidth (–3 dB)(1)	Foreground calibration		8.0		GHz
XTALK	Channel-to-channel crosstalk	Aggressor = 400 MHz, –1 dBFS		-93		dB
		Aggressor = 1000 MHz, –1 dBFS		-80		
CER	Code error rate	Maximum CER		10^{-18}		errors/ sample
NSD	Noise spectral density, no input signal	Maximum full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xFFFF) setting		-148.0		dBFS/Hz
		Default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000) setting		-146.7		
NF	Noise figure	Maximum full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xFFFF) setting, no input, Z_S = 100 Ω		27.0		dB
		Default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000) setting, no input, Z_S = 100 Ω		26.3		
$NOISE_{DC}$	DC input noise standard deviation	No input, excludes DC offset, includes fixed interleaving spur (F_S/2 spur)		1.9		LSB
SNR	Signal-to-noise ratio, large signal, excluding DC, HD2 to HD9 and interleaving spurs	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		56.6		dBFS
		f_{IN} = 97 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting		57.3		
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		56.7		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		56.5		
SNR	Signal-to-noise ratio, small signal, excluding DC, HD2 to HD9 and interleaving spurs	f_{IN} = 97 MHz, AIN = –16 dBFS		57		dBFS
		f_{IN} = 347 MHz, A_{IN} = –16 dBFS		56.9		
		f_{IN} = 797 MHz, A_{IN} = –16 dBFS		57.1		
SINAD	Signal-to-noise and distortion ratio, large signal, excluding DC and F_S/2 fixed spurs	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		55.7		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		56.3		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		55.8		
ENOB	Effective number of bits, large signal, excluding DC and F_S/2 fixed spurs	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		9.0		bits
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		9.1		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		9.0		
SFDR	Spurious-free dynamic range, large signal, excluding DC and F_S/2 fixed spurs	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		67		dBFS
		f_{IN} = 97 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting		65		
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		65		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		62		
SFDR	Spurious-free dynamic range, small signal, excluding DC and F_S/2 fixed spurs	f_{IN} = 97 MHz, A_{IN} = –16 dBFS		72		dBFS
		f_{IN} = 347 MHz, A_{IN} = –16 dBFS		72		
		f_{IN} = 797 MHz, A_{IN} = –16 dBFS		73		
F_S/2	F_S/2 fixed interleaving spur, independent of input signal	No input		-74		dBFS

5.7 Electrical Characteristics: AC Specifications (Dual-Channel Mode) (continued)

Typical values at T_A = +25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-$V_{PP-DIFF}$ sine-wave clock, DES_EN = 0, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM), foreground calibration; minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in the Recommending Operating Conditions table.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD2	2nd-order harmonic	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-71		dBFS
		f_{IN} = 97 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting		-71		
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-71		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		-65		
HD3	3rd-order harmonic	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-68		dBFS
		f_{IN} = 97 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting		-66		
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-69		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		-69		
$F_S/2-F_{IN}$	$F_S/2-F_{IN}$ interleaving spur, signal dependent	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-74		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-73		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		-73		
SPUR	Worst harmonic 4th-order or higher	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-72		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-70		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		-70		
IMD3	3rd-order intermodulation	f_{IN} = 97 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		-87		dBFS
		f_{IN} = 347 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		-85		
		f_{IN} = 797 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		-83		
ADC12DL2500						
FPBW	Full-power input bandwidth (–3 dB)(1)	Foreground calibration		8.0		GHz
XTALK	Channel-to-channel crosstalk	Aggressor = 400 MHz, –1 dBFS		-83		dB
		Aggressor = 1000 MHz, –1 dBFS		-76		
		Aggressor = 3000 MHz, –1 dBFS		-59		
CER	Code error rate	Maximum CER		10^{-18}		errors/ sample
NSD	Noise spectral density, no input signal	Maximum full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xFFFF) setting		-149.8		dBFS/Hz
		Default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000) setting		-148.3		
NF	Noise figure	Maximum full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xFFFF) setting, no input, Z_S = 100 Ω		25.2		dB
		Default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000) setting, no input, Z_S = 100 Ω		24.7		
$NOISE_{DC}$	DC input noise standard deviation	No input, excludes DC offset, includes fixed interleaving spur ($F_S/2$ spur)		2.0		LSB
SNR	Signal-to-noise ratio, large signal, excluding DC, HD2 to HD9 and interleaving spurs	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		56.3		dBFS
		f_{IN} = 97 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting		57		
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		56.1		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		56		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS		54.6		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting		55.1		

5.7 Electrical Characteristics: AC Specifications (Dual-Channel Mode) (continued)

Typical values at T_A = +25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-$V_{PP-DIFF}$ sine-wave clock, DES_EN = 0, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM), foreground calibration; minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in the Recommending Operating Conditions table.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio, small signal, excluding DC, HD2 to HD9 and interleaving spurs	f_{IN} = 97 MHz, AIN = –16 dBFS		56.8		dBFS
		f_{IN} = 347 MHz, A_{IN} = –16 dBFS		56.5		
		f_{IN} = 797 MHz, A_{IN} = –16 dBFS		56.7		
		f_{IN} = 2397 MHz, A_{IN} = –16 dBFS		56.7		
SINAD	Signal-to-noise and distortion ratio, large signal, excluding DC and F_S/2 fixed spurs	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		55.9		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		55.7		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		54.6		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS		53.2		
ENOB	Effective number of bits, large signal, excluding DC and F_S/2 fixed spurs	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		9.0		bits
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		9.0		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		8.8		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS		8.5		
SFDR	Spurious-free dynamic range, large signal, excluding DC and F_S/2 fixed spurs	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		65		dBFS
		f_{IN} = 97 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting		65		
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		66		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		64		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS		60		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting		56		
SFDR	Spurious-free dynamic range, small signal, excluding DC and F_S/2 fixed spurs	f_{IN} = 97 MHz, A_{IN} = –16 dBFS		74		dBFS
		f_{IN} = 347 MHz, A_{IN} = –16 dBFS		72		
		f_{IN} = 797 MHz, A_{IN} = –16 dBFS		72		
		f_{IN} = 2397 MHz, A_{IN} = –16 dBFS		73		
F_S/2	F_S/2 fixed interleaving spur, independent of input signal	No input		-75		dBFS
HD2	2nd-order harmonic	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-76		dBFS
		f_{IN} = 97 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting		-71		
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-73		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		-68		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS		-62		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting		-59		
HD3	3rd-order harmonic	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-68		dBFS
		f_{IN} = 97 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting		-66		
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-68		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		-65		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS		-63		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting		-58		
$F_S/2-F_{IN}$	$F_S/2-F_{IN}$ interleaving spur, signal dependent	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-72		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-72		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		-74		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS		-68		

5.7 Electrical Characteristics: AC Specifications (Dual-Channel Mode) (continued)

Typical values at T_A = +25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-$V_{PP-DIFF}$ sine-wave clock, DES_EN = 0, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM), foreground calibration; minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in the Recommending Operating Conditions table.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPUR	Worst harmonic 4^{th}-order or higher	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-71		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-70		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		-69		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS		-69		
IMD3	3^{rd}-order intermodulation	f_{IN} = 97 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		-80		dBFS
		f_{IN} = 347 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		-79		
		f_{IN} = 797 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		-83		
		f_{IN} = 2397 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		-69		

(1) Full-power input bandwidth (FPBW) is defined as the input frequency where the reconstructed output of the ADC has dropped 3 dB below the power of a full-scale input signal at a low input frequency. Useable bandwidth may exceed the –3-dB full-power input bandwidth.

5.8 Electrical Characteristics: AC Specifications (Single-Channel Mode)

Typical values at T_A = +25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-$V_{PP-DIFF}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM), foreground calibration; minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in the Recommended Operating Conditions table.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC12DL500						
FPBW	Full-power input bandwidth (–3 dB)[1]	Foreground calibration		7.5		GHz
CER	Code error rate	Maximum CER		10^{-18}		errors/sample
NSD	Noise spectral density, no input signal, excludes fixed interleaving spurs (F_S/2 and F_S/4 spurs)	Maximum full-scale voltage (FS_RANGE_A = 0xFFFF) setting		-146.2		dBFS/Hz
		Default full-scale voltage (FS_RANGE_A = 0xA000) setting		-144.4		
NF	Noise figure	Maximum full-scale voltage (FS_RANGE_A = 0xFFFF) setting, no input, Z_S = 100 Ω		28.8		dB
		Default full-scale voltage (FS_RANGE_A = 0xA000) setting, no input, Z_S = 100 Ω		28.6		
$NOISE_{DC}$	DC input noise standard deviation	No input, excludes DC offset, includes fixed interleaving spurs (F_S/2 and F_S/4 spurs)		2.0		LSB
SNR	Signal-to-noise ratio, large signal, excluding DC, HD2 to HD9 and interleaving spurs	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		56.7		dBFS
		f_{IN} = 97 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting		57.6		
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		56.7		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		56.5		
SNR	Signal-to-noise ratio, small signal, excluding DC, HD2 to HD9 and interleaving spurs	f_{IN} = 97 MHz, A_{IN} = –16 dBFS		57.5		dBFS
		f_{IN} = 347 MHz, A_{IN} = –16 dBFS		57.5		
		f_{IN} = 797 MHz, A_{IN} = –16 dBFS		57.4		
SINAD	Signal-to-noise and distortion ratio, large signal, excluding DC and F_S/2 fixed spurs	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		55.2		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		55.1		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		53.9		
ENOB	Effective number of bits, large signal, excluding DC and F_S/2 fixed spurs	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		8.9		bits
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		8.9		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		8.7		
SFDR	Spurious-free dynamic range, large signal, excluding DC, F_S/4 and F_S/2 fixed spurs	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		61		dBFS
	Spurious-free dynamic range, large signal, excluding DC, F_S/4 and F_S/2 fixed spurs	f_{IN} = 97 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting		63		
	Spurious-free dynamic range, large signal, excluding DC, F_S/4 and F_S/2 fixed spurs	f_{IN} = 347 MHz, A_{IN} = –1 dBFS		62		
	Spurious-free dynamic range, large signal, excluding DC, F_S/4 and F_S/2 fixed spurs	f_{IN} = 797 MHz, A_{IN} = –1 dBFS		59		
SFDR	Spurious-free dynamic range, small signal, excluding DC, F_S/4 and F_S/2 fixed spurs	f_{IN} = 97 MHz, A_{IN} = –16 dBFS		74		dBFS
		f_{IN} = 347 MHz, A_{IN} = –16 dBFS		76		
		f_{IN} = 797 MHz, A_{IN} = –16 dBFS		73		
F_S/2	F_S/2 fixed interleaving spur, independent of input signal	No input		-65		dBFS
F_S/4	F_S/4 fixed interleaving spur, independent of input signal	No input		-63		dBFS
HD2	2nd-order harmonic	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-71		dBFS
		f_{IN} = 97 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting		-73		
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-77		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		-67		

5.8 Electrical Characteristics: AC Specifications (Single-Channel Mode) (continued)

Typical values at T_A = +25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-$V_{PP-DIFF}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM), foreground calibration; minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in the Recommended Operating Conditions table.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD3	3rd-order harmonic	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-72		dBFS
		f_{IN} = 97 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting		-68		
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-70		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		-66		
$F_S/2-F_{IN}$	$F_S/2-F_{IN}$ interleaving spur, signal dependent	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-66		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-63		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		-61		
$F_S/4\pm F_{IN}$	$F_S/4\pm F_{IN}$ interleaving spurs, signal dependent	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-72		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-74		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		-70		
SPUR	Worst harmonic 4th-order or higher	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-72		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-73		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		-72		
IMD3	3rd-order intermodulation	f_{IN} = 97 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		-85		dBFS
		f_{IN} = 347 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		-79		
		f_{IN} = 797 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		-79		
ADC12DL1500						
FPBW	Full-power input bandwidth (–3 dB)[1]	Foreground calibration		7.5		GHz
CER	Code error rate	Maximum CER		10^{-18}		errors/sample
NSD	Noise spectral density, no input signal, excludes fixed interleaving spurs (F_S/2 and F_S/4 spurs)	Maximum full-scale voltage (FS_RANGE_A = 0xFFFF) setting		-150.3		dBFS/Hz
		Default full-scale voltage (FS_RANGE_A = 0xA000) setting		-149.4		
NF	Noise figure	Maximum full-scale voltage (FS_RANGE_A = 0xFFFF) setting, no input, Z_S = 100 Ω		24.7		dB
		Default full-scale voltage (FS_RANGE_A = 0xA000) setting, no input, Z_S = 100 Ω		23.6		
$NOISE_{DC}$	DC input noise standard deviation	No input, excludes DC offset, includes fixed interleaving spurs (F_S/2 and F_S/4 spurs)		2.0		LSB
SNR	Signal-to-noise ratio, large signal, excluding DC, HD2 to HD9 and interleaving spurs	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		56.6		dBFS
		f_{IN} = 97 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting		57.3		
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		56.7		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		56.5		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS		55.7		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting		56.2		
SNR	Signal-to-noise ratio, small signal, excluding DC, HD2 to HD9 and interleaving spurs	f_{IN} = 97 MHz, A_{IN} = –16 dBFS		57.2		dBFS
		f_{IN} = 347 MHz, A_{IN} = –16 dBFS		57.2		
		f_{IN} = 797 MHz, A_{IN} = –16 dBFS		57.2		
		f_{IN} = 2397 MHz, A_{IN} = –16 dBFS		57.1		

5.8 Electrical Characteristics: AC Specifications (Single-Channel Mode) (continued)

Typical values at T_A = +25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-$V_{PP-DIFF}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM), foreground calibration; minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in the Recommended Operating Conditions table.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise and distortion ratio, large signal, excluding DC and F_S/2 fixed spurs	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		55.8		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		55.8		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		55.4		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS		53.9		
ENOB	Effective number of bits, large signal, excluding DC and F_S/2 fixed spurs	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		9.0		bits
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		9.0		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		8.9		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS		8.7		
SFDR	Spurious-free dynamic range, large signal, excluding DC, F_S/4 and F_S/2 fixed spurs	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		67		dBFS
		f_{IN} = 97 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting		64		
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		63		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		63		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS		58		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting		54		
SFDR	Spurious-free dynamic range, small signal, excluding DC, F_S/4 and F_S/2 fixed spurs	f_{IN} = 97 MHz, A_{IN} = –16 dBFS		75		dBFS
		f_{IN} = 347 MHz, A_{IN} = –16 dBFS		72		
		f_{IN} = 797 MHz, A_{IN} = –16 dBFS		73		
		f_{IN} = 2397 MHz, A_{IN} = –16 dBFS		73		
F_S/2	F_S/2 fixed interleaving spur, independent of input signal	No input		-65		dBFS
F_S/4	F_S/4 fixed interleaving spur, independent of input signal	No input		-69		dBFS
HD2	2nd-order harmonic	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-71		dBFS
		f_{IN} = 97 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting		-71		
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-73		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		-66		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS		-61		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting		-61		
HD3	3rd-order harmonic	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-68		dBFS
		f_{IN} = 97 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting		-64		
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-72		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		-70		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS		-58		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting		-54		
F_S/2-F_{IN}	F_S/2-F_{IN} interleaving spur, signal dependent	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-71		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-65		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		-64		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS		-63		
F_S/4±F_{IN}	F_S/4±F_{IN} interleaving spurs, signal dependent	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-74		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-74		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		-70		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS		-74		

5.8 Electrical Characteristics: AC Specifications (Single-Channel Mode) (continued)

Typical values at T_A = +25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-$V_{PP-DIFF}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM), foreground calibration; minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in the Recommended Operating Conditions table.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPUR	Worst harmonic 4^{th}-order or higher	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-69		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-73		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		-72		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS		-73		
IMD3	3^{rd}-order intermodulation	f_{IN} = 97 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		-85		dBFS
		f_{IN} = 347 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		-84		
		f_{IN} = 797 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		-83		
		f_{IN} = 2397 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		-70		
ADC12DL2500						
FPBW	Full-power input bandwidth (–3 dB)[(1)]	Foreground calibration		7.5		GHz
CER	Code error rate	Maximum CER		10^{-18}		errors/sample
NSD	Noise spectral density, no input signal, excludes fixed interleaving spurs (F_S/2 and F_S/4 spurs)	Maximum full-scale voltage (FS_RANGE_A = 0xFFFF) setting		-152.2		dBFS/Hz
		Default full-scale voltage (FS_RANGE_A = 0xA000) setting		-151.3		
NF	Noise figure	Maximum full-scale voltage (FS_RANGE_A = 0xFFFF) setting, no input, Z_S = 100 Ω		22.8		dB
		Default full-scale voltage (FS_RANGE_A = 0xA000) setting, no input, Z_S = 100 Ω		21.7		
$NOISE_{DC}$	DC input noise standard deviation	No input, excludes DC offset, includes fixed interleaving spurs (F_S/2 and F_S/4 spurs)		2.0		LSB
SNR	Signal-to-noise ratio, large signal, excluding DC, HD2 to HD9 and interleaving spurs	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		56.1		dBFS
		f_{IN} = 97 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting		57.1		
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		56.2		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		56.1		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS		55.2		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting		55.6		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS		52.2		
SNR	Signal-to-noise ratio, small signal, excluding DC, HD2 to HD9 and interleaving spurs	f_{IN} = 97 MHz, A_{IN} = –16 dBFS		56.7		dBFS
		f_{IN} = 347 MHz, A_{IN} = –16 dBFS		56.8		
		f_{IN} = 797 MHz, A_{IN} = –16 dBFS		56.8		
		f_{IN} = 2397 MHz, A_{IN} = –16 dBFS		56.6		
		f_{IN} = 4997 MHz, A_{IN} = –16 dBFS		56.3		
SINAD	Signal-to-noise and distortion ratio, large signal, excluding DC and F_S/2 fixed spurs	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		55.4		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		55.5		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		53.9		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS		52.9		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS		48.29		

5.8 Electrical Characteristics: AC Specifications (Single-Channel Mode) (continued)

Typical values at T_A = +25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-$V_{PP-DIFF}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM), foreground calibration; minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in the Recommended Operating Conditions table.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENOB	Effective number of bits, large signal, excluding DC and F_S/2 fixed spurs	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		8.9		bits
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		8.9		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		8.7		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS		8.5		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS		7.7		
SFDR	Spurious-free dynamic range, large signal, excluding DC, F_S/4 and F_S/2 fixed spurs	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		65		dBFS
		f_{IN} = 97 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting		63		
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		65		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		60		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS		55		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting		54		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS		48		
SFDR	Spurious-free dynamic range, small signal, excluding DC, F_S/4 and F_S/2 fixed spurs	f_{IN} = 97 MHz, A_{IN} = –16 dBFS		71		dBFS
		f_{IN} = 347 MHz, A_{IN} = –16 dBFS		74		
		f_{IN} = 797 MHz, A_{IN} = –16 dBFS		72		
		f_{IN} = 2397 MHz, A_{IN} = –16 dBFS		68		
		f_{IN} = 4997 MHz, A_{IN} = –16 dBFS		64		
F_S/2	F_S/2 fixed interleaving spur, independent of input signal	No input		-60		dBFS
F_S/4	F_S/4 fixed interleaving spur, independent of input signal	No input		-64		dBFS
HD2	2nd-order harmonic	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-74		dBFS
		f_{IN} = 97 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting		-74		
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-71		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		-68		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS		-60		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting		-60		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS		-61		
HD3	3rd-order harmonic	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-67		dBFS
		f_{IN} = 97 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting		-63		
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-69		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		-68		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS		-64		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting		-57		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS		-54		
$F_S/2-F_{IN}$	$F_S/2-F_{IN}$ interleaving spur, signal dependent	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-69		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-66		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		-62		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS		-58		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS		-54		

5.8 Electrical Characteristics: AC Specifications (Single-Channel Mode) (continued)

Typical values at T_A = +25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-$V_{PP-DIFF}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM), foreground calibration; minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in the Recommended Operating Conditions table.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$F_S/4 \pm F_{IN}$	$F_S/4 \pm F_{IN}$ interleaving spurs, signal dependent	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-74		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-69		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		-69		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS		-65		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS		-63		
SPUR	Worst harmonic 4^{th}-order or higher	f_{IN} = 97 MHz, A_{IN} = –1 dBFS		-71		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS		-72		
		f_{IN} = 797 MHz, A_{IN} = –1 dBFS		-72		
		f_{IN} = 2397 MHz, A_{IN} = –1 dBFS		-71		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS		-66		
IMD3	3^{rd}-order intermodulation	f_{IN} = 97 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		-79		dBFS
		f_{IN} = 347 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		-82		
		f_{IN} = 797 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		-84		
		f_{IN} = 2397 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		-68		
		f_{IN} = 4997 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		-57		

(1) Full-power input bandwidth (FPBW) is defined as the input frequency where the reconstructed output of the ADC has dropped 3 dB below the power of a full-scale input signal at a low input frequency. Useable bandwidth may exceed the –3-dB full-power input bandwidth.

5.9 Timing Requirements

			MIN	NOM	MAX	UNIT
DEVICE (SAMPLING) CLOCK (CLK+, CLK–)						
f_{CLK}	Input clock frequency (CLK+, CLK–), both single-channel and dual-channel modes(1)		500(3)		2500	MHz
t_{CLK}	Input clock period (CLK+, CLK–), both single-channel and dual-channel modes(1)		400		2000(4)	ps
SYSREF (SYSREF+, SYSREF–)						
$t_{INV(SYSREF)}$	Width of invalid SYSREF capture region of CLK± period, indicating setup or hold time violation, as measured by SYSREF_POS status register(2)			49		ps
$t_{INV(TEMP)}$	Drift of invalid SYSREF capture region over temperature, positive number indicates a shift toward MSB of SYSREF_POS register			0		ps/°C
$t_{INV(VA11)}$	Drift of invalid SYSREF capture region over VA11 supply voltage, positive number indicates a shift toward MSB of SYSREF_POS register			0.36		ps/mV
$t_{STEP(SP)}$	Delay of SYSREF_POS LSB	SYSREF_ZOOM = 0		77		ps
		SYSREF_ZOOM = 1		24		
$t_{(PH\_SYS)}$	Minimum SYSREF± assertion duration after SYSREF± rising edge event			4		ns
$t_{(PL\_SYS)}$	Minimum SYSREF± deassertion duration after SYSREF± falling edge event			4		ns
SERIAL PROGRAMMING INTERFACE (SCLK, SDI, $\overline{SCS}$)						
$f_{CLK(SCLK)}$	Serial clock frequency		0		15.625	MHz
$t_{(PH)}$	Serial clock high value pulse width		32			ns
$t_{(PL)}$	Serial clock low value pulse width		32			ns
$t_{SU(\overline{SCS})}$	Setup time from $\overline{SCS}$ to rising edge of SCLK		25			ns
$t_{H(\overline{SCS})}$	Hold time from rising edge of SCLK to $\overline{SCS}$		3			ns
$t_{SU(SDI)}$	Setup time from SDI to rising edge of SCLK		25			ns
$t_{H(SDI)}$	Hold time from rising edge of SCLK to SDI		3			ns

(1) Unless functionally limited to a smaller range than described in the LVDS Output Modes table based on programmed LVDS output mode.
(2) Use SYSREF_POS to select an optimal SYSREF_SEL value for SYSREF capture, see the SYSREF Position Detector and Sampling Position Selection (SYSREF Windowing) section for more information on SYSREF windowing. The invalid region, specified by $t_{INV(SYSREF)}$, indicates the portion of the CLK± period (t_{CLK}), as measured by SYSREF_SEL, that may result in a setup and hold violation. Verify that the timing skew between SYSREF± and CLK± over system operating conditions from the nominal conditions (that were used to find optimal SYSREF_SEL) does not result in the invalid region occurring at the selected SYSREF_SEL position in SYSREF_POS, otherwise a temperature dependent SYSREF_SEL selection may be needed to track the skew between CLK± and SYSREF±.
(3) Minimum sampling clock down to 0°C. 800MHz below 0°C to -40°C.
(4) Minimum period down to 0°C. 1250ps below 0°C to -40°C.

5.10 Switching Characteristics

typical values at T_A = +25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-$V_{PP-DIFF}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM), foreground calibration; minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in the Recommended Operating Conditions table

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE (SAMPLING) CLOCK (CLK+, CLK–)						
t_{AD}	Sampling (aperture) delay from CLK± rising edge (dual channel mode) or rising and falling edge (single channel mode) to sampling instant(4)	TAD_COARSE = 0x00, TAD_FINE = 0x00 and TAD_INV = 0		360		ps
$t_{AD(MAX)}$	Maximum t_{AD} Adjust programmable delay, not including clock inversion (TAD_INV = 0)	Coarse adjustment (TAD_COARSE = 0xFF)		289		ps
		Fine adjustment (TAD_FINE = 0xFF)		4.9		
$t_{AD(STEP)}$	Aperture delay step size	Coarse adjustment (TAD_COARSE)		1.13		ps
		Fine adjustment (TAD_FINE)		19		fs

5.10 Switching Characteristics (continued)

typical values at T_A = +25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-$V_{PP-DIFF}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM), foreground calibration; minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in the Recommended Operating Conditions table

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{AJ}	Aperture jitter, rms	Minimum t_{AD} Adjust coarse setting (TAD_COARSE = 0x00, TAD_INV = 0), dither disabled (ADC_DITH_EN = 0)		55		fs
		Minimum t_{AD} Adjust coarse setting (TAD_COARSE = 0xFF, TAD_INV = 0), dither enabled (ADC_DITH_EN = 1)		70		
		Maximum t_{AD} Adjust coarse setting (TAD_COARSE = 0xFF) excluding TAD_INV (TAD_INV = 0), dither disabled (ADC_DITH_EN = 0)		70[1]		
		Maximum t_{AD} Adjust coarse setting (TAD_COARSE = 0xFF) excluding TAD_INV (TAD_INV = 0), dither enabled (ADC_DITH_EN = 1)		80[1]		
LVDS OUTPUTS (DACLK±, DASTR±, DA[11:0]±, DBCLK±, DBSTR±, DB[11:0]±, DCCLK±, DCSTR±, DC[11:0]±, DDCLK±, DDSTR±, DD[11:0]±)						
f_{BIT}	Output bit rate per output data pair				1.6	Gbps
f_{DCLK}	DDR data clock frequency				800	MHz
t_{DJ}	DDR data clock total jitter, peak-to-peak, with random jitter portion defined with respect to a BER=1e–15 (Q=7.94)	UPAT_CTRL = 0x10		36		ps
$t_{SKEW(SAME)}$	Maximum timing skew between any two LVDS output pairs (DxCLK±, Dx[11:0]±, DxSTR±) within the same LVDS bank over operating conditions			75		ps
$t_{SKEW(ALL)}$	Maximum timing skew between any two LVDS output pairs (DxCLK±, Dx[11:0]±, DxSTR±) in all LVDS banks over operating conditions with t_{OSAB}, t_{OSAC} and t_{OSBD} skew excluded			125		ps
t_{OSAB}	Functional timing offset between DACLK± rising edge and DBCLK± rising edge, positive number indicates that DACLK± leads DBCLK±	DES_EN = 0, LDEMUX = 0, LALIGNED = 0		0		t_{CLK}
		DES_EN = 0, LDEMUX = 0, LALIGNED = 1		0		
		DES_EN = 0, LDEMUX = 1, LALIGNED = 0		0		
		DES_EN = 0, LDEMUX = 1, LALIGNED = 1		0		
		DES_EN = 1, LDEMUX = 0, LALIGNED = 0		0.5		
		DES_EN = 1, LDEMUX = 0, LALIGNED = 1		0		
		DES_EN = 1, LDEMUX = 1, LALIGNED = 0		0.5		
		DES_EN = 1, LDEMUX = 1, LALIGNED = 1		0		
t_{OSAC}	Functional timing offset between DACLK± rising edge and DCCLK± rising edge, positive number indicates that DACLK± leads DCCLK±	DES_EN = 0, LDEMUX = 1, LALIGNED = 0		1		t_{CLK}
		DES_EN = 0, LDEMUX = 1, LALIGNED = 1		0		
		DES_EN = 1, LDEMUX = 1, LALIGNED = 0		1		
		DES_EN = 1, LDEMUX = 1, LALIGNED = 1		0		
t_{OSBD}	Functional timing offset between DBCLK± rising edge and DDCLK± rising edge, positive number indicates that DBCLK± leads DDCLK±	DES_EN = 0, LDEMUX = 1, LALIGNED = 0		1		t_{CLK}
		DES_EN = 0, LDEMUX = 1, LALIGNED = 1		0		
		DES_EN = 1, LDEMUX = 1, LALIGNED = 0		1		
		DES_EN = 1, LDEMUX = 1, LALIGNED = 1		0		
t_{TLH}	Low-to-high transition time (differential)	20% to 80%, 1.6 Gbps, V_{LVDS} = 1.9 V, UPAT_CTRL = 0x10		125		ps
		20% to 80%, 1.6 Gbps, V_{LVDS} = 1.1 V, UPAT_CTRL = 0x10		200		
t_{THL}	High-to-low transition time (differential)	80% to 20%, 1.6 Gbps, V_{LVDS} = 1.9 V, UPAT_CTRL = 0x10		125		ps
		80% to 20%, 1.6 Gbps, V_{LVDS} = 1.1 V, UPAT_CTRL = 0x10		200		

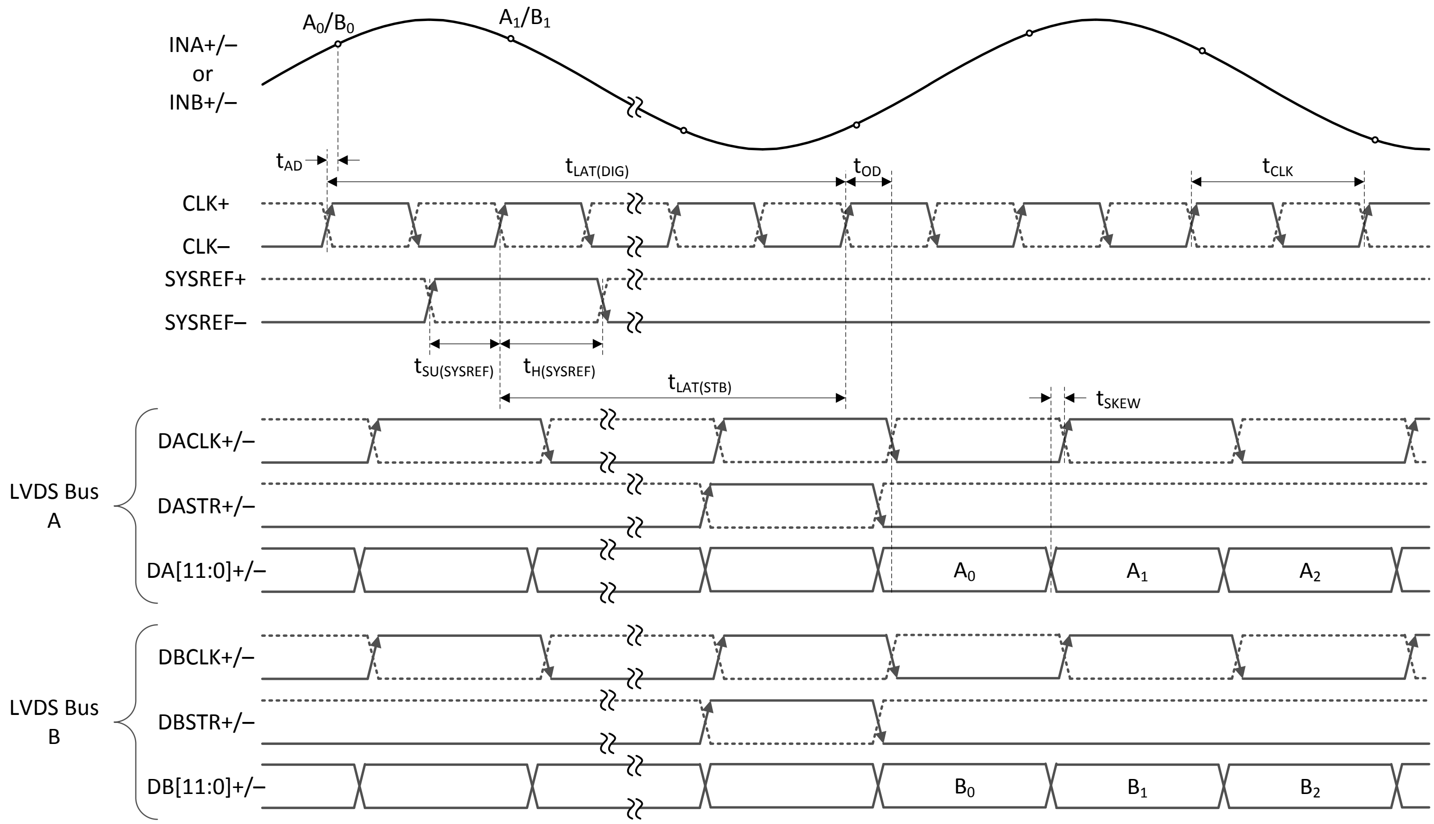
5.10 Switching Characteristics (continued)

typical values at T_A = +25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-$V_{PP-DIFF}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM), foreground calibration; minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in the Recommended Operating Conditions table

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LATENCY						
t_{OD}	Output delay from CLK± rising edge (dual-channel mode) or falling edge (single-channel mode) to DACLK± output[4]	TAD_COARSE = 0x00, TAD_FINE = 0x00 and TAD_INV = 0		1.5		ns
$t_{LAT(DIG)}$	CLK± edge that samples input signal to CLK± edge that launches data, digital latency only[2] [4]	DES_EN = 0, LDEMUX = 0, LALIGNED = 0		26		t_{CLK}
		DES_EN = 0, LDEMUX = 0, LALIGNED = 1		26		
		DES_EN = 0, LDEMUX = 1, LALIGNED = 0		26		
		DES_EN = 0, LDEMUX = 1, LALIGNED = 1		27		
		DES_EN = 1, LDEMUX = 0, LALIGNED = 0		26		
		DES_EN = 1, LDEMUX = 0, LALIGNED = 1		26.5		
		DES_EN = 1, LDEMUX = 1, LALIGNED = 0		26		
		DES_EN = 1, LDEMUX = 1, LALIGNED = 1		27.5		
$t_{LAT(STB)}$	Latency from SYSREF± being sampled by rising edge of CLK± to the start of the corresponding data frame[3]	DES_EN = 0, LDEMUX = 0, LALIGNED = 0		47		t_{CLK}
		DES_EN = 0, LDEMUX = 0, LALIGNED = 1		47		
		DES_EN = 0, LDEMUX = 1, LALIGNED = 0		47		
		DES_EN = 0, LDEMUX = 1, LALIGNED = 1		48		
		DES_EN = 1, LDEMUX = 0, LALIGNED = 0		46.5		
		DES_EN = 1, LDEMUX = 0, LALIGNED = 1		47		
		DES_EN = 1, LDEMUX = 1, LALIGNED = 0		46.5		
		DES_EN = 1, LDEMUX = 1, LALIGNED = 1		48		
$t_{LAT(\overline{SYNCSE})}$	Latency from $\overline{SYNCSE}$ assertion or deassertion to DB0± (LSB) changing from normal data to strobe output or strobe output to normal data, digital latency only	LDEMUX = 0	26		36+1*LFRAME	t_{CLK}
		LDEMUX = 1	26		36+2*LFRAME	
SERIAL PROGRAMMING INTERFACE (SDO)						
$t_{(OZD)}$	Delay from falling edge of 16th SCLK cycle during read operation for SDO transition from tri-state to valid data		1			ns
$t_{(ODZ)}$	Delay from $\overline{SCS}$ rising edge for SDO to transition from valid data to tri-state				10	ns
$t_{(OD)}$	Delay from falling edge of SCLK during read operation to SDO valid		1		10	ns

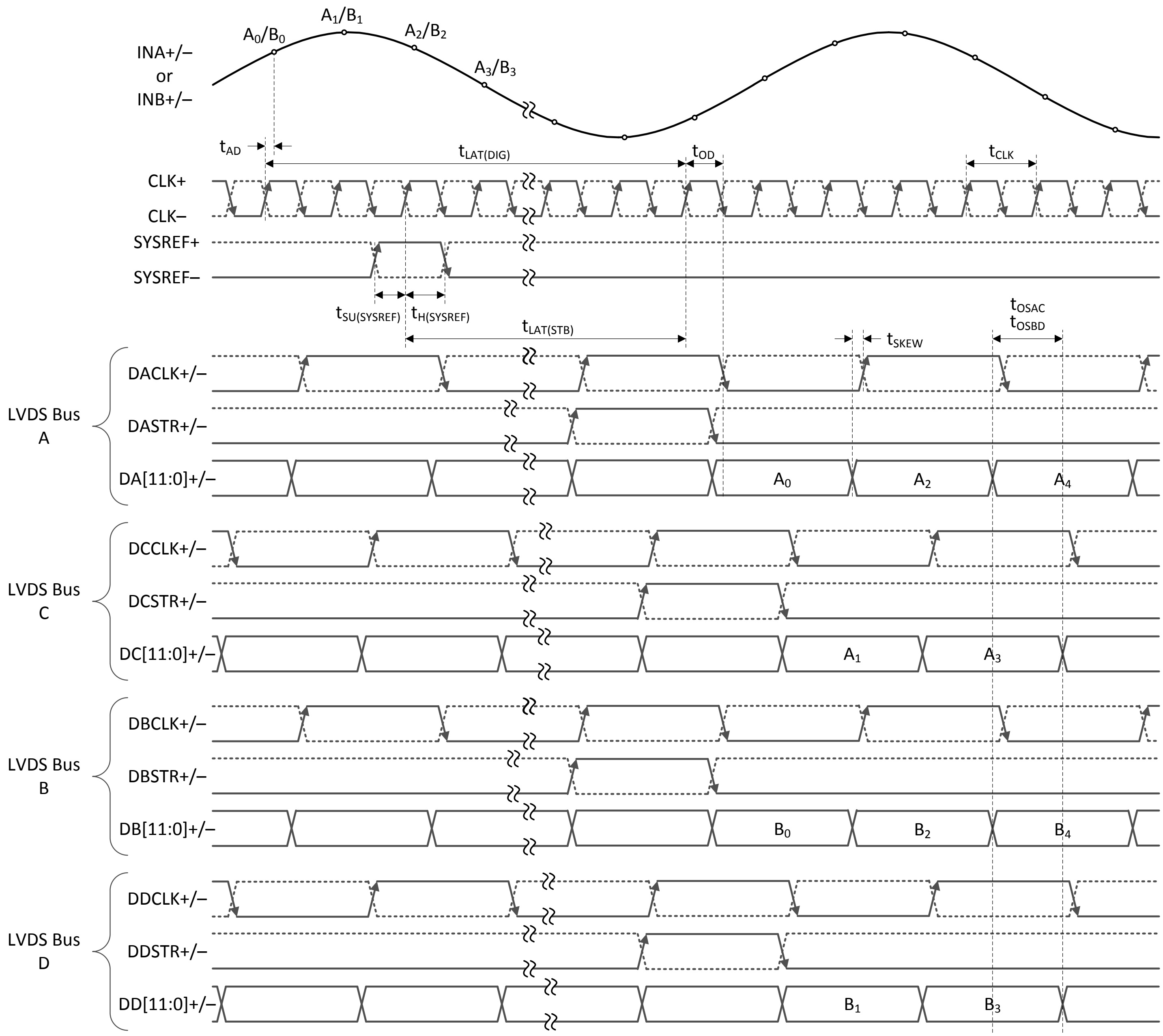
(1) t_{AJ} increases because of additional attenuation on internal clock path.
(2) When LDEMUX = 1 the output buses are aligned in time requiring the earlier sample(s) to be delayed before outputting on the LVDS buses to align with the later samples. The latency for the buses will be slightly different due to added delays. The number shown is for the worst case bus.
(3) When LDEMUX = 0 the output buses are staggered in time and therefore the start of data frames occur at staggered times. The number shown is for the earliest output frame. The strobe signals are output at the end of a frame so the start of a data frame corresponds to the data output immediately after a strobe output.
(4) Both t_{AD} and t_{OD} increase by the delay introduced by TAD_COARSE, TAD_FINE and TAD_INV when t_{AD} Adjust is used to delay the sampling instant. The total latency through the device does not include the aperture delay. Total latency through device is t_{LAT} = $t_{LAT(DIG)}$ + t_{OD} - t_{AD}.

5.11 Timing Diagrams



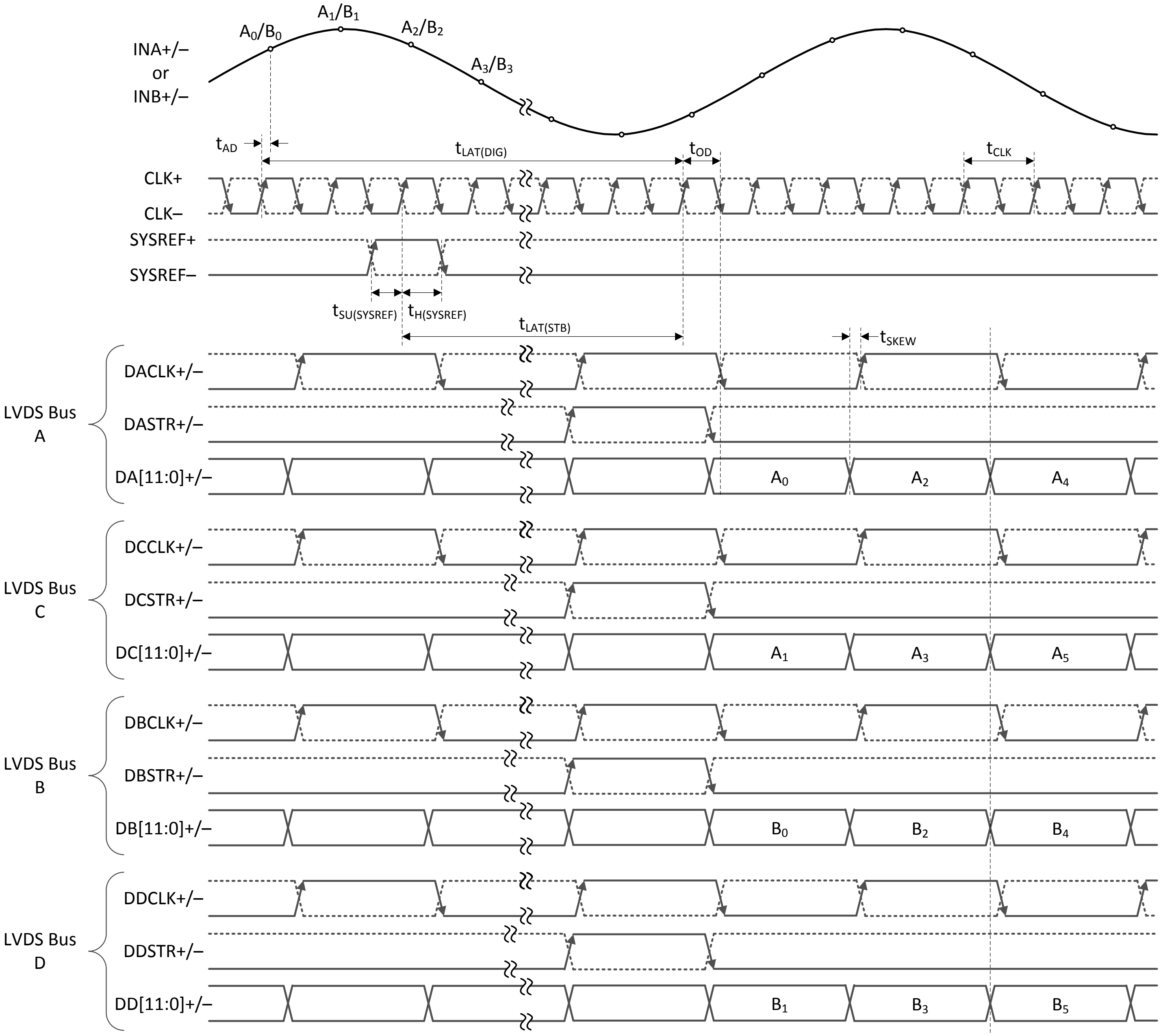
$t_{SU(SYSREF)}$ and $t_{H(SYSREF)}$ are only shown for completeness. Use automatic SYSREF calibration or SYSREF windowing to meet SYSREF timing.

Figure 5-1. Dual-Channel, 2-Bus Mode Timing (LDEMUX = 0, DES_EN = 0, LALIGNED = 0 or 1)



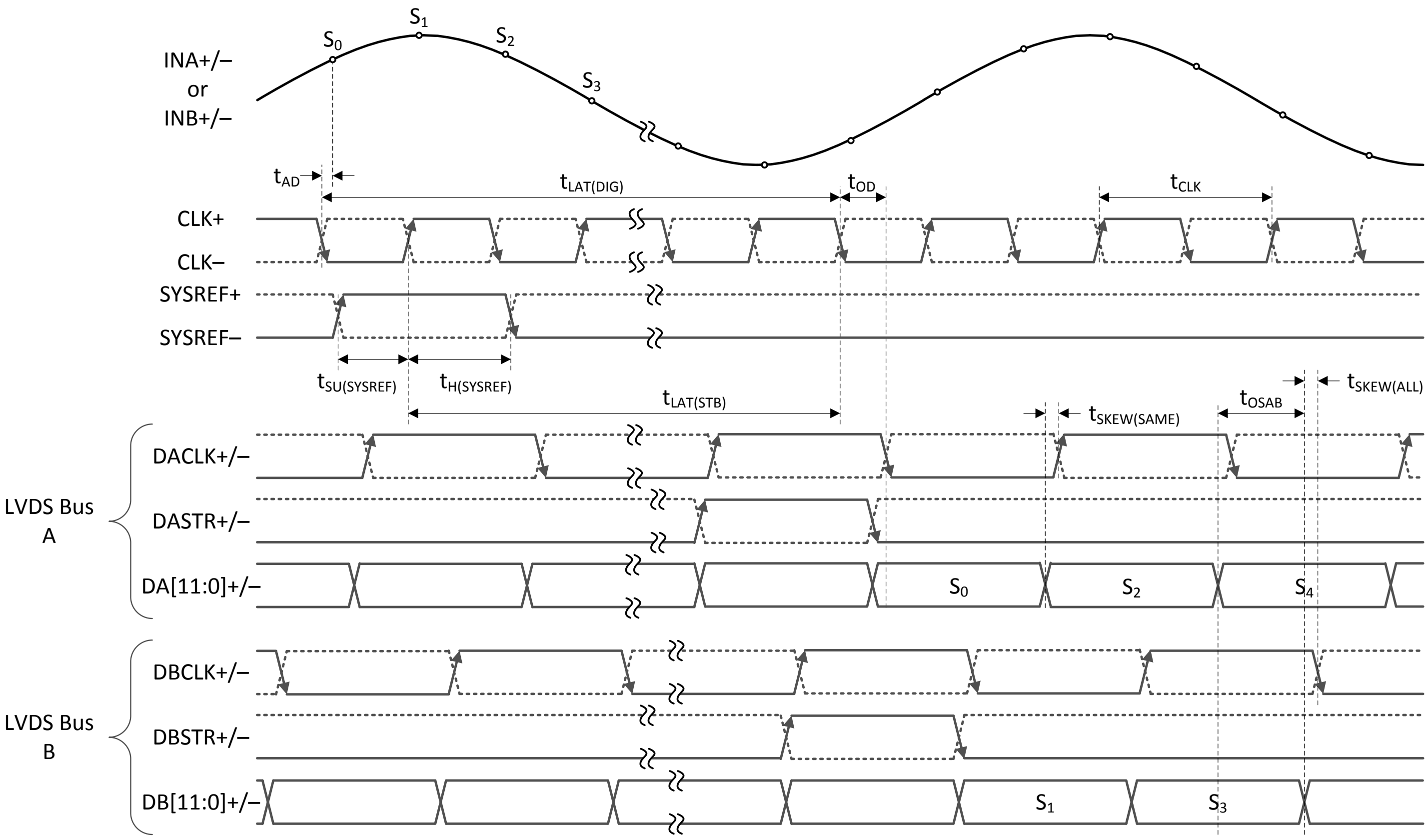
$t_{SU(SYSREF)}$ and $t_{H(SYSREF)}$ are only shown for completeness. Use automatic SYSREF calibration or SYSREF windowing to meet SYSREF timing.

Figure 5-2. Dual-Channel, 4-Bus, Staggered-Mode Timing (LDEMUX = 1, DES_EN = 0, LALIGNED = 0)



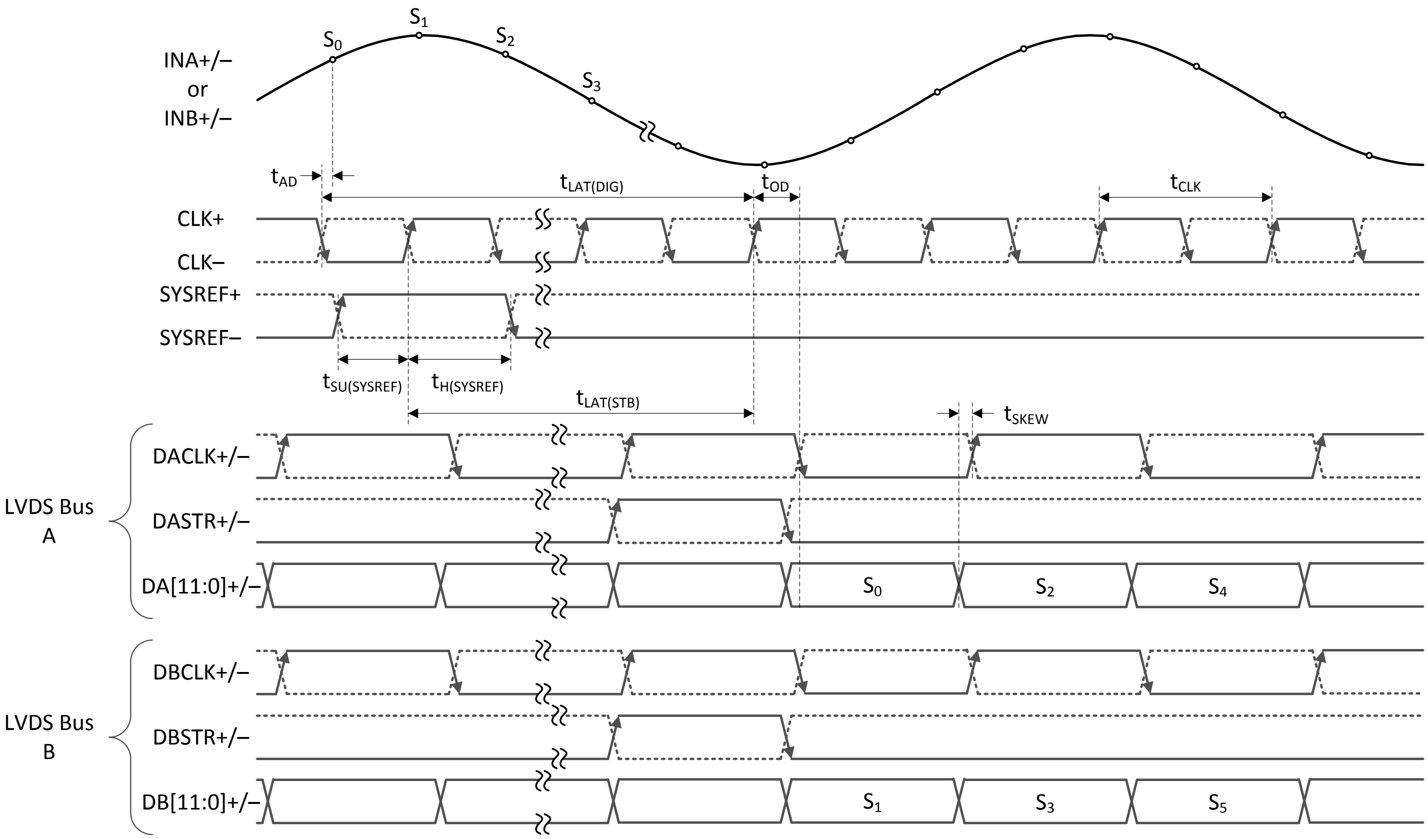
$t_{SU(SYSREF)}$ and $t_{H(SYSREF)}$ are only shown for completeness. Use automatic SYSREF calibration or SYSREF windowing to meet SYSREF timing.

Figure 5-3. Dual-Channel, 4-Bus, Aligned-Mode Timing (LDEMUX = 1, DES_EN = 0, LALIGNED = 1)



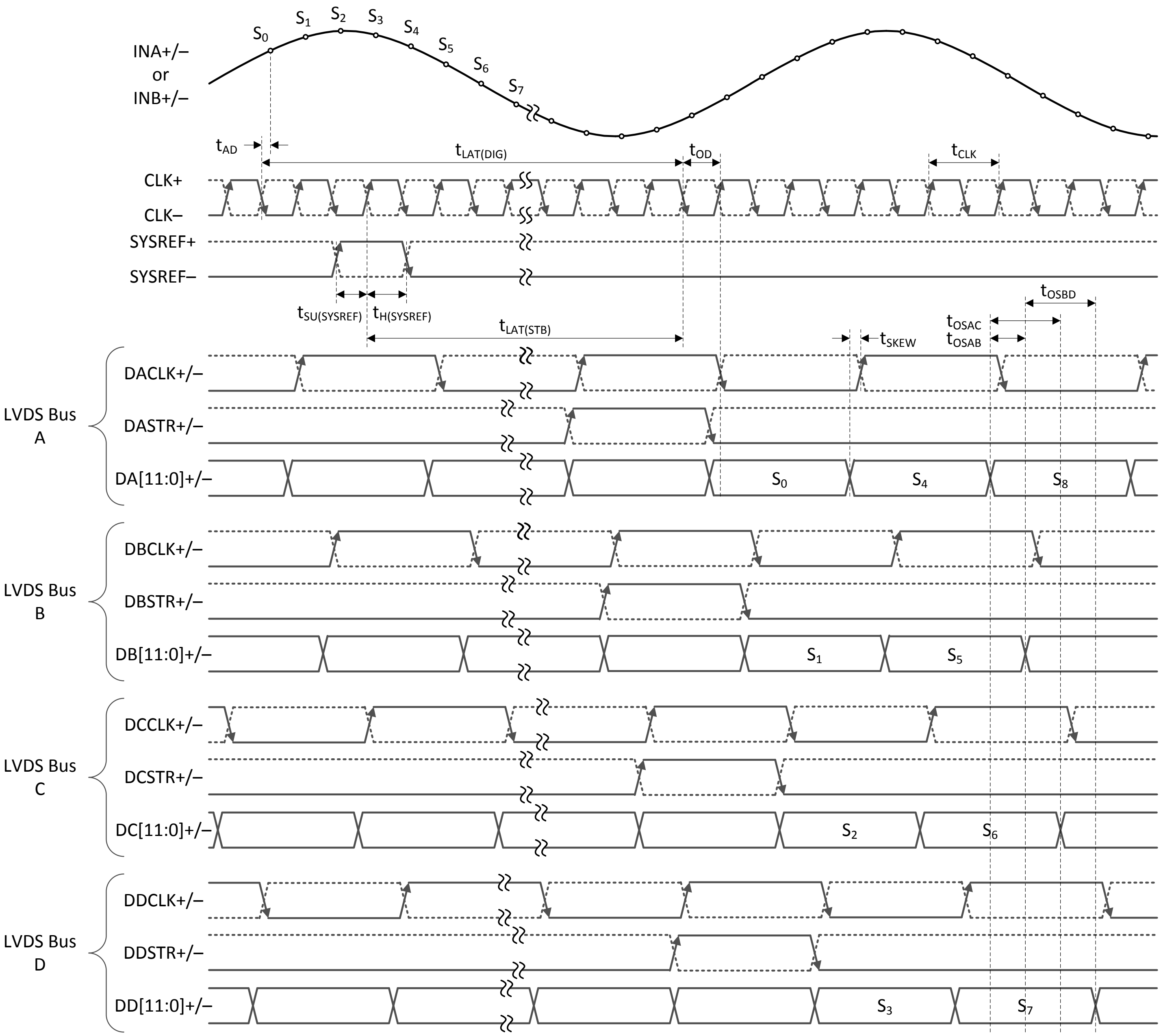
$t_{SU(SYSREF)}$ and $t_{H(SYSREF)}$ are only shown for completeness. Use automatic SYSREF calibration or SYSREF windowing to meet SYSREF timing.

Figure 5-4. Single-Channel, 2-Bus, Staggered-Mode Timing (LDEMUX = 0, DES_EN = 1, LALIGNED = 0)



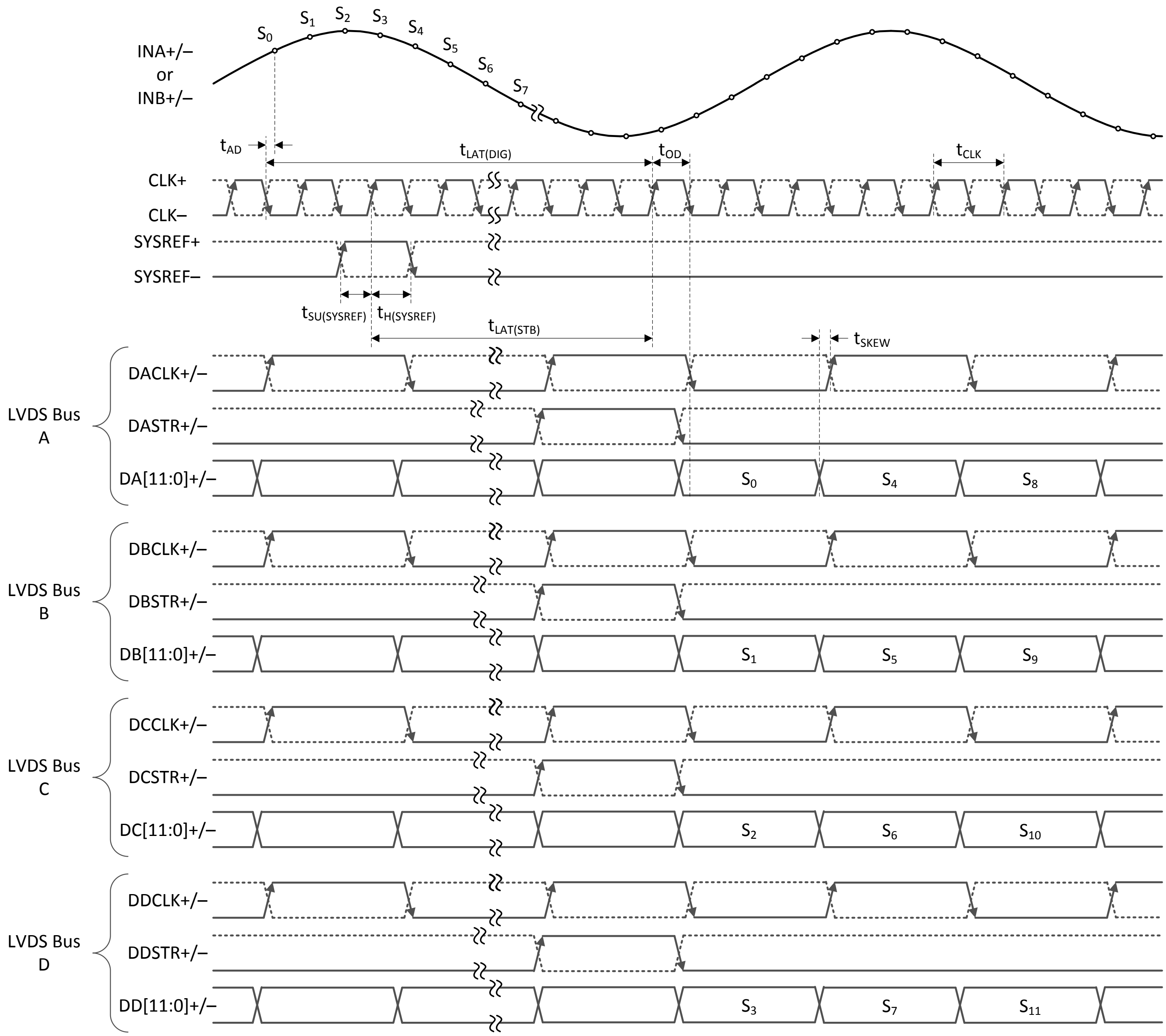
$t_{SU(SYSREF)}$ and $t_{H(SYSREF)}$ are only shown for completeness. Use automatic SYSREF calibration or SYSREF windowing to meet SYSREF timing.

Figure 5-5. Single-Channel, 2-Bus, Aligned-Mode Timing (LDEMUX = 0, DES_EN = 1, LALIGNED = 1)



$t_{SU(SYSREF)}$ and $t_{H(SYSREF)}$ are only shown for completeness. Use automatic SYSREF calibration or SYSREF windowing to meet SYSREF timing.

Figure 5-6. Single-Channel, 4-Bus, Staggered-Mode Timing (LDEMUX = 1, DES_EN = 1, LALIGNED = 0)



$t_{SU(SYSREF)}$ and $t_{H(SYSREF)}$ are only shown for completeness. Use automatic SYSREF calibration or SYSREF windowing to meet SYSREF timing.

Figure 5-7. Single-Channel, 4-Bus, Aligned-Mode Timing (LDEMUX = 1, DES_EN = 1, LALIGNED = 1)

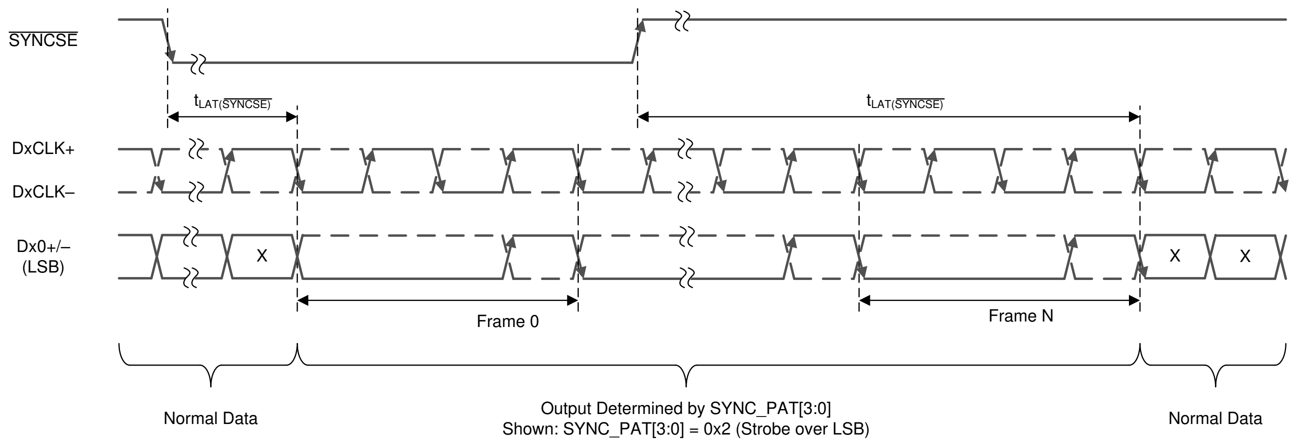


Figure 5-8. $\overline{\text{SYNCSE}}$ Timing Diagram

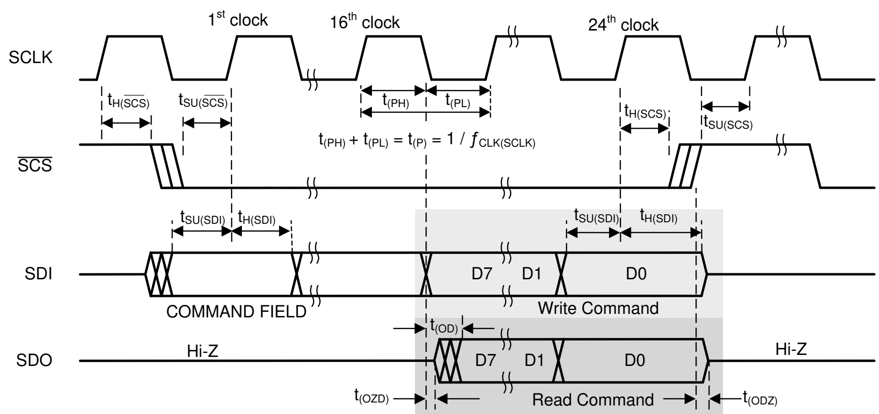
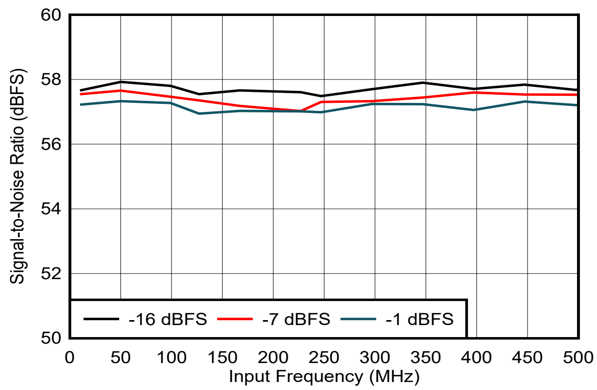


Figure 5-9. Serial Interface Timing

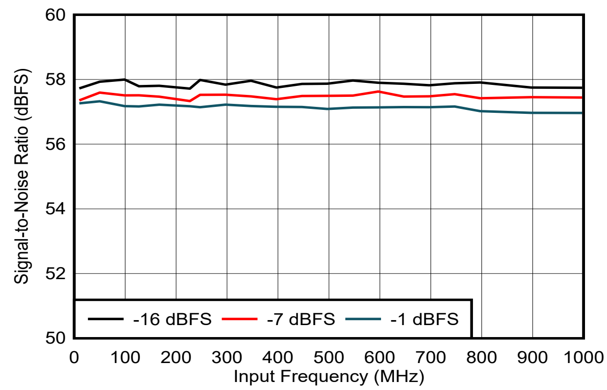
5.12 Typical Characteristics - ADC12DL500

typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 97MHz, A_{IN} = –1dBFS, f_{CLK} = 500MHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



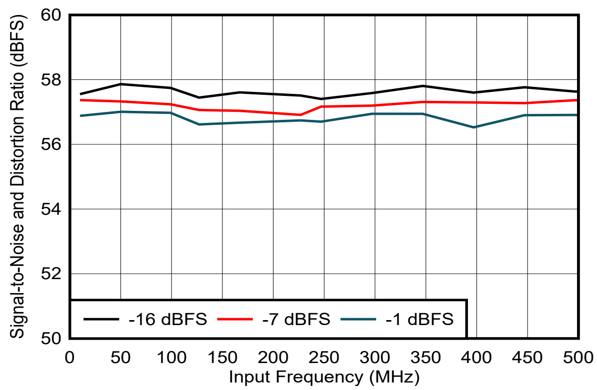
DES_EN = 0, f_S = 500MHz, FG calibration

Figure 5-10. SNR vs Input Frequency



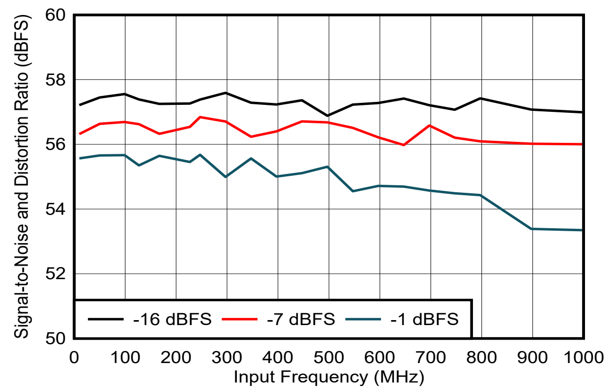
DES_EN = 1, f_S = 1000MHz, FG calibration

Figure 5-11. SNR vs Input Frequency



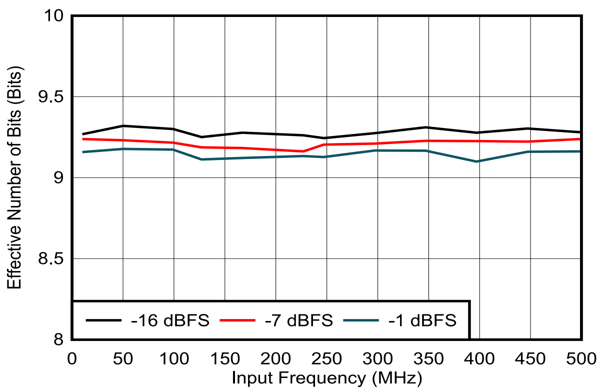
DES_EN = 0, f_S = 500MHz, FG calibration

Figure 5-12. SINAD vs Input Frequency



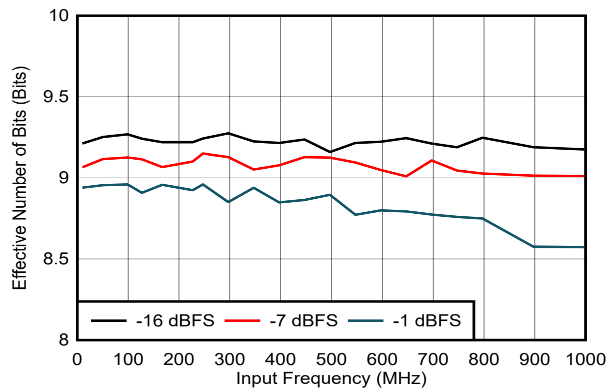
DES_EN = 1, f_S = 1000MHz, FG calibration

Figure 5-13. SINAD vs Input Frequency



DES_EN = 0, f_S = 500MHz, FG calibration

Figure 5-14. ENOB vs Input Frequency

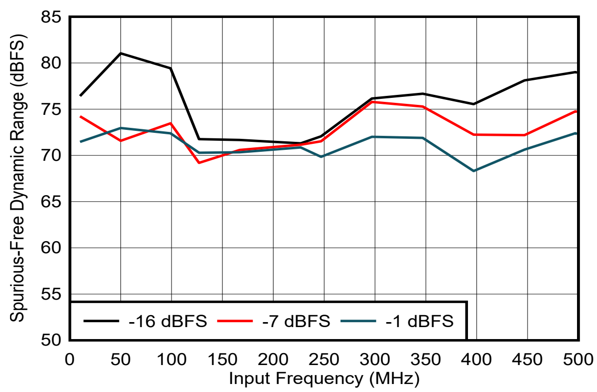


DES_EN = 1, f_S = 1000MHz, FG calibration

Figure 5-15. ENOB vs Input Frequency

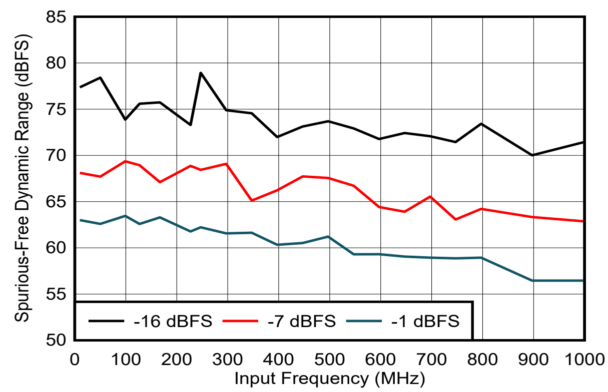
5.12 Typical Characteristics - ADC12DL500 (continued)

typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 97MHz, A_{IN} = –1dBFS, f_{CLK} = 500MHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



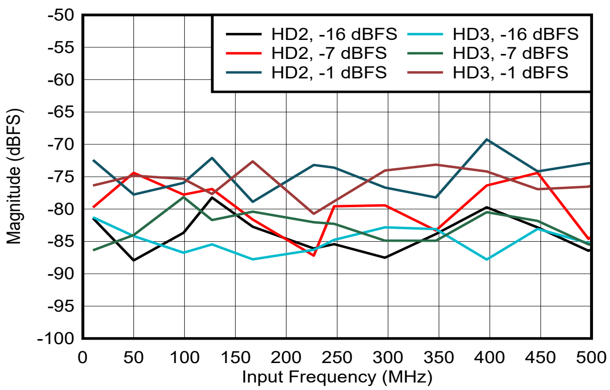
DES_EN = 0, f_S = 500MHz, FG calibration

Figure 5-16. SFDR vs Input Frequency



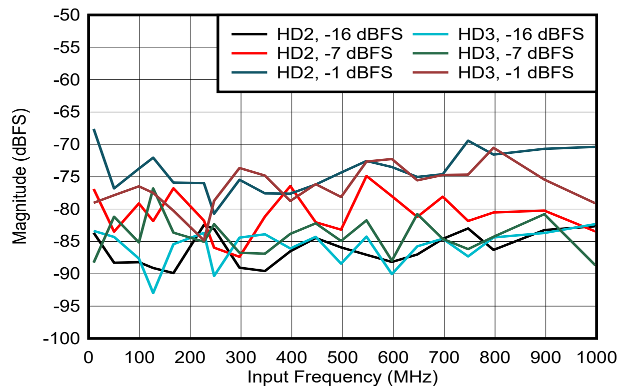
DES_EN = 1, f_S = 1000MHz, FG calibration

Figure 5-17. SFDR vs Input Frequency



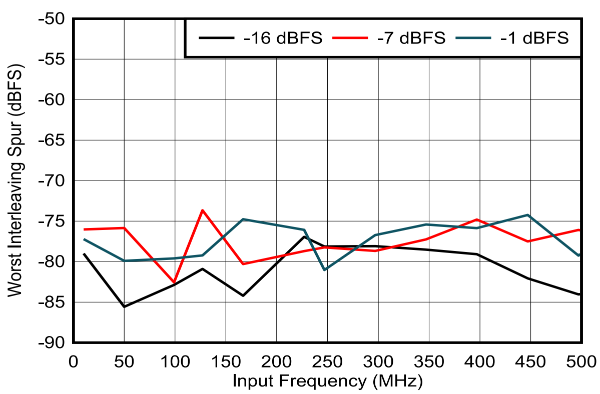
DES_EN = 0, f_S = 500MHz, FG calibration

Figure 5-18. HD2 and HD3 vs Input Frequency



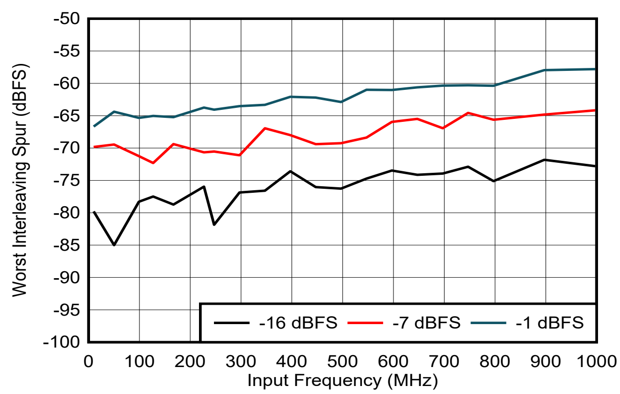
DES_EN = 1, f_S = 1000MHz, FG calibration

Figure 5-19. HD2 and HD3 vs Input Frequency



DES_EN = 0, f_S = 500MHz, FG calibration, includes f_S / 2 – f_{IN} spur only

Figure 5-20. Worst Interleaving Spur vs Input Frequency

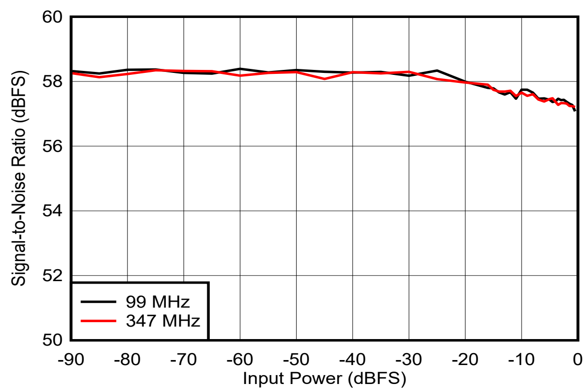


DES_EN = 1, f_S = 1000MHz, FG calibration, includes f_S / 2 – f_{IN} and f_S /4 ± f_{IN} spurs only

Figure 5-21. Worst Interleaving Spur vs Input Frequency

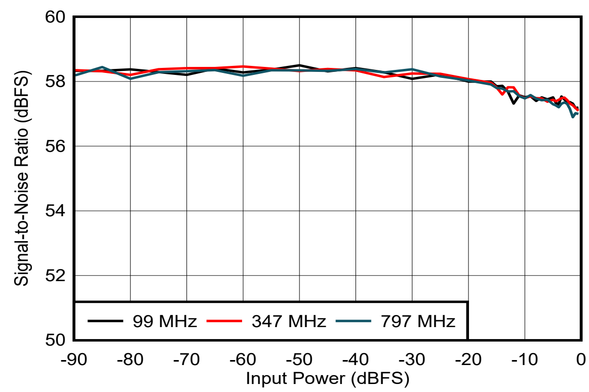
5.12 Typical Characteristics - ADC12DL500 (continued)

typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 97MHz, A_{IN} = –1dBFS, f_{CLK} = 500MHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



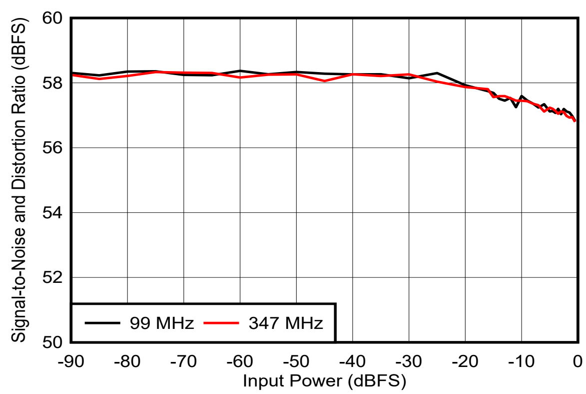
DES_EN = 0, f_S = 500MHz, FG calibration

Figure 5-22. SNR vs Input Power



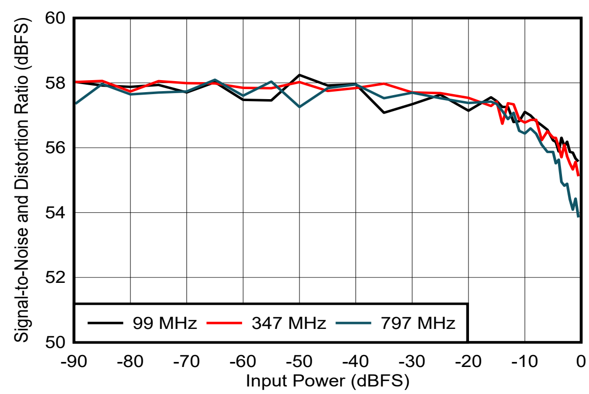
DES_EN = 1, f_S = 1000MHz, FG calibration

Figure 5-23. SNR vs Input Power



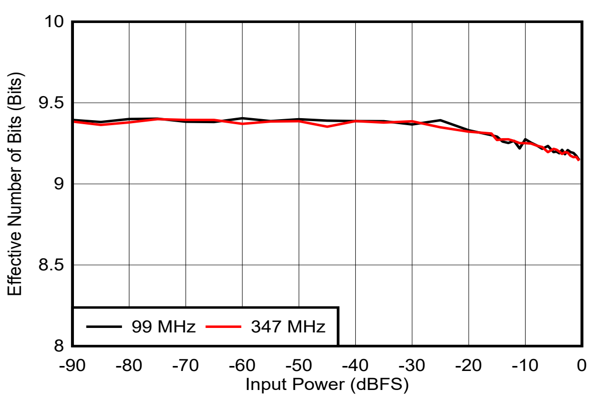
DES_EN = 0, f_S = 500MHz, FG calibration

Figure 5-24. SINAD vs Input Power



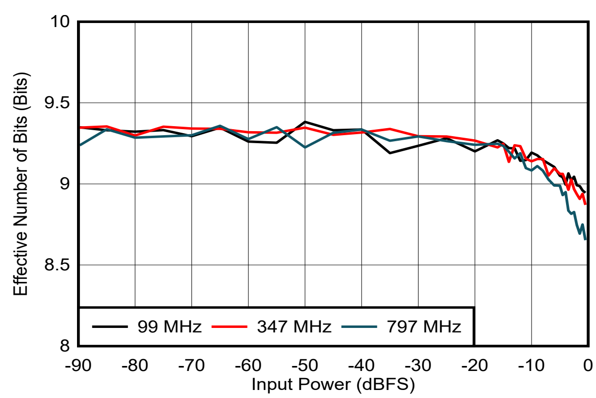
DES_EN = 1, f_S = 1000MHz, FG calibration

Figure 5-25. SINAD vs Input Power



DES_EN = 0, f_S = 500MHz, FG calibration

Figure 5-26. ENOB vs Input Power

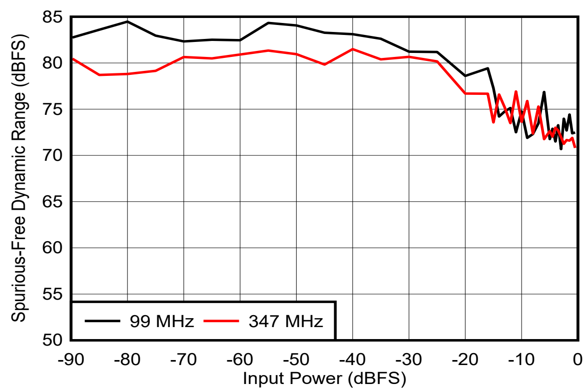


DES_EN = 1, f_S = 1000MHz, FG calibration

Figure 5-27. ENOB vs Input Power

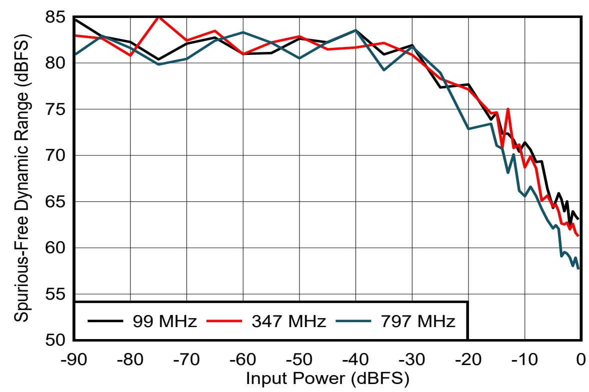
5.12 Typical Characteristics - ADC12DL500 (continued)

typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 97MHz, A_{IN} = –1dBFS, f_{CLK} = 500MHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



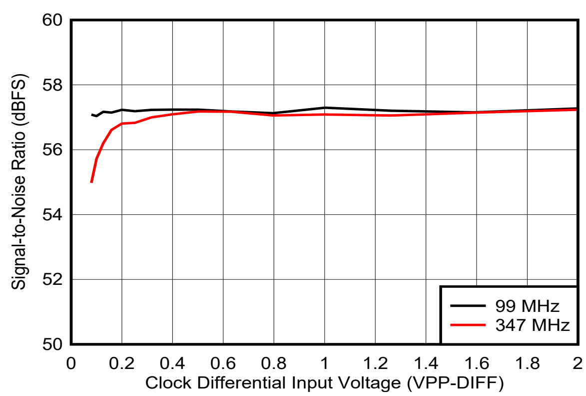
DES_EN = 0, f_S = 500MHz, FG calibration

Figure 5-28. SFDR vs Input Power



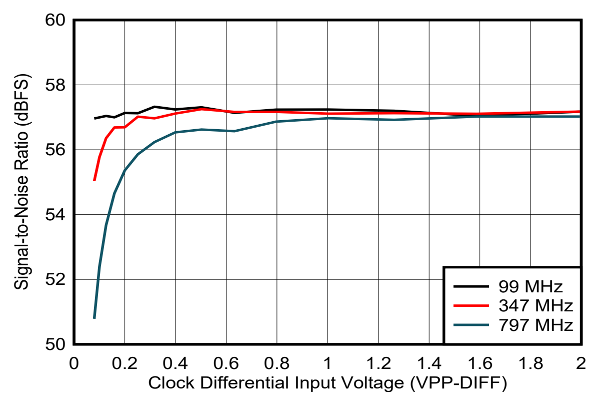
DES_EN = 1, f_S = 1000MHz, FG calibration

Figure 5-29. SFDR vs Input Power



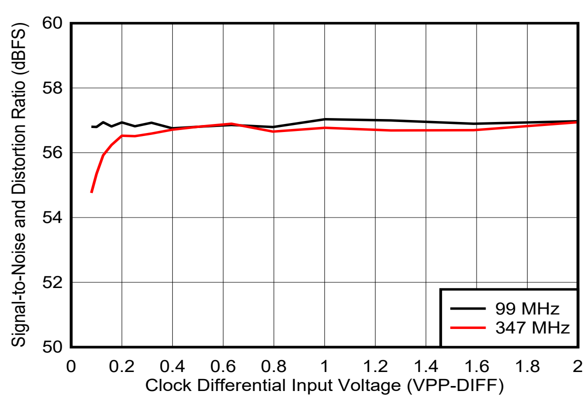
DES_EN = 0, f_S = 500MHz, FG calibration

Figure 5-30. SNR vs Clock Amplitude



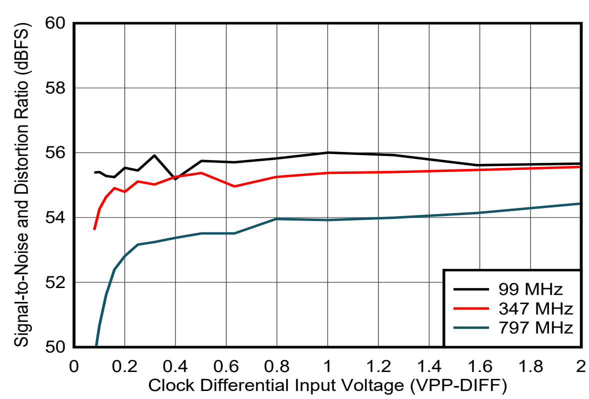
DES_EN = 1, f_S = 1000MHz, FG calibration

Figure 5-31. SNR vs Clock Amplitude



DES_EN = 0, f_S = 500MHz, FG calibration

Figure 5-32. SINAD vs Clock Amplitude

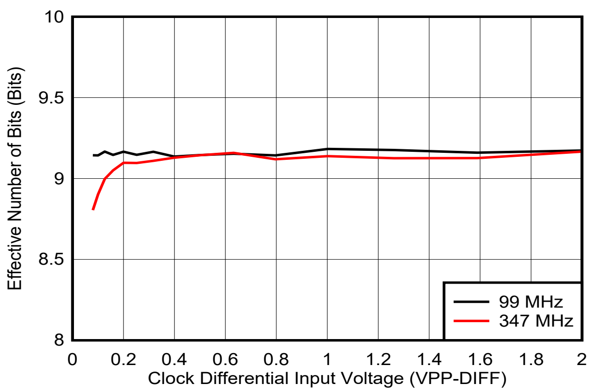


DES_EN = 1, f_S = 1000MHz, FG calibration

Figure 5-33. SINAD vs Clock Amplitude

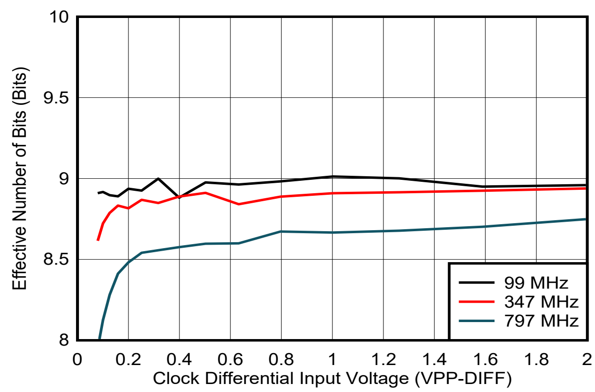
5.12 Typical Characteristics - ADC12DL500 (continued)

typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 97MHz, A_{IN} = –1dBFS, f_{CLK} = 500MHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



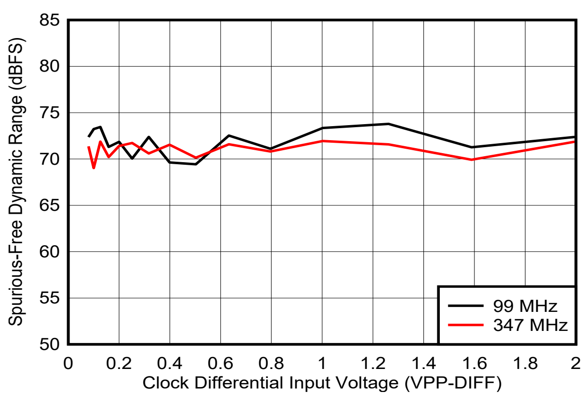
DES_EN = 0, f_S = 500MHz, FG calibration

Figure 5-34. ENOB vs Clock Amplitude



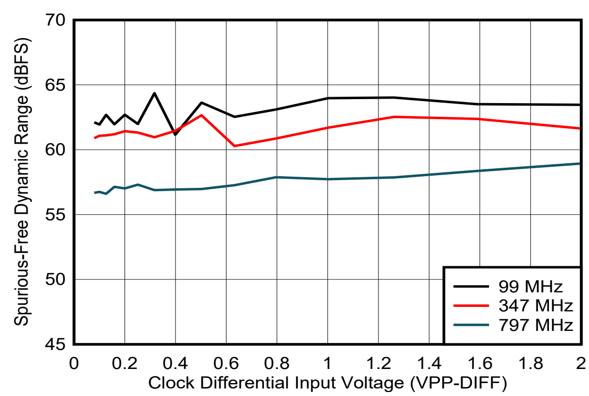
DES_EN = 1, f_S = 1000MHz, FG calibration

Figure 5-35. ENOB vs Clock Amplitude



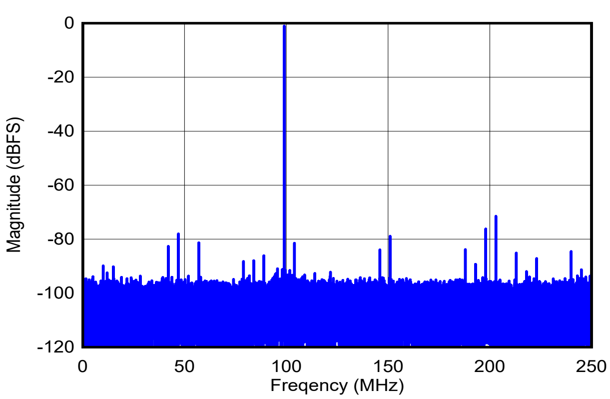
DES_EN = 0, f_S = 500MHz, FG calibration

Figure 5-36. SFDR vs Clock Amplitude



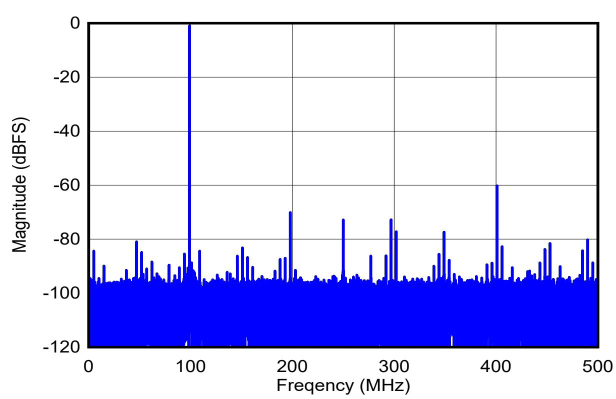
DES_EN = 1, f_S = 1000MHz, FG calibration

Figure 5-37. SFDR vs Clock Amplitude



DES_EN = 0, f_S = 500MHz, FG calibration, SNR = 57.5dBFS, SFDR = 71.4dBFS, ENOB = 9.2 bits

Figure 5-38. Single-Tone FFT at f_{IN} = 99MHz, AIN = –1dBFS

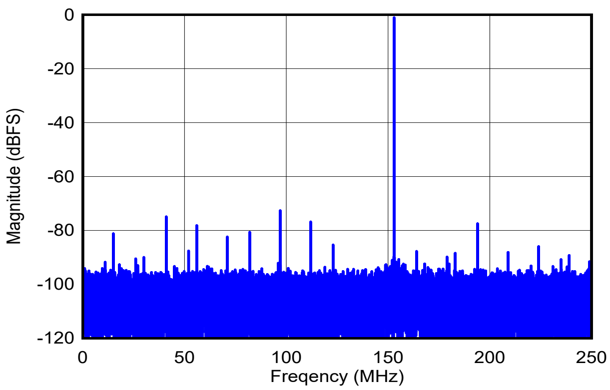


DES_EN = 1, f_S = 1000MHz, FG calibration, SNR = 57.1dBFS, SFDR = 60.5dBFS, ENOB = 8.8 bits

Figure 5-39. Single-Tone FFT at f_{IN} = 99MHz, AIN = –1dBFS

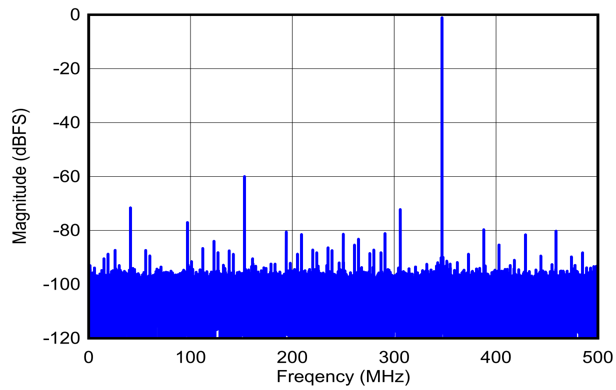
5.12 Typical Characteristics - ADC12DL500 (continued)

typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 97MHz, A_{IN} = –1dBFS, f_{CLK} = 500MHz, filtered 1V_{PP} sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



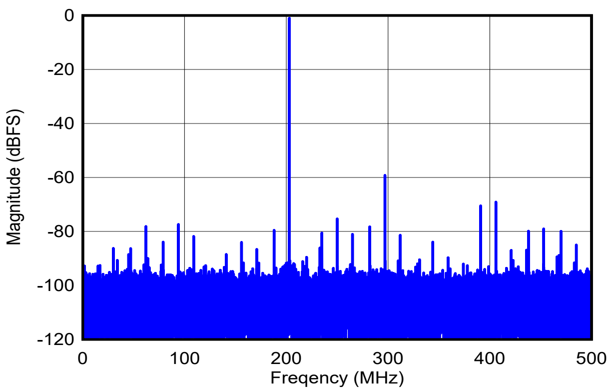
DES_EN = 0, f_S = 500MHz, FG calibration, SNR = 57.5dBFS, SFDR = 72.5dBFS, ENOB = 9.2 bits

Figure 5-40. Single-Tone FFT at f_{IN} = 347MHz, AIN = –1dBFS



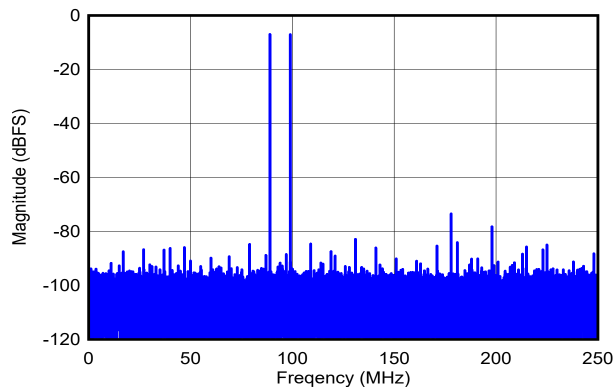
DES_EN = 1, f_S = 1000MHz, FG calibration, SNR = 57.3dBFS, SFDR = 60.0dBFS, ENOB = 8.8 bits

Figure 5-41. Single-Tone FFT at f_{IN} = 347MHz, AIN = –1dBFS



DES_EN = 1, f_S = 1000MHz, FG calibration, SNR = 57.1dBFS, SFDR = 59.0dBFS, ENOB = 8.7 bits

Figure 5-42. Single-Tone FFT at f_{IN} = 797MHz, AIN = –1dBFS

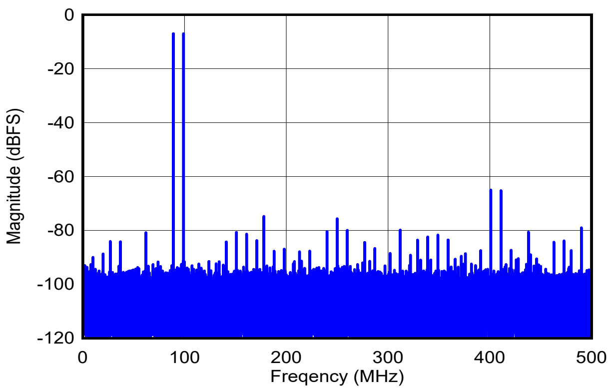


DES_EN = 0, f_S = 500MHz, FG calibration, f_1 = 89MHz, f_2 = 99MHz, A_{IN} = -7dBFS per tone, SFDR = -73dBFS, IMD3 = -85dBFS, IMD2 = -92dBFS

Figure 5-43. Two-Tone FFT at f_{IN} = 94MHz, AIN = –1dBFS

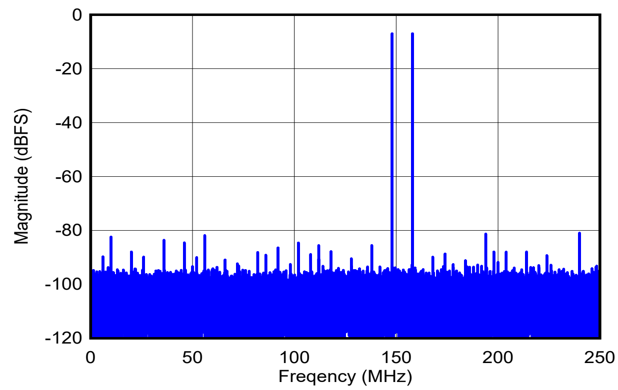
5.12 Typical Characteristics - ADC12DL500 (continued)

typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 97MHz, A_{IN} = –1dBFS, f_{CLK} = 500MHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



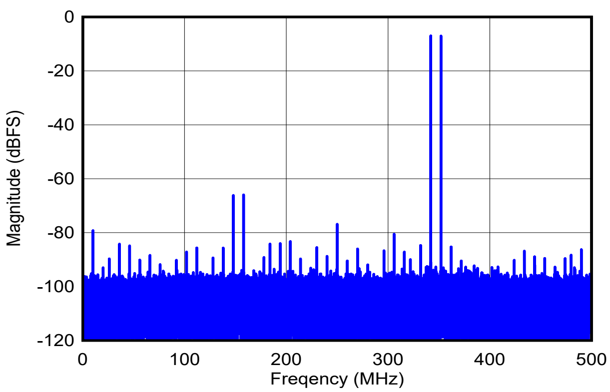
DES_EN = 1, f_S = 1000MHz, FG calibration, f_1 = 89MHz, f_2 = 99MHz, A_{IN} = -7dBFS per tone, SFDR = -65dBFS, IMD3 = -95dBFS, IMD2 = -89dBFS

Figure 5-44. Two-Tone FFT at f_{IN} = 94MHz, AIN = –1dBFS



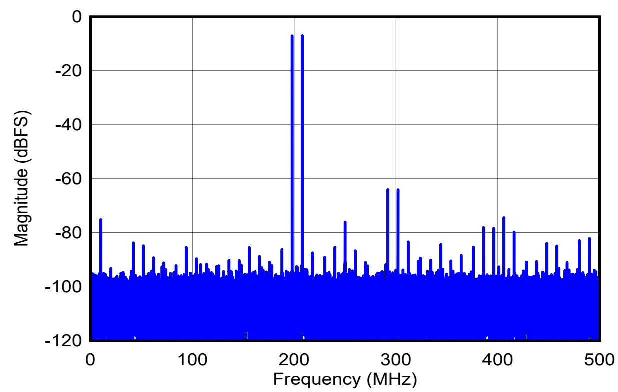
DES_EN = 0, f_S = 500MHz, FG calibration, f_1 = 342MHz, f_2 = 352MHz, A_{IN} = -7dBFS per tone, SFDR = -81dBFS, IMD3 = -87dBFS, IMD2 = -82dBFS

Figure 5-45. Two-Tone FFT at f_{IN} = 347MHz, AIN = –1dBFS



DES_EN = 1, f_S = 1000MHz, FG calibration, f_1 = 342MHz, f_2 = 352MHz, A_{IN} = -7dBFS per tone, SFDR = -66dBFS, IMD3 = -85dBFS, IMD2 = -80dBFS

Figure 5-46. Two-Tone FFT at f_{IN} = 347MHz, AIN = –1dBFS

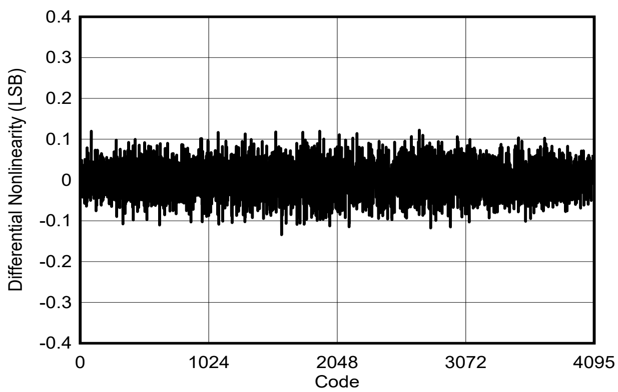


DES_EN = 1, f_S = 1000MHz, FG calibration, f_1 = 792MHz, f_2 = 802MHz, A_{IN} = -7dBFS per tone, SFDR = -64dBFS, IMD3 = -87dBFS, IMD2 = -75dBFS

Figure 5-47. Two-Tone FFT at f_{IN} = 797MHz, AIN = –1dBFS

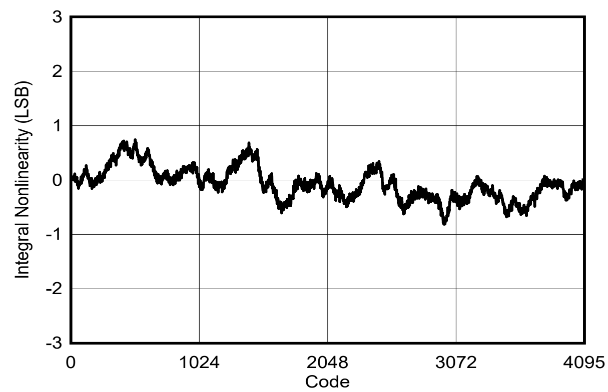
5.12 Typical Characteristics - ADC12DL500 (continued)

typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 97MHz, A_{IN} = –1dBFS, f_{CLK} = 500MHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



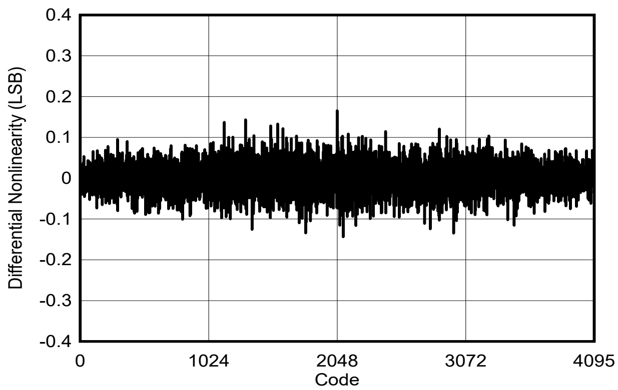
DES_EN = 0, f_S = 500MHz, FG calibration, F_{IN} = 99MHz

Figure 5-48. DNL vs Code



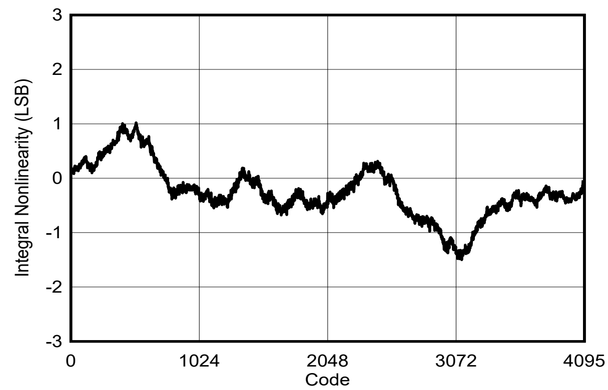
DES_EN = 0, f_S = 500MHz, FG calibration, F_{IN} = 99MHz

Figure 5-49. INL vs Code



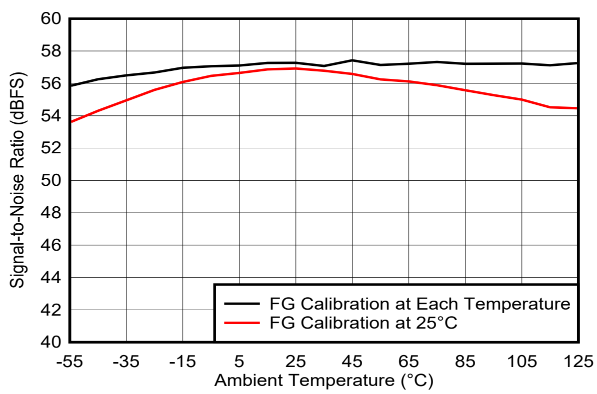
DES_EN = 1, f_S = 1000MHz, FG calibration, F_{IN} = 99MHz

Figure 5-50. DNL vs Code



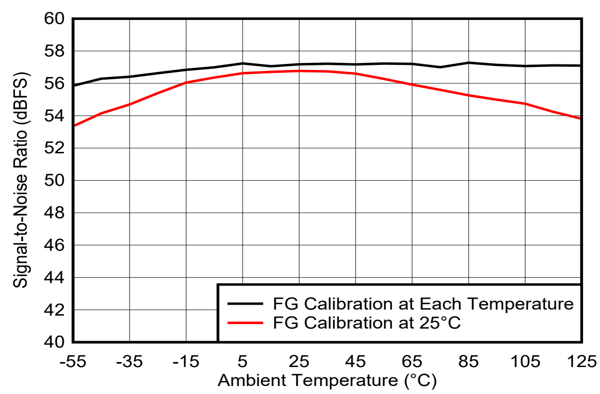
DES_EN = 1, f_S = 1000MHz, FG calibration, F_{IN} = 99MHz

Figure 5-51. INL vs Code



DES_EN = 0, f_S = 500MHz, F_{IN} = 99MHz, A_{IN} = -1dBFS

Figure 5-52. SNR vs Temperature and Calibration Mode

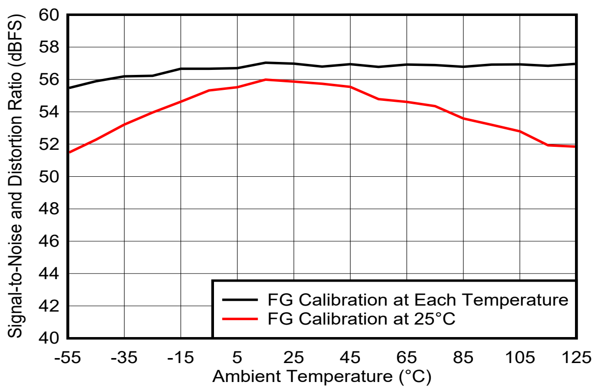


DES_EN = 1, f_S = 1000MHz, F_{IN} = 99MHz, A_{IN} = -1dBFS

Figure 5-53. SNR vs Temperature and Calibration Mode

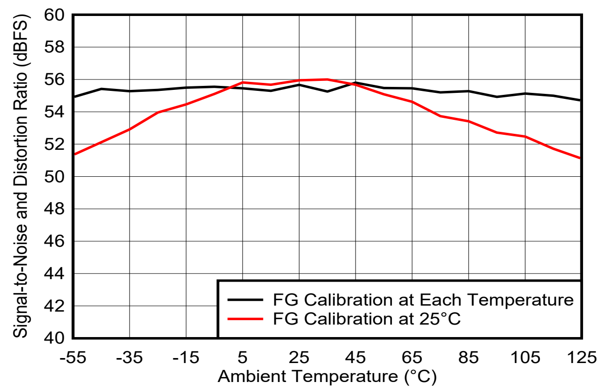
5.12 Typical Characteristics - ADC12DL500 (continued)

typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 97MHz, A_{IN} = –1dBFS, f_{CLK} = 500MHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



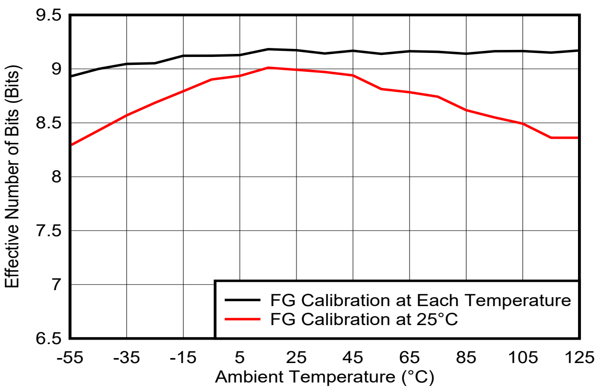
DES_EN = 0, f_S = 500MHz, F_{IN} = 99MHz, A_{IN} = -1dBFS

Figure 5-54. SINAD vs Temperature and Calibration Mode



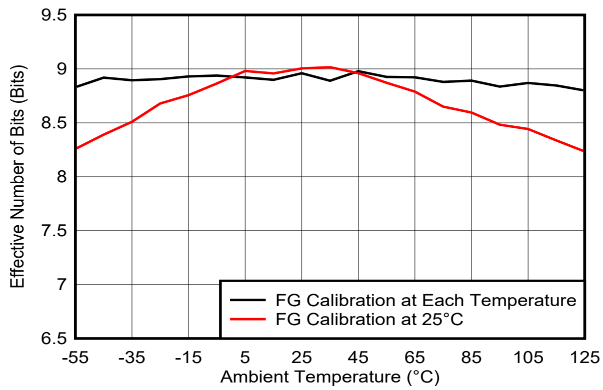
DES_EN = 1, f_S = 1000MHz, F_{IN} = 99MHz, A_{IN} = -1dBFS

Figure 5-55. SINAD vs Temperature and Calibration Mode



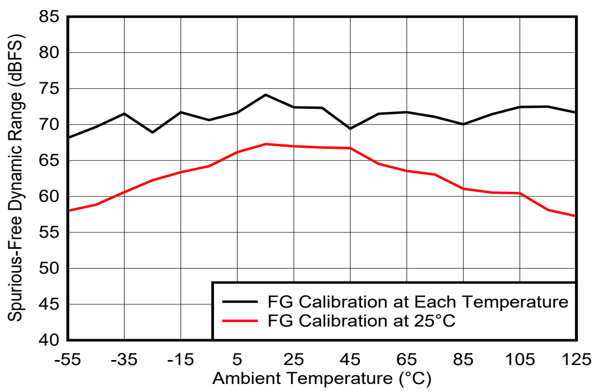
DES_EN = 0, f_S = 500MHz, F_{IN} = 99MHz, A_{IN} = -1dBFS

Figure 5-56. ENOB vs Temperature and Calibration Mode



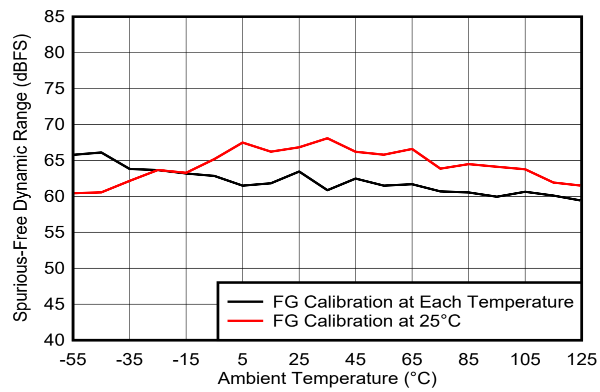
DES_EN = 1, f_S = 1000MHz, F_{IN} = 99MHz, A_{IN} = -1dBFS

Figure 5-57. ENOB vs Temperature and Calibration Mode



DES_EN = 0, f_S = 500MHz, F_{IN} = 99MHz, A_{IN} = -1dBFS

Figure 5-58. SFDR vs Temperature and Calibration Mode

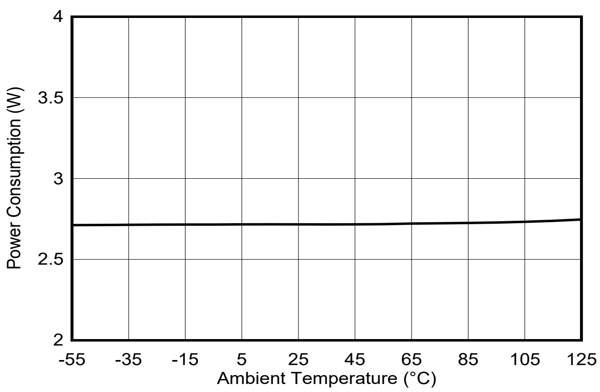


DES_EN = 1, f_S = 1000MHz, F_{IN} = 99MHz, A_{IN} = -1dBFS

Figure 5-59. SFDR vs Temperature and Calibration Mode

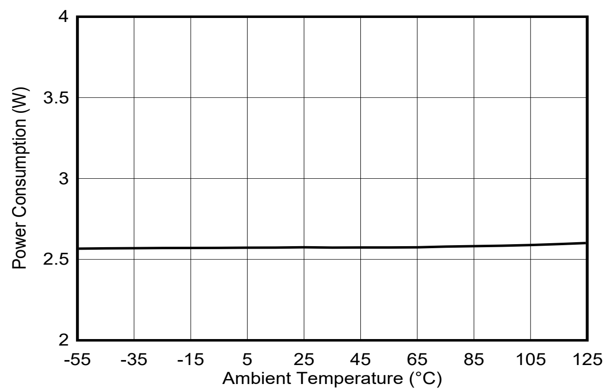
5.12 Typical Characteristics - ADC12DL500 (continued)

typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 97MHz, A_{IN} = –1dBFS, f_{CLK} = 500MHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



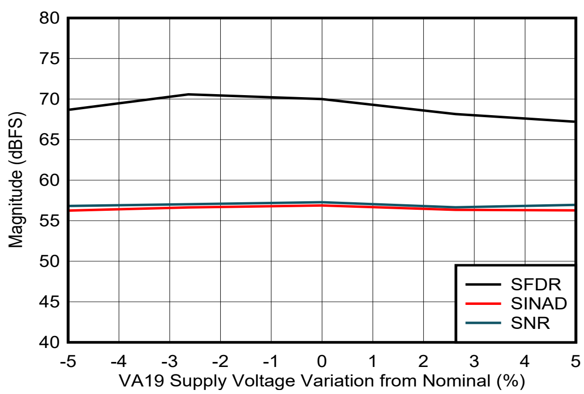
DES_EN = 0, f_S = 500MHz, F_{IN} = 99MHz, A_{IN} = -1dBFS

Figure 5-60. Power Consumption vs Temperature



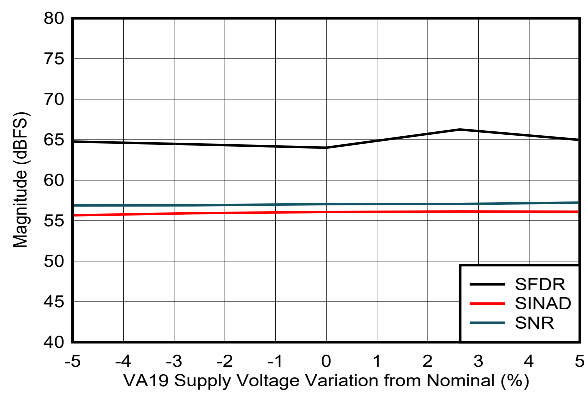
DES_EN = 1, f_S = 1000MHz, F_{IN} = 99MHz, A_{IN} = -1dBFS

Figure 5-61. Power Consumption vs Temperature



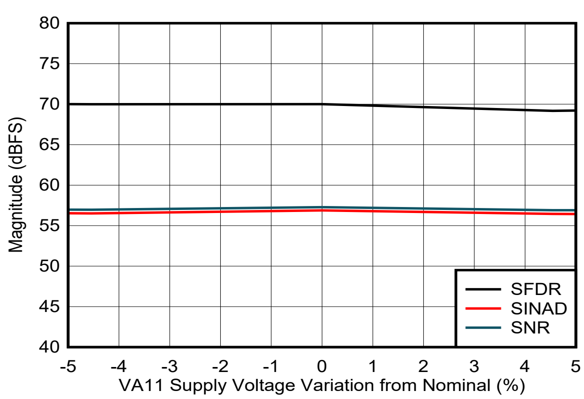
DES_EN = 0, f_S = 500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-62. Performance vs VA19 Supply Voltage



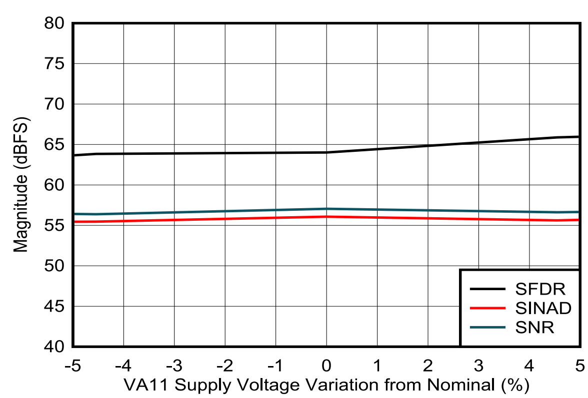
DES_EN = 1, f_S = 1000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-63. Performance vs VA19 Supply Voltage



DES_EN = 0, f_S = 500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-64. Performance vs VA11 Supply Voltage

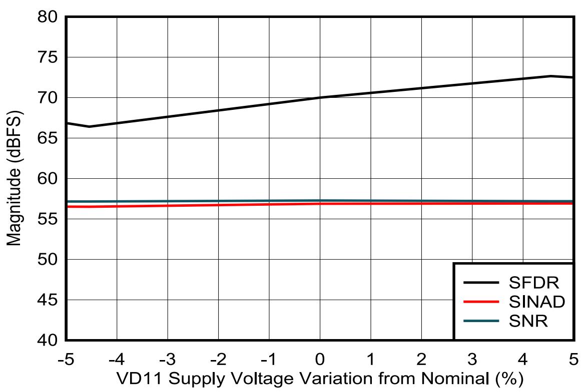


DES_EN = 1, f_S = 1000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-65. Performance vs VA11 Supply Voltage

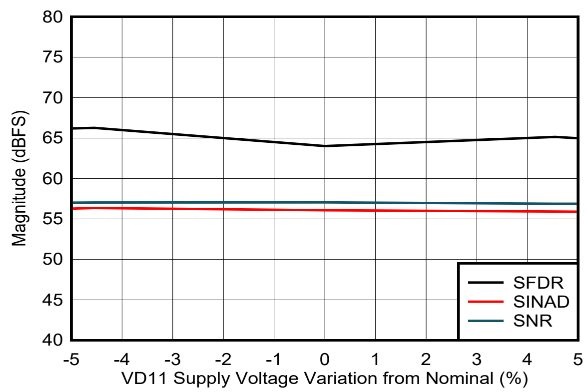
5.12 Typical Characteristics - ADC12DL500 (continued)

typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 97MHz, A_{IN} = –1dBFS, f_{CLK} = 500MHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



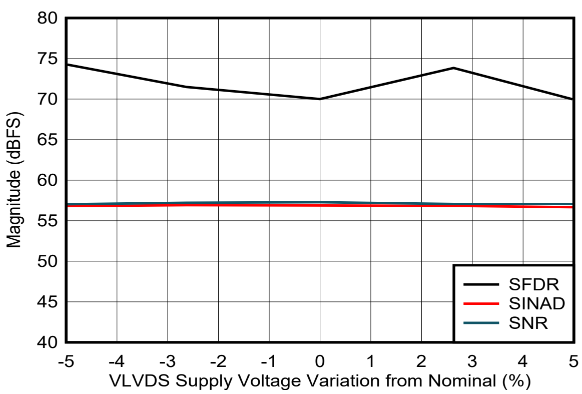
DES_EN = 0, f_S = 500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-66. Performance vs VD11 Supply Voltage



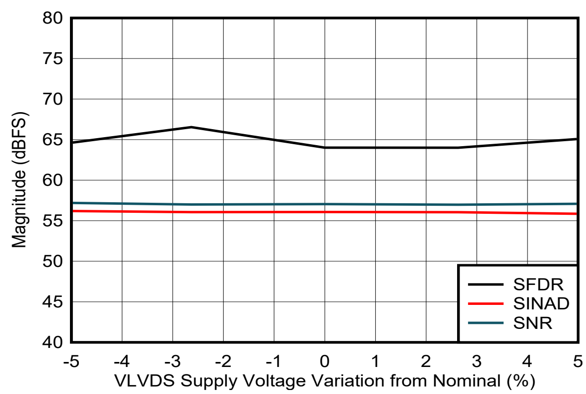
DES_EN = 1, f_S = 1000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-67. Performance vs VD11 Supply Voltage



DES_EN = 0, f_S = 500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-68. Performance vs VLVDS Supply Voltage

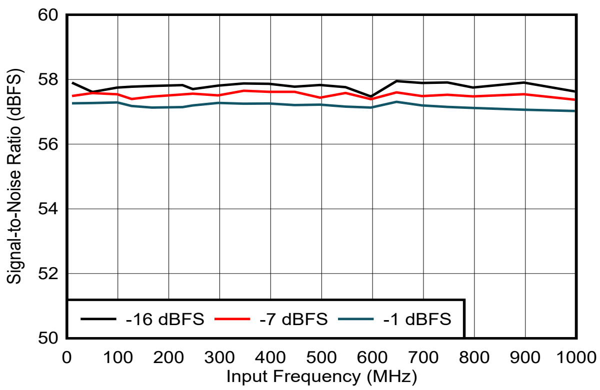


DES_EN = 1, f_S = 1000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-69. Performance vs VLVDS Supply Voltage

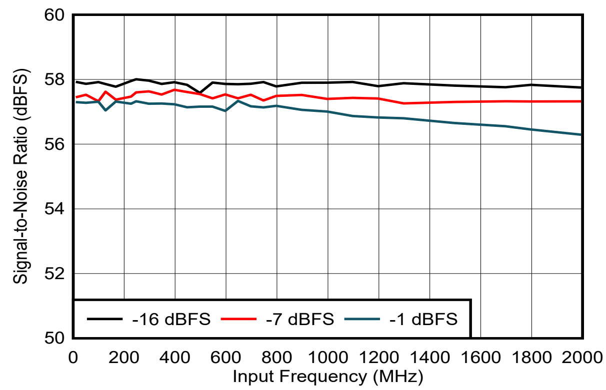
5.13 Typical Characteristics - ADC12DL1500 (1GSPS)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 1GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



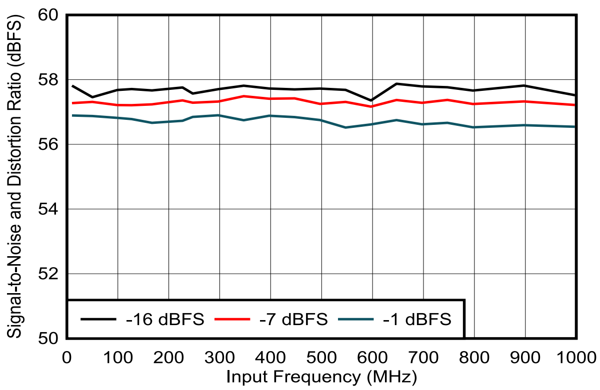
DES_EN = 0, f_S = 1000MHz, FG calibration

Figure 5-70. SNR vs Input Frequency



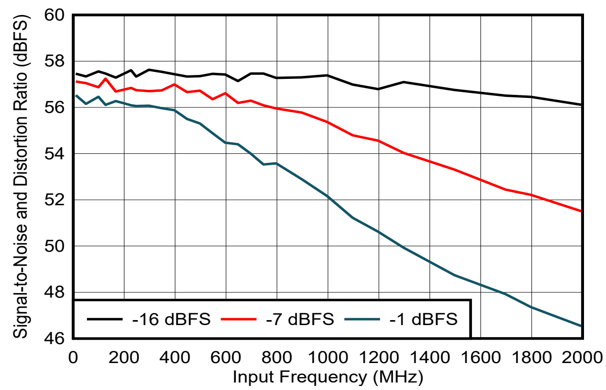
DES_EN = 1, f_S = 2000MHz, FG calibration

Figure 5-71. SNR vs Input Frequency



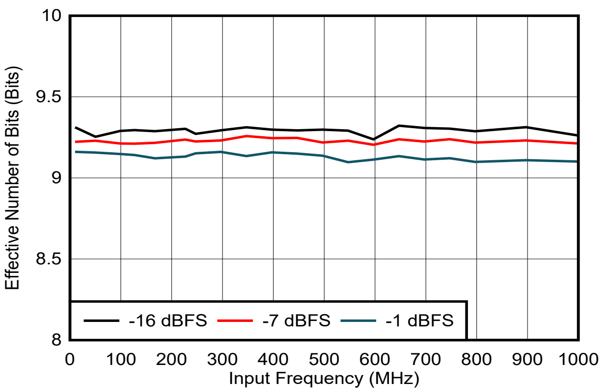
DES_EN = 0, f_S = 1000MHz, FG calibration

Figure 5-72. SINAD vs Input Frequency



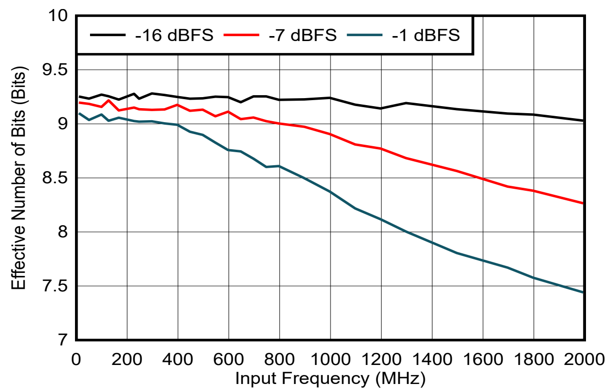
DES_EN = 1, f_S = 2000MHz, FG calibration

Figure 5-73. SINAD vs Input Frequency



DES_EN = 0, f_S = 1000MHz, FG calibration

Figure 5-74. ENOB vs Input Frequency

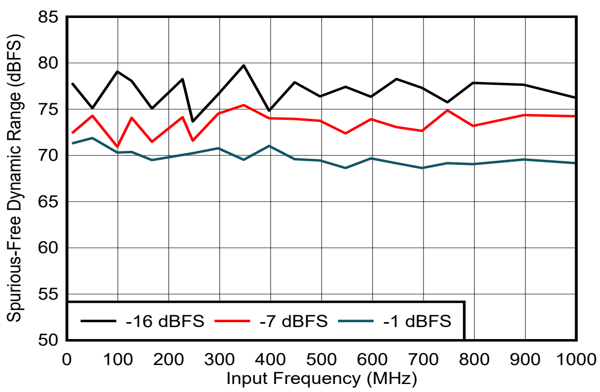


DES_EN = 1, f_S = 2000MHz, FG calibration

Figure 5-75. ENOB vs Input Frequency

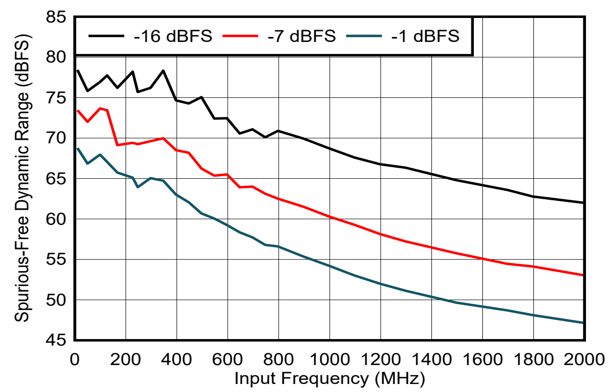
5.13 Typical Characteristics - ADC12DL1500 (1GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 1GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



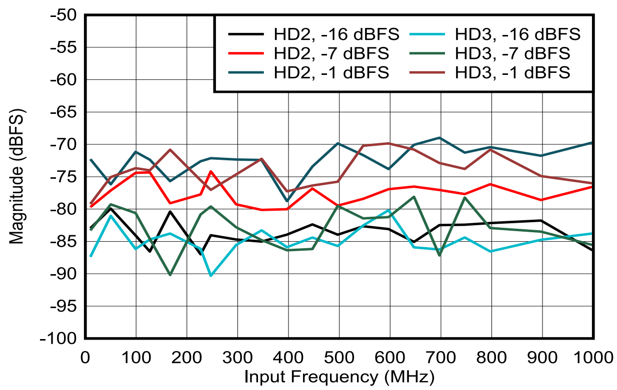
DES_EN = 0, f_S = 1000MHz, FG calibration

Figure 5-76. SFDR vs Input Frequency



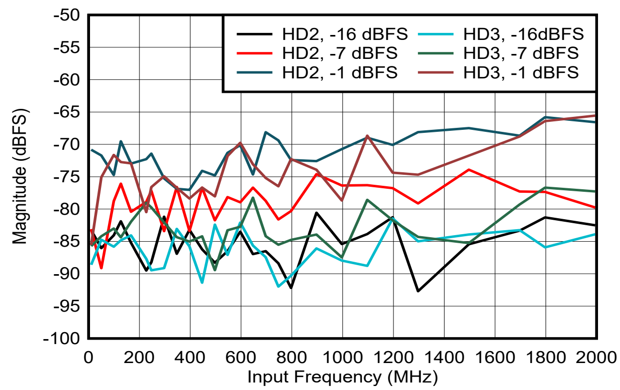
DES_EN = 1, f_S = 2000MHz, FG calibration

Figure 5-77. SFDR vs Input Frequency



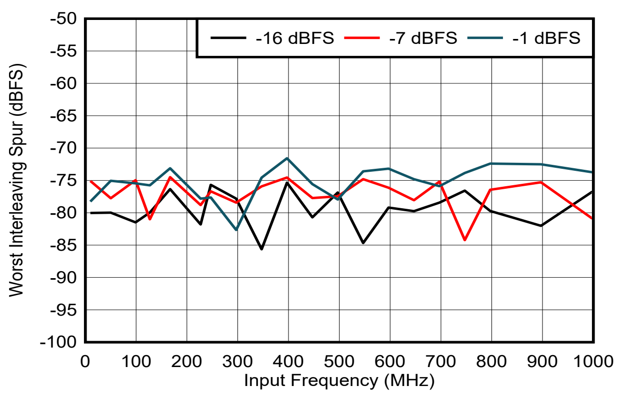
DES_EN = 0, f_S = 1000MHz, FG calibration

Figure 5-78. HD2 and HD3 vs Input Frequency



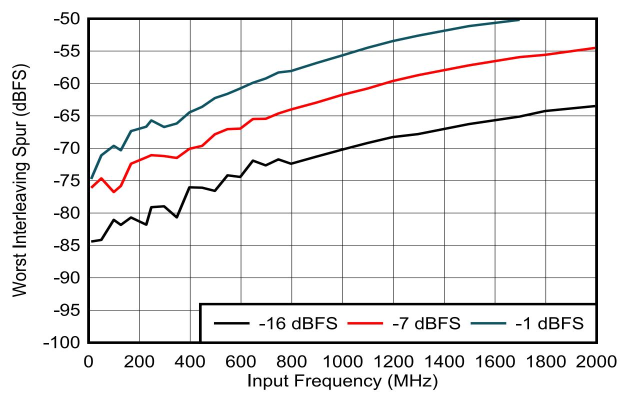
DES_EN = 1, f_S = 2000MHz, FG calibration

Figure 5-79. HD2 and HD3 vs Input Frequency



DES_EN = 0, f_S = 1000MHz, FG calibration, includes f_S / 2 – f_{IN} spur only

Figure 5-80. Worst Interleaving Spur vs Input Frequency

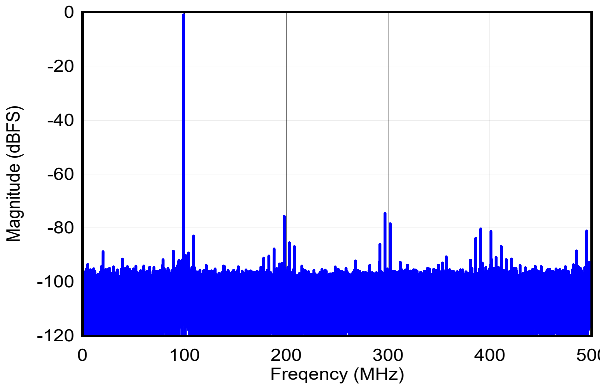


DES_EN = 1, f_S = 2000MHz, FG calibration, includes f_S / 2 – f_{IN} and f_S /4 ± f_{IN} spurs only

Figure 5-81. Worst Interleaving Spur vs Input Frequency

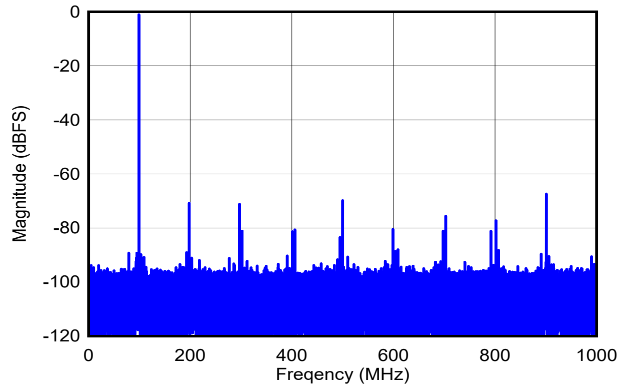
5.13 Typical Characteristics - ADC12DL1500 (1GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 1GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



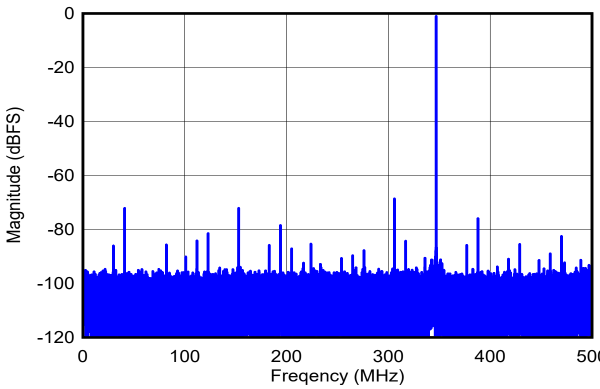
DES_EN = 0, f_S = 1000MHz, FG calibration, SNR = 57.5dBFS, SFDR = 74.4dBFS, ENOB = 9.2 bits

Figure 5-82. Single-Tone FFT at f_{IN} = 99MHz, AIN = –1dBFS



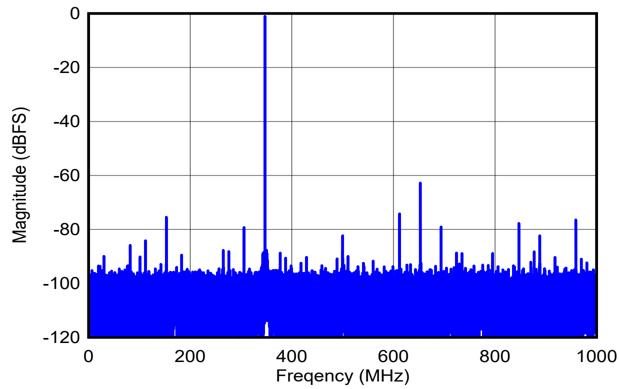
DES_EN = 1, f_S = 2000MHz, FG calibration, SNR = 57.4dBFS, SFDR = 67.3dBFS, ENOB = 9.0 bits

Figure 5-83. Single-Tone FFT at f_{IN} = 99MHz, AIN = –1dBFS



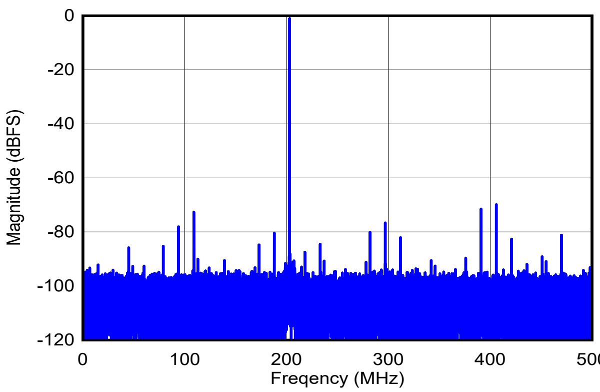
DES_EN = 0, f_S = 1000MHz, FG calibration, SNR = 57.8dBFS, SFDR = 68.5dBFS, ENOB = 9.1 bits

Figure 5-84. Single-Tone FFT at f_{IN} = 347MHz, AIN = –1dBFS



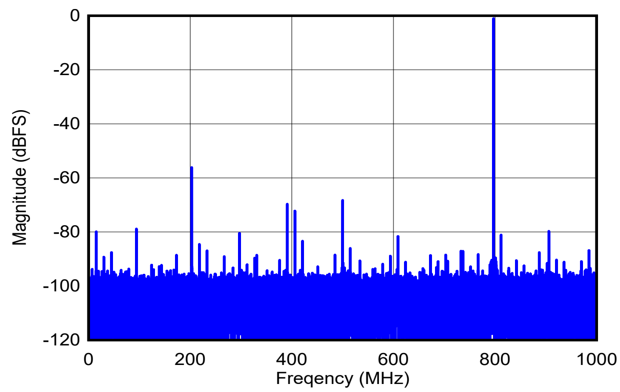
DES_EN = 1, f_S = 2000MHz, FG calibration, SNR = 57.5dBFS, SFDR = 62.8dBFS, ENOB = 9.0 bits

Figure 5-85. Single-Tone FFT at f_{IN} = 347MHz, AIN = –1dBFS



DES_EN = 0, f_S = 1000MHz, FG calibration, SNR = 57.3dBFS, SFDR = 69.8dBFS, ENOB = 9.1 bits

Figure 5-86. Single-Tone FFT at f_{IN} = 797MHz, AIN = –1dBFS

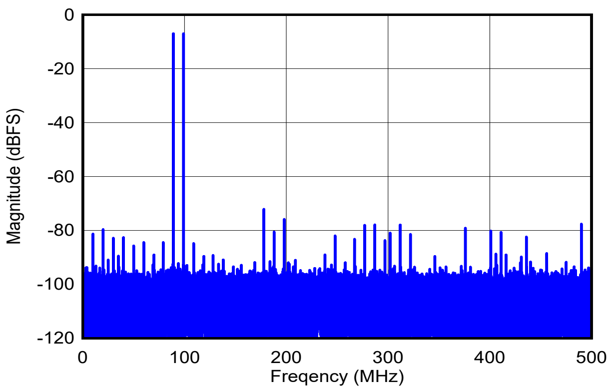


DES_EN = 1, f_S = 2000MHz, FG calibration, SNR = 57.3dBFS, SFDR = 56.0dBFS, ENOB = 8.5 bits

Figure 5-87. Single-Tone FFT at f_{IN} = 797MHz, AIN = –1dBFS

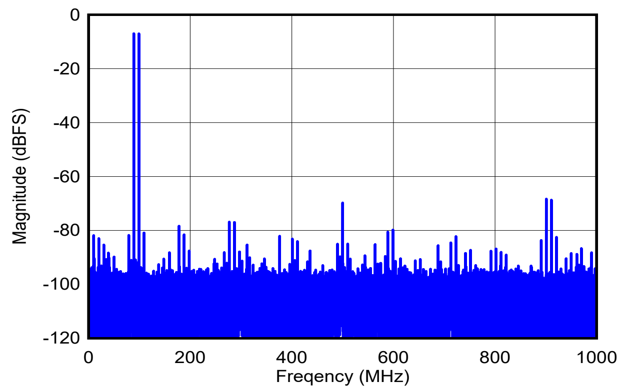
5.13 Typical Characteristics - ADC12DL1500 (1GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 1GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



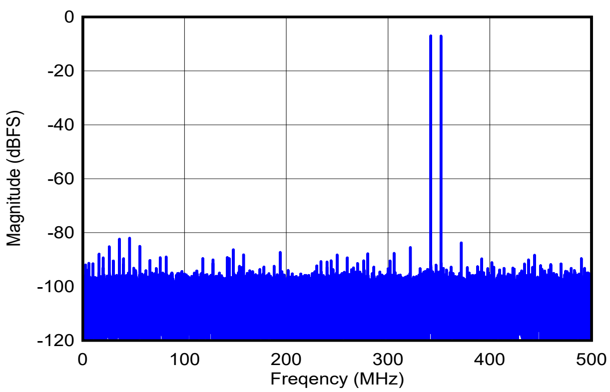
DES_EN = 0, f_S = 1000MHz, FG calibration, f_1 = 89MHz, f_2 = 99MHz, A_{IN} = -7dBFS per tone, SFDR = -72dBFS, IMD3 = -85dBFS, IMD2 = -81dBFS

Figure 5-88. Two-Tone FFT at f_{IN} = 94MHz, AIN = –1dBFS



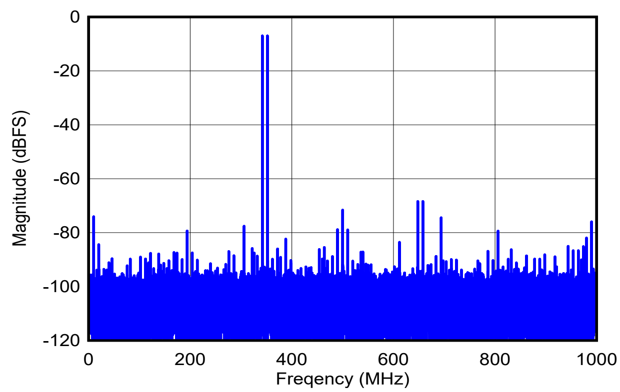
DES_EN = 1, f_S = 2000MHz, FG calibration, f_1 = 89MHz, f_2 = 99MHz, A_{IN} = -7dBFS per tone, SFDR = -68dBFS, IMD3 = -81dBFS, IMD2 = -82dBFS

Figure 5-89. Two-Tone FFT at f_{IN} = 94MHz, AIN = –1dBFS



DES_EN = 0, f_S = 1000MHz, FG calibration, f_1 = 342MHz, f_2 = 352MHz, A_{IN} = -7dBFS per tone, SFDR = -82dBFS, IMD3 = -96dBFS, IMD2 = -89dBFS

Figure 5-90. Two-Tone FFT at f_{IN} = 347MHz, AIN = –1dBFS

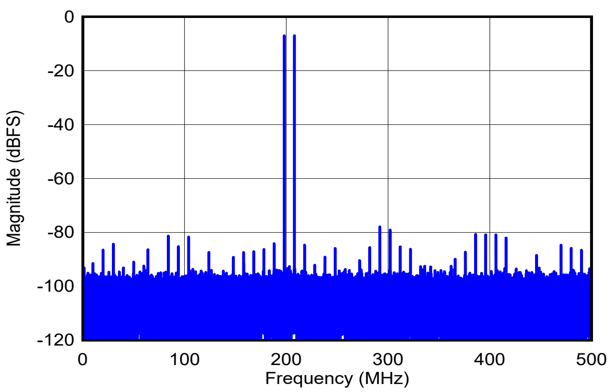


DES_EN = 1, f_S = 2000MHz, FG calibration, f_1 = 342MHz, f_2 = 352MHz, A_{IN} = -7dBFS per tone, SFDR = -68dBFS, IMD3 = -89dBFS, IMD2 = -74dBFS

Figure 5-91. Two-Tone FFT at f_{IN} = 347MHz, AIN = –1dBFS

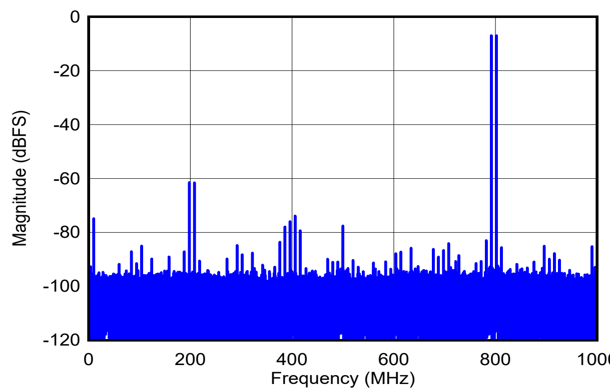
5.13 Typical Characteristics - ADC12DL1500 (1GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 1GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



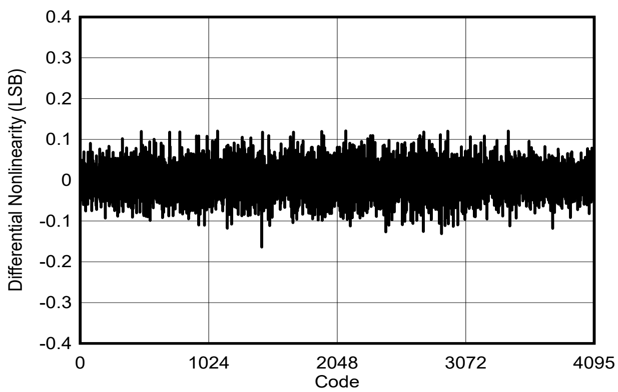
DES_EN = 0, f_S = 1000MHz, FG calibration, f_1 = 792MHz, f_2 = 802MHz, A_{IN} = -7dBFS per tone, SFDR = -78dBFS, IMD3 = -84dBFS, IMD2 = -85dBFS

Figure 5-92. Two-Tone FFT at f_{IN} = 797MHz, AIN = –1dBFS



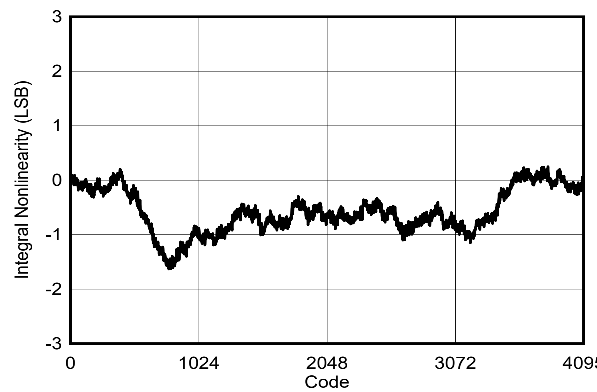
DES_EN = 1, f_S = 2000MHz, FG calibration, f_1 = 792MHz, f_2 = 802MHz, A_{IN} = -7dBFS per tone, SFDR = -62dBFS, IMD3 = -84dBFS, IMD2 = -74dBFS

Figure 5-93. Two-Tone FFT at f_{IN} = 797MHz, AIN = –1dBFS



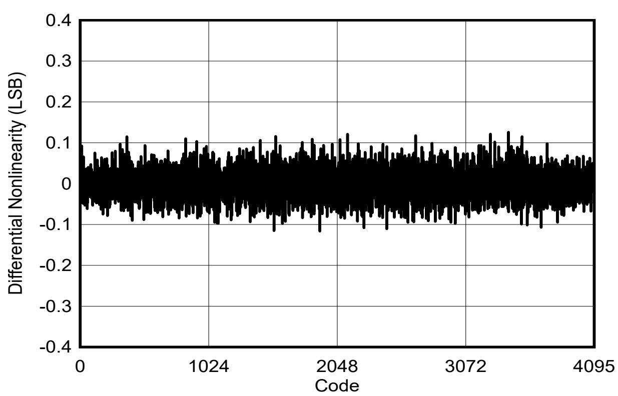
DES_EN = 0, f_S = 1000MHz, FG calibration, F_{IN} = 99MHz

Figure 5-94. DNL vs Code



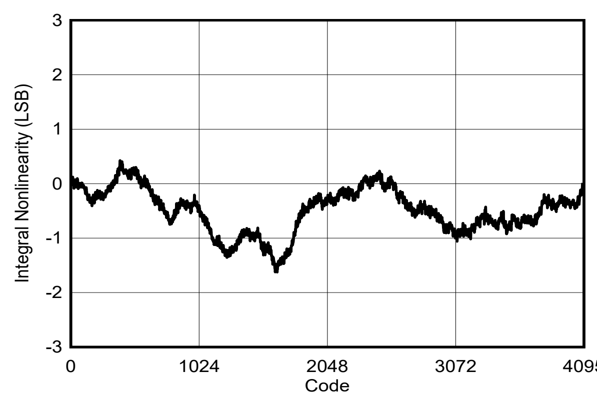
DES_EN = 0, f_S = 1000MHz, FG calibration, F_{IN} = 99MHz

Figure 5-95. INL vs Code



DES_EN = 1, f_S = 2000MHz, FG calibration, F_{IN} = 99MHz

Figure 5-96. DNL vs Code

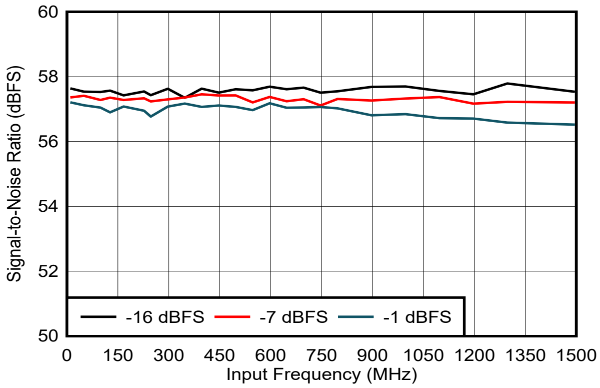


DES_EN = 1, f_S = 2000MHz, FG calibration, F_{IN} = 99MHz

Figure 5-97. INL vs Code

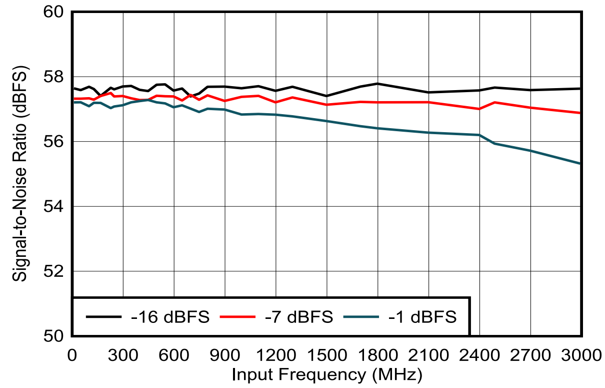
5.14 Typical Characteristics - ADC12DL1500 (1.5GSPS)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 1.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



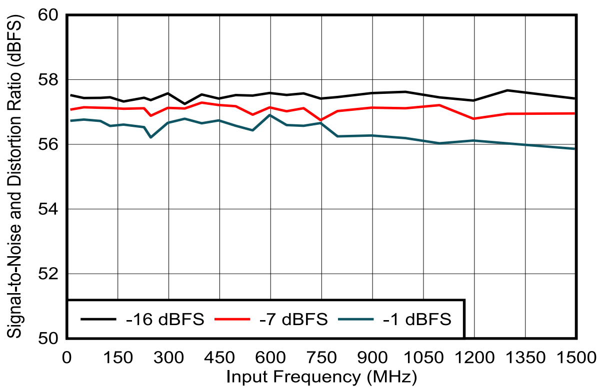
DES_EN = 0, f_S = 1500MHz, FG calibration

Figure 5-98. SNR vs Input Frequency



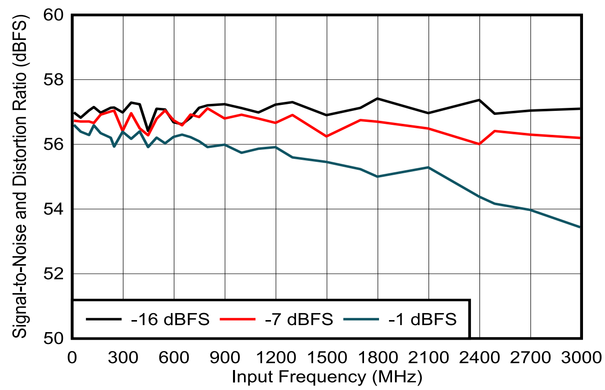
DES_EN = 1, f_S = 3000MHz, FG calibration

Figure 5-99. SNR vs Input Frequency



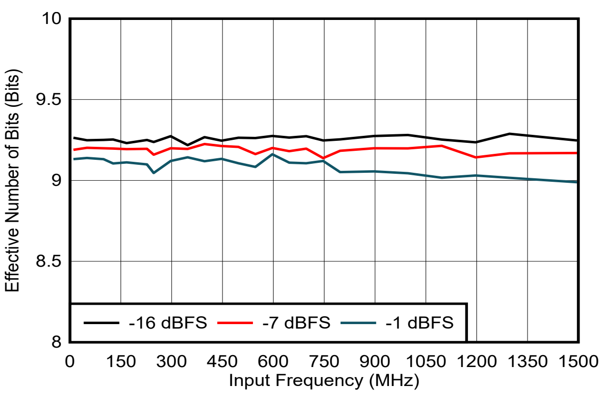
DES_EN = 0, f_S = 1500MHz, FG calibration

Figure 5-100. SINAD vs Input Frequency



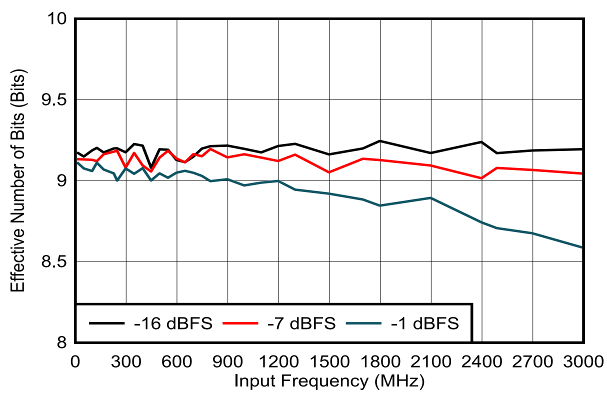
DES_EN = 1, f_S = 3000MHz, FG calibration

Figure 5-101. SINAD vs Input Frequency



DES_EN = 0, f_S = 1500MHz, FG calibration

Figure 5-102. ENOB vs Input Frequency

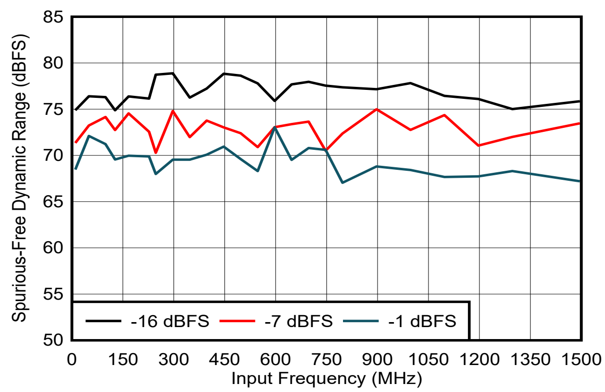


DES_EN = 1, f_S = 3000MHz, FG calibration

Figure 5-103. ENOB vs Input Frequency

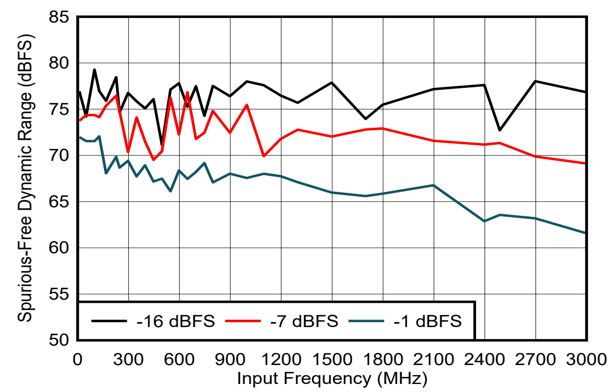
5.14 Typical Characteristics - ADC12DL1500 (1.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 1.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



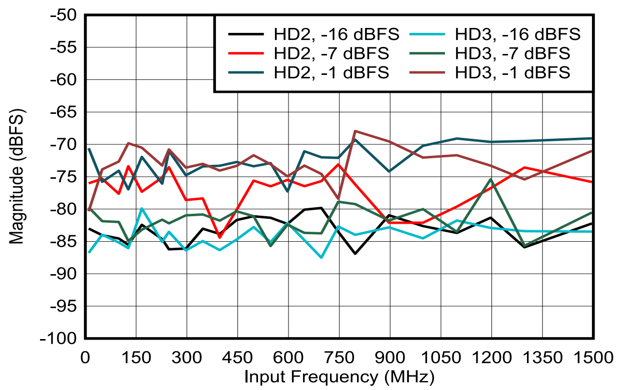
DES_EN = 0, f_S = 1500MHz, FG calibration

Figure 5-104. SFDR vs Input Frequency



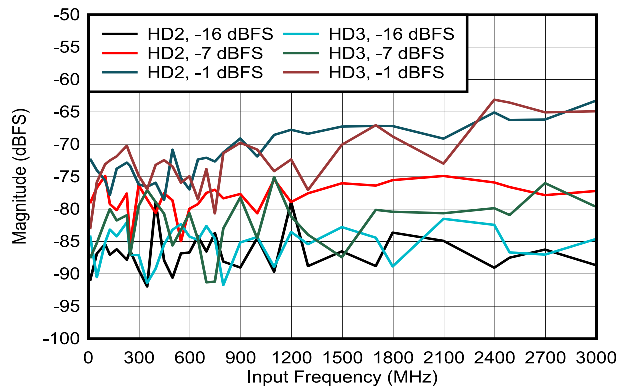
DES_EN = 1, f_S = 3000MHz, FG calibration

Figure 5-105. SFDR vs Input Frequency



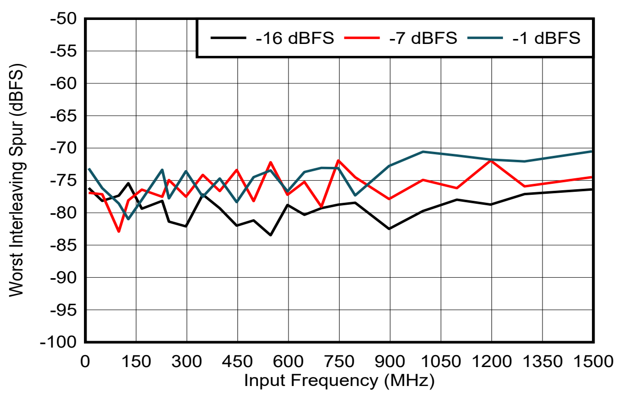
DES_EN = 0, f_S = 1500MHz, FG calibration

Figure 5-106. HD2 and HD3 vs Input Frequency



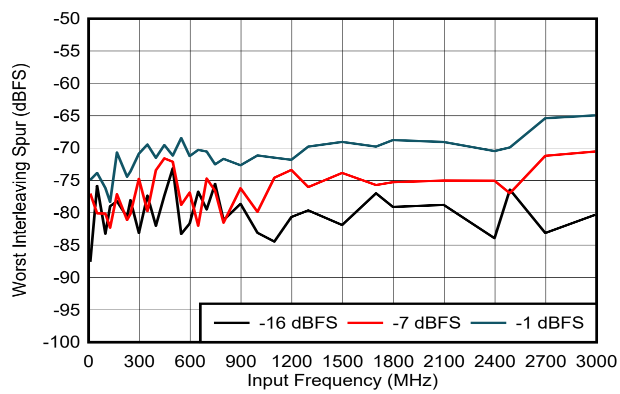
DES_EN = 1, f_S = 3000MHz, FG calibration

Figure 5-107. HD2 and HD3 vs Input Frequency



DES_EN = 0, f_S = 1500MHz, FG calibration, includes f_S / 2 – f_{IN} spur only

Figure 5-108. Worst Interleaving Spur vs Input Frequency

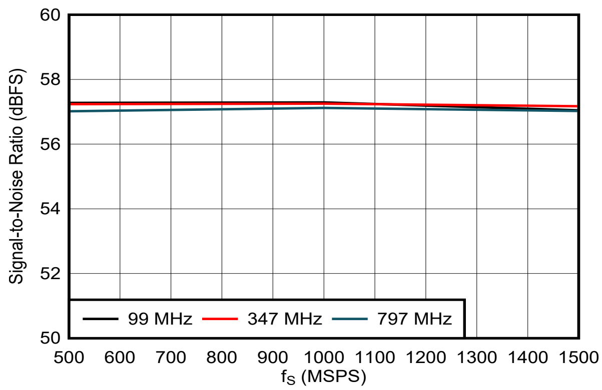


DES_EN = 1, f_S = 3000MHz, FG calibration, includes f_S / 2 – f_{IN} and f_S /4 ± f_{IN} spurs only

Figure 5-109. Worst Interleaving Spur vs Input Frequency

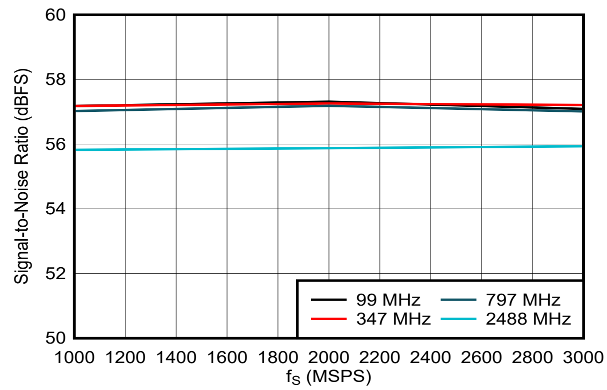
5.14 Typical Characteristics - ADC12DL1500 (1.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 1.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



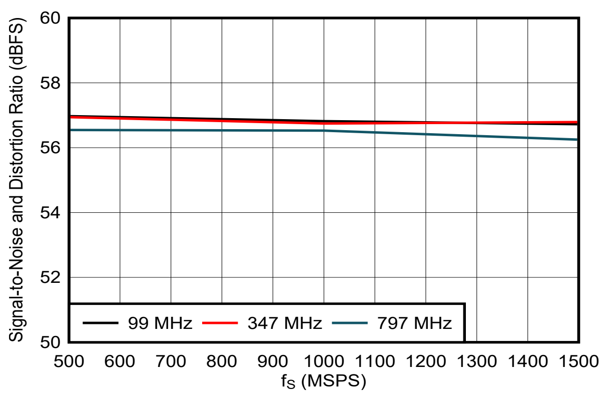
DES_EN = 0, f_S = 1500MHz, FG calibration

Figure 5-110. SNR vs Sampling Rate



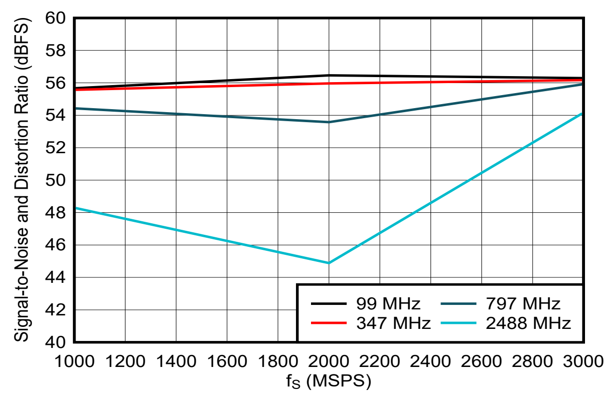
DES_EN = 1, f_S = 3000MHz, FG calibration

Figure 5-111. SNR vs Sampling Rate



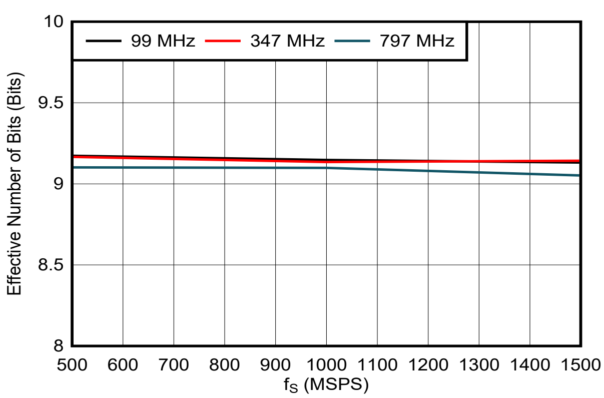
DES_EN = 0, f_S = 1500MHz, FG calibration

Figure 5-112. SINAD vs Sampling Rate



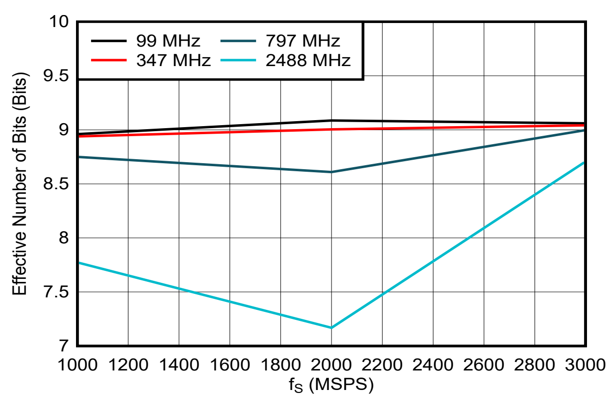
DES_EN = 1, f_S = 3000MHz, FG calibration

Figure 5-113. SINAD vs Sampling Rate



DES_EN = 0, f_S = 1500MHz, FG calibration

Figure 5-114. ENOB vs Sampling Rate

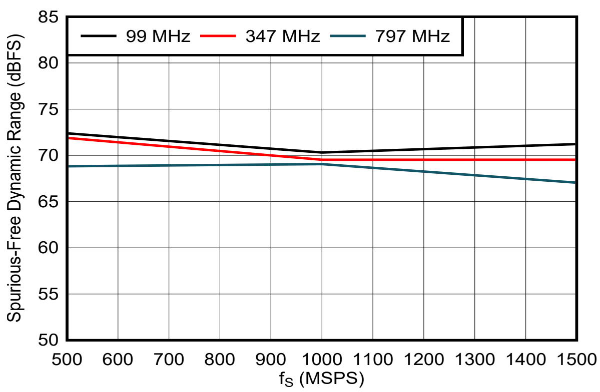


DES_EN = 1, f_S = 3000MHz, FG calibration

Figure 5-115. ENOB vs Sampling Rate

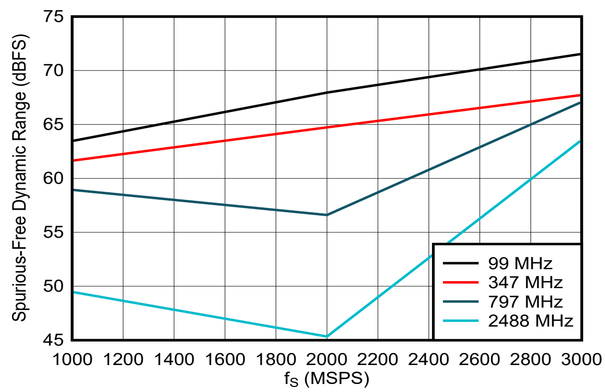
5.14 Typical Characteristics - ADC12DL1500 (1.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 1.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



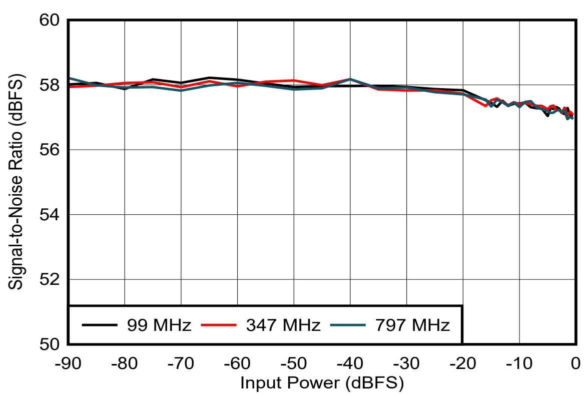
DES_EN = 0, f_S = 1500MHz, FG calibration

Figure 5-116. SFDR vs Sampling Rate



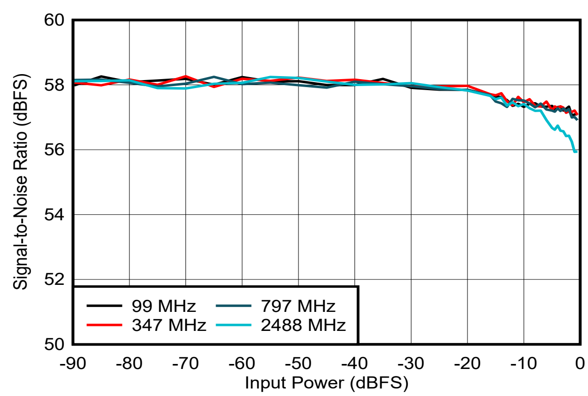
DES_EN = 1, f_S = 3000MHz, FG calibration

Figure 5-117. SFDR vs Sampling Rate



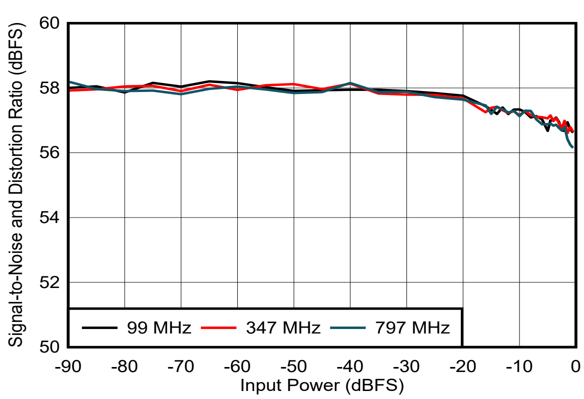
DES_EN = 0, f_S = 1500MHz, FG calibration

Figure 5-118. SNR vs Input Power



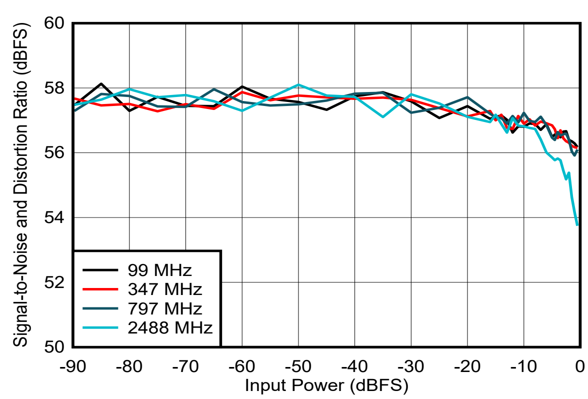
DES_EN = 1, f_S = 3000MHz, FG calibration

Figure 5-119. SNR vs Input Power



DES_EN = 0, f_S = 1500MHz, FG calibration

Figure 5-120. SINAD vs Input Power

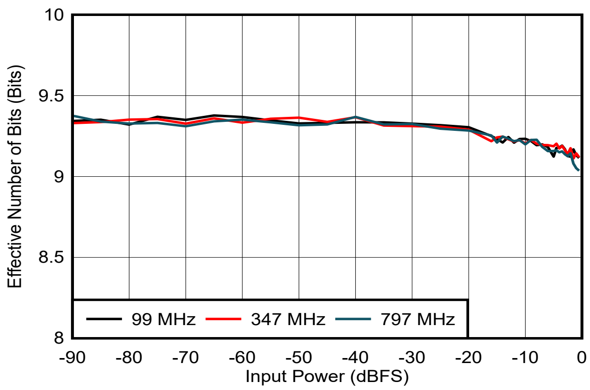


DES_EN = 1, f_S = 3000MHz, FG calibration

Figure 5-121. SINAD vs Input Power

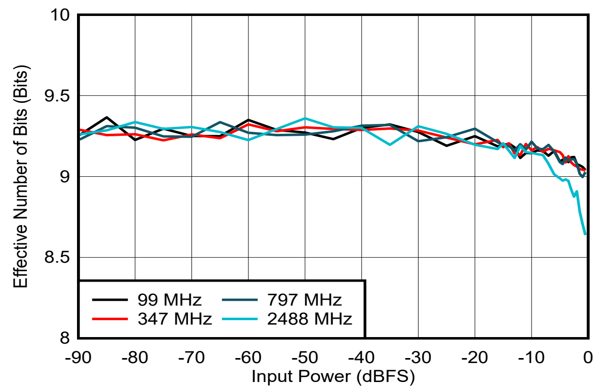
5.14 Typical Characteristics - ADC12DL1500 (1.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 1.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



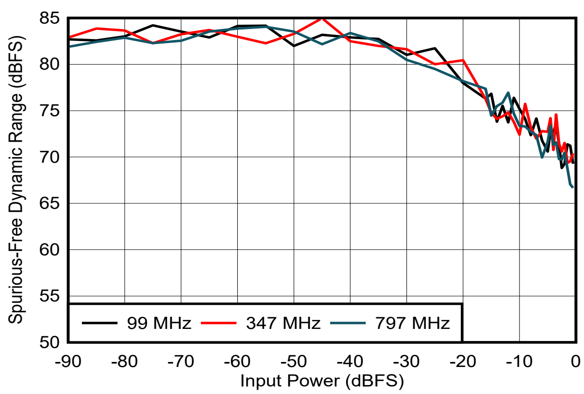
DES_EN = 0, f_S = 1500MHz, FG calibration

Figure 5-122. ENOB vs Input Power



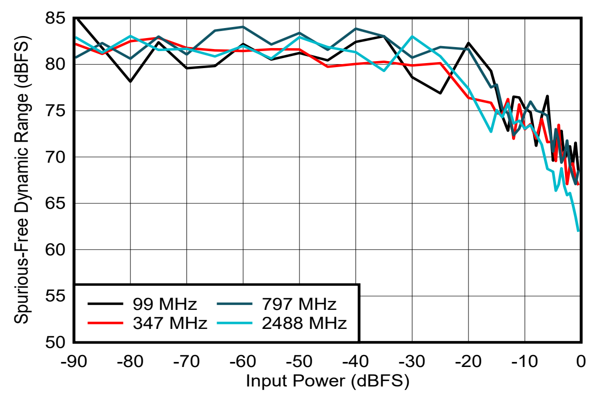
DES_EN = 1, f_S = 3000MHz, FG calibration

Figure 5-123. ENOB vs Input Power



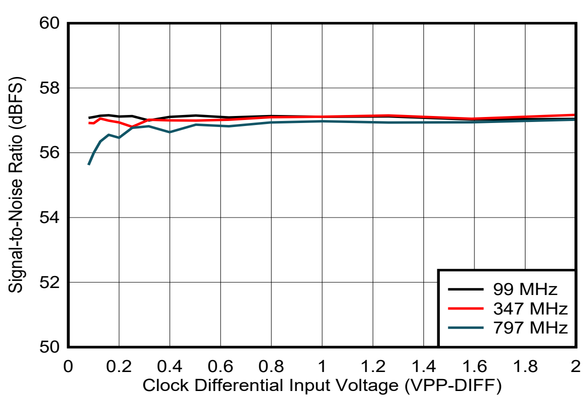
DES_EN = 0, f_S = 1500MHz, FG calibration

Figure 5-124. SFDR vs Input Power



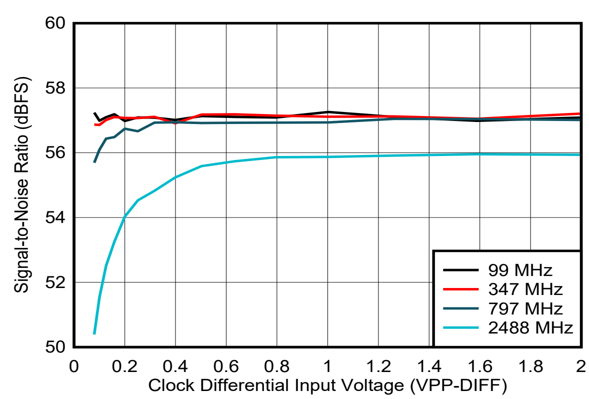
DES_EN = 1, f_S = 3000MHz, FG calibration

Figure 5-125. SFDR vs Input Frequency



DES_EN = 0, f_S = 1500MHz, FG calibration

Figure 5-126. SNR vs Clock Amplitude

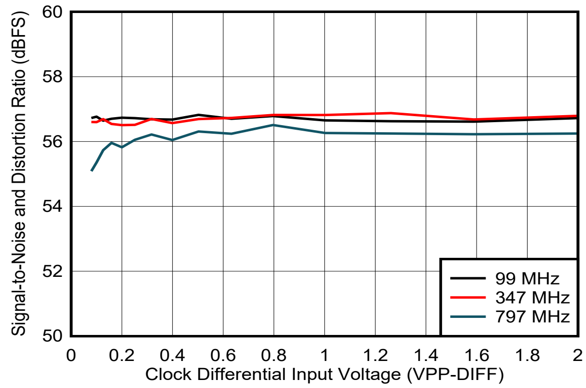


DES_EN = 1, f_S = 3000MHz, FG calibration

Figure 5-127. SNR vs Clock Amplitude

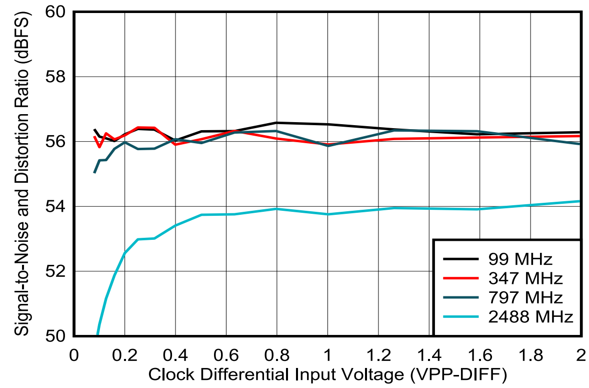
5.14 Typical Characteristics - ADC12DL1500 (1.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 1.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



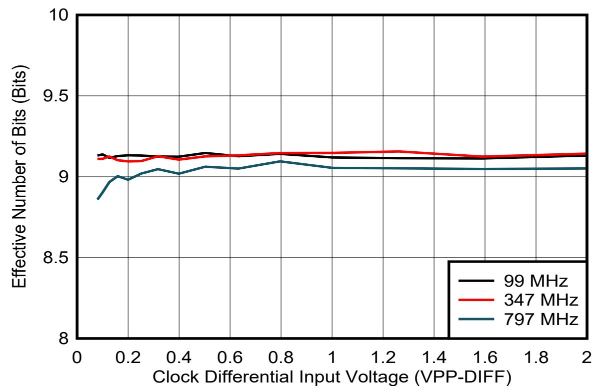
DES_EN = 0, f_S = 1500MHz, FG calibration

Figure 5-128. SINAD vs Clock Amplitude



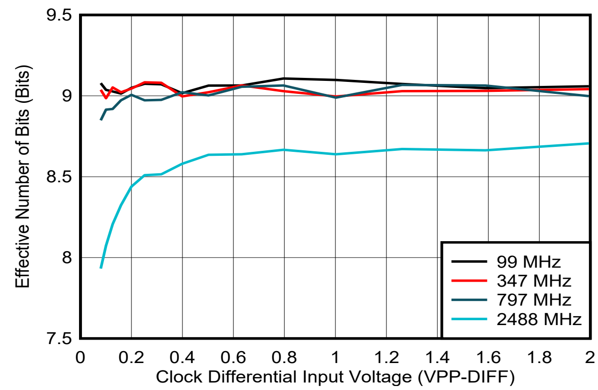
DES_EN = 1, f_S = 3000MHz, FG calibration

Figure 5-129. SINAD vs Clock Amplitude



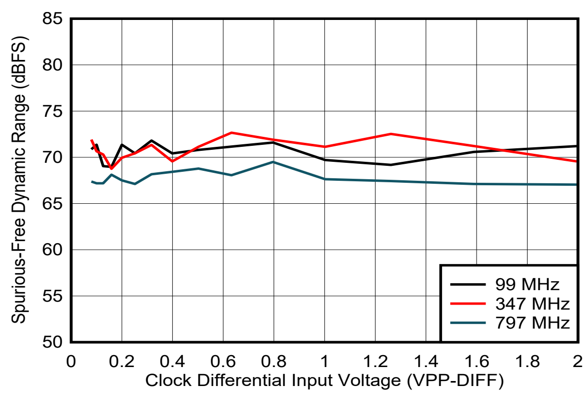
DES_EN = 0, f_S = 1500MHz, FG calibration

Figure 5-130. ENOB vs Clock Amplitude



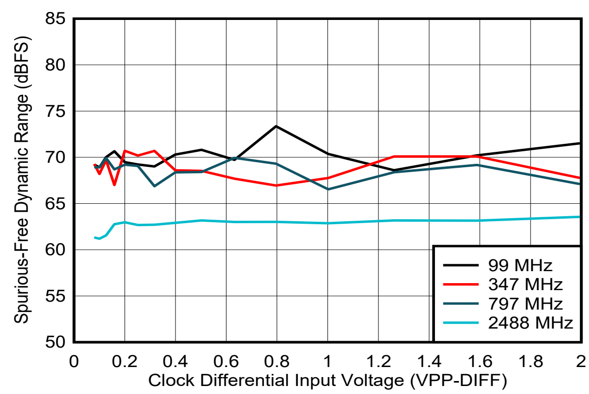
DES_EN = 1, f_S = 3000MHz, FG calibration

Figure 5-131. ENOB vs Clock Amplitude



DES_EN = 0, f_S = 1500MHz, FG calibration

Figure 5-132. SFDR vs Clock Amplitude

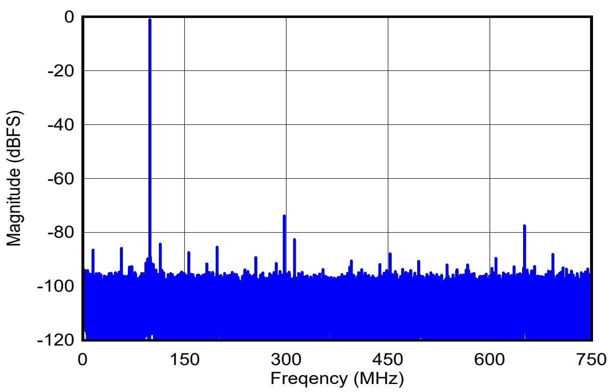


DES_EN = 1, f_S = 3000MHz, FG calibration

Figure 5-133. SFDR vs Clock Amplitude

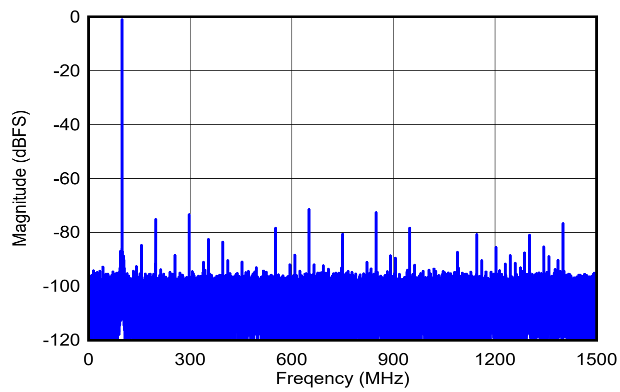
5.14 Typical Characteristics - ADC12DL1500 (1.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 1.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



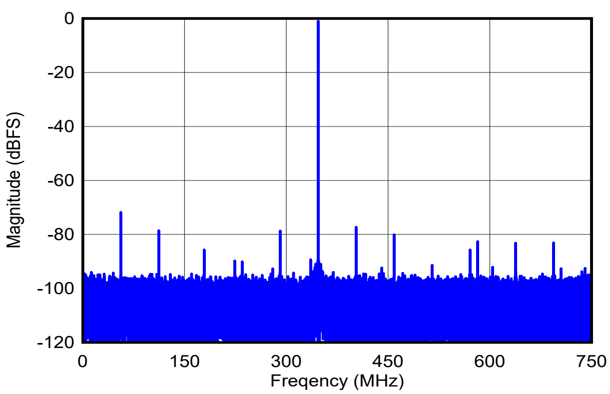
DES_EN = 0, f_S = 1500MHz, FG calibration, SNR = 57.5dBFS, SFDR = 73.8dBFS, ENOB = 9.2 bits

Figure 5-134. Single-Tone FFT at f_{IN} = 99MHz, AIN = –1dBFS



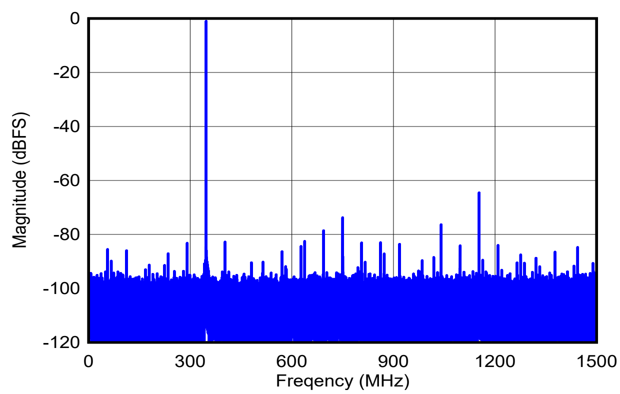
DES_EN = 1, f_S = 3000MHz, FG calibration, SNR = 57.4dBFS, SFDR = 71.3dBFS, ENOB = 9.0 bits

Figure 5-135. Single-Tone FFT at f_{IN} = 99MHz, AIN = –1dBFS



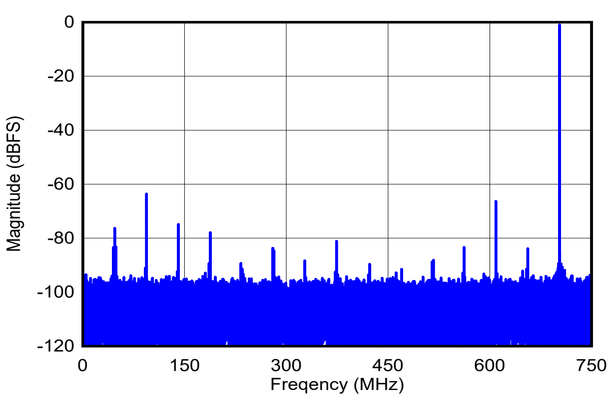
DES_EN = 0, f_S = 1500MHz, FG calibration, SNR = 57.6dBFS, SFDR = 71.7dBFS, ENOB = 9.2 bits

Figure 5-136. Single-Tone FFT at f_{IN} = 347MHz, AIN = –1dBFS



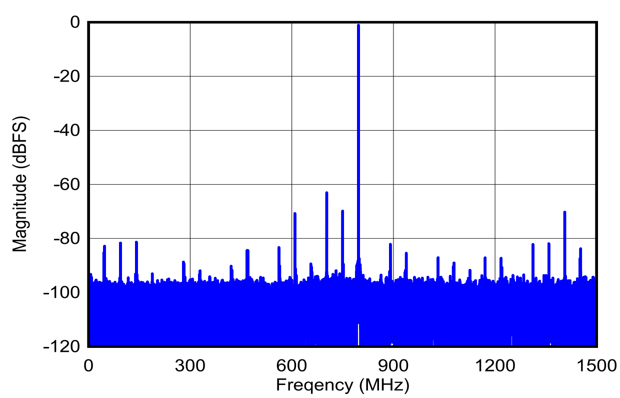
DES_EN = 1, f_S = 3000MHz, FG calibration, SNR = 57.6dBFS, SFDR = 64.2dBFS, ENOB = 9.1 bits

Figure 5-137. Single-Tone FFT at f_{IN} = 347MHz, AIN = –1dBFS



DES_EN = 0, f_S = 1500MHz, FG calibration, SNR = 57.2dBFS, SFDR = 63.5dBFS, ENOB = 8.9 bits

Figure 5-138. Single-Tone FFT at f_{IN} = 797MHz, AIN = –1dBFS

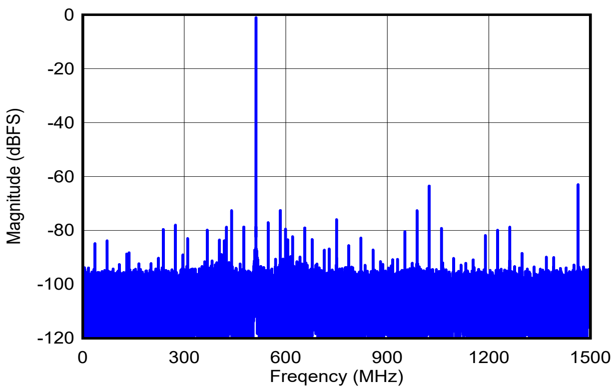


DES_EN = 1, f_S = 3000MHz, FG calibration, SNR = 57.3dBFS, SFDR = 62.8dBFS, ENOB = 8.9 bits

Figure 5-139. Single-Tone FFT at f_{IN} = 797MHz, AIN = –1dBFS

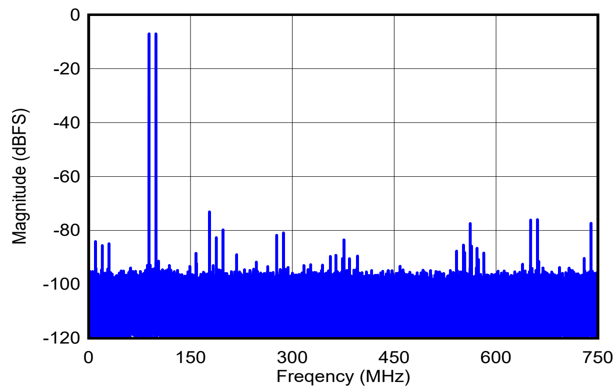
5.14 Typical Characteristics - ADC12DL1500 (1.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 1.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



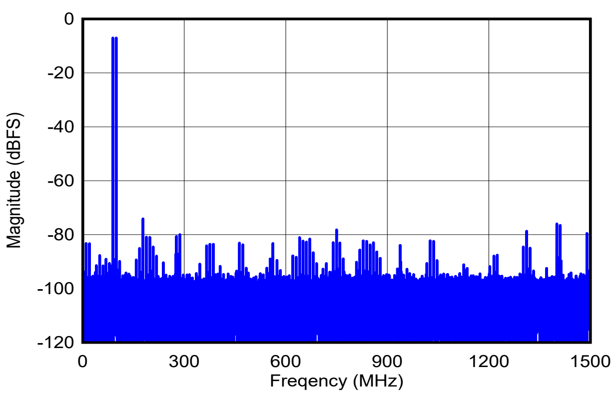
DES_EN = 1, f_S = 3000MHz, FG calibration, SNR = 56.2dBFS, SFDR = 62.8dBFS, ENOB = 8.7 bits

Figure 5-140. Single-Tone FFT at f_{IN} = 2488MHz, AIN = –1dBFS



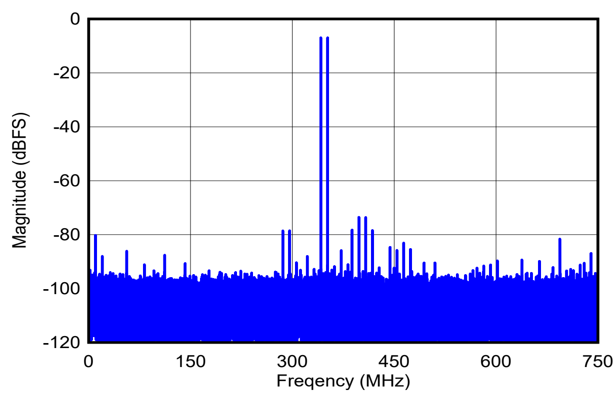
DES_EN = 0, f_S = 1500MHz, FG calibration, f_1 = 89MHz, f_2 = 99MHz, A_{IN} = -7dBFS per tone, SFDR = -73dBFS, IMD3 = -98dBFS, IMD2 = -83dBFS

Figure 5-141. Two-Tone FFT at f_{IN} = 94MHz, AIN = –1dBFS



DES_EN = 1, f_S = 3000MHz, FG calibration, f_1 = 89MHz, f_2 = 99MHz, A_{IN} = -7dBFS per tone, SFDR = -74dBFS, IMD3 = -90dBFS, IMD2 = -82dBFS

Figure 5-142. Two-Tone FFT at f_{IN} = 94MHz, AIN = –1dBFS

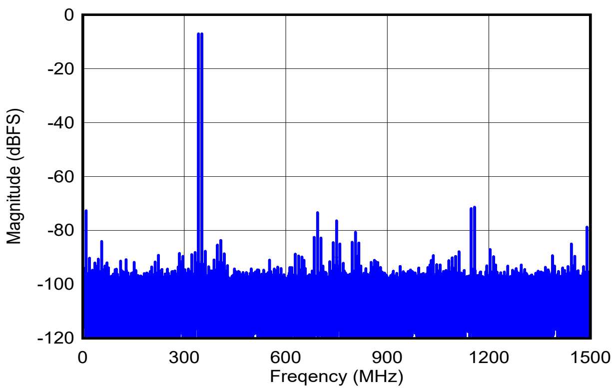


DES_EN = 0, f_S = 1500MHz, FG calibration, f_1 = 342MHz, f_2 = 352MHz, A_{IN} = -7dBFS per tone, SFDR = -74dBFS, IMD3 = -92dBFS, IMD2 = -81dBFS

Figure 5-143. Two-Tone FFT at f_{IN} = 347MHz, AIN = –1dBFS

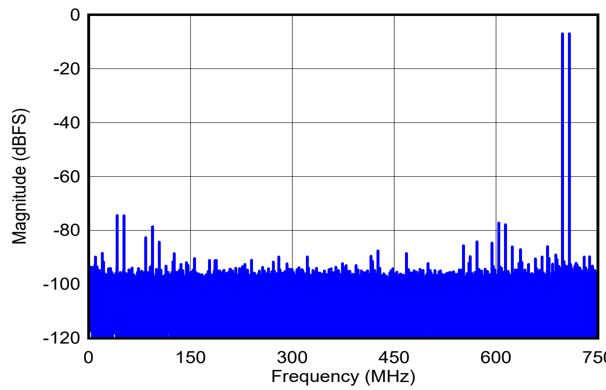
5.14 Typical Characteristics - ADC12DL1500 (1.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 1.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



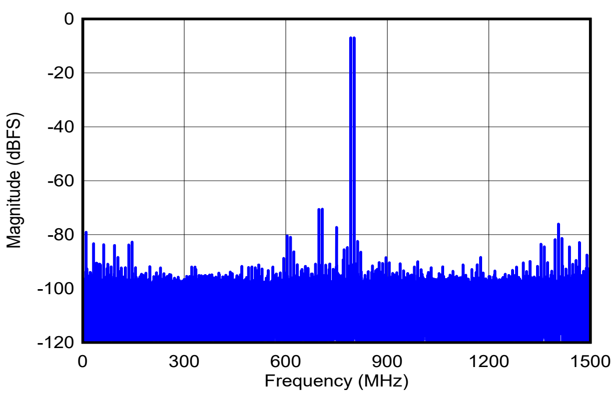
DES_EN = 1, f_S = 3000MHz, FG calibration, f_1 = 342MHz, f_2 = 352MHz, A_{IN} = -7dBFS per tone, SFDR = -71dBFS, IMD3 = -88dBFS, IMD2 = -73dBFS

Figure 5-144. Two-Tone FFT at f_{IN} = 347MHz, AIN = –1dBFS



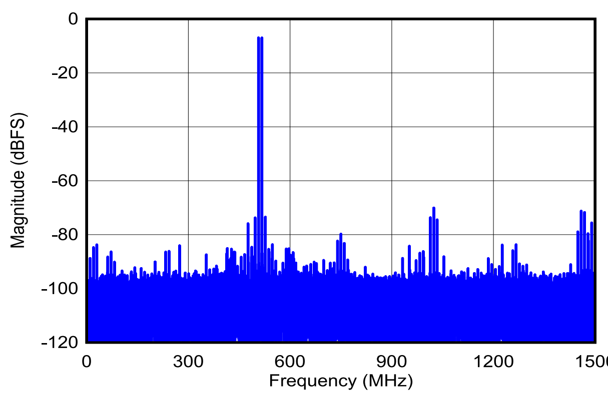
DES_EN = 0, f_S = 1500MHz, FG calibration, f_1 = 792MHz, f_2 = 802MHz, A_{IN} = -7dBFS per tone, SFDR = -74dBFS, IMD3 = -90dBFS, IMD2 = -82dBFS

Figure 5-145. Two-Tone FFT at f_{IN} = 797MHz, AIN = –1dBFS



DES_EN = 1, f_S = 3000MHz, FG calibration, f_1 = 792MHz, f_2 = 802MHz, A_{IN} = -7dBFS per tone, SFDR = -71dBFS, IMD3 = -84dBFS, IMD2 = -77dBFS

Figure 5-146. Two-Tone FFT at f_{IN} = 797MHz, AIN = –1dBFS

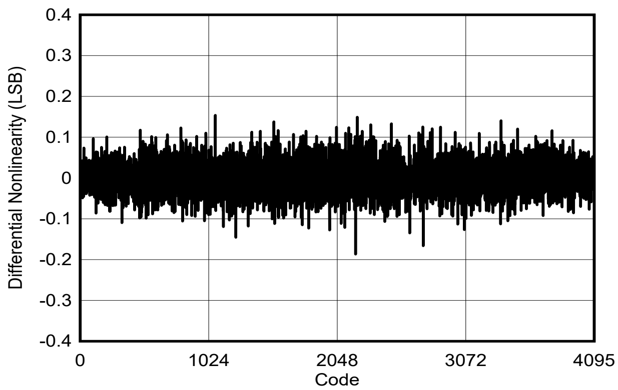


DES_EN = 1, f_S = 3000MHz, FG calibration, f_1 = 2483MHz, f_2 = 2493MHz, A_{IN} = -7dBFS per tone, SFDR = -70dBFS, IMD3 = -74dBFS, IMD2 = -75dBFS

Figure 5-147. Two-Tone FFT at f_{IN} = 2488MHz, AIN = –1dBFS

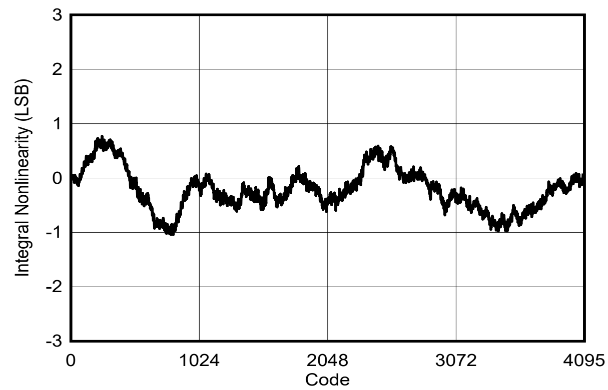
5.14 Typical Characteristics - ADC12DL1500 (1.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 1.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



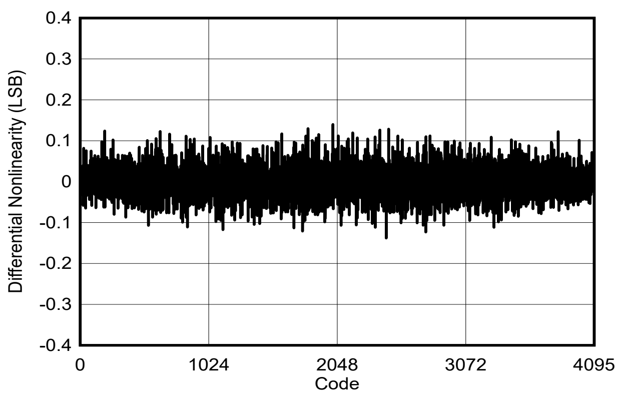
DES_EN = 0, f_S = 1500MHz, FG calibration, F_{IN} = 99MHz

Figure 5-148. DNL vs Code



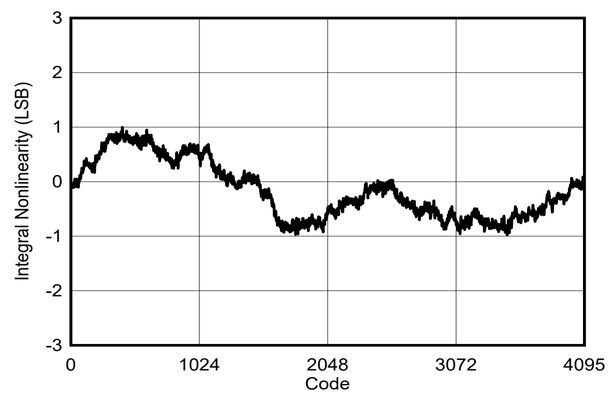
DES_EN = 0, f_S = 1500MHz, FG calibration, F_{IN} = 99MHz

Figure 5-149. INL vs Code



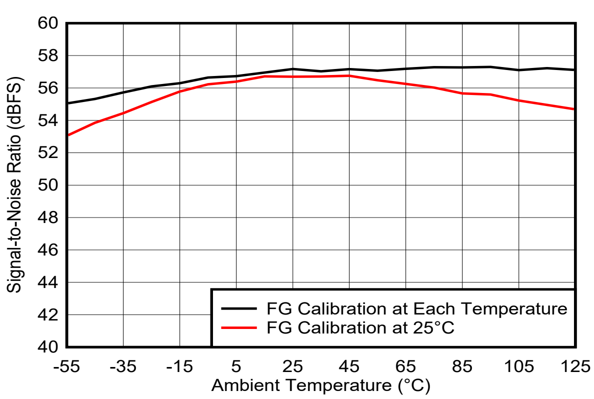
DES_EN = 1, f_S = 3000MHz, FG calibration, F_{IN} = 99MHz

Figure 5-150. DNL vs Code



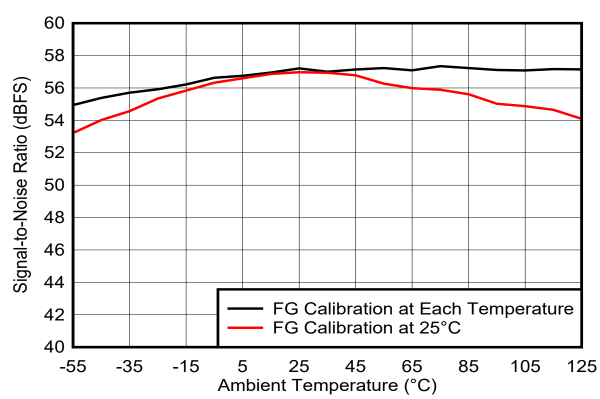
DES_EN = 1, f_S = 3000MHz, FG calibration, F_{IN} = 99MHz

Figure 5-151. INL vs Code



DES_EN = 0, f_S = 1500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-152. SNR vs Temperature and Calibration Mode

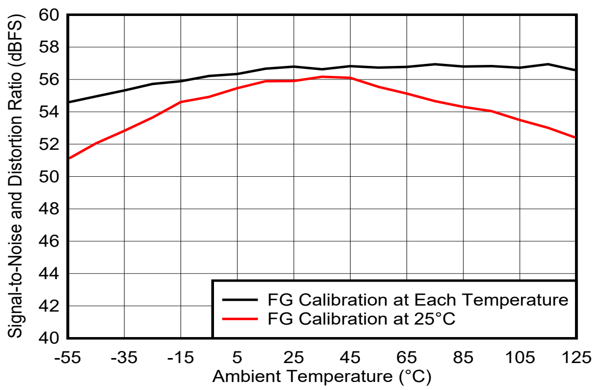


DES_EN = 1, f_S = 3000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-153. SNR vs Temperature and Calibration Mode

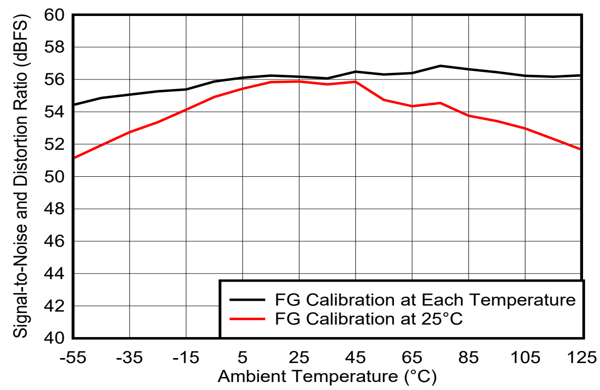
5.14 Typical Characteristics - ADC12DL1500 (1.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 1.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



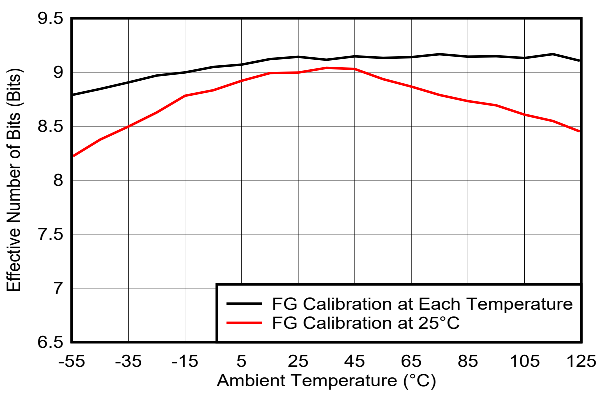
DES_EN = 0, f_S = 1500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-154. SINAD vs Temperature and Calibration Mode



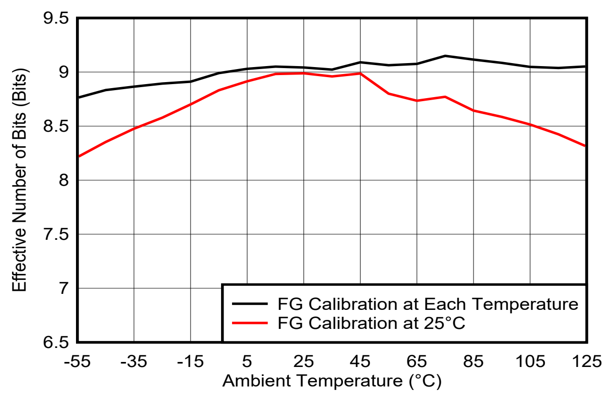
DES_EN = 1, f_S = 3000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-155. SINAD vs Temperature and Calibration Mode



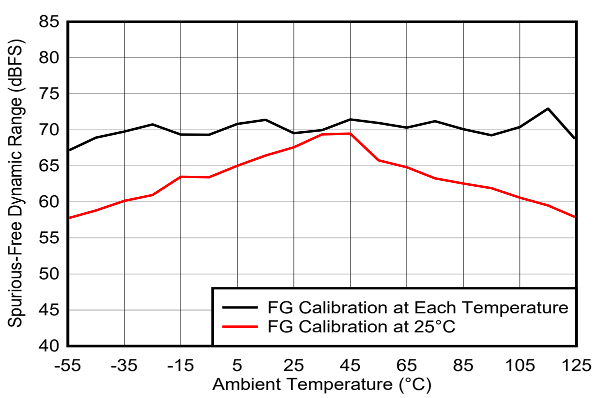
DES_EN = 0, f_S = 1500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-156. ENOB vs Temperature and Calibration Mode



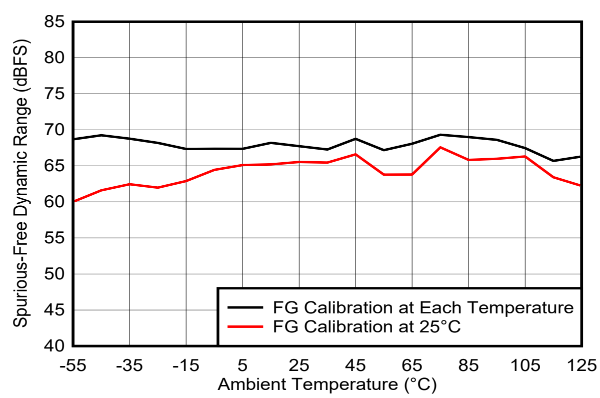
DES_EN = 1, f_S = 3000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-157. ENOB vs Temperature and Calibration Mode



DES_EN = 0, f_S = 1500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-158. SFDR vs Temperature and Calibration Mode

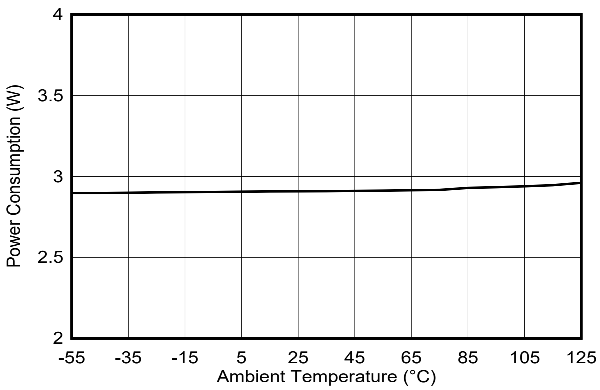


DES_EN = 1, f_S = 3000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-159. SFDR vs Temperature and Calibration Mode

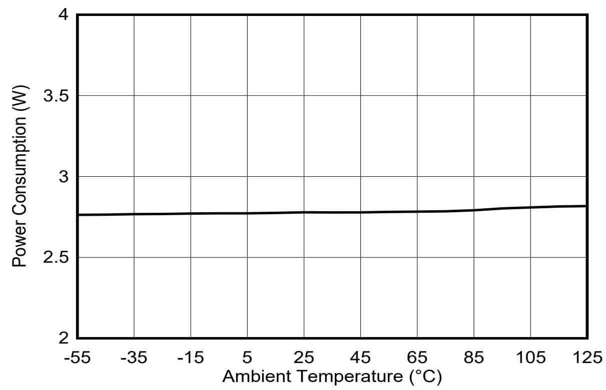
5.14 Typical Characteristics - ADC12DL1500 (1.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 1.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



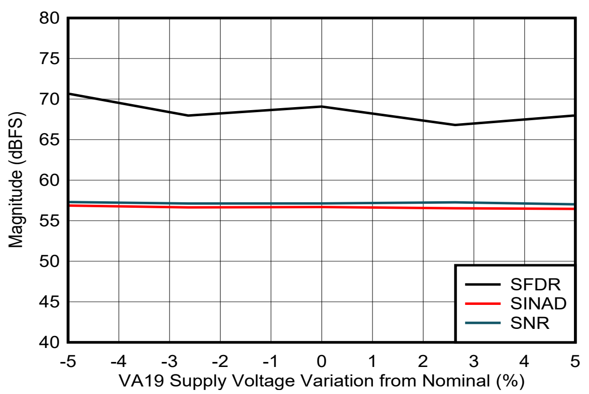
DES_EN = 0, f_S = 1500MHz, F_{IN} = 99MHz, A_{IN} = -1dBFS

Figure 5-160. Power Consumption vs Temperature



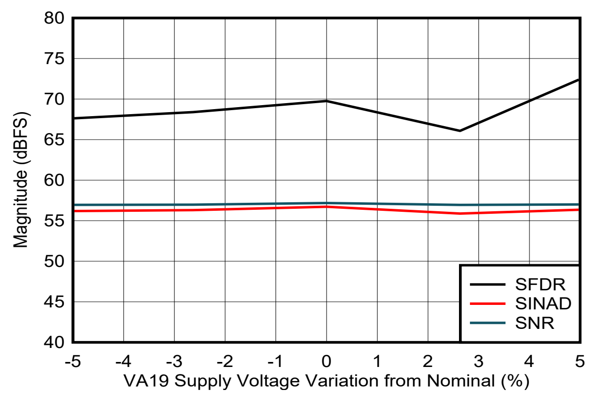
DES_EN = 1, f_S = 3000MHz, F_{IN} = 99MHz, A_{IN} = -1dBFS

Figure 5-161. Power Consumption vs Temperature



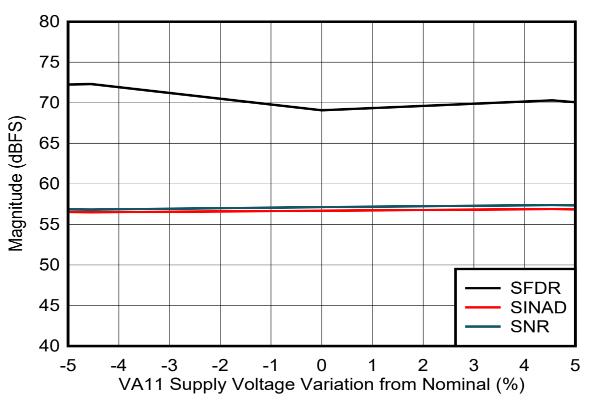
DES_EN = 0, f_S = 1500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-162. Performance vs VA19 Supply Voltage



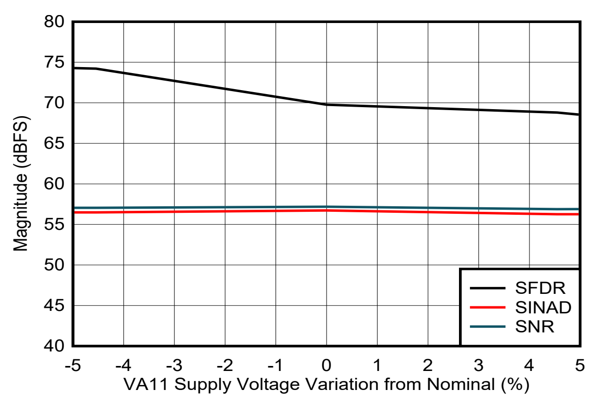
DES_EN = 1, f_S = 3000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-163. Performance vs VA19 Supply Voltage



DES_EN = 0, f_S = 1500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-164. Performance vs VA11 Supply Voltage

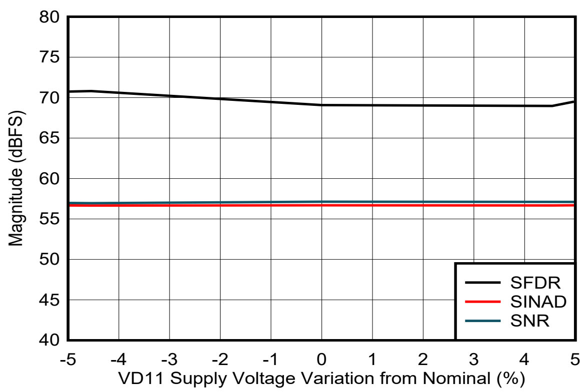


DES_EN = 1, f_S = 3000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-165. Performance vs VA11 Supply Voltage

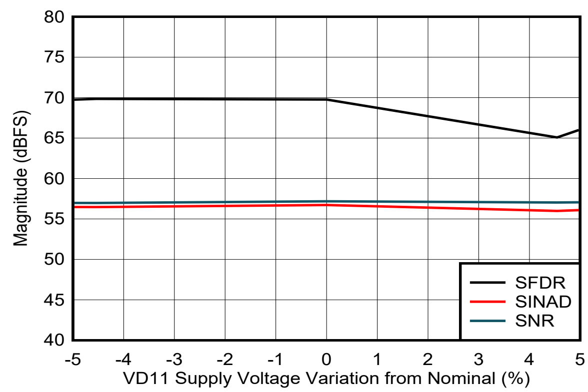
5.14 Typical Characteristics - ADC12DL1500 (1.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 1.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



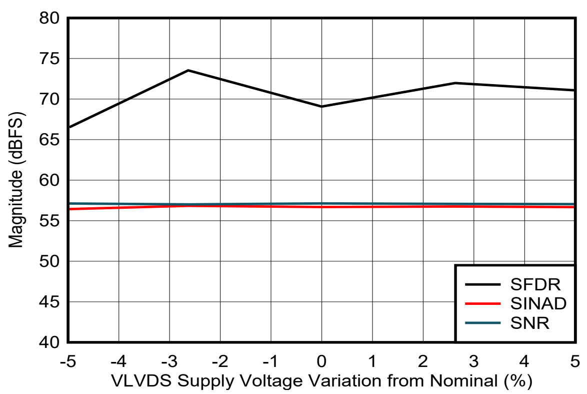
DES_EN = 0, f_S = 1500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-166. Performance vs VD11 Supply Voltage



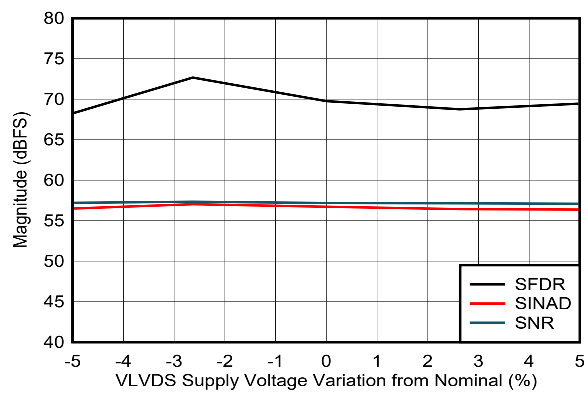
DES_EN = 1, f_S = 3000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-167. Performance vs VD11 Supply Voltage



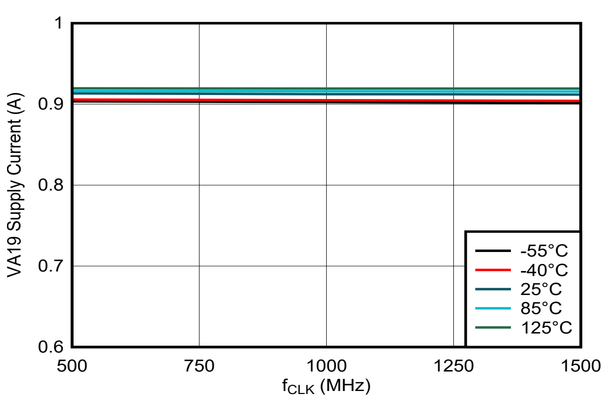
DES_EN = 0, f_S = 1500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-168. Performance vs VLVDS Supply Voltage



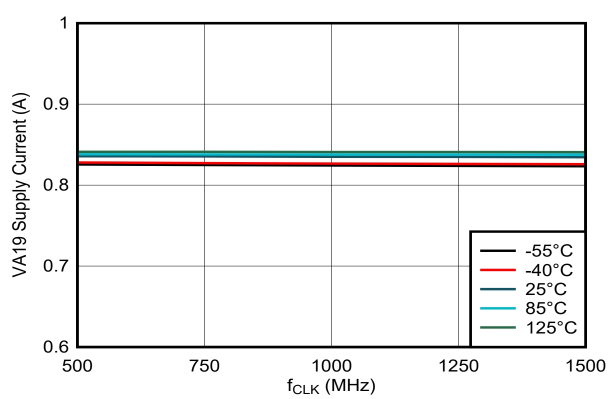
DES_EN = 1, f_S = 3000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-169. Performance vs VLVDS Supply Voltage



DES_EN = 0, f_S = 1500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-170. VA19 Supply Current vs Clock Rate

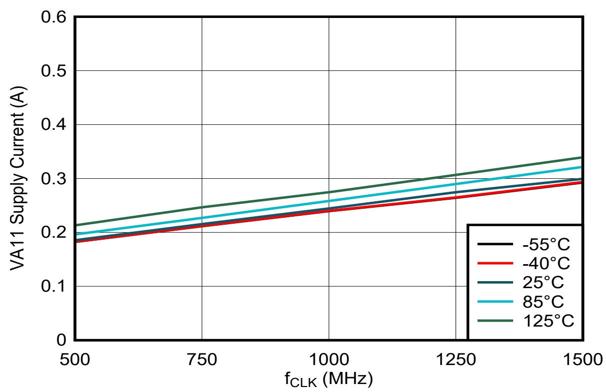


DES_EN = 1, f_S = 3000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-171. VA19 Supply Current vs Clock Rate

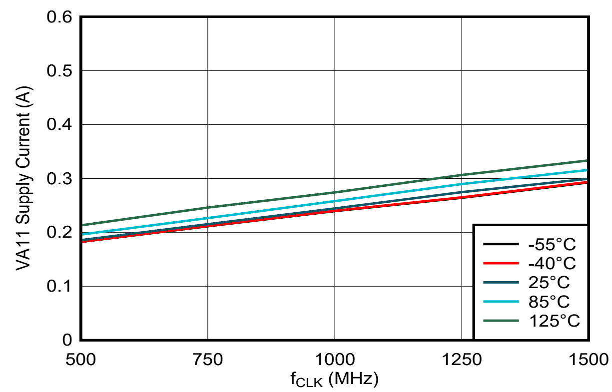
5.14 Typical Characteristics - ADC12DL1500 (1.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 1.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



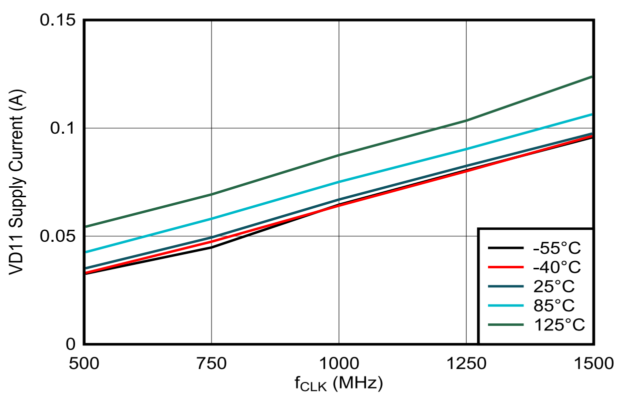
DES_EN = 0, f_S = 1500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-172. VA11 Supply Current vs Clock Rate



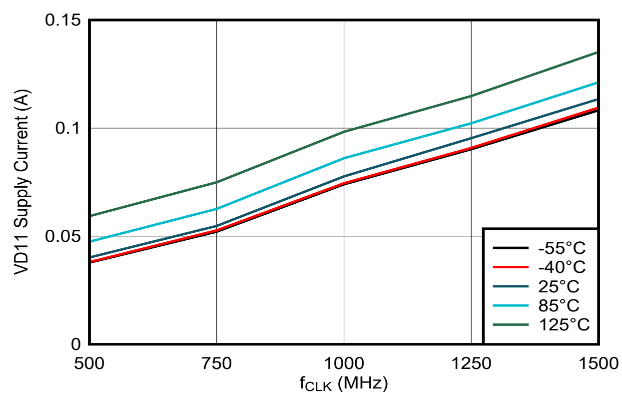
DES_EN = 1, f_S = 3000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-173. VA11 Supply Current vs Clock Rate



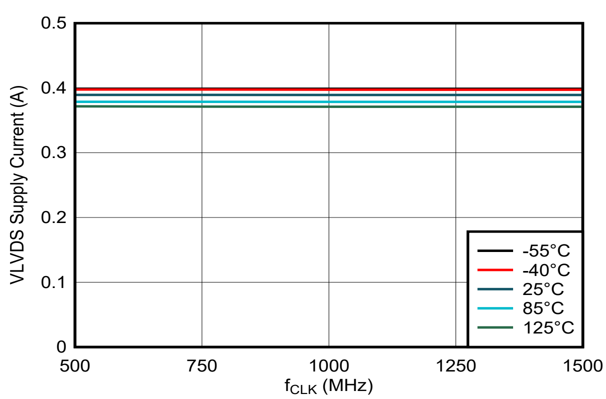
DES_EN = 0, f_S = 1500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-174. VD11 Supply Current vs Clock Rate



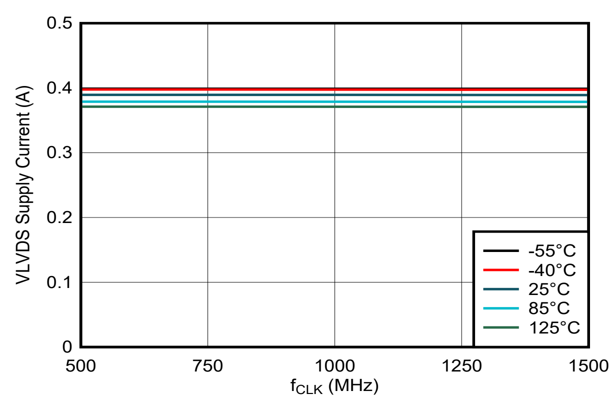
DES_EN = 1, f_S = 3000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-175. VD11 Supply Current vs Clock Rate



DES_EN = 0, f_S = 1500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-176. VLVDS Supply Current vs Clock Rate

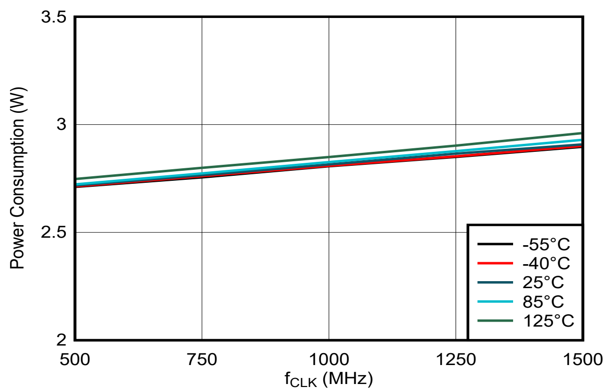


DES_EN = 1, f_S = 3000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-177. VLVDS Supply Current vs Clock Rate

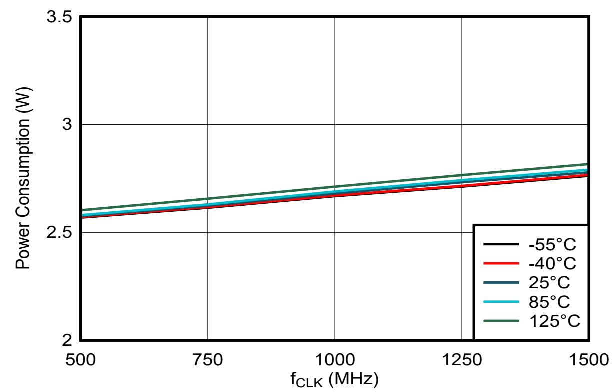
5.14 Typical Characteristics - ADC12DL1500 (1.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 1.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



DES_EN = 0, f_S = 1500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-178. Power Consumption vs Clock Rate

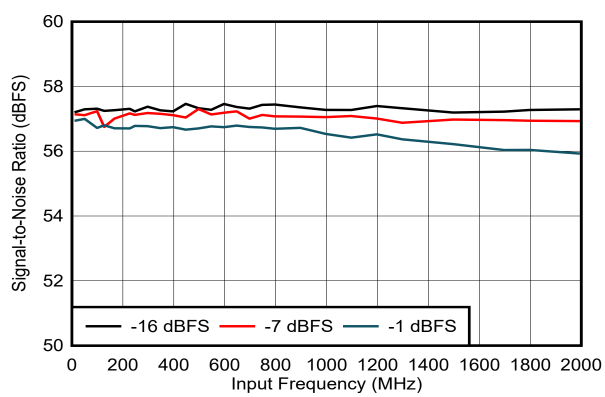


DES_EN = 1, f_S = 3000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-179. Power Consumption vs Clock Rate

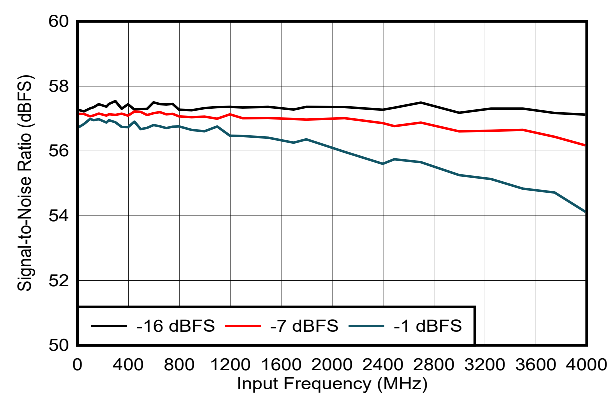
5.15 Typical Characteristics - ADC12DL2500 (2GSPS)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 2GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



DES_EN = 0, f_S = 2000MHz, FG calibration

Figure 5-180. SNR vs Input Frequency

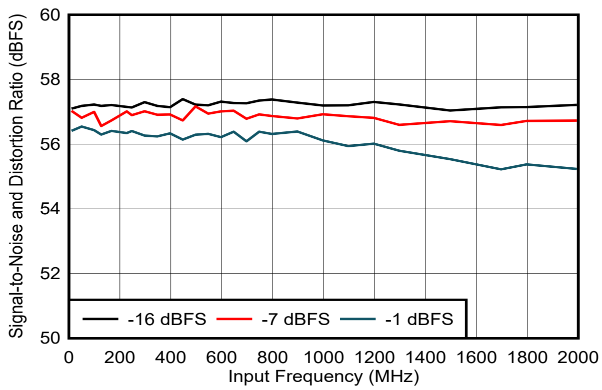


DES_EN = 1, f_S = 4000MHz, FG calibration

Figure 5-181. SNR vs Input Frequency

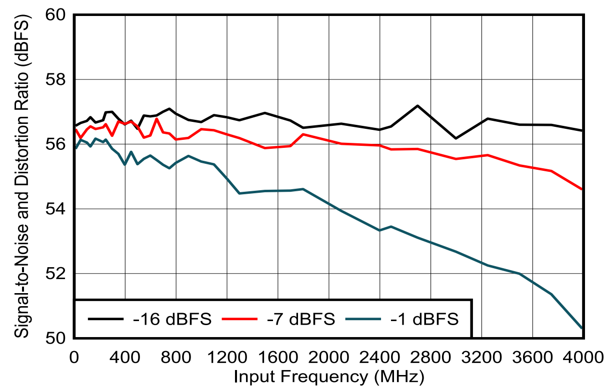
5.15 Typical Characteristics - ADC12DL2500 (2GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 2GHz, filtered 1V_{PP} sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



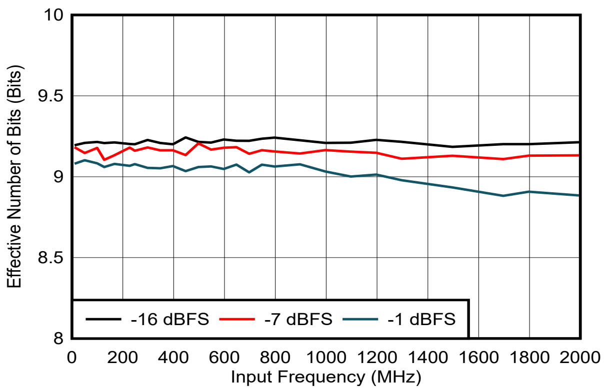
DES_EN = 0, f_S = 2000MHz, FG calibration

Figure 5-182. SINAD vs Input Frequency



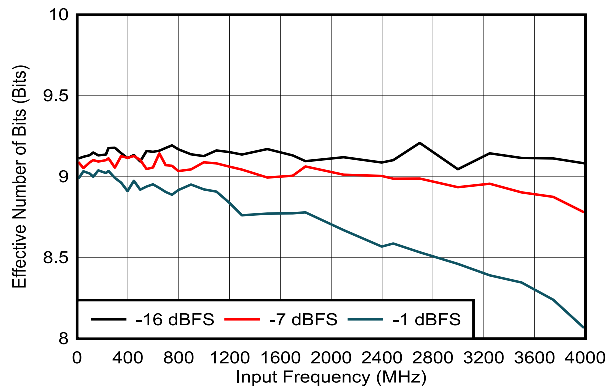
DES_EN = 1, f_S = 4000MHz, FG calibration

Figure 5-183. SINAD vs Input Frequency



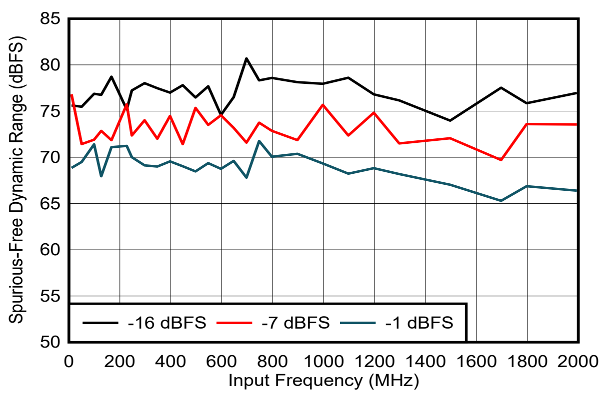
DES_EN = 0, f_S = 2000MHz, FG calibration

Figure 5-184. ENOB vs Input Frequency



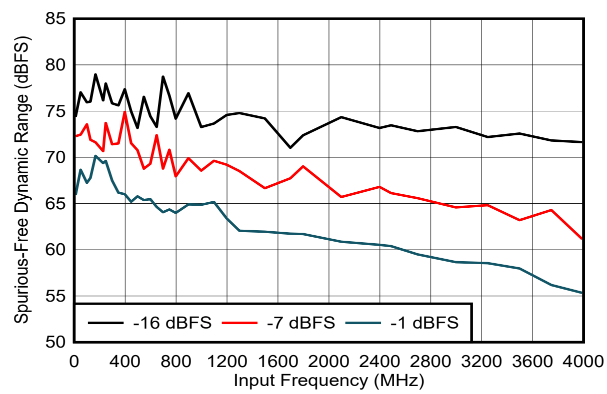
DES_EN = 1, f_S = 4000MHz, FG calibration

Figure 5-185. ENOB vs Input Frequency



DES_EN = 0, f_S = 2000MHz, FG calibration

Figure 5-186. SFDR vs Input Frequency

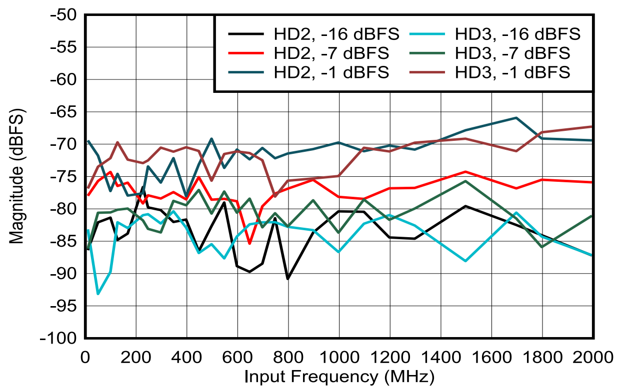


DES_EN = 1, f_S = 4000MHz, FG calibration

Figure 5-187. SFDR vs Input Frequency

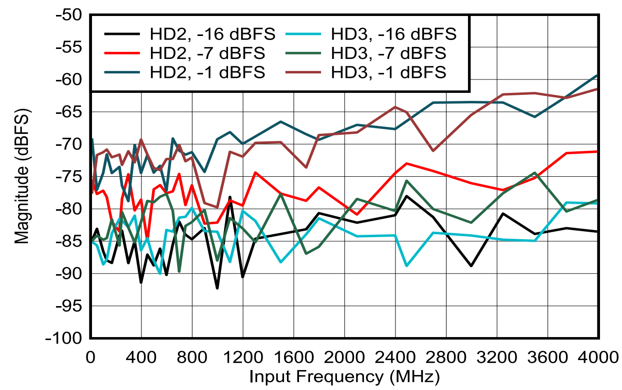
5.15 Typical Characteristics - ADC12DL2500 (2GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 2GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



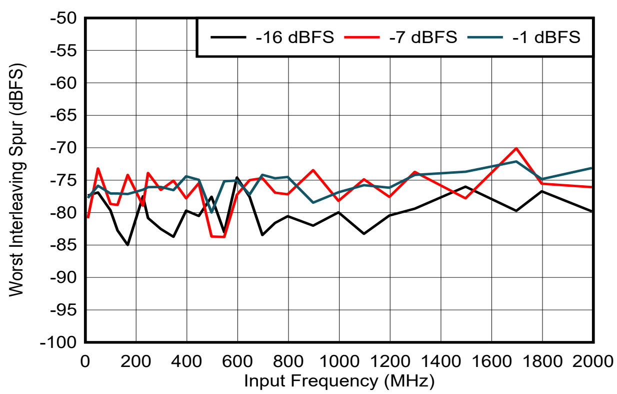
DES_EN = 0, f_S = 2000MHz, FG calibration

Figure 5-188. HD2 and HD3 vs Input Frequency



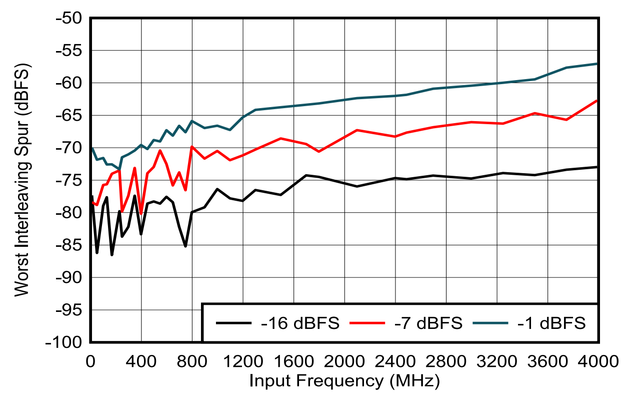
DES_EN = 1, f_S = 4000MHz, FG calibration

Figure 5-189. HD2 and HD3 vs Input Frequency



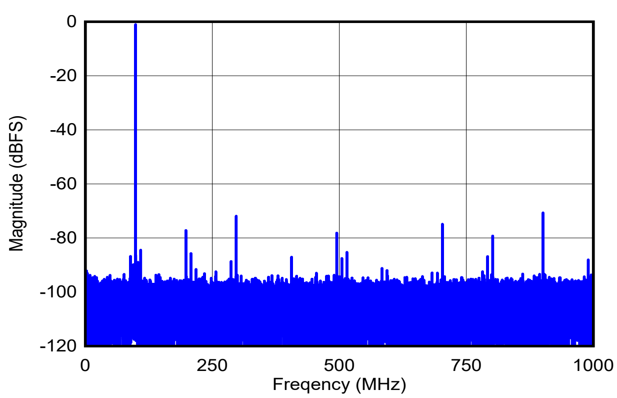
DES_EN = 0, f_S = 2000MHz, FG calibration, includes f_S / 2 – f_{IN} spur only

Figure 5-190. Worst Interleaving Spur vs Input Frequency



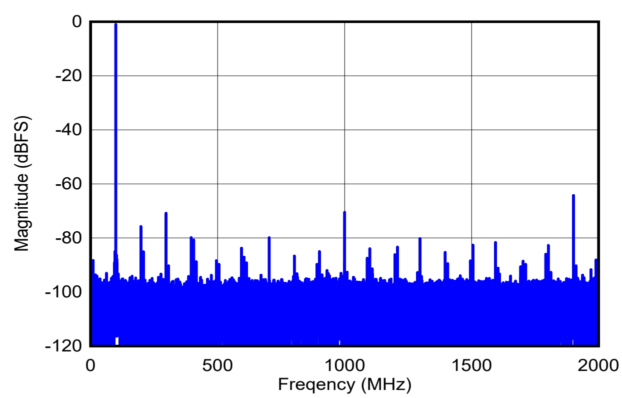
DES_EN = 1, f_S = 4000MHz, FG calibration, includes f_S / 2 – f_{IN} and f_S /4 ± f_{IN} spurs only

Figure 5-191. Worst Interleaving Spur vs Input Frequency



DES_EN = 0, f_S = 2000MHz, FG calibration, SNR = 57.3dBFS, SFDR = 70.6dBFS, ENOB = 9.1 bits

Figure 5-192. Single-Tone FFT at f_{IN} = 99MHz, AIN = –1dBFS

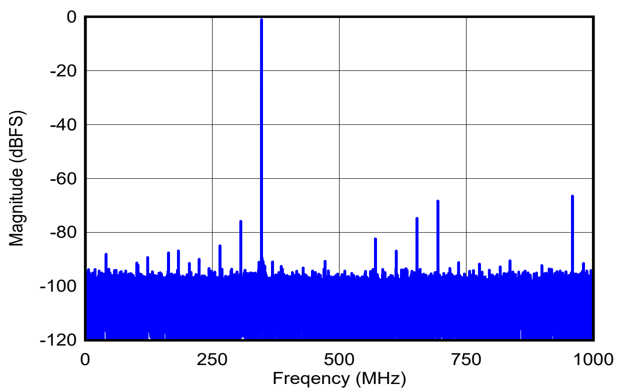


DES_EN = 1, f_S = 4000MHz, FG calibration, SNR = 57.3dBFS, SFDR = 64.4dBFS, ENOB = 9.0 bits

Figure 5-193. Single-Tone FFT at f_{IN} = 99MHz, AIN = –1dBFS

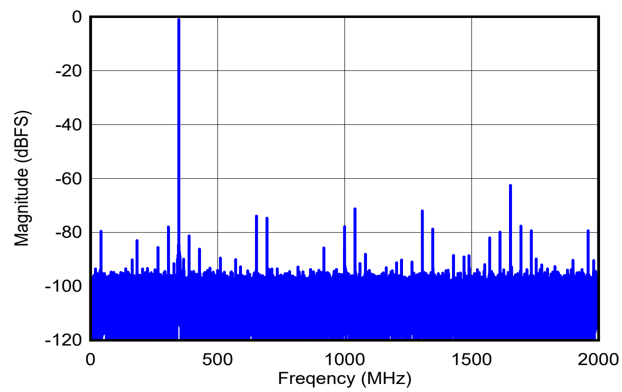
5.15 Typical Characteristics - ADC12DL2500 (2GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 2GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



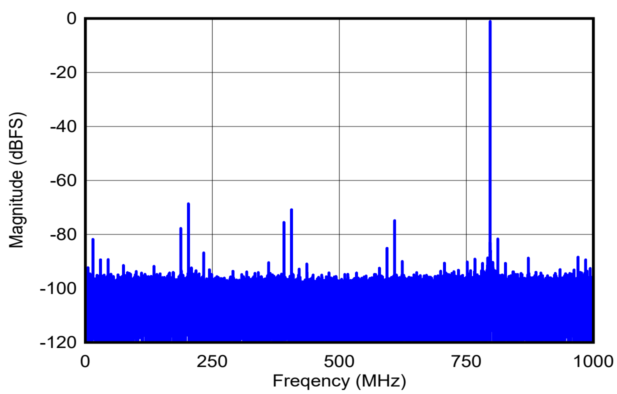
DES_EN = 0, f_S = 2000MHz, FG calibration, SNR = 57.3dBFS, SFDR = 66.4dBFS, ENOB = 9.0 bits

Figure 5-194. Single-Tone FFT at f_{IN} = 347MHz, AIN = –1dBFS



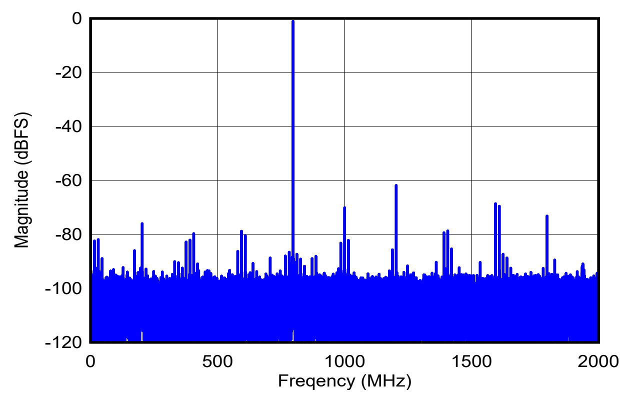
DES_EN = 1, f_S = 4000MHz, FG calibration, SNR = 56.9dBFS, SFDR = 62.7dBFS, ENOB = 8.9 bits

Figure 5-195. Single-Tone FFT at f_{IN} = 347MHz, AIN = –1dBFS



DES_EN = 0, f_S = 2000MHz, FG calibration, SNR = 57.0dBFS, SFDR = 68.5dBFS, ENOB = 9.1 bits

Figure 5-196. Single-Tone FFT at f_{IN} = 797MHz, AIN = –1dBFS

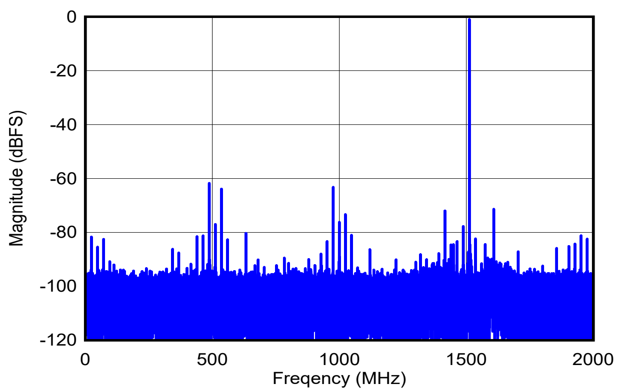


DES_EN = 1, f_S = 4000MHz, FG calibration, SNR = 57.1dBFS, SFDR = 61.7dBFS, ENOB = 8.8 bits

Figure 5-197. Single-Tone FFT at f_{IN} = 797MHz, AIN = –1dBFS

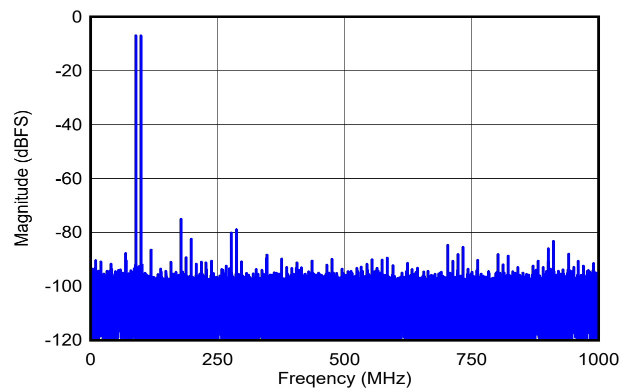
5.15 Typical Characteristics - ADC12DL2500 (2GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 2GHz, filtered 1V_{PP} sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



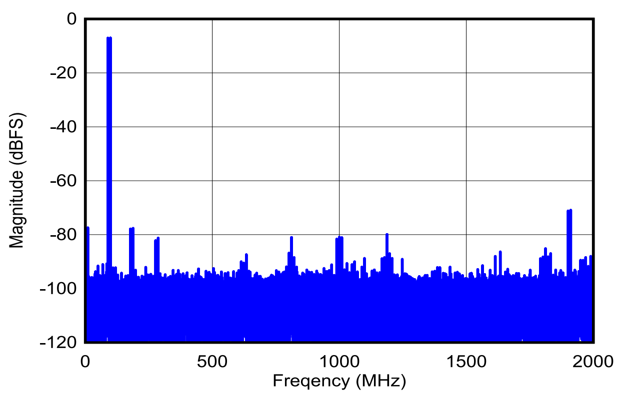
DES_EN = 1, f_S = 4000MHz, FG calibration, SNR = 56.2dBFS, SFDR = 61.8dBFS, ENOB = 8.6 bits

Figure 5-198. Single-Tone FFT at f_{IN} = 2488MHz, AIN = –1dBFS



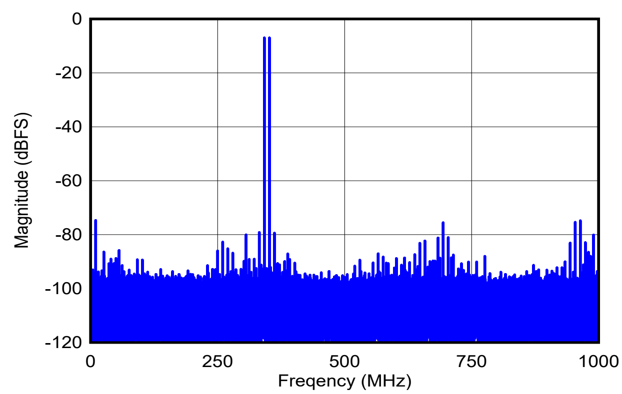
DES_EN = 0, f_S = 2000MHz, FG calibration, f_1 = 89MHz, f_2 = 99MHz, A_{IN} = -7dBFS per tone, SFDR = -75dBFS, IMD3 = -95dBFS, IMD2 = -90dBFS

Figure 5-199. Two-Tone FFT at f_{IN} = 94MHz, AIN = –1dBFS



DES_EN = 1, f_S = 4000MHz, FG calibration, f_1 = 89MHz, f_2 = 99MHz, A_{IN} = -7dBFS per tone, SFDR = -71dBFS, IMD3 = -94dBFS, IMD2 = -77dBFS

Figure 5-200. Two-Tone FFT at f_{IN} = 94MHz, AIN = –1dBFS

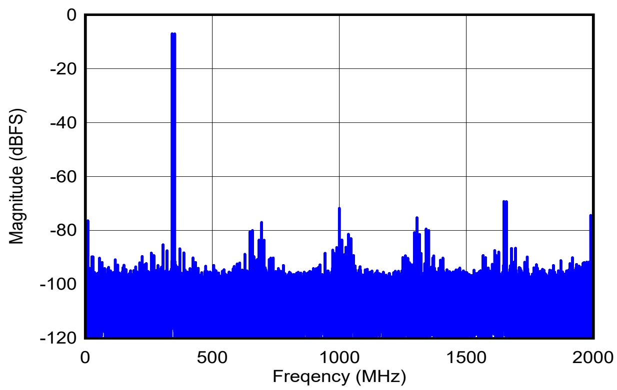


DES_EN = 0, f_S = 2000MHz, FG calibration, f_1 = 342MHz, f_2 = 352MHz, A_{IN} = -7dBFS per tone, SFDR = -75dBFS, IMD3 = -79dBFS, IMD2 = -75dBFS

Figure 5-201. Two-Tone FFT at f_{IN} = 347MHz, AIN = –1dBFS

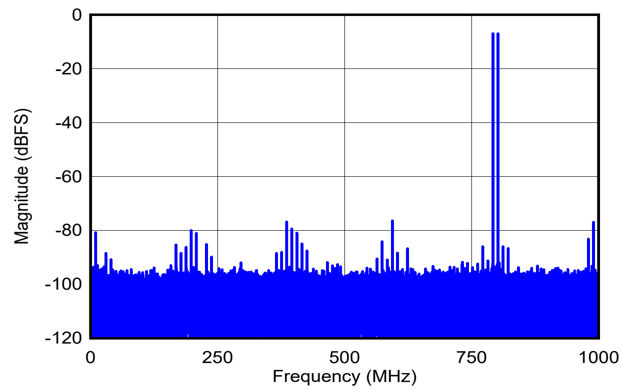
5.15 Typical Characteristics - ADC12DL2500 (2GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 2GHz, filtered 1V_{PP} sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



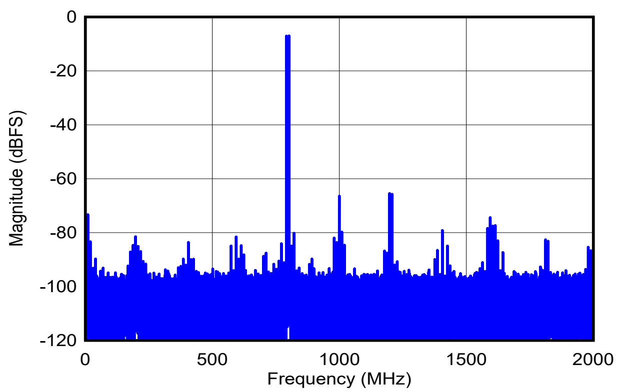
DES_EN = 1, f_S = 4000MHz, FG calibration, f_1 = 342MHz, f_2 = 352MHz, A_{IN} = -7dBFS per tone, SFDR = -69dBFS, IMD3 = -95dBFS, IMD2 = -77dBFS

Figure 5-202. Two-Tone FFT at f_{IN} = 347MHz, AIN = –1dBFS



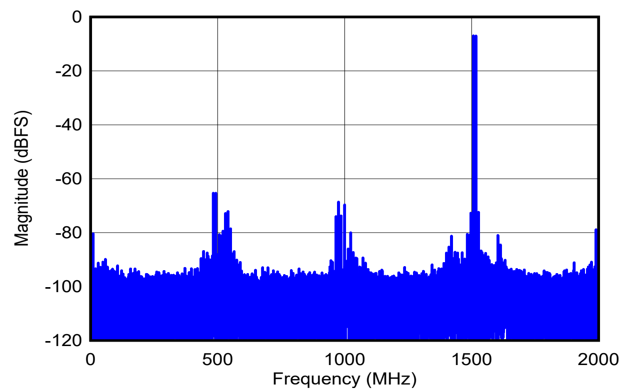
DES_EN = 0, f_S = 2000MHz, FG calibration, f_1 = 792MHz, f_2 = 802MHz, A_{IN} = -7dBFS per tone, SFDR = -76dBFS, IMD3 = -88dBFS, IMD2 = -81dBFS

Figure 5-203. Two-Tone FFT at f_{IN} = 797MHz, AIN = –1dBFS



DES_EN = 1, f_S = 4000MHz, FG calibration, f_1 = 792MHz, f_2 = 802MHz, A_{IN} = -7dBFS per tone, SFDR = -65dBFS, IMD3 = -87dBFS, IMD2 = -74dBFS

Figure 5-204. Two-Tone FFT at f_{IN} = 797MHz, AIN = –1dBFS

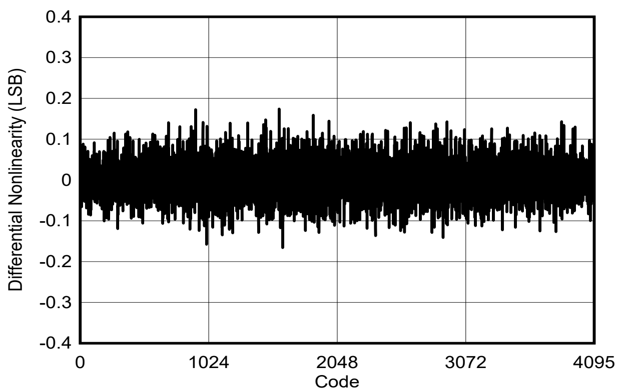


DES_EN = 1, f_S = 4000MHz, FG calibration, f_1 = 2483MHz, f_2 = 2493MHz, A_{IN} = -7dBFS per tone, SFDR = -65dBFS, IMD3 = -73dBFS, IMD2 = -73dBFS

Figure 5-205. Two-Tone FFT at f_{IN} = 2488MHz, AIN = –1dBFS

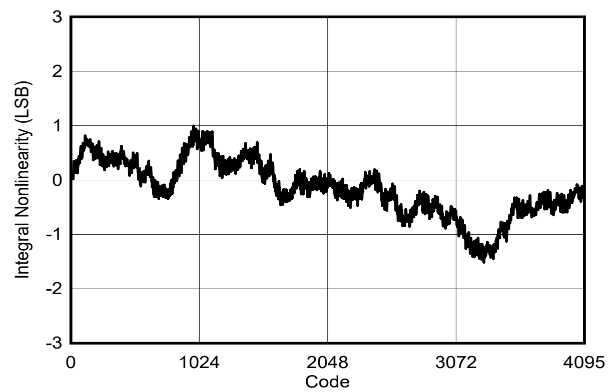
5.15 Typical Characteristics - ADC12DL2500 (2GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 2GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



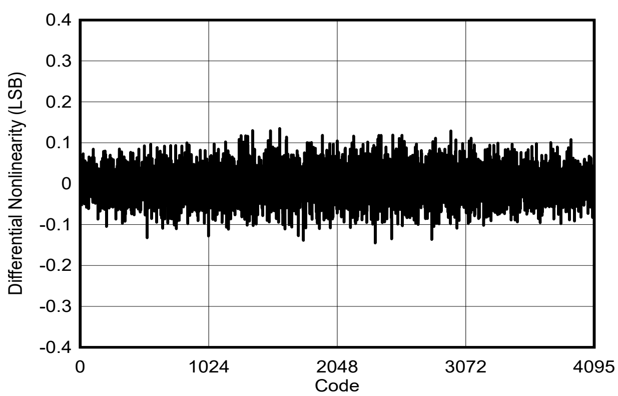
DES_EN = 0, f_S = 2000MHz, FG calibration, F_{IN} = 99MHz

Figure 5-206. DNL vs Code



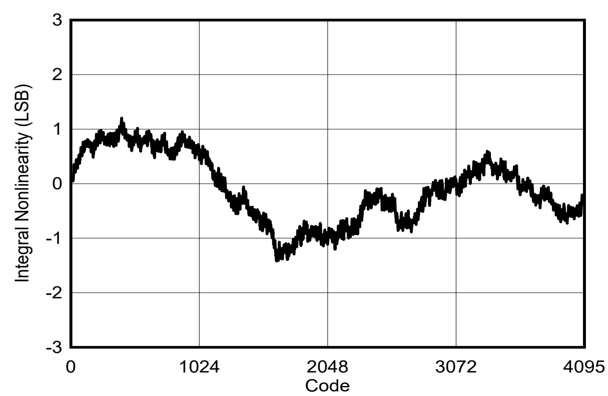
DES_EN = 0, f_S = 2000MHz, FG calibration, F_{IN} = 99MHz

Figure 5-207. INL vs Code



DES_EN = 1, f_S = 4000MHz, FG calibration, F_{IN} = 99MHz

Figure 5-208. DNL vs Code

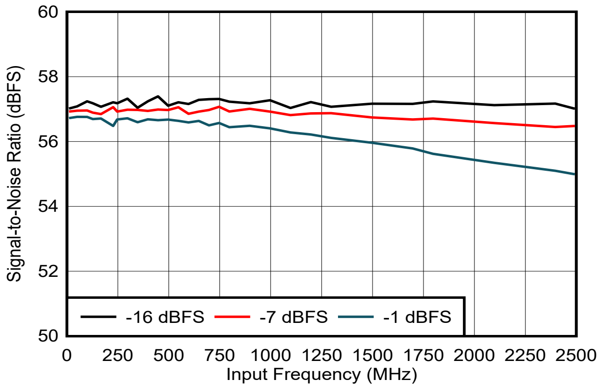


DES_EN = 1, f_S = 4000MHz, FG calibration, F_{IN} = 99MHz

Figure 5-209. INL vs Code

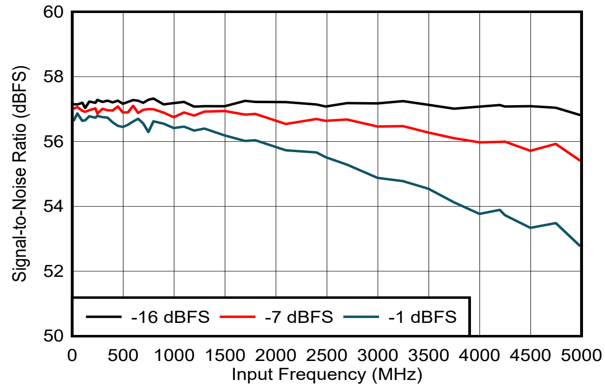
5.16 Typical Characteristics - ADC12DL2500 (2.5GSPS)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 2.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



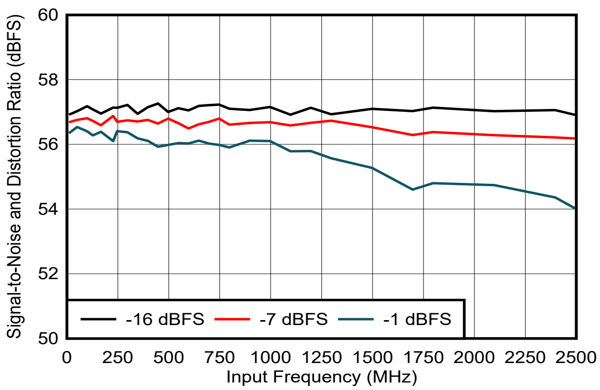
DES_EN = 0, f_S = 2500MHz, FG calibration

Figure 5-210. SNR vs Input Frequency



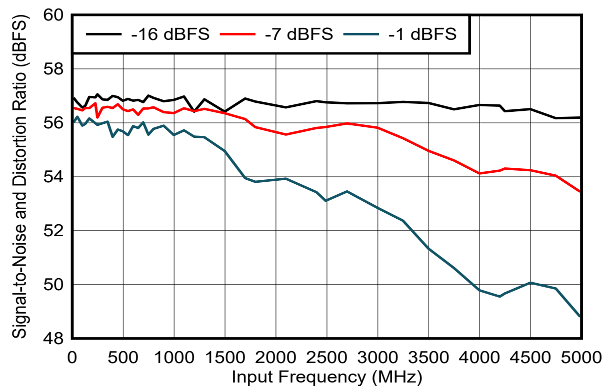
DES_EN = 1, f_S = 5000MHz, FG calibration

Figure 5-211. SNR vs Input Frequency



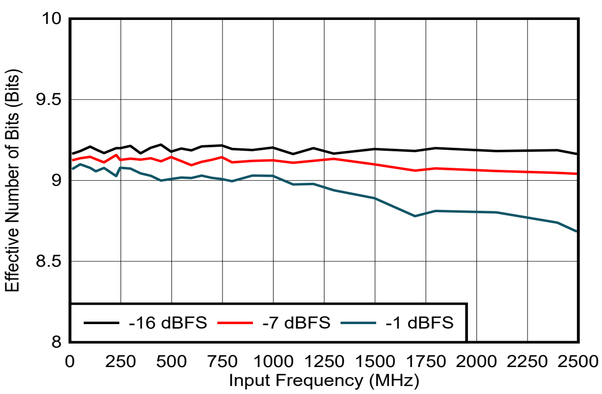
DES_EN = 0, f_S = 2500MHz, FG calibration

Figure 5-212. SINAD vs Input Frequency



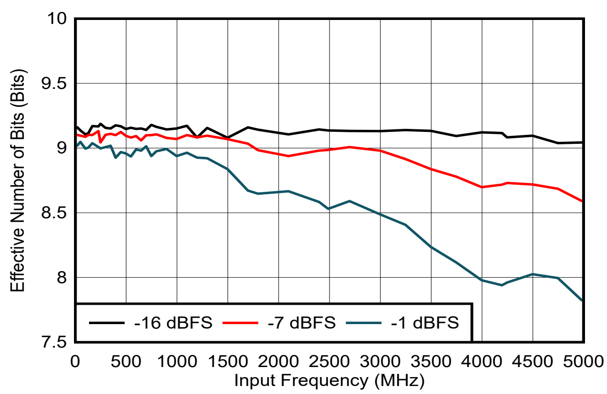
DES_EN = 1, f_S = 5000MHz, FG calibration

Figure 5-213. SINAD vs Input Frequency



DES_EN = 0, f_S = 2500MHz, FG calibration

Figure 5-214. ENOB vs Input Frequency

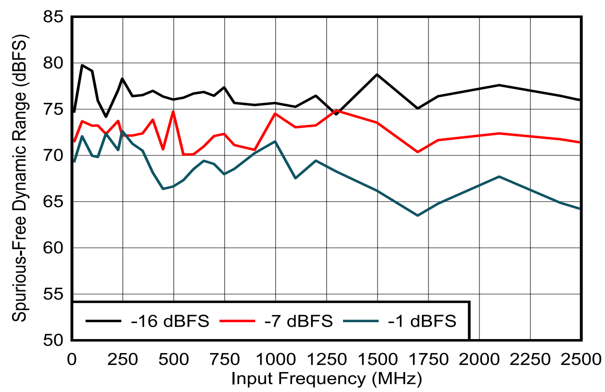


DES_EN = 1, f_S = 5000MHz, FG calibration

Figure 5-215. ENOB vs Input Frequency

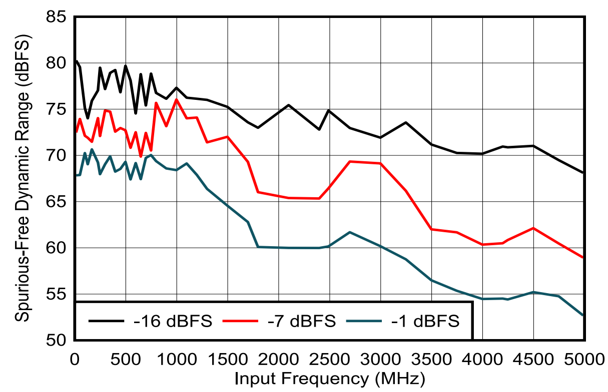
5.16 Typical Characteristics - ADC12DL2500 (2.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 2.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



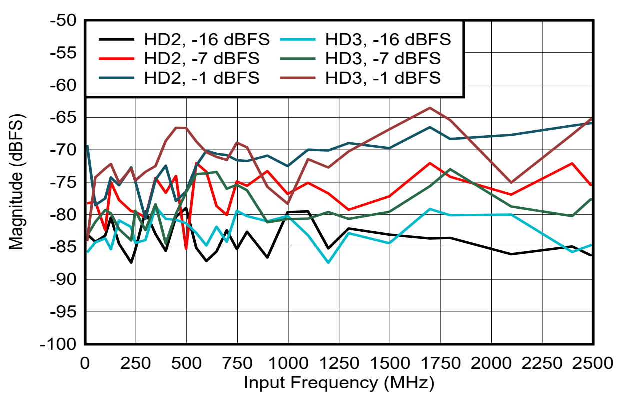
DES_EN = 0, f_S = 2500MHz, FG calibration

Figure 5-216. SFDR vs Input Frequency



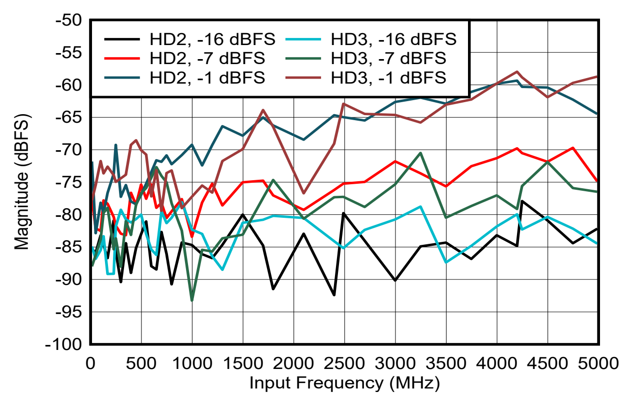
DES_EN = 1, f_S = 5000MHz, FG calibration

Figure 5-217. SFDR vs Input Frequency



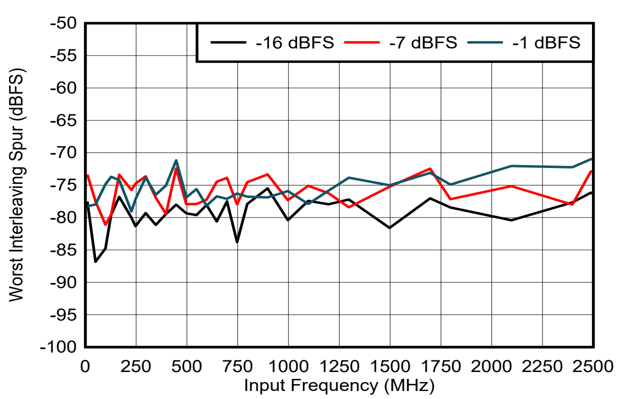
DES_EN = 0, f_S = 2500MHz, FG calibration

Figure 5-218. HD2 and HD3 vs Input Frequency



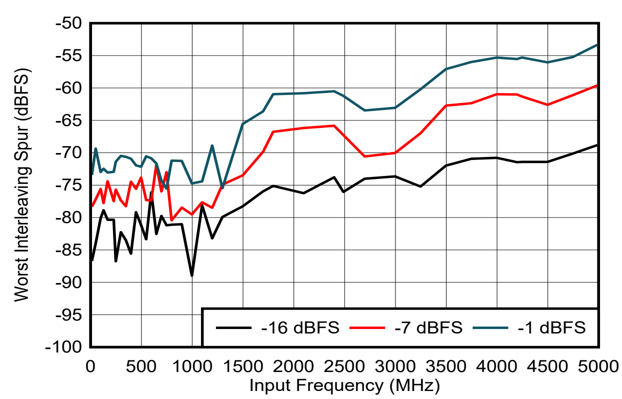
DES_EN = 1, f_S = 5000MHz, FG calibration

Figure 5-219. HD2 and HD3 vs Input Frequency



DES_EN = 0, f_S = 2500MHz, FG calibration, includes f_S / 2 – f_{IN} spur only

Figure 5-220. Worst Interleaving Spur vs Input Frequency

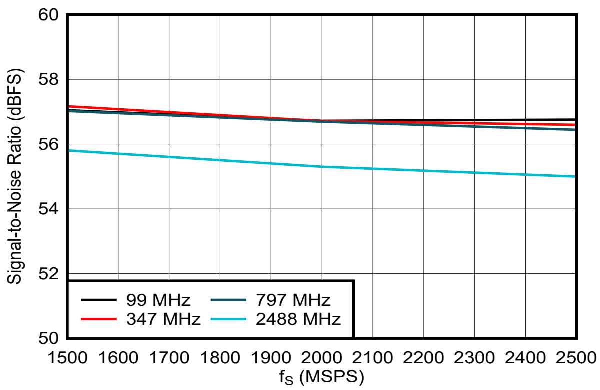


DES_EN = 1, f_S = 5000MHz, FG calibration, includes f_S / 2 – f_{IN} and f_S /4 ± f_{IN} spurs only

Figure 5-221. Worst Interleaving Spur vs Input Frequency

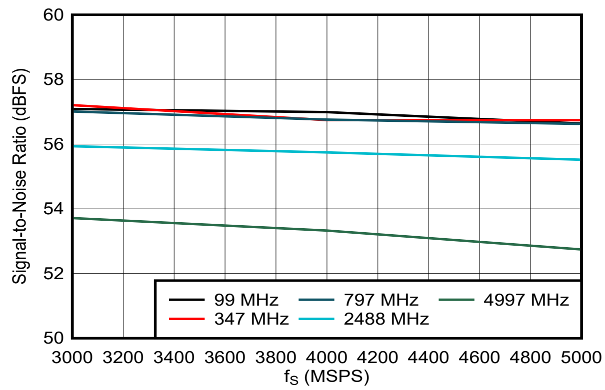
5.16 Typical Characteristics - ADC12DL2500 (2.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 2.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



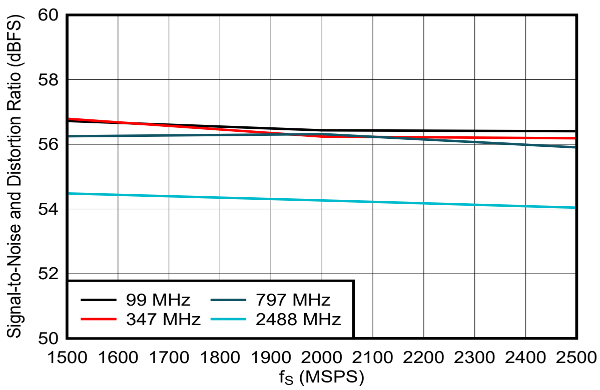
DES_EN = 0, f_S = 2500MHz, FG calibration

Figure 5-222. SNR vs Sampling Rate



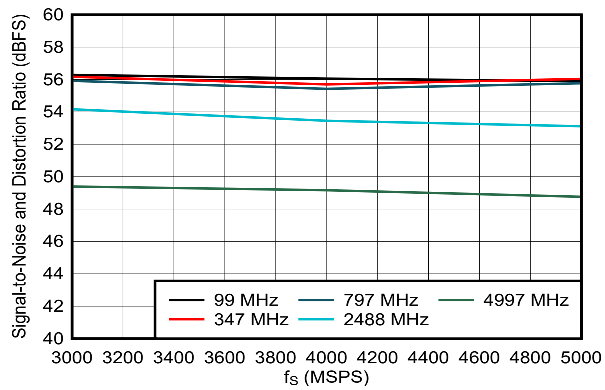
DES_EN = 1, f_S = 5000MHz, FG calibration

Figure 5-223. SNR vs Sampling Rate



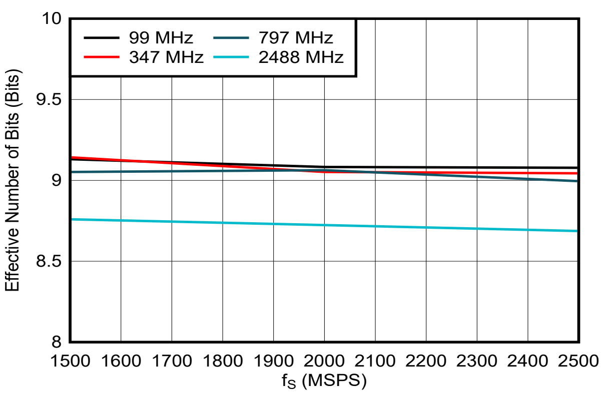
DES_EN = 0, f_S = 2500MHz, FG calibration

Figure 5-224. SINAD vs Sampling Rate



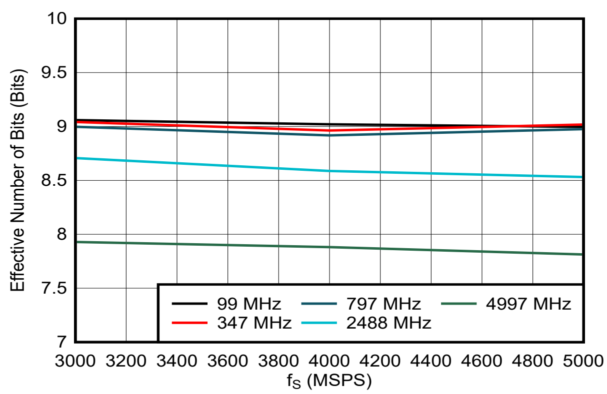
DES_EN = 1, f_S = 5000MHz, FG calibration

Figure 5-225. SINAD vs Sampling Rate



DES_EN = 0, f_S = 2500MHz, FG calibration

Figure 5-226. ENOB vs Sampling Rate

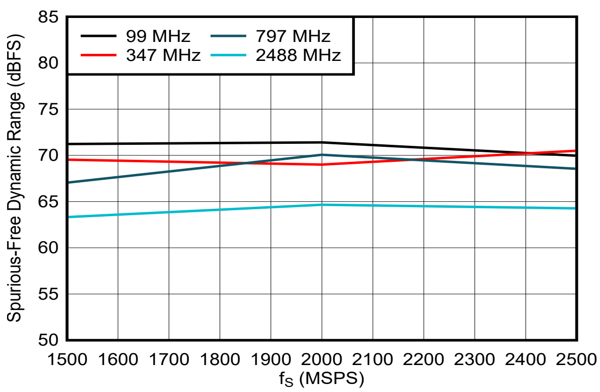


DES_EN = 1, f_S = 5000MHz, FG calibration

Figure 5-227. ENOB vs Sampling Rate

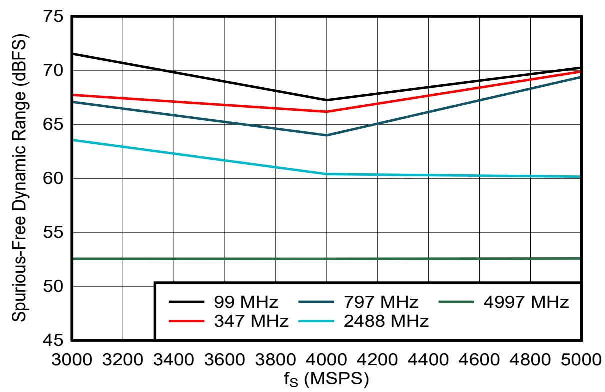
5.16 Typical Characteristics - ADC12DL2500 (2.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 2.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



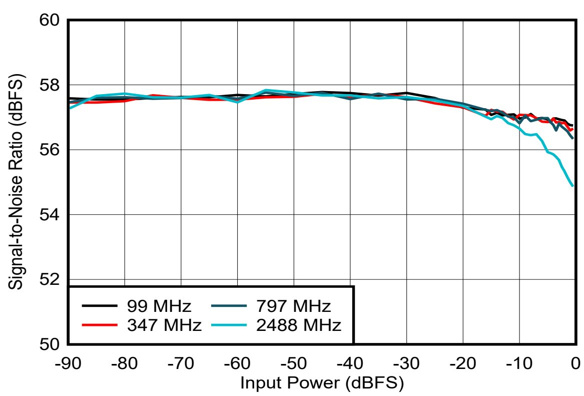
DES_EN = 0, f_S = 2500MHz, FG calibration

Figure 5-228. SFDR vs Sampling Rate



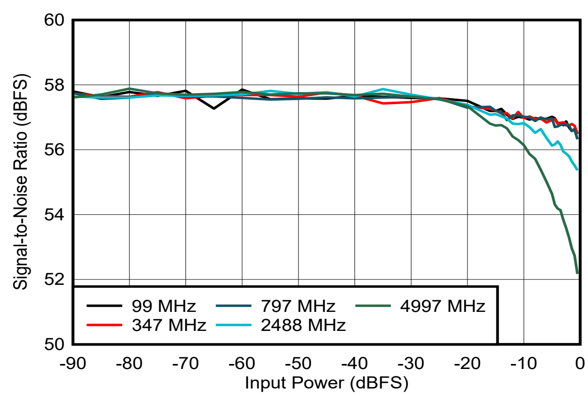
DES_EN = 1, f_S = 5000MHz, FG calibration

Figure 5-229. SFDR vs Sampling Rate



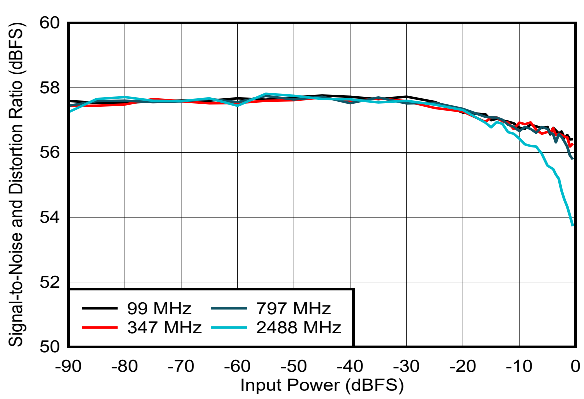
DES_EN = 0, f_S = 2500MHz, FG calibration

Figure 5-230. SNR vs Input Power



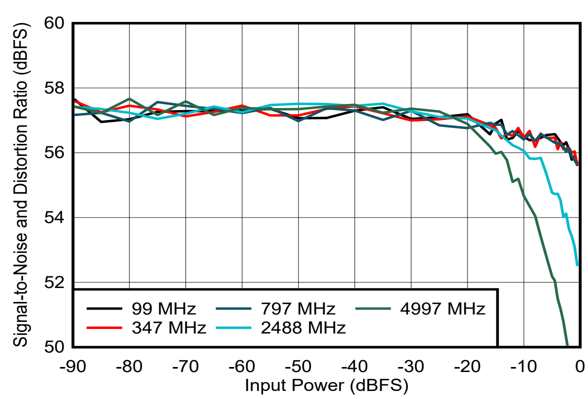
DES_EN = 1, f_S = 5000MHz, FG calibration

Figure 5-231. SNR vs Input Power



DES_EN = 0, f_S = 2500MHz, FG calibration

Figure 5-232. SINAD vs Input Power

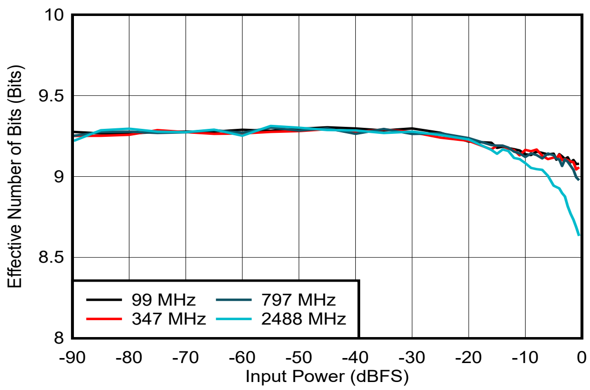


DES_EN = 1, f_S = 5000MHz, FG calibration

Figure 5-233. SINAD vs Input Power

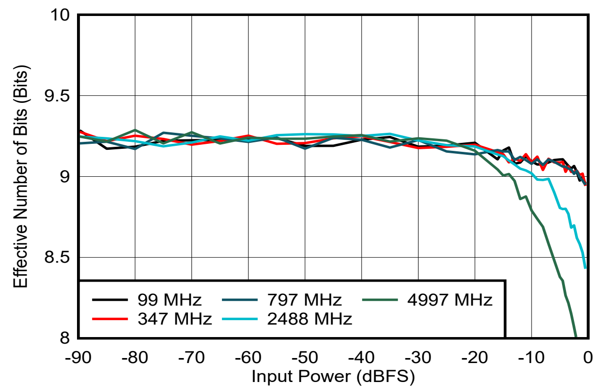
5.16 Typical Characteristics - ADC12DL2500 (2.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 2.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



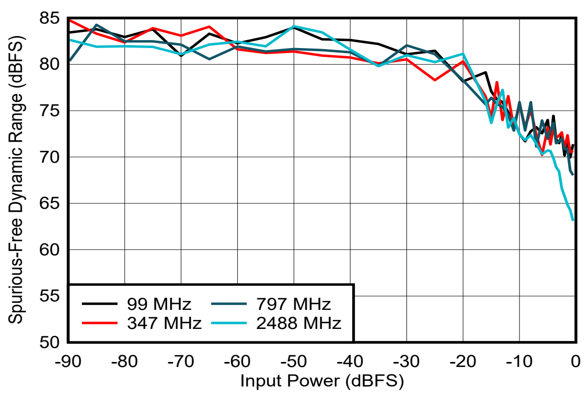
DES_EN = 0, f_S = 2500MHz, FG calibration

Figure 5-234. ENOB vs Input Power



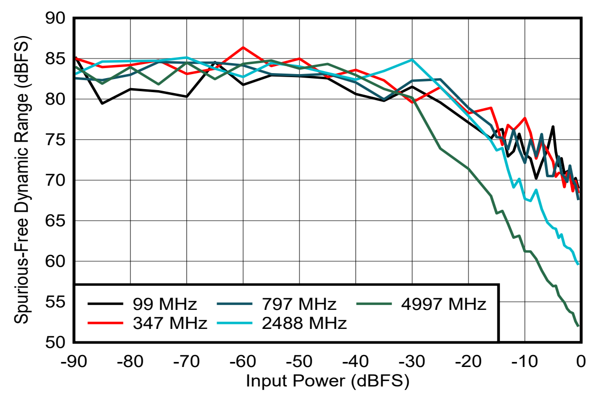
DES_EN = 1, f_S = 5000MHz, FG calibration

Figure 5-235. ENOB vs Input Power



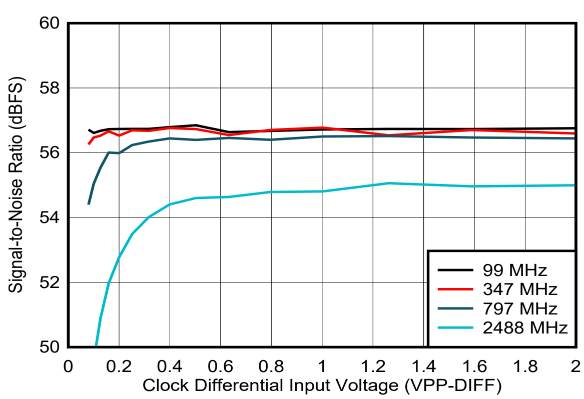
DES_EN = 0, f_S = 2500MHz, FG calibration

Figure 5-236. SFDR vs Input Power



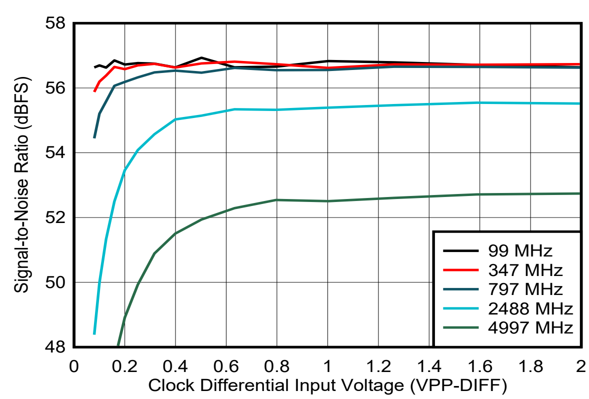
DES_EN = 1, f_S = 5000MHz, FG calibration

Figure 5-237. SFDR vs Input Power



DES_EN = 0, f_S = 2500MHz, FG calibration

Figure 5-238. SNR vs Clock Amplitude

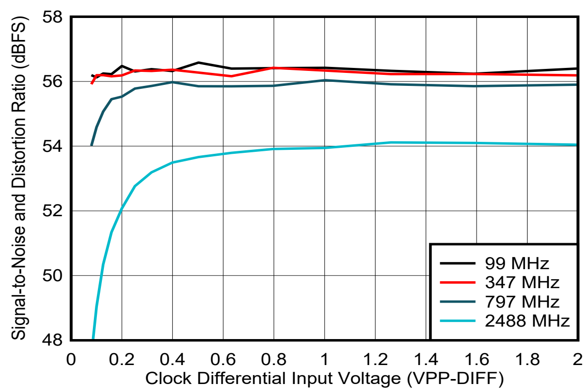


DES_EN = 1, f_S = 5000MHz, FG calibration

Figure 5-239. SNR vs Clock Amplitude

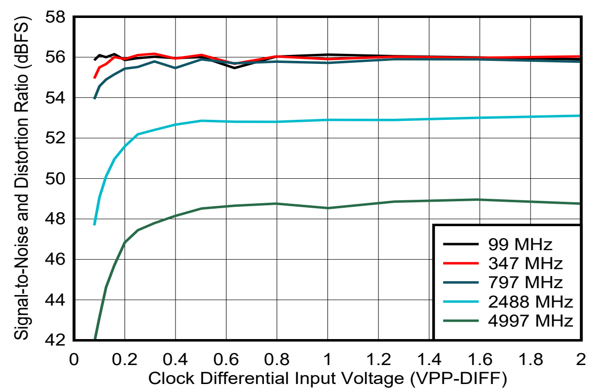
5.16 Typical Characteristics - ADC12DL2500 (2.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 2.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



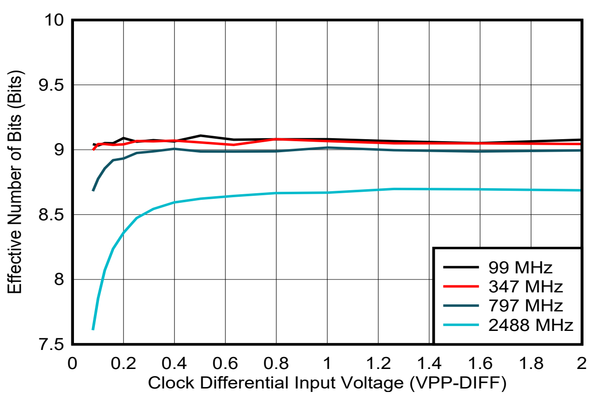
DES_EN = 0, f_S = 2500MHz, FG calibration

Figure 5-240. SINAD vs Clock Amplitude



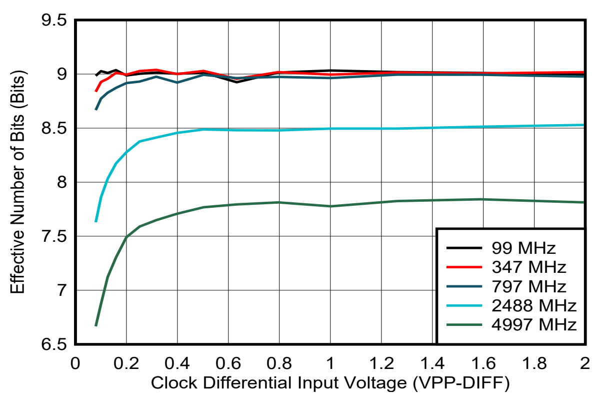
DES_EN = 1, f_S = 5000MHz, FG calibration

Figure 5-241. SINAD vs Clock Amplitude



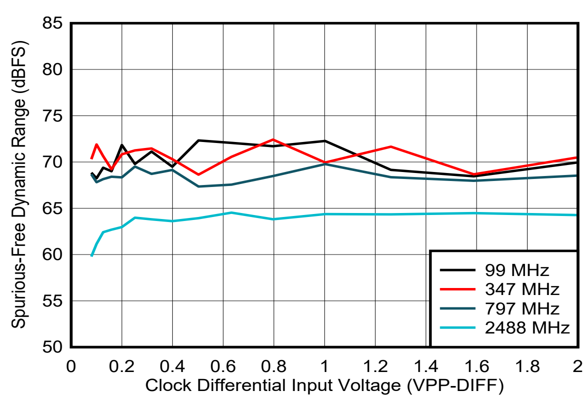
DES_EN = 0, f_S = 2500MHz, FG calibration

Figure 5-242. ENOB vs Clock Amplitude



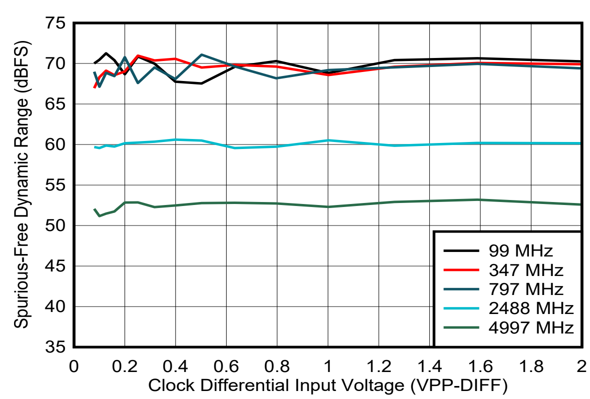
DES_EN = 1, f_S = 5000MHz, FG calibration

Figure 5-243. ENOB vs Clock Amplitude



DES_EN = 0, f_S = 2500MHz, FG calibration

Figure 5-244. SFDR vs Clock Amplitude

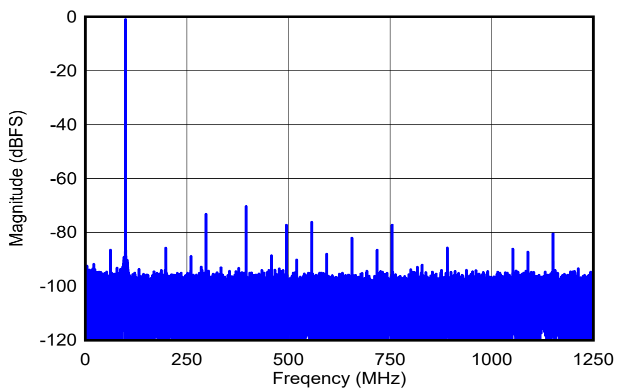


DES_EN = 1, f_S = 5000MHz, FG calibration

Figure 5-245. SFDR vs Clock Amplitude

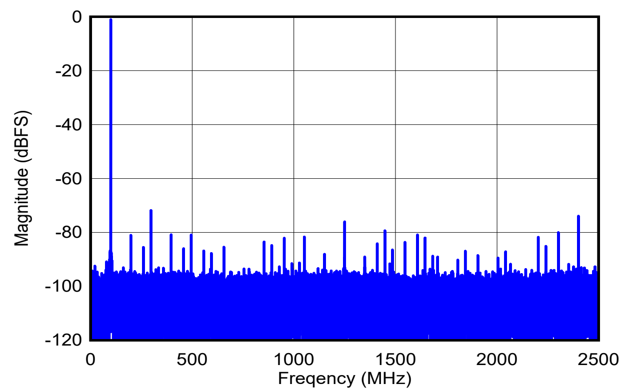
5.16 Typical Characteristics - ADC12DL2500 (2.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 2.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



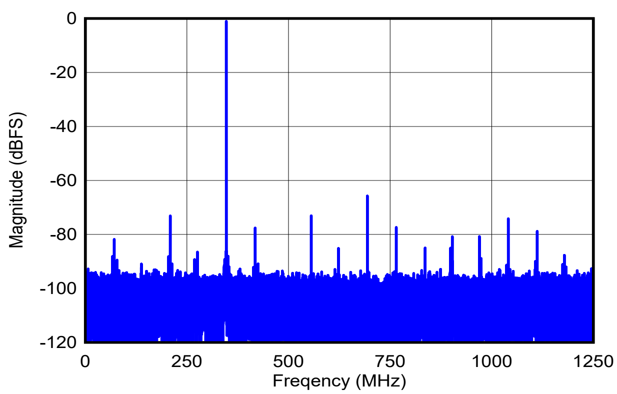
DES_EN = 0, f_S = 2500MHz, FG calibration, SNR = 57.1dBFS, SFDR = 70.3dBFS, ENOB = 9.1 bits

Figure 5-246. Single-Tone FFT at f_{IN} = 99MHz, AIN = –1dBFS



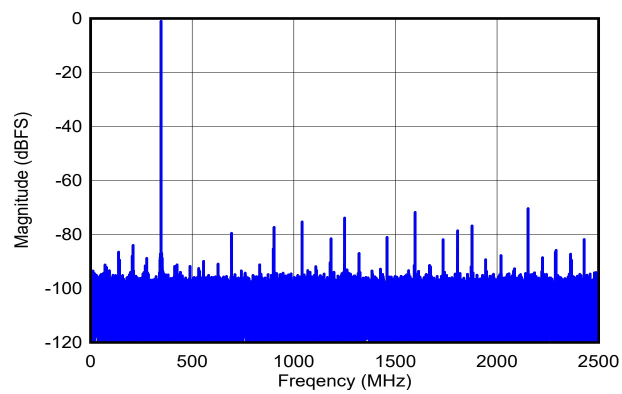
DES_EN = 1, f_S = 5000MHz, FG calibration, SNR = 57.0dBFS, SFDR = 71.7dBFS, ENOB = 9.1 bits

Figure 5-247. Single-Tone FFT at f_{IN} = 99MHz, AIN = –1dBFS



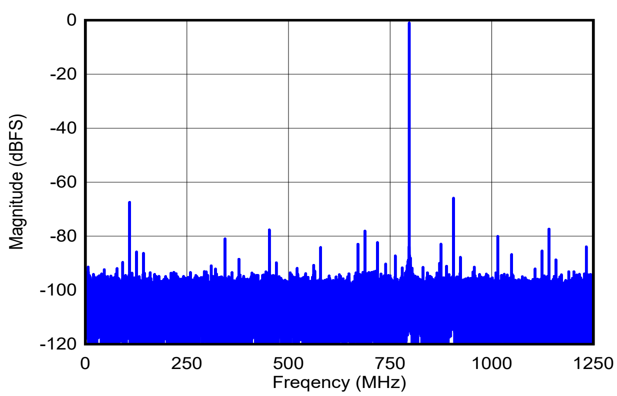
DES_EN = 0, f_S = 2500MHz, FG calibration, SNR = 56.7dBFS, SFDR = 65.7dBFS, ENOB = 9.0 bits

Figure 5-248. Single-Tone FFT at f_{IN} = 347MHz, AIN = –1dBFS



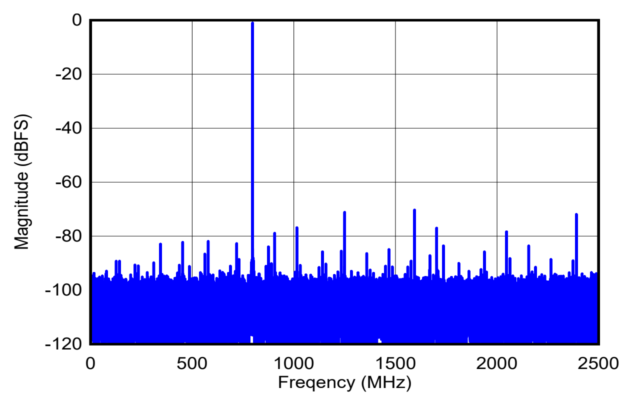
DES_EN = 1, f_S = 5000MHz, FG calibration, SNR = 57.3dBFS, SFDR = 70.1dBFS, ENOB = 9.1 bits

Figure 5-249. Single-Tone FFT at f_{IN} = 347MHz, AIN = –1dBFS



DES_EN = 0, f_S = 2500MHz, FG calibration, SNR = 56.8dBFS, SFDR = 65.8dBFS, ENOB = 9.0 bits

Figure 5-250. Single-Tone FFT at f_{IN} = 797MHz, AIN = –1dBFS

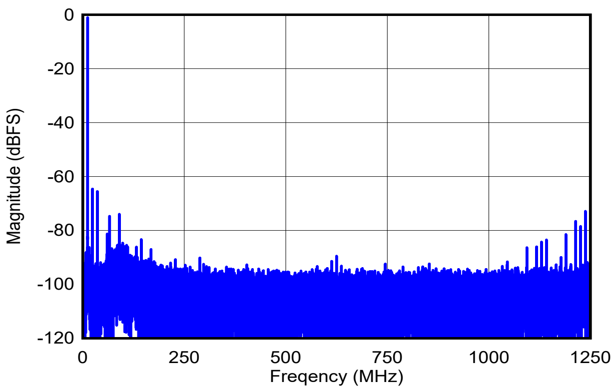


DES_EN = 1, f_S = 5000MHz, FG calibration, SNR = 57.1dBFS, SFDR = 70.2dBFS, ENOB = 9.0 bits

Figure 5-251. Single-Tone FFT at f_{IN} = 797MHz, AIN = –1dBFS

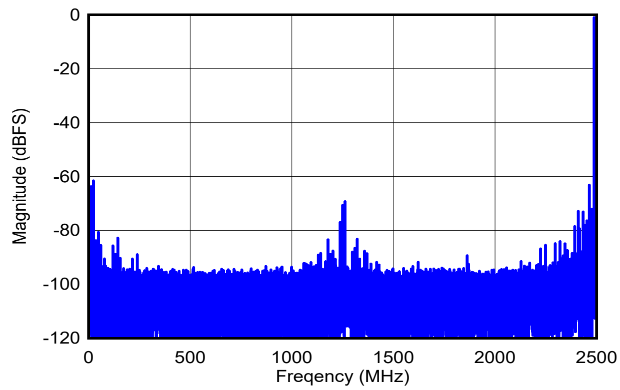
5.16 Typical Characteristics - ADC12DL2500 (2.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 2.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



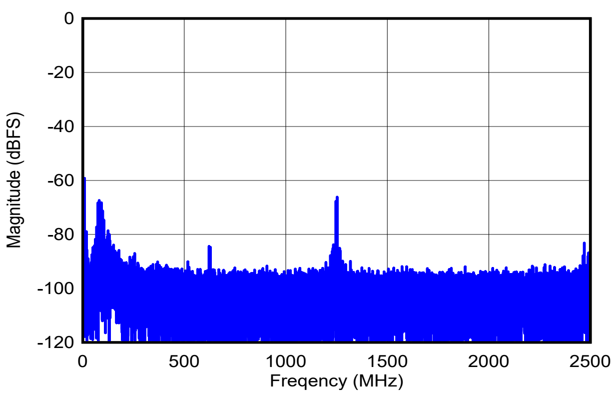
DES_EN = 0, f_S = 2500MHz, FG calibration, SNR = 55.2dBFS, SFDR = 64.6dBFS, ENOB = 8.7 bits

Figure 5-252. Single-Tone FFT at f_{IN} = 2488MHz, AIN = –1dBFS



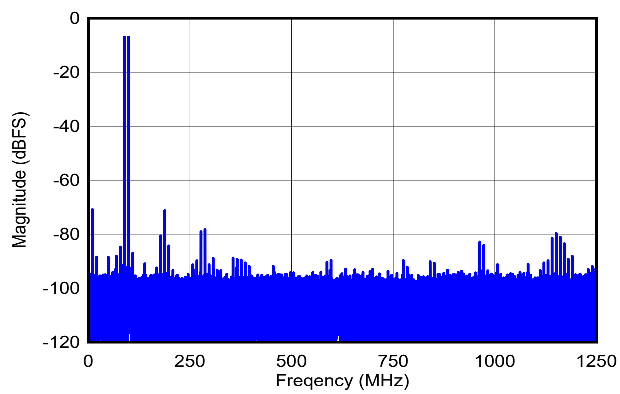
DES_EN = 1, f_S = 5000MHz, FG calibration, SNR = 55.7dBFS, SFDR = 61.5dBFS, ENOB = 8.5 bits

Figure 5-253. Single-Tone FFT at f_{IN} = 2488MHz, AIN = –1dBFS



DES_EN = 1, f_S = 5000MHz, FG calibration, SNR = 53.2dBFS, SFDR = 53.2dBFS, ENOB = 7.9 bits

Figure 5-254. Single-Tone FFT at f_{IN} = 4997MHz, AIN = –1dBFS

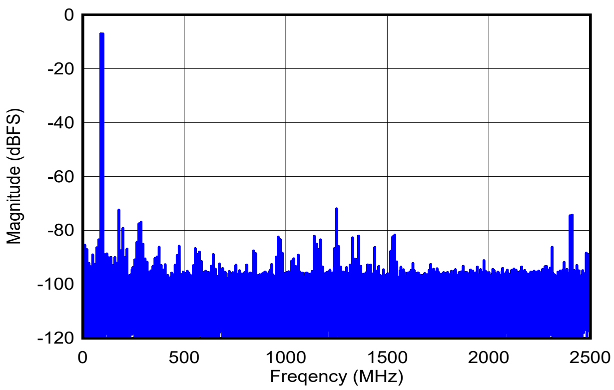


DES_EN = 0, f_S = 2500MHz, FG calibration, f_1 = 89MHz, f_2 = 99MHz, A_{IN} = -7dBFS per tone, SFDR = -71dBFS, IMD3 = -86dBFS, IMD2 = -71dBFS

Figure 5-255. Two-Tone FFT at f_{IN} = 94MHz, AIN = –1dBFS

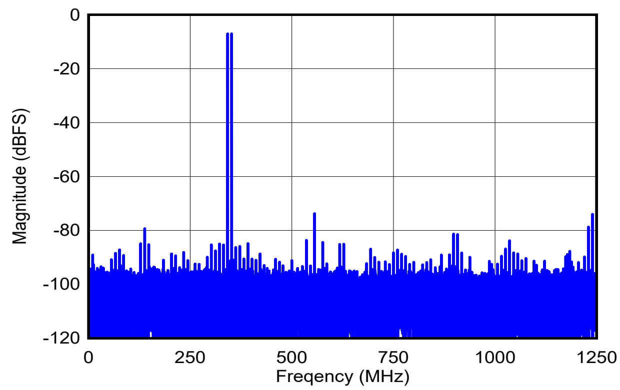
5.16 Typical Characteristics - ADC12DL2500 (2.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 2.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



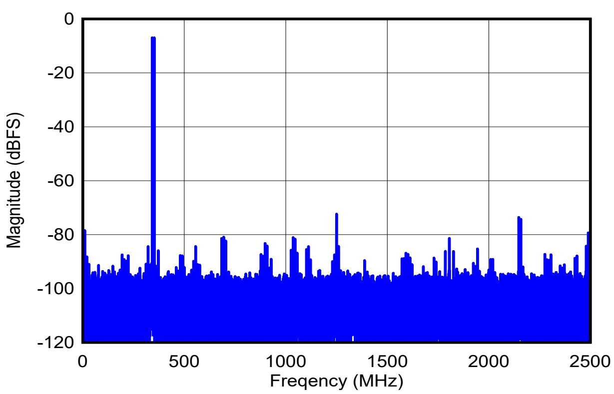
DES_EN = 1, f_S = 5000MHz, FG calibration, f_1 = 89MHz, f_2 = 99MHz, A_{IN} = -7dBFS per tone, SFDR = -72dBFS, IMD3 = -86dBFS, IMD2 = -86dBFS

Figure 5-256. Two-Tone FFT at f_{IN} = 94MHz, AIN = –1dBFS



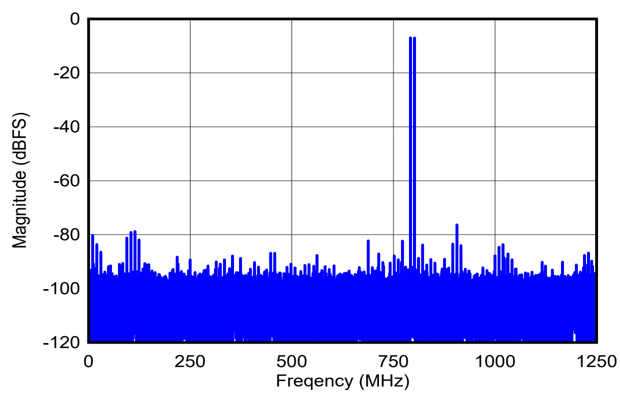
DES_EN = 0, f_S = 2500MHz, FG calibration, f_1 = 342MHz, f_2 = 352MHz, A_{IN} = -7dBFS per tone, SFDR = -74dBFS, IMD3 = -86dBFS, IMD2 = -88dBFS

Figure 5-257. Two-Tone FFT at f_{IN} = 347MHz, AIN = –1dBFS



DES_EN = 1, f_S = 5000MHz, FG calibration, f_1 = 342MHz, f_2 = 352MHz, A_{IN} = -7dBFS per tone, SFDR = -74dBFS, IMD3 = -91dBFS, IMD2 = -80dBFS

Figure 5-258. Two-Tone FFT at f_{IN} = 347MHz, AIN = –1dBFS

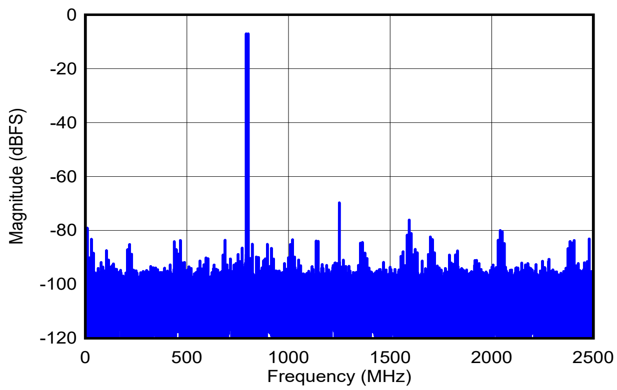


DES_EN = 0, f_S = 2500MHz, FG calibration, f_1 = 792MHz, f_2 = 802MHz, A_{IN} = -7dBFS per tone, SFDR = -76dBFS, IMD3 = -91dBFS, IMD2 = -78dBFS

Figure 5-259. Two-Tone FFT at f_{IN} = 797MHz, AIN = –1dBFS

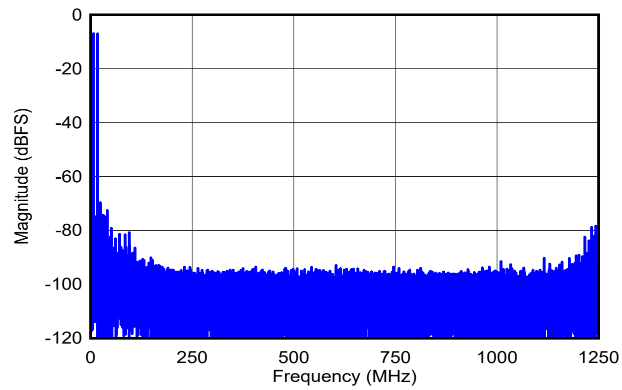
5.16 Typical Characteristics - ADC12DL2500 (2.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 2.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



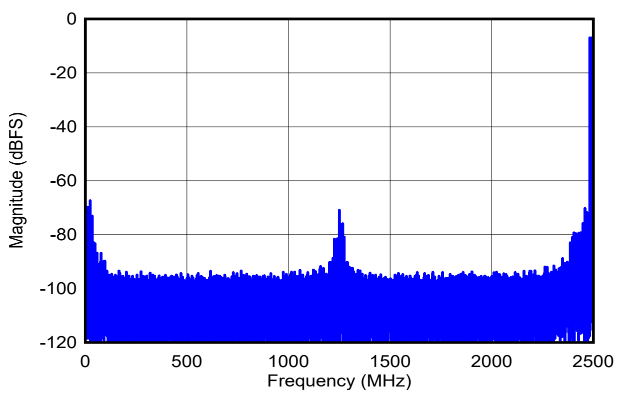
DES_EN = 1, f_S = 5000MHz, FG calibration, f_1 = 792MHz, f_2 = 802MHz, A_{IN} = -7dBFS per tone, SFDR = -76dBFS, IMD3 = -93dBFS, IMD2 = -77dBFS

Figure 5-260. Two-Tone FFT at f_{IN} = 797MHz, AIN = –1dBFS



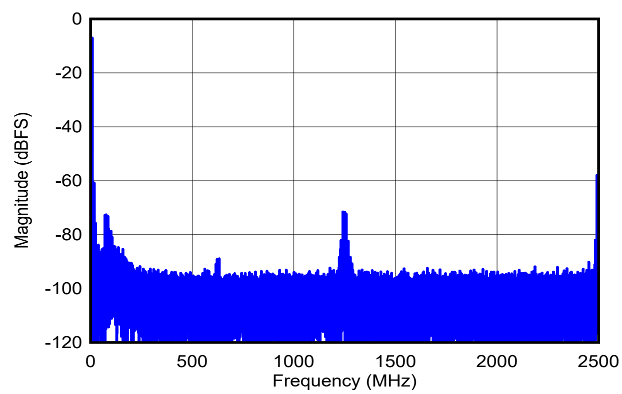
DES_EN = 0, f_S = 2500MHz, FG calibration, f_1 = 2483MHz, f_2 = 2493MHz, A_{IN} = -7dBFS per tone, SFDR = -70dBFS, IMD3 = -76dBFS, IMD2 = -74dBFS

Figure 5-261. Two-Tone FFT at f_{IN} = 2488MHz, AIN = –1dBFS



DES_EN = 1, f_S = 5000MHz, FG calibration, f_1 = 2483MHz, f_2 = 2493MHz, A_{IN} = -7dBFS per tone, SFDR = -67dBFS, IMD3 = -74dBFS, IMD2 = -73dBFS

Figure 5-262. Two-Tone FFT at f_{IN} = 2488MHz, AIN = –1dBFS

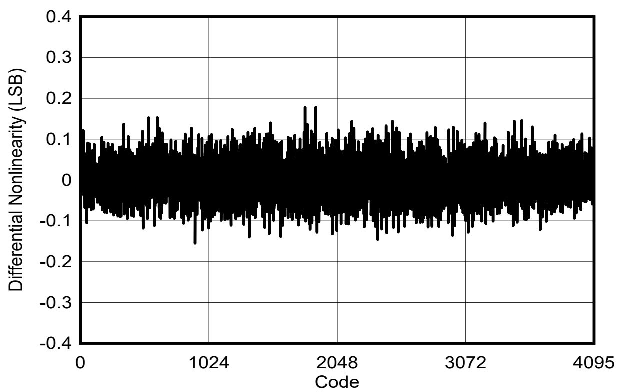


DES_EN = 1, f_S = 5000MHz, FG calibration, f_1 = 4992MHz, f_2 = 5002MHz, A_{IN} = -7dBFS per tone, SFDR = -58dBFS, IMD3 = -61dBFS, IMD2 = -78dBFS

Figure 5-263. Two-Tone FFT at f_{IN} = 4997MHz, AIN = –1dBFS

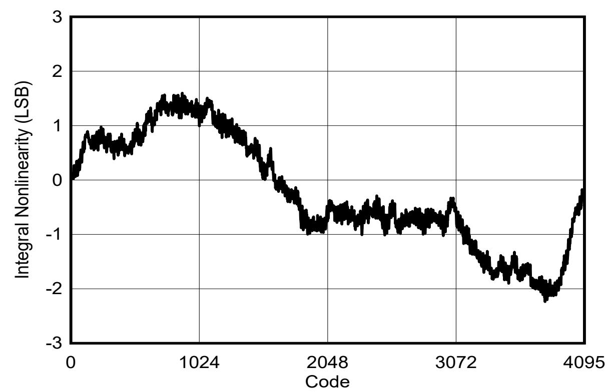
5.16 Typical Characteristics - ADC12DL2500 (2.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 2.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



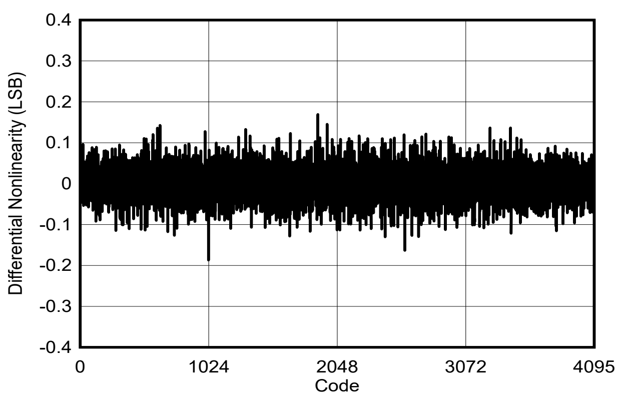
DES_EN = 0, f_S = 2500MHz, FG calibration, F_{IN} = 99MHz

Figure 5-264. DNL vs Code



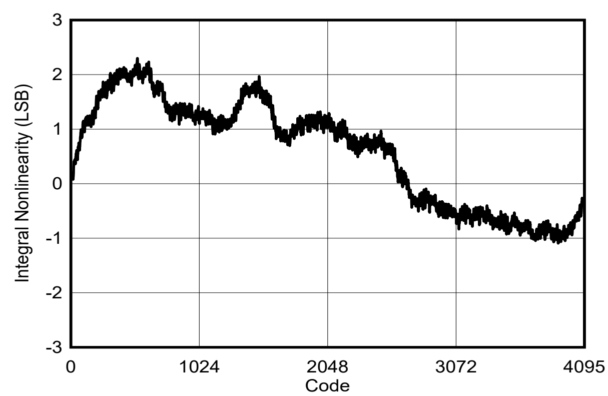
DES_EN = 0, f_S = 2500MHz, FG calibration, F_{IN} = 99MHz

Figure 5-265. INL vs Code



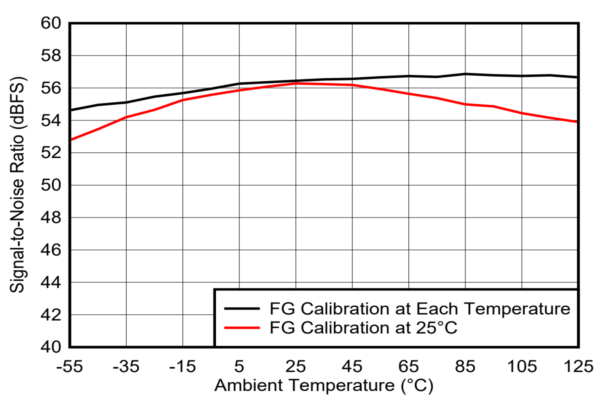
DES_EN = 1, f_S = 5000MHz, FG calibration, F_{IN} = 99MHz

Figure 5-266. DNL vs Code



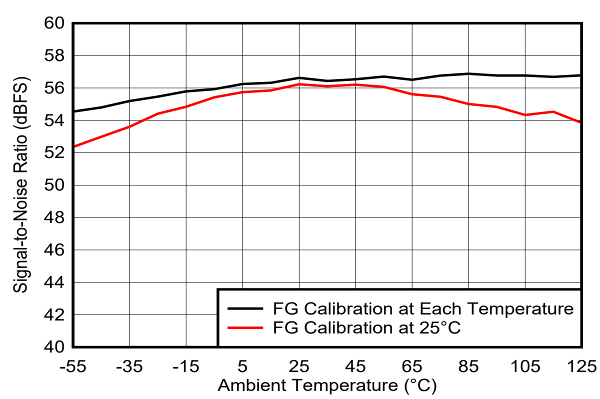
DES_EN = 1, f_S = 5000MHz, FG calibration, F_{IN} = 99MHz

Figure 5-267. INL vs Code



DES_EN = 0, f_S = 2500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-268. SNR vs Temperature and Calibration Mode

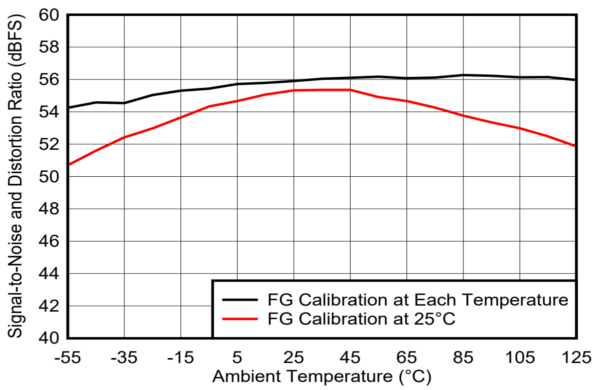


DES_EN = 1, f_S = 5000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-269. SNR vs Temperature and Calibration Mode

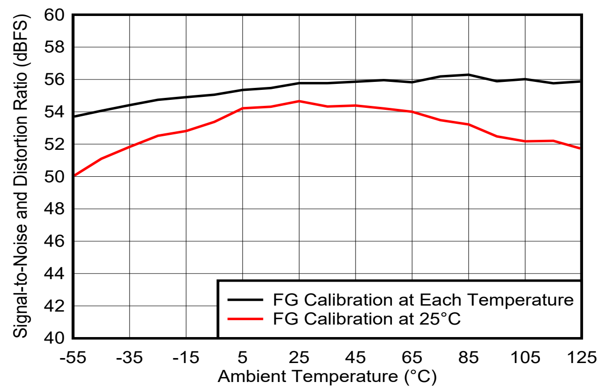
5.16 Typical Characteristics - ADC12DL2500 (2.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 2.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



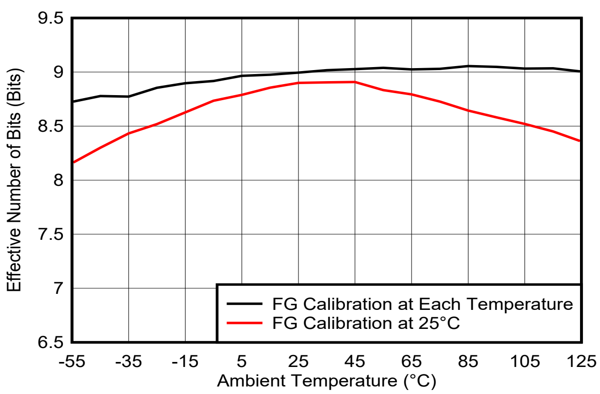
DES_EN = 0, f_S = 2500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-270. SINAD vs Temperature and Calibration Mode



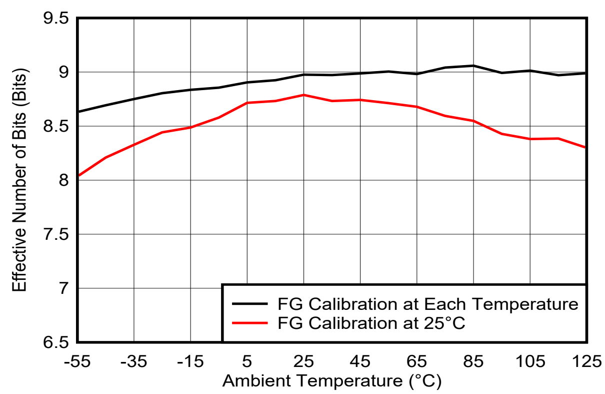
DES_EN = 1, f_S = 5000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-271. SINAD vs Temperature and Calibration Mode



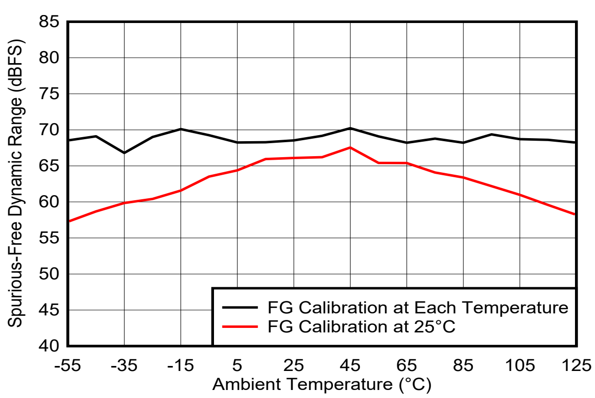
DES_EN = 0, f_S = 2500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-272. ENOB vs Temperature and Calibration Mode



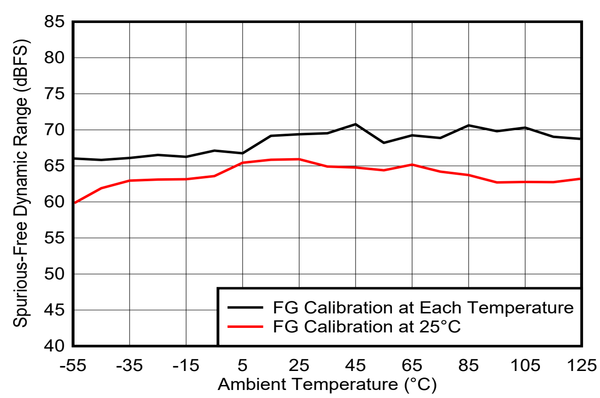
DES_EN = 1, f_S = 5000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-273. ENOB vs Temperature and Calibration Mode



DES_EN = 0, f_S = 2500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-274. SFDR vs Temperature and Calibration Mode

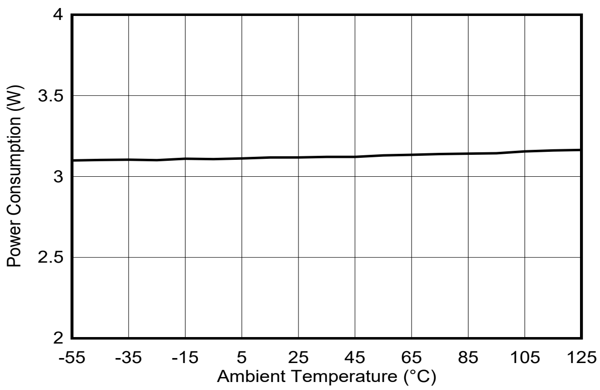


DES_EN = 1, f_S = 5000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-275. SFDR vs Temperature and Calibration Mode

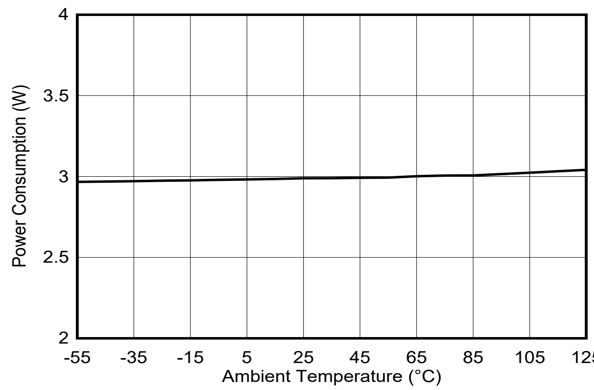
5.16 Typical Characteristics - ADC12DL2500 (2.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 2.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



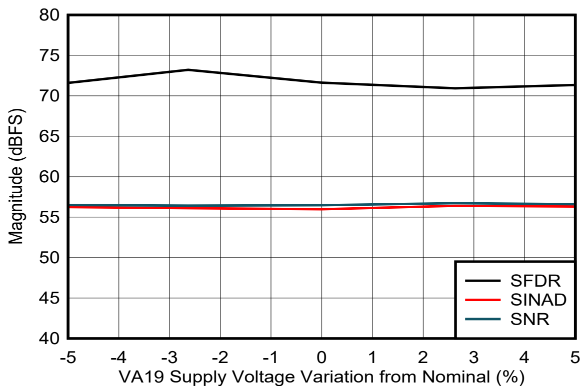
DES_EN = 0, f_S = 2500MHz, F_{IN} = 99MHz, A_{IN} = -1dBFS

Figure 5-276. Power Consumption vs Temperature



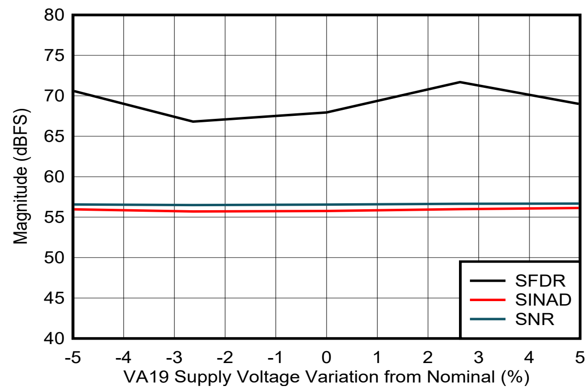
DES_EN = 1, f_S = 5000MHz, F_{IN} = 99MHz, A_{IN} = -1dBFS

Figure 5-277. Power Consumption vs Temperature



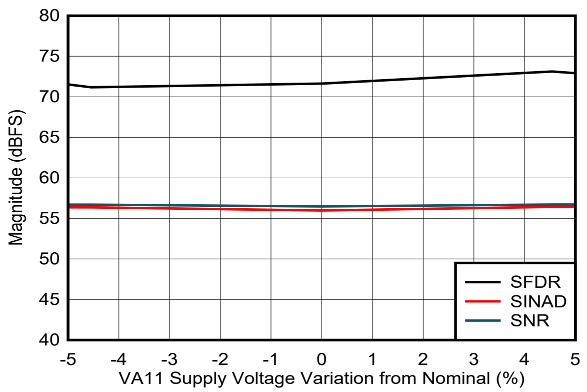
DES_EN = 0, f_S = 2500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-278. Performance vs VA19 Supply Voltage



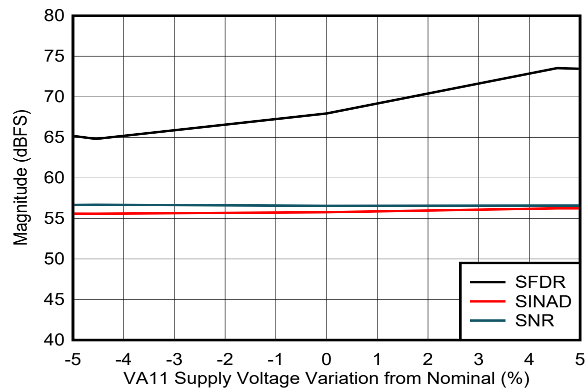
DES_EN = 1, f_S = 5000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-279. Performance vs VA19 Supply Voltage



DES_EN = 0, f_S = 2500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-280. Performance vs VA11 Supply Voltage

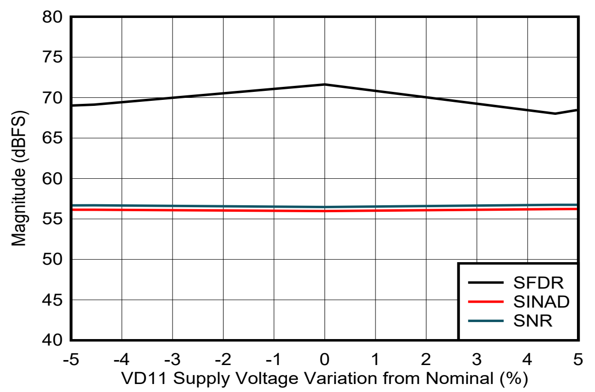


DES_EN = 1, f_S = 5000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-281. Performance vs VA11 Supply Voltage

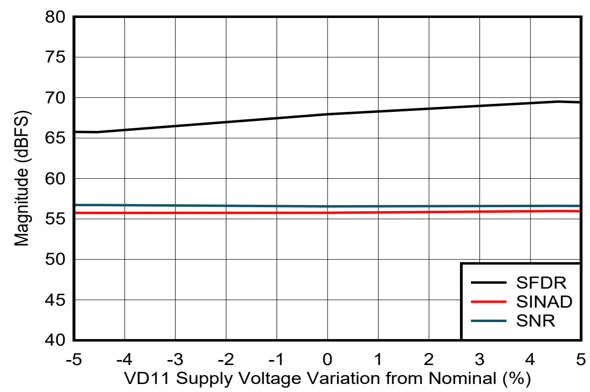
5.16 Typical Characteristics - ADC12DL2500 (2.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 2.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



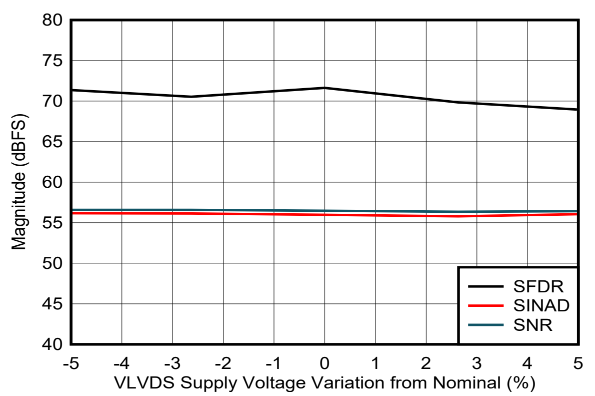
DES_EN = 0, f_S = 2500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-282. Performance vs VD11 Supply Voltage



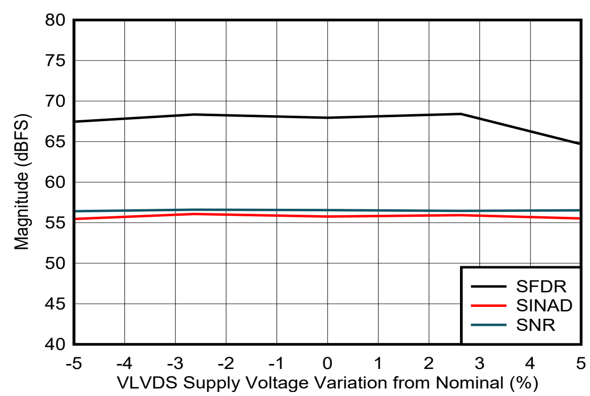
DES_EN = 1, f_S = 5000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-283. Performance vs VD11 Supply Voltage



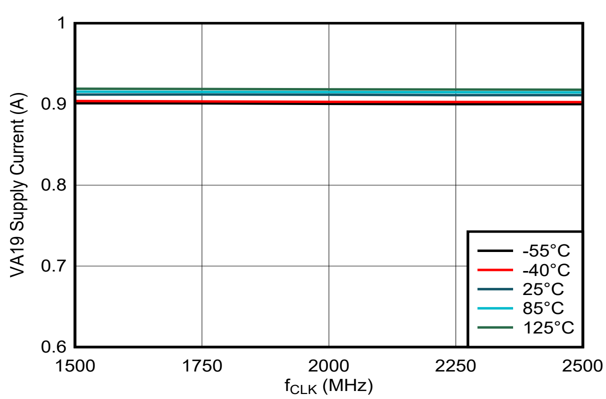
DES_EN = 0, f_S = 2500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-284. Performance vs VLVDS Supply Voltage



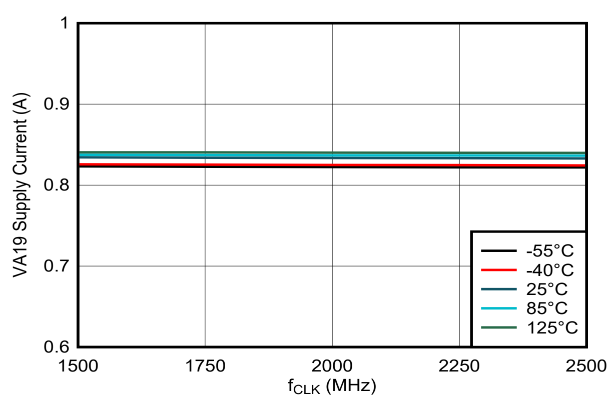
DES_EN = 1, f_S = 5000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-285. Performance vs VLVDS Supply Voltage



DES_EN = 0, f_S = 2500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-286. VA19 Supply Current vs Clock Rate

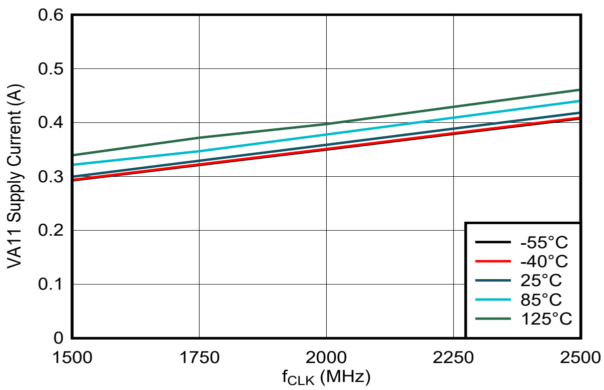


DES_EN = 1, f_S = 5000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-287. VA19 Supply Current vs Clock Rate

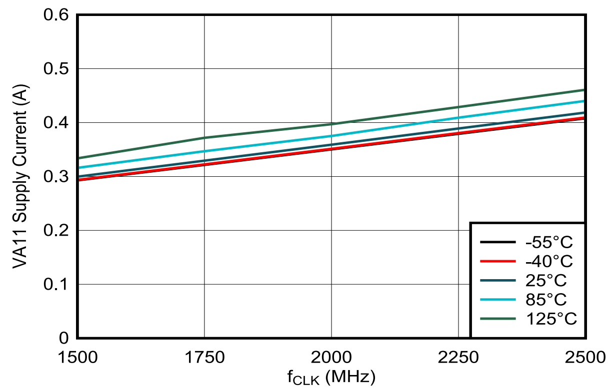
5.16 Typical Characteristics - ADC12DL2500 (2.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 2.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



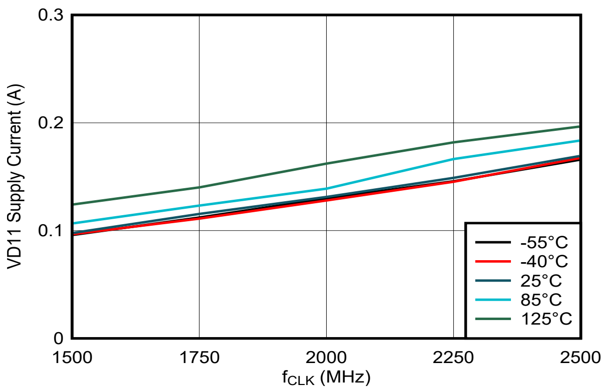
DES_EN = 0, f_S = 2500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-288. VA11 Supply Current vs Clock Rate



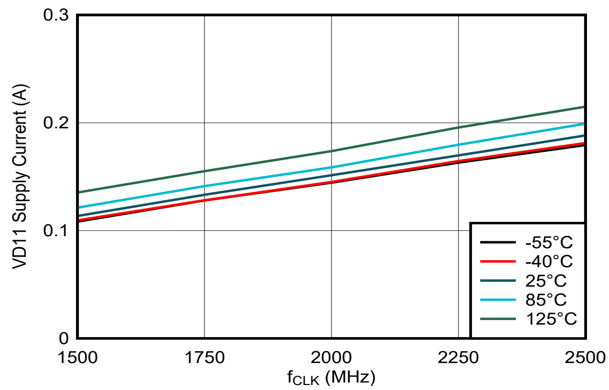
DES_EN = 1, f_S = 5000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-289. VA11 Supply Current vs Clock Rate



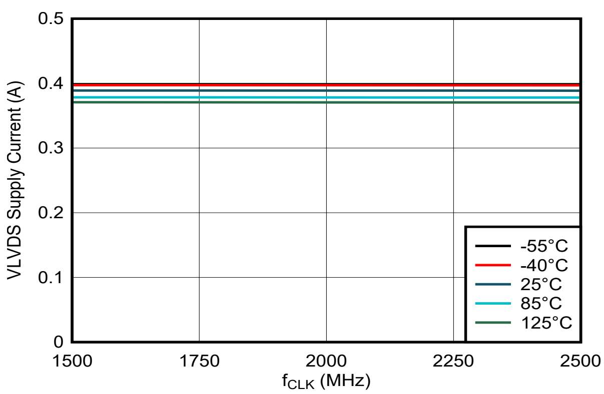
DES_EN = 0, f_S = 2500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-290. VD11 Supply Current vs Clock Rate



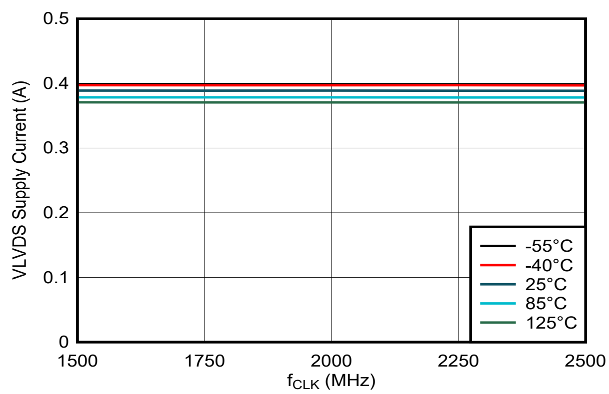
DES_EN = 1, f_S = 5000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-291. VD11 Supply Current vs Clock Rate



DES_EN = 0, f_S = 2500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-292. VLVDS Supply Current vs Clock Rate

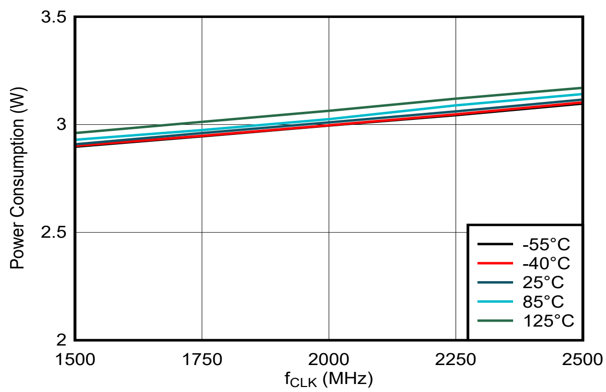


DES_EN = 1, f_S = 5000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-293. VLVDS Supply Current vs Clock Rate

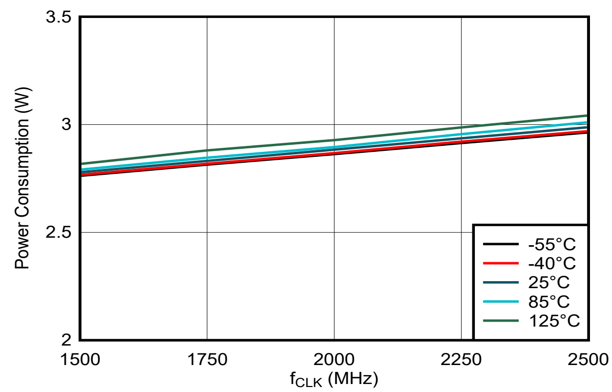
5.16 Typical Characteristics - ADC12DL2500 (2.5GSPS) (continued)

Typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN} = 347MHz, A_{IN} = –1dBFS, f_{CLK} = 2.5GHz, filtered $1V_{PP}$ sine-wave clock, DES_EN = 1, LDEMUX = 1, LALIGNED = 0, ADC_DITH = 0x01, LVDS driver high-swing mode (HSM) and foreground calibration; SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



DES_EN = 0, f_S = 2500MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-294. Power Consumption vs Clock Rate



DES_EN = 1, f_S = 5000MHz, F_{IN} = 347MHz, A_{IN} = -1dBFS

Figure 5-295. Power Consumption vs Clock Rate

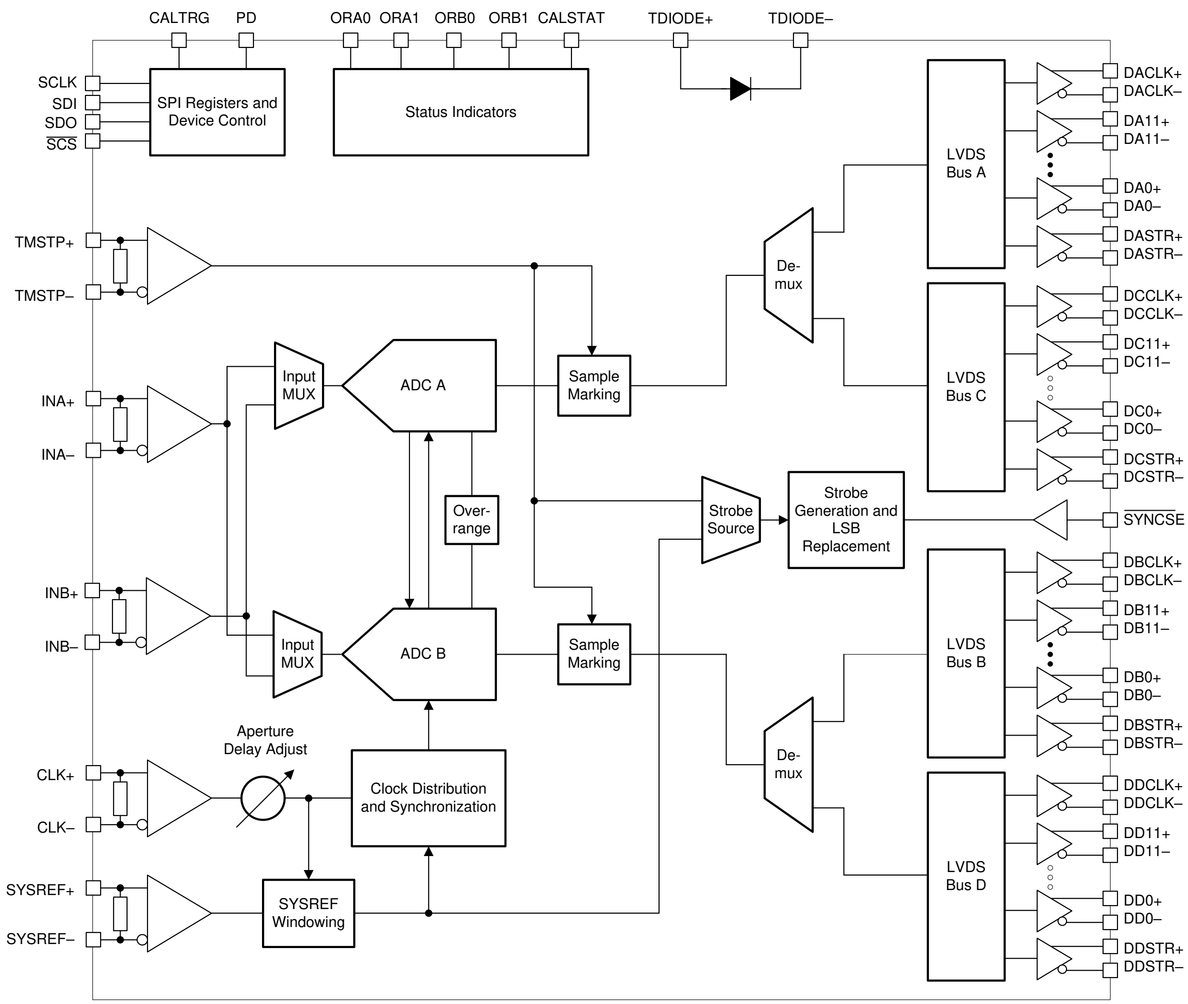
6 Detailed Description

6.1 Overview

The ADC12DL500, ADC12DL1500 and ADC12DL2500 are a family of giga-sample, analog-to-digital converters (ADC) that can sample up to 500MSPS, 1.5GSPS, and 2.5GSPS in dual-channel mode and up to 1GSPS, 3GSPS, and 5GSPS in single-channel mode. Programmable tradeoffs in channel count (dual-channel mode) and sample rate (single-channel mode) allow development of flexible hardware that meets the needs of both high-channel count or wide instantaneous signal bandwidth applications.

The ADC12DLx500 uses a low latency, low-voltage differential signaling (LVDS) interface for latency sensitive applications or when the simplicity of LVDS is preferred. The interface uses up to 48 data pairs, 4 double data rate (DDR) clocks and 4 strobe signals arranged in four 12-bit data buses. The interface supports signaling rates of up to 1.6Gbps. Strobe signals simplify synchronization across buses and between multiple devices. The strobe is generated internally and can be reset at a deterministic time by the SYSREF input. Multi-device synchronization is further eased by innovative synchronization features such as noiseless aperture delay (T_{AD}) adjustment and SYSREF windowing.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Analog Inputs

The analog inputs of the ADC12Dx500 family have internal buffers to enable high input bandwidth and isolate sampling capacitor glitch noise from the input circuit. The analog inputs must be driven differentially as operation with a single-ended signal is not recommended because of performance degradation. AC-coupling or DC-coupling can be used with the analog inputs. The common-mode voltage of the analog inputs is 0V and is biased internally through single-ended, 50Ω resistors to AGND on each input pin. When DC-coupled input signals are used the applied differential signal must have a common-mode voltage that meets the device Input common-mode requirements. See V_{CMI} in the *Recommended Operating Conditions* table. The 0V input common-mode voltage simplifies the interface to split-supply differential amplifiers and to a variety of transformers and baluns.

In single-channel mode, either analog input (AIN+ and AIN– or BIN+ and BIN–) can be used as the input to the ADC core. There is no degradation in analog input bandwidth when using single-channel mode versus dual-channel mode. The input can be chosen using SINGLE_INPUT in the *INPUT_MUX register*. In dual-channel mode, the analog inputs can be swapped using DUAL_INPUT in the *INPUT_MUX register.*

6.3.1.1 Analog Input Protection

The analog inputs are protected against overdrive conditions by internal clamping diodes that are capable of sourcing or sinking input currents during overrange conditions; see the voltage and current limits in the *Absolute Maximum Ratings* table. The overrange protection is also defined for a peak RF input power in the *Absolute Maximum Ratings* table, which is frequency independent. Operation above the maximum conditions listed in the *Recommended Operating Conditions* table results in an increase in failure-in-time (FIT) rate, so the system must correct the overdrive condition as quickly as possible. Figure 6-1 shows the analog input protection diodes.

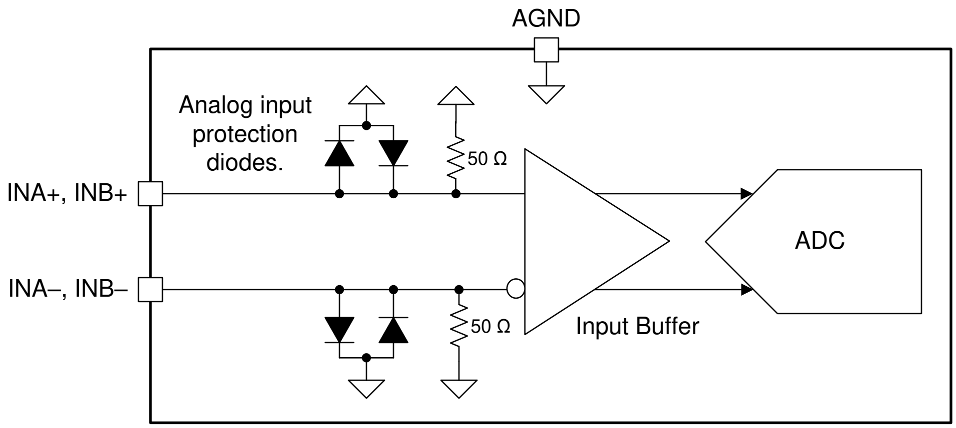


Figure 6-1. ADC12Dx500 Analog Input Internal Termination

6.3.1.2 Full-Scale Voltage (V_{FS}) Adjustment

Input full-scale voltage (V_{FS}) adjustment is available, in fine increments, for each analog input through the FS_RANGE_A (see the INA full-scale range adjust register) and FS_RANGE_B register settings (see the INB full-scale range adjust register) for INA± and INB±, respectively. The available adjustment range is specified in the *Electrical Characteristics: DC Specifications* table. Larger full-scale voltages improve SNR performance, but can degrade harmonic distortion. The full-scale voltage adjustment is useful for matching the full-scale range of multiple ADCs when developing a multi-converter system or for external interleaving of multiple ADC12DLx500s to achieve higher sampling rates.

6.3.1.3 Analog Input Offset Adjust

The input offset voltage for each input can be adjusted through the OADJ_x_FG0_VINy and OADJ_x_FG90_VINy registers (registers 0x330 to 0x34F), where x represents the ADC core (A or B) and y represents the analog input (INA± or INB±). The adjustment range is approximately 28mV to –28mV differential. See *Section 6.4.7* for more information.

6.3.2 ADC Core

The ADC12DLx500 consists of a total of six ADC cores. The cores are interleaved for higher sampling rates and swapped on-the-fly for calibration as required by the operating mode. In dual-channel mode each ADC channel is two-way interleaved. In single-channel mode the ADC is four-way interleaved. This section highlights the theory of operation and key features of the ADC cores.

6.3.2.1 ADC Theory of Operation

The differential voltages at the analog inputs are captured by the rising edge of CLK± in dual-channel mode or by the rising and falling edges of CLK± in single-channel mode. After capturing the input signal, the ADC converts the analog voltage to a digital value by comparing the voltage to the internal reference voltage. If the voltage on INA– or INB– is higher than the voltage on INA+ or INB+, respectively, then the digital output is a negative 2's complement value. If the voltage on INA+ or INB+ is higher than the voltage on INA– or INB–, respectively, then the digital output is a positive 2's complement value. Equation 1 can calculate the differential voltage at the input pins from the digital output.

$$V_{IN} = \frac{Code}{2^N} V_{FS} \tag{1}$$

where

- Code is the signed decimation output code (for example, –2048 to +2047)
- N is the ADC resolution
- V_{FS} is the full-scale input voltage of the ADC as specified in the *Recommended Operating Conditions* table, including any adjustment performed by programming FS_RANGE_A or FS_RANGE_B

6.3.2.2 ADC Core Calibration

ADC core calibration is required to optimize the analog performance of the ADC cores. Calibration must be repeated when operating conditions change significantly, namely temperature, to maintain optimal performance. The ADC12DLx500 has a built-in calibration routine that can be run as a foreground operation . Foreground operation requires ADC downtime, where the ADC is no longer sampling the input signal, to complete the process. See the *Section 6.4.7* section for detailed information on each mode.

6.3.2.3 ADC Overrange Detection

To make sure the system gain management has the quickest possible response time, a low-latency configurable overrange function is included. The overrange function works by monitoring the converted 12-bit samples at the ADC to quickly detect if the ADC is near saturation or already in an overrange condition. The absolute value of the upper eight bits of the ADC data are checked against two programmable thresholds, OVR_T0 and OVR_T1. These thresholds apply to both channel A and channel B in dual-channel mode. Table 6-1 lists how an ADC sample is converted to an absolute value for a comparison of the thresholds.

Table 6-1. Conversion of ADC Sample for Overrange Comparison

ADC SAMPLE (Offset Binary)	ADC SAMPLE (2's Complement)	ABSOLUTE VALUE	UPPER 8 BITS USED FOR COMPARISON
1111 1111 1111 (4095)	0111 1111 1111 (2047)	111 1111 1111 (2047)	1111 1111 (255)
1111 1111 0000 (4080)	0111 1111 0000 (2032)	111 1111 0000 (2032)	1111 1110 (254)
1000 0000 0000 (2048)	0000 0000 0000 (0)	000 0000 0000 (0)	0000 0000 (0)
0000 0001 0000 (16)	1000 0001 0000 (–2032)	111 1111 0000 (2032)	1111 1110 (254)
0000 0000 0000 (0)	1000 0000 0000 (–2048)	111 1111 1111 (2047)	1111 1111 (255)

If the upper eight bits of the absolute value equal or exceed the OVR_T0 or OVR_T1 thresholds during the monitoring period, then the overrange bit associated with the threshold is set to 1, otherwise the overrange bit is 0. In dual-channel mode, the overrange status can be monitored on the ORA0 and ORA1 pins for channel A and the ORB0 and ORB1 pins for channel B, where ORx0 corresponds to the OVR_T0 threshold and ORx1 corresponds to the OVR_T1 threshold. In single-channel mode, the overrange status for the OVR_T0 threshold is determined by monitoring both the ORA0 and ORB0 outputs and the OVR_T1 threshold is determined by monitoring both ORA1 and ORB1 outputs. In single-channel mode, the two outputs for each threshold must be OR'd together to determine whether an over-range condition occurred. OVR_N can be used to set the output pulse duration from the last overrange event. Table 6-2 lists the overrange pulse durations for the various OVR_N settings (see the overrange configuration register).

Table 6-2. Overrange Monitoring Period for the ORA0, ORA1, ORB0, and ORB1 Outputs

OVR_N	OVERRANGE PULSE DURATION FROM LAST OVERRANGE EVENT (DEVCLK Cycles)
0	8
1	16
2	32
3	64
4	128
5	256
6	512
7	1024

Typically, the OVR_T0 threshold can be set near the full-scale value (228 for example). When the threshold is triggered, a typical system can turn down the system gain to avoid clipping. The OVR_T1 threshold can be set much lower. For example, the OVR_T1 threshold can be set to 64 (peak input voltage of −12 dBFS). If the input signal is strong, the OVR_T1 threshold is tripped occasionally. If the input is quite weak, the threshold is never tripped. The downstream logic device monitors the OVR_T1 bit. If OVR_T1 stays low for an extended period of time, then the system gain can be increased until the threshold is occasionally tripped (meaning the peak level of the signal is above −12 dBFS).

6.3.2.4 Code Error Rate (CER)

ADC cores can generate bit errors within a sample, often called *code errors (CER)* or referred to as *sparkle codes*, resulting from metastability caused by non-ideal comparator limitations. The ADC12DLx500 uses a unique ADC architecture that inherently allows significant code error rate improvements from traditional pipelined flash or successive approximation register (SAR) ADCs. The code error rate of the ADC12DLx500 is multiple orders of magnitude better than what can be achieved in alternative architectures at equivalent sampling rates, providing significant signal reliability improvements.

6.3.2.5 Internal Dither

The ADC12DLx500 includes internal dither to smooth out the integral nonlinearity (INL) curve. Dither improves the high-order harmonic performance of the ADC cores that results in a reduction of spurs in the frequency spectrum for single-tone and narrow-band signals. The dither signal is subtracted out of converted data so that dither does not show up in the output signal and thus reduce the signal-to-noise signal.

6.3.3 Timestamp

The TMSTP+ and TMSTP– differential inputs can be used as a timestamp input to mark a specific sample based on the timing of an external trigger event relative to the sampled signal. TIME_STAMP_EN (see the LSB control bit output register) must be set to use the timestamp feature and output the timestamp data. When enabled, the LSB of the 12-bit ADC digital output reports the status of the TMSTP± input. In effect, the 12-bit output sample consists of the upper 11-bits of the 12-bit converter and the LSB of the 12-bit output sample is the output of a parallel 1-bit converter (TMSTP±) with the same latency as the ADC core. The trigger must be applied to the differential TMSTP+ and TMSTP– inputs. The trigger can be asynchronous to the ADC sampling clock and is sampled at approximately the same time as the analog input. Alternatively, the SYSREF± inputs can be used as the timestamp input when SYSREF_TIME_STAMP_EN is set to 1 in the CLK_CTRL1 register.

6.3.4 Clocking

The clocking subsystem of the ADC12DLx500 has two input signals: the device clock (CLK+, CLK–) and SYSREF (SYSREF+, SYSREF–). Within the clocking subsystem there is a noiseless aperture delay adjustment (t_{AD} adjust), a clock duty cycle corrector, and a SYSREF capture block. Figure 6-2 shows the clocking subsystem.

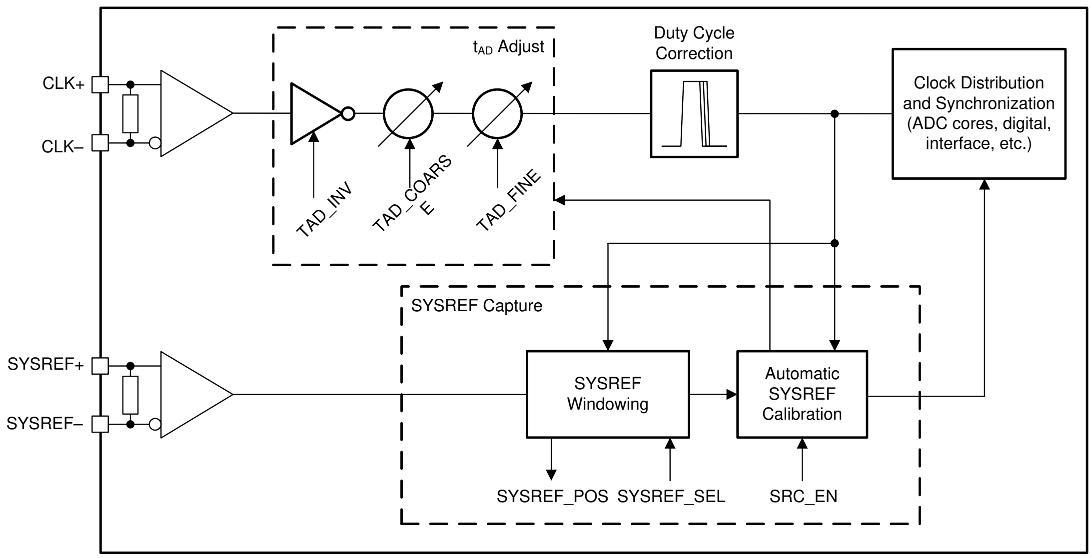


Figure 6-2. ADC12DLx500 Clocking Subsystem

The device clock is used as the sampling clock for the ADC core as well as the clocking for the digital processing and LVDS outputs. Use a low-noise (low jitter) device clock to maintain high signal-to-noise ratio (SNR) within the ADC. In dual-channel mode, the analog input signal for each input is sampled on the rising edge of the device clock. In single-channel mode, both the rising and falling edges of the device clock are used to capture the analog signal to reduce the maximum clock rate required by the ADC. A noiseless aperture delay adjustment (t_{AD} adjust) allows the sampling instance of the ADC to be shifted in fine steps to synchronize multiple ADC12DLx500 devices or to fine-tune system latency. Duty cycle correction is implemented in the ADC12DLx500 to ease the requirements on the external device clock while maintaining high performance. Table 6-3 summarizes the device clock interface in dual-channel mode and single-channel mode.

Table 6-3. Device Clock versus Mode of Operation

MODE OF OPERATION	SAMPLING RATE VS f_{CLK}	SAMPLING INSTANT
Dual-channel mode	$1 \times f_{CLK}$	Rising edge
Single-channel mode	$2 \times f_{CLK}$	Rising and falling edge

SYSREF is a system timing reference used to reset clock dividers and strobe generation within the ADC12DLx500 that is similar to the SYSREF signal used by JESD204B interface devices. SYSREF is used to synchronize multiple ADC12DLx500 devices. SYSREF must be captured by the correct device clock edge to achieve repeatable latency and synchronization. The ADC12DLx500 includes SYSREF windowing and automatic SYSREF calibration to ease the requirements on the external clocking circuits and to simplify the synchronization process. SYSREF can be implemented as a single pulse or as a periodic clock. In periodic implementations, SYSREF must be equal to, or an integer division of, the frame clock frequency. Equation 2 can be used to calculate valid SYSREF frequencies.

$$f_{SYSREF} = \frac{f_{CLK}}{(LDEMUX + 1) \times LFRAME \times n} \tag{2}$$

where

- LDEMUX and LFRAME are register settings
- f_{CLK} is the device clock frequency (CLK±)
- n is any positive integer

6.3.4.1 Noiseless Aperture Delay Adjustment (t_{AD} Adjust)

The ADC12DLx500 contains a delay adjustment on the device clock (sampling clock) input path, called t_{AD} adjust, that can be used to shift the sampling instance within the device to align sampling instances among multiple devices or for external interleaving of multiple ADC12DLx500 devices. Further, t_{AD} adjust can be used for automatic SYSREF calibration to simplify synchronization; see the *Section 6.3.4.3.2* section. Aperture delay adjustment is implemented in a way that adds no additional noise to the clock path, however a slight degradation in aperture jitter (t_{AJ}) is possible at large values of TAD_COARSE because of internal clock path attenuation. The degradation in aperture jitter can result in minor SNR degradations at high input frequencies (see t_{AJ} in the *Section 5.11* table). This feature is programmed using TAD_INV, TAD_COARSE, and TAD_FINE in the DEVCLK timing adjust ramp control register. Setting TAD_INV inverts the input clock resulting in a delay equal to half the clock period. Table 6-4 summarizes the step sizes and ranges of the TAD_COARSE and TAD_FINE variable analog delays. All three delay options are independent and can be used in conjunction. All clocks within the device are shifted by the programmed t_{AD} adjust amount, which results in a shift of the timing of the LVDS data interface and affects the capture of SYSREF.

Table 6-4. t_{AD} Adjust Adjustment Ranges

ADJUSTMENT PARAMETER	ADJUSTMENT STEP	DELAY SETTINGS	MAXIMUM DELAY
TAD_INV	$1 / (f_{CLK} \times 2)$	1	$1 / (f_{CLK} \times 2)$
TAD_COARSE	See $t_{TAD(STEP)}$ in the *Section 5.11* table	256	See $t_{TAD(MAX)}$ in the *Section 5.11* table
TAD_FINE	See $t_{TAD(STEP)}$ in the *Section 5.11* table	256	See $t_{TAD(MAX)}$ in the *Section 5.11* table

To maintain timing alignment between converters, stable and matched power-supply voltages and device temperatures must be provided.

Aperture delay adjustment can be changed on-the-fly during normal operation, however changing the aperture delay also shifts the clock for the LVDS data interface (DxCLK±, DxSTR±, and Dx[11:0]±). The receiving circuit must be tolerant of shifts in the LVDS data timing. Use of the TAD_RAMP feature may help the receiver avoid loss of synchronization; see the *Section 6.3.4.2* section.

6.3.4.2 Aperture Delay Ramp Control (TAD_RAMP)

The ADC12DLx500 contains a function to gradually adjust the t_{AD} adjust setting towards the newly written TAD_COARSE value. This functionality allows the t_{AD} adjust setting to be adjusted with minimal internal clock circuitry glitches. The TAD_RAMP_RATE parameter allows either a slower (one TAD_COARSE LSB per 256 t_{CLK} cycles) or faster ramp (four TAD_COARSE LSBs per 256 t_{CLK} cycles) to be selected. The TAD_RAMP_EN parameter enables the ramp feature and any subsequent writes to TAD_COARSE to initiate a new ramp.

6.3.4.3 SYSREF Capture for Multi-Device Synchronization and Deterministic Latency

The clocking subsystem is largely responsible for achieving multi-device synchronization and deterministic latency. The SYSREF signal must be captured by a deterministic device clock (CLK±) edge at each system power-on and at each device in the system. This requirement imposes setup and hold constraints on SYSREF relative to CLK±, which can be difficult to meet at giga-sample clock rates over all system operating conditions. The ADC12DLx500 includes a number of features to simplify this synchronization process and to relax system timing constraints:

- The ADC12DLx500 uses dual-edge sampling (DES) in single-channel mode to reduce the CLK± input frequency by half and double the timing window for SYSREF (see Table 6-3)
- A SYSREF position detector (relative to CLK±) and selectable SYSREF sampling position aid in meeting setup and hold times over all conditions; see the *Section 6.3.4.3.1* section

- Easy-to-use automatic SYSREF calibration uses the aperture timing adjust block (t_{AD} adjust) to shift the ADC sampling instance based on the phase of SYSREF (rather than adjusting SYSREF based on the phase of the ADC sampling instance); see the *Section 6.3.4.3.2* section

6.3.4.3.1 SYSREF Position Detector and Sampling Position Selection (SYSREF Windowing)

The SYSREF windowing block is used to first detect the position of SYSREF relative to the CLK± rising edge and then to select a desired SYSREF sampling instance, which is a delay version of CLK±, to maximize setup and hold timing margins. In many cases a single SYSREF sampling position (SYSREF_SEL) is sufficient to meet timing for all systems (device-to-device variation) and conditions (temperature and voltage variations). However, this feature can also be used by the system to expand the timing window by tracking the movement of SYSREF as operating conditions change or to remove system-to-system variation at production test by finding a unique optimal value at nominal conditions for each system.

This section describes proper usage of the SYSREF windowing block. First, apply the device clock and SYSREF to the device. The location of SYSREF relative to the device clock cycle is determined and stored in the SYSREF_POS bits of the SYSREF capture position register. Each bit of SYSREF_POS represents a potential SYSREF sampling position. If a bit in SYSREF_POS is set to 1, then the corresponding SYSREF sampling position has a potential setup or hold violation. Upon determining the valid SYSREF sampling positions (the positions of SYSREF_POS that are set to 0) the desired sampling position can be chosen by setting SYSREF_SEL in clock control register 0 to the value corresponding to that SYSREF_POS position. In general, the middle sampling position between two setup and hold instances is chosen. Ideally, SYSREF_POS and SYSREF_SEL are performed at the nominal operating conditions of the system (temperature and supply voltage) to provide maximum margin for operating condition variations. This process can be performed at final test and the optimal SYSREF_SEL setting can be stored for use at every system power up. Further, SYSREF_POS can be used to characterize the skew between CLK± and SYSREF± over operating conditions for a system by sweeping the system temperature and supply voltages. For systems that have large variations in CLK± to SYSREF± skew, this characterization can be used to track the optimal SYSREF sampling position as system operating conditions change. In general, a single value can be found that meets timing over all conditions for well-matched systems, such as those where CLK± and SYSREF± come from a single clocking device.

Note

SYSREF_SEL must be set to 0 when using automatic SYSREF calibration; see the *Section 6.3.4.3.2* section.

The step size between each SYSREF_POS sampling position can be adjusted using SYSREF_ZOOM. When SYSREF_ZOOM is set to 0, the delay steps are coarser. When SYSREF_ZOOM is set to 1, the delay steps are finer. See the *Section 5.11* table for delay step sizes when SYSREF_ZOOM is enabled and disabled. In general, SYSREF_ZOOM is recommended to always be used (SYSREF_ZOOM = 1) unless a transition region (defined by 1's in SYSREF_POS) is not observed, which can be the case for low clock rates. Bits 0 and 23 of SYSREF_POS are always be set to 1 because there is insufficient information to determine if these settings are close to a timing violation, although the actual valid window can extend beyond these sampling positions. The value programmed into SYSREF_SEL is the decimal number representing the desired bit location in SYSREF_POS. Table 6-5 lists some example SYSREF_POS readings and the optimal SYSREF_SEL settings. Although 24 sampling positions are provided by the SYSREF_POS status register, SYSREF_SEL only allows selection of the first 16 sampling positions, corresponding to SYSREF_POS bits 0 to 15. The additional SYSREF_POS status bits are intended only to provide additional knowledge of the SYSREF valid window. In general, lower values of SYSREF_SEL are selected because of delay variation over supply voltage; however, in the fourth example a value of 15 provides additional margin and can be selected instead.

Table 6-5. Examples of SYSREF_POS Readings and SYSREF_SEL Selections

SYSREF_POS[23:0]			OPTIMAL SYSREF_SEL SETTING
0x02E[7:0] (Largest Delay)	0x02D[7:0][(1)]	0x02C[7:0][(1)] (Smallest Delay)	
b10000000	b01100000	b00011001	8 or 9

Table 6-5. Examples of SYSREF_POS Readings and SYSREF_SEL Selections (continued)

SYSREF_POS[23:0]			OPTIMAL SYSREF_SEL SETTING
0x02E[7:0] (Largest Delay)	0x02D[7:0][(1)]	0x02C[7:0][(1)] (Smallest Delay)	
b10011000	b00000000	b00110001	12
b10000000	b01100000	b0 0000001	6 or 7
b10000000	b00000011	b00000001	4 or 15
b10001100	b01100011	b00011001	6

(1) Red coloration indicates the bits that are selected, as given in the last column of this table.

6.3.4.3.2 Automatic SYSREF Calibration

The ADC12DLx500 has an automatic SYSREF calibration feature to alleviate the often challenging setup and hold times associated with capturing SYSREF for giga-sample data converters. Automatic SYSREF calibration uses the t_{AD} adjust feature to shift the device clock to maximize the SYSREF setup and hold times or to align the sampling instance based on the SYSREF rising edge.

The ADC12DLx500 must have a proper device clock applied and be programmed for normal operation before starting the automatic SYSREF calibration. When ready to initiate automatic SYSREF calibration, a continuous SYSREF signal must be applied. SYSREF must be a continuous (periodic) signal when using the automatic SYSREF calibration. Start the calibration process by setting SRC_EN high in the SYSREF calibration enable register after configuring the automatic SYSREF calibration using the SRC_CFG register. Upon setting SRC_EN high, the ADC12DLx500 searches for the optimal t_{AD} adjust setting until the device clock falling edge is internally aligned to the SYSREF rising edge. SRC_DONE in the SYSREF calibration status register is monitored to make sure the SYSREF calibration has finished. By aligning the device clock falling edge with the SYSREF rising edge, automatic SYSREF calibration maximizes the internal SYSREF setup and hold times relative to the device clock, and also sets the sampling instant based on the SYSREF rising edge. After the automatic SYSREF calibration finishes, the rest of the start up procedure can be performed to finish bringing up the system.

For multi-device synchronization, the SYSREF rising edge timing must be matched at all devices and therefore trace lengths must be matched from a common SYSREF source to each ADC12DLx500. Any skew between the SYSREF rising edge at each device results in additional error in the sampling instance between devices, however repeatable deterministic latency from system start up to start up through each device must still be achieved.

Figure 6-3 provides a timing diagram of the SYSREF calibration procedure. The optimized setup and hold times are shown as $t_{SU(OPT)}$ and $t_{H(OPT)}$, respectively. The device clock and SYSREF are referred to as *internal* in this diagram because the phase of the internal signals are aligned within the device and not to the external (applied) phase of the device clock or SYSREF.

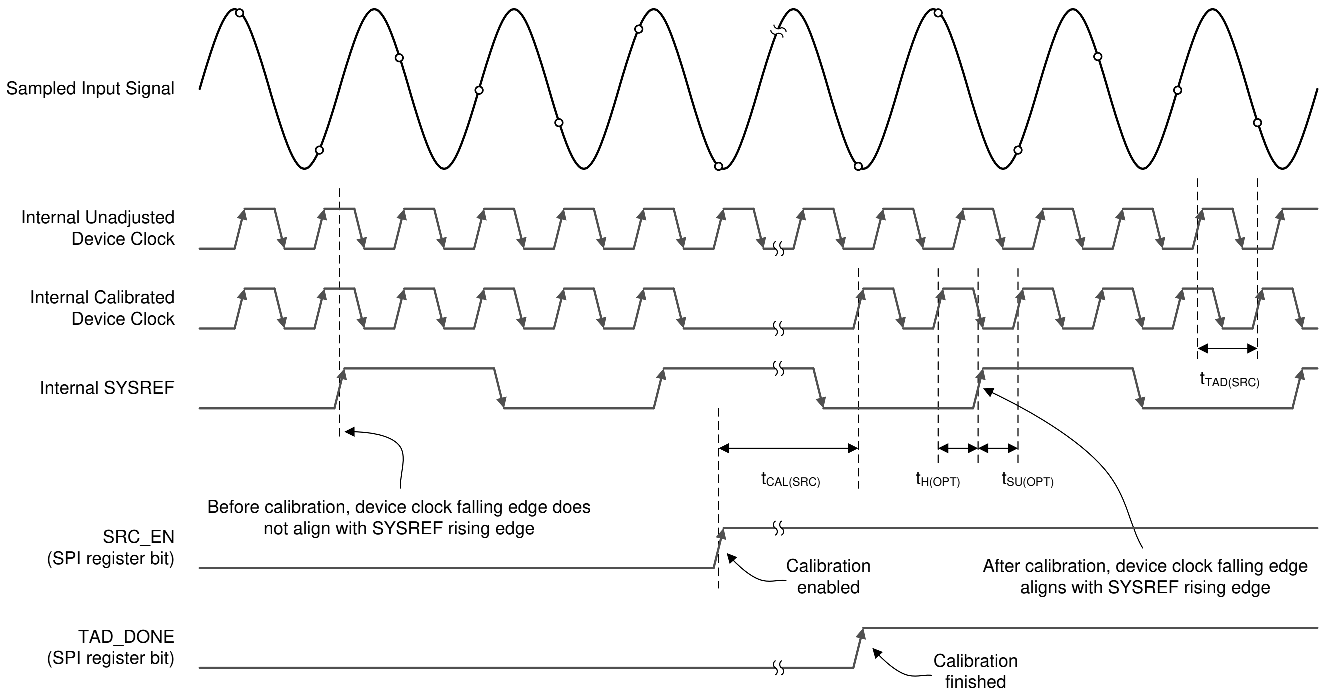


Figure 6-3. SYSREF Calibration Timing Diagram

When finished, the t_{AD} adjust setting found by the automatic SYSREF calibration can be read from SRC_TAD in the SYSREF calibration status register. After calibration, the system continues to use the calibrated t_{AD} adjust setting for operation until the system is powered down. However, if desired, the SYSREF calibration can then be disabled and the t_{AD} adjust setting can be fine-tuned according to the systems needs. Alternatively, the use of the automatic SYSREF calibration can be done at product test (or periodic recalibration) of the optimal t_{AD} adjust setting for each system. This value can be stored and written to the TAD register (TAD_INV, TAD_COARSE, and TAD_FINE) upon system start up.

Do not run the SYSREF calibration when the ADC calibration is running. SYSREF_SEL in the clock control register 0 must be set to 0 when using SYSREF calibration.

SYSREF calibration searches the TAD_COARSE delays using both noninverted (TAD_INV = 0) and inverted clock polarity (TAD_INV = 1) to minimize the required TAD_COARSE setting to minimize loss on the clock path to reduce aperture jitter (t_{AJ}).

6.3.5 LVDS Digital Interface

The ADC12DLx500 uses a low-voltage differential signaling (LVDS) interface to output the digital samples. This interface offers simplicity in its implementation compared to serialized interfaces and provides low latency for latency-sensitive applications. The interface uses up to 48 data pairs, four DDR clocks, and four strobe signals arranged in four 12-bit data buses. Strobe signals simplify synchronization across buses and synchronization between multiple devices. The strobe can be generated internally or mirrored from the TMSTP± or SYSREF± inputs. Flexible strobe configurations allow tradeoffs in reliability or number of LVDS pairs and the on-the-fly use of strobe is SPI or pin selectable.

Digital interface scrambling is available to avoid spurious noise generated by the digital interface from leaking into the ADC samples. The receiver must undo the scrambling operation to extract the proper digital samples (see the *Section 6.4.5.5* section) when used. Scrambling is optional.

6.3.5.1 Multi-Device Synchronization and Deterministic Latency Using Strobes

The ADC12DLx500 is able to achieve multi-device synchronization through deterministic latency across the LVDS interface. First, SYSREF is issued to all devices as a known timing reference for synchronization. SYSREF resets internal clock dividers and the strobe generation block within the ADC12DLx500. The

ADC12DLx500 issues strobe signals across each bus of the interface to provide timing information to the receiver. The receiver uses this timing information to achieve fixed latency and for alignment among multiple ADC12DLx500 devices. The strobe generator block provides internal generation of a repeating strobe signal to reflect the end of a data *frame*. The generated strobe can be sent across the interface using a dedicated LVDS pair (DxSTR±) or as a replacement of the sample LSB with the strobe. Strobe generation can be controlled by the $\overline{\text{SYNC}}$ signal through the SPI or by using the $\overline{\text{SYNCSE}}$ or TMSTP± inputs (see SYNC_SEL in the LCTRL register). In all modes, the strobe output can be treated as a data pair with the same timing as the data outputs (Dx[11:0]±) that is source-synchronous with the associated data clock (DxCLK±).

The strobe generator sets the last unit interval (UI) of a frame high to signal the end of a frame. Frame length is programmable through the LFRAME register. The SYSREF input marks the start of a frame and, if run periodically, then the SYSREF period must be an integer number of frames long.

6.3.5.1.1 Dedicated Strobe Pins

Dedicated strobe pins are recommended for applications with robust requirements. Each LVDS bus has a dedicated strobe (DxSTR±), up to four total, which is source synchronous to its associated data clock (DxCLK±). The strobe can run continuously or can be enabled and disabled as needed. When enabled, this mode allows the data bus to still send all 12 bits of the digital samples for highest performance. The tradeoff is that more pins are needed, two per LVDS bus, for up to eight total pins when operating in DMUX-by-2 mode. Table 6-6 describes the strobe output. The $\overline{\text{SYNC}}$ signal is not required to output the dedicated strobe signal.

Table 6-6. Strobe Output for Dedicated Strobe Pins

FRAME SAMPLE NUMBER (UI)	1 FRAME (LFRAME = 0x08)							
	0	1	2	3	4	5	6	7
Dx[11:0]	S0[11:0]	S1[11:0]	S2[11:0]	S3[11:0]	S4[11:0]	S5[11:0]	S6[11:0]	S7[11:0]
DxSTR	0	0	0	0	0	0	0	1

6.3.5.1.2 Reduced Width Interface With Dedicated Strobe Pins

In four LVDS output modes (see Table 6-11), the data clock (DxCLK±) and strobe (DxSTR±) for LVDS buses C and D can be disabled to reduce the total number of LVDS pins by eight. In this mode, the LVDS bus A data clock (DACLK±) and strobe (DASTR±) can be used with the data from bus C and the same signals for bus B can be used for LVDS bus D. The tradeoff is that digital interface timing may become more difficult. See the *Section 6.4.5.3* and *Section 6.4.5.4* sections.

6.3.5.1.3 LSB Replacement With a Strobe

The strobe signals can also be output over the LSB of the digital sample for each LVDS bus. During transmission of the strobe the LSB of the sample is replaced by the strobe signal and, therefore, the digital sample is only 11 bits wide resulting in a small loss in ENOB. When the strobe is disabled, all 12 bits of the digital sample are sent across the interface for full performance. The strobe can be enabled periodically, allowing a tradeoff in ENOB and robustness and reducing the interface width. Enable this mode by setting SYNC_PAT in the PAT_SEL register to 0x2. Transmission of the strobe is controlled by the source selected by SYNC_SEL in the LCTRL register. The $\overline{\text{SYNCSE}}$ pin controls transmission of the strobe by default. Table 6-7 describes the strobe output when the LSB is replaced with the strobe signal data when $\overline{\text{SYNC}}$ is asserted. Table 6-8 describes the strobe output when the active pattern is used ($\overline{\text{SYNC}}$ de-asserted).

Table 6-7. Sync Pattern Output for LSB Replacement With Strobe ($\overline{\text{SYNC}}$ Asserted)

FRAME SAMPLE NUMBER (UI)	1 FRAME (LFRAME = 0x08)							
	0	1	2	3	4	5	6	7
Dx[11:1]	S0[11:1]	S1[11:1]	S2[11:1]	S3[11:1]	S4[11:1]	S5[11:1]	S6[11:1]	S7[11:1]
Dx0 (LSB)	0	0	0	0	0	0	0	1

Table 6-8. Active Pattern Output for LSB Replacement With Strobe ($\overline{\text{SYNC}}$ De-Asserted)

FRAME SAMPLE NUMBER (UI)	1 FRAME (LFRAME = 0x08)							
	0	1	2	3	4	5	6	7
Dx[11:1]	S0[11:1]	S1[11:1]	S2[11:1]	S3[11:1]	S4[11:1]	S5[11:1]	S6[11:1]	S7[11:1]
Dx0 (LSB)	S0[0]	S1[0]	S2[0]	S3[0]	S4[0]	S5[0]	S6[0]	S7[0]

6.3.5.1.4 Strobe Over All Data Pairs

The strobe signal can also be output over all LVDS lanes. During transmission of the strobe, the entire sample is replaced by the strobe signal and therefore the sampled data are lost. When the strobe is disabled, all 12 bits of the digital sample are sent across the interface for full performance. The strobe can be enabled periodically to make sure synchronization is maintained only if loss of digital samples is allowed by the application. Enable this mode by setting SYNC_PAT in the PAT_SEL register to 0x3. Transmission of the strobe pattern is controlled by the source selected by SYNC_SEL in the LCTRL register. The $\overline{\text{SYNCSE}}$ pin controls transmission of the strobe pattern by default. Table 6-9 describes the strobe output when the strobe signal is output over all data pairs when $\overline{\text{SYNC}}$ is asserted. Table 6-10 describes the strobe output when the active pattern is used ($\overline{\text{SYNC}}$ de-asserted).

Table 6-9. Sync Pattern Output for Strobe Over All Data Pairs ($\overline{\text{SYNC}}$ Asserted)

FRAME SAMPLE NUMBER (UI)	1 FRAME (LFRAME = 0x08)							
	0	1	2	3	4	5	6	7
Dx[11:0]	0x000	0x000	0x000	0x000	0x000	0x000	0x000	0xFFF
DxSTR (if enabled)	0	0	0	0	0	0	0	1

Table 6-10. Active Pattern Output for Strobe Over All Data Pairs ($\overline{\text{SYNC}}$ De-Asserted)

FRAME SAMPLE NUMBER (UI)	1 FRAME (LFRAME = 0x08)							
	0	1	2	3	4	5	6	7
Dx[11:0]	S0[11:0]	S1[11:0]	S2[11:0]	S3[11:0]	S4[11:0]	S5[11:0]	S6[11:0]	S7[11:0]
DxSTR (if enabled)	0	0	0	0	0	0	0	1

6.3.6 Alarm Monitoring

Built-in alarms are available to monitor internal events. Two types of alarms and upsets are detected by this feature:

1. SYSREF caused internal clocks to be realigned
2. An upset that affects the internal clocks

When an alarm occurs, a bit for each specific alarm is set in ALM_STATUS. Each alarm bit remains set until the host system writes a 1 to clear it. If the alarm type is not masked (see the ALM_MASK register), then the alarm is also indicated by the ALARM register. The CALSTAT output pin can be configured as an alarm output that goes high when an alarm occurs. See CAL_STATUS_SEL in the CAL_PIN_CFG register.

6.3.6.1 Clock Upset Detection

The CLK_ALM register bit indicates if the internal clocks may have been upset. The clocks in channel A are continuously compared to channel B. If these clocks differ for even one DEVCLK / 2 cycle, the CLK_ALM register bit is set and remains set until cleared by the host system by writing a 1. For the CLK_ALM register bit to function properly, follow this usage model:

1. Program LVDS_EN = 0
2. Make sure the device is configured to use both channels (PD_ACH = 0, PD_BCH = 0)
3. Program LVDS_EN = 1
4. Write CLK_ALM = 1 to clear CLK_ALM
5. Monitor the CLK_ALM status bit or the CALSTAT output pin if CAL_STATUS_SEL is properly configured
6. When exiting global power-down (via MODE in the DEVICE_CONFIG register or via the PD pin), the CLK_ALM status bit can be set and must be cleared by writing a 1 to CLK_ALM

6.3.7 Temperature Monitoring Diode

A built-in thermal monitoring diode is available on the TDIODE+ and TDIODE– pins. This diode facilitates temperature monitoring and characterization of the device in higher ambient temperature environments. Although the on-chip diode is not highly characterized, the diode can be used effectively by performing a baseline measurement (offset) at a known ambient or board temperature and creating a linear equation with the diode voltage slope provided in the *Electrical Characteristics: DC Specifications* table. Perform offset measurement with the device unpowered or with the PD pin asserted to minimize device self-heating. Recommended monitoring devices include the LM95233 device and similar remote-diode temperature monitoring products from Texas Instruments.

6.3.8 Analog Reference Voltage

The reference voltage for the ADC12DLx500 is derived from an internal band-gap reference. A buffered version of the reference voltage is available at the BG pin for convenience. This output has an output-current capability of ±100 µA. The BG output must be buffered if more current is required. No provision exists for the use of an external reference voltage, but the full-scale input voltage can be adjusted through the full-scale-range register settings. In unique cases, the VA11 supply voltage can act as the reference voltage by setting BG_BYPASS (see the internal reference bypass register).

6.4 Device Functional Modes

The ADC12DLx500 can be configured to operate in a number of functional modes. These modes are described in this section.

6.4.1 Dual-Channel Mode (Non-DES Mode)

The ADC12DLx500 can be used as a dual-channel ADC where the sampling rate is equal to the clock frequency (f_S = f_{CLK}) provided at the CLK+ and CLK– pins. The two inputs, AIN± and BIN±, serve as the respective inputs for each channel in this mode. This mode is chosen simply by setting DES_EN to 0. The analog inputs can be swapped by setting DUAL_INPUT (see the input mux control register).

6.4.2 Internal Dither Modes

Dither can be disabled by setting ADC_DITH_EN to 0 in the ADC_DITH register, which can result in a slight improvement in SNR. The amount of dither can be increased by setting ADC_DITH_AMP to 1. The increased dither can result in further spurious improvements, but can also result in a reduction in SNR. Certain dither values, caused by device-to-device variations, can result in rounding errors that can either reduce SNR or reduce fixed spur performance (DC, f_S / 4, and f_S / 2 spurs). The choice of tradeoff can be made by setting ADC_DITH_ERR to 0 to degrade SNR and 1 to degrade the DC, f_S / 4 (single-channel mode only), and f_S / 2 spurs.

6.4.3 Single-Channel Mode (DES Mode)

The ADC12DLx500 can also be used as a single-channel ADC where the sampling rate is equal to two times the clock frequency (f_S = 2 × f_{CLK}) provided at the CLK+ and CLK– pins. This mode effectively interleaves the two ADC channels together to form a single-channel ADC at twice the sampling rate. This mode is chosen simply by setting DES_EN to 1. Either analog input, INA± or INB±, can serve as the input to the ADC. ADC trim settings are automatically adjusted based on the chosen input. The analog input can be selected using SINGLE_INPUT (see the input mux control register).

6.4.4 LVDS Output Driver Modes

The LVDS output drivers can be configured for various swings, terminations and output common-mode levels to meet the needs of different receivers. The swing can be adjusted between high swing (default) and low swing mode to save power by setting LVDS_SWING to 0x1. Also, power savings can be gained by choosing the high-Z termination mode by setting LVDS_SWING to 0x3. Only use high-Z termination mode with short transmission lines and for receivers with high-Z termination. The common-mode voltage is adjusted by adjusting the VLVDS supply voltage. The output common-mode voltage roughly tracks the VLVDS supply voltage by V_{OCM} = V_{LVDS} – 0.6V.

6.4.5 LVDS Output Modes

The LVDS output buses can be configured to demux the output data from each ADC channel by one or two by setting the LDEMUX parameter. When a demux-by-2 option is selected (LDEMUX = 1), the number of output strobes and data clocks can be reduced by using LCS_EN. The two channels of the ADC12DLx500 can be interleaved together to achieve double the sample rate (that is, single-channel mode) by setting DES_EN to 1. Table 6-11 lists the available interface and configuration modes. When the LSB replacement with strobe option is used (SYNC_PAT = 0x2), the strobe column of Table 6-11 can be ignored and replaced with 0 because all dedicated strobe outputs can be disabled.

Table 6-11. LVDS Output Modes

LVDS OUTPUT MODE	USER-PROGRAMMED VALUES			DATA PAIRS	DATA CLOCKS	STROBES	ALLOWED f_S RANGE (MSPS)	ALLOWED f_{CLK} RANGE (MHz)	TIMING DIAGRAM
	DES_EN	LDEMUX	LALIGNED						
Single channel, 2 LVDS buses, staggered data	1	0	0	24	2	2	1000–2500	500–1250	Figure 5-4
Single channel, 2 LVDS buses, aligned data	1	0	1	24	2	2	1000–2500	500–1250	Figure 5-5
Single channel, 4 LVDS buses, staggered data	1	1	0	48	4	4	1000–5000	500–2500	Figure 5-6
Single channel, 4 LVDS buses, aligned data	1	1	1	48	4	4	1000–5000	500–2500	Figure 5-7
Dual channel, 2 LVDS buses	0	0	0 or 1	24	2	2	500–1500	500–1500	Figure 5-1
Dual channel, 4 LVDS buses, staggered data	0	1	0	48	4	4	500–2500	500–2500	Figure 5-2
Dual channel, 4 LVDS buses, aligned data	0	1	1	48	4	4	500–2500	500–2500	Figure 5-3

6.4.5.1 Staggered Output Mode

Setting LALIGNED to 0 results in the LVDS output buses being staggered in time. Staggering the output buses causes an LVDS output switching event to occur at each sampling instance and may result in better spurious performance than what is described in the *Section 6.4.5.2* section. Table 6-11 provides links to the timing diagrams for staggered output mode.

6.4.5.2 Aligned Output Mode

Setting LALIGNED to 1 results in the LVDS outputs buses being aligned in time, meaning that all buses switch at the same time. The switching instance is a sub-harmonic of the sampling clock and may result in additional spurs in the output spectrum as compared to the *Section 6.4.5.1* section. Table 6-11 provides links to the timing diagrams for aligned output mode.

6.4.5.3 Reducing the Number of Strobes

One strobe is provided for each LVDS bus; however, the number of output strobes can either be reduced or the strobes can be disabled altogether. Typical use cases for reduced strobes include sharing a single strobe among multiple buses or implementing a receiver that does not have a FIFO that needs to be synchronized by the strobes. STBx_EN in the LCS_EN register can be used to disable any unused strobe outputs.

6.4.5.4 Reducing the Number of Data Clocks

One data clock is provided for each LVDS bus; however, the number of data clocks used in the system can be reduced. The number of data clocks can be reduced if a data clock is shared among multiple buses, which can be applicable at lower data rates. DCLKx_EN in the LCS_EN register can be used to disable any unused data clock outputs.

6.4.5.5 Scrambling

The LVDS outputs can be scrambled in order to reduce spectral peaks in the output data, especially for repeating patterns. Spectral peaks can couple back to the ADC analog input and result in degraded noise or spurious performance in the ADC output data. Enable scrambling by setting SCR in the LCTRL register. The scrambler does not require any memory (only uses the current sample) and uses simple XOR operations in order to minimize latency. Scrambling does require the two LSBs of each sample to be random (as is the case for ADC input thermal noise), but also works when the LSB is used as a strobe or timestamp. The scrambler is enabled by setting SCR in the LCTRL register to 1. The scrambling operation changes slightly depending on the LWIDTH parameter, as Table 6-12 to Table 6-15 describes. Each table also describes the descrambling operation that the receiving device must implement in order to recover the original samples. In Table 6-12 to Table 6-15, d[x] corresponds to bit x of the unscrambled digitized ADC sample at LVDS bus q (q = A, B, C, or D) before scrambling and y[k] corresponds to the scrambled bit k output from the interface over data pair Dqk±. Likewise, strobe is the unscrambled strobe signal at the LVDS bus q (q = A, B, C, or D) and strobe_y is the scrambled strobe output on data pair DqSTR±. The ⊕ symbol denotes the bitwise XOR operation.

Table 6-12. Scrambling and Descrambling Operations (12-Bit Mode, LWIDTH = 0x0)

SCRAMBLER	DESCRAMBLER
y[11] = d[11] ⊕ d[1] ⊕ d[0]	d[11] = y[11] ⊕ y[0]
y[10] = d[10] ⊕ d[1] ⊕ d[0]	d[10] = y[10] ⊕ y[0]
y[9] = d[9] ⊕ d[1] ⊕ d[0]	d[9] = y[9] ⊕ y[0]
y[8] = d[8] ⊕ d[1] ⊕ d[0]	d[8] = y[8] ⊕ y[0]
y[7] = d[7] ⊕ d[1] ⊕ d[0]	d[7] = y[7] ⊕ y[0]
y[6] = d[6] ⊕ d[1] ⊕ d[0]	d[6] = y[6] ⊕ y[0]
y[5] = d[5] ⊕ d[1] ⊕ d[0]	d[5] = y[5] ⊕ y[0]
y[4] = d[4] ⊕ d[1] ⊕ d[0]	d[4] = y[4] ⊕ y[0]
y[3] = d[3] ⊕ d[1] ⊕ d[0]	d[3] = y[3] ⊕ y[0]
y[2] = d[2] ⊕ d[1] ⊕ d[0]	d[2] = y[2] ⊕ y[0]
y[1] = d[1]	d[1] = y[1]
y[0] = d[0] ⊕ d[1]	d[0] = y[0] ⊕ y[1]
strobe_y = strobe ⊕ d[1] ⊕ d[0]	strobe = strobe_y ⊕ y[0]

Table 6-13. Scrambling and Descrambling Operations (11-Bit Mode, LWIDTH = 0x1)

SCRAMBLER	DESCRAMBLER
y[11] = d[11] ⊕ d[2] ⊕ d[1]	d[11] = y[11] ⊕ y[1]
y[10] = d[10] ⊕ d[2] ⊕ d[1]	d[10] = y[10] ⊕ y[1]
y[9] = d[9] ⊕ d[2] ⊕ d[1]	d[9] = y[9] ⊕ y[1]
y[8] = d[8] ⊕ d[2] ⊕ d[1]	d[8] = y[8] ⊕ y[1]
y[7] = d[7] ⊕ d[2] ⊕ d[1]	d[7] = y[7] ⊕ y[1]
y[6] = d[6] ⊕ d[2] ⊕ d[1]	d[6] = y[6] ⊕ y[1]
y[5] = d[5] ⊕ d[2] ⊕ d[1]	d[5] = y[5] ⊕ y[1]
y[4] = d[4] ⊕ d[2] ⊕ d[1]	d[4] = y[4] ⊕ y[1]
y[3] = d[3] ⊕ d[2] ⊕ d[1]	d[3] = y[3] ⊕ y[1]
y[2] = d[2]	d[2] = y[2]
y[1] = d[2] ⊕ d[1]	d[1] = y[2] ⊕ y[1]
y[0] = d[2] ⊕ d[1] ⊕ d[0](1)	d[0] = y[1] ⊕ y[0](1)
strobe_y = strobe ⊕ d[1] ⊕ d[0]	strobe = strobe_y ⊕ y[1]

(1) Only used if LSB_SEL in the LSB_SEL register is set to 0 and TIME_STAMP_EN is set to 1.

Table 6-14. Scrambling and Descrambling Operations (10-Bit Mode, LWIDTH = 0x2)

SCRAMBLER	DESCRAMBLER
y[11] = d[11] ⊕ d[3] ⊕ d[2]	d[11] = y[11] ⊕ y[2]
y[10] = d[10] ⊕ d[3] ⊕ d[2]	d[10] = y[10] ⊕ y[2]
y[9] = d[9] ⊕ d[3] ⊕ d[2]	d[9] = y[9] ⊕ y[2]
y[8] = d[8] ⊕ d[3] ⊕ d[2]	d[8] = y[8] ⊕ y[2]

Table 6-14. Scrambling and Descrambling Operations (10-Bit Mode, LWIDTH = 0x2) (continued)

SCRAMBLER	DESCRAMBLER
y[7] = d[7] ⊕ d[3] ⊕ d[2]	d[7] = y[7] ⊕ y[2]
y[6] = d[6] ⊕ d[3] ⊕ d[2]	d[6] = y[6] ⊕ y[2]
y[5] = d[5] ⊕ d[3] ⊕ d[2]	d[5] = y[5] ⊕ y[2]
y[4] = d[4] ⊕ d[3] ⊕ d[2]	d[4] = y[4] ⊕ y[2]
y[3] = d[3]	d[3] = y[3]
y[2] = d[2] ⊕ d[3]	d[2] = y[2] ⊕ y[3]
y[1] = 0 (not used)	d[1] = 0 (not used)
y[0] = d[0] ⊕ d[3] ⊕ d[2](1)	d[0] = y[0] ⊕ y[2](1)
strobe_y = strobe ⊕ d[3] ⊕ d[2]	strobe = strobe_y ⊕ y[2]

(1) Only used if LSB_SEL in the LSB_SEL register is set to 0 and TIME_STAMP_EN is set to 1.

Table 6-15. Scrambling and Descrambling Operations (8-Bit Mode, LWIDTH = 0x3)

SCRAMBLER	DESCRAMBLER
y[11] = d[11] ⊕ d[5] ⊕ d[4]	d[11] = y[11] ⊕ y[4]
y[10] = d[10] ⊕ d[5] ⊕ d[4]	d[10] = y[10] ⊕ y[4]
y[9] = d[9] ⊕ d[5] ⊕ d[4]	d[9] = y[9] ⊕ y[4]
y[8] = d[8] ⊕ d[5] ⊕ d[4]	d[8] = y[8] ⊕ y[4]
y[7] = d[7] ⊕ d[5] ⊕ d[4]	d[7] = y[7] ⊕ y[4]
y[6] = d[6] ⊕ d[5] ⊕ d[4]	d[6] = y[6] ⊕ y[4]
y[5] = d[5]	d[5] = y[5]
y[4] = d[4] ⊕ d[5]	d[4] = y[4] ⊕ y[5]
y[3] = 0 (not used)	d[3] = 0 (not used)
y[2] = 0 (not used)	d[2] = 0 (not used)
y[1] = 0 (not used)	d[1] = 0 (not used)
y[0] = d[0] ⊕ d[5] ⊕ d[4](1)	d[0] = y[0] ⊕ y[4](1)
strobe_y = strobe ⊕ d[5] ⊕ d[4]	strobe = strobe_y ⊕ y[4]

(1) Only used if LSB_SEL in the LSB_SEL register is set to 0 and TIME_STAMP_EN is set to 1.

6.4.5.6 Digital Interface Test Patterns and LVSD $\overline{\text{SYNC}}$ Functionality

A number of device test patterns are available. These modes insert known patterns into the device data path for assistance with system debug, development, or characterization. The test patterns can also be used during system power-up to synchronize the digital interface logic in the receiving device. Two patterns are available at any time, and are referred to as the active pattern and the sychronization pattern. Toggling between the two patterns is controlled by the source selected by SYNC_SEL in the LCTRL register. Selecting the active pattern or synchronization pattern is controlled by the $\overline{\text{SYNCSE}}$ pin by default. The pattern always changes state on a frame boundary (falling edge of the strobe).

6.4.5.6.1 Active Pattern

The active pattern is chosen by setting ACT_PAT in the PAT_SEL register. The available active patterns are given below:

- Digitized samples from the ADC (normal operation)
- All LVDS lanes output the user-defined pattern (see the *Section 6.4.5.6.3* section)

6.4.5.6.2 Synchronization Pattern

The synchronization pattern is chosen by setting SYNC_PAT in the PAT_SEL register. The available synchronization patterns are given below:

- All LVDS lanes transmit the user-defined pattern (see the *Section 6.4.5.6.3* section)

- Frame strobe is transmitted on the LSB of the digital samples of each active LVDS bus. The digitized samples (ADC output data) are still output on the other LVDS lanes.
- Frame strobe is transmitted on all active LVDS data lanes

6.4.5.6.3 User-Defined Test Pattern

A user-defined test pattern mode allows the user to define a pattern to meet various system needs. Example patterns included strobe patterns to look for inter-symbol interference issues, single-bit patterns to verify TX to RX lane connections, and multi-bit patterns to verify time alignment. The pattern is up to eight samples long and is programmed using the UPAT0 through UPAT7 registers. The user pattern repeats at the beginning of each frame. If the frame length is less than eight samples than the user pattern is truncated. If the frame length is greater than eight samples then the user pattern repeats until the end of the frame.

Additionally, there are controls to invert specific bits of the user-defined pattern for each of the LVDS buses to allow a unique pattern on each bus. UPAT_INV_x (x = A, B, C, or D) in the UPAT_CTRL register, as shown in Table 6-16, inverts the specified bit in each LVDS bus when set to 1. The inversion is independent of the other buses.

Table 6-16. UPAT_INV_x Control Definition

REGISTER CONTROL	LVDS BUS AFFECTED	LVDS BUS BIT INVERTED	BUS INVERSION MASK
UPAT_INV_A	A	8	0001 0000 0000
UPAT_INV_B	B	9	0010 0000 0000
UPAT_INV_C	C	10	0100 0000 0000
UPAT_INV_D	D	11	1000 0000 0000

A predefined pattern can also be selected by setting LANE_PAT in the UPAT_CTRL register to 1. LANE_PAT automatically overrides the programmed user pattern. LANE_PAT is a fixed eight sample sequence output on each LVDS bus. The pattern is 0x000, 0xFFF, 0x000, 0x000, 0x000, 0xFFF, 0xFFF, and 0xFFF. The repetition rules regarding frame length defined for the user pattern apply to the lane pattern as well.

6.4.6 Power-Down Modes

The PD input pin allows ADC12DLx500 devices to be entirely powered down. Power-down can also be controlled by MODE (see the device configuration register). The LVDS data output drivers are disabled when PD is high. When the device returns to normal operation, the LVDS interface must be re-established, which results in the ADC data pipeline containing meaningless information so the system must wait a sufficient time for the data to be flushed.

6.4.7 Calibration Modes and Trimming

The ADC12DLx500 has foreground calibration available. When foreground calibration is initiated the ADCs are automatically taken offline and the output data become mid-code (0x000 in 2's complement) while a calibration is occurring. Additional offset calibration features are available in foreground calibration mode. Further, a number of ADC parameters can be trimmed to optimize performance in a user system.

The ADC12DLx500 consists of a total of six sub-ADCs, each referred to as a *bank*, with two banks forming an ADC core. The banks sample out-of-phase so that each ADC core is two-way interleaved. The six banks form three ADC cores, referred to as ADC A, ADC B, and ADC C. In foreground calibration mode, ADC A samples INA± and ADC B samples INB± in dual-channel mode and both ADC A and ADC B sample INA± (or INB±) in single-channel mode.

Figure 6-4 shows a diagram of the calibration system including labeling of the banks that make up each ADC core. When calibration is performed, the linearity, gain, and offset voltage for each bank are calibrated to an internally generated calibration signal. The analog inputs can be driven during calibration except that when offset calibration (see CAL_OS in the CAL_CFG0 register) is used. There must be no signals (or aliased signals) near DC for proper estimation of the offset (see *Section 6.4.8*).

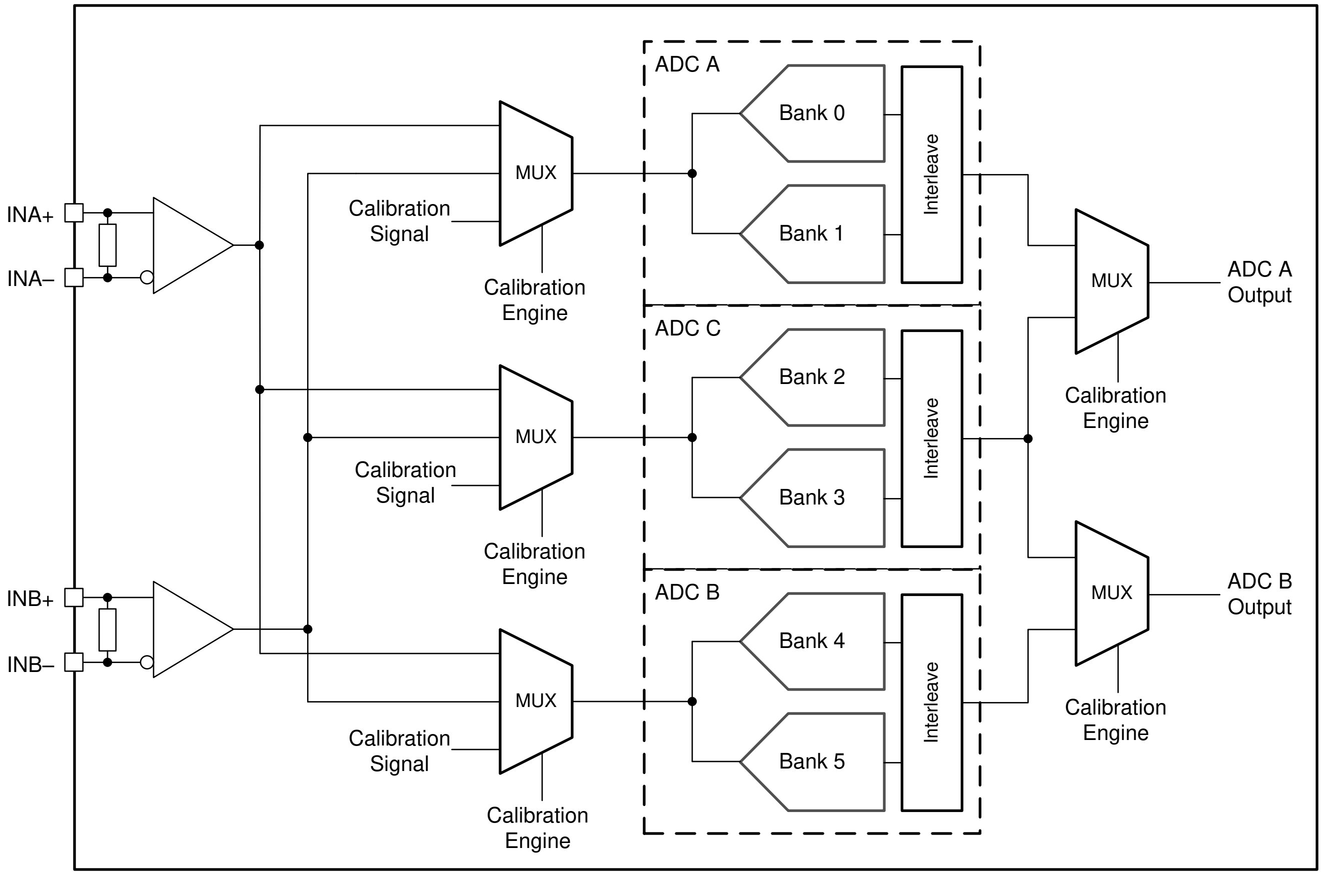


Figure 6-4. ADC12DLx500 Calibration System Block Diagram

In addition to calibration, a number of ADC parameters are user-controllable to provide trimming for optimal performance. These parameters include input offset voltage, ADC gain, interleaving timing, and input termination resistance. The default trim values are programmed at the factory to unique values for each device that are determined to be optimal at the test system operating conditions. The factory-programmed values can be read from the trim registers and adjusted as desired. The register fields that control the trimming are labeled according to the input that is being sampled (INA± or INB±), the bank that is being trimmed, or the ADC core that is being trimmed. Trim values are not expected to change as operating conditions change, however optimal performance can be obtained by doing so. Any custom trimming must be done on a per device basis because of process variations, meaning that there is no global optimal setting for all parts. See *Section 6.4.9* for information about the available trim parameters and associated registers.

6.4.7.1 Foreground Calibration Mode

Foreground calibration requires the ADC to stop converting the analog input signals during the procedure. Foreground calibration always runs on power-up and a sufficient period of time must elapse before programming the device to make sure the calibration is finished. Foreground calibration can be initiated by triggering the calibration engine. The trigger source can be either the CAL_TRIG pin or CAL_SOFT_TRIG (see the calibration software trigger register) and is chosen by setting CAL_TRIG_EN (see the calibration pin configuration register).

6.4.8 Offset Calibration

Foreground calibration mode inherently calibrates the offsets of the ADC cores; however, the input buffers sit outside of the calibration loop. Therefore, the offsets are not calibrated by the standard calibration process. In both dual-channel mode and single-channel mode, uncalibrated input buffer offsets result in a shift in the mid-code output (DC offset) with no input. Also, in single-channel mode, uncalibrated input buffer offsets can result in a fixed spur at f_S / 2. A separate calibration is provided to correct the input buffer offsets.

There must be no signals at or near DC or aliased signals that fall at or near DC to properly calibration the offsets. Requiring the system to make sure this condition during normal operation or have the ability to mute the input signal during calibration. Foreground offset calibration is enabled via CAL_OS and only performs the calibration one time as part of the foreground calibration procedure.

The offset calibration correction uses the input offset voltage trim registers (see *Section 6.4.9*) to correct the offset. When offset calibration is used, it must not be written by the user. The calibrated values can be read by reading the OADJ_x_FG0_VINy and OADJ_x_FG90_VINy registers, where x is the ADC core (A or B) and y is the input (INA± or INB±), after calibration is completed. Only read the values when FG_DONE is read as 1 when using foreground offset calibration (CAL_OS = 1).

6.4.9 Trimming

Table 6-17 lists the parameters that can be trimmed and the associated registers. Manual trimming is only allowed in foreground calibration mode.

Table 6-17. Trim Register Descriptions

TRIM PARAMETER	TRIM REGISTER	NOTES
Band-gap reference	BG_TRIM	Measurement on the BG output pin.
Input termination resistance	RTRIM_x, where x = A for INA± or B for INB±)	The device must be powered on with a clock applied.
Input offset voltage	OADJ_x_FG0_VINy and OADJ_A_FG90_VINy, where x = ADC core (A or B) and y = A for INA± or B for INB±	A different trim value is allowed for each ADC core (A or B) to allow trimming of the offsets as operating conditions change. OADJ_A_FG90_VINy is used to trim the offsets of ADC A in single-channel mode.
INA± and INB± gain	GAIN_TRIM_x, where x = A for INA± or B for INB±	Set FS_RANGE_A and FS_RANGE_B to default values before trimming the input. Use FS_RANGE_A and FS_RANGE_B to adjust the full-scale input voltage.
Bank gain trim	GAIN_Bx, where x = 0, 1, 2, or 3	Trims the gain of the individual ADC banks to improve gain matching between ADC cores.
INA± and INB± full-scale input voltage	FS_RANGE_x, where x = A for INA± or B for INB±	Full-scale input voltage adjustment for each input. The default value is effected by GAIN_TRIM_x (x = A or B). Trim GAIN_TRIM_x with FS_RANGE_x set to the default value. FS_RANGE_x can then be used to trim the full-scale input voltage.
Intra-ADC core timing (bank timing)	Bx_TIME_y, where x = bank number (0–5) and y = 0° or –90° clock phase	Trims the timing between the two banks of an ADC core (ADC A or B) for two clock phases, either 0° or –90°. The –90° clock phase is used by ADC A in single-channel mode only.
Inter-ADC core timing (dual-channel mode)	TADJ_A, TADJ_B	The suffix letter (A or B) indicates the ADC core that is being trimmed.
Inter-ADC core timing (single-channel mode)	TADJ_A_FG90, TADJ_B_FG0	The middle letter (A or B) indicates the ADC core that is being trimmed. The suffix of 0 or 90 indicates the clock phase applied to the ADC core. 0 indicates a 0° clock and is sampling in-phase with the clock input (applies to ADC B). 90 indicates a –90° clock and therefore is sampling out-of-phase with the clock input (applies to ADC A).

6.5 Programming

6.5.1 Using the Serial Interface

The serial interface is accessed using the following four pins: serial clock (SCLK), serial data input (SDI), serial data output (SDO), and serial-interface chip-select ($\overline{SCS}$). Register access is enabled through the $\overline{SCS}$ pin.

6.5.1.1 $\overline{SCS}$

This signal must be asserted low to access a register through the serial interface. Setup and hold times with respect to the SCLK must be followed.

6.5.1.2 SCLK

Serial data input is accepted at the rising edge of this signal. SCLK has no minimum frequency requirement.

6.5.1.3 SDI

Each register access requires a specific 24-bit pattern at this input. This pattern consists of a read-and-write (R/W) bit, register address, and register value. The data are shifted in MSB first and multi-byte registers are always in little-endian format (least significant byte stored at the lowest address). Setup and hold times with respect to the SCLK must be followed (see the *Timing Requirements* table).

6.5.1.4 SDO

The SDO signal provides the output data requested by a read command. This output is high impedance during write bus cycles and during the read bit and register address portion of read bus cycles.

6.5.1.5

Figure 6-5 shows that each register access consists of 24 bits. The first bit is high for a read and low for a write.

The next 15 bits are the address of the register that is to be written to. During write operations, the last eight bits are the data written to the addressed register. During read operations, the last eight bits on SDI are ignored, and, during this time, the SDO outputs the data from the addressed register. Figure 6-5 shows the serial protocol details.

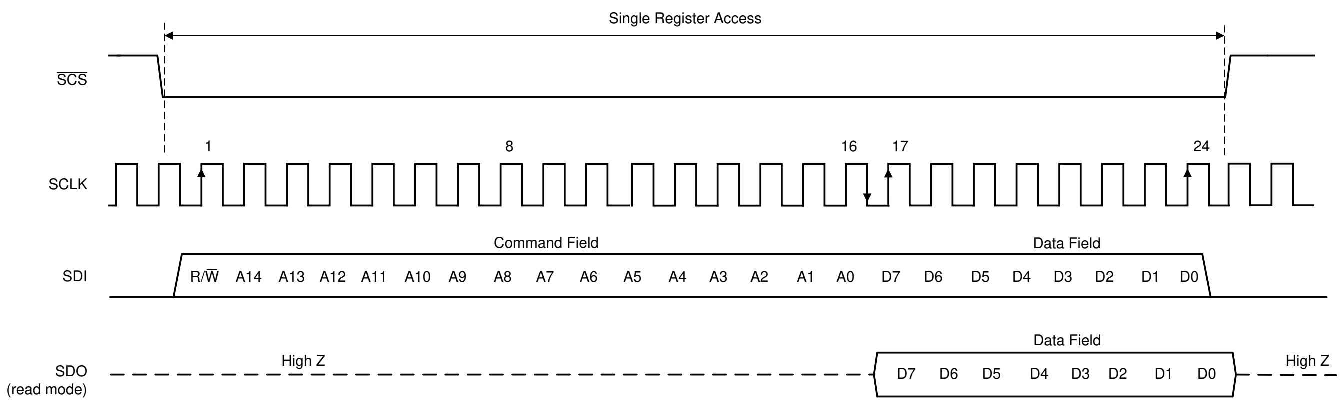


Figure 6-5. Serial Interface Protocol: Single Read/Write Operation

6.5.1.6 Streaming Mode

The serial interface supports streaming reads and writes. In this mode, the initial 24 bits of the transaction specifics the access type, register address, and data value as normal. Additional clock cycles of write or read data are immediately transferred, as long as the $\overline{SCS}$ input is maintained in the asserted (logic low) state. The register address auto increments (default) or decrements for each subsequent 8 bit transfer of the streaming transaction. The ADDR_ASC bit (register 000h, bits 5 and 2) controls whether the address value ascends (increments) or descends (decrements). Streaming mode can be disabled by setting the ADDR_HOLD bit in the USR0 register. Figure 6-6 shows the streaming mode transaction details.

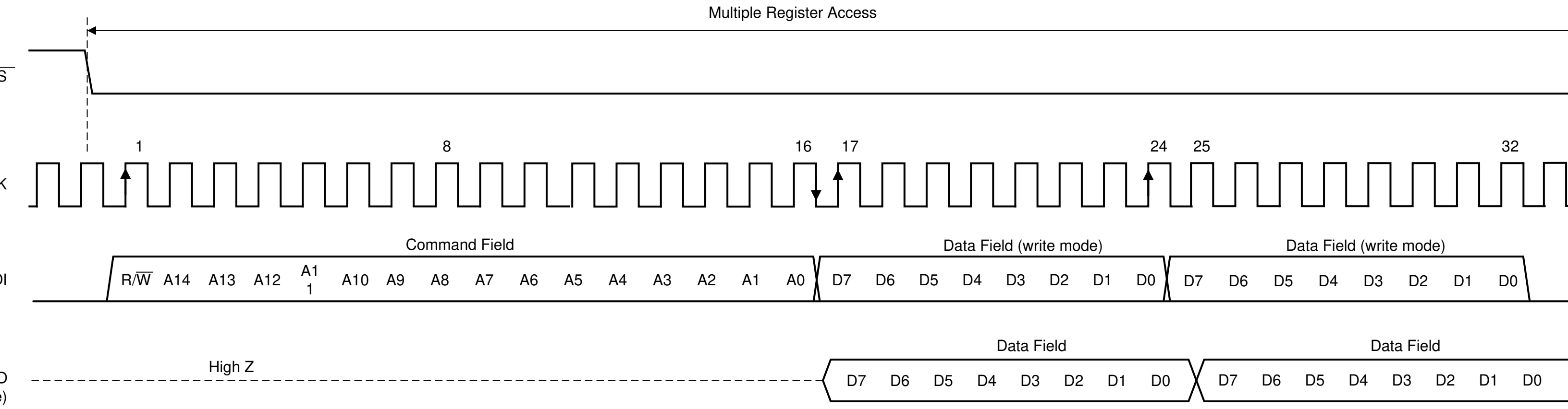


Figure 6-6. Serial Interface Protocol: Streaming Read/Write Operation

6.5.1.7

See the *Section 8* section for detailed information regarding the registers.

Note

The serial interface must not be accessed during calibration of the ADC. Accessing the serial interface during this time impairs the performance of the device until the device is calibrated correctly. Writing or reading the serial registers also reduces dynamic performance of the ADC for the duration of the register access time.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The ADC12DLx500 can be used in a wide range of applications including oscilloscopes & digitizers, time-of-flight and LiDAR distance measurement and spectrometry. The high sampling rate allows signal bandwidths of up to 2.5GHz. The ADC12DLx500 can also be DC-coupled to meet the needs of oscilloscopes. The *Section 7.2* section describes a configuration that meet the needs of a number of these applications.

7.2 Typical Applications

7.2.1 Reconfigurable Dual-Channel 2.5GSPS or Single-Channel 5GSPS Oscilloscope

This section demonstrates the use of the ADC12DLx500 in a reconfigurable oscilloscope. The oscilloscope can operate as a dual-channel oscilloscope running up to 2.5GSPS or can be reconfigured through SPI programming as a single-channel, up to 5GSPS oscilloscope. This reconfigurable setup allows tradeoffs between the number of channels and the sampling rate of the oscilloscope as needed without changing the hardware. Set the input bandwidth to the desired maximum signal bandwidth through the use of an antialiasing, low-pass filter. Digital filtering can then be used to reconfigure the analog bandwidth as required. For instance, the maximum bandwidth can be set to 1GHz for use during pulsed transient detection and then reconfigured to 100MHz through digital filtering for low-noise, power-supply ripple observation. Figure 7-1 shows the application block diagram for a reconfigurable oscilloscope.

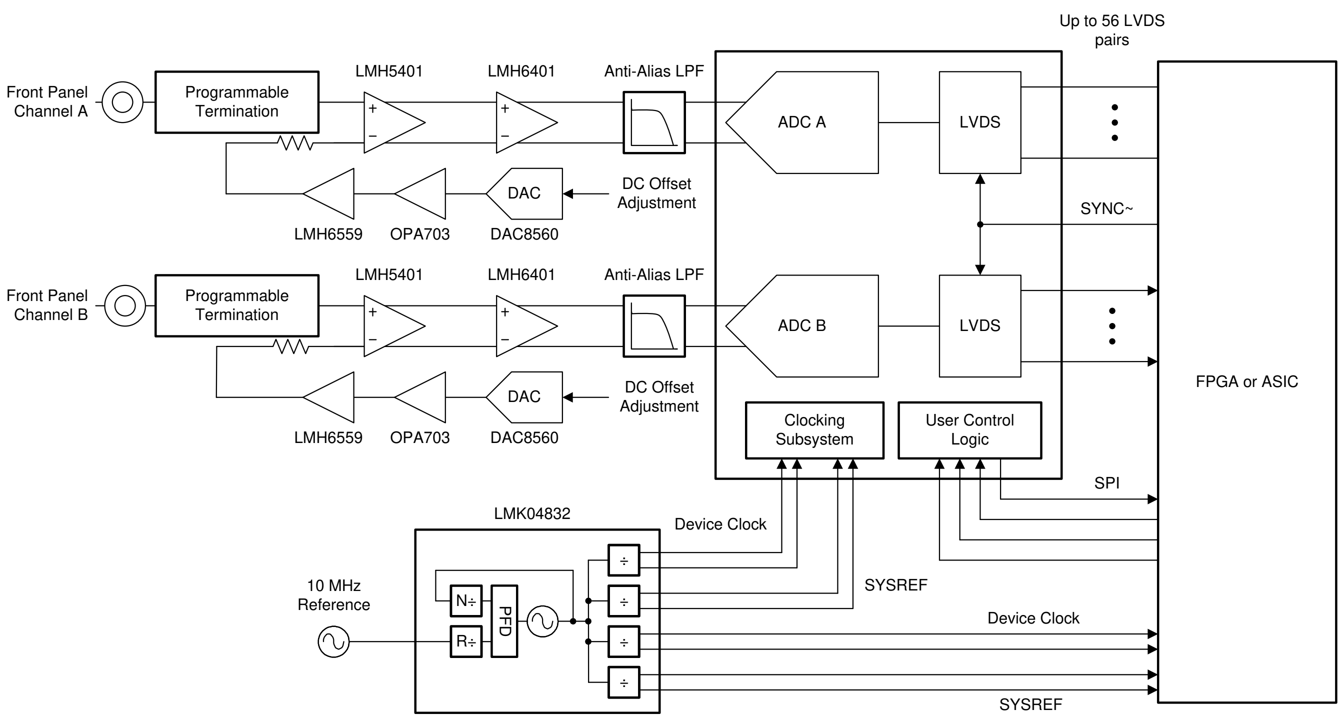


Figure 7-1. Typical Configuration for a Reconfigurable Oscilloscope

7.2.1.1 Design Requirements

7.2.1.1.1 Input Signal Path

Most oscilloscopes are required to be DC-coupled to monitor DC or low-frequency signals. This requirement forces the design to use DC-coupled, fully differential amplifiers to convert from single-ended signaling at the front panel to differential signaling at the ADC. This design uses two differential amplifiers. The first amplifier shown in Figure 7-1 is the LMH5401 that converts from single-ended to differential signaling. The LMH5401 interfaces with the front panel through a programmable termination network and has an offset adjustment input. The amplifier has an 8GHz, gain-bandwidth product that is sufficient to support a 1-GHz bandwidth oscilloscope. A second amplifier, the LMH6401, comes after the LMH5401 to provide a digitally programmable gain control for the oscilloscope. The LMH6401 supports a gain range from –6dB to 26dB in 1dB steps. If gain control is not necessary or is performed in a different location in the signal chain, then this amplifier can be replaced with a second LMH5401 for additional fixed gain or omitted altogether.

The input of the oscilloscope contains a programmable termination block that is not covered in detail here. This block enables the front-panel input termination to be programmed. For instance, many oscilloscopes allow the termination to be programmed as either 50Ω or 1MΩ to meet the needs of various applications. A 75Ω termination can also be desired to support cable infrastructure use cases. This block can also contain an option for DC blocking to remove the DC component of the external signal and therefore pass only AC signals.

A precision digital-to-analog converter (DAC) is used to configure the offset of the oscilloscope front-end to prevent saturation of the analog signal chain for input signals containing large DC offsets. The DAC8560 is shown in Figure 7-1 along with signal-conditioning amplifiers OPA703 and LMH6559. The first differential amplifier, LMH5401, is driven by the front panel input circuitry on one input, and the DC offset bias on the second input. The impedance of these driving signals must be matched at DC and over frequency for good even-order harmonic performance in the single-ended to differential conversion operation. The high bandwidth of the LMH6559 allows the device to maintain low impedance over a wide frequency range.

An antialiasing, low-pass filter is positioned at the input of the ADC to limit the bandwidth of the input signal into the ADC. This amplifier also band-limits the front-end noise to prevent aliased noise from degrading the signal-to-noise ratio of the overall system. Design this filter for the maximum input signal bandwidth specified by the oscilloscope. The input bandwidth can then be reconfigured through the use of digital filters in the FPGA or ASIC to limit the oscilloscope input bandwidth to a bandwidth less than the maximum.

7.2.1.1.2 Clocking

The ADC12DLx500 clock inputs must be AC-coupled to the device for rated performance. The clock source must have extremely low jitter (integrated phase noise) to enable rated performance. Recommended clock synthesizers include the LMX2594, LMX2592, and LMX2582.

For multi-device synchronization or deterministic latency the data converter system (ADC plus FPGA) requires a SYSREF signal in addition to the device (sampling) clock, which is similar to that used for JESD204B converters. Therefore, JESD204B compatible clock devices are a good choice for clocking the ADC12DLx500. The LMK04832, LMK04828, LMK04826, and LMK04821 devices are suitable to generate these clocks. Depending on the ADC clock frequency and jitter requirements, this device can also be used as the system clock synthesizer or as a device clock and SYSREF distribution device when multiple ADC12DLx500 devices are used in a system.

7.2.1.1.3 ADC12DLx500

The ADC12DLx500 is used for oscilloscope applications. The ability to tradeoff channel count and sampling speed allows designers to build flexible hardware to meet multiple needs. This flexibility saves development time and cost, allows hardware reuse for various projects, and enables software upgrade paths for additional functionality. The low code-error rate eliminates concerns about undesired time-domain glitches or sparkle codes. This rate makes the ADC12DLx500 a perfect fit for long-duration transient detection measurements and reduces the probability of false triggers. The input common-mode voltage of 0V allows the driving amplifiers to use equal split power supplies that center the amplifier output common-mode voltage at 0V and eliminates the need for common-mode voltage shifting before the ADC inputs. The high input bandwidth of the ADC12DLx500 simplifies the design of the driving amplifier circuit and antialiasing, low-pass filter. The use of dual-edge sampling (DES) in single-channel mode eliminates the need to change the clock frequency when switching between dual- and single-channel modes and simplifies synchronization by relaxing the setup and hold timing requirements of SYSREF. The t_{AD} adjust circuit allows the user to time-align the sampling instances of multiple ADC12DLx500 devices.

7.2.1.2 Application Curves

The following application curves demonstrate performance and results only of the ADC. The amplifier front-end is not included in these measurements. Figure 7-2 to Figure 7-9 illustrate the following configurations and measurements:

- 12 bit, 5GSPS, single-channel oscilloscope
  - 50MHz, square-wave time domain
  - 50MHz, square-wave (unwrapped) time domain
  - 200MHz, sine-wave time domain
  - 200MHz, sine-wave frequency domain (FFT)
  - Idle-channel noise (no input)
- 12 bit, 2.5GSPS, dual-channel oscilloscope
  - 200MHz, sine-wave (channel A) and 50MHz, square-wave (channel B) time domain
  - 200MHz, sine-wave (channel A) frequency domain (FFT)
  - Idle-channel noise (no input)

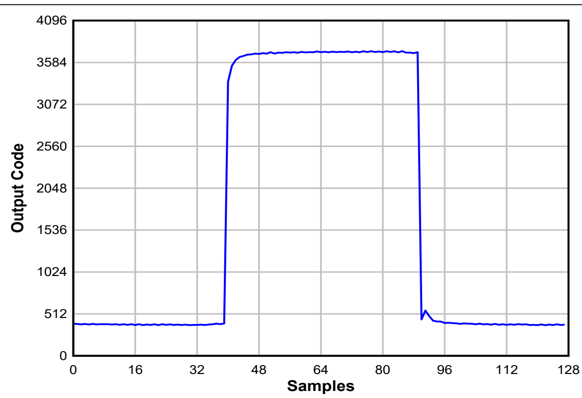


Figure 7-2. 50MHz, Square-Wave Time Domain for 5GSPS, Single-Channel Oscilloscope

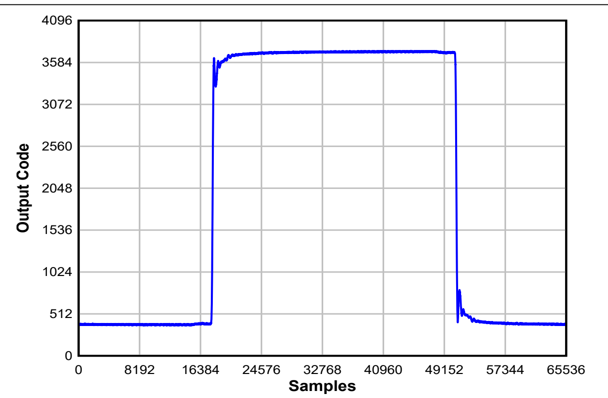


Figure 7-3. 50MHz, Unwrapped Square-Wave Time Domain for 5GSPS, Single-Channel Oscilloscope

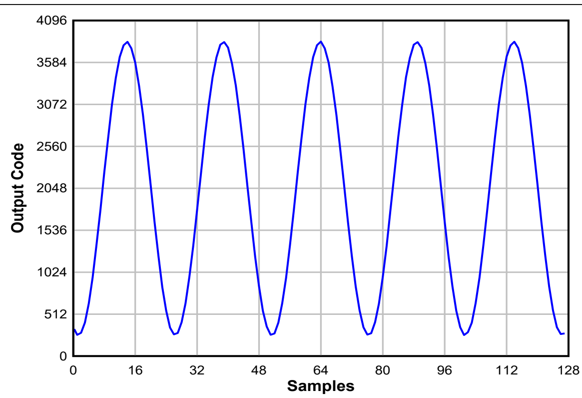


Figure 7-4. 200MHz, Sine-Wave Time Domain for 5GSPS, Single-Channel Oscilloscope

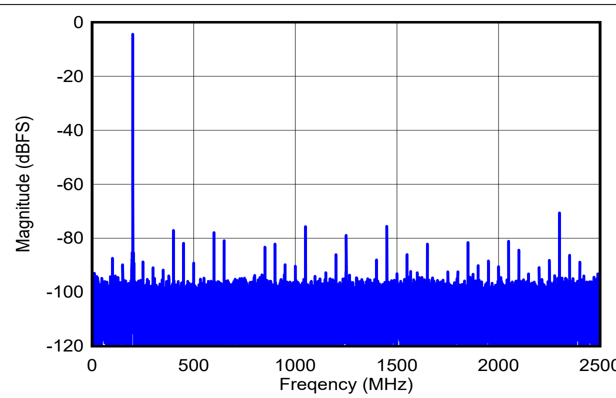


Figure 7-5. 200MHz, Sine-Wave Frequency Domain (FFT) for 5GSPS, Single-Channel Oscilloscope

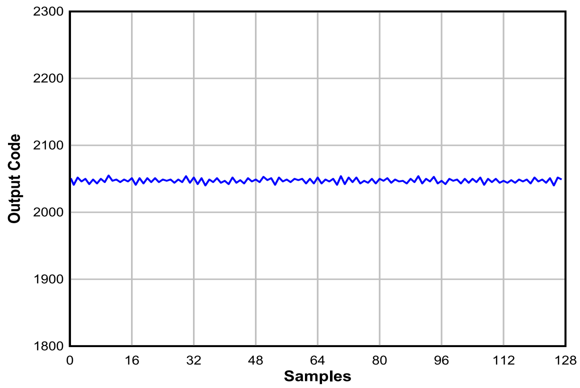


Figure 7-6. Idle-Channel Noise (No Input) for 5GSPS, Single-Channel Oscilloscope

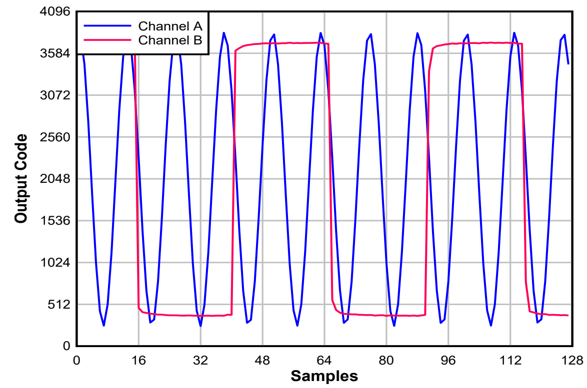


Figure 7-7. 200MHz, Sine-Wave (Channel A) and 50MHz, Square-Wave (Channel B) Time Domain for 2.5GSPS, Dual-Channel Oscilloscope

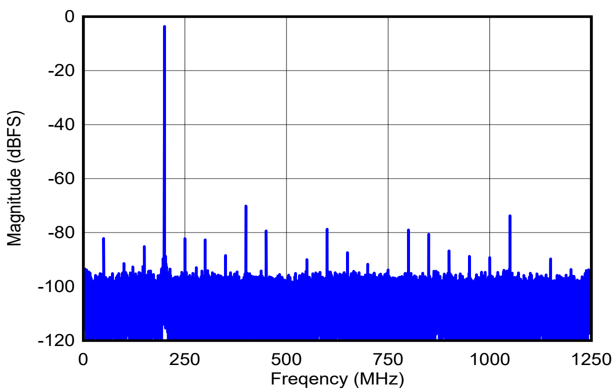


Figure 7-8. 200MHz, Sine-Wave (Channel A) Frequency Domain (FFT) for 2.5GSPS, Dual-Channel Oscilloscope

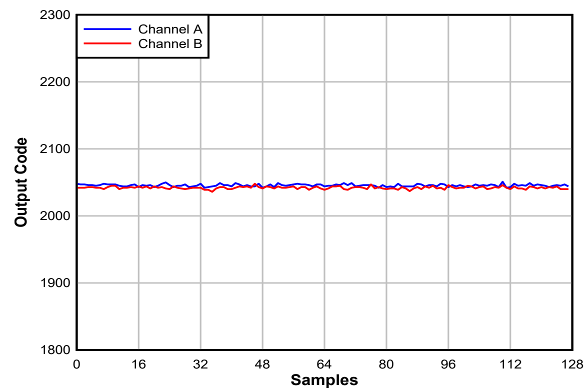


Figure 7-9. Idle-Channel Noise (No Input) for 2.5GSPS, Dual-Channel Oscilloscope

7.3 Initialization Set Up

The device requires a specific startup and alignment sequence. The general order of that sequence is listed in the following steps.

1. Power-up or reset the device.
2. Apply a stable device CLK signal at the desired frequency.
3. Program LVDS_EN = 0 to stop the LVDS state machine and allow setting changes.
4. Program CAL_EN = 0 to stop the calibration state machine and allow setting changes.
5. Program the LMODE register to the desired LVDS output mode.
6. Program SYNC_SEL as needed. Choose $\overline{\text{SYNCSE}}$ or the TMSTP± differential inputs.
7. Configure device calibration settings as desired. Select foreground calibration modes and offset calibration as needed.
8. Program CAL_EN = 1 to enable the calibration state machine.
9. Enable overrange via OVR_EN and adjust settings if desired.
10. Program LVDS_EN = 1 to enable the LVDS interface and allow the receiver to initialize.
11. Assert the $\overline{\text{SYNC}}$ signal (set by SYNC_SEL) if required to send the strobe signal or user-defined pattern.
12. Program CAL_SOFT_TRIG = 0.
13. Program CAL_SOFT_TRIG = 1 to initiate a calibration.

7.4 Power Supply Recommendations

The device requires two different power-supply voltages. 1.9V DC is required for the VA19 power bus and 1.1V DC is required for the VA11 and VD11 power buses. VLVDS can be set to any voltage between 1.9V and 1.1V. The LVDS output driver common-mode voltage tracks the VLVDS supply voltage. In general, a 1.9V supply voltage for VLVDS can be used for standard LVDS receivers.

The power-supply voltages must be low noise and provide the needed current to achieve rated device performance.

Table 7-1. Power Supply Current Requirement

DEVICE POWER SUPPLY	SUPPLY VOLTAGE	CURRENT REQUIREMENT
VA19	1.9V	1A
VA11	1.1V	600mA
VD11	1.1V	300mA
VLVDS	1.1-1.9V	500mA

There are two recommended power-supply architectures:

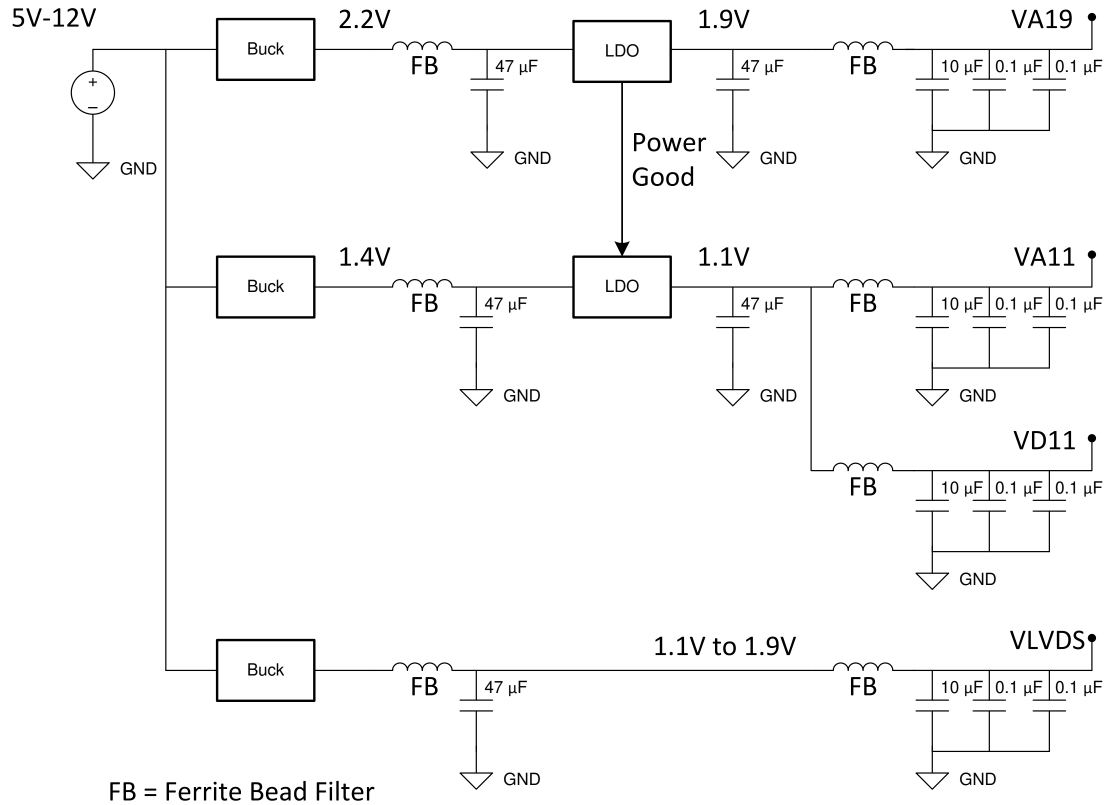
1. Step down using high-efficiency switching converters, followed by a second stage of regulation to provide switching noise reduction and improved voltage accuracy.
2. Directly step down the final ADC supply voltage using high-efficiency switching converters. This approach provides the best efficiency, but care must be taken to ensure switching noise is minimized to prevent degraded ADC performance.

TI WEBENCH® Power Designer can be used to select and design the individual power-supply elements needed: see the WEBENCH® Power Designer

Recommended switching regulators for the first stage include the TPS62085, TPS82130, TPS62130A, and similar devices.

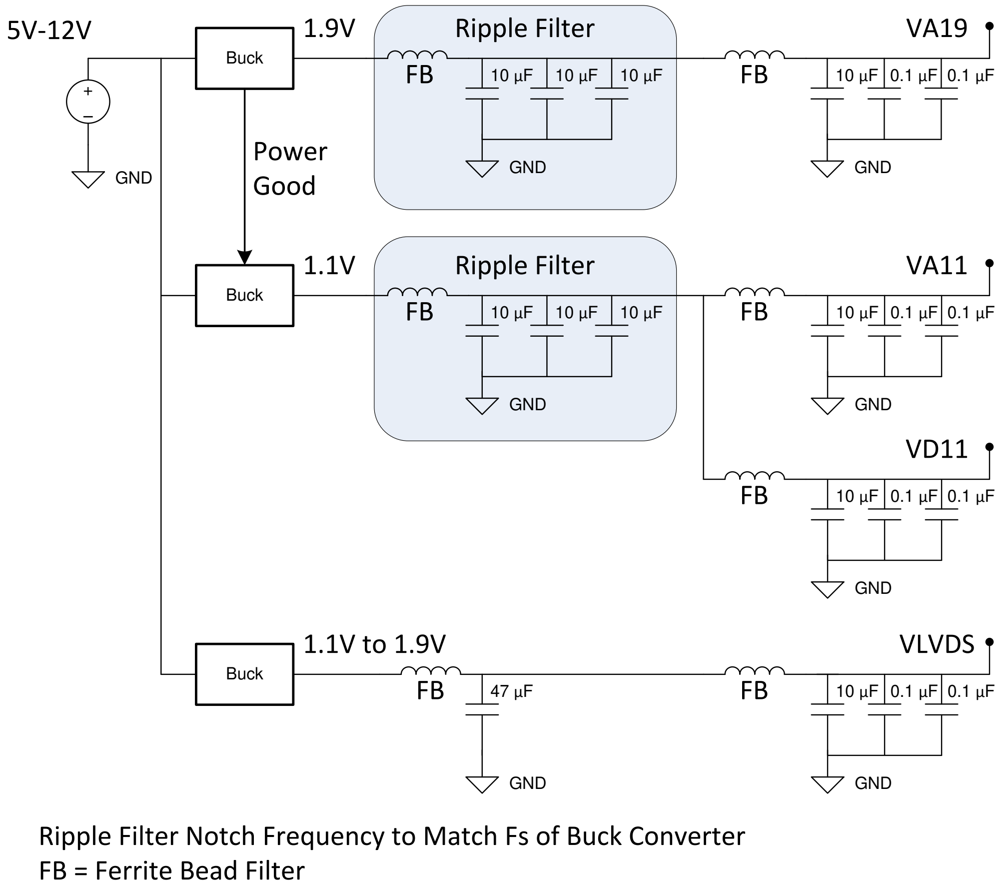
Recommended low dropout (LDO) linear regulators include the TPS7A7200, TPS74401, and similar devices.

For the switcher only approach, the ripple filter must be designed with a notch frequency that aligns with the switching ripple frequency of the DC/DC converter. Make a note of the switching frequency reported from WEBENCH® and design the EMI filter and capacitor combination to have the notch frequency centered as needed. Figure 7-10 and Figure 7-11 illustrate the two approaches. Do not share VLVDS with the analog supply voltages in order to prevent digital switching noise from coupling into the analog signal chain. If VLVDS must be shared with either VA11 or VA19, apply careful power supply filtering to limit digital noise at the analog supply pins.



FB = ferrite bead filter.

Figure 7-10. LDO Linear Regulator Approach Example



Ripple filter notch frequency to match the fs of the buck converter.

FB = ferrite bead filter.

Figure 7-11. Switcher-Only Approach Example

7.4.1 Power Sequencing

The voltage regulators must be sequenced using the power-good outputs and enable inputs to ensure that the Vx11 regulator is enabled after the VA19 supply is good. Similarly, as soon as the VA19 supply drops out of regulation on power-down, the Vx11 regulator is disabled.

The general requirement for the ADC is that VA19 ≥ Vx11 during power-up, operation, and power-down.

TI also recommends that VA11 and VD11 are derived from a common 1.1V regulator. This recommendation ensures that all 1.1V blocks are at the same voltage, and no sequencing problems exist between these supplies. Also use ferrite bead filters to isolate any noise on the VA11 and VD11 buses from affecting each other. If VA11 and VD11 are powered from separate regulators, then the device is sensitive to voltage drops that affect the VA11 input. If the VA11 voltage is brought down below 0.6V, the device must be reset through the SOFT_RESET bit in the CONFIG_A register.

VLVDS can be powered up independently of the other supplies.

7.5 Layout

7.5.1 Layout Guidelines

There are many critical signals that require specific care during board design:

1. Analog input signals
2. CLK and SYSREF
3. LVDS data outputs at up to 1.6Gbps
4. Power connections
5. Ground connections

Items 1 and 2 must be routed for excellent signal quality at high frequencies. Use the following general practices for these signals:

1. Route using loosely coupled 100Ω differential traces. This routing minimizes impact of corners and length-matching serpentine on pair impedance.
2. Provide adequate pair-to-pair spacing to minimize crosstalk.
3. Provide adequate ground plane pour spacing to minimize coupling with the high-speed traces.
4. Use smoothly radiused corners. Avoid 45- or 90-degree bends.
5. Incorporate ground plane cutouts at component landing pads to avoid impedance discontinuities at these locations. Cutout below the landing pads on one or multiple ground planes to achieve a pad size or stackup height that achieves the needed 50-Ω, single-ended impedance.
6. Avoid routing traces near irregularities in the reference ground planes. Irregularities include ground plane clearances associated with power and signal vias and through-hole component leads.
7. Provide symmetrically located ground tie vias adjacent to any high-speed signal vias.
8. When high-speed signals must transition to another layer using vias, transition as far through the board as possible (top to bottom is best case) to minimize via stubs on top or bottom of the vias. If layer selection is not flexible, use back-drilled or buried, blind vias to eliminate stubs.

The LVDS data outputs must be routed with sufficient signal quality using the following general practices:

1. Route using tightly coupled 100Ω differential traces to minimize the routing area and decrease crosstalk between adjacent data pairs.
2. Use smoothly radiused corners or 45-degree bends. Avoid 90-degree bends.
3. Avoid routing traces near irregularities in the reference ground planes. Irregularities include ground plane clearances associated with power and signal vias and through-hole component leads.
4. Provide symmetrically located ground tie vias adjacent to any high-speed signal vias.
5. Data, clock, and strobe pairs must be sufficiently delay matched to provide adequate timing margin at the receiver. If routing on multiple layers, trace lengths must be compensated for the delay mismatch introduced by the effective dielectric constant of each layer.

In addition, TI recommends performing signal quality simulations of the critical signal traces before committing to fabrication. Perform insertion loss, return loss, and time domain reflectometry (TDR) evaluations.

The power and ground connections for the device are also very important. These rules must be followed:

1. Provide low-resistance connection paths to all power and ground pins.
2. Use multiple power layers if necessary to access all pins.
3. Avoid narrow isolated paths that increase connection resistance.
4. Use a signal, ground, or power circuit board stackup to maximum coupling between the ground and power planes.

7.5.2 Layout Example

Figure 7-12 to Figure 7-14 provide examples of the critical traces routed on the device evaluation module (EVM). Figure 7-15 provides an example printed circuit board (PCB) layer stackup.

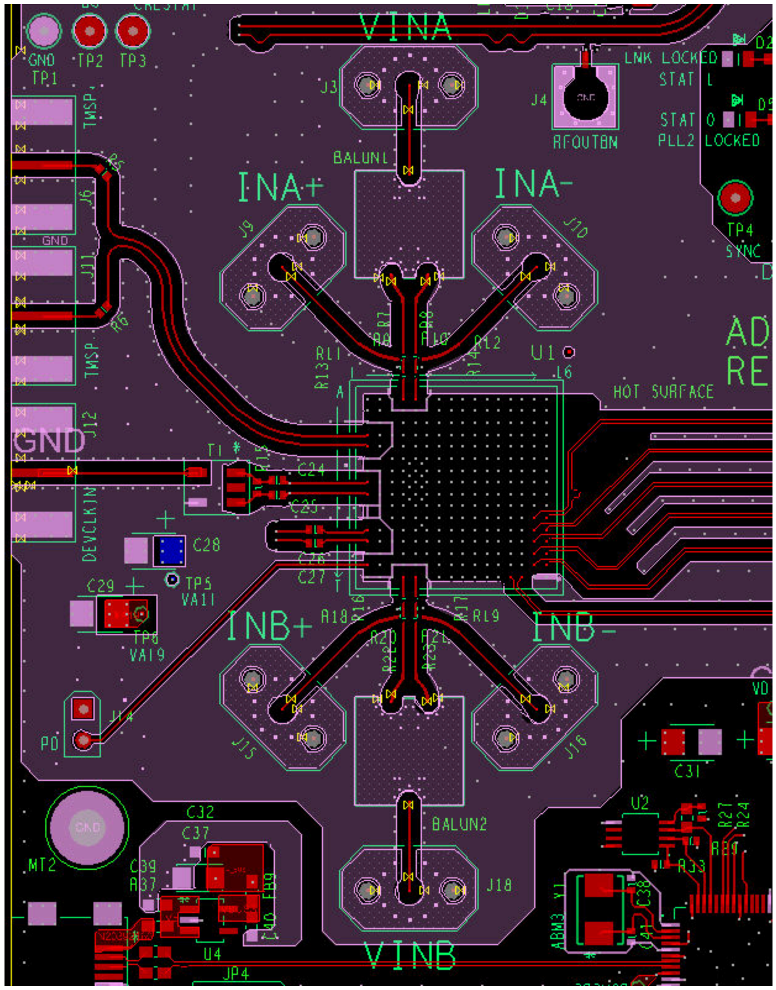


Figure 7-12. Top Layer Routing: Analog Inputs, CLK and SYSREF, DA0-3, DB0-3

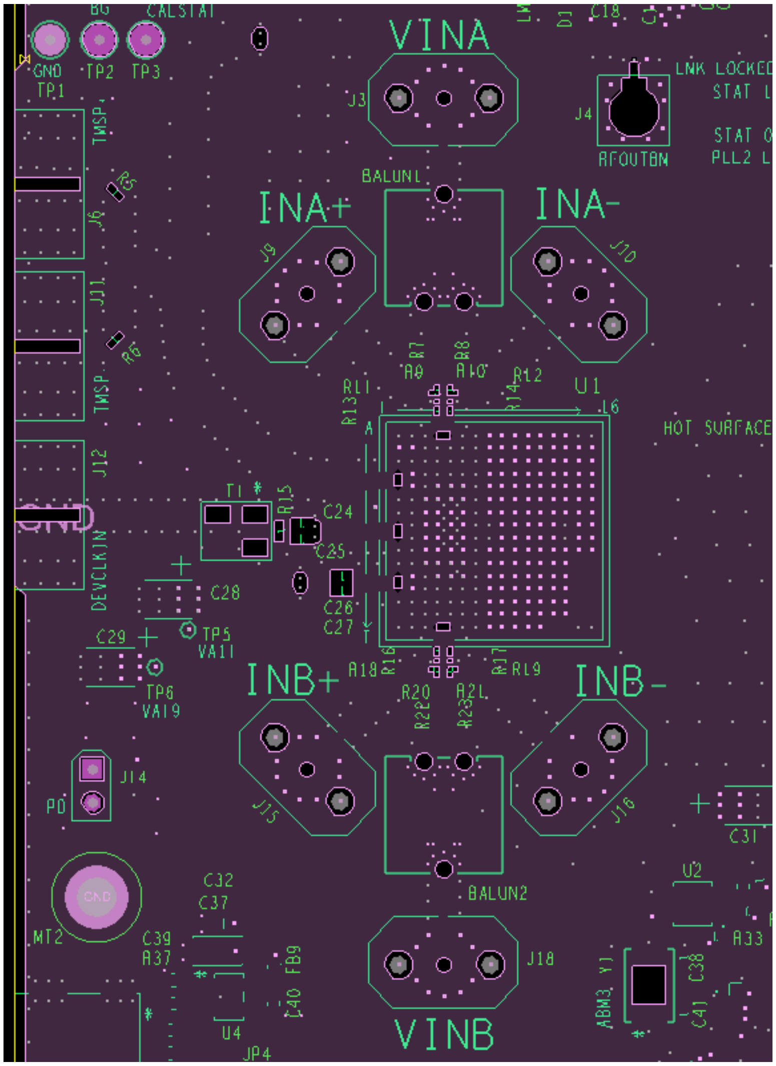


Figure 7-13. GND1 Cutouts to Optimize Impedance of Component Pads

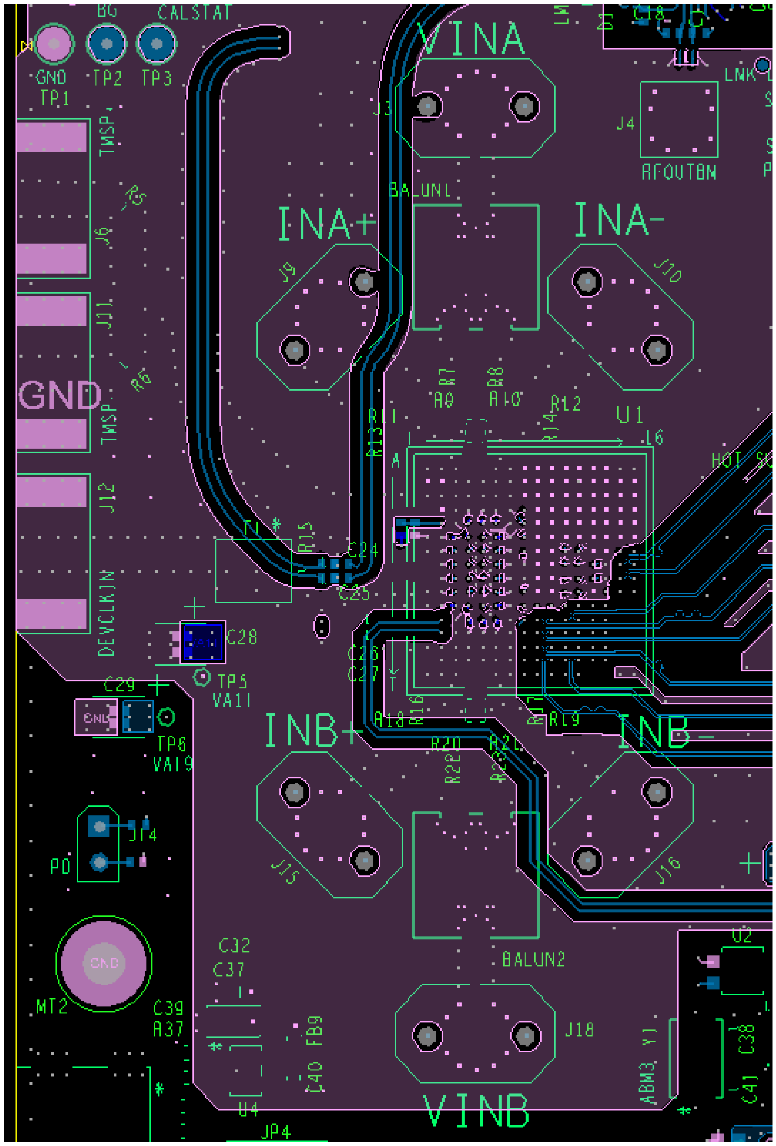


Figure 7-14. Bottom Layer Routing: Additional CLK Routing, DA4-7, DB4-7

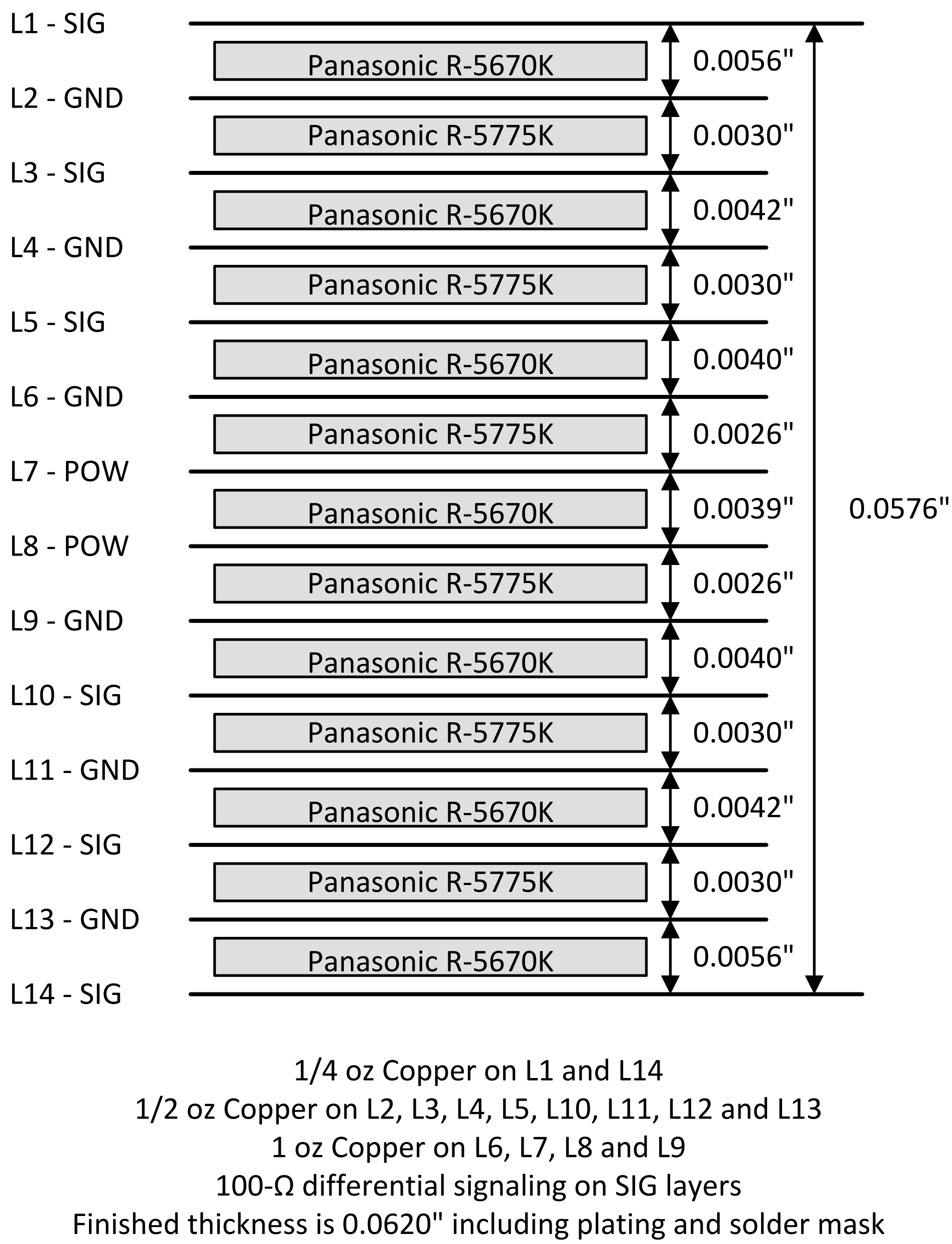


Figure 7-15. Example PCB Stackup

8 Register Maps

8.1 SPI_REGISTER_MAP Registers

Table 8-1 lists the memory-mapped registers for the SPI_REGISTER_MAP. All register offset addresses not listed in Table 8-1 are considered reserved locations and the register contents are not to be modified.

Table 8-1. SPI_REGISTER_MAP Registers

Address	Acronym	Register Name	Section
0x000	CONFIG_A	Configuration A (Default: 0x30)	Go
0x002	DEVICE_CONFIG	Device Configuration (Default: 0x00)	Go
0x003	CHIP_TYPE	Chip Type (Default: 0x03)	Go
0x00C-0x00D	VENDOR_ID	Vendor Identification (Default: 0x0451)	Go
0x010	USR0	User SPI Configuration (Default: 0x00)	Go
0x029	CLK_CTRL0	Clock Control 0 (Default: 0x00)	Go
0x02A	CLK_CTRL1	Clock Control 1 (Default: 0x00)	Go
0x02C-0x02E	SYSREF_POS	SYSREF Capture Position (Read-only status)	Go
0x030-0x031	FS_RANGE_A	Full-Scale Voltage for INA± (Default: 0xA000)	Go
0x032-0x033	FS_RANGE_B	Full-Scale Voltage for INB± (Default: 0xA000)	Go
0x038	BG_BYPASS	Band-Gap Bypass (Default: 0x00)	Go
0x03B	SYNC_CTRL	$\overline{\text{SYNC\_SE}}$/TIMESTAMP Control (Default: 0x00)	Go
0x048	LVDS_SWING	LVDS Swing Mode (Default: 0x00)	Go
0x060	INPUT_MUX	Input Mux Control (Default: 0x01)	Go
0x061	CAL_EN	Calibration Enable (Default: 0x01)	Go
0x062	CAL_CFG0	Calibration Configuration 0 (Default: 0x01)	Go
0x06A	CAL_STATUS	Calibration Status (Default: undefined; read-only)	Go
0x06B	CAL_PIN_CFG	Calibration Pin Configuration (Default: 0x00)	Go
0x06C	CAL_SOFT_TRIG	Calibration Software Trigger (Default: 0x01)	Go
0x070	CAL_DATA_EN	Calibration Data Enable (Default: 0x00)	Go
0x071	CAL_DATA	Calibration Data (Default: undefined)	Go
0x07A	GAIN_TRIM_A	Gain DAC Trim A (Default from fuse ROM)	Go
0x07B	GAIN_TRIM_B	Gain DAC Trim B (Default from fuse ROM)	Go
0x07C	BG_TRIM	Band-Gap Trim (Default from fuse ROM)	Go
0x07E	RTRIM_A	Resistor TRIM for INA± (Default from fuse ROM)	Go
0x07F	RTRIM_B	Resistor TRIM for INB± (Default from fuse ROM)	Go
0x09D	ADC_DITH	ADC Dither register (Default: 0x01)	Go
0x102	B0_TIME_0	Time Adjustment for Bank 0 (0° clock) (Default from fuse ROM)	Go
0x103	B0_TIME_90	Time Adjustment for Bank 0 (–90° clock) (Default from fuse ROM)	Go
0x112	B1_TIME_0	Time Adjustment for Bank 1 (0° clock) (Default from fuse ROM)	Go
0x113	B1_TIME_90	Time Adjustment for Bank 1 (–90° clock) (Default from fuse ROM)	Go
0x142	B4_TIME_0	Time Adjustment for Bank 4 (0° clock) (Default from fuse ROM)	Go
0x152	B5_TIME_0	Time Adjustment for Bank 5 (0° clock) (Default from fuse ROM)	Go
0x160	LSB_CTRL	LSB Control Bit Output (Default: 0x00)	Go
0x161	LSB_SEL	LSB Control Bit Position (Default: 0x00)	Go
0x180-0x181	UPAT0	User-Defined Pattern (Sample 0; default: 0x0000)	Go
0x182-0x183	UPAT1	User-Defined Pattern (Sample 1; default: 0x0FFF; same format as UPAT0)	Go
0x184-0x185	UPAT2	User-Defined Pattern (Sample 2; default: 0x0000; same format as UPAT0)	Go
0x186-0x187	UPAT3	User-Defined Pattern (Sample 3; default: 0x0FFF; same format as UPAT0)	Go
0x188-0x189	UPAT4	User-Defined Pattern (Sample 4; default: 0x0000; same format as UPAT0)	Go

Table 8-1. SPI_REGISTER_MAP Registers (continued)

Address	Acronym	Register Name	Section
0x18A-0x18B	UPAT5	User-Defined Pattern (Sample 5; default: 0x0FFF; same format as UPAT0)	Go
0x18C-0x18D	UPAT6	User-Defined Pattern (Sample 6; default: 0x0000; same format as UPAT0)	Go
0x18E-0x18F	UPAT7	User-Defined Pattern (Sample 7; default: 0x0FFF; same format as UPAT0)	Go
0x190	UPAT_CTRL	User-Defined Pattern Control (Default: 0x1E)	Go
0x200	LVDS_EN	LVDS Subsystem Enable (Default: 0x01)	Go
0x201	LMODE	LVDS Mode (Default: 0x01)	Go
0x202	LFRAME	LVDS Frame Length (Default: 0x80; 128 decimal)	Go
0x203	LSYNC_N	LVDS Manual Sync Request (Default: 0x01)	Go
0x204	LCTRL	LVDS Control (Default: 0x02)	Go
0x205	PAT_SEL	LVDS Pattern Control (Default: 0x02)	Go
0x206	LCS_EN	LVDS Clock and Strobe Enables (Default: 0xFF)	Go
0x208	LVDS_STATUS	System Status Register	Go
0x209	PD_CH	ADC Channel Power-Down (Default: 0x00)	Go
0x211	OVR_T0	Overrange Threshold 0 (Default: 0xF2)	Go
0x212	OVR_T1	Overrange Threshold 1 (Default: 0xAB)	Go
0x213	OVR_CFG	Overrange Enable/Hold Off (Default: 0x07)	Go
0x2B0	SRC_EN	SYSREF Calibration Enable (Default: 0x00)	Go
0x2B1	SRC_CFG	SYSREF Calibration Configuration (Default: 0x05)	Go
0x2B2-0x2B4	SRC_STATUS	SYSREF Calibration Status (Default: undefined; read-only)	Go
0x2B5-0x2B7	TAD	CLK± Timing Adjust (Default: 0x00)	Go
0x2B8	TAD_RAMP	CLK± Timing Adjust Ramp Control (Default: 0x00)	Go
0x2C0	ALARM	Alarm Interrupt (Read-only)	Go
0x2C1	ALM_STATUS	Alarm Status (Default: 0x05; write to clear)	Go
0x2C2	ALM_MASK	Alarm Mask Register (Default: 0x05)	Go
0x310	TADJ_A	Timing Adjust for A-ADC, Dual Mode (Default from fuse ROM)	Go
0x313	TADJ_B	Timing Adjust for B-ADC, Dual Mode (Default from fuse ROM)	Go
0x314	TADJ_A_FG90_VINA	Timing Adjust for A-ADC, DES, Foreground Calibration, INA± (Default from fuse ROM)	Go
0x315	TADJ_B_FG0_VINA	Timing Adjust for B-ADC, DES, Foreground Calibration, INA± (Default from fuse ROM)	Go
0x31A	TADJ_A_FG90_VINB	Timing Adjust for A-ADC, DES, Foreground Calibration, INB± (Default from fuse ROM)	Go
0x31B	TADJ_B_FG0_VINB	Timing Adjust for B-ADC, DES, Foreground Calibration, INB± (Default from fuse ROM)	Go
0x344-0x345	OADJ_A_FG0_VINA	Offset Adjustment for A-ADC, Foreground Calibration, 0° Clock, INA± (Default from fuse ROM)	Go
0x346-0x347	OADJ_A_FG0_VINB	Offset Adjustment for A-ADC, Foreground Calibration, 0° Clock, INB± (Default from fuse ROM)	Go
0x348-0x349	OADJ_A_FG90_VINA	Offset Adjustment for A-ADC, Foreground Calibration, 90° Clock, INA± (Default from fuse ROM)	Go
0x34A-0x34B	OADJ_A_FG90_VINB	Offset Adjustment for A-ADC, Foreground Calibration, 90° Clock, INB± (Default from fuse ROM)	Go
0x34C-0x34D	OADJ_B_FG0_VINA	Offset Adjustment for B-ADC, Foreground Calibration, INA± (Default from fuse ROM)	Go
0x34E-0x34F	OADJ_B_FG0_VINB	Offset Adjustment for B-ADC, Foreground Calibration, INB± (Default from fuse ROM)	Go

Table 8-1. SPI_REGISTER_MAP Registers (continued)

Address	Acronym	Register Name	Section
0x360	GAIN_B0	Fine Gain Adjust for Bank 0 (Default from fuse ROM)	Go
0x361	GAIN_B1	Fine Gain Adjust for Bank 1 (Default from fuse ROM)	Go
0x364	GAIN_B4	Fine Gain Adjust for Bank 4 (Default from fuse ROM)	Go
0x365	GAIN_B5	Fine Gain Adjust for Bank 5 (Default from fuse ROM)	Go

Complex bit access types are encoded to fit into small table cells. Table 8-2 shows the codes that are used for access types in this section.

Table 8-2. SPI_REGISTER_MAP Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.1.1 CONFIG_A Register (Address = 0x000) [reset = 0x30]

CONFIG_A is shown in Figure 8-1 and described in Table 8-3.

Return to Summary Table.

Configuration A register (default: 0x30). This register controls device reset and SPI interface parameters.

Figure 8-1. CONFIG_A Register

7	6	5	4	3	2	1	0
SOFT_RESET	RESERVED	ASCEND	SDO_ACTIVE	RESERVED			
R/W-0x0	R/W-0x0	R/W-0x1	R-0x1	R/W-0x0			

Table 8-3. CONFIG_A Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SOFT_RESET	R/W	0x0	Setting this bit causes a full reset of the device and all SPI registers (including CONFIG_A). This bit is self-clearing. After writing this bit, the device may take up to 750 ns to reset. During this time, do not perform any SPI transactions.
6	RESERVED	R/W	0x0	Reserved
5	ASCEND	R/W	0x1	0 : Address is decremented during streaming reads or writes 1 : Address is incremented during streaming reads or writes (default)
4	SDO_ACTIVE	R	0x1	Always returns 1. Always use SDO for SPI reads. No SDIO mode is supported.
3-0	RESERVED	R/W	0x0	Reserved

8.1.2 DEVICE_CONFIG Register (Address = 0x002) [reset = 0x00]

DEVICE_CONFIG is shown in Figure 8-2 and described in Table 8-4.

Return to Summary Table.

Device Configuration register (default: 0x00). This device controls the power-down of the device.

Figure 8-2. DEVICE_CONFIG Register

7	6	5	4	3	2	1	0
RESERVED						MODE	
R/W-0x0						R/W-0x0	

Table 8-4. DEVICE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0x0	Reserved
1-0	MODE	R/W	0x0	0 : Normal operation (default) 1 : Reserved 2 : Reserved 3 : Power-down

8.1.3 CHIP_TYPE Register (Address = 0x003) [reset = 0x03]

CHIP_TYPE is shown in Figure 8-3 and described in Table 8-5.

Return to Summary Table.

Chip Type register (default: 0x03). This register returns the chip type.

Figure 8-3. CHIP_TYPE Register

7	6	5	4	3	2	1	0
RESERVED				CHIP_TYPE			
R/W-0x0				R-0x3			

Table 8-5. CHIP_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0x0	Reserved
3-0	CHIP_TYPE	R	0x3	Always returns 0x3, indicating that the device is a high-speed ADC.

8.1.4 VENDOR_ID Register (Address = 0xC) [reset = 0x0451]

VENDOR_ID is shown in Figure 8-4 and described in Table 8-6.

Return to Summary Table.

Vendor Identification register (default = 0x0451). This register returns the vendor identification number.

Figure 8-4. VENDOR_ID Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VENDOR_ID															
R-0x0451															

Table 8-6. VENDOR_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VENDOR_ID	R	0x0451	Always returns 0x0451 (vendor ID for Texas Instruments).

8.1.5 USR0 Register (Address = 0x010) [reset = 0x00]

USR0 is shown in Figure 8-5 and described in Table 8-7.

Return to Summary Table.

User SPI Configuration register (default: 0x00). This register enables holding of the current address during streaming SPI transactions.

Figure 8-5. USR0 Register

7	6	5	4	3	2	1	0
RESERVED							ADDR_HOLD
R/W-0x0							R/W-0x0

Table 8-7. USR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0x0	Reserved
0	ADDR_HOLD	R/W	0x0	0 : Use the ASCEND register to select address ascend or descend mode (default) 1 : Address stays constant throughout streaming operation; useful for reading and writing calibration vector information at the CAL_DATA register

8.1.6 CLK_CTRL0 Register (Address = 0x029) [reset = 0x00]

CLK_CTRL0 is shown in Figure 8-6 and described in Table 8-8.

Return to Summary Table.

Clock Control 0 register (default: 0x00). This register is used to control the SYSREF receiver (SYSREF±), processing of the SYSREF signal and the SYSREF windowing zoom and delay settings.

Figure 8-6. CLK_CTRL0 Register

7	6	5	4	3	2	1	0
RESERVED	SYSREF_PROC_EN	SYSREF_RECV_EN	SYSREF_ZOOM	SYSREF_SEL			
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0			

Table 8-8. CLK_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	Reserved
6	SYSREF_PROC_EN	R/W	0x0	This bit enables the SYSREF processor, which allows the device to process SYSREF events (default: disabled). SYSREF_RECV_EN must be set before setting SYSREF_PROC_EN.
5	SYSREF_RECV_EN	R/W	0x0	Set this bit to enable the SYSREF receiver circuit (default: disabled).
4	SYSREF_ZOOM	R/W	0x0	Set this bit to *zoom* in the SYSREF windowing status and delays (impacts SYSERF_POS and SYSREF_SEL). When set, the delays used in the SYSREF windowing feature (reported in the SYSREF_POS register) become smaller. Use SYSREF_ZOOM for high clock rates, specifically when multiple SYSREF valid windows are encountered in the SYSREF_POS register; see the *Section 6.3.4.3.1* section.

Table 8-8. CLK_CTRL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	SYSREF_SEL	R/W	0x0	Set this field to select which SYSREF delay to use. Set this field based on the results returned by SYSREF_POS; see the *Section 6.3.4.3.1* section. These bits must be set to 0 to use SYSREF calibration; see the *Section 6.3.4.3.2* section.

8.1.7 CLK_CTRL1 Register (Address = 0x02A) [reset = 0x00]

CLK_CTRL1 is shown in Figure 8-7 and described in Table 8-9.

Return to Summary Table.

Clock Control 1 register (default: 0x00). This register allows SYSREF to be used as the timestamp input, allows inversion of the SYSREF signal, and enables the DC-coupled receiver mode for the CLK± and SYSREF± inputs.

Figure 8-7. CLK_CTRL1 Register

7 6 5 4	3	2	1	0
RESERVED	SYSREF_TIME_STAMP_EN	DEVCLK_LVPECL_EN	SYSREF_LVPECL_EN	SYSREF_INVERTED
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0

Table 8-9. CLK_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0x0	Reserved
3	SYSREF_TIME_STAMP_EN	R/W	0x0	The SYSREF signal is output on the LSB of the LVDS output samples when SYSREF_TIMESTAMP_EN and TIME_STAMP_EN are both set. This bit allows SYSREF± to be used as the timestamp input.
2	DEVCLK_LVPECL_EN	R/W	0x0	Activate DC-coupled, low-voltage PECL mode for CLK±; see the *Pin Functions* table.
1	SYSREF_LVPECL_EN	R/W	0x0	Activate DC-coupled, low-voltage PECL mode for SYSREF±; see the *Pin Functions* table.
0	SYSREF_INVERTED	R/W	0x0	This bit inverts the SYSREF signal used for alignment.

8.1.8 SYSREF_POS Register (Address = 0x02C-0x02E) [reset = Undefined]

SYSREF_POS is shown in Figure 8-8 and described in Table 8-10.

Return to Summary Table.

SYSREF Capture Position register (read-only status). This register is used by the SYSREF windowing feature to report back the valid SYSREF capture windows; see the *Section 6.3.4.3.1* section.

Figure 8-8. SYSREF_POS Register

23	22	21	20	19	18	17	16
SYSREF_POS[23:16]							
R-Undefined							
15	14	13	12	11	10	9	8
SYSREF_POS[15:8]							
R-Undefined							
7	6	5	4	3	2	1	0
SYSREF_POS[7:0]							
R-Undefined							

Table 8-10. SYSREF_POS Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	SYSREF_POS	R/W	Undefined	Returns a 24-bit status value that indicates the position of the SYSREF edge with respect to CLK±. Use this field to program SYSREF_SEL.

8.1.9 INA Full-Scale Range Adjust Register (Address = 0x030-0x031) [reset = 0xA000]

FS_RANGE_A is shown in Figure 8-9 and described in Table 8-11.

Return to Summary Table.

INA± Full-Scale Range Adjust register (default: 0xA000). This register is used to change the full-scale input voltage of the INA± input. Calibration must be performed after changing this register; see the *Section 6.3.1.2* section.

Figure 8-9. FS_RANGE_A Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FS_RANGE_A															
R/W-0xA000															

Table 8-11. FS_RANGE_A Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	FS_RANGE_A	R/W	0xA000	These bits enable adjustment of the analog full-scale range for INA±. 0x0000: Settings below 0x2000 result in degraded performance 0x2000: 500 mV_{PP} - Recommended minimum setting 0xA000: 800 mV_{PP} (default) 0xFFFF: 1000 mV_{PP} - Maximum setting

8.1.10 INB Full-Scale Range Adjust Register (Address = 0x032-0x033) [reset = 0xA000]

FS_RANGE_B is shown in Figure 8-10 and described in Table 8-12.

Return to Summary Table.

INB± Full-Scale Range Adjust register (default: 0xA000). This register is used to change the full-scale input voltage of the INB± input. Calibration must be performed after changing this register; see the *Section 6.3.1.2* section.

Figure 8-10. FS_RANGE_B Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FS_RANGE_B															
R/W-0xA000															

Table 8-12. FS_RANGE_B Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	FS_RANGE_B	R/W	0xA000	These bits enable adjustment of the analog full-scale range for INB±. 0x0000: Settings below 0x2000 result in degraded performance 0x2000: 500 mV_{PP} - Recommended minimum setting 0xA000: 800 mV_{PP} (default) 0xFFFF: 1000 mV_{PP} - Maximum setting

8.1.11 BG_BYPASS Register (Address = 0x038) [reset = 0x00]

BG_BYPASS is shown in Figure 8-11 and described in Table 8-13.

Return to Summary Table.

Band-Gap Bypass register (default: 0x00). This register can be used to bypass the internal reference and use the VA11 supply voltage instead.

Figure 8-11. BG_BYPASS Register

7	6	5	4	3	2	1	0
RESERVED							BG_BYPASS
R/W-0x0							R/W-0x0

Table 8-13. BG_BYPASS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0x0	Reserved
0	BG_BYPASS	R/W	0x0	When set, VA11 is used as the voltage reference instead of the band-gap voltage.

8.1.12 TMSTP_CTRL Register (Address = 0x03B) [reset = 0x00]

TMSTP_CTRL is shown in Figure 8-12 and described in Table 8-14.

Return to Summary Table.

TMSTP± and Differential SYNC Control register (default: 0x00). This register enables or disables the TMSTP± input and determines the termination scheme for this input.

Figure 8-12. TMSTP_CTRL Register

7	6	5	4	3	2	1	0
RESERVED						TMSTP_LVPECL_EN	TMSTP_RECV_EN
R/W-0x0						R/W-0x0	R/W-0x0

Table 8-14. SYNC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0x0	Reserved
1	TMSTP_LVPECL_EN	R/W	0x0	When set, this bit activates the DC-coupled, low-voltage PECL mode for the differential TMSTP± receiver; see the *Pin Functions* table.
0	TMSTP_RECV_EN	R/W	0x0	This bit enables the differential TMSTP± receiver.

8.1.13 LVDS_SWING Register (Address = 0x048) [reset = 0x00]

LVDS_SWING is shown in Figure 8-13 and described in Table 8-15.

Return to Summary Table.

LVDS Swing Mode register (default: 0x00). This register determines the operating mode of the LVDS output drivers.

Figure 8-13. LVDS_SWING Register

7	6	5	4	3	2	1	0
RESERVED						LVDS_SWING	
R/W-0x0						R/W-0x0	

Table 8-15. LVDS_SWING Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0x0	Reserved
1-0	LVDS_SWING	R/W	0x0	These bits set the swing mode of the LVDS output buffers: 0 : High-swing mode (HSM) (default) 1 : Low-swing mode (LSM) 2 : Reserved (do not use) 3 : Low-swing mode for use with receivers that have a high-Z load termination (HZM). Only use with short transmission lines to avoid reflections caused by a high-Z receiver.

8.1.14 INPUT_MUX Register (Address = 0x060) [reset = 0x01]

INPUT_MUX is shown in Figure 8-14 and described in Table 8-16.

Return to Summary Table.

Input Mux Control register (default: 0x01). This register controls the input used in single-channel mode and the swapping of inputs in dual-channel mode; see the *Section 6.3.1* section.

Figure 8-14. INPUT_MUX Register

7	6	5	4	3	2	1	0
RESERVED			DUAL_INPUT	RESERVED		SINGLE_INPUT	
R/W-0x0			R/W-0x0	R/W-0x0		R/W-0x1	

Table 8-16. INPUT_MUX Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0x0	Reserved
4	DUAL_INPUT	R/W	0x0	This bit selects the input for dual-channel mode (non-DES mode). Only applies if DES_EN = 0. 0 : Channel A samples INA±, channel B samples INB± (no swap) (default) 1 : Channel A samples INB±, channel B samples INA± (swap)
3-2	RESERVED	R/W	0x0	Reserved

Table 8-16. INPUT_MUX Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	SINGLE_INPUT	R/W	0x1	These bits define which chip input is sampled in single-channel mode (DES mode). Only applies if DES_EN = 1. 0 : Reserved 1 : INA± is sampled (DESA mode) 2 : INB± is sampled (DESB mode) 3 : Reserved

8.1.15 CAL_EN Register (Address = 0x61) [reset = 0x01]

CAL_EN is shown in Figure 8-15 and described in Table 8-17.

Return to Summary Table.

Calibration Enable register (default: 0x01). This register is used to enable or disable ADC core calibration.

Figure 8-15. CAL_EN Register

7	6	5	4	3	2	1	0
RESERVED							CAL_EN
R/W-0x0							R/W-0x1

Table 8-17. CAL_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0x0	Reserved
0	CAL_EN	R/W	0x1	This bit enables calibration. Set this bit high to run calibration. Set this bit low to hold calibration in reset to program new calibration settings. Clearing CAL_EN also resets the clock dividers that clock the encoders and LVDS interface. Note 1: Many calibration SPI registers are not synchronized to the internal clock that runs the calibration logic. Changing these registers may corrupt the calibration state machine. Always clear CAL_EN before making any changes to these registers. All registers with this requirement contain a note in their descriptions. After changing the registers, set CAL_EN to re-run calibration with the new settings. Note 2: Always set CAL_EN before setting LVDS_EN. Note 3: Always clear LVDS_EN before clearing CAL_EN.

8.1.16 CAL_CFG0 Register (Address = 0x062) [reset = 0x01]

CAL_CFG0 is shown in Figure 8-16 and described in Table 8-18.

Return to Summary Table.

Calibration Configuration 0 register (default: 0x01). This register controls offset calibration. Only change this register when CAL_EN is 0.

Figure 8-16. CAL_CFG0 Register

7	6	5	4	3	2	1	0
RESERVED					CAL_OS	RESERVED	CAL_FG
R/W-0x0					R/W-0x0	R/W-0x0	R/W-0x1

Table 8-18. CAL_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0x0	Reserved
2	CAL_OS	R/W	0x0	0 : Disable foreground offset calibration (default) 1 : Enable foreground offset calibration (requires CAL_FG to be set)
1	RESERVED	R/W	0x0	Reserved
0	CAL_FG	R/W	0x1	0 : Reset calibration values, skip foreground calibration. 1 : Reset calibration values, then run foreground calibration (default).

8.1.17 CAL_AVG Register (Address = 0x68) [reset = 0x61]

CAL_AVG is shown in Figure 8-17 and described in Table 8-19.

Return to Summary Table.

Calibration Averaging register (default: 0x61). This address determines the amount of averaging used for offset calibration.

Figure 8-17. CAL_AVG Register

7	6	5	4	3	2	1	0
RESERVED	OS_AVG			RESERVED			
R/W-0x0	R/W-0x6			R-0x1			

Table 8-19. CAL_AVG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	Reserved
6-4	OS_AVG	R/W	0x6	Select the amount of averaging used for each measurement of the offset correction search. A larger number corresponds to more averaging.
3-0	RESERVED	R	0x1	Always write 0x1.

8.1.18 CAL_STATUS Register (Address = 0x06A) [reset = Undefined]

CAL_STATUS is shown in Figure 8-18 and described in Table 8-20.

Return to Summary Table.

Calibration Status register (default: Undefined) (read-only). This register is used to read out the calibration status information.

Figure 8-18. CAL_STATUS Register

7	6	5	4	3	2	1	0
RESERVED			CAL_STAT			CAL_STOPPED	FG_DONE
R-Undefined			R-Undefined			R-Undefined	R-Undefined

Table 8-20. CAL_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	Undefined	Reserved
4-2	CAL_STAT	R	Undefined	Calibration status code
1	CAL_STOPPED	R	Undefined	This bit is set when foreground calibration is completed or skipped.
0	FG_DONE	R	Undefined	This bit is high to indicate that foreground calibration has completed (or was skipped).

8.1.19 CAL_PIN_CFG Register (Address = 0x06B) [reset = 0x00]

CAL_PIN_CFG is shown in Figure 8-19 and described in Table 8-21.

Return to Summary Table.

Calibration Pin Configuration register (default: 0x00). This register sets the function of the CALSTAT pin and selects whether hardware or software CALTRIG is used.

Figure 8-19. CAL_PIN_CFG Register

7	6	5	4	3	2	1	0
RESERVED					CAL_STATUS_SEL		CAL_TRIG_EN
R/W-0x0					R/W-0x0		R/W-0x0

Table 8-21. CAL_PIN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0x0	Reserved
2-1	CAL_STATUS_SEL	R/W	0x0	0 : CALSTAT output pin matches FG_DONE 1 : CALSTAT output pin matches CAL_STOPPED 2 : CALSTAT output pin matches ALARM 3 : CALSTAT output is always low
0	CAL_TRIG_EN	R/W	0x0	This bit selects the hardware or software trigger source. 0 : Use the CAL_SOFT_TRIG register for the calibration trigger. The CALTRIG input is disabled (ignored). 1 : Use the CALTRIG input for the calibration trigger. The CAL_SOFT_TRIG register is ignored.

8.1.20 CAL_SOFT_TRIG Register (Address = 0x06C) [reset = 0x01]

CAL_SOFT_TRIG is shown in Figure 8-20 and described in Table 8-22.

Return to Summary Table.

Calibration Software Trigger register (default: 0x01). This register is used as the software CALTRIG.

Figure 8-20. CAL_SOFT_TRIG Register

7	6	5	4	3	2	1	0
RESERVED							CAL_SOFT_TRIG
R/W-0x0							R/W-0x1

Table 8-22. CAL_SOFT_TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0x0	Reserved
0	CAL_SOFT_TRIG	R/W	0x1	CAL_SOFT_TRIG is a software bit to provide the functionality of the CALTRIG input when there are no hardware resources to drive CALTRIG. Program CAL_TRIG_EN = 0 to use CAL_SOFT_TRIG for the calibration trigger. Note: If no calibration trigger is needed, leave CAL_TRIG_EN = 0 and CAL_SOFT_TRIG = 1 (trigger set high).

8.1.21 CAL_DATA_EN Register (Address = 0x70) [reset = 0x00]

CAL_DATA_EN is shown in Figure 8-21 and described in Table 8-23.

Return to Summary Table.

Calibration Data Enable register (default: 0x00). This register enables reading calibration data.

Figure 8-21. CAL_DATA_EN Register

7	6	5	4	3	2	1	0
RESERVED							CAL_DATA_EN
R/W-0x0							R/W-0x0

Table 8-23. CAL_DATA_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0x0	Reserved
0	CAL_DATA_EN	R/W	0x0	Set this bit to enable the CAL_DATA register to enable reading and writing of calibration data; see the CAL_DATA register for more information.

8.1.22 CAL_DATA Register (Address = 0x71) [reset = Undefined]

CAL_DATA is shown in Figure 8-22 and described in Table 8-24.

Return to Summary Table.

Calibration Data register (default: Undefined). This register is used to read out the calibration data.

Figure 8-22. CAL_DATA Register

7	6	5	4	3	2	1	0
CAL_DATA							
R/W-0x0							

Table 8-24. CAL_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CAL_DATA	R/W	0x0	After setting CAL_DATA_EN, repeated reads of this register return all calibration values for the ADCs. Repeated writes of this register input all calibration values for the ADCs. To read the calibration data, read the register 673 times. To write the vector, write the register 673 times with previously stored calibration data. To speed up the read or write operation, set ADDR_HOLD = 1 and use streaming read or write process. IMPORTANT: Accessing the CAL_DATA register when CAL_STOPPED = 0 corrupts the calibration. Also, stopping the process before reading or writing 673 times leaves the calibration data in an invalid state.

8.1.23 GAIN_TRIM_A Register (Address = 0x07A) [reset = Undefined]

GAIN_TRIM_A is shown in Figure 8-23 and described in Table 8-25.

Return to Summary Table.

Gain DAC Trim A register (default from fuse ROM). This register is used for trimming the INA± gain.

Figure 8-23. GAIN_TRIM_A Register

7	6	5	4	3	2	1	0
GAIN_TRIM_A							
R/W-Undefined							

Table 8-25. GAIN_TRIM_A Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GAIN_TRIM_A	R/W	Undefined	This register enables gain trim of channel A. After reset, the factory trimmed value can be read and adjusted as required. Use FS_RANGE_A to adjust the analog full-scale voltage (V_{fs}) of INA±.

8.1.24 GAIN_TRIM_B Register (Address = 0x07B) [reset = Undefined]

GAIN_TRIM_B is shown in Figure 8-24 and described in Table 8-26.

Return to Summary Table.

Gain DAC Trim B register (default from fuse ROM). This register is used for trimming the INB± gain.

Figure 8-24. GAIN_TRIM_B Register

7	6	5	4	3	2	1	0
GAIN_TRIM_B							
R/W-Undefined							

Table 8-26. GAIN_TRIM_B Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GAIN_TRIM_B	R/W	Undefined	This register enables gain trim of channel B. After reset, the factory trimmed value can be read and adjusted as required. Use FS_RANGE_B to adjust the analog full-scale voltage (V_{fs}) of INB±.

8.1.25 BG_TRIM Register (Address = 0x07C) [reset = Undefined]

BG_TRIM is shown in Figure 8-25 and described in Table 8-27.

Return to Summary Table.

Band-Gap Trim register (default from fuse ROM). Use this register to trim the internal band-gap reference. The voltage can be measured on the BG pin.

Figure 8-25. BG_TRIM Register

7	6	5	4	3	2	1	0
RESERVED				BG_TRIM			
R/W-0x0				R/W-Undefined			

Table 8-27. BG_TRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0x0	Reserved
3-0	BG_TRIM	R/W	Undefined	This register enables trimming of the internal band-gap reference. After reset, the factory trimmed value can be read and adjusted as required.

8.1.26 RTRIM_A Register (Address = 0x07E) [reset = Undefined]

RTRIM_A is shown in Figure 8-26 and described in Table 8-28.

Return to Summary Table.

Resistor TRIM for INA± register (default from fuse ROM). This register can be used to trim the input termination resistance of INA±.

Figure 8-26. RTRIM_A Register

7	6	5	4	3	2	1	0
RTRIM_A							
R/W-Undefined							

Table 8-28. RTRIM_A Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RTRIM_A	R/W	Undefined	This register controls the INA± ADC input termination trim. After reset, the factory trimmed value can be read and adjusted as required.

8.1.27 RTRIM_B Register (Address = 0x7F) [reset = Undefined]

RTRIM_B is shown in Figure 8-27 and described in Table 8-29.

Return to Summary Table.

Resistor TRIM for INB± (default from fuse ROM). This register can be used to trim the input termination resistance of INB±.

Figure 8-27. RTRIM_B Register

7	6	5	4	3	2	1	0
RTRIM_B							
R/W-Undefined							

Table 8-29. RTRIM_B Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RTRIM_B	R/W	Undefined	This register controls the INB± ADC input termination trim. After reset, the factory trimmed value can be read and adjusted as required.

8.1.28 ADC_DITH Register (Address = 0x9D) [reset = 0x01]

ADC_DITH is shown in Figure 8-28 and described in Table 8-30.

Return to Summary Table.

ADC Dither register (default: 0x01). This register can be used enable or disable ADC dither and to adjust the amount of dither used.

Figure 8-28. ADC_DITH Register

7	6	5	4	3	2	1	0
RESERVED					ADC_DITH_ERR	ADC_DITH_AMP	ADC_DITH_EN
R/W-0x00					0x0	0x0	0x1

Table 8-30. ADC_DITH Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0x00	Reserved
2	ADC_DITH_ERR	R/W	0x0	Small rounding errors may occur when subtracting the dither signal. The error can be chosen to either slightly degrade SNR or to slightly increase the DC offset and $F_S/2$ spur. In addition, the $F_S/4$ spur will also be increased slightly while in single channel mode. 0 : Rounding error degrades SNR 1 : Rounding error degrades DC offset, $F_S/2$ spur and $F_S/4$ spur
1	ADC_DITH_AMP	R/W	0x0	0 : Small dither for better SNR (default) 1 : Large dither for better spurious performance
0	ADC_DITH_EN	R/W	0x1	Set this bit to enable ADC dither. Dither can improve spurious performance at the expense of slightly degraded SNR. The dither amplitude (ADC_DITH_AMP) can be used to further tradeoff SNR and spurious performance.

8.1.29 Timing Adjustment for Bank 0 (0° Clock) Register (Address = 0x102) [reset = Undefined]

B0_TIME_0 is shown in Figure 8-29 and described in Table 8-31.

Return to Summary Table.

Timing Adjustment for Bank 0 (0° clock) register (default from fuse ROM). This register is used to adjust the timing of the Bank 0 ADC when ADC A is configured for a 0° clock phase (dual channel mode).

Figure 8-29. B0_TIME_0 Register

7	6	5	4	3	2	1	0
B0_TIME_0							
R/W-Undefined							

Table 8-31. B0_TIME_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B0_TIME_0	R/W	Undefined	Timing adjustment for bank 0 when ADC A is configured for 0° clock phase (dual channel mode).

8.1.30 Timing Adjustment for Bank 0 (90° Clock) Register (Address = 0x103) [reset = Undefined]

B0_TIME_90 is shown in Figure 8-30 and described in Table 8-32.

Return to Summary Table.

Timing Adjustment for Bank 0 (–90° clock) register (default from fuse ROM). This register is used to adjust the timing of the Bank 0 ADC when ADC A is configured for a –90° clock phase (single channel mode).

Figure 8-30. B0_TIME_90 Register

7	6	5	4	3	2	1	0
B0_TIME_90							
R/W-Undefined							

Table 8-32. B0_TIME_90 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B0_TIME_90	R/W	Undefined	Time adjustment for bank 0 applied when ADC is configured for –90° clock phase (single channel mode).

8.1.31 Timing Adjustment for Bank 1 (0° Clock) Register (Address = 0x112) [reset = Undefined]

B1_TIME_0 is shown in Figure 8-31 and described in Table 8-33.

Return to Summary Table.

Timing Adjustment for Bank 1 (0° clock) register (default from fuse ROM). This register is used to adjust the timing of the Bank 1 ADC when ADC A is configured for a 0° clock phase (dual channel mode).

Figure 8-31. B1_TIME_0 Register

7	6	5	4	3	2	1	0
B1_TIME_0							
R/W-Undefined							

Table 8-33. B1_TIME_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B1_TIME_0	R/W	Undefined	Timing adjustment for bank 1 applied when ADC is configured for 0° clock phase (dual channel mode).

8.1.32 Timing Adjustment for Bank 1 (90° Clock) Register (Address = 0x113) [reset = Undefined]

B1_TIME_90 is shown in Figure 8-32 and described in Table 8-34.

Return to Summary Table.

Timing Adjustment for Bank 1 (–90° clock) register (default from fuse ROM). This register is used to adjust the timing of the Bank 1 ADC when ADC A is configured for a –90° clock phase (single channel mode).

Figure 8-32. B1_TIME_90 Register

7	6	5	4	3	2	1	0
B1_TIME_90							
R/W-Undefined							

Table 8-34. B1_TIME_90 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B1_TIME_90	R/W	Undefined	Time adjustment for bank 1 applied when ADC is configured for –90° clock phase (single channel mode).

8.1.33 Timing Adjustment for Bank 4 (0° Clock) Register (Address = 0x142) [reset = Undefined]

B4_TIME_0 is shown in Figure 8-33 and described in Table 8-35.

Return to Summary Table.

Timing Adjustment for Bank 4 (0° clock) register (default from fuse ROM). This register is used to adjust the timing of the Bank 4 ADC when ADC B is configured for a 0° clock phase (dual channel mode and single channel mode).

Figure 8-33. B4_TIME_0 Register

7	6	5	4	3	2	1	0
B4_TIME_0							
R/W-Undefined							

Table 8-35. B4_TIME_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B4_TIME_0	R/W	Undefined	Timing adjustment for bank 4 applied when ADC is configured for 0° clock phase (dual channel mode and single channel mode).

8.1.34 Timing Adjustment for Bank 5 (0° Clock) Register (Address = 0x152) [reset = Undefined]

B5_TIME_0 is shown in Figure 8-34 and described in Table 8-36.

Return to Summary Table.

Timing Adjustment for Bank 5 (0° clock) register (default from fuse ROM). This register is used to adjust the timing of the Bank 5 ADC when ADC B is configured for a 0° clock phase (dual channel mode and single channel mode).

Figure 8-34. B5_TIME_0 Register

7	6	5	4	3	2	1	0
B5_TIME_0							
R/W-Undefined							

Table 8-36. B5_TIME_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B5_TIME_0	R/W	Undefined	Timing adjustment for bank 5 applied when ADC is configured for 0° clock phase (dual channel mode and single channel mode).

8.1.35 LSB_CTRL Register (Address = 0x160) [reset = 0x00]

LSB_CTRL is shown in Figure 8-35 and described in Table 8-37.

Return to Summary Table.

LSB Control Bit Output register (default: 0x00). This register enables output of the timestamp signal on the LSB of the output samples.

Figure 8-35. LSB_CTRL Register

7	6	5	4	3	2	1	0
RESERVED							TIME_STAMP_EN
R/W-0x0							R/W-0x0

Table 8-37. LSB_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0x0	Reserved
0	TIME_STAMP_EN	R/W	0x0	When set, the timestamp signal is transmitted on the LSB of the output samples. The latency of the timestamp signal (through the entire chip) matches the latency of the analog ADC inputs. Also set SYNC_RECV_EN when using TIME_STAMP_EN.

8.1.36 LSB_SEL Register (Address = 0x161) [reset = 0x00]

LSB_SEL is shown in Figure 8-36 and described in Table 8-38.

Return to Summary Table.

LSB Control Bit Position register (default: 0x00). This register defines the position of the timestamp signal output on the LSB of the samples.

Figure 8-36. LSB_SEL Register

7	6	5	4	3	2	1	0
RESERVED							LSB_SEL
R/W-0x0							R/W-0x0

Table 8-38. LSB_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0x0	Reserved
0	LSB_SEL	R/W	0x0	0 : Place timestamp on lane 0 (Dx0±) of each LVDS output bus, independent of the LWIDTH setting. Lane 0 of each bus is enabled regardless of LWIDTH. 1 : Place timestamp on the LSB of the effective sample size as set by the LWIDTH parameter. The timestamp is placed on the LSB of the output sample. The lane that carries timestamp depends on the selected output sample width (LWIDTH). For 12-bit samples, lane 0 carries the control data. For 11-bit samples, lane 1 carries the control data. For 10-bit samples, lane 2 carries the control data. For 8-bit samples, lane 4 carries the control data.

8.1.37 UPAT0 Register (Address = 0x180) [reset = 0x0000]

UPAT0 is shown in Figure 8-37 and described in Table 8-39.

Return to Summary Table.

User-Defined Pattern (sample 0) register (default: 0x0000). This register, and the UPATx registers that follow, define the user defined test pattern that can be used to test various aspects of the LVDS interface.

Figure 8-37. UPAT0 Register

15	14	13	12	11	10	9	8
RESERVED				UPAT0			
R/W-0x0				R/W-0x0			
7	6	5	4	3	2	1	0
UPAT0							
R/W-0x0							

Table 8-39. UPAT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0x0	Reserved
11-0	UPAT0	R/W	0x0	Defines the value for sample 0 of the user defined pattern. See the PAT_SEL register and the *Section 6.4.5.6* section. Note: Only change this register when LVDS_EN = 0.

8.1.38 UPAT1 Register (Address = 0x182) [reset = 0x0FFF]

UPAT1 is shown in Figure 8-38 and described in Table 8-40.

Return to Summary Table.

User-Defined Pattern (sample 1) register (default: 0x0FFF).

Figure 8-38. UPAT1 Register

15	14	13	12	11	10	9	8
RESERVED				UPAT1			
R/W-0x0				R/W-0xF			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UPAT1							
R/W-0xFF							

Table 8-40. UPAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0x0	Reserved
11-0	UPAT1	R/W	0xFFF	Defines the value for sample 1 of the user defined pattern. See UPAT0 register. Note: Only change this register when LVDS_EN = 0.

8.1.39 UPAT2 Register (Address = 0x184) [reset = 0x0000]

UPAT2 is shown in Figure 8-39 and described in Table 8-41.

Return to Summary Table.

User-Defined Pattern (sample 2) register (default: 0x0000).

Figure 8-39. UPAT2 Register

15	14	13	12	11	10	9	8
RESERVED				UPAT2			
R/W-0x0				R/W-0x0			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UPAT2							
R/W-0x00							

Table 8-41. UPAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0x0	Reserved
11-0	UPAT2	R/W	0x000	Defines the value for sample 2 of the user defined pattern. See UPAT0 register. Note: Only change this register when LVDS_EN = 0.

8.1.40 UPAT3 Register (Address = 0x186) [reset = 0x0FFF]

UPAT3 is shown in Figure 8-40 and described in Table 8-42.

Return to Summary Table.

User-Defined Pattern (sample 3) register (default: 0x0FFF)

Figure 8-40. UPAT3 Register

15	14	13	12	11	10	9	8
RESERVED				UPAT3			
R/W-0x0				R/W-0xF			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UPAT3							
R/W-0xFF							

Table 8-42. UPAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0x0	Reserved
11-0	UPAT3	R/W	0xFFF	Defines the value for sample 3 of the user defined pattern. See UPAT0 register. Note: Only change this register when LVDS_EN = 0.

8.1.41 UPAT4 Register (Address = 0x188) [reset = 0x0000]

UPAT4 is shown in Figure 8-41 and described in Table 8-43.

Return to Summary Table.

User-Defined Pattern (sample 4) register (default: 0x0000).

Figure 8-41. UPAT4 Register

15	14	13	12	11	10	9	8
RESERVED				UPAT4			
R/W-0x0				R/W-0x0			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UPAT4							
R/W-0x00							

Table 8-43. UPAT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0x0	Reserved
11-0	UPAT4	R/W	0x000	Defines the value for sample 4 of the user defined pattern. See UPAT0 register. Note: Only change this register when LVDS_EN = 0.

8.1.42 UPAT5 Register (Address = 0x18A) [reset = 0x0FFF]

UPAT5 is shown in Figure 8-42 and described in Table 8-44.

Return to Summary Table.

User-Defined Pattern (sample 5) register (default: 0x0FFF).

Figure 8-42. UPAT5 Register

15	14	13	12	11	10	9	8
RESERVED				UPAT5			
R/W-0x0				R/W-0xF			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UPAT5							
R/W-0xFF							

Table 8-44. UPAT5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0x0	Reserved
11-0	UPAT5	R/W	0xFFF	Defines the value for sample 5 of the user defined pattern. See UPAT0 register. Note: Only change this register when LVDS_EN = 0.

8.1.43 UPAT6 Register (Address = 0x18C) [reset = 0x0000]

UPAT6 is shown in Figure 8-43 and described in Table 8-45.

Return to Summary Table.

User-Defined Pattern (sample 6) register (default: 0x0000).

Figure 8-43. UPAT6 Register

15	14	13	12	11	10	9	8
RESERVED				UPAT6			
R/W-0x0				R/W-0x0			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UPAT6							
R/W-0x00							

Table 8-45. UPAT6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0x0	Reserved
11-0	UPAT6	R/W	0x000	Defines the value for sample 6 of the user defined pattern. See UPAT0 register. Note: Only change this register when LVDS_EN = 0.

8.1.44 UPAT7 Register (Address = 0x18E) [reset = 0x0FFF]

UPAT7 is shown in Figure 8-44 and described in Table 8-46.

Return to Summary Table.

User-Defined Pattern (sample 7) register (default: 0x0FFF).

Figure 8-44. UPAT7 Register

15	14	13	12	11	10	9	8
RESERVED				UPAT7			
R/W-0x0				R/W-0xF			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UPAT7							
R/W-0xFF							

Table 8-46. UPAT7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0x0	Reserved
11-0	UPAT7	R/W	0xFFF	Defines the value for sample 7 of the user defined pattern. See UPAT0 register. Note: Only change this register when LVDS_EN = 0.

8.1.45 UPAT_CTRL Register (Address = 0x190) [reset = 0x1E]

UPAT_CTRL is shown in Figure 8-45 and described in Table 8-47.

Return to Summary Table.

User-Defined Pattern Control register (default: 0x1E). This register allows selection of the predefined lane pattern instead of the user defined pattern and the inversion of specified bits for each lane during user defined pattern transmission.

Figure 8-45. UPAT_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			LANE_PAT	UPAT_INV_D	UPAT_INV_C	UPAT_INV_B	UPAT_INV_A
R/W-0x0			R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x0

Table 8-47. UPAT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0x0	Reserved
4	LANE_PAT	R/W	0x1	When set, the UPATn registers are ignored, and the user-defined pattern is set to: 0x000, 0xFFF, 0x000, 0x000, 0x000, 0xFFF, 0xFFF, 0xFFF. This bit acts as a shortcut to avoid programming the UPATn registers. PAT_SEL register must still be programmed to configure the interface to select the user-defined pattern. The UPAT_INV_* registers still apply when using LANE_PAT.
3	UPAT_INV_D	R/W	0x1	When set, bit [11] of the user-defined pattern is inverted on the bus D output.
2	UPAT_INV_C	R/W	0x1	When set, bit [10] of the user-defined pattern is inverted on the bus C output.
1	UPAT_INV_B	R/W	0x1	When set, bit [9] of the user-defined pattern is inverted on the bus B output.

Table 8-47. UPAT_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	UPAT_INV_A	R/W	0x0	When set, bit [8] of the user-defined pattern is inverted on the bus A output. Note: Only change this register when LVDS_EN = 0.

8.1.46 LVDS_EN Register (Address = 0x200) [reset = 0x01]

LVDS_EN is shown in Figure 8-46 and described in Table 8-48.

Return to Summary Table.

LVDS Subsystem Enable register (default: 0x01). Use this register to enable or disable the LVDS interface.

Figure 8-46. LVDS_EN Register

7	6	5	4	3	2	1	0
RESERVED							LVDS_EN
R/W-0x0							R/W-0x1

Table 8-48. LVDS_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0x0	Reserved
0	LVDS_EN	R/W	0x1	0 : Disable LVDS interface 1 : Enable LVDS interface Note 1: Before altering other LVDS registers, you must clear LVDS_EN. When LVDS_EN is 0, the LVDS interface block is held in reset and the outputs are powered down. The clocks are gated off to save power. The frame counter is also held in reset, so SYSREF will not align the frame counter. Note 2: Always set CAL_EN before setting LVDS_EN. Note 3: Always clear LVDS_EN before clearing CAL_EN.

8.1.47 LMODE Register (Address = 0x201) [reset = 0x01]

LMODE is shown in Figure 8-47 and described in Table 8-49.

Return to Summary Table.

LVDS Mode register (default: 0x01). This register is used to define the configuration of the LVDS interface. LVDS_EN must be 0 before making any changes to this register. Additionally, CAL_EN must be 0 before changing DES_EN.

Figure 8-47. LMODE Register

7	6	5	4	3	2	1	0
RESERVED		LWIDTH		RESERVED	DES_EN	LALIGNED	LDEMUX
R/W-0x0		R/W-0x0		R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x1

Table 8-49. LMODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0x0	Reserved
5-4	LWIDTH	R/W	0x0	Specifies the sample width for the LVDS output interface. 0 : 12-bit sample width (default) 1 : 11-bit sample width 2 : 10-bit sample width 3 : 8-bit sample width
3	RESERVED	R/W	0x0	Reserved
2	DES_EN	R/W	0x0	0 : Disable DES mode (enable dual channel mode) 1 : Enable DES mode (enable single channel mode) CAL_EN must be 0 before changing DES_EN.
1	LALIGNED	R/W	0x0	0 : The LVDS buses are staggered for optimized switching noise and latency. 1 : The LVDS buses are aligned for simplified timing.
0	LDEMUX	R/W	0x1	0 : Demux-by-1, uses 2 LVDS buses total 1 : Demux-by-2, uses 4 LVDS buses total

8.1.48 LFRAME Register (Address = 0x202) [reset = 0x80]

LFRAME is shown in Figure 8-48 and described in Table 8-50.

Return to Summary Table.

LVDS Frame Length register (default: 0x80) (128 decimal). This register sets the length of the frame and subsequently the period of the strobe signal. Only change this register when LVDS_EN = 0.

Figure 8-48. LFRAME Register

7	6	5	4	3	2	1	0
LFRAME							
R/W-0x80							

Table 8-50. LFRAME Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LFRAME	R/W	0x80	Defines the number of UIs in each LVDS frame. Any multiple of 4 from 4 to 128 is supported. All other values are unsupported. When LDEMUX=0, one UI is one CLK± cycle. When LDEMUX=1, one UI is two CLK± cycles. Note: Setting LFRAME to 4 is not recommended, as it may be difficult to achieve deterministic latency over all process, voltage, and temperature conditions. The propagation delay variation may be larger than the frame period.

8.1.49 LSYNC_N Register (Address = 0x203) [reset = 0x01]

LSYNC_N is shown in Figure 8-49 and described in Table 8-51.

Return to Summary Table.

LVDS Manual Sync Request register (default: 0x01). This register can be used as a software replacement for the LVDS $\overline{\text{SYNC}}$ signal.

Figure 8-49. LSYNC_N Register

7	6	5	4	3	2	1	0
RESERVED							LSYNC_N
R/W-0x0							R/W-0x1

Table 8-51. LSYNC_N Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0x0	Reserved
0	LSYNC_N	R/W	0x1	Set this bit to 0 to request LVDS synchronization (equivalent to the hardware $\overline{\text{SYNC}}$ signal being asserted, as selected by SYNC_SEL). For normal operation, leave this bit set to 1. Note: The LSYNC_N register can always generate a synchronization request, regardless of the SYNC_SEL setting in the LCTRL register. However, if the selected sync pin is stuck low, the synchronization request cannot be de-asserted unless SYNC_SEL=2.

8.1.50 LCTRL Register (Address = 0x204) [reset = 0x02]

LCTRL is shown in Figure 8-50 and described in Table 8-52.

Return to Summary Table.

LVDS Control register (default: 0x02). This register is used to configure aspects of the LVDS interface including scrambling, hardware $\overline{\text{SYNC}}$ input and the output format. Only change this register when LVDS_EN = 0.

Figure 8-50. LCTRL Register

7	6	5	4	3	2	1	0
RESERVED			SCR	SYNC_SEL		SFORMAT	RESERVED
R/W-0x0			R/W-0x0	R/W-0x0		R/W-0x1	R/W-0x0

Table 8-52. LCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0x0	Reserved
4	SCR	R/W	0x0	When set, all LVDS data and strobes are scrambled. This also includes the part-time strobes or timestamp signals (since they are output on the data lanes). See the *Section 6.4.5.5* section.
3-2	SYNC_SEL	R/W	0x0	0 : Use the $\overline{\text{SYNC\_SE}}$ input for $\overline{\text{SYNC}}$ function (default) 1 : Use the TMSTP± input for $\overline{\text{SYNC}}$ function. also set SYNC_RECV_EN to use the differential TMSTP± input. 2 : Do not use any $\overline{\text{SYNC}}$ input pin, set if using LSYNC_N.
1	SFORMAT	R/W	0x1	Output sample format for LVDS output samples 0 : Offset binary 1 : Signed 2's complement (default)
0	RESERVED	R/W	0x0	Reserved

8.1.51 PAT_SEL Register (Address = 0x205) [reset = 0x02]

PAT_SEL is shown in Figure 8-51 and described in Table 8-53.

Return to Summary Table.

LVDS Pattern Control register (default: 0x02). This register controls the output data or pattern used during active mode ($\overline{\text{SYNC}}$ de-asserted) and sync mode ($\overline{\text{SYNC}}$ asserted). During normal operation, the active pattern should be set to the ADC output data and the $\overline{\text{SYNC}}$ pattern can be set to the mode used by the receiver for synchronizing the interface. The input used for $\overline{\text{SYNC}}$ is chosen by SYNC_SEL.

Figure 8-51. PAT_SEL Register

7	6	5	4	3	2	1	0
ACT_PAT				SYNC_PAT			
R/W-0x0				R/W-0x2			

Table 8-53. PAT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	ACT_PAT	R/W	0x0	This selects the output pattern that is generated when the $\overline{\text{SYNC}}$ signal is de-asserted. 0: ADC output data 1: All LVDS lanes output the user-defined pattern (see UPAT registers) 2-15: Reserved
3-0	SYNC_PAT	R/W	0x2	This selects the output pattern that is generated when the $\overline{\text{SYNC}}$ signal is asserted. 0: Reserved 1: All LVDS lanes output the user-defined pattern (see UPAT registers) 2: Frame strobe is transmitted on the LSB of the output samples only. The other bits transmit data based on ACT_PAT. 3: The frame strobe is transmitted on all active LVDS data lanes and strobes. 4-15: Reserved

8.1.52 LCS_EN Register (Address = 0x206) [reset = 0xFF]

LCS_EN is shown in Figure 8-52 and described in Table 8-54.

Return to Summary Table.

LVDS Clock and Strobe Enables register (default: 0xFF). Use these registers to enable or disable specific LVDS output clocks (DxCLK±) and frame strobes (DxSTB±) if the receiver will not use them. If an entire LVDS bus is disabled (because of PD_CH or LDEMUX) then its associated clock and frame strobe are disabled automatically, regardless of this register. Note: Only change this register when LVDS_EN = 0.

Figure 8-52. LCS_EN Register

7	6	5	4	3	2	1	0
DDSTB_EN	DCSTB_EN	DBSTB_EN	DASTB_EN	DDCLK_EN	DCCLK_EN	DBCLK_EN	DACLK_EN
R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1

Table 8-54. LCS_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DDSTB_EN	R/W	0x1	Enable DDSTB± output
6	DCSTB_EN	R/W	0x1	Enable DCSTB± output
5	DBSTB_EN	R/W	0x1	Enable DBSTB± output
4	DASTB_EN	R/W	0x1	Enable DASTB± output
3	DDCLK_EN	R/W	0x1	Enable DDCLK± output
2	DCCLK_EN	R/W	0x1	Enable DCCLK± output
1	DBCLK_EN	R/W	0x1	Enable DBCLK± output
0	DACLK_EN	R/W	0x1	Enable DACLK± output

8.1.53 LVDS_STATUS Register (Address = 0x208) [reset = Undefined]

LVDS_STATUS is shown in Figure 8-53 and described in Table 8-55.

Return to Summary Table.

System Status register (default: undefined). This register returns status bits for the device including $\overline{\text{SYNC}}$ status for the LVDS interface and internal clock status.

Figure 8-53. LVDS_STATUS Register

7	6	5	4	3	2	1	0
RESERVED		SYNC_STATUS	REALIGNED	ALIGNED	RESERVED		
R/W-0x0		R/W-Undefined	R/W-Undefined	R/W-Undefined	R/W-0x0		

Table 8-55. LVDS_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0x0	Reserved
5	SYNC_STATUS	R/W	Undefined	Returns the instantaneous state of the LVDS interface $\overline{\text{SYNC}}$ signal ($\overline{\text{SYNC\_SE}}$ or TMSTP±). 0 : $\overline{\text{SYNC}}$ asserted 1 : $\overline{\text{SYNC}}$ de-asserted
4	REALIGNED	R/W	Undefined	When high, indicates that SYSREF realigned internal clocks. REALIGNED_ALM should be used for monitoring of realignment events instead of this bit. Writing a 1 to this bit will clear it, but will not affect the REALIGNED_ALM bit.
3	ALIGNED	R/W	Undefined	When high, indicates that internal clock phases have been established by SYSREF. Any SYSREF rising edge that is processed after enabling the LVDS system will set this bit. This bit can be monitored during startup to verify that SYSREF has been processed before continuing system initialization. Writing a 1 to this bit will clear it and the next SYSREF event will set it again.
2-0	RESERVED	R/W	0x0	Reserved

8.1.54 PD_CH Register (Address = 0x209) [reset = 0x00]

PD_CH is shown in Figure 8-54 and described in Table 8-56.

Return to Summary Table.

ADC Channel Power Down (default: 0x00). This register allows individual channels to be powered down. LVDS_EN and CAL_EN must be set to 0 before changing PD_CH.

Figure 8-54. PD_CH Register

7	6	5	4	3	2	1	0
RESERVED						PD_BCH	PD_ACH
R/W-0x0						R/W-0x0	R/W-0x0

Table 8-56. PD_CH Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0x0	Reserved
1	PD_BCH	R/W	0x0	When set, the “B” ADC channel is powered down.

Table 8-56. PD_CH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PD_ACH	R/W	0x0	When set, the “A” ADC channel is powered down. Important notes: LVDS_EN and CAL_EN must be set to 0 before changing PD_CH. PD_CH disables the LVDS lanes (Dx[11:0], DxSTB, DxCLK) for the powered down channel. To power down both ADC channels, use MODE or the PD pin.

8.1.55 OVR_T0 Register (Address = 0x211) [reset = 0xF2]

OVR_T0 is shown in Figure 8-55 and described in Table 8-57.

Return to Summary Table.

Overrange Threshold 0 register (default: 0xF2). This register sets threshold 0 for ADC overrange detection.

Figure 8-55. OVR_T0 Register

7	6	5	4	3	2	1	0
OVR_T0							
R/W-0xF2							

Table 8-57. OVR_T0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OVR_T0	R/W	0xF2	This parameter defines the absolute sample level that causes OVA0 or OVB0 to be set. The detection level in dBFS (peak) is 20log10(OVR_T0/256) (default: 0xF2 = 242 –> -0.5dBFS)

8.1.56 OVR_T1 Register (Address = 0x212) [reset = 0xAB]

OVR_T1 is shown in Figure 8-56 and described in Table 8-58.

Return to Summary Table.

Overrange Threshold 1 register (default: 0xAB). This register sets threshold 1 for ADC overrange detection.

Figure 8-56. OVR_T1 Register

7	6	5	4	3	2	1	0
OVR_T1							
R/W-0xAB							

Table 8-58. OVR_T1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OVR_T1	R/W	0xAB	This parameter defines the absolute sample level that causes OVA1 or OVB1 to be set. The detection level in dBFS (peak) is 20log10(OVR_T1/256) (default: 0xAB = 171 –> -3.5dBFS)

8.1.57 OVR_CFG Register (Address = 0x213) [reset = 0x07]

OVR_CFG is shown in Figure 8-57 and described in Table 8-59.

Return to Summary Table.

Overrange Enable/Hold Off register (default: 0x07). This register enables overrange detection and sets the output pulse duration for an overrange event. The maximum overrange pulse duration is recommended to avoid excess switching noise.

Figure 8-57. OVR_CFG Register

7	6	5	4	3	2	1	0
RESERVED				OVR_EN	OVR_N		
R/W-0x0				R/W-0x0	R/W-0x7		

Table 8-59. OVR_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0x0	Reserved
3	OVR_EN	R/W	0x0	ORA0, ORA1, ORB0 and ORB1 outputs pins are enabled and output the overrange status when this bit is set high. The outputs are held low when this bit is set low.
2-0	OVR_N	R/W	0x7	Program this register to adjust the pulse length for the ORA0, ORA1 and ORB0, ORB1 outputs. The minimum pulse duration of the overrange outputs is 8×2^{OVR_N} CLK± cycles.

8.1.58 SRC_EN Register (Address = 0x2B0) [reset = 0x00]

SRC_EN is shown in Figure 8-58 and described in Table 8-60.

Return to Summary Table.

SYSREF Calibration Enable register (default: 0x00). This register starts the SYSREF calibration process.

Figure 8-58. SRC_EN Register

7	6	5	4	3	2	1	0
RESERVED							SRC_EN
R/W-0x0							R/W-0x0

Table 8-60. SRC_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0x0	Reserved
0	SRC_EN	R/W	0x0	0 : SYSREF calibration disabled (default). Use the TAD register to manually control the t_{AD} Adjust setting and adjust the CLK± aperture delay. 1: SYSREF calibration enabled. The CLK± delay is automatically calibrated. The TAD register is ignored. A 0-to-1 transition on SRC_EN starts the SYSREF calibration sequence. Program SRC_CFG before setting SRC_EN. Make sur the ADC calibration is not running before setting SRC_EN.

8.1.59 SRC_CFG Register (Address = 0x2B1) [reset = 0x05]

SRC_CFG is shown in Figure 8-59 and described in Table 8-61.

Return to Summary Table.

SYSREF Calibration Configuration register (default: 0x05). This register determines the amount of averaging performed for automatic SYSREF calibration and sets the maximum supported SYSREF cycle. The total duration of SYSREF calibration will be no longer than: TSYSREFCAL (in CLK± cycles) = 256 * 19 * 4 * (SRC_AVG + SRC_HDUR + 2).

Figure 8-59. SRC_CFG Register

7	6	5	4	3	2	1	0
RESERVED				SRC_AVG		SRC_HDUR	
R/W-0x0				R/W-0x1		R-0x1	

Table 8-61. SRC_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0x0	Reserved
3-2	SRC_AVG	R/W	0x1	Specifies the amount of averaging used for SYSREF Calibration. Larger values will increase calibration time and reduce the variance of the calibrated value. 0: 4 high-speed accumulations for each SYSREF measurement 1: 16 high-speed accumulations for each SYSREF measurement 2: 64 high-speed accumulations for each SYSREF measurement 3: 256 high-speed accumulations for each SYSREF measurement
1-0	SRC_HDUR	R/W	0x1	Specifies the duration of each high-speed accumulation for SYSREF Calibration. If the SYSREF period exceeds the supported value, calibration will fail. Larger values will increase calibration time and support longer SYSREF periods. For a given SYSREF period, larger values will also reduce the variance of the calibrated value. 0: 4 cycles per accumulation, supporting SYSREF periods of up to 85 CLK± cycles 1: 16 cycles per accumulation, supporting SYSREF periods of up to 1100 CLK± cycles 2: 64 cycles per accumulation, supporting SYSREF periods of up to 5200 CLK± cycles 3: 256 cycles per accumulation, supporting SYSREF periods of up to 21580 CLK± cycles

8.1.60 SRC_STATUS Register (Address = 0x2B2) [reset = Undefined]

SRC_STATUS is shown in Figure 8-60 and described in Table 8-62.

Return to Summary Table.

SYSREF Calibration Status register (read-only, default: undefined). This register indicates that the SYSREF calibration process has completed and outputs the result of the SYSREF calibration process.

Figure 8-60. SRC_STATUS Register

23	22	21	20	19	18	17	16
RESERVED						SRC_DONE	SRC_TAD[16]
R-Undefined						R-Undefined	R-Undefined
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SRC_TAD[15:8]							
R-Undefined							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SRC_TAD[7:0]							
R-Undefined							

Table 8-62. SRC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
23-18	RESERVED	R/W	0x0	Reserved
17	SRC_DONE	R/W	0x0	This bit returns ‘1’ when SRC_EN=1 and SYSREF Calibration has been completed.
16-0	SRC_TAD	R/W	0x0	This field returns the value for t_{AD} Adjust computed by SYSREF Calibration. It is only valid if SRC_DONE=1. SRC_TAD[16] indicates if CLK± has been inverted. SRC_TAD[15:8] indicates the coarse delay adjustment. SRC_TAD[7:0] indicates the fine delay adjustment. SRC_TAD can be read out and manually written to the TAD register during subsequent boot cycles for repeatability.

8.1.61 TAD Register (Address = 0x2B5-2B7) [reset = 0x000000]

TAD is shown in Figure 8-61 and described in Table 8-63.

Return to Summary Table.

CLK± Timing Adjust register (default: 0x00). This register sets the t_{AD} Adjust delay when automatic SYRSEF calibration is not used.

Figure 8-61. TAD Register

23	22	21	20	19	18	17	16
RESERVED							TAD[16]
R-Undefined							R-0x0
15	14	13	12	11	10	9	8
TAD[15:8]							
R-0x00							
7	6	5	4	3	2	1	0
TAD[7:0]							
R-0x00							

Table 8-63. TAD Register Field Descriptions

Bit	Field	Type	Reset	Description
23-17	RESERVED	R/W	0x0	Reserved
16-0	TAD	R/W	0x0	This register controls t_{AD} Adjust when SRC_EN=0. Use this register to manually control the CLK± inversion and delay when SYSREF Calibration is disabled. TAD[16] inverts CLK± when set. TAD[15:8] controls the coarse delay adjustment. TAD[7:0] controls the fine delay adjustment. If ADC calibration is enabled (CAL_EN=1), or the LVDS interface is enabled (LVDS_EN=1), the following rules must be obeyed to avoid clock glitches and unpredictable behavior: Do not change TAD[16]. CAL_EN and LVDS_EN must be set to 0 before changing TAD[16]. TAD[15:8] must be increased or decreased gradually (no more than 4 codes at a time). This rule can be obeyed manually via SPI writes or by setting TAD_RAMP_EN. TAD[7:0] may be changed to any value at any time since its resolution is too fine to cause clock glitches.

8.1.62 TAD_RAMP Register (Address = 0x2B8) [reset = 0x00]

TAD_RAMP is shown in Figure 8-62 and described in Table 8-64.

Return to Summary Table.

CLK± Timing Adjust Ramp Control register (default: 0x00). This register enables the t_{AD} adjust ramping feature and sets the ramp rate.

Figure 8-62. TAD_RAMP Register

7	6	5	4	3	2	1	0
RESERVED						TAD_RAMP_RATE	TAD_RAMP_EN
R/W-0x0						R/W-0x0	R/W-0x0

Table 8-64. TAD_RAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0x0	Reserved
1	TAD_RAMP_RATE	R/W	0x0	Specify the ramp rate for t_{AD} adjust when the TAD[15:8] register is written while TAD_RAMP_EN is 1. 0 : t_{AD} adjust ramps up or down one code per 256 CLK± cycles. 1 : t_{AD} adjust ramps up or down four codes per 256 CLK± cycles.
0	TAD_RAMP_EN	R/W	0x0	TAD ramp enable. Set this bit if ramping of the coarse t_{AD} adjust is desired. 0 : After writing the TAD[15:8] register, t_{AD} adjust is updated fully within 1024 CLK± cycles (ramp feature disabled). 1 : After writing the TAD[15:8] register, t_{AD} adjust ramps up or down gradually until it matches the TAD[15:8] register. When TAD_RAMP_EN is 1, and the user writes the TAD[15:8] register, a digital counter will automatically ramp t_{AD} adjust up or down until it matches the TAD[15:8] register value. This makes sure the coarse delay changes gradually and does not cause glitches in the delayed CLK± waveform.

8.1.63 ALARM Register (Address = 0x2C0) [reset = Undefined]

ALARM is shown in Figure 8-63 and described in Table 8-65.

Return to Summary Table.

Alarm Interrupt register (read-only). This register indicates if any unmasked alarm in has been triggered in the ALM_STATUS register.

Figure 8-63. ALARM Register

7	6	5	4	3	2	1	0
RESERVED							ALARM
R-Undefined							R-Undefined

Table 8-65. ALARM Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	Undefined	Reserved
0	ALARM	R	Undefined	This bit returns a ‘1’ whenever any unmasked alarm is set in the ALM_STATUS register. Use ALM_MASK to mask (disable) individual alarms. CAL_STATUS_SEL can be used to drive the ALARM bit onto the CAL_STAT pin to provide a hardware alarm interrupt signal.

8.1.64 ALM_STATUS Register (Address = 0x2C1) [reset = 0x05]

ALM_STATUS is shown in Figure 8-64 and described in Table 8-66.

Return to Summary Table.

Alarm Status register (default: 0x05, write to clear). This register indicates if the individual alarms have been triggered.

Figure 8-64. ALM_STATUS Register

7	6	5	4	3	2	1	0
RESERVED					REALIGNED_ALM	RESERVED	CLK_ALM
R/W-0x0					R/W-0x1	R/W-0x0	R/W-0x1

Table 8-66. ALM_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0x0	Reserved
2	REALIGNED_ALM	R/W	0x1	Realigned Alarm: This bit is set whenever SYSREF causes the internal clocks (including the frame counter) to be realigned to a new phase. Write a ‘1’ to clear this bit.
1	RESERVED	R/W	0x0	Reserved
0	CLK_ALM	R/W	0x1	Clock Alarm: This bit can be used to detect an upset to the internal clocks. This bit is set whenever the internal clock dividers for the A and B channels do not match. Write a ‘1’ to clear this bit. Refer to Alarm Monitoring for the proper usage of this register. Note: After power-on reset or soft-reset, all alarm bits are set to ‘1.’

8.1.65 ALM_MASK Register (Address = 0x2C2) [reset = 0x05]

ALM_MASK is shown in Figure 8-65 and described in Table 8-67.

Return to Summary Table.

Alarm Mask register (default: 0x05). This register is used to mask out alarms that should not trigger the ALARM interrupt.

Figure 8-65. ALM_MASK Register

7	6	5	4	3	2	1	0
RESERVED					MASK_REALIGNED_ALM	RESERVED	MASK_CLK_ALM
R/W-0x0					R/W-0x1	R/W-0x0	R/W-0x1

Table 8-67. ALM_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0x0	Reserved
2	MASK_REALIGNED_ALM	R/W	0x1	When set, REALIGNED_ALM is masked and will not impact the ALARM register bit.
1	RESERVED	R/W	0x0	Reserved
0	MASK_CLK_ALM	R/W	0x1	When set, CLK_ALM is masked and will not impact the ALARM register bit.

8.1.66 TADJ_A Register (Address = 0x310) [reset = Undefined]

TADJ_A is shown in Figure 8-66 and described in Table 8-68.

Return to Summary Table.

Timing Adjust for A-ADC, Dual Mode register (default from fuse ROM). This register is used for ADC timing trim. Refer to the Trimming section for more information.

Figure 8-66. TADJ_A Register

7	6	5	4	3	2	1	0
TADJ_A							
R/W-Undefined							

Table 8-68. TADJ_A Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TADJ_A	R/W	Undefined	This register (and other TADJ* registers that follow it) are used to adjust the sampling instant of each ADC core. Different TADJ registers apply to different ADCs under different modes of operation. The default values for all TADJ* registers are loaded from the fuse ROM. The factory trimmed values can be read out and adjusted as required.

8.1.67 TADJ_B Register (Address = 0x313) [reset = Undefined]

TADJ_B is shown in Figure 8-67 and described in Table 8-69.

Return to Summary Table.

Timing Adjust for B-ADC, Dual Mode register (default from fuse ROM). This register is used for ADC timing trim. Refer to the Trimming section for more information.

Figure 8-67. TADJ_B Register

7	6	5	4	3	2	1	0
TADJ_B							
R/W-Undefined							

Table 8-69. TADJ_B Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TADJ_B	R/W	Undefined	See TADJ_A register for description.

8.1.68 TADJ_A_FG90_VINA Register (Address = 0x314) [reset = Undefined]

TADJ_A_FG90_VINA is shown in Figure 8-68 and described in Table 8-70.

Return to Summary Table.

Timing Adjust for A-ADC, DES, Foreground Calibration, INA± register (default from fuse ROM). This register is used for ADC timing trim. Refer to the Trimming section for more information.

Figure 8-68. TADJ_A_FG90_VINA Register

7	6	5	4	3	2	1	0
TADJ_A_FG90_VINA							
R/W-Undefined							

Table 8-70. TADJ_A_FG90_VINA Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TADJ_A_FG90_VINA	R/W	Undefined	See TADJ_A register for description.

8.1.69 TADJ_B_FG0_VINA Register (Address = 0x315) [reset = Undefined]

TADJ_B_FG0_VINA is shown in Figure 8-69 and described in Table 8-71.

Return to Summary Table.

Timing Adjust for B-ADC, DES, Foreground Calibration, INA± regsiter (default from fuse ROM). This register is used for ADC timing trim. Refer to the Trimming section for more information.

Figure 8-69. TADJ_B_FG0_VINA Register

7	6	5	4	3	2	1	0
TADJ_B_FG0_VINA							
R/W-Undefined							

Table 8-71. TADJ_B_FG0_VINA Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TADJ_B_FG0_VINA	R/W	Undefined	See TADJ_A register for description.

8.1.70 TADJ_A_FG90_VINB Register (Address = 0x31A) [reset = Undefined]

TADJ_A_FG90_VINB is shown in Figure 8-70 and described in Table 8-72.

Return to Summary Table.

Timing Adjust for A-ADC, DES, Foreground Calibration, INB± register (default from fuse ROM). This register is used for ADC timing trim. Refer to the Trimming section for more information.

Figure 8-70. TADJ_A_FG90_VINB Register

7	6	5	4	3	2	1	0
TADJ_A_FG90_VINB							
R/W-Undefined							

Table 8-72. TADJ_A_FG90_VINB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TADJ_A_FG90_VINB	R/W	Undefined	See TADJ_A register for description.

8.1.71 TADJ_B_FG0_VINB Register (Address = 0x31B) [reset = 0x0]

TADJ_B_FG0_VINB is shown in Figure 8-71 and described in Table 8-73.

Return to Summary Table.

Timing Adjust for B-ADC, DES, Foreground Calibration, INB± register (default from fuse ROM). This register is used for ADC timing trim. Refer to the Trimming section for more information.

Figure 8-71. TADJ_B_FG0_VINB Register

7	6	5	4	3	2	1	0
TADJ_B_FG0_VINB							
R/W-Undefined							

Table 8-73. TADJ_B_FG0_VINB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TADJ_B_FG0_VINB	R/W	Undefined	See TADJ_A register for description.

8.1.72 OADJ_A_FG0_VINA Register (Address = 0x344) [reset = Undefined]

OADJ_A_FG0_VINA is shown in Figure 8-72 and described in Table 8-74.

Return to Summary Table.

Offset Adjustment for A-ADC / Foreground Calibration / 0° Clock / INA± register (default from fuse ROM). This register is used for ADC core offset trimming. See the Trimming section for more details.

Figure 8-72. OADJ_A_FG0_VINA Register

15	14	13	12	11	10	9	8
RESERVED				OADJ_A_FG0_VINA			
R/W-Undefined				R/W-Undefined			
7	6	5	4	3	2	1	0
OADJ_A_FG0_VINA							
R/W-Undefined							

Table 8-74. OADJ_A_FG0_VINA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	Undefined	Reserved
11-0	OADJ_A_FG0_VINA	R/W	Undefined	Offset adjustment value applied to A-ADC when it samples INA± using 0° clock phase and foreground calibration is enabled.

8.1.73 OADJ_A_FG0_VINB Register (Address = 0x346) [reset = Undefined]

OADJ_A_FG0_VINB is shown in Figure 8-73 and described in Table 8-75.

Return to Summary Table.

Offset Adjustment for A-ADC / Foreground Calibration / 0° Clock / INB± register (default from fuse ROM). This register is used for ADC core offset trimming. See the Trimming section for more details.

Figure 8-73. OADJ_A_FG0_VINB Register

15	14	13	12	11	10	9	8
RESERVED				OADJ_A_FG_VINB			
R/W-Undefined				R/W-Undefined			
7	6	5	4	3	2	1	0
OADJ_A_FG_VINB							
R/W-Undefined							

Table 8-75. OADJ_A_FG0_VINB Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	Undefined	Reserved
11-0	OADJ_A_FG0_VINB	R/W	Undefined	Offset adjustment value applied to A-ADC when it samples INB± using 0° clock phase and foreground calibration is enabled.

8.1.74 OADJ_A_FG90_VINA Register (Address = 0x348) [reset = Undefined]

OADJ_A_FG90_VINA is shown in Figure 8-74 and described in Table 8-76.

Return to Summary Table.

Offset Adjustment for A-ADC / Foreground Calibration / 90° Clock / INA± register (default from fuse ROM). This register is used for ADC core offset trimming. See the Trimming section for more details.

Figure 8-74. OADJ_A_FG90_VINA Register

15	14	13	12	11	10	9	8
RESERVED				OADJ_A_FG90_VINA			
R/W-Undefined				R/W-Undefined			
7	6	5	4	3	2	1	0
OADJ_A_FG90_VINA							
R/W-Undefined							

Table 8-76. OADJ_A_FG90_VINA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	Undefined	Reserved
11-0	OADJ_A_FG90_VINA	R/W	Undefined	Offset adjustment value applied to A-ADC when it samples INA± using 90° clock phase and foreground calibration is enabled.

8.1.75 OADJ_A_FG90_VINB Register (Address = 0x34A) [reset = Undefined]

OADJ_A_FG90_VINB is shown in Figure 8-75 and described in Table 8-77.

Return to Summary Table.

Offset Adjustment for A-ADC / Foreground Calibration / 90° Clock / INB± register (default from fuse ROM). This register is used for ADC core offset trimming. See the Trimming section for more details.

Figure 8-75. OADJ_A_FG90_VINB Register

15	14	13	12	11	10	9	8
RESERVED				OADJ_A_FG90_VINB			
R/W-Undefined				R/W-Undefined			

7	6	5	4	3	2	1	0
OADJ_A_FG90_VINB							
R/W-Undefined							

Table 8-77. OADJ_A_FG90_VINB Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	Undefined	Reserved
11-0	OADJ_A_FG90_VINB	R/W	Undefined	Offset adjustment value applied to A-ADC when it samples INB± using 90° clock phase and foreground calibration is enabled.

8.1.76 OADJ_B_FG0_VINA Register (Address = 0x34C) [reset = Undefined]

OADJ_B_FG0_VINA is shown in Figure 8-76 and described in Table 8-78.

Return to Summary Table.

Offset Adjustment for B-ADC / Foreground Calibration / INA± register (default from fuse ROM). This register is used for ADC core offset trimming. See the Trimming section for more details.

Figure 8-76. OADJ_B_FG0_VINA Register

15	14	13	12	11	10	9	8
RESERVED				OADJ_B_FG0_VINA			
R/W-Undefined				R/W-Undefined			

7	6	5	4	3	2	1	0
OADJ_B_FG0_VINA							
R/W-Undefined							

Table 8-78. OADJ_B_FG0_VINA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	Undefined	Reserved
11-0	OADJ_B_FG0_VINA	R/W	Undefined	Offset adjustment value applied to B-ADC when it samples INA± using 0° clock phase and foreground calibration is enabled.

8.1.77 OADJ_B_FG0_VINB Register (Address = 0x34E) [reset = Undefined]

OADJ_B_FG0_VINB is shown in Figure 8-77 and described in Table 8-79.

Return to Summary Table.

Offset Adjustment for B-ADC / Foreground Calibration / INB± register (default from fuse ROM). This register is used for ADC core offset trimming. See the Trimming section for more details.

Figure 8-77. OADJ_B_FG0_VINB Register

15	14	13	12	11	10	9	8
RESERVED				OADJ_B_FG0_VINB			
R/W-Undefined				R/W-Undefined			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OADJ_B_FG0_VINB							
R/W-Undefined							

Table 8-79. OADJ_B_FG0_VINB Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	Undefined	Reserved
11-0	OADJ_B_FG0_VINB	R/W	Undefined	Offset adjustment value applied to B-ADC when it samples INB± using 0° clock phase and foreground calibration is enabled.

8.1.78 GAIN_B0 Register (Address = 0x360) [reset = Undefined]

GAIN_B0 is shown in Figure 8-78 and described in Table 8-80.

Return to Summary Table.

Fine Gain Adjust for Bank 0 register (default from fuse ROM). This register adjusts the gain of the Bank 0 ADC.

Figure 8-78. GAIN_B0 Register

7	6	5	4	3	2	1	0
RESERVED			GAIN_B0				
R/W-Undefined			R/W-Undefined				

Table 8-80. GAIN_B0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	Undefined	Reserved
4-0	GAIN_B0	R/W	Undefined	Fine gain adjustment for bank 0.

8.1.79 GAIN_B1 Register (Address = 0x361) [reset = Undefined]

GAIN_B1 is shown in Figure 8-79 and described in Table 8-81.

Return to Summary Table.

Fine Gain Adjust for Bank 1 register (default from fuse ROM). This register adjusts the gain of the Bank 1 ADC.

Figure 8-79. GAIN_B1 Register

7	6	5	4	3	2	1	0
RESERVED			GAIN_B1				
R/W-Undefined			R/W-Undefined				

Table 8-81. GAIN_B1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	Undefined	Reserved
4-0	GAIN_B1	R/W	Undefined	Fine gain adjustment for bank 1.

8.1.80 GAIN_B4 Register (Address = 0x364) [reset = Undefined]

GAIN_B4 is shown in Figure 8-80 and described in Table 8-82.

Return to Summary Table.

Fine Gain Adjust for Bank 4 register (default from fuse ROM). This register adjusts the gain of the Bank 4 ADC.

Figure 8-80. GAIN_B4 Register

7	6	5	4	3	2	1	0
RESERVED			GAIN_B4				
R/W-Undefined			R/W-Undefined				

Table 8-82. GAIN_B4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	Undefined	Reserved
4-0	GAIN_B4	R/W	Undefined	Fine gain adjustment for bank 4.

8.1.81 GAIN_B5 Register (Address = 0x365) [reset = Undefined]

GAIN_B5 is shown in Figure 8-81 and described in Table 8-83.

Return to Summary Table.

Fine Gain Adjust for Bank 5 register (default from fuse ROM). This register adjusts the gain of the Bank 5 ADC.

Figure 8-81. GAIN_B5 Register

7	6	5	4	3	2	1	0
RESERVED			GAIN_B5				
R/W-Undefined			R/W-Undefined				

Table 8-83. GAIN_B5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	Undefined	Reserved
4-0	GAIN_B5	R/W	Undefined	Fine gain adjustment for bank 5.

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

WEBENCH® Power Designer

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2024	*	Draft

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC12DL1500ACF	Active	Production	FCBGA (ACF) | 256	90 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	ADC12DL15
ADC12DL1500ACF.A	Active	Production	FCBGA (ACF) | 256	90 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	ADC12DL15
ADC12DL2500ACF	Active	Production	FCBGA (ACF) | 256	90 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	ADC12DL25
ADC12DL2500ACF.A	Active	Production	FCBGA (ACF) | 256	90 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	ADC12DL25
ADC12DL500ACF	Active	Production	FCBGA (ACF) | 256	90 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	ADC12DL05
ADC12DL500ACF.A	Active	Production	FCBGA (ACF) | 256	90 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	0 to 85	ADC12DL05

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

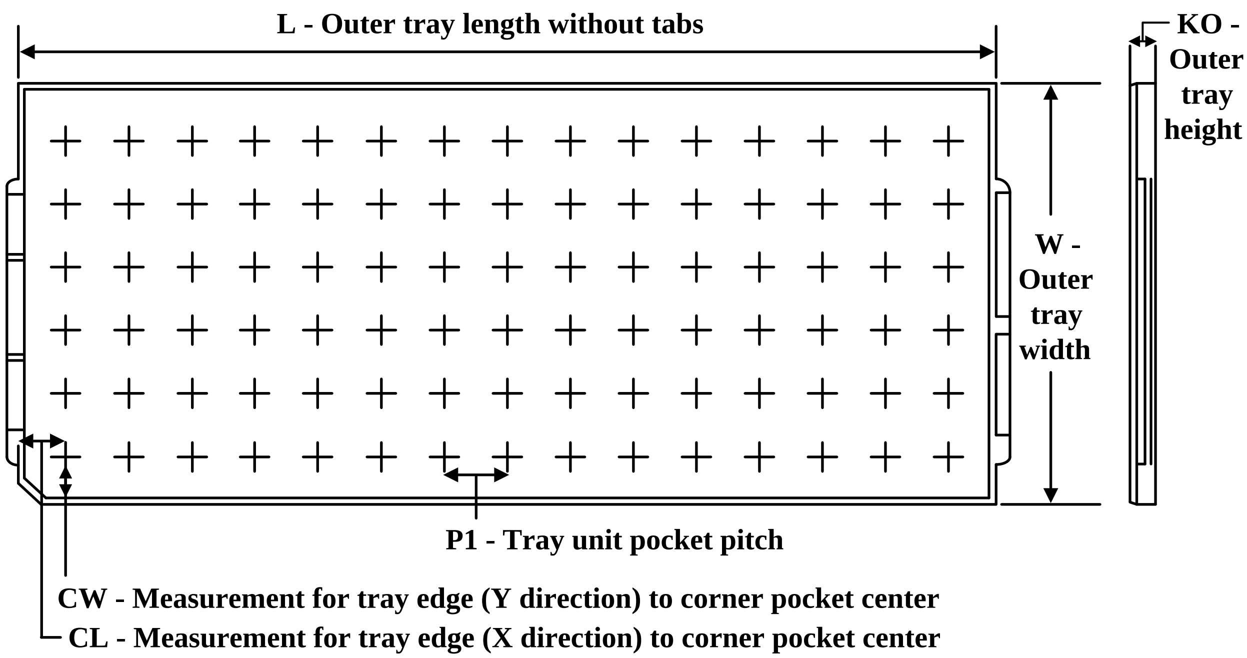
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

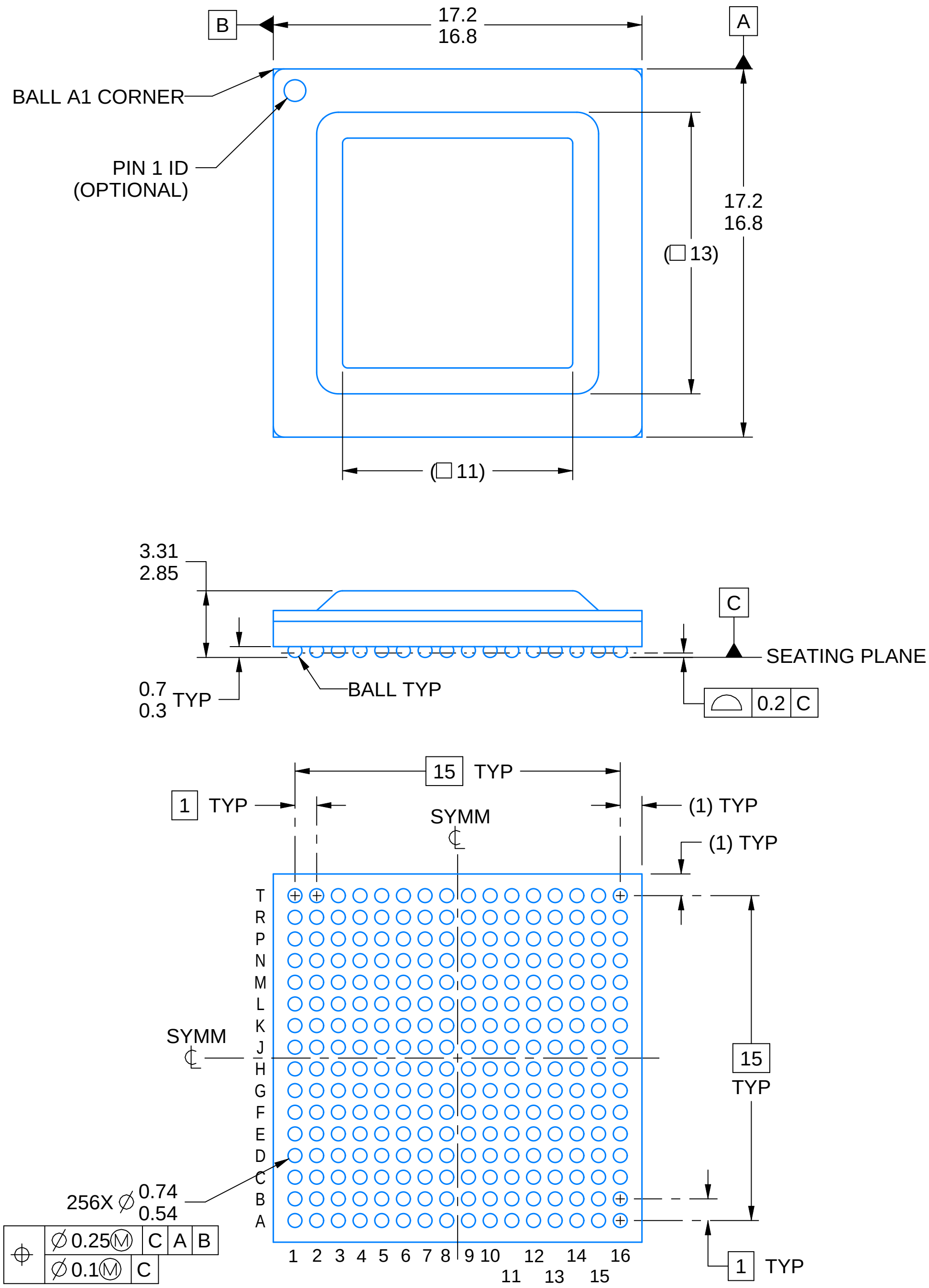
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADC12DL1500ACF	ACF	FCBGA	256	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
ADC12DL1500ACF.A	ACF	FCBGA	256	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
ADC12DL2500ACF	ACF	FCBGA	256	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
ADC12DL2500ACF.A	ACF	FCBGA	256	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
ADC12DL500ACF	ACF	FCBGA	256	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
ADC12DL500ACF.A	ACF	FCBGA	256	90	6 x 15	150	315	135.9	7620	19.5	21	19.2



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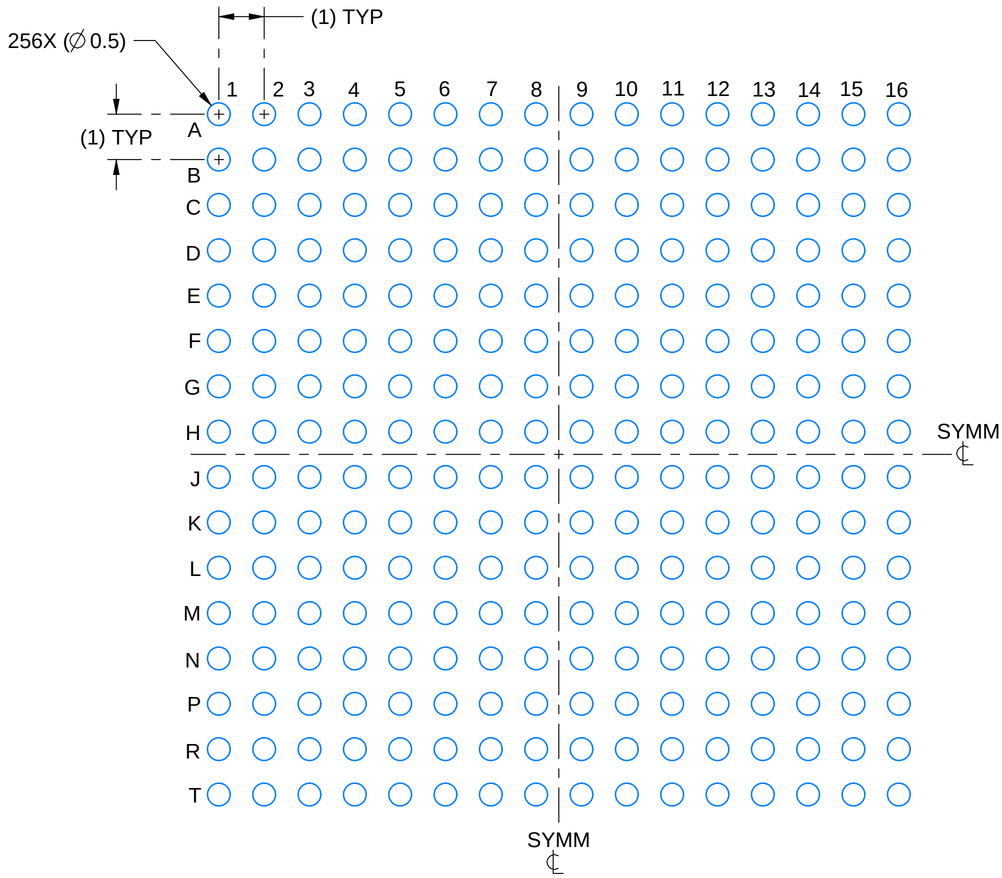
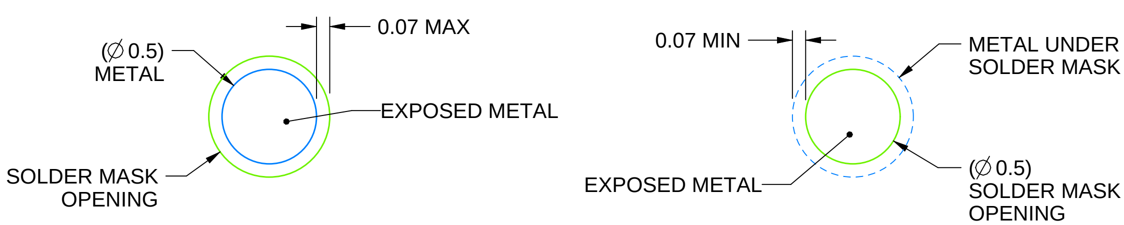
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pb-Free die bump and solder ball.
4. The lids are electrically floating (e.g. not tied to GND).



LAND PATTERN EXAMPLE
EXPOSED METAL SNOWN
SCALE:6X



NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

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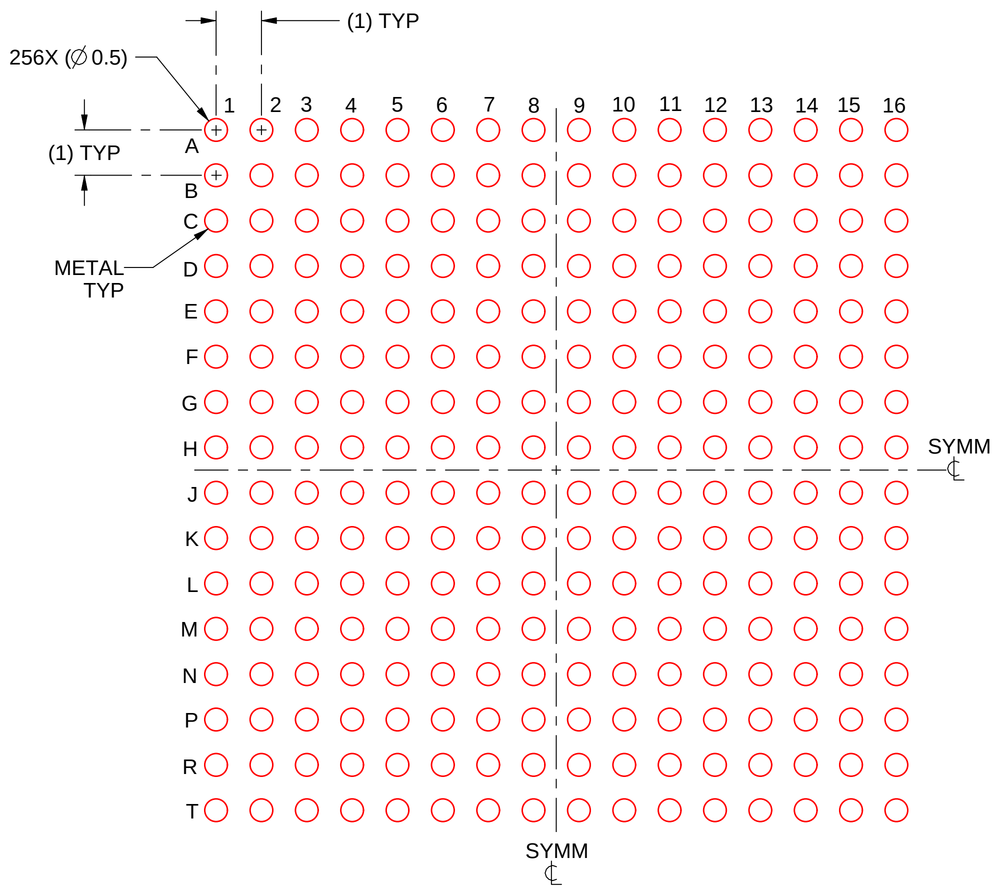
NOTES: (continued)

5. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE: 6X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.