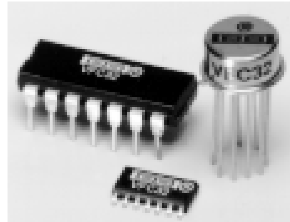
BURR - BROWN®



VFC32

Voltage-to-Frequency and Frequency-to-Voltage CONVERTER

FEATURES

- OPERATION UP TO 500kHz
- EXCELLENT LINEARITY
  ±0.01% max at 10kHz FS
  ±0.05% max at 100kHz FS
- V/F OR F/V CONVERSION
- MONOTONIC
- VOLTAGE OR CURRENT INPUT

APPLICATIONS

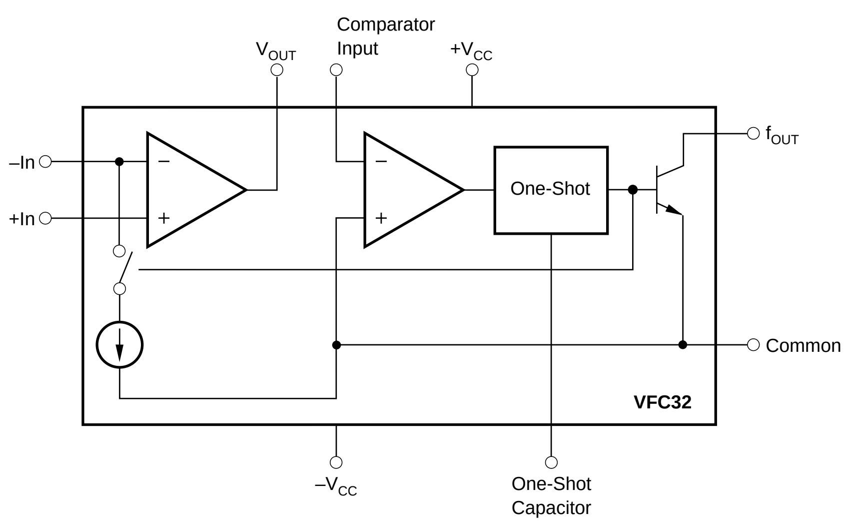
- INTEGRATING A/D CONVERTER
- SERIAL FREQUENCY OUTPUT
- ISOLATED DATA TRANSMISSION
- FM ANALOG SIGNAL MOD/DEMOD
- MOTOR SPEED CONTROL
- TACHOMETER

DESCRIPTION

The VFC32 voltage-to-frequency converter provides an output frequency accurately proportional to its input voltage. The digital open-collector frequency output is compatible with all common logic families. Its integrating input characteristics give the VFC32 excellent noise immunity and low nonlinearity.

Full-scale output frequency is determined by an external capacitor and resistor and can be scaled over a wide range. The VFC32 can also be configured as a frequency-to-voltage converter.

The VFC32 is available in 14-pin plastic DIP, SO-14 surface-mount, and metal TO-100 packages. Commercial, industrial, and military temperature range models are available.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

 PDS-372G Printed in U.S.A. October, 1998

SBVS015

SPECIFICATIONS

At T_A = +25°C and V_{CC} = ±15V, unless otherwise noted.

		VFC32KP, KU			VFC32BM			VFC32SM			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT (V/F CONVERTER) $F_{OUT} = V_{IN}/7.5\ R_1\ C_1$											
Voltage Range(1)											
Positive Input		>0		+0.25mA x R_1	✻		✻	✻		✻	V
Negative Input		>0		–10	✻		✻	✻		✻	V
Current Range(1)		>0		+0.25	✻		✻	✻		✻	mA
Bias Current											
Inverting Input			20	100		✻	✻		✻	✻	nA
Noninverting Input			100	250		✻	✻		✻	✻	nA
Offset Voltage(2)			1	4		✻	✻		✻	✻	mV
Differential Impedance		300 || 10	650 || 10		✻	✻		✻	✻		kΩ || pF
Common-mode Impedance		300 || 3	500 || 3		✻	✻		✻	✻		MΩ || pF
INPUT (F/V CONVERTER) $V_{OUT} = 7.5\ R_1\ C_1\ F_{IN}$											
Impedance		50 || 10	150 || 10		✻	✻		✻	✻		kΩ || pF
Logic "1"			+1.0		✻		✻	✻		✻	V
Logic "0"			–0.05		✻		✻	✻		✻	V
Pulse-width Range		0.1		$150k/F_{MAX}$	✻		✻	✻		✻	µs
ACCURACY											
Linearity Error(3)	0.01Hz ≤ Oper Freq ≤ 10kHz		±0.005	±0.010(4)		✻	✻		✻	✻	% of FSR(5)
	0.1Hz ≤ Oper Freq ≤ 100kHz		±0.025	±0.05		✻	✻		✻	✻	% of FSR
	0.5Hz ≤ Oper Freq ≤ 500kHz		±0.05			✻			✻		% of FSR
Offset Error Input Offset Votlage(2)			1	4		✻	✻		✻	✻	mV
Offset Drift(6)			±3			✻			✻		ppm of FSR/°C
Gain Error(2)			5			✻			✻		% of FSR
Gain Drift(6)	f = 10kHz		±75			±50	±100		±70	±150	ppm/°C
Full Scale Drift (offset drift and gain drift)(6, 7)	f = 10kHz		±75			±50	±100		±70	±150	ppm of FSR/°C
Power Supply Sensitivity	f = DC, ±V_{CC} = 12VDC to 18VDC			±0.015			✻			✻	% of FSR/%
OUTPUT (V/F CONVERTER) (open collector output)											
Voltage, Logic "0"	I_{SINK} = 8mA	0	0.2	0.4	✻	✻	✻	✻	✻	✻	V
Leakage Current, Logic "1"	V_O = 15V		0.01	1.0		✻	✻		✻	✻	µA
Voltage, Logic "1"	External Pull-up Resistor Required (see Figure 4)			V_{PU}			✻			✻	V
Pulse Width	For Best Linearity		$0.25/F_{MAX}$			✻			✻		s
Fall Time	I_{OUT} = 5mA, C_{LOAD} = 500pF			400			✻			✻	ns
OUTPUT (F/V CONVERTER) V_{OUT}											
Voltage	I_O ≤ 7mA	0 to +10			✻			✻			V
Current	V_O ≤ 7VDC	+10			✻			✻			mA
Impedance	Closed Loop			1			✻			✻	Ω
Capacitive Load	Without Oscillation			100			✻			✻	pF
DYNAMIC RESPONSE											
Full Scale Frequency				500(8)	✻			✻			kHz
Dynamic Range		6			✻			✻			decades
Settling Time	(V/F) to Specified Linearity for a Full Scale Input Step		(9)			✻			✻		
Overload Recovery	< 50% Overload		(9)			✻			✻		
POWER SUPPLY											
Rated Voltage			±15								V
Voltage Range		±11		±20					✻		V
Quiescent Current			±5.5	±6.0		✻	✻		✻		mA
TEMPERATURE RANGE											
Specification		0		+70	–25		+85	–55		+125	°C
Operating		–25		+85	–55		+125	–55		+125	°C
Storage		–25		+85	–65		+150	–65		+150	°C

✻ Specification the same as VFC32KP.

NOTES: (1) A 25% duty cycle (0.25mA input current) is recommended for best linearity. (2) Adjustable to zero. See Offset and Gain Adjustment section. (3) Linearity error is specified at any operating frequency from the straight line intersecting 90% of full scale frequency and 0.1% of full scale frequency. See Discussion of Specifications section. Above 200kHz, it is recommended all grades be operated below +85°C. (4) ±0.015% of FSR for negative inputs shown in Figure 5. Positive inputs are shown in Figure 1. (5) FSR = Full Scale Range (corresponds to full scale frequency and full scale input voltage). (6) Exclusive of external components' drift. (7) Positive drift is defined to be increasing frequency with increasing temperature. (8) For operations above 200kHz up to 500kHz, see Discussion of Specifications and Installation and Operation sections. (9) One pulse of new frequency plus 1µs.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Output Sink Current (F_{OUT})	50mA
Output Current (V_{OUT})	+20mA
Input Voltage, –Input	±Supply
Input Voltage, +Input	±Supply
Comparator Input	±Supply
Storage Temperature Range:	
VFC32BM, SM	–65°C to +150°C
VFC32KP, KU	–25°C to +85°C

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
VFC32KP	14-Pin Plastic DIP	010	0°C to 70°C
VFC32BM	TO-100 Metal	007	–25°C to +85°C
VFC32SM	TO-100 Metal	007	–55°C to +125°C
VFC32KU	SO-14 SOIC	235	0°C to +70°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

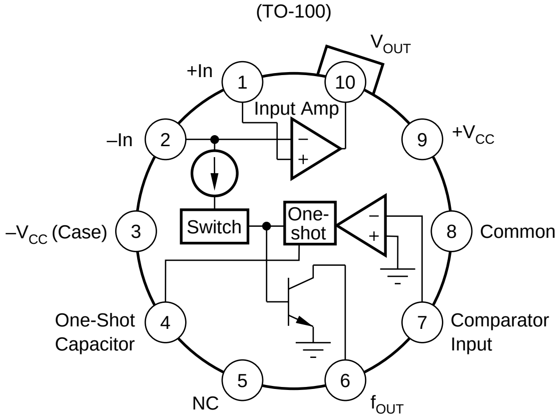
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATIONS

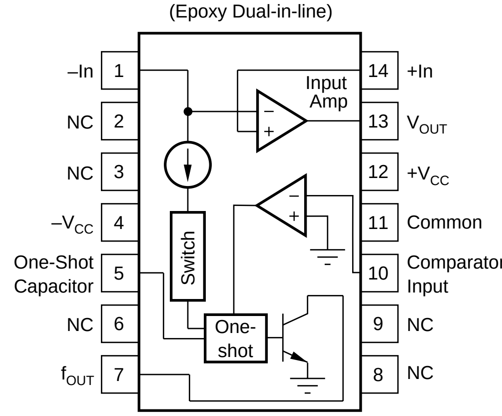
Top View

M Package
(TO-100)



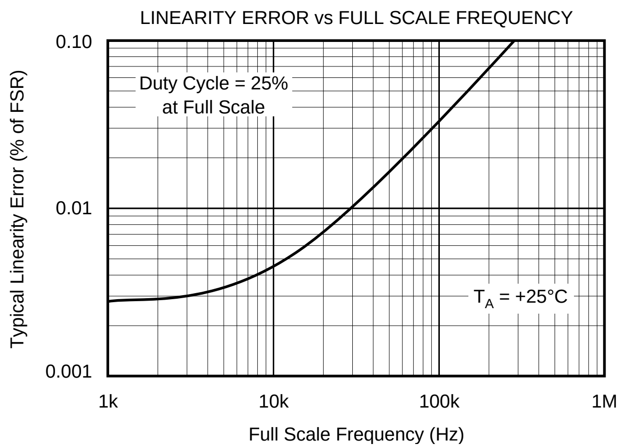
NC = no internal connection
External connection permitted.

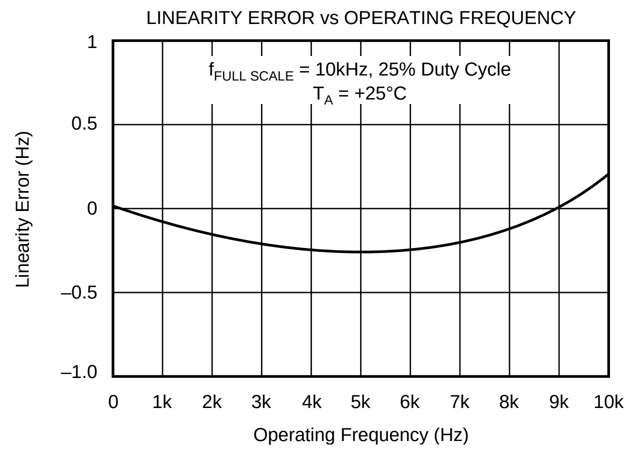
P Package
U Package
(Epoxy Dual-in-line)

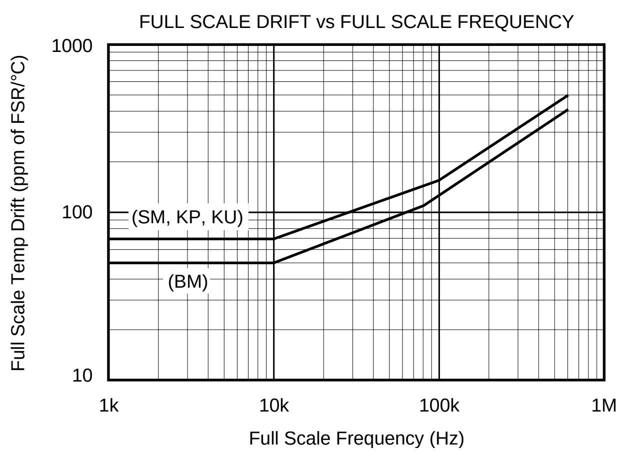


TYPICAL PERFORMANCE CURVES

At T_A = +25°C and V_{CC} = ±15V, unless otherwise noted.







APPLICATION INFORMATION

Figure 1 shows the basic connection diagram for frequency-to-voltage conversion. R_1 sets the input voltage range. For a 10V full-scale input, a 40kΩ input resistor is recommended. Other input voltage ranges can be achieved by changing the value of R_1.

$$R_1 = \frac{V_{FS}}{0.25mA} \tag{1}$$

R_1 should be a metal film type for good stability. Manufacturing tolerances can produce approximately ±10% variation in output frequency. Full-scale output frequency can be trimmed by adjusting the value of R_1—see Figure 3.

The full-scale output frequency is determined by C_1. Values shown in Figure 1 are for a full-scale output frequency of 10kHz. Values for other full-scale frequencies can be read from Figure 2. Any variation in C_1—tolerance, temperature drift, aging—directly affect the output frequency. Ceramic NPO or silver-mica types are a good choice.

For full-scale frequencies above 200kHz, use larger capacitor values as indicated in Figure 2, with R_1 = 20kΩ.

The value of the integrating capacitor, C_2, does not directly influence the output frequency, but its value must be chosen within certain bounds. Values chosen from Figure 2 produce approximately 2.5Vp-p integrator voltage waveform. If C_2's value is made too low, the integrator output voltage can exceed its linear output swing, resulting in a nonlinear response. Using C_2 values larger than shown in Figure 2 is acceptable.

Accuracy or temperature stability of C_2 is not critical because its value does not directly affect the output frequency. For best linearity, however, C_2 should have low leakage and low dielectric absorption. Polycarbonate and other film capacitors are generally excellent. Many ceramic types are adequate, but some low-voltage ceramic capacitor types may degrade nonlinearity. Electrolytic types are not recommended.

FREQUENCY OUTPUT PIN

The frequency output terminal is an open-collector logic output. A pull-up resistor is usually connected to a 5V logic supply to create standard logic-level pulses. It can, however, be connected to any power supply up to $+V_{CC}$. Output pulses have a constant duration and positive-going during the one-shot period. Current flowing in the open-collector output transistor returns through the Common terminal. This terminal should be connected to logic ground.

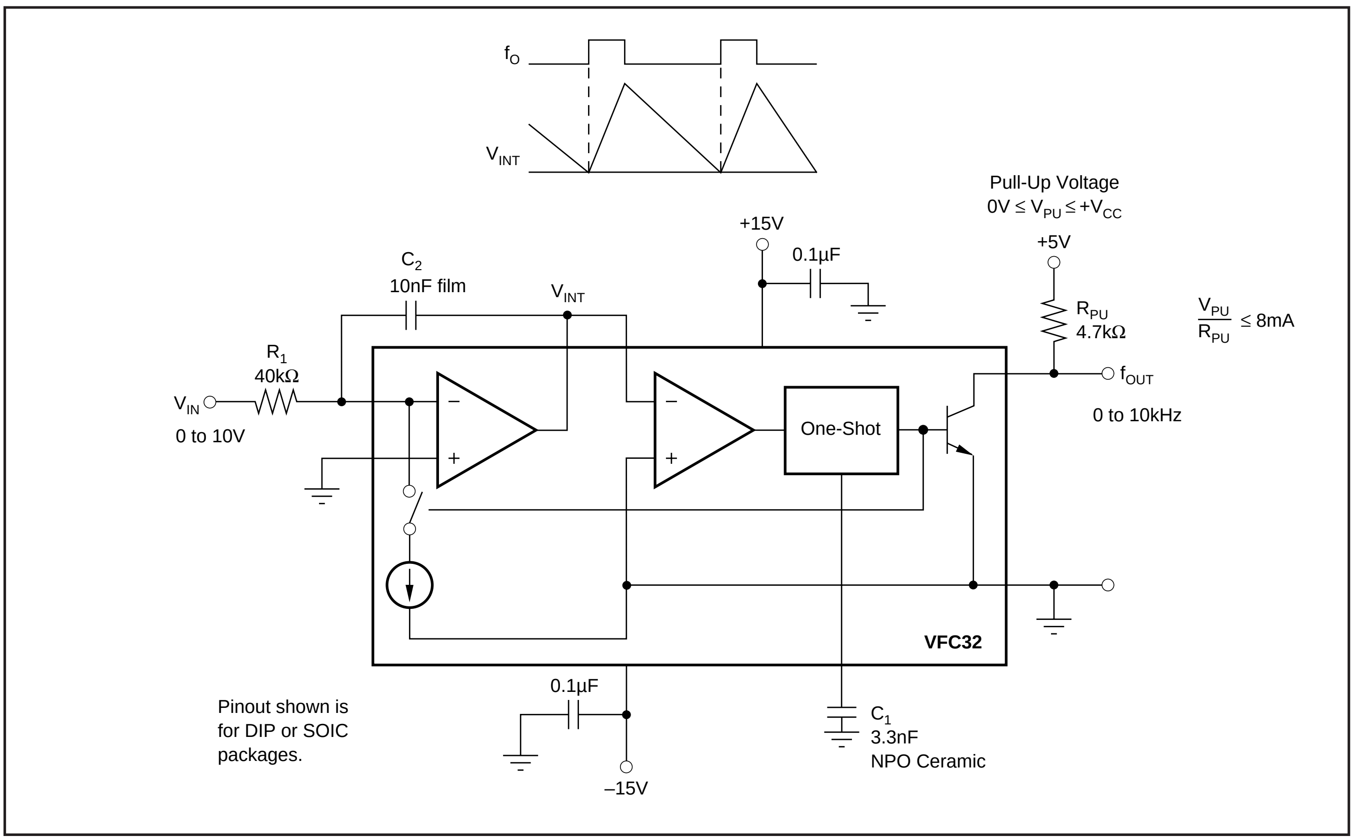


FIGURE 1. Voltage-to-Frequency Converter Circuit.

FREQUENCY-TO-VOLTAGE CONVERSION

Figure 4 shows the VFC32 connected as a frequency-to-voltage converter. The capacitive-coupled input network C_3, R_6 and R_7 allow standard 5V logic levels to trigger the comparator input. The comparator triggers the one-shot on the falling edge of the frequency input pulses. Threshold voltage of the comparator is approximately –0.7V. For frequency input waveforms less than 5V logic levels, the R_6/R_7 voltage divider can be adjusted to a lower voltage to assure that the comparator is triggered.

The value of C_1 is chosen from Figure 2 according to the full-scale input frequency. C_2 smooths the output voltage waveform. Larger values of C_2 reduce the ripple in the output voltage. Smaller values of C_2 allow the output voltage to settle faster in response to a change in input frequency. Resistor R_1 can be trimmed to achieve the desired output voltage at the full-scale input frequency.

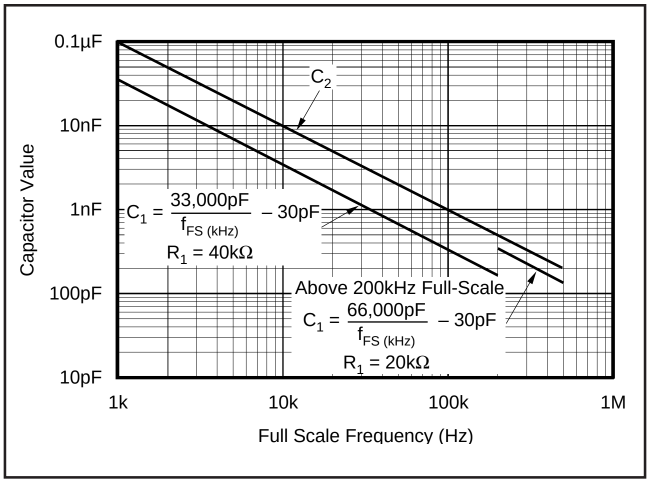


FIGURE 2. Capacitor Value Selection.

PRINCIPLES OF OPERATION

The VFC32 operates on a principle of charge balance. The signal input current is equal to V_{IN}/R_1. This current is integrated by input op amp and C_2, producing a downward ramping integrator output voltage. When the integrator output ramps to the threshold of the comparator, the one-shot is triggered. The 1mA reference current is switched to the integrator input during the one-shot period, causing the integrator output ramp upward. After the one-shot period, the integrator again ramps downward.

The oscillation process forces a long-term balance of charge (or average current) between the input signal current and the reference current. The equation for charge balance is:

$$I_{IN} = I_{R(AVERAGE)} \tag{2}$$

$$\frac{V_{IN}}{R_1} = f_O t_{OS}(1mA) \tag{3}$$

Where:

f_O is the output frequency

t_{OS} is the one-shot period, equal to

t_{OS} = 7500 C_1 (Farads) (4)

The values suggested for R_1 and C_1 are chosen to produce a 25% duty cycle at full-scale frequency output. For full-scale frequencies above 200kHz, the recommended values produce a 50% duty cycle.

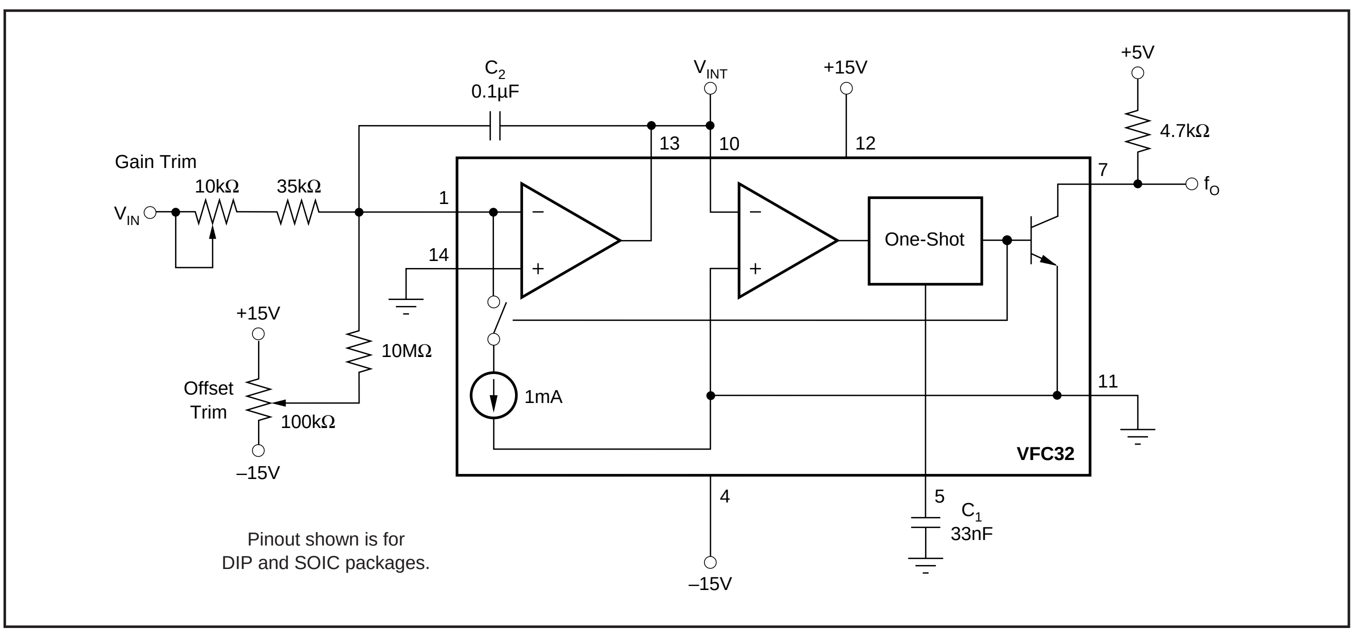


FIGURE 3. Gain and Offset Voltage Trim Circuit.

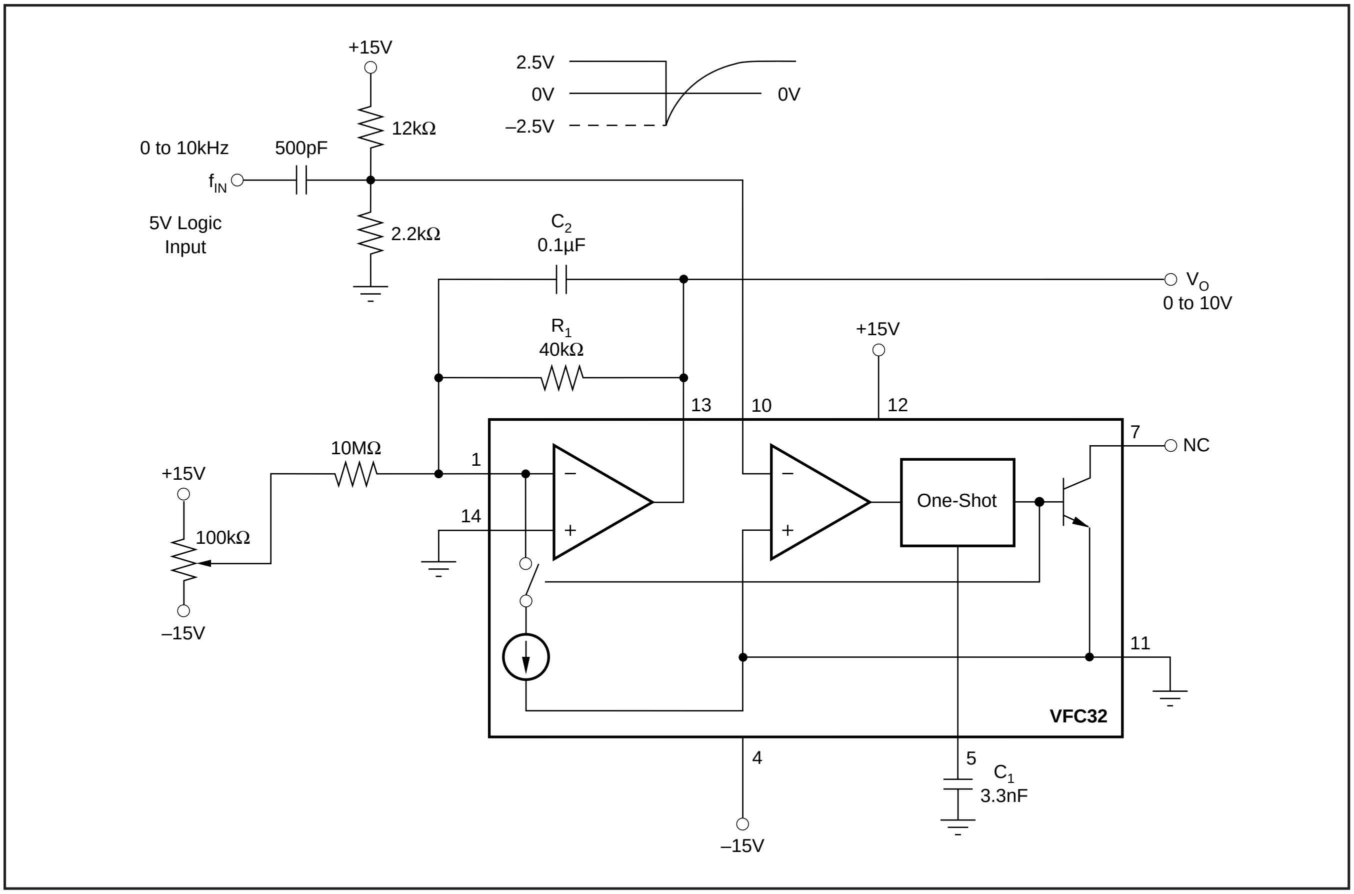


FIGURE 4. Frequency-to-Voltage Converter Circuit.

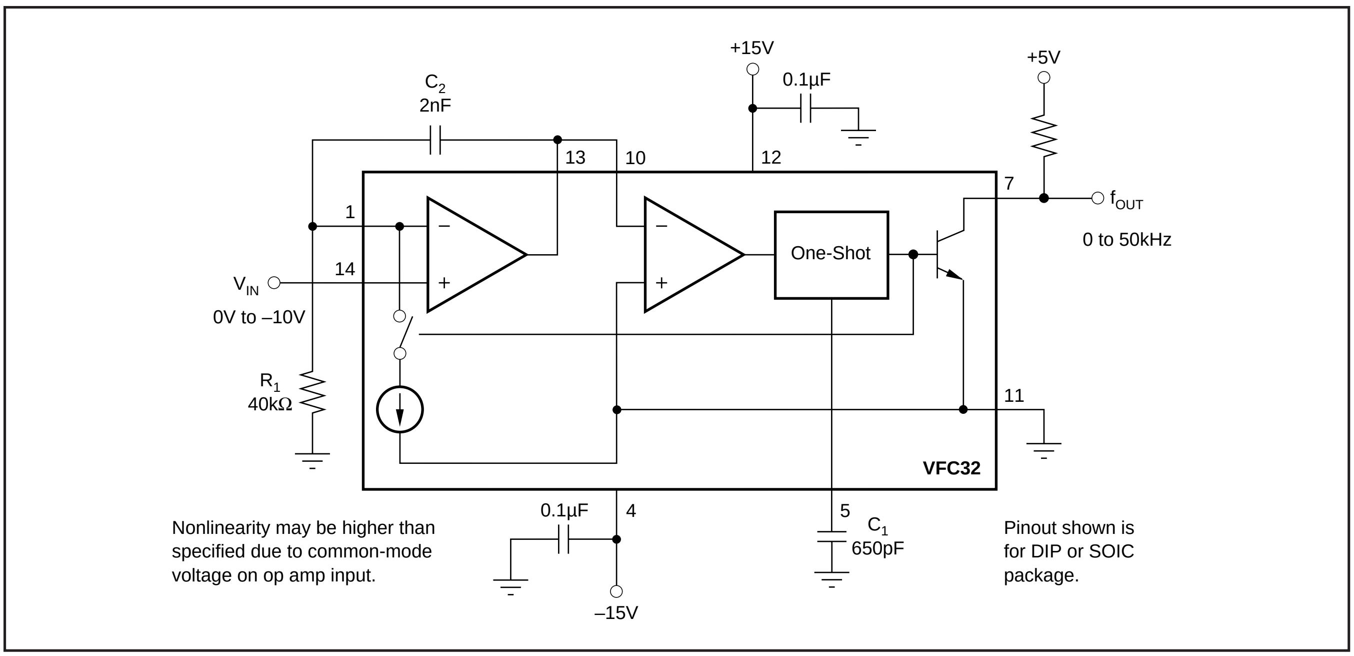


FIGURE 5. V/F Converter—Negative Input Voltage.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
VFC32KP	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	VFC32KP
VFC32KP.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	VFC32KP
VFC32KU	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	VFC32KU
VFC32KU.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	VFC32KU
VFC32KU/2K5	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	VFC32KU
VFC32KU/2K5.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	VFC32KU

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

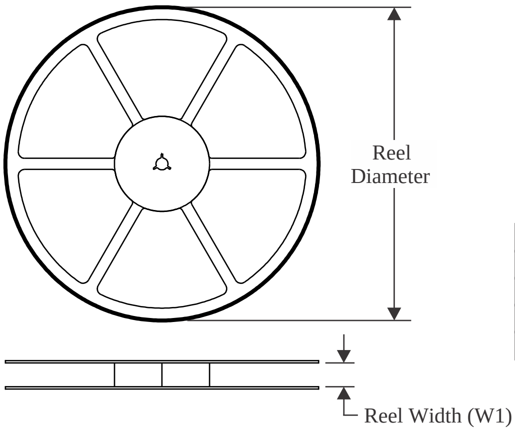
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

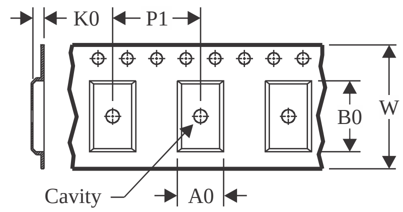
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

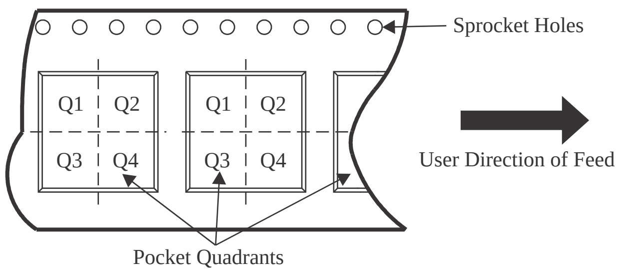


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

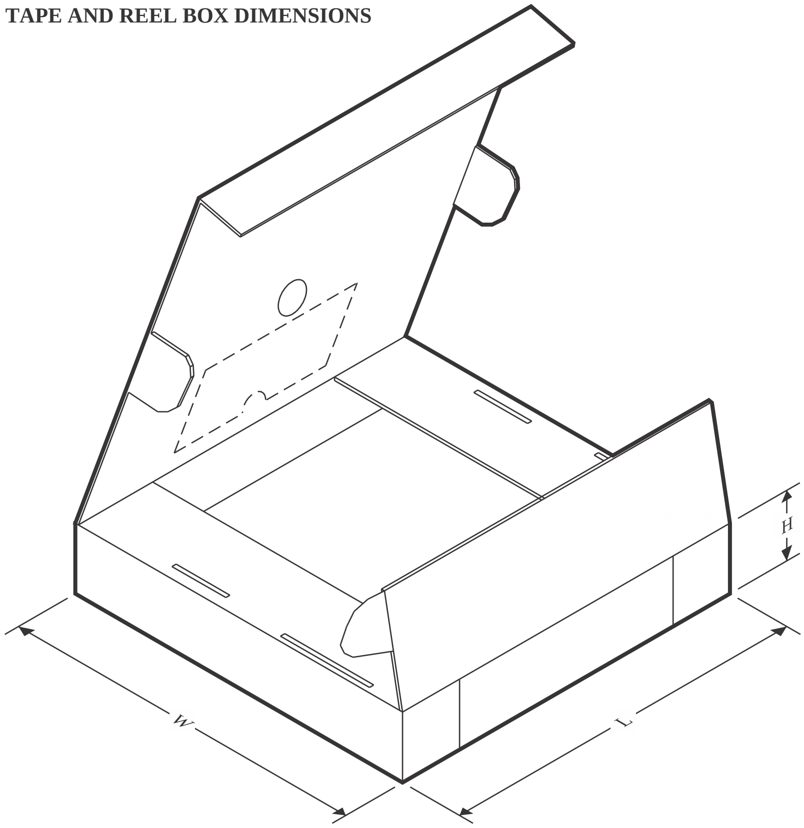
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VFC32KU/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

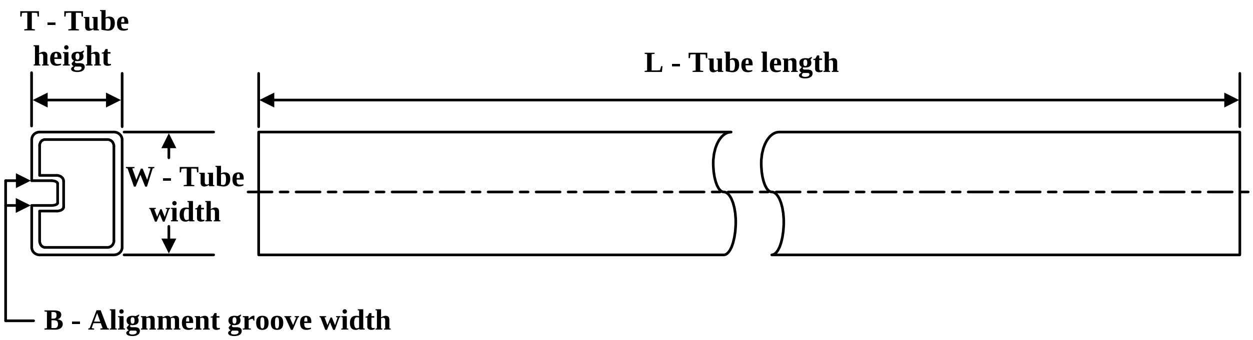
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VFC32KU/2K5	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
VFC32KP	N	PDIP	14	25	506	13.97	11230	4.32
VFC32KP.A	N	PDIP	14	25	506	13.97	11230	4.32
VFC32KU	D	SOIC	14	50	506.6	8	3940	4.32
VFC32KU.A	D	SOIC	14	50	506.6	8	3940	4.32