

具有光耦合器反馈功能的 UCC28742 高效反激式控制器

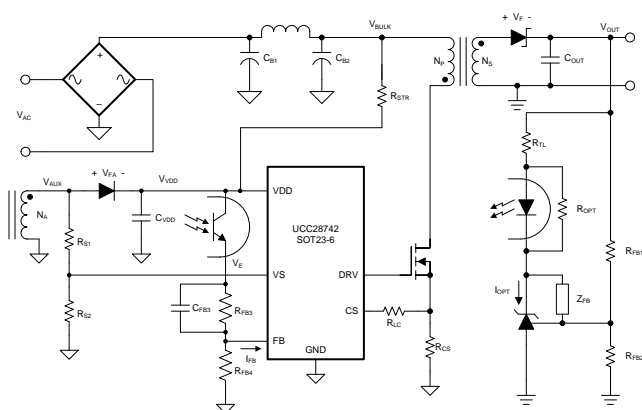
1 特性

- 光耦合反馈可实现精度高达 1% 的调节
- 精确电流限制以及过载超时保护和延迟断续响应
- 谐振谷底开关运行模式可实现最高总体效率
- 最大开关频率为 80kHz
- 简化电磁干扰 (EMI) 兼容性的频率抖动
- 针对金属氧化物半导体场效应晶体管 (MOSFET) 的已钳制栅极驱动输出
- 超低启动电流和大型 VDD 迟滞
 - 高值启动电阻器
 - 低偏置电容
- 故障保护
 - 输入低线路
 - 输出过压
 - 过流
 - 短路
- SOT23-6 封装
- 使用 UCC28742 并借助 WEBENCH® 电源设计器创建定制设计方案

2 应用

- 工业和医疗交流/直流电源
- 智能电表
- UPS、服务器 PSU 等的偏置电源
- 电缆调制解调器、电视、机顶盒和无线路由器的电源
- 电器的交流/直流电源

简化原理图



3 说明

UCC28742 离线反激式控制器是一款高度集成的 6 引脚次级侧稳压 PWM 控制器，适用于高效交流/直流电源。这是一种隔离式反激电源控制器，使用一个光耦合器来提供恒定电压 (CV)，从而改善对大型负载阶跃的瞬态响应。此器件处理来自光耦合反馈和辅助反激式绕组的信息，以此实现对输出电压和电流的高性能控制。

UCC28742 采用先进的控制算法来实现高运行效率和性能。驱动输出接至一个 MOSFET 电源开关。带有谷值开关的断续传导模式 (DCM) 减少了开关损耗。开关频率的调制和初级电流峰值振幅 (FM 和 AM) 在整个负载和线路范围内保持较高的转换效率。

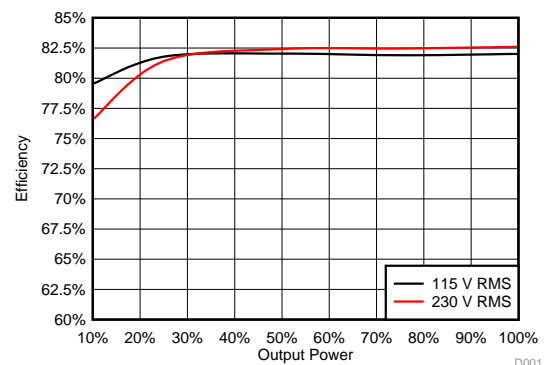
此控制器的最大开关频率为 80kHz，并且一直保持对变压器内峰值一次侧电流的控制。200Hz 的最小开关频率有助于实现较低的空载输入功率。

器件信息 (1)

器件型号	封装	封装尺寸 (标称值)
UCC28742	SOT23-6	2.90mm × 1.60mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

10W、5V 交流/直流转换器的典型效率



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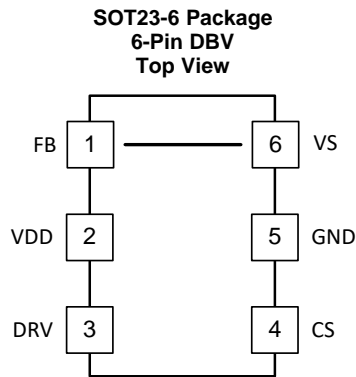
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4 修订历史记录

日期	修订版本	说明
2018 年 5 月	A	最初发布版本。

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CS	4	I	The current-sense (CS) input connects to a ground-referenced current-sense resistor in series with the power switch. The resulting voltage monitors and controls the peak primary current. A series resistor is added to this pin to compensate for peak switch current levels as the AC-mains input varies.
DRV	3	O	DRV is an output pin used to drive the gate of an external high voltage MOSFET switching transistor.
FB	1	I	The feedback (FB) input receives a current signal from the optocoupler output transistor. An internal current mirror divides the feedback current applies it to an internal pullup resistor to generate a control voltage, VCL. The voltage at this resistor directly drives the control law function, which determines the switching frequency and the peak amplitude of the switching current.
GND	5	G	The ground (GND) pin is both the reference pin for the controller, and the low-side return for the drive output. Special care must be taken to return all AC-decoupling capacitors as close as possible to this pin and avoid any common trace length with analog signal-return paths.
VDD	2	P	VDD is the bias supply input pin to the device. A carefully placed bypass capacitor to GND is required on this pin. Typical bypass capacitor values are from 0.047 μ F to 10 μ F depending on a design.
VS	6	I	Voltage sense (VS) is an input used to provide demagnetization timing feedback to the controller to limit frequency, to control constant-current operation, and to provide output-overvoltage detection. VS is also used for AC-mains input-voltage detection for peak primary-current compensation. This pin connects to a voltage divider between an auxiliary winding and GND. The value of the upper resistor of this divider programs the AC-mains run and stop thresholds, and factors into line compensation at the CS pin.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{VDD}	Bias supply voltage		38	V
V _S	Voltage range	−0.75	7	V
FB	Voltage range	−0.5	7	V
CS	Voltage range	−0.5	5	V
V _{DRV}	Gate-drive voltage at DRV	−0.5	Self-limiting	V
I _{DRV}	DRV continuous sink current		50	mA
I _{DRV}	DRV continuous source current		15	mA
I _{DRV}	DRV peak sourcing current, V _{DRV} = 10 V to 0 V		Self-limiting	mA
I _{DRV}	DRV peak sink current, V _{DRV} = 0 V to 10 V		Self-limiting	mA
I _{FB}	FB, peak current		1.0	mA
I _{VS}	VS, peak, 1% duty-cycle, when detecting line voltage		1.2	mA
T _J	Operating junction temperature range	−55	150	°C
T _{STG}	Storage temperature	−65	150	°C
T _{LEAD}	Lead temperature 0.6 mm from case for 10 seconds		260	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
V _(ESD)	Electrostatic discharge	Charged-device model (CDM) ESD stress voltage ⁽²⁾	±500	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{DD}	Bias supply operating voltage	9	35	V
C _{DD}	VDD bypass capacitor	0.047	no limit	μF
I _{FB}	Feedback current, continuous		50	μA
I _{VS}	VS pin sourcing current when detecting line voltage		1.0	mA
T _J	Operating junction temperature	−40	125	°C

6.4 Thermal Information

THERMAL METRIC		UCC28742	UNIT
		DBV	
		6 PINS	
θ_{JA}	Junction-to-ambient thermal resistance ⁽¹⁾	150	°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance ⁽²⁾	55	°C/W
θ_{JB}	Junction-to-board thermal resistance ⁽³⁾	60	°C/W
ψ_{JT}	Junction-to-top characterization parameter ⁽⁴⁾	3	°C/W
ψ_{JB}	Junction-to-board characterization parameter ⁽⁵⁾	55	°C/W

- (1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (4) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (5) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

6.5 Electrical Characteristics

Over operating free-air temperature range, $V_{DD} = 25\text{ V}$, $V_{FB} = 0\text{ V}$, $V_{VS} = 4\text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$, $T_J = T_A$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS SUPPLY INPUT						
I _{RUN}	Supply current, run	I _{DRV} = 0, run state	1.30	1.80	2.40	mA
I _{WAIT}	Supply current, wait	I _{DRV} = 0, V _{VDD} = 20 V, wait state	50	80	115	μA
I _{START}	Supply current, start	I _{DRV} = 0, V _{VDD} = 17 V, start state		1.50	2.75	μA
I _{FAULT}	Supply current, fault	I _{DRV} = 0, fault state	1.30	1.80	2.40	mA
UNDER-VOLTAGE LOCKOUT						
V _{VDD(on)}	VDD turn-on threshold	V _{VDD} low to high	17.5	21.6	24.5	V
V _{VDD(off)}	VDD turn-off threshold	V _{VDD} high to low	7.25	7.80	8.30	V
VS INPUT						
V _{VSNC}	Negative clamp level	I _{VS} = −300 μA	−304	−225	−164	mV
I _{VSB}	Input bias current	V _{VS} = 4 V	−0.25	0	0.25	μA
FB INPUT						
I _{FBMAX}	Full-range input current	f _{SW} = f _{SW(min)}	16	23	30	μA
V _{FBMAX}	Input voltage at full-range	I _{FB} = 26 μA	0.70	0.90	1.10	V
R _{FB}	FB-input resistance	ΔI _{FB} = 6 to 26 μA	10	14	18	kΩ
CS INPUT						
V _{CST(max)}	Max CS threshold voltage ⁽¹⁾	I _{FB} = 0 μA	710	770	830	mV
V _{CST(min)}	Min CS threshold voltage ⁽¹⁾	I _{FB} = 35 μA	164	190	216	mV
K _{AM}	AM control ratio	V _{CST(max)} / V _{CST(min)}	3.55	4.00	4.50	V/V
V _{CCR}	Constant-current regulating level		338	363	390	mV
K _{LC}	Line compensating current ratio, I _{VSLs} / (current out of CS pin)	I _{VSLs} = −300 μA	23	25	29	A/A
T _{CSLEB}	Leading-edge blanking time	DRV output duration, V _{CS} = 1 V	195	270	350	ns

- (1) These threshold voltages represent average levels. This device automatically varies the current sense threshold to improve EMI performance.

Electrical Characteristics (continued)

Over operating free-air temperature range, $V_{DD} = 25\text{ V}$, $V_{FB} = 0\text{ V}$, $V_{VS} = 4\text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$, $T_J = T_A$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRV						
I_{DRS}	DRV source current	$V_{DRV} = 5\text{ V}$, $V_{DD} = 9\text{ V}$	24	30	36	mA
R_{DRVLS}	DRV low-side drive resistance	$I_{DRV} = 10\text{ mA}$		6.5	12	Ω
V_{DRCL}	DRV clamp voltage	$V_{DD} = 35\text{ V}$	8.8	10.6	13	V
R_{DRVSS}	DRV pull-down in start state		135	175	250	k Ω
TIMING						
$f_{SW(max)}$	Maximum switching frequency ⁽²⁾	$I_{FB} = 0\text{ }\mu\text{A}$	80	105	130	kHz
$f_{SW(min)}$	Minimum switching frequency	$I_{FB} = 35\text{ }\mu\text{A}$	140	200	255	Hz
t_{ZTO}	Zero-crossing timeout delay		1.45	2.45	3.30	μs
t_{OVL_TIME}	Delay time before shutdown	$\text{Demag_Duty} = V_{CCR} / V_{CST(max)}$	85	120	160	ms
PROTECTION						
V_{OVP}	Over-voltage threshold ⁽³⁾	At VS input, $T_J = 25^{\circ}\text{C}$	4.45	4.65	4.85	V
V_{OCP}	Over-current threshold ⁽³⁾	At CS input	1.41	1.50	1.59	V
$I_{VSL(run)}$	VS line-sense run current	Current out of VS pin – increasing	170	210	250	μA
$I_{VSL(stop)}$	VS line-sense stop current	Current out of VS pin – decreasing	60	75	90	μA
K_{VSL}	VS pin, line-sense current ratio, $I_{VSL(run)} / I_{VSL(stop)}$		2.50	2.80	3.05	A/A
$T_{J(stop)}$	Thermal shut-down temperature ⁽⁴⁾	Internal junction temperature		165		$^{\circ}\text{C}$

(2) These frequency limits represent average levels. This device automatically varies the switching frequency to improve EMI performance.

(3) The OVP threshold at VS decrease with increasing temperature by 1 mV/ $^{\circ}\text{C}$. This compensation over temperature is included to reduce the variances in power supply over-voltage detection with respect to the external output rectifier.

(4) Ensured by design. Not tested in production.

6.6 Typical Characteristics

V_{DD} = 25 V, unless otherwise noted.

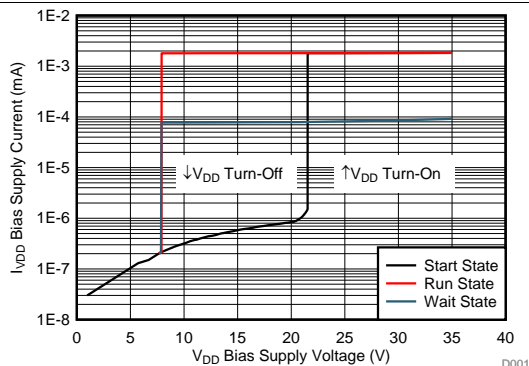


图 1. Bias Supply Current vs. Bias Supply Voltage

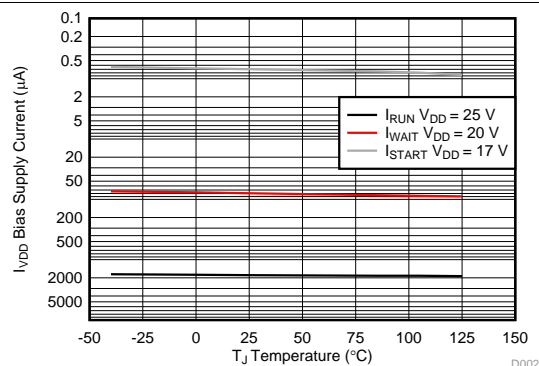


图 2. Bias Supply Current vs. Temperature

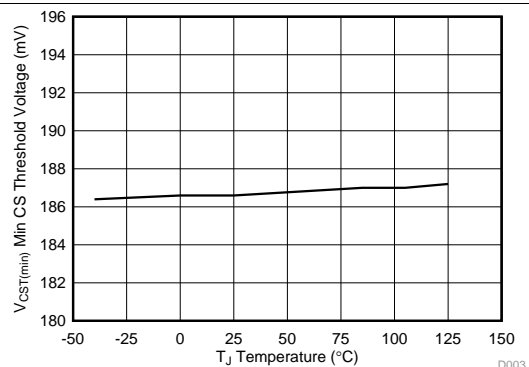


图 3. Minimum CS Threshold vs. Temperature

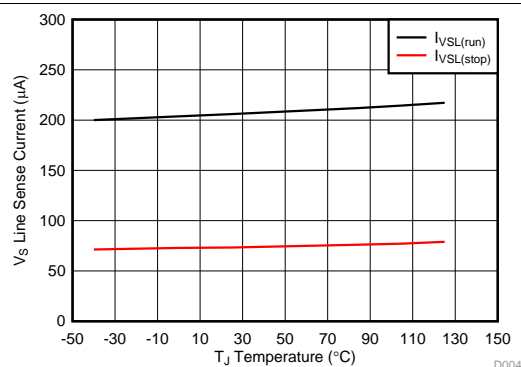


图 4. VS Line-Sense Current vs. Temperature

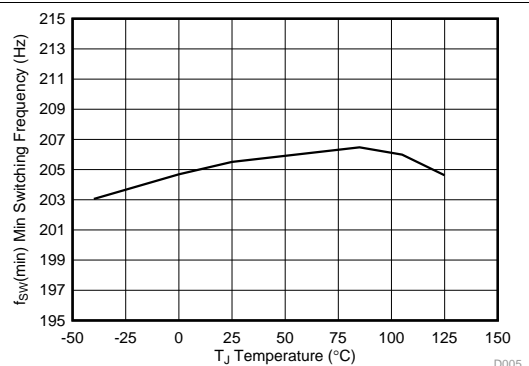


图 5. Minimum Switching Frequency vs. Temperature

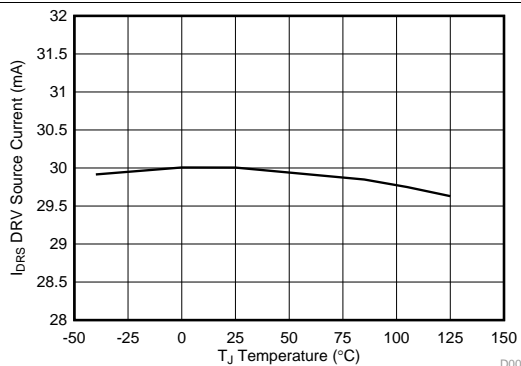


图 6. DRV Source Current vs. Temperature

Typical Characteristics (接下页)

VDD = 25 V, unless otherwise noted.

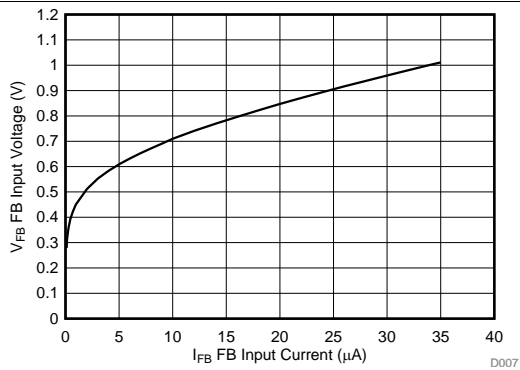


图 7. FB Input Voltage vs. FB Input Current

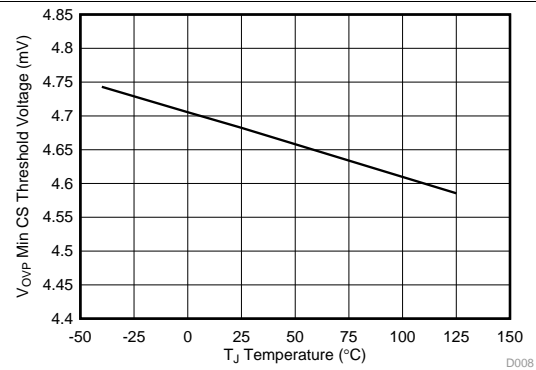


图 8. VS Overvoltage Threshold vs. Temperature

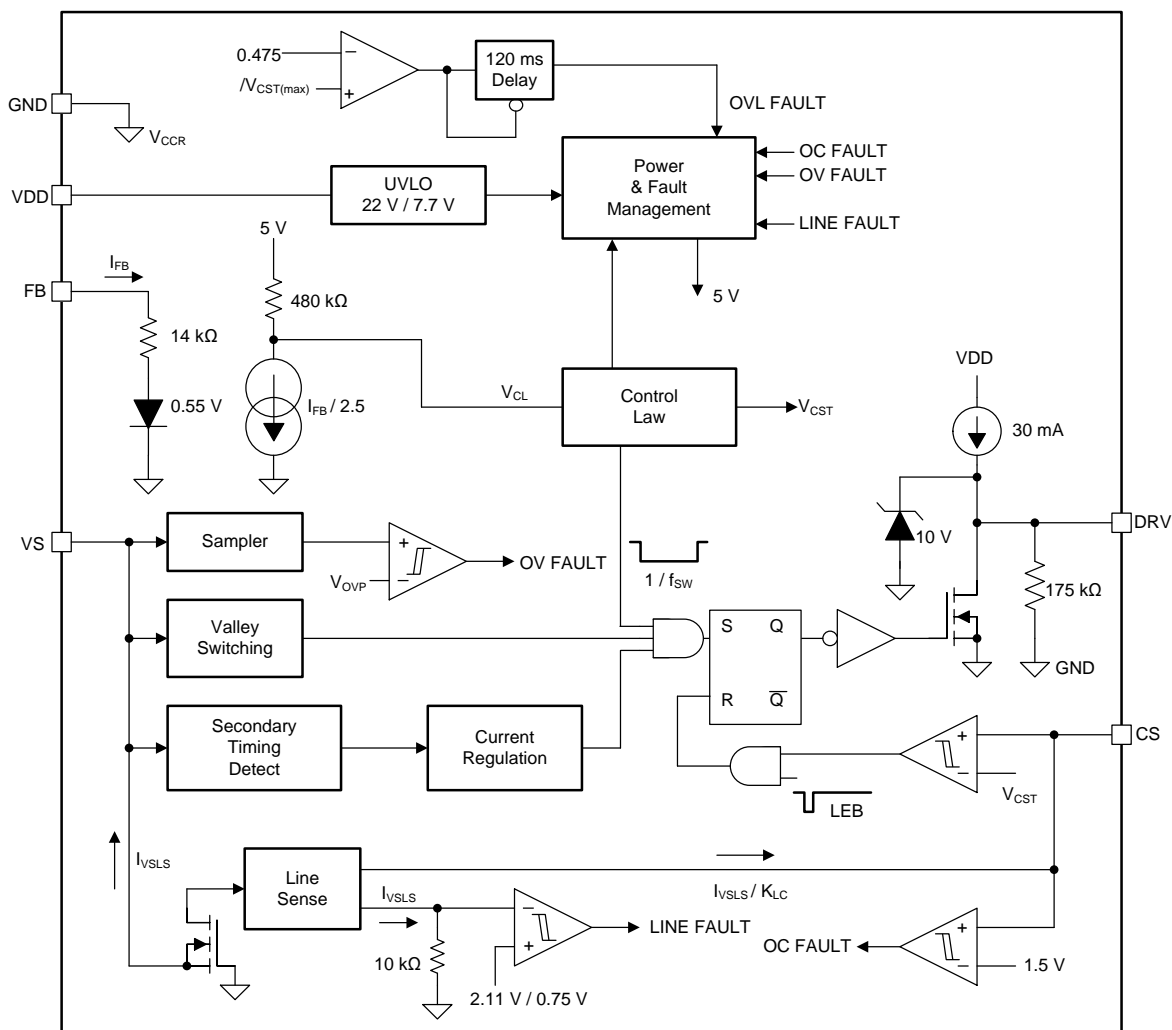
7 Detailed Description

7.1 Overview

The UCC28742 is a flyback power-supply controller which provides high-performance voltage regulation using an optically coupled feedback signal from a secondary-side voltage regulator. The device provides accurate constant-current regulation using primary-side feedback. The controller operates in discontinuous-conduction mode (DCM) with valley-switching to minimize switching losses and allow for the use of low cost output rectifiers. The control law scheme combines frequency with primary peak-current amplitude modulation to provide high conversion efficiency across the load range. The control law provides a wide dynamic operating range of output power which allows the power-supply designer to achieve low standby power dissipation.

During low-power operating conditions, the power-management features of the controller reduce the device-operating current at switching frequencies below 25 kHz. At and above this frequency, the UCC28742 includes features in the modulator to reduce the EMI peak energy of the fundamental switching frequency and harmonics. A complete low-cost and low component-count solution is realized using a straight-forward design process.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Detailed Pin Description

7.3.1.1 VDD (Device Bias Voltage Supply)

The VDD pin is typically powered from a rectified auxiliary transformer winding, the same winding that is used to capture the output voltage level. A bypass capacitor, with minimum value 0.047 μF , on the VDD pin is used for initially biasing the device to start-up along with a resistive or active source of start-up charging current. UVLO start / stop levels of 21.6 V / 7.8 V accommodate lower values of VDD capacitance that in turns keeps the start-up current low, which for resistive start-up has an impact on both stand-by power and power-on delay. A high, 35-V, maximum operating level on VDD alleviates concerns with leakage energy charging of VDD and gives added flexibility to when varying power supply output voltage must be supported.

7.3.1.2 GND (Ground)

This is an external return pin, and provides the reference point for both external signal and the gate drive of the device. The VDD bypass capacitor should be placed close to this pin. Critical component GND connections from the VS, FB and CS pins should have dedicated and short paths to this pin.

Feature Description (接下页)

7.3.1.3 VS (Voltage-Sense)

The VS pin connects to a resistor-divider from the auxiliary winding to ground. The auxiliary voltage waveform is sampled at the end of the transformer secondary-current demagnetization time. The waveform on the VS pin determines (1) the timing information to achieve valley-switching, (2) the timing to control the duty-cycle of the transformer secondary current, and (3) the output voltage over-voltage. Avoid placing a filter capacitor on this input which interferes with accurate sensing of this waveform.

Besides, the VS pin also has these two functions: (4) senses the bulk capacitor input voltage to provide for ac-input run and stop thresholds, and (5) to compensate the current-sense threshold across the AC-input range. This information is sensed by monitoring the current pulled out of the VS pin during the MOSFET on-time. During this time the voltage on the VS pin is clamped to about 250 mV below GND. As a result, the current out of the pin is determined by the upper VS divider resistor, the auxiliary to primary turns-ratio and the bulk input voltage level. For the AC-input run/stop function, the run threshold on VS is $I_{VSL(run)}$ (typical 210 μ A) and the stop threshold is $I_{VSL(stop)}$ (typical 75 μ A). The values for the auxiliary voltage divider upper-resistor R_{S1} and lower-resistor R_{S2} can be determined by the equations below.

$$R_{S1} = \frac{\sqrt{2} \times V_{IN(run)}}{N_{PA} \times I_{VSL(run)}} \approx \frac{V_{BULK(run)}}{N_{PA} \times I_{VSL(run)}}$$

where

- N_{PA} is the transformer primary-to-auxiliary turns ratio,
- $V_{IN(run)}$ is the AC rms voltage to enable turn-on of the flyback converter (run),
- $V_{BULK(run)}$ is the DC bulk voltage to enable turn-on of the flyback converter (run),
- $I_{VSL(run)}$ is the run-threshold for the current pulled out of the VS pin during the primary MOSFET on-time. (see the [Electrical Characteristics](#) table). (1)

$$R_{S2} = \frac{R_{S1} \times V_{OVP}}{N_{AS} \times (V_{OV} + V_F) - V_{OVP}}$$

where

- V_{OV} is the maximum allowable peak voltage at the converter output,
- V_F is the output rectifier forward voltage drop at near-zero current,
- N_{AS} is the transformer auxiliary to secondary turns ratio,
- R_{S1} is the VS divider upper-resistor resistance,
- V_{OVP} is the overvoltage detection threshold at the VS input (see the [Electrical Characteristics](#) table). (2)

Notice that VS pin absolute maximum current I_{VS} in its negative clamping is 1.2 mA. After determined R_{S1} it is required to check if VS pin current stays ≤ 1.2 mA. The check is to determine the input voltage ratio in this design and make $V_{IN(max)} / V_{IN(run)} \leq I_{VS} / I_{VSL(run)} = 1.2 \text{ mA} / 0.25 \text{ mA} = 4.8$, i.e., $V_{IN(max)} / V_{IN(run)} \leq 4.8$. If the design cannot meet this criterion, external circuit is needed to add in to make sure VS pin current ≤ 1.2 mA, for example, to use a zener type of device to clamp the transformer aux-winding negative voltage to achieve $V_{IN(max)} / V_{IN(run)} \leq 4.8$.

7.3.1.4 DRV (Gate Drive)

The DRV pin is connected to the MOSFET gate pin, usually through a series resistor. The DRV provides a gate drive signal which is clamped to 10-V internally. During turn-on the driver applies a typical 30-mA current source out of the DRV pin. When the DRV voltage rises to above 9 V the output current is reduced to about 100 μ A. This current brings the DRV voltage to the 10-V clamp level, or to VDD, whichever is less. The 30-mA current provides adequate turn-on speed while automatically limiting noise generated at turn-on by the MOSFET drain dv/dt and by the leading edge turn-on current spike. The gate drive turn-off current is internally limited to about 400 mA when DRV is above about 4 V. At lower DRV voltages the current will reduce, eventually being limited by the low-side on resistance, $R_{DS(on)}$. The drain turn-on and turn-off dv/dt can be further impacted by adding external resistor in series with DRV pin. The drain current resonances can be damped with a small series gate resistor, generally less than a 1 Ω .

Feature Description (接下页)

7.3.1.5 CS (Current Sense)

The current sense pin is connected through a series resistor (R_{LC}) to the current-sense resistor (R_{CS}). The controller varies the internal current sense threshold between 190 mV and 770 mV, setting a corresponding control range for the peak-primary winding current to a 4-to-1 range. The series resistor R_{LC} provides an input voltage feed-forward function. The voltage drop across this resistor reduces primary-side peak current as the line voltage increases, compensating for the increased di/dt and delays in the MOSFET turn-off. There is an internal leading-edge blanking time of 270 ns to eliminate sensitivity to the MOSFET turn-on leading edge current spike. If additional blanking time is needed, a small bypass capacitor, up to 30 pF, can be placed on between CS pin and GND pin. The value of R_{CS} is determined by the target output current in constant current (CC) regulation. The values of R_{CS} and R_{LC} can be determined by the equations below. The term η_{XFMR} is intended to account for the energy stored in the transformer but not delivered to the secondary. This includes transformer core and copper losses, bias power, and primary leakage inductance losses.

Example: With a transformer core and copper losses of 3%, leakage inductance caused power losses 2%, and bias power to output power ratio of 0.5%. The transformer power transfer efficiency is estimated as $\eta_{XFMR} = 100\% - 3\% - 2\% - 0.5\% = 94.5\%$

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2 \times I_{OCC}} \times \sqrt{\eta_{XFMR}}$$

where

- V_{CCR} is a current regulation constant (see the [Electrical Characteristics](#) table),
- N_{PS} is the transformer primary-to-secondary turns ratio (a typical turns-ratio of 12 to 15 is recommended for 5-V output as an example),
- I_{OCC} is the target output current in constant-current limit (refer to [Constant Current Limit and Delayed Shutdown](#) for more detail),
- η_{XFMR} is the transformer efficiency. (3)

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times (t_D + t_{GATE_OFF}) \times N_{PA}}{L_P}$$

where

- R_{S1} is the VS pin high-side resistor value,
- R_{CS} is the current-sense resistor value,
- t_D is the current-sense delay (typical 50 ns) plus MOSFET turn-off delay,
- t_{GATE_OFF} is the primary-side main MOSFET turn-off time,
- N_{PA} is the transformer primary-to-auxiliary turns-ratio,
- L_P is the transformer primary inductance,
- K_{LC} is a current-scaling constant (see the [Electrical Characteristics](#) table). (4)

7.3.1.6 FB (Feedback)

The FB pin connects to the emitter of an analog optocoupler output transistor which usually has the collector connected to VDD. The current supplied to FB by the optocoupler is reduced internally by a factor of 2.5 and the resulting current is applied to an internal 480-kΩ resistor to generate the control law voltage (V_{CL}). This V_{CL} directly determines the converter switching frequency and peak primary current required for regulation per the control-law for any given line and load condition.

Typical circuit connection between FB and optocoupler along with typical values of resistors and capacitors should be made as shown in [图 9](#). The resistors and capacitors in the connections help to stabilize operation during control mode transition.

Feature Description (接下页)

7.3.2 Secondary-Side Optically Coupled Constant-Voltage (CV) Regulation

图 9 shows a simplified flyback converter with the main output-regulation blocks of the device shown, along with typical implementation of secondary-side-derived regulation. The power-train operation is the same as any DCM-flyback circuit. A feedback current is optically coupled to the controller from a shunt-regulator sensing the output voltage.

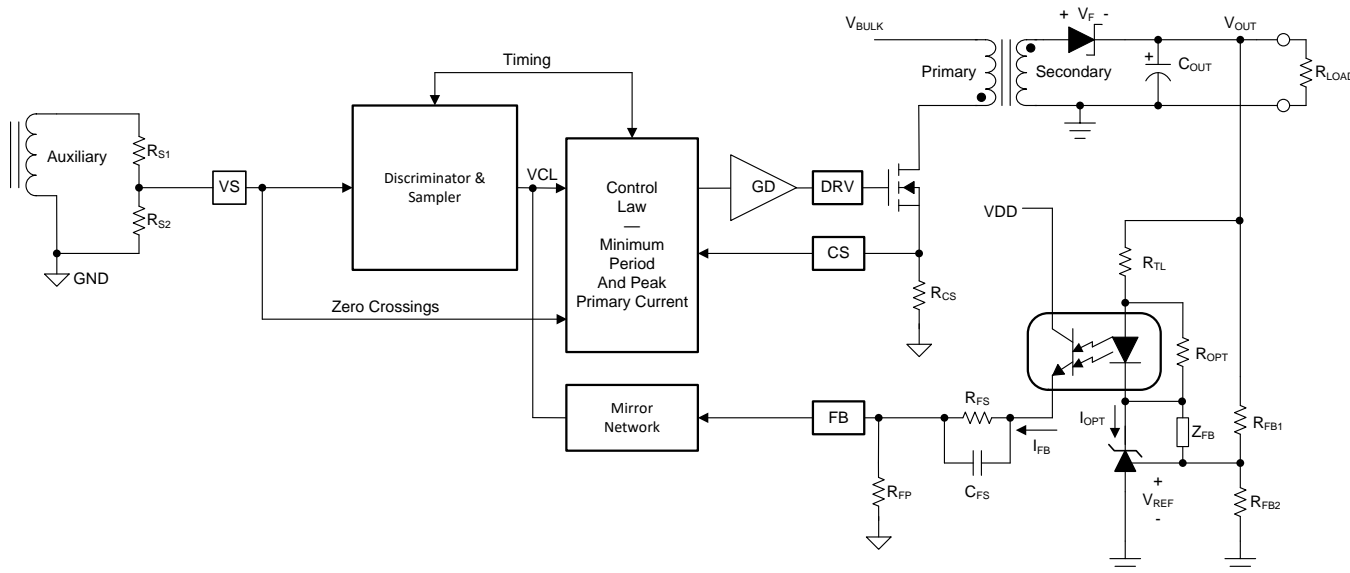


图 9. Simplified Flyback Converter
(with the Main Voltage Regulation Blocks)

In this configuration, a secondary-side shunt-regulator, such as the TL431 (or ATL431), generates a current through the input photo-diode of an optocoupler. The photo-transistor delivers a proportional current that is dependent on the current-transfer ratio (CTR) of the optocoupler to the FB input of the UCC28742 controller. This FB current then converts into the V_{CL} by the input-mirror network, detailed in the device block diagram (see [Functional Block Diagram](#)). Output-voltage variations convert to FB-current variations. The FB-current variations modify the V_{CL} which dictates the appropriate I_{PP} and f_{SW} necessary to maintain CV regulation. At the same time, the VS input senses the auxiliary winding voltage during the transfer of transformer energy to the secondary output to monitor for an output overvoltage condition. When f_{SW} reaches the converter target maximum frequency (i.e., corresponding de-mag time duty reaches 0.475), Constant Current Limit is triggered and further increases in V_{CL} cannot increase f_{SW} anymore. (see [图 10, Control Law](#) and [Constant Current Limit and Delayed Shutdown](#))

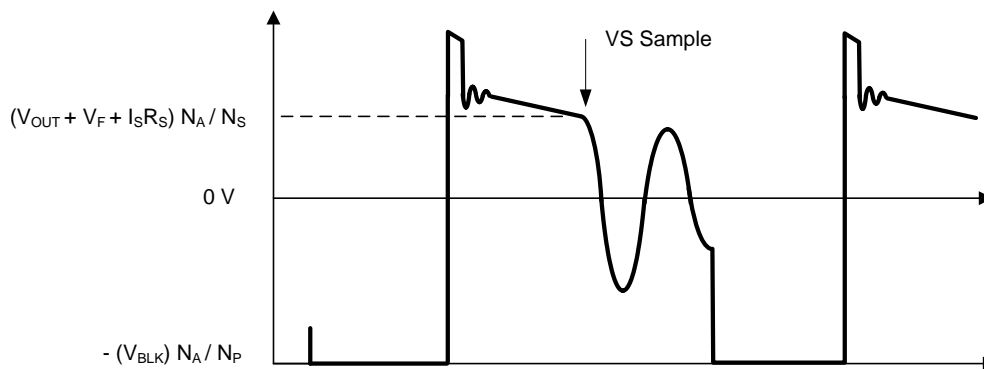


图 10. Auxiliary Winding Voltage

Feature Description (接下页)

The UCC28742 samples the VS input voltage at the end of demagnetization time for output overvoltage detection and to determine the total demagnetization time for output current control in Constant Current Limit operation.

In order to maintain best performance of these functions the reset time and ringing of the auxiliary winding voltage should meet certain guidelines. Referring to 图 11, the width of the leakage spike at the VS input should be less than t_{DM_BLANK} . Minimum t_{DM_BLANK} is 3 μs at maximum peak primary current levels and proportionally less at lower peak primary current levels (the lowest 0.75 μs should be observed at high line and no load condition). In addition, any ringing following the spike should be reduced to < 160 mVpp (scaled to the VS pin) 200 ns before the end of the demagnetization time.

As mentioned in [Device Functional Modes](#), when $I_{PP} < I_{PP(max)}$, the device operation enters a “Wait” state during each switching cycle of its non-switching portion as shown in 图 11. In the *Wait* state, the device bias current changes to I_{WAIT} (typical 80 μA) from I_{RUN} (typical 1.8 mA), reducing its bias power to help boost efficiency at light load and to reduce no-load input power.

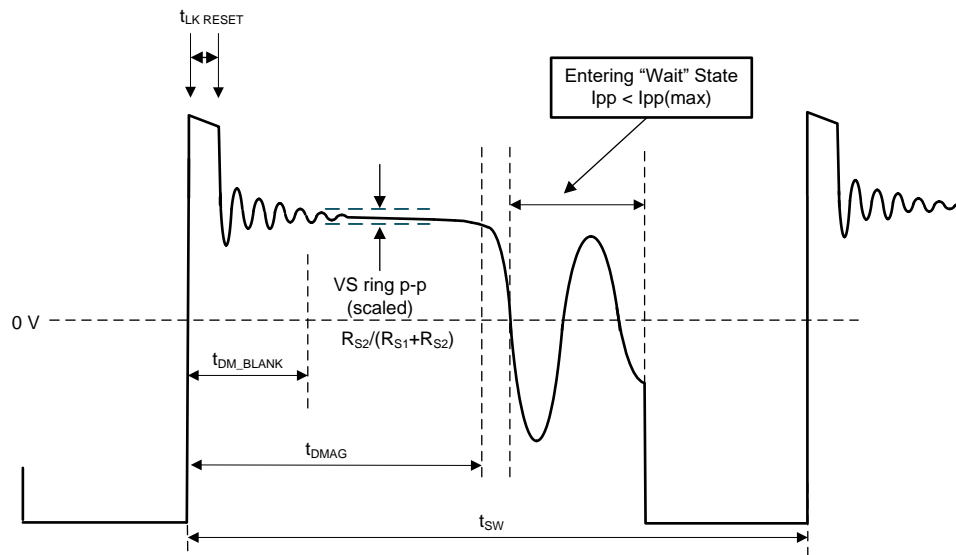


图 11. Auxiliary Waveform Details

Feature Description (接下页)

7.3.3 Control Law

During voltage regulation (CV mode), the controller operates in frequency modulation mode and peak current amplitude modulation mode as illustrated in 图 12 below. In CV mode operation, the control consists of four regions, namely, region FM 1, 2, AM and FM 3. The device internal V_{CL} sets a particular region of operation. Refer to 图 12 for V_{CL} .

The device internally limits its operating frequency between $f_{SW(min)}$ and $f_{SW(max)}$, typically between 200 Hz and 105 kHz. The choice of transformer primary inductance and primary-peak current sets the maximum operating frequency of the converter, which must be equal to or lower than $f_{SW(max)}$. Conversely, the choice of maximum target operating frequency and primary-peak current determines the transformer primary-inductance value. The actual minimum switching frequency for any particular converter depends on several factors, including minimum loading level, leakage inductance losses, switch-node capacitance losses, other switching and conduction losses, and bias-supply requirements. In any case, the minimum steady-state frequency of the converter must always exceed $f_{SW(min)}$ or the output voltage may rise to the over-voltage protection level (OVP) and the controller responds as described in [Fault Protection](#).

To achieve a regulated output voltage in the CV mode operation, energy balance has to be maintained. As the UCC28742 has a minimum switching frequency typical 200 Hz, together with the energy per switching cycle determined by converter parameters, such as the transformer primary inductance L_p and the selected R_{CS} resistor, the converter has a minimum input power. A proper pre-load needs to be selected to ensure that this minimum energy is balanced during the no-load condition. The selection of the line compensation resistor value (R_{LC}) connected to the CS pin can impact the energy per switching cycle based on low-line and high-line conditions. [Typical Application](#) section provides a design example to show how to implement these considerations.

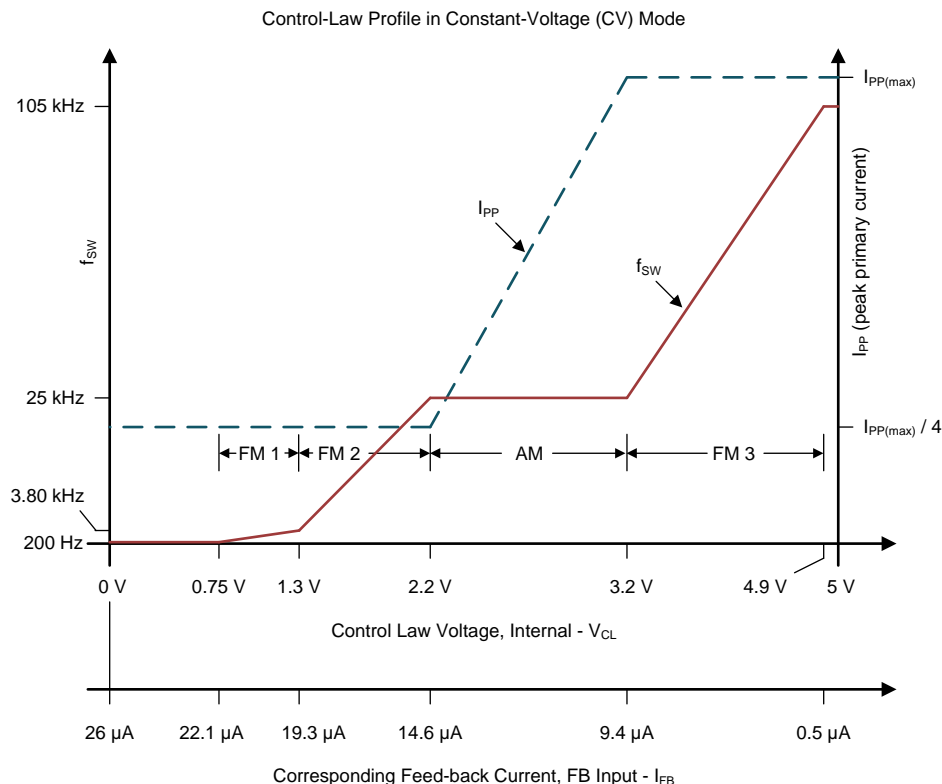


图 12. Frequency and Amplitude Modulation Modes (during CV mode)

Feature Description (接下页)

The steady-state control-law voltage, V_{CL} , ranges between 0.75 V to 4.90 V. Heavy load operation is usually in Region FM 3 where frequency modulation to output regulation is used and primary-peak current is controlled at its maximum. The AM region is usually for medium-load range typically from 10% load and above. In this region switching frequency is fixed at nominal 25 kHz along with primary-peak current varying from 25% to 100% of its maximum. The low operating frequency ranges are for lighter loads to achieve stable regulation at low frequencies. In regions FM 1 and 2, peak-primary current is always maintained at $I_{PP(max)}/4$. Transitions between levels are automatically accomplished by the controller depending on the internal control-law voltage, V_{CL} and its corresponding FB pin current I_{FB} . An internal frequency-dithering mechanism is enabled in Region FM 3 to reduce conducted EMI, and is disabled otherwise. The *Wait* state is enabled in regions FM 1, 2, and AM, refer to 图 11.

7.3.4 Constant Current Limit and Delayed Shutdown

Timing information at the VS pin and current information at the CS pin allow accurate regulation of the secondary constant current limit, CCL, thus to achieve load over-current protection. The control law dictates that as power is increased in CV regulation and approaching CCL the primary-peak current is at $I_{PP(max)}$. Referring to 图 13 below, the primary peak current (I_{PP}), turns-ratio (N_S/N_P), secondary demagnetization time (t_{DMAG}), and switching period (t_{SW}) determine the secondary average output current. Ignoring leakage inductance effects, the average output current is given by 公式 5. By regulating the secondary rectifier conduction duty cycle, the output current limit is achieved for given I_{PP} and transformer turns-ratio. When the load increases, the secondary-side rectifier conduction duty cycle keep increasing. Once this duty cycle reaches preset value of 0.475, the converter switching frequency stops increasing and starts adjusting to reduce and maintain 0.475 secondary-side duty cycle. Therefore, the output constant current limit is achieved. Because the current is kept constant, the increasing load results in lower output voltage.

$$I_{OUT} = \frac{I_{PP}}{2} \times \frac{N_P}{N_S} \times \frac{t_{DMAG}}{t_{SW}} \quad (5)$$

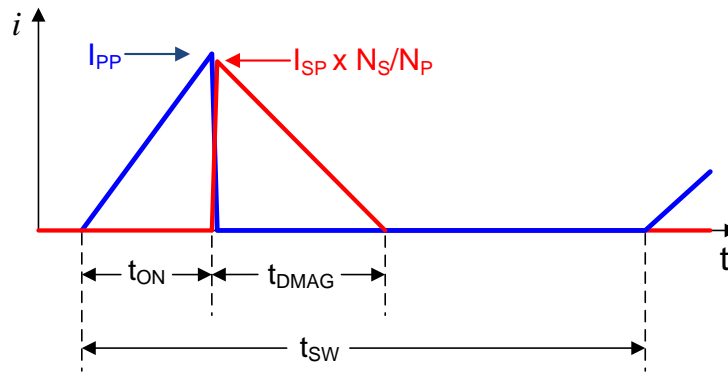


图 13. Transformer Currents

As shown in 图 14 below, CV mode operation is from $I_O = 0$ to $< I_{OCC}$; at $I_O = I_{OCC}$, the operation enters constant current limit mode and V_O starts to drop as the load resistance becomes further lower while I_O is maintained at I_{OCC} for a time interval specified by t_{OVL_TIME} typically 120 ms then DRV stops to achieve converter output delayed shutdown. During the 120-ms timing interval, if load I_O reduces to $< I_{OCC}$, the timer will be reset and no shutdown will occur. The V-I curve corresponding to the operation is shown in 图 14, and the delayed shutdown timing diagram is shown in 图 15. Note (1) The timer t_{OVL_TIME} is triggered whenever I_O reaches I_{OCC} and reset when I_O drops to $< I_{OCC}$ before 120ms-time-out. (2) during 120-ms time interval, when load resistance becomes so low during constant current interval that causes the device VDD to reach its $V_{VDD(off)}$ and then the shutdown will be through VDD undervoltage lockout instead of through Constant Current Limit and Delayed Shutdown. In such a case, the shutdown can happen before 120ms timer out.

Feature Description (接下页)

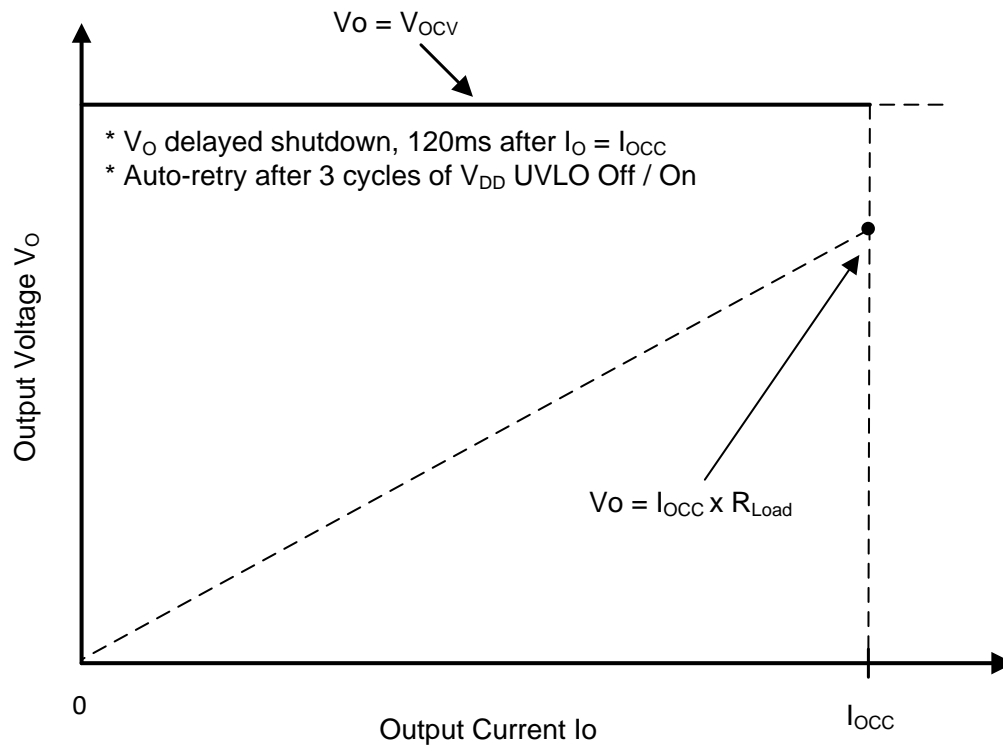


图 14. Typical Target Output V-I Characteristics

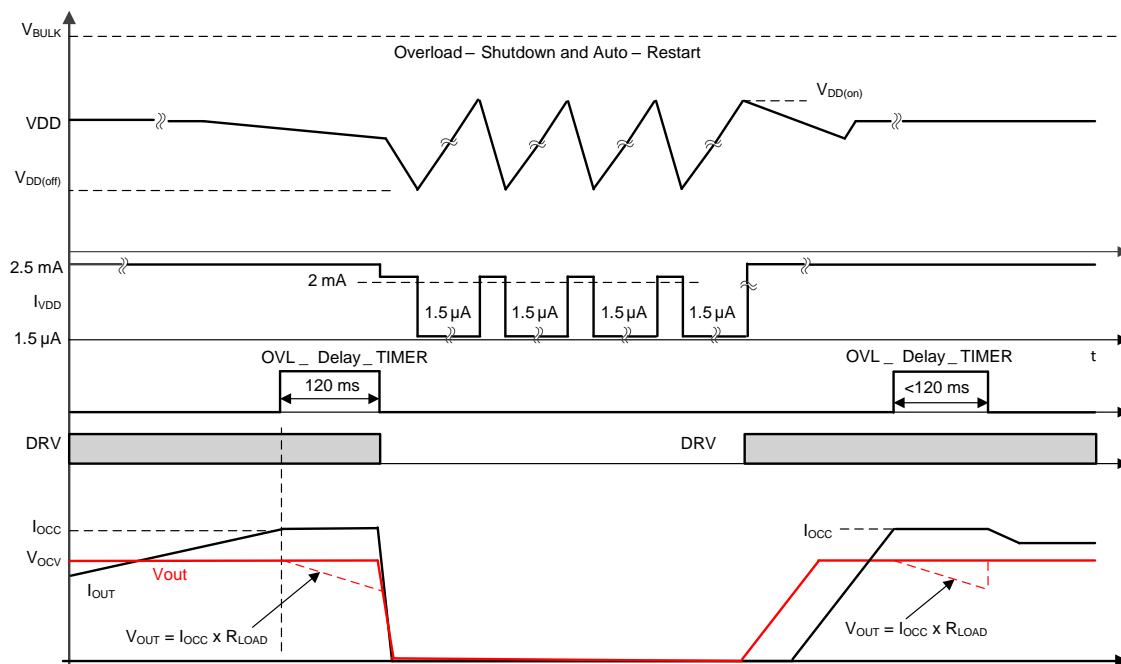


图 15. Output Delayed Shutdown Timing

Feature Description (接下页)

7.3.5 Valley-Switching and Valley-Skipping

The UCC28742 utilizes valley switching to reduce switching losses in the MOSFET, reduce induced-EMI, and minimize the turn-on current spike at the sense resistor. The controller operates in valley-switching in all load conditions unless the V_{DS} ringing diminished.

Referring to 图 16 below, the UCC28742 operates in a valley-skipping mode in most load conditions to maintain an accurate voltage or current regulation point and still switch on the lowest available V_{DS} voltage.

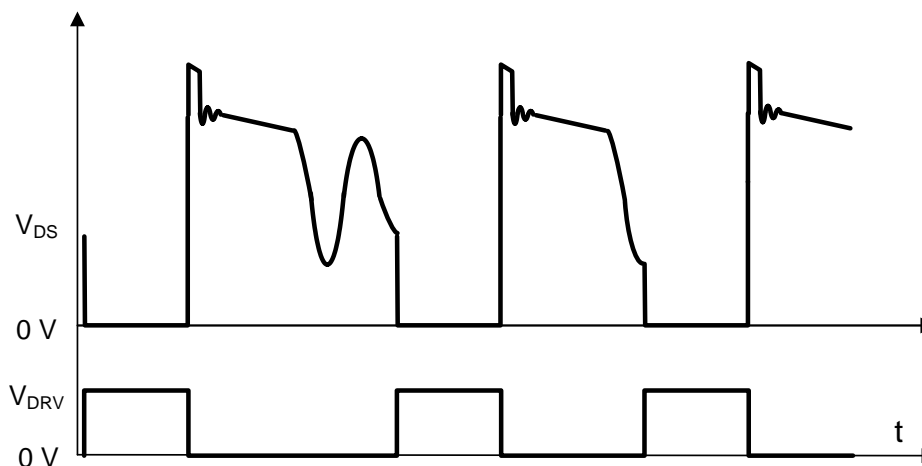


图 16. Valley-Skipping Mode

The UCC28742 forces a controlled minimum switching period corresponding to the power supply operating frequency. In each switching cycle, after the minimum period is expired, the UCC28742 looks for the next resonant valley on the auxiliary winding. The controller initiates a new power cycle at this valley point which corresponds to a reduced voltage level on the power MOSFET. If at the point in time when the minimum period expires ringing on the transformer winding has decayed such that no further resonant valleys can be detected a new power cycle is initiated following a fixed time, t_{ZTO} . This also applies when primary inductance L_P is designed with a high value that causes de-mag end ringing cycle longer than t_{ZTO} . When either happens, the valley switching is lost but the converter output voltage will still be in regulation.

Feature Description (接下页)

7.3.6 Start-Up Operation

Upon application of input voltage to the converter, the start up resistance connected to VDD from the bulk capacitor voltage (V_{BULK}) charges the VDD capacitor. During charging of the VDD capacitor, the device supply current is typical 1.5 μ A. When VDD reaches the 21.6-V UVLO turn-on threshold, the controller is enabled and the converter starts switching. The peak-primary currents with initial three cycles are limited to $I_{PP(min)}$. This allows sensing any initial input or output faults with minimal power delivery. When confirmed that the input voltage is above the programmed converter turn-on voltage and with no faults detected, the start-up process proceeds and normal power conversion follows. The converter remains in discontinuous conduction mode operation during charging of the output capacitor(s), maintaining a constant output current until the output voltage is in regulation.

A commonly used initial power-on approach for UCC28742 is to use a start-up resistor, R_{STR} , to tie VDD to V_{BULK} , as show in 图 17. With this approach, the VDD pin is connected to a bypass capacitor to ground and a start-up resistance to the input bulk capacitor (+) terminal. The VDD turn-on UVLO threshold is 21.6 V ($V_{VDD(on)}$) and turn-off UVLO threshold is 7.8 V ($V_{VDD(off)}$), with an available operating range up to 35 V. The additional VDD headroom up to 35 V allows for VDD to rise due to the leakage energy delivered to the VDD capacitor in heavy-load conditions. Also, the wide VDD range provides the advantage of selecting a relatively small VDD capacitor and high-value startup resistance to minimize no-load standby power loss in the startup resistor.

The R_{STR} value has an effect to power-on delay time and no-load standby power losses. Both are usually part of the design specifications. Increasing R_{STR} reduces standby power losses while also increasing power-on delay time. A typical range of R_{STR} is between 1 M Ω and 10 M Ω as a good initial design point for off-line AC-to-DC adapters. Due to the limited voltage rating, R_{STR} is normally implemented by two or three resistors in series.

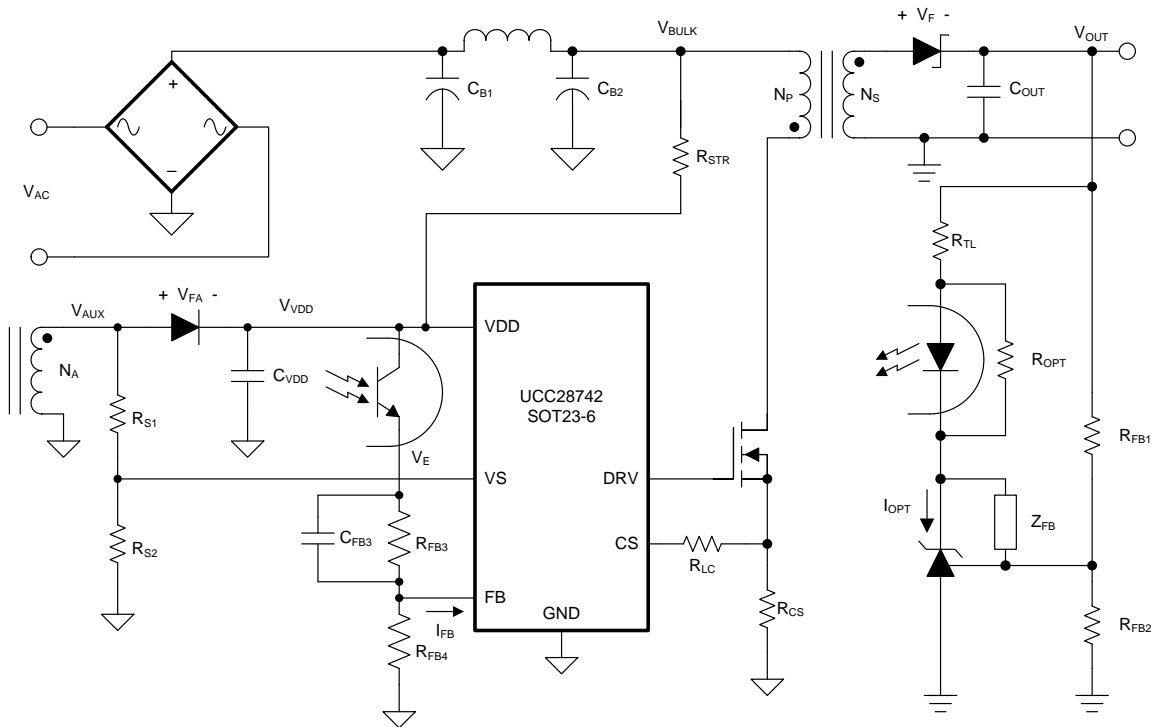


图 17. Power-On with Start-Up Resistor

Feature Description (接下页)

7.3.7 Fault Protection

There is comprehensive fault protection incorporated into the UCC28742. Protection functions include:

- Output Over-Voltage
- Input Under-Voltage
- Primary Over-Current Fault
- CS Pin Open Fault
- CS Pin Short-to-GND Fault
- VS Pin Fault
- Device Internal Over-Temperature
- Constant Current Limit and Delayed Output Shutdown - Output Over-Current Protection

Output Over-Voltage: The output over-voltage function is determined by the voltage feedback on the VS pin. If the voltage sample on VS exceeds 4.65 V (V_{OVP}), for three consecutive switching cycles an OV fault is asserted. Once asserted the device stops switching, initiating a UVLO reset and re-start fault cycle. During the fault, the VDD bias current remains at the run current level, discharging the VDD pin to the UVLO turn-off threshold, $V_{VDD(off)}$. After that, the device returns to the start state, VDD now charging to $V_{VDD(on)}$ where switching is initiated. The UVLO sequence repeats as long as the fault condition persists.

Input Under-Voltage: The line input run and stop thresholds are determined by current information at the VS pin during the MOSFET on-time. While the VS pin is clamped close to GND during the MOSFET on-time, the current through R_{S1} , out of the VS pin, is monitored to determine a sample of the bulk capacitor voltage. A wide separation of run and stop thresholds allows clean start-up and shut-down of the power supply with the line voltage. From the start state, the sensed VS current, I_{VSL} , must exceed the run current threshold, $I_{VSL(run)}$ (typical 211 μ A), within the first three cycles after switching starts as VDD reaches $V_{VDD(on)}$. If it does not, then switching stops and the UVLO reset and re-start fault cycle is initiated. Once running, I_{VSL} must drop below the stop level, $I_{VSL(stop)}$ (typically 75 μ A), for three consecutive cycles to initiate the fault response.

Primary Over-Current: The UCC28742 always operates with cycle-by-cycle primary-peak current control. The normal operating range of the CS pin is 190 mV to 770 mV. If the voltage on CS exceeds the 1.5-V over-current level, any time after the internal leading edge blanking time and before the end of the transformer demagnetization, for three consecutive cycles, the device shuts down and the UVLO reset and re-start fault cycle begins.

CS Pin Open: The CS pin has a 2- μ A minimum pull-up that brings the CS pin above the 1.5-V OC fault level if the CS pin is open. This causes the primary over-current fault after three cycles.

CS Pin Short to GND: On the first, and only the first, cycle at start-up during power on, the device checks to verify that the $V_{CST(min)}$ threshold is reached at the CS pin within 5 μ s of DRV going high. If the CS voltage fails to reach this level then the device terminates the current cycle and immediately enters the UVLO reset and re-start fault sequence.

VS Pin: Protection is included in the event of component failures on the VS pin. If the high-side VS divider resistor opens the controller stops switching. VDD collapses to its $V_{VDD(off)}$ threshold, a start-up attempt follows with a single DRV on-time when VDD reaches $V_{VDD(on)}$. The UVLO cycle will repeat. If the low-side VS divider resistor is open then an output over-voltage fault occurs.

Device Internal OTP: The internal over-temperature protection threshold is 165 °C. If the junction temperature of the device reaches this threshold the device initiates the UVLO reset and re-start fault cycle. If the temperature is still high at the end of the UVLO cycle, the protection cycle repeats.

Constant Current Limit and Delayed Output Shutdown - Output Over-Current Protection: The load over-current protection is made precisely using constant current limit and delayed output shutdown as described in section [Constant Current Limit and Delayed Shutdown](#)

7.4 Device Functional Modes

The UCC28742 operates in different modes according to input voltage, VDD voltage, and output load conditions:

- At start-up, when VDD is less than the turn-on threshold, $V_{VDD(on)}$, the device is simply waiting for VDD to reach this threshold while the VDD capacitor is getting charged.
- When VDD exceeds $V_{VDD(on)}$, the device starts switching to deliver power to the converter output. The initial 3 switching cycles control the primary-peak current to $I_{PP(min)}$. This allows sensing any initial input or output faults with minimal power delivery. When confirmed with input voltage above predetermined level and no fault conditions, start up process proceeds and normal power conversion follows. The converter will remain in discontinuous current mode operation during charging of the output capacitor(s), maintaining a constant output current, I_{OCC} , until the output voltage reaches its regulation point. The maximum time duration when I_O stays on I_{OCC} can only last 120 ms, and when 120-ms timer out, the device will initiate shutdown. Therefore, a design needs to make sure the maximum time when output current reaches and stays on I_{OCC} does not exceed 120 ms during start. For more details refer to [Constant Current Limit and Delayed Shutdown](#)
- When operating with $I_{PP} = I_{PP(max)}$, the UCC28742 operates continuously in the *run* state. In this state, the VDD bias current is always at I_{RUN} plus the average gate-drive current.
- When operating with $I_{PP} < I_{PP(max)}$, the UCC28742 operates in the *wait* state between switching cycles and in the *run* state during a switching cycle. In the *wait* state, the VDD bias current is reduced to I_{WAIT} after demagnetizing time of each switching cycle to improve efficiency at light loads. This helps reduce no-load to medium-load power losses, particularly for achieving higher efficiency at 10%, 25% load conditions, and possible at < 50% load conditions, depending on a design.
- The device operation will stop if any events occur as listed below:
 - If VDD drops below the $V_{VDD(off)}$ threshold, the device stops switching, its bias current consumption is lowered to I_{START} until VDD rises above the $V_{VDD(on)}$ threshold. The device then resumes operation through start-up.
 - If a fault condition is detected, the device stops switching and its bias current consumption becomes I_{FAULT} . This current level discharges VDD to $V_{VDD(off)}$ where the bias current changes from I_{FAULT} to I_{START} until VDD rises above the $V_{VDD(on)}$ threshold.
- If a fault condition persists, the operation sequence described above in repeats until the fault condition or the input voltage is removed. Refer to [Fault Protection](#) for fault conditions and post-fault operation.

Typical Application (接下页)

8.2.1 Design Requirements

The following table illustrates a typical subset of high-level design requirements for a particular converter of which many of the parameter values are used in the various design equations in this section. Other necessary design parameters, $V_{BULK(min)}$ for example, may not be listed in such a table. These values may be selected based on design experience or other considerations, and may be iterated to obtain optimal results.

表 1. UCC28742 Design Parameters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V _{IN}	AC-line input voltage		85	115/230	265	V _{RMS}
f _{LINE}	Line frequency		47	50/60	63	Hz
P _{STBY}	No-load input power	V _{IN} = typ, I _O = 0A	65			mW
OUTPUT CHARACTERISTICS						
V _O	DC output voltage	V _{IN} = typ, I _O = 0 to I _{OR}	5			V
V _{RIPPLE}	Output voltage ripple	V _{IN} = typ, I _O = I _{OR}	50			mV
I _{OR}	Output rated current	V _{IN} = min to max	2.0			A
I _{OVL}	Overload current Limit	V _{IN} = typ	2.05			A
OVL delay	Overload shutdown delay	V _{IN} = typ, I _O = I _{OCC}	120			ms
η _{AVG}	Average efficiency	V _{IN} = typ, average of 25%, 50%, 75%, and 100% Load	82			%
SYSTEMS CHARACTERISTICS						
f _{sw}	Switching frequency		0.2	65		kHz

8.2.2 Detailed Design Procedure

This procedure outlines the steps to design a constant output voltage (V_{OCV}) flyback converter using the UCC28742 controller. Please refer to the [Figure 18](#) for circuit details and section for variable definitions used in the applications equations below.

8.2.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the UCC28742 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 VDD Capacitance, C_{DD}

The capacitance on VDD needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage. At this time the auxiliary winding can sustain the voltage to the UCC28742. The total output current available to the load and to charge the output capacitors is the constant-current regulation target. The equation below assumes the output current of the flyback is available to charge the output capacitance until the minimum output voltage is achieved to maintain VDD above its $V_{DD(on)}$. The gate-drive current depends on particular MOSFET to be used. If with an estimated average 1.0 mA of gate-drive current, C_{DD} is determined by [Equation 6](#), and at I_{OCC} , $V_{OCC} = V_{OCV}$.

$$C_{DD} = \frac{(I_{RUN} + 1.0mA) \times \frac{C_{OUT} \times V_{OCV}}{I_{OCC}}}{(V_{DD(on),min} - V_{DD(off),max})} \quad (6)$$

8.2.2.3 VDD Start-Up Resistance, R_{STR}

Once the VDD capacitance is known, the start-up resistance from V_{BULK} to achieve the power-on delay time (t_{STR}) target can be determined.

$$R_{STR} = \frac{\sqrt{2} \times V_{IN(min)}}{I_{START} + \frac{V_{DD(on)} \times C_{DD}}{t_{STR}}} \quad (7)$$

8.2.2.4 Input Bulk Capacitance and Minimum Bulk Voltage

Determine the minimum voltage on the input capacitance, C_{B1} and C_{B2} total, in order to determine the maximum N_p to N_s turns ratio of the transformer. The input power of the converter based on target full-load efficiency, minimum input rms voltage, and minimum AC input frequency are used to determine the input capacitance requirement.

Maximum input power is determined based on V_{OCV} , load current over load $I_{OVL} = I_{OCC}$, and the full-load efficiency target. An initial estimate of efficiency can be assumed for full-load efficiency, for example 89% for a converter of rated power 48 W and output voltage 24 V.

$$P_{IN} = \frac{V_{OCV} \times I_{OCC}}{\eta} \quad (8)$$

公式 9 provides an accurate solution for input capacitance based on a target minimum bulk capacitor voltage. To target a given input capacitance value, iterate the minimum capacitor voltage to achieve the target capacitance.

$$C_{BULK} = \frac{P_{IN} \times \left(0.5 + \frac{1}{\pi} \times \arcsin \left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}} \right) \right)}{(2V_{IN(min)}^2 - V_{BULK(min)}^2) \times f_{LINE}} \quad (9)$$

8.2.2.5 Transformer Turns Ratio, Inductance, Primary-Peak Current

The maximum primary-to-secondary turns ratio can be determined by the target maximum switching frequency at full load, the minimum input capacitor bulk voltage, and the estimated DCM resonant time.

Initially determine the maximum available total duty cycle of the on time and secondary conduction time based on target switching frequency and DCM resonant time. For DCM resonant time, assume 500 kHz if you do not have an estimate from previous designs. For the transition mode operation limit, the period required from the end of secondary current conduction to the first valley of the V_{DS} voltage is $\frac{1}{2}$ of the DCM resonant period, or 1 μ s assuming 500-kHz resonant frequency. D_{MAX} can be determined using 公式 10.

$$D_{MAX} = 1 - \left(\frac{t_R}{2} \times f_{MAX} \right) - D_{MAGCC} \quad (10)$$

Once D_{MAX} is known, the maximum turns ratio of the primary to secondary can be determined with the equation below. D_{MAGCC} is defined as the secondary diode conduction duty cycle when load current reaches a specified limit operation. It is set internally by the UCC28742 at 0.475. The total voltage on the secondary winding needs to be determined; which is the sum of V_{OCV} and the secondary rectifier V_F .

$$N_{PS(max)} = \frac{D_{MAX} \times V_{BULK(min)}}{D_{MAGCC} \times (V_{OCV} + V_F)} \quad (11)$$

N_{PS} is determined also with other design factors such as voltage and current ratings of primary MOSFET, secondary rectifier diode, as well as secondary MOSFET if synchronous rectifier is used. Once an optimum turns-ratio is determined from a detailed transformer design, use this ratio for the following parameters.

The UCC28742 controller constant current limit is achieved by maintaining $D_{MAGCC} = 0.475$ at the maximum primary current setting. The transformer turns ratio and current limit determine the current sense resistor for a target constant current limit.

Since not all of the energy stored in the transformer is transferred to the secondary, a transformer efficiency term is included. This efficiency number includes the core and winding losses, leakage inductance ratio, and bias power ratio to rated output power. A bias power can be initially estimated at 0.1% to 0.5% rated power depending on power rating. An overall transformer efficiency of 94.5% is a good estimation of assuming 2% leakage inductance, 3% core and winding loss, and 0.5% bias power.

R_{CS} is used to program the primary-peak current with 公式 12:

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2 \times I_{OCC}} \times \sqrt{\eta_{XFMR}} \quad (12)$$

The primary transformer inductance can be calculated using the standard energy storage equation for flyback transformers. Primary current, maximum switching frequency, output and transformer efficiency are included in [公式 14](#).

Initially the transformer primary current should be determined. Primary current is simply the maximum current sense threshold divided by the current sense resistance.

$$I_{PP(max)} = \frac{V_{CST(max)}}{R_{CS}} \quad (13)$$

$$L_P = \frac{2 \times (V_{OCV} + V_F) \times I_{OCC}}{\eta_{XFMR} \times I_{PP(max)}^2 \times f_{MAX}} \quad (14)$$

The primary inductance L_P in [公式 14](#) also needs to consider primary MOSFET minimum turn on time as described in [Transformer Parameter Verification](#).

The auxiliary winding to secondary winding transformer turns-ratio (N_{AS}) is determined by the lowest target operating output voltage V_{OVL} at current limit and above the $V_{DD(off)}$ of the UCC28742. The output voltage reaches V_{OVL} when output current reaches its limit I_{OCC} ; V_{OVL} is determined by I_{OCC} and the expected minimum load resistance R_{LOAD} at I_{OCC} , i.e., $V_{OVL} = I_{OCC} \times R_{LOAD}$. Note that V_{OVL} can only be maintained within typical 120ms, and after that time, the output voltage will enter the cycle of shutdown and auto-start retry, as described in [Constant Current Limit and Delayed Shutdown](#), and shown in [图 14](#) and [图 15](#). There is additional energy supplied to VDD from the transformer leakage inductance energy which may allow a slightly lower turns-ratio to be used in a design. The N_{AS} is then determined by the below equation.

$$N_{AS} = \frac{V_{DD(off)} + V_{FA}}{V_{OCC} + V_F} \quad (15)$$

8.2.2.6 Transformer Parameter Verification

The transformer turns-ratio selected affects the MOSFET V_{DS} and secondary rectifier reverse voltage so these should be reviewed. The UCC28742 controller requires a minimum on time of the MOSFET (t_{ON}) and minimum D_{MAG} time ($t_{DMAG(min)}$) of the secondary rectifier in the high line, under minimum-load condition. The selection of f_{MAX} , L_P and R_{CS} affects the minimum t_{ON} and t_{DMAG} .

The secondary rectifier and MOSFET voltage stress can be determined by the equations below.

$$V_{REV} = \frac{V_{IN(max)} \times \sqrt{2}}{N_{PS}} + V_{OCV} \quad (16)$$

For the MOSFET V_{DS} voltage stress, an estimated leakage inductance voltage spike (V_{LK}) needs to be included.

$$V_{DSPK} = \left(V_{IN(max)} \times \sqrt{2} \right) + \left(V_{OCV} + V_F \right) \times N_{PS} + V_{LK} \quad (17)$$

The following equations are used to determine for the minimum t_{ON} target of 0.35 μs and minimum de-mag time, $t_{DMAG(min)}$, target of 1.7 μs . Notice that the minimum t_{ON} target of 0.35 μs is determined by CS pin **Leading-edge blanking time**, T_{CSLEB} in [Electrical Characteristics](#). The target is to design L_P and make $t_{ON(min)} \geq T_{CSLEB}$. But in very worst normal operation condition, during the $t_{ON(min)}$, the CS pin OCP should not be triggered, i.e., the CS pin should not reach near 1.41 V defined by V_{OCP} in [Electrical Characteristics](#).

$$t_{ON(min)} = \frac{L_P}{V_{IN(max)} \times \sqrt{2}} \times \frac{I_{PP(max)}}{K_{AM}} \quad (18)$$

$$t_{DMAG(min)} = \frac{t_{ON(min)} \times V_{IN(max)} \times \sqrt{2}}{N_{PS} \times (V_{OCV} + V_F)} \quad (19)$$

8.2.2.7 VS Resistor Divider and Line Compensation

The VS divider resistors determine the output voltage regulation point of the flyback converter, also the high-side divider resistor (R_{S1}) determines the line voltage at which the controller enables continuous DRV operation. R_{S1} is initially determined based on the transformer auxiliary to primary turns-ratio and the desired input voltage operating threshold.

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(run)}} \quad (20)$$

$I_{VSL(run)}$ is VS pin run current with a typical value 210 μ A for a design. The low-side VS pin resistor is selected based on desired output over voltage V_{OV} .

$$R_{S2} = \frac{R_{S1} \times V_{OVP}}{N_{AS} \times (V_{OV} + V_F) - V_{OVP}} \quad (21)$$

The UCC28742 can maintain tight output current limit over input line by utilizing the line compensation feature. The line compensation resistor (R_{LC}) value is determined by current flowing in R_{S1} and expected gate drive and MOSFET turn-off delay. Assume a 50-ns internal delay in the UCC28742.

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times (t_D + t_{GATE_OFF}) \times N_{PA}}{L_P} \quad (22)$$

8.2.2.8 Standby Power Estimate

Assuming no-load standby power is a required design parameter, determine the estimated no-load power based on target converter maximum switching frequency and output power rating. The following equation estimates the stand-by power of the converter.

$$P_{SB_CONV} \cong \frac{P_{OUT} \times f_{MIN}}{\eta \times K_{AM}^2 \times f_{MAX}} \quad (23)$$

The output preload resistor can be estimated by V_{OCV} and the difference between the converter stand-by power and the no-load bias power P_{NL_BIAS} (that can be set as zero initially and adjust it later, particularly through the bench test), then the preload resistor value is estimated in 公式 24 :

$$R_{PL} = \frac{V_{OCV}^2}{P_{SB_CONV} - P_{NL_BIAS}} \quad (24)$$

A physical resistor component R_{PL} may not be needed as other components on the secondary-side such as TL431 can already provide enough preload.

The capacitor bulk voltage for the loss estimation is based on the highest voltage for the standby power measurement, typically as $325 V_{DC}$ (or AC input of $230 V_{rms}$). Power loss of R_{STR} is estimated in 公式 25:

$$P_{RSTR} = \frac{(V_{BULK} - V_{DD})^2}{R_{STR}} \quad (25)$$

The total standby power, including the converter standby power loss, the start-up resistance power, and the snubber power loss, is estimated in 公式 26:

$$P_{SB} = P_{SB_CONV} + P_{RSTR} + P_{SNBR} \quad (26)$$

8.2.2.9 Output Capacitance

The output capacitance value is typically determined by the transient response requirement. 公式 27 assumes that the switching frequency can be at the UCC28742 minimum of $f_{SW(min)}$.

$$C_{OUT} = \frac{I_{TRAN} \left(\frac{1}{f_{SW(min)}} + 50\mu s \right)}{\Delta V_O} \quad (27)$$

Another consideration of the output capacitor(s) is the ripple voltage requirement. The output capacitors and their total ESR are the main factors to determine the output voltage ripple. 公式 28 provides a formula to determine required ESR value R_{ESR} , and 公式 28 provides a formula to determine required capacitance. The total output ripple is the sum of these two parts with scale factors and 10mV to consider other noise as shown in 公式 30,

$$R_{ESR} = \frac{1}{I_{PP(max)} \times N_{PS}} \times V_{RIPPLE_R} \quad (28)$$

$$C_{OUT} = \frac{L_P \times I_{PP(max)}^2}{4 \times (V_{OCV})} \times \frac{1}{V_{RIPPLE_C}} \quad (29)$$

$$V_{RIPPLE} = 0.81 \times V_{RIPPLE_R} + 1.15 \times V_{RIPPLE_C} + 10mV \quad (30)$$

Example: if require $V_{RIPPLE} = 70 mV$, assume $0.81 \times V_{RIPPLE_R} = 1.15 \times V_{RIPPLE_C} = 30 mV$, then $R_{ESR} = 4.05 m\Omega$, and $C_{OUT} = 643 \mu F$, with assumption of $L_P = 700 \mu H$, $I_{PP(max)} = 0.713 A$, $N_{PS} = 13$, $V_{OCV} = 5.3 V$.

8.2.2.10 Feedback Loop Design Consideration

Refer to 图 18, the UCC28742 converter feedback network is composed of TL431, optocoupler and several resistors and capacitors. R_{FB1} and R_{FB2} set up the converter output regulation point. A series-resistor R_{FB3} is necessary to limit the current into FB and to avoid excess draining of C_{VDD} during this type of transient situation, although connecting the emitter directly to the FB input of the UCC28742 is possible. However, an unload-step response may unavoidably drive the optocoupler into saturation which will overload the FB input with full VDD applied. The value of R_{FB3} is to limit the excess I_{FB} to an acceptable level when the optocoupler is saturated. The R_{FB3} value is chosen to allow the current into the FB pin to reach the 30 μ A. the maximum I_{FB} control level. This will be met if the voltage at I_{FB} can reach 1V at no load conditions. To improve transient response R_{FB3} can be bypassed with C_{FB3} .

R_{FB4} can be used to set a nominal operating current of the optocoupler to improve the current transfer ratio and bandwidth of the optocoupler. For low standby power this operating current level should be kept small since it must be supplied from VDD operating voltage. The value of R_{FB4} is determined empirically due to the variable nature of the specific optocoupler chosen for the design. The ratio of R_{FB4} to R_{FB3} is typically in a range of 1/10 to 1/4 with typical value of R_{FB4} in 4 k Ω to 25 k Ω , and R_{FB3} in 25 k Ω to 200 k Ω . A good starting point is to select R_{FB4} around 4 k Ω and R_{FB3} around 30 k Ω for a design.

The shunt-regulator compensation network, Z_{FB} , is determined using well-established design techniques for control-loop stability. Typically, a Type-II compensation network is used. An effective approach is to set Z_{FB} to be a capacitor, $Z_{FB} = C_{FB}$ to form an integrator, and adding a bypass capacitor R_{FB3} will extend the frequency response of the optocoupler CTR.

Referring again to 图 18, the shunt-regulator (typically a TL431) current is at about 1 mA even when almost no optocoupler diode current flows. Since even a near-zero diode current establishes a forward voltage, R_{OPT} is selected to provide regulator bias current such as for TL431. The optocoupler input diode must be characterized by the designer to obtain the actual forward voltage versus forward current at the low currents expected. At the full-load condition of the converter, I_{FB} is around 0.5 μ A, I_{CE} may be around (0.4 V / R_{FB4}), and CTR at this level is about 10%, so the diode current typically falls in the range of 25 μ A to 100 μ A. Typical opto-diode forward voltage at this level is about 0.97 V which is applied across R_{OPT} . If R_{OPT} is set equal to 1 k Ω , this provides 970 μ A plus the diode current for I_{OPT} .

As output load decreases, the voltage across the shunt-regulator also decreases to increase the current through the optocoupler diode. This increases the diode forward voltage across R_{OPT} . CTR at no-load (when I_{CE} is higher) is generally a few percent higher than CTR at full-load (when I_{CE} is lower). At steady-state no-load condition, the shunt-regulator current is maximized and can be estimated by and 公式 31. I_{OPTNL} , plus the sum of the leakage currents of all the components on the output of the converter, constitute the total current required for use in to estimate secondary-side standby loss.

$$I_{OPTNL} = \frac{I_{CENL}}{CTR_{NL}} + \frac{V_{OPTNL}}{R_{OPT}} \quad (31)$$

The shunt-regulator voltage can decrease to a minimum, saturated level of about 2 V. To prevent excessive diode current, a series resistor, R_{TL} , is added to limit I_{OPT} to the maximum value necessary for regulation. 公式 32 provides an estimated initial value for R_{TL} , which may be adjusted for optimal limiting later during the prototype evaluation process.

$$R_{TL} = \frac{V_{OUTNL} - V_{OPTNL} - 2 \text{ V}}{I_{OPTNL}} \quad (32)$$

8.2.3 Application Curves

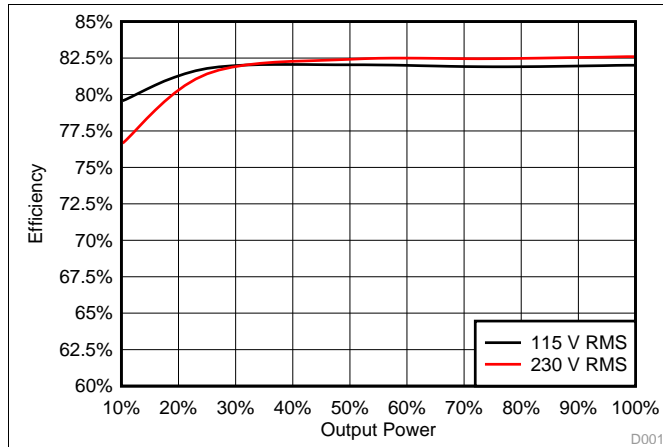


图 19. Efficiency

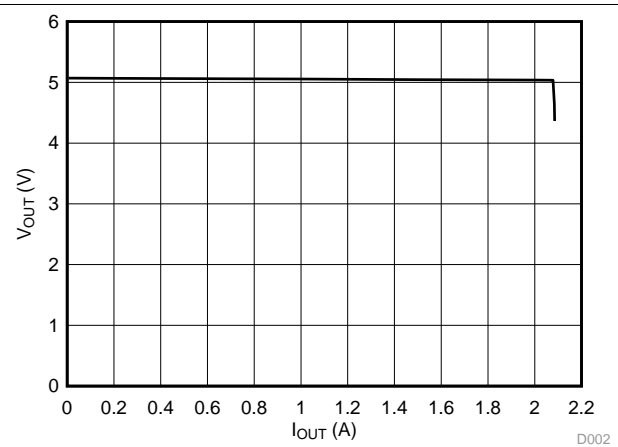


图 20. Output V-I Curves

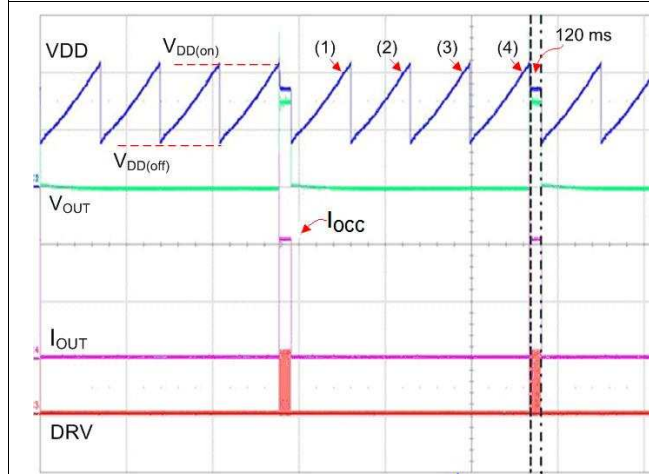


图 21. Constant Current Limit and Delayed Shutdown



图 22. Response to Load Step Changes

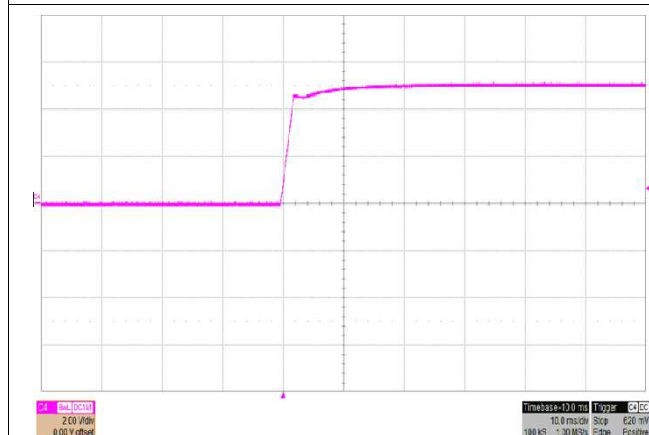


图 23. Typical V_{OUT} Start Up

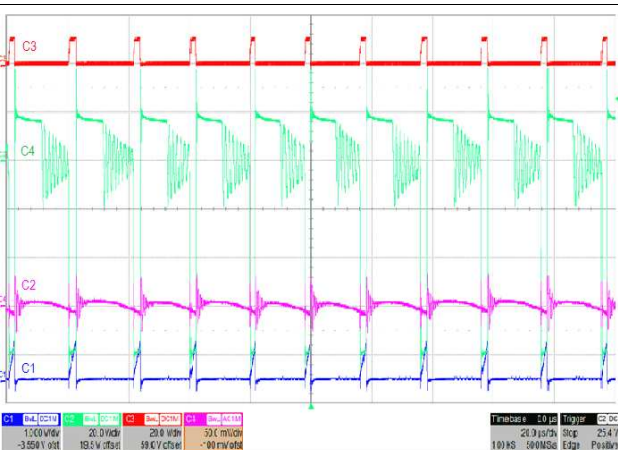


图 24. Switching Waveforms (C3 = DRV, C4 = V_{DS}, C2 = V_O Ripple, C1 = I_{pp})

8.3 Do's and Don'ts

- During no-load operation, do allow sufficient margin for variations in VDD level to avoid the UVLO shutdown threshold. Also, at no-load, keep the average switching frequency greater than $1.5 \times f_{SW(min)}$ typical to avoid a rise in output voltage. R_{LC} needs to be adjusted based on no-load operation accounting for both low-line and high-line operation..
- Do clean flux residue and contaminants from the PCB after assembly. Uncontrolled leakage current from VS to GND causes the output voltage to increase, while leakage current from VDD to VS can cause output voltage to increase.
- If ceramic capacitors are used for VDD, do use quality parts with X7R or X5R dielectric rated 50 V or higher to minimize reduction of capacitance due to DC-bias voltage and temperature variation.
- Do not use leaky components if low stand-by input power consumption is a design requirement.
- Do not probe the VS node with an ordinary oscilloscope probe; the probe capacitance can alter the signal and disrupt regulation.
- Do observe VS indirectly by probing the auxiliary winding voltage at R_{S1} and scaling the waveform by the VS divider ratio.
- Do follow [公式 27](#) to [公式 30](#) for C_{OUT} .

9 Power Supply Recommendations

The UCC28742 is intended for AC-to-DC adapters and chargers with universal input voltage range of 85 V_{RMS} to 265 V_{RMS}, 47 Hz to 63 Hz, using flyback topology. It can also be used in other applications and converter topologies with different input voltages. Be sure that all voltages and currents are within the recommended operating conditions and absolute maximum ratings of the device.

10 Layout

10.1 Layout Guidelines

In general, try to keep all high current loop areas as small as possible. Keep all traces with high current and high frequency away from other traces in the design. If necessary, high frequency/high current traces should be perpendicular to signal traces, not parallel to them. Shielding signal traces with ground traces can help reduce noise pick up. Always consider appropriate clearances between the high-voltage connections and any low-voltage nets.

In order to increase the reliability and feasibility of the project it is recommended to adhere to the following guidelines for PCB layout. 图 25 shows a typical 10-W, 5-V/2-A converter design schematics.

- Minimize stray capacitance on the VS node. Place the voltage sense resistors (R_{S1} and R_{S2} in) close to the VS pin.
- Arrange the components to minimize the loop areas of the switching currents as much as possible. These areas include such loops as the transformer primary winding current loop (a), the MOSFET gate-drive loop (b), the primary snubber loop (c), the auxiliary winding loop (d) and the secondary output current loop (e). In practice, trade-offs may have to be made. Loops with higher current should be minimized with higher priority. As a rule of thumb, the priority goes from high to low as (a) – (e) – (c) – (d) – (b).
- The R_{LC} resistor location is critical. To avoid any dv/dt induced noise (for example MOSFET drain dv/dt) coupled onto this resistor, it is better to place R_{LC} closer to the controller and avoid nearby the MOSFET.
- Using Kelvin connection for long distance connection such as for connection between optocoupler and FB pin.
- To improve thermal performance increase the copper area connected to GND pins.

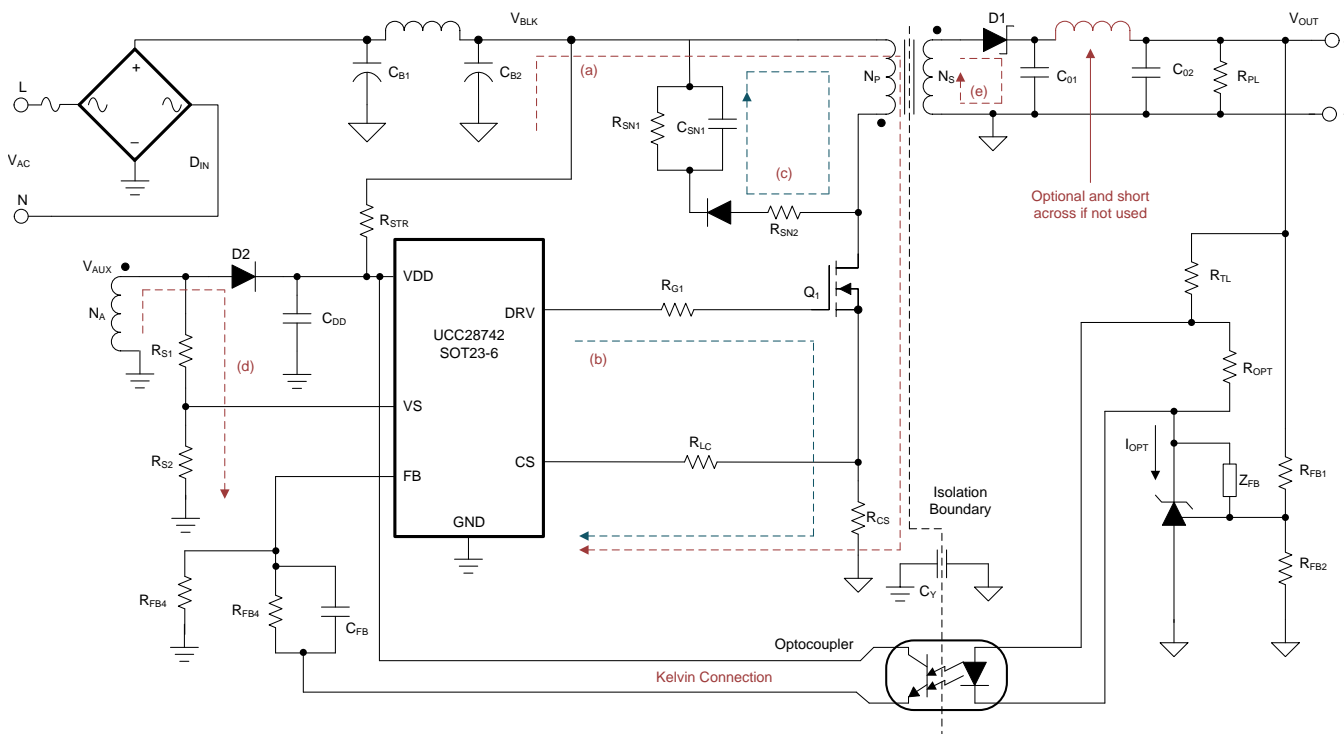


图 25. 10-W, 5-V/2-A Converter Schematics

10.2 Layout Example

图 26 demonstrates a layout of 10-W, 5-V/2-A converter with trade-offs to minimize the loops while effectively placing components and tracks for low noise operation on a single-layer printed circuit board. In addition to the consideration of minimal loops, one another layout guideline is always to use the device GND as reference point. This applies to both power and signal to return to the device GND pin (pin 5).

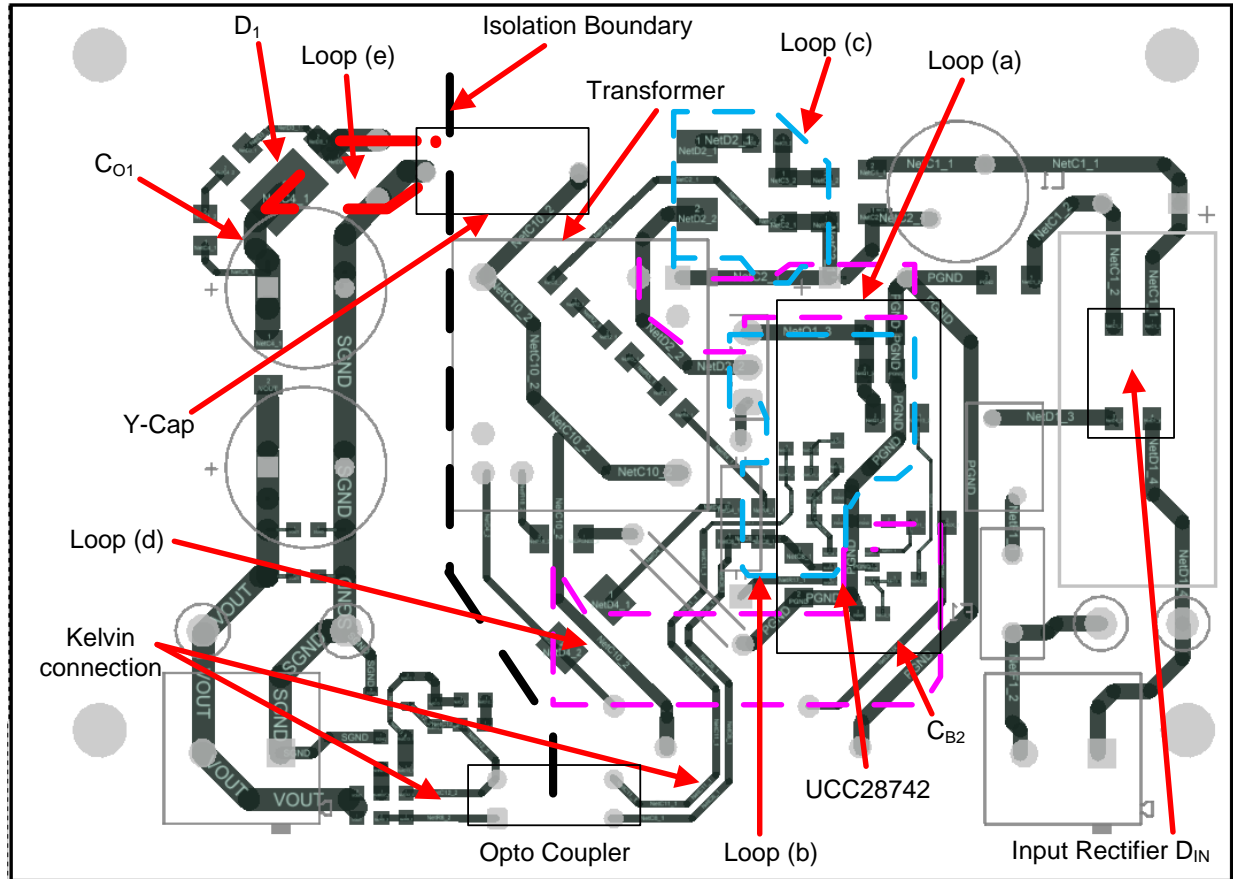


图 26. Layout Example

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 使用 **WEBENCH®** 工具创建定制设计

请单击[此处](#)，使用 UCC28742 器件并借助 WEBENCH® 电源设计器创建定制设计方案。

1. 首先输入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化该设计的关键参数，如效率、尺寸和成本。
3. 将生成的设计与德州仪器 (TI) 的其他可行的解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案以常用 CAD 格式导出
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com.cn/WEBENCH。

11.1.2 器件命名规则

11.1.2.1 电容术语（以法拉为单位）

C_{BULK} C_{B1} 和 C_{B2} 的总输入电容。

C_{DD} VDD 引脚所需的最小电容。

C_{OUT} 所需的最小输出电容。

11.1.2.2 占空比术语

D_{MAGCC} CC 中二次侧二极管导通占空比，0.475。

D_{MAX} 最大 MOSFET 导通时间占空比。

11.1.2.3 频率术语（以赫兹为单位）

f_{LINE} 最低线路频率。

f_{MAX} 转换器的最高目标满载开关频率。

f_{MIN} 转换器的最低开关频率，在器件 $f_{SW(min)}$ 限值基础上增加 15% 的裕度。

$f_{SW(lim)}$ 负载减小后的瞬态开关频率

$F_{SW(min)}$ 最低开关频率（见 [Electrical Characteristics](#) 表）

$f_{SW(max)}$ 最大开关频率（见 [Electrical Characteristics](#) 表）

$f_{SW(standby)}$ 轻负载条件下负载变化之前的开关频率

11.1.2.4 电流术语（以安培为单位）

I_{OCC} 转换器输出恒流目标。

I_{OR} 转换器额定输出电流。

$I_{PP(max)}$ 变压器一次侧最大电流。

I_{START} 启动偏置电源电流（见 [Electrical Characteristics](#) 表）。

I_{TRAN} 所需的正负载阶跃电流。

$I_{VSL(run)}$ VS 引脚运行电流（见 [Electrical Characteristics](#) 表）。

器件支持 (接下页)

I_{WAIT} 等待状态期间的 VDD 偏置电流。(见 [Electrical Characteristics](#) 表)。

11.1.2.5 电流和电压调节术语

K_{AM} 一次侧峰峰值电流比 (见 [Electrical Characteristics](#) 表)。

K_{Co} 稳定性因子为 100, 用于计算 C_{OUT} 。

K_{LC} 电流调节常量 (见 [Electrical Characteristics](#) 表)。

器件支持 (接下页)

11.1.2.6 变压器术语

L_P	变压器一次侧电感。
L_S	变压器二次侧电感。
N_{AS}	变压器辅助绕组与二次侧绕组匝数比。
N_{PA}	变压器一次侧绕组与辅助绕组匝数比。
N_{PS}	变压器一次侧绕组与二次侧绕组匝数比。
N_A	变压器辅助绕组的匝数。
N_P	变压器一次侧绕组的匝数。
N_S	变压器二次侧绕组的匝数。

11.1.2.7 功率术语 (以瓦特为单位)

P_{IN}	转换器最大输入功率。
P_{OUT}	转换器的满载输出功率。
P_{RSTR}	VDD 启动电阻功耗。
P_{SB}	总待机功耗。
P_{SB_CONV}	P_{SB} 与启动电阻和缓冲器功耗的差值。

11.1.2.8 电阻术语 (以 Ω 为单位)

R_{CS}	一次侧电流编程电阻
R_{ESR}	输出电容的总 ESR。
R_{PL}	转换器输出端的预载电阻。
R_{S1}	高侧 VS 引脚电阻。
R_{S2}	低侧 VS 引脚电阻。
R_{STR}	高电压与 VDD 之间连接的启动电阻

11.1.2.9 时序术语 (以秒为单位)

t_D	电流感测延迟。
$t_{DMAG(min)}$	二次侧整流器最短导通时间。
t_{GATE_OFF}	一次侧主 MOSFET 关断时间。
$t_{ON(min)}$	MOSFET 最短导通时间。
t_R	t_{DMAG} 之后的谐振环周期。
t_{STR}	由于 VDD 电容 C_{DD} 需要充电时间所造成的上电延时。
t_{ZTO}	tZTO: 未检测到过零点时 VS 引脚上的过零点超时延迟 (见 Electrical Characteristics 表)

器件支持 (接下页)

11.1.2.10 电压术语 (以伏特为单位)

V_{BLK} 或 **V_{BULK}** Bulk 电容器电压。

V_{BULK(max)} 用于待机功耗测量的 Bulk 电容器最高电压。

V_{BULK(min)} 满功率条件下 **C_{B1}** 和 **C_{B2}** 的最低电压。

V_{BULK(run)} 转换器启动 (运行) 高电压。

V_{CBC} 满载时电路板端输出的电缆补偿电压。

V_{CCR} 恒流调节电压 (见 [Electrical Characteristics](#) 表)。

V_{CCUV} 恒流输出电压关断的 VS 阈值 (见 [Electrical Characteristics](#) 表)。

V_{CST(max)} CS 引脚的最大电流感测阈值 (见 [Electrical Characteristics](#) 表)。

V_{CST(min)} CS 引脚的最小电流感测阈值 (见 [Electrical Characteristics](#) 表)。

V_{DD(off)} 或 **V_{VDD(off)}** UVLO 关断电压 (见 [Electrical Characteristics](#) 表)。

V_{VDD(on)} 或 **V_{DD(on)}** UVLO 导通电压 (见 [Electrical Characteristics](#) 表)。

V_F 电流接近零时的二次侧整流器正向压降。

V_{FA} 辅助整流器正向压降。

V_{LK} 估计的漏感能量复位电压。

V_{OCV} 经稳压的转换器输出电压。

V_{OCC} 恒流稳压条件下的最低目标转换器输出电压。

V_{OVL} 当输出电流达到其限值 **I_{OCC}** 时, 输出电压会达到 **V_{OVL}**; **V_{OVL}** 取决于 **I_{OCC}** 和 **I_{OCC}** 下的预期最低负载电阻 **R_{LOAD}**, 也就是说 **V_{OVL} = I_{OCC} × R_{LOAD}**。

V_{RIPPLE} 满载条件下的输出峰峰值纹波电压。

V_{VSR} VS 输入端的 CV 调节电平 (见 [Electrical Characteristics](#) 表)。

11.1.2.11 交流电压术语 (以 **V_{RMS}** 为单位)

V_{IN(max)} 转换器的最大输入电压。

V_{IN(min)} 转换器的最小输入电压。

V_{IN(run)} 转换器输入启动 (运行) 电压。

11.1.2.12 效率术语

η 转换器总体效率。

η₁₀ 10% 负载时的效率。

η_{AVG} 25%、50%、75% 和 100% 负载时的算术平均效率。

η_{XFMR} 变压器一次侧与二次侧之间的功率传输效率。

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档:

- 《UCC28742-1EVM-724 评估模块的用法》, [SLUUBF1](#)
- 《UCC28742 设计计算器》, [SLUC652](#)

11.3 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](http://ti.com.cn) 上的器件产品文件夹。单击右上角的通知我 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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11.6 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 术语表

SLYZ022 — TI 术语表。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC28742DBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U742
UCC28742DBVR.A	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U742
UCC28742DBVR.B	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U742
UCC28742DBVT	Active	Production	SOT-23 (DBV) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U742
UCC28742DBVT.A	Active	Production	SOT-23 (DBV) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U742
UCC28742DBVT.B	Active	Production	SOT-23 (DBV) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U742

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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DBV0006A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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