UCC28070 和 UCC28070A 扩展频率范围（10kHz 至 300kHz）交错式连续导通模式 PFC 控制器

1 特性

- 具有固有电流匹配的交错平均电流模式 PWM 控制
- 先进的电流合成器电流检测可实现卓越的效率
- 同步外部时钟功能
- 具有内部量化电压前馈的高线性乘法器输出，用于近单位 PF
- 通过电压放大器输出电流的压摆率校正增强了瞬态响应
- 扩展范围的可编程频率
  - UCC28070A：10kHz 至 300kHz
  - UCC28070：30kHz 至 300kHz
- 可编程最大占空比钳位
- 可编程频率抖动速率和幅度（最高 30kHz）可降低 EMI
- 可编程软启动
- 可编程峰值电流限制
- 外部 PFC 禁用接口
- 保护：偏置电源 UVLO、输出过压、开-环路检测、VSENSE 和 VINAC 上的开路检测，以及 PFC 使能监控

2 应用

- IGBT、Si 或 GaN 电源开关的 PFC
- 空调和大家电
- 电力输送、电信和服务器电源
- 电视、台式机和专业音频
- 电动汽车充电基础设施

3 说明

UCC28070A 和 UCC28070 是高级功率因数校正 (PFC) 控制器，每款控制器都集成了两个在 CCM 升压模式下由 180° 交错运行的脉宽调制器 (PWM)。这两款器件都可以在高达 300kHz 的频率下进行开关，而对于大功率应用中基于 IGBT 功率开关的 PFC 转换器，UCC28070A 器件能够在低至 10kHz 的频率下运行。UCC28070 器件的最小运行频率限制为 30kHz。

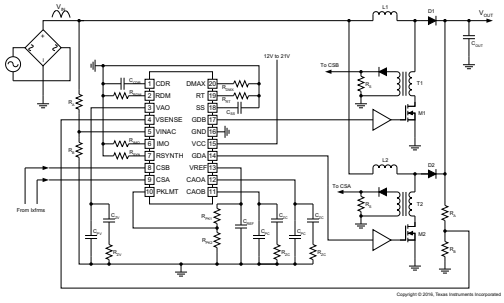
180° 异相交错运行方式可以显著减少输入和输出纹波电流，与此同时，传导 EMI 滤波变得更简单，成本也更低。UCC28070A 和 UCC28070 器件的所有其他特性和优势相同。

两款器件都具有多项创新功能，包括电流合成和量化电压前馈，以促进 PF、效率、THD 和瞬态响应方面的性能增强。此外，频率抖动、时钟同步和压摆率增强进一步扩大性能增强的潜力。此外，保护功能还包括输出过压检测、可编程峰值电流限制、欠压锁定和开-环路保护。

封装信息

器件型号	封装(1)	封装尺寸(2)
UCC28070A	PW（TSSOP，20）	6.50mm × 4.40mm
UCC28070		
UCC28070	DW（SOIC，20）	12.80mm × 7.50mm

(1) 有关所有可用封装，请参阅机械、封装和可订购信息。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



简化版应用示意图

本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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4 Pin Configuration and Functions

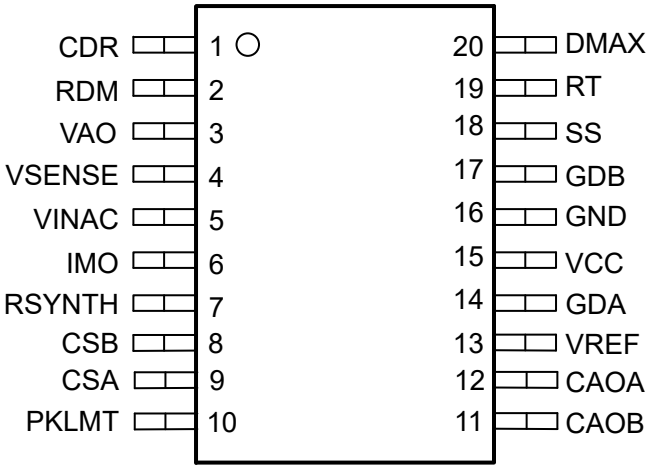


图 4-1. PW Package, 20-Pin TSSOP (Top View) and DW Package, 20-Pin Wide-SOIC

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表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	CDR	I	Dither rate capacitor. Frequency-dithering timing pin. An external capacitor to GND programs the rate of oscillator dither. To disable dithering, connect the CDR pin to the VREF pin and connect the RDM pin to GND.
2	RDM (SYNC)	I	Dither magnitude resistor. Frequency-dithering magnitude and external synchronization pin. An external resistor to GND programs the magnitude of oscillator-frequency dither. When frequency dithering is disabled (CDR > 5V), the internal master clock synchronizes to rising edges presented on the RDM pin. Connect RDM to GND with a zero-ohm resistance when dithering is disabled and synchronization is not used.
3	VAO	O	Voltage amplifier output. Output of transconductance voltage error amplifier. Internally connected to the multiplier input and the zero-power comparator. Connect the voltage regulation loop compensation components between this pin and GND.
4	VSENSE	I	Output voltage sense. Internally connected to the inverting input of the transconductance voltage error amplifier in addition to the positive terminal of the current synthesis difference amplifier. Also connected to the OVP, PFC enable, and slew-rate comparators. Connect to PFC output with a resistor-divider network.
5	VINAC	I	Scaled AC line input voltage. Internally connected to the multiplier and negative terminal of the current synthesis difference amplifier. Connect a resistor-divider network between V_{IN}, VINAC, and GND identical to the PFC output divider network connected at VSENSE.
6	IMO	O	Multiplier output current. Connect a resistor between this pin and GND to set the multiplier gain.
7	RSYNTH	I	Current synthesis down-slope programming. Connect a resistor between this pin and GND to set the rate of the current synthesizer down-slope. Connecting RSYNTH to VREF disables current synthesis and internally connects CSA and CSB directly to their respective current amplifiers.
8	CSB	I	Phase-B current sense input. During the ON-time of GDB, CSB is internally connected to the inverting input of phase-B current amplifier through the current synthesis stage, unless RSYNTH is connected to VREF.
9	CSA	I	Phase-A current sense input. During the ON-time of GDA, CSA is internally connected to the inverting input of phase-A current amplifier through the current synthesis stage, unless RSYNTH is connected to VREF.
10	PKLMT	I	Peak current limit programming. Connect a resistor-divider network between VREF and this pin to set the voltage threshold of the cycle-by-cycle peak current limiting comparators. Allows adjustment for desired ΔI_{LB}.
11	CAOB	O	Phase-B current amplifier output. Output of phase-B transconductance current amplifier. Internally connected to the inverting input of phase-B PWM comparator for trailing-edge modulation. Connect the current regulation loop compensation components between this pin and GND.
12	CAOA	O	Phase-A current amplifier output. Output of phase-A transconductance current amplifier. Internally connected to the inverting input of phase-A PWM comparator for trailing-edge modulation. Connect the current regulation loop compensation components between this pin and GND.
13	VREF	O	6V reference voltage and internal bias voltage. Connect a 0.1 µF ceramic bypass capacitor as close as possible to this pin and GND.
14	GDA	O	Phase-A gate drive. This limited-current output is intended to connect to a separate gate-drive device suitable for driving the phase-A switching components. The output voltage is typically clamped to 13.5V.
15	VCC	I	Bias voltage input. Connect a 0.1 µF ceramic bypass capacitor as close as possible to this pin and GND.
16	GND	I/O	Device ground reference. Connect all compensation and programming resistor and capacitor networks to this pin. Connect this pin to the system through a separate trace for high-current noise isolation.
17	GDB	O	Phase-B gate drive. This limited-current output is intended to connect to a separate gate-drive device suitable for driving the phase-B switching component(s). The output voltage is typically clamped to 13.5V.
18	SS	I	Soft-start and external fault interface. Connect a capacitor to GND on this pin to set the soft-start slew rate based on an internally-fixed, 10 µA current source. The regulation reference voltage for VSENSE is clamped to V_{SS} until V_{SS} exceeds 3V. Upon recovery from certain fault conditions, a 1mA current source is present at the SS pin until the SS voltage equals the VSENSE voltage. Pulling the SS pin below 0.6V immediately disables both GDA and GDB outputs.
19	RT	I	Timing resistor. Oscillator frequency programming pin. A resistor to GND sets the running frequency of the internal oscillator.
20	DMAX	I	Maximum duty-cycle resistor. Maximum PWM duty-cycle programming pin. A resistor to GND sets the PWM maximum duty-cycle based on the ratio of R_{DMX} / R_{RT}.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2) (3) (4)

		MIN	MAX	UNIT
Supply voltage	VCC		22	V
Supply current, I_{VCC}			20	mA
Gate drive current – continuous	GDA, GDB		±0.25	A
Gate drive current – pulsed	GDA, GDB		±0.75	A
Voltage	GDA, GDB	–0.5	V_{CC} + 0.3	V
	DMAX, RDM, RT, CDR, VINAC, VSENSE, SS, VAO, IMO, CSA, CSB, CAOA, CAOB, PKLMT, VREF	–0.5	7	
Current	RT, DMAX, RDM, RSYNTH		–0.5	mA
	VREF, VAO, CAOA, CAOB, IMO		10	
Lead temperature (10 seconds)			260	°C
Operating junction temperature, T_J		–40	125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under 节 5.3. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.
(3) All currents are positive into the terminal, negative out of the terminal.
(4) In normal use, terminals GDA and GDB are connected to an external gate driver and are internally limited in output current.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
	Input voltage (from a low-impedance source) to VCC	V_{UVLO} + 1	21	V
	Load current on VREF		2	mA
	Input voltage to VINAC	0	3	V
	Voltage on IMO	0	3.3	V
	Voltage on CSA, CSB, PKLMT	0	3.6	V
R_{SYN}	RSYNTH resistance	15	750	kΩ
R_{RDM}	RDM resistance	30	330	kΩ

5.4 Thermal Information

THERMAL METRIC(1)		UCC28070	UCC28070A UCC28070	UNIT
		DW (Wide-SOIC)	PW (TSSOP)	
		20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	78.1	99.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.5	34.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46	50.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.5	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.5	50.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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5.5 Electrical Characteristics

$T_J = T_A =$ –40°C to 125°C, V_{CC} = 12V, GND = 0V, R_{RT} = 75kΩ, R_{DMX} = 68.1kΩ, $R_{RDM} = R_{SYN}$ = 100kΩ, C_{CDR} = 2.2nF, $C_{SS} = C_{VREF}$ = 0.1 µF, C_{VCC} = 1 µF, I_{VREF} = 0mA (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS SUPPLY							
$V_{CC(SHUNT)}$	V_{CC} shunt voltage(1)		I_{VCC} = 10mA	23	25	27	V
I_{VCC}	Supply current	Disabled	V_{VSENSE} = 0V		7		mA
		Enabled	V_{VSENSE} = 3V (switching)		9	12	
		UVLO	V_{CC} = 7V			200	µA
			V_{CC} = 9V		4	6	mA
V_{UVLO}	UVLO turnon threshold		Measured at VCC (rising)	9.8	10.2	10.6	V
	UVLO hysteresis		Measured at VCC (falling)		1		
	VREF enable threshold		Measured at VCC (rising)	7.5	8	8.5	V
LINEAR REGULATOR							
V_{VREF}	Reference voltage	No load	I_{VREF} = 0mA	5.82	6	6.18	V
		Load rejection	Measured as the change in V_{VREF} (I_{VREF} = 0mA and –2mA)	–12		12	mV
		Line rejection	Measured as the change in V_{VREF} (V_{CC} = 11V and 20V, I_{VREF} = 0 µA)	–12		12	
PFC ENABLE							
V_{EN}	Enable threshold		Measured at VSENSE (rising)	0.65	0.75	0.85	V
	Enable hysteresis				0.15		
EXTERNAL PFC DISABLE							
	Disable threshold		Measured at SS (falling)	0.5	0.6		V
	Hysteresis		V_{VSENSE} > 0.85V		0.15		V
OSCILLATOR							
	Output phase shift		Measured between GDA and GDB	179	180	181	°
V_{DMAX}, V_{RT}, V_{RDM}	Timing regulation voltages		Measured at DMAX, RT, and RDM	2.91	3	3.09	V
f_{PWM}	PWM switching frequency, UCC28070A only		R_{RT} = 750kΩ, R_{DMX} = 681kΩ, V_{RDM} = 0V, V_{CDR} = 6V	9.75	10.25	10.75	kHz
	PWM switching frequency, UCC28070A and UCC28070		R_{RT} = 75kΩ, R_{DMX} = 68.1kΩ, V_{RDM} = 0V, V_{CDR} = 6V	95	100	105	
			R_{RT} = 24.9kΩ, R_{DMX} = 22.6kΩ, V_{RDM} = 0V, V_{CDR} = 6V	270	290	330	
D_{MAX}	Duty-cycle clamp		R_{RT} = 75kΩ, R_{DMX} = 68.1kΩ, V_{RDM} = 0V, V_{CDR} = 6V	92%	95%	98%	
	Minimum programmable OFF-time		R_{RT} = 24.9kΩ, R_{DMX} = 22.6kΩ, V_{RDM} = 0V, V_{CDR} = 6V	50	150	250	ns
f_{DM}	Frequency dithering magnitude change in f_{PWM}		R_{RDM} = 316kΩ, R_{RT} = 75kΩ	2	3	4	kHz
			R_{RDM} = 31.6kΩ, R_{RT} = 24.9kΩ	24	30	36	
f_{DR}	Frequency dithering rate of change in f_{PWM}		R_{RDM} = 100kΩ, C_{CDR} = 2.2nF		3		kHz
			R_{RDM} = 100kΩ, C_{CDR} = 0.3nF		20		
I_{CDR}	Dither rate current		Measured at CDR (sink and source)		±10		µA
	Dither disable threshold		Measured at CDR (rising)		5	5.25	V

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5.5 Electrical Characteristics（续）

$T_J = T_A =$ –40°C to 125°C, V_{CC} = 12V, GND = 0V, R_{RT} = 75kΩ, R_{DMX} = 68.1kΩ, $R_{RDM} = R_{SYN}$ = 100kΩ, C_{CDR} = 2.2nF, $C_{SS} = C_{VREF}$ = 0.1 μF, C_{VCC} = 1 μF, I_{VREF} = 0mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLOCK SYNCHRONIZATION						
V_{CDR}	SYNC enable threshold	Measured at CDR (rising)		5	5.25	V
	SYNC propagation delay	V_{CDR} = 6V, measured from RDM (rising) to GDx (rising)		50	100	ns
	SYNC threshold (rising)	V_{CDR} = 6V, measured at RDM		1.2	1.5	V
	SYNC threshold (falling)	V_{CDR} = 6V, measured at RDM	0.4	0.7		V
t_{SYNC}	SYNC pulse width, minimum	Positive pulse	0.2			μs
	Maximum SYNC pulse duty cycle(2)			50%		
VOLTAGE AMPLIFIER						
	VSENSE voltage	In regulation, T_A = 25°C	2.97	3	3.03	V
	VSENSE voltage	In regulation	2.94	3	3.06	V
	VSENSE input bias current	In regulation		250	500	nA
	VAO high voltage	V_{VSENSE} = 2.9V	4.8	5	5.2	V
	VAO low voltage	V_{VSENSE} = 3.1V		0.05	0.5	V
g_{MV}	VAO transconductance	V_{VSENSE} = 2.8V to 3.2V, V_{VAO} = 3V		70		μS
	VAO sink current, overdriven limit	V_{VSENSE} = 3.5V, V_{VAO} = 3V		30		μA
	VAO source current, overdriven	V_{VSENSE} = 2.5V, V_{VAO} = 3V, SS = 3V		–30		μA
	VAO source current, overdriven limit + I_{SRC}	V_{VSENSE} = 2.5V, V_{VAO} = 3V		–130		μA
	Slew-rate correction threshold	Measured as V_{VSENSE} (falling) / V_{VSENSE} (regulation)	92%	93%	95%	
	Slew-rate correction hysteresis	Measured at VSENSE (rising)		3	9	mV
I_{SRC}	Slew-rate correction current	Measured at VAO, in addition to VAO source current		–100		μA
	Slew-rate correction enable threshold	Measured at SS (rising)		4		V
	VAO discharge current	V_{VSENSE} = 0.5V, V_{VAO} = 1V		10		μA
SOFT START						
I_{SS}	SS source current	V_{VSENSE} = 0.9V, V_{SS} = 1V		–10		μA
	Adaptive source current	V_{VSENSE} = 2V, V_{SS} = 1V		–1.5	–2.5	mA
	Adaptive SS disable	Measured as $V_{VSENSE} - V_{SS}$	–30	0	30	mV
	SS sink current	V_{VSENSE} = 0.5V, V_{SS} = 0.2V	0.5	0.9		mA
OVERVOLTAGE						
V_{OVP}	OVP threshold	Measured as V_{VSENSE} (rising) / V_{VSENSE} (regulation)	104%	106%	108%	
	OVP hysteresis	Measured at VSENSE (falling)		100		mV
	OVP propagation delay	Measured between VSENSE (rising) and GDx (falling)		0.2	0.3	μs

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5.5 Electrical Characteristics（续）

$T_J = T_A =$ –40°C to 125°C, V_{CC} = 12V, GND = 0V, R_{RT} = 75kΩ, R_{DMX} = 68.1kΩ, $R_{RDM} = R_{SYN}$ = 100kΩ, C_{CDR} = 2.2nF, $C_{SS} = C_{VREF}$ = 0.1 μF, C_{VCC} = 1 μF, I_{VREF} = 0mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ZERO-POWER						
V_{ZPWR}	Zero-power detect threshold	Measured at VAO (falling)	0.65	0.75		V
	Zero-power hysteresis			0.15		V
MULTIPLIER						
k_{MULT}	Gain constant	$V_{VAO} \geqslant$ 1.5V, T_A = 25°C	16	17	18	μA
		V_{VAO} = 1.2V, T_A = 25°C	14.5	17	19.5	
		$V_{VAO} \geqslant$ 1.5V	15	17	19	
		V_{VAO} = 1.2V	13	17	21	
I_{IMO}	Output current: zero	$V_{VINAC} = 0.9V_{PK}$, V_{VAO} = 0.8V	–0.2	0	0.2	μA
		V_{VINAC} = 0V, V_{VAO} = 5V	–0.2	0	0.2	
QUANTIZED VOLTAGE FEEDFORWARD						
V_{LVL1}	Level 1 threshold(3)	Measured at VINAC (rising)	0.6	0.7	0.8	V
V_{LVL2}	Level 2 threshold	Measured at VINAC (rising)		1.0		V
V_{LVL3}	Level 3 threshold	Measured at VINAC (rising)		1.2		V
V_{LVL4}	Level 4 threshold	Measured at VINAC (rising)		1.4		V
V_{LVL5}	Level 5 threshold	Measured at VINAC (rising)		1.65		V
V_{LVL6}	Level 6 threshold	Measured at VINAC (rising)		1.95		V
V_{LVL7}	Level 7 threshold	Measured at VINAC (rising)		2.25		V
V_{LVL8}	Level 8 threshold	Measured at VINAC (rising)		2.6		V
CURRENT AMPLIFIERS						
	CAOx high voltage		5.75	6		V
	CAOx low voltage				0.1	V
g_{MC}	CAOx transconductance			100		μS
	CAOx sink current, overdriven			50		μA
	CAOx source current, overdriven			–50		μA
	Input common mode range		0		3.6	V
	Input offset voltage	V_{RSYNTH} = 6V, T_A = 25°C	–4	–8	–13	mV
		V_{RSYNTH} = 6V	0	–8	–20	
	Input offset voltage		0	–8	–20	mV
	Phase mismatch	Measured as phase A input offset minus phase B input offset	–12	0	12	mV
	CAOx pulldown current	V_{VSENSE} = 0.5V, V_{CAOx} = 0.2V	0.5	0.9		mA
CURRENT SYNTHESIZER						
V_{RSYNTH}	Regulation voltage	V_{VSENSE} = 3V, V_{VINAC} = 0V	2.91	3	3.09	V
		V_{VSENSE} = 3V, V_{VINAC} = 2.85V	0.1	0.15	0.2	
	Synthesizer disable threshold	Measured at RSYNTH (rising)		5	5.25	V
	VINAC input bias current			0.25	0.5	μA

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5.5 Electrical Characteristics（续）

$T_J = T_A$ = –40°C to 125°C, V_{CC} = 12V, GND = 0V, R_{RT} = 75kΩ, R_{DMX} = 68.1kΩ, $R_{RDM} = R_{SYN}$ = 100kΩ, C_{CDR} = 2.2nF, $C_{SS} = C_{VREF}$ = 0.1 μF, C_{VCC} = 1 μF, I_{VREF} = 0mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PEAK CURRENT LIMIT						
	Peak current limit threshold	V_{PKLMT} = 3.3V, measured at CSx (rising)	3.27	3.3	3.33	V
	Peak current limit propagation delay	Measured between CSx (rising) and GDx (falling) edges		60	100	ns
PWM RAMP						
V_{RMP}	PWM ramp amplitude		3.8	4	4.2	V
	PWM ramp offset voltage	T_A = 25°C, R_{RT} = 75kΩ	0.65	0.7		V
	PWM ramp offset temperature coefficient			–2		mV/°C
GATE DRIVE						
	GDA, GDB output voltage, high, clamped	V_{CC} = 20V, C_{LOAD} = 1nF	11.5	13	15	V
	GDA, GDB output voltage, high	C_{LOAD} = 1nF	10	10.5		V
	GDA, GDB output voltage, low	C_{LOAD} = 1nF		0.2	0.3	V
	Rise time GDx	1V to 9V, C_{LOAD} = 1nF		18	30	ns
	Fall time GDx	9V to 1V, C_{LOAD} = 1nF		12	25	ns
	GDA, GDB output voltage, UVLO	V_{CC} = 0V, I_{GDA}, I_{GDB} = 2.5mA		0.7	2	V
THERMAL SHUTDOWN						
	Thermal shutdown threshold			160		°C
	Thermal shutdown recovery			140		°C

(1) Excessive VCC input voltage or current damages the device. The VCC clamp does not protect the device from an unregulated bias supply. If an unregulated supply is used, TI recommends a series-connected fixed positive-voltage regulator such as a UA78L15A. See 节 5.1 for the limits on VCC voltage and current.

(2) Due to the influence of the synchronization pulse-width on the programmability of the maximum PWM switching duty-cycle (D_{MAX}), TI recommends to minimize the duty-cycle of the synchronization signal.

(3) The Level 1 threshold represents the *zero-crossing* detection threshold above which VINAC must rise to initiate a new input half-cycle, and below which VINAC must fall to terminate that half-cycle.

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5.6 Typical Characteristics

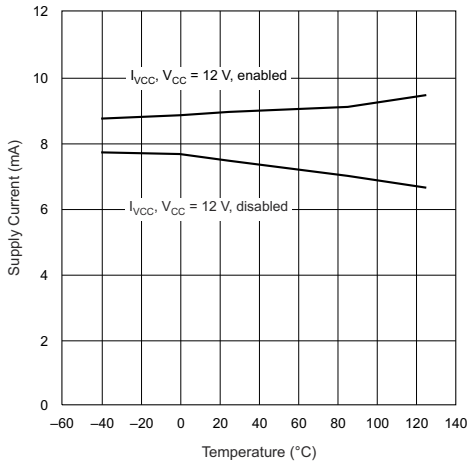
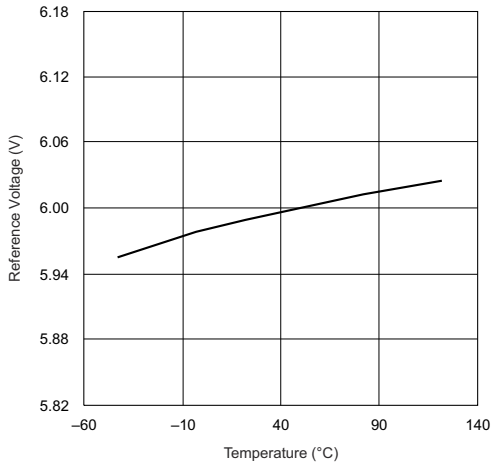


图 5-1. VCC Supply Current vs Junction Temperature



I_{VREF} = 0mA

图 5-2. V_{VREF} vs Junction Temperature

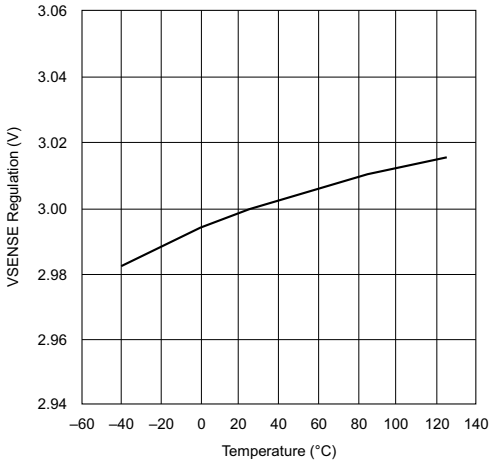


图 5-3. V_{VSENSE} Regulation vs Junction Temperature

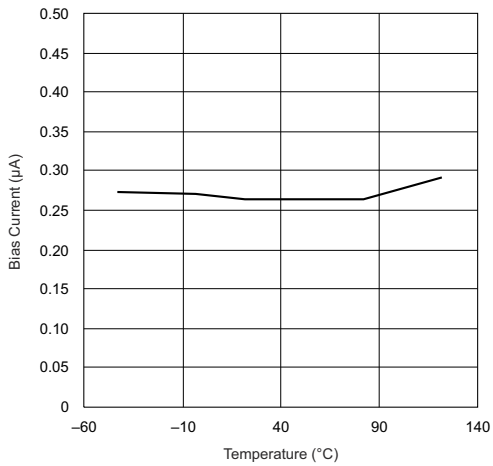


图 5-4. I_{VSENSE} Bias Current vs Junction Temperature

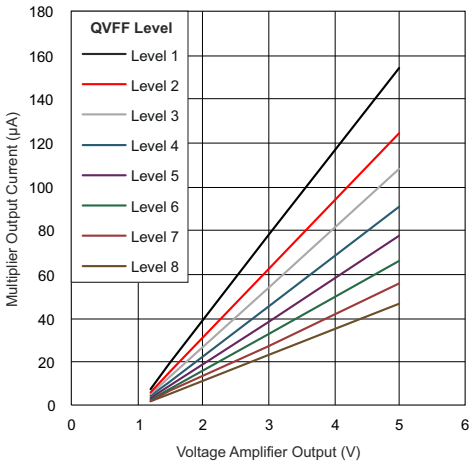


图 5-5. IMO, Multiplier Output Current vs V_{VAO}

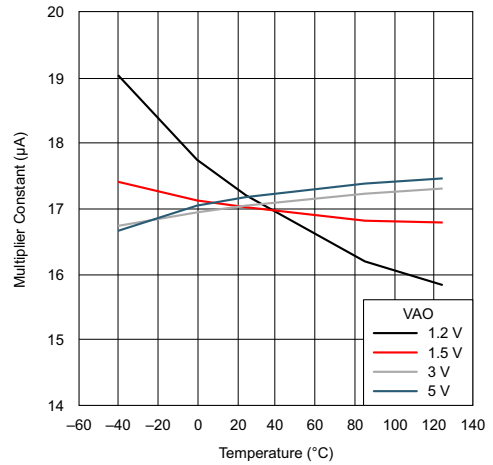


图 5-6. Multiplier Constant vs Junction Temperature

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5.6 Typical Characteristics (continued)

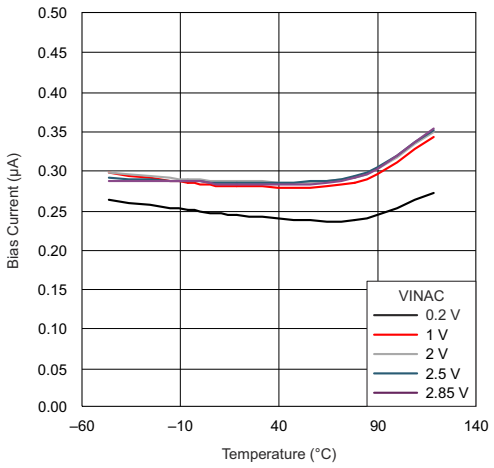


图 5-7. I_{VINAC} Bias Current vs Junction Temperature

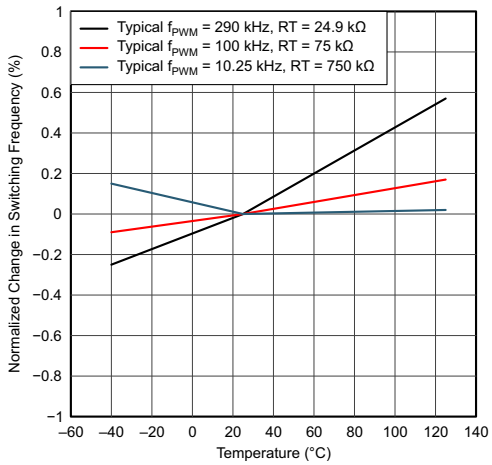


图 5-8. Switching Frequency vs Temperature

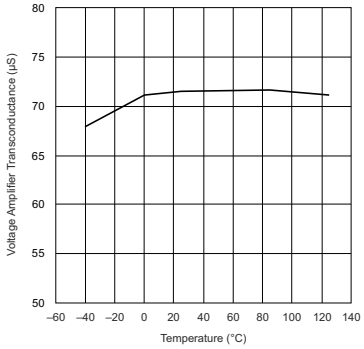


图 5-9. VAO, Voltage Amplifier Transconductance vs Junction Temperature

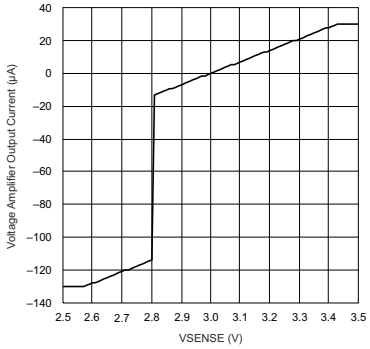


图 5-10. Voltage Amplifier Transfer Function vs V_{VSENSE}

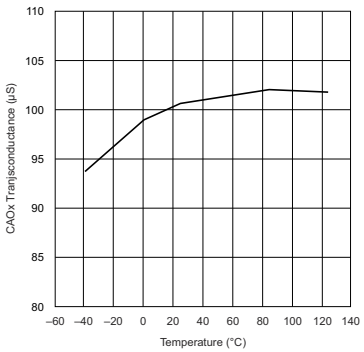
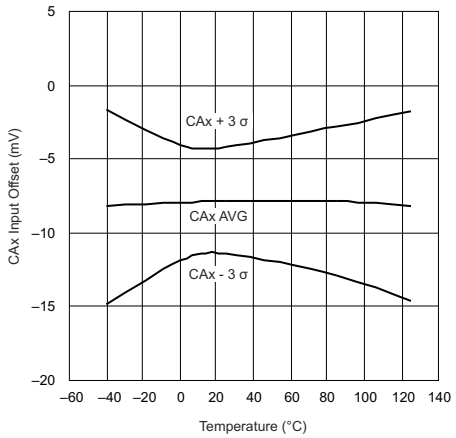


图 5-11. Current Amplifier Transconductance vs Junction Temperature

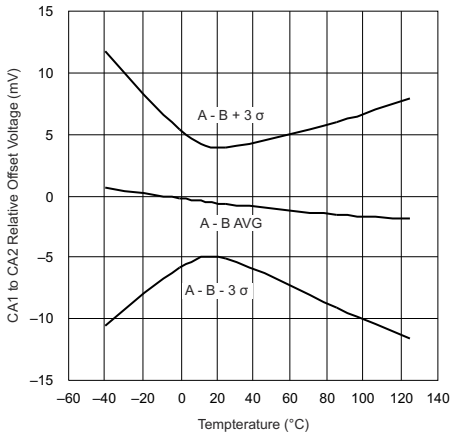
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5.6 Typical Characteristics (continued)



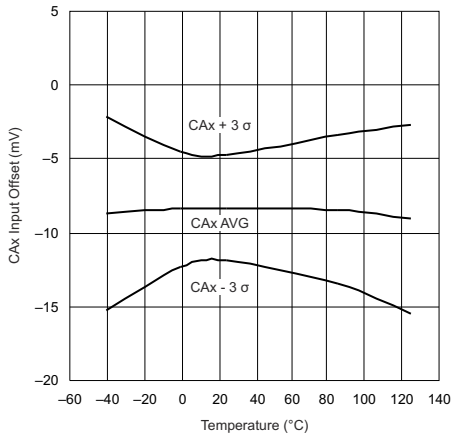
0.8V Common Mode

图 5-12. CAx Input Offset Voltage vs Junction Temperature



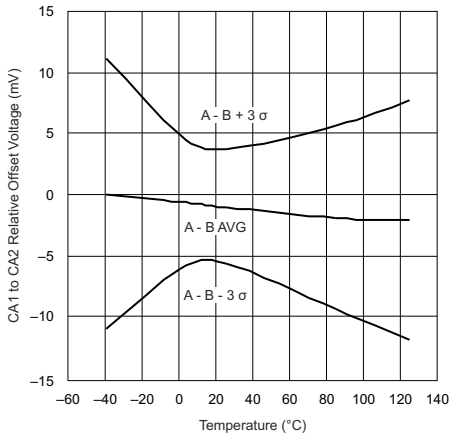
0.8V Common Mode

图 5-13. CA1 to CA2 Relative Offset vs Junction Temperature



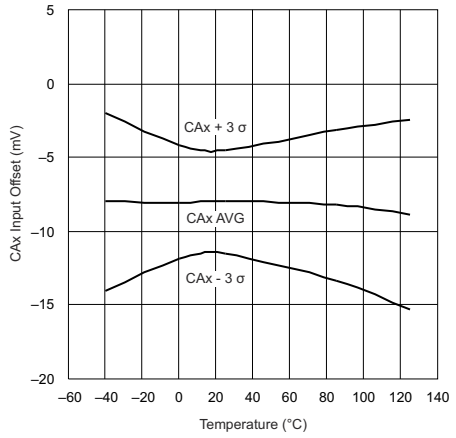
2V Common Mode

图 5-14. CAx Input Offset Voltage vs Junction Temperature



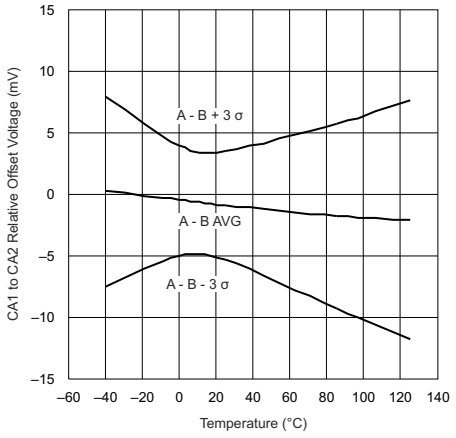
2V Common Mode

图 5-15. CA1 to CA2 Relative Offset vs Junction Temperature



3.6V Common Mode

图 5-16. CAx Input Offset Voltage vs Junction Temperature



3.6V Common Mode

图 5-17. CA1 to CA2 Relative Offset vs Junction Temperature

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6 Detailed Description

6.1 Overview

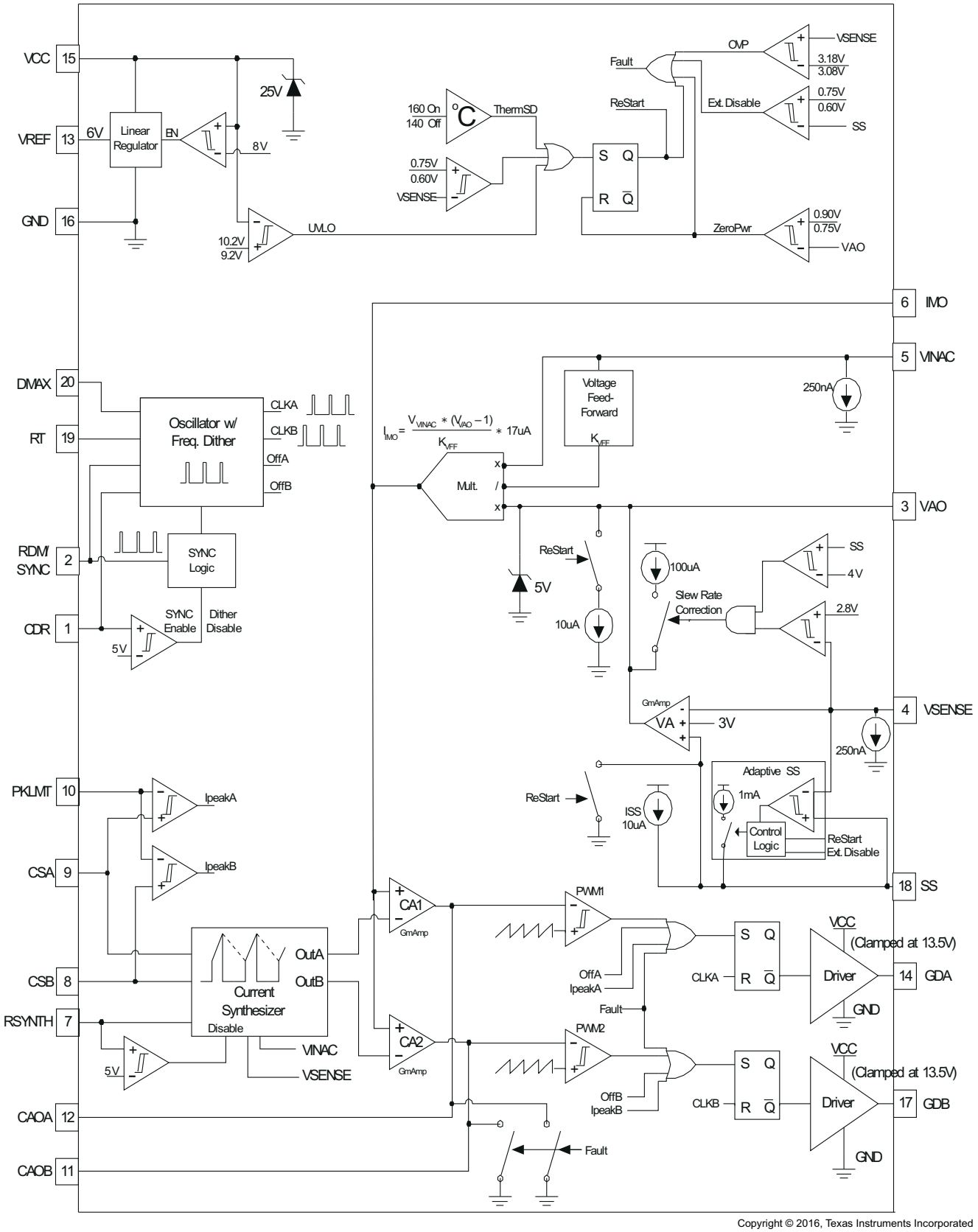
The UCC28070 and the UCC28070A are power factor correction ICs each of which controls two CCM (Continuous Conduction Mode) Boost PFC power stages operating 180° out of phase with each other. This interleaving action reduces the input and output ripple currents so that less EMI filtering is needed and allows operation at higher power levels than a non-interleaved solution.

Except for their respective switching frequency ranges, the UCC28070 and the UCC28070A are interchangeable devices that can operate over a wide range of frequencies, making them suitable for use with both MOSFET and IGBT power switches. The UCC28070A is capable of operating down to 10kHz minimum switching frequency, while the UCC28070 is limited to 30kHz minimum switching frequency.

Except as noted, all references to UCC28070A apply equally to the UCC28070 throughout this document. This device is especially suited to high-performance, high-power, PFC applications where the use of Average Current Mode PWM control gives low THDi. Multiple controllers can be synchronized for use in higher-power applications where more than two interleaved power stages are needed.

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6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 Interleaving

One of the main benefits from the 180° interleaving of phases is significant reductions in the high-frequency ripple components of both the input current and the current into the output capacitor of the PFC preregulator. Compared to that of a single-phase PFC stage of equal power, the reduced ripple on the input current eases the burden of filtering conducted-EMI noise and helps reduce the EMI filter and C_{IN} sizes. Additionally, reduced high-frequency ripple current into the PFC output capacitor, C_{OUT}, helps to reduce its size and cost. Furthermore, with reduced ripple and average current in each phase, the boost inductor size can be smaller than in a single-phase design [3].

Ripple current reduction due to interleaving is often referred to as ripple cancellation, but strictly speaking, the peak-to-peak ripple is completely cancelled only at 50% duty-cycle in a 2-phase system. At duty-cycles other than 50%, ripple reduction occurs in the form of partial cancellation due to the superposition of the individual phase currents. Nevertheless, compared to the ripple currents of an equivalent single-phase PFC preregulator, those of a 2-phase interleaved design are extraordinarily smaller [3]. Independent of ripple cancellation, the frequency of the interleaved ripple current, at both the input and output, is 2 × f_{PWM}.

At the PFC input, 180° interleaving reduces the peak-to-peak current-ripple amplitude to ½ or less of the ripple amplitude of the equivalent single-phase current.

At the PFC output, 180° interleaving reduces the rms value of the PFC-generated ripple current in the output capacitor by a factor of slightly more than $\sqrt{2}$, for PWM duty-cycles > 50%.

This can be seen in the following derivations, adapting the method by Erickson [4].

In a single-phase PFC preregulator, the total rms output-capacitor current contributed by the PFC stage at all duty-cycles can be shown to be approximated by:

$$i_{CRMS1\varphi} = \left(\frac{I_O}{\eta}\right)\sqrt{\left(\left(\frac{16 \times V_O}{3\pi \times V_M}\right) - \eta^2\right)} \quad (1)$$

where

- I_O is the average PFC output load current
- V_O is the average PFC output voltage
- V_M is the peak of the input AC-line voltage
- η is the efficiency of the PFC stage at these conditions

In a dual-phase interleaved PFC preregulator, the total rms output-capacitor current contributed by the PFC stage for D > 50% can be shown to be approximated by:

$$i_{CRMS2\varphi} = \left(\frac{I_O}{\eta}\right)\sqrt{\left(\left(\frac{16 \times V_O}{6\pi \times V_M}\right) - \eta^2\right)} \quad (2)$$

It can be seen that the quantity under the radical for $i_{CRMS2\phi}$ is slightly smaller than ½ of that under the radical for $i_{CRMS1\phi}$. The rms currents shown contain both the low-frequency and the high-frequency components of the PFC output current. Interleaving reduces the high-frequency component, but not the low-frequency component.

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6.3.2 Programming the PWM Frequency and Maximum Duty-Cycle Clamp

The PWM frequency and maximum duty-cycle limit for GDA and GDB outputs of the UCC28070A are programmed through the selection of the resistors connected to the RT and DMAX pins, respectively. The selection of the RT resistor (R_{RT}) directly sets the PWM frequency (f_{PWM}).

$$R_{RT}(k\Omega) = \frac{7500}{f_{PWM}(kHz)}, \text{ therefore } f_{PWM}(kHz) = \frac{7500}{R_{RT}(k\Omega)} \quad (3)$$

Once R_{RT} has been determined, the D_{MAX} resistor (R_{DMX}) may be derived.

$$R_{DMX}(k\Omega) = R_{RT}(k\Omega) \times (2 \times D_{MAX} - 1), \text{ therefore } D_{MAX} = \frac{1}{2}\left(\frac{R_{DMX}(k\Omega)}{R_{RT}(k\Omega)} + 1\right) \quad (4)$$

where

- D_{MAX} is the desired maximum PWM duty-cycle (D_{MAX} *must* be > 0.50)

6.3.3 Frequency Dithering (Magnitude and Rate)

Frequency dithering refers to modulating the switching frequency to achieve a reduction in conducted-EMI noise beyond the capability of the line filter alone. The UCC28070A implements a triangular modulation method which results in equal time spent at every point along the switching frequency range. This total range from minimum to maximum frequency is defined as the dither magnitude, and is centered around the nominal switching frequency f_{PWM} set with R_{RT}. For example, a dither magnitude of 20kHz on a nominal f_{PWM} of 100kHz results in a frequency range of 100kHz ±10kHz. Furthermore, the programmed duty-cycle clamp set by R_{DMX} remains constant at the programmed value across the entire range of the frequency dithering.

The rate at which f_{PWM} traverses from one extreme to the other and back again is defined as the dither rate. For example, a dither rate of 1kHz would linearly modulate the nominal frequency from 110kHz to 90kHz to 110kHz once every millisecond. A good initial design target for dither magnitude is ±10% of f_{PWM}. Most boost components can tolerate such a spread in f_{PWM}. The designer can then iterate around there to find the best compromise between EMI reduction, component tolerances, and loop stability.

The desired dither magnitude is set by a resistor from the RDM pin to GND, of value calculated with 方程式 5:

$$R_{RDM}(k\Omega) = \frac{937.5}{f_{DM}(kHz)} \quad (5)$$

Once the value of R_{RDM} is determined, the desired dither rate may be set by a capacitor from the CDR pin to GND, of value calculated with 方程式 6:

$$C_{CDR}(pF) = 66.7 \times \left(\frac{R_{RDM}(k\Omega)}{f_{DR}(kHz)}\right) \quad (6)$$

Frequency dithering may be fully disabled by forcing the CDR pin > 5V or by connecting it to VREF (6V) and connecting the RDM pin directly to GND. (If populated, the relatively high impedance of the RDM resistor may allow system switching noise to couple in and interfere with the controller timing functions if not bypassed with a low impedance path when dithering is disabled.)

If an external frequency source is used to synchronize f_{PWM} and frequency dithering is desired, the external frequency source must provide the dither magnitude and rate functions as the internal dither circuitry is disabled to prevent undesired performance during synchronization. (See *External Clock Synchronization* for more details.)

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6.3.4 External Clock Synchronization

The UCC28070A has also been designed to be easily synchronized to almost any external frequency source. By disabling frequency dithering (pulling CDR > 5V), the SYNC circuitry is enabled permitting the internal oscillator to be synchronized with pulses presented on the RDM pin. To ensure that a precise 180° phase shift is maintained between the GDA and GDB outputs, the frequency (f_{SYNC}) of the pulses presented at the RDM pin must be at twice the desired f_{PWM}. For example, if a PWM switching frequency of 100kHz is desired, the f_{SYNC} must be 200kHz.

$$f_{PWM} = \frac{f_{SYNC}}{2}, \text{ therefore } f_{SYNC} = 2 \times f_{PWM} \quad (7)$$

To ensure the internal oscillator does not interfere with the SYNC function, R_{RT} must be sized to set the internal oscillator frequency about 10% below the minimum expected f_{SYNC}.

$$R_{RT}\,(k\Omega) = \frac{15000}{f_{SYNC}\,(kHz)} \times 1.1 \quad (8)$$

It must be noted that the PWM modulator gain is reduced by a factor equivalent to the scaled R_{RT} due to a direct correlation between the PWM ramp current and R_{RT}. Adjustments to the current-loop gains must be made accordingly, using the k_{SYNC} factor as indicated in Current Loop Compensation.

It must also be noted that the maximum duty-cycle clamp programmability is affected during external synchronization. The internal timing circuitry responsible for setting the maximum duty cycle is initiated on the falling edge of the synchronization pulse. Therefore, the selection of R_{DMX} becomes dependent on the synchronization pulse width (t_{SYNC}). In this context, t_{SYNC} is a pulse width; t_{SYNC} is *not* the inverse of f_{SYNC}.

$$D_{SYNC} = t_{SYNC} \times f_{SYNC} \text{ (For use in } R_{DMX} \text{ equation immediately below.)} \quad (9)$$

$$R_{DMX}\,(k\Omega) = \left(\frac{15000}{f_{SYNC}\,(kHz)}\right) \times \left(2 \times D_{MAX} - 1 - D_{SYNC}\right) \quad (10)$$

Consequently to minimize the impact of the t_{SYNC} it is clearly advantageous to use the smallest synchronization pulse width feasible (see *Electrical Characteristics Table* for minimum allowable pulse width).

备注

When external synchronization is used, a propagation delay of approximately 50ns to 100ns exists between internal timing circuits and the falling edge of the SYNC signal, which may result in reduced OFF-time at the highest of switching frequencies. Therefore, at high SYNC frequencies R_{DMX} value must be adjusted downward slightly by (t_{SYNC} – 0.1 µs) / t_{SYNC} to compensate. At lower SYNC frequencies, this delay becomes an insignificant fraction of the PWM period, and can be neglected.

备注

The oscillator in the UCC28070A device is not designed to accommodate wide variations in the external SYNC frequency. Do not allow the SYNC frequency variation to exceed ±10% of the nominal f_{SYNC} as used in 方程式 8. Excessive variation of f_{SYNC} can cause malfunction of the controller to occur. R_{RT} value must be calculated at the lowest f_{SYNC}.

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6.3.5 Multi-phase Operation

External synchronization also facilitates using more than 2 phases for interleaving. Multiple UCC28070A devices can easily be paralleled to add an even number of additional phases for higher-power applications. With appropriate phase-shifting of the synchronization signals, even more input and output ripple current cancellation can be obtained. (An odd number of phases can be accommodated if desired, but the ripple cancellation would not be optimal.) For 4-, 6-, or any 2 × n-phases (where n = the number of UCC28070A controllers), each controller must receive a SYNC signal which is 360/n degrees out of phase with each other.

For a 4-phase application interleaving with two controllers, SYNC1 must be 180° out of phase with SYNC2 for optimal ripple cancellation. Similarly for a 6-phase system, SYNC1, SYNC2, and SYNC3 must be 120° out of phase with each other for optimal ripple cancellation.

In a multi-phase interleaved system, each current loop is independent and treated separately; however, there is only one common voltage loop. To maintain a single voltage control loop, all VSENSE, VINAC, SS, IMO, and VAO signals are paralleled, respectively, between the n controllers. Where current-source outputs are combined (SS, IMO, VAO), the calculated load impedances must be adjusted by 1/n to maintain the same performance as with a single controller.

图 6-1 illustrates the paralleling of two controllers for a 4-phase, 90-degree-interleaved PFC system.

6.3.6 VSENSE and VINAC Resistor Configuration

The primary purpose of the VSENSE input is to provide the voltage feedback from the output to the voltage control loop. Thus, a traditional resistor-divider network must be sized and connected between the output capacitor and the VSENSE pin to set the desired output voltage based on the 3V regulation voltage on VSENSE.

A unique aspect of the UCC28070A is the need to place the same resistor-divider network on the V_{IN} side of the inductor to the VINAC pin. This provides the scaled input voltage monitoring needed for the linear multiplier and current synthesizer circuitry. It is not required that the actual resistance of the VINAC network be identical to the VSENSE network, but it is necessary that the attenuation (k_R) of the two divider networks be equivalent for proper PFC operation.

$$k_R = \frac{R_B}{(R_A + R_B)} \tag{11}$$

In noisy environments, it may be beneficial for small filter capacitors to be applied to the VSENSE and VINAC inputs to avoid the destabilizing effects of excessive noise on these inputs. If applied, the RC time-constant must not exceed 100 µs on the VSENSE input to avoid significant delay in the output transient response. The RC time-constant must also not exceed 100 µs on the VINAC input to avoid degrading of the wave-shape zero-crossings. Usually, a time constant of 3 / f_{PWM} is adequate to filter out typical noise on VSENSE and VINAC. Some design and test iteration may be required to find the optimal amount of filtering required in a particular application.

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6.3.7 VSENSE and VINAC Open-Circuit Protection

Both the VSENSE and VINAC pins have been designed with an internal 250nA current sink to ensure that in the event of an open circuit at either pin, the voltage is not left undefined, and the UCC28070A remains in a safe operating mode.

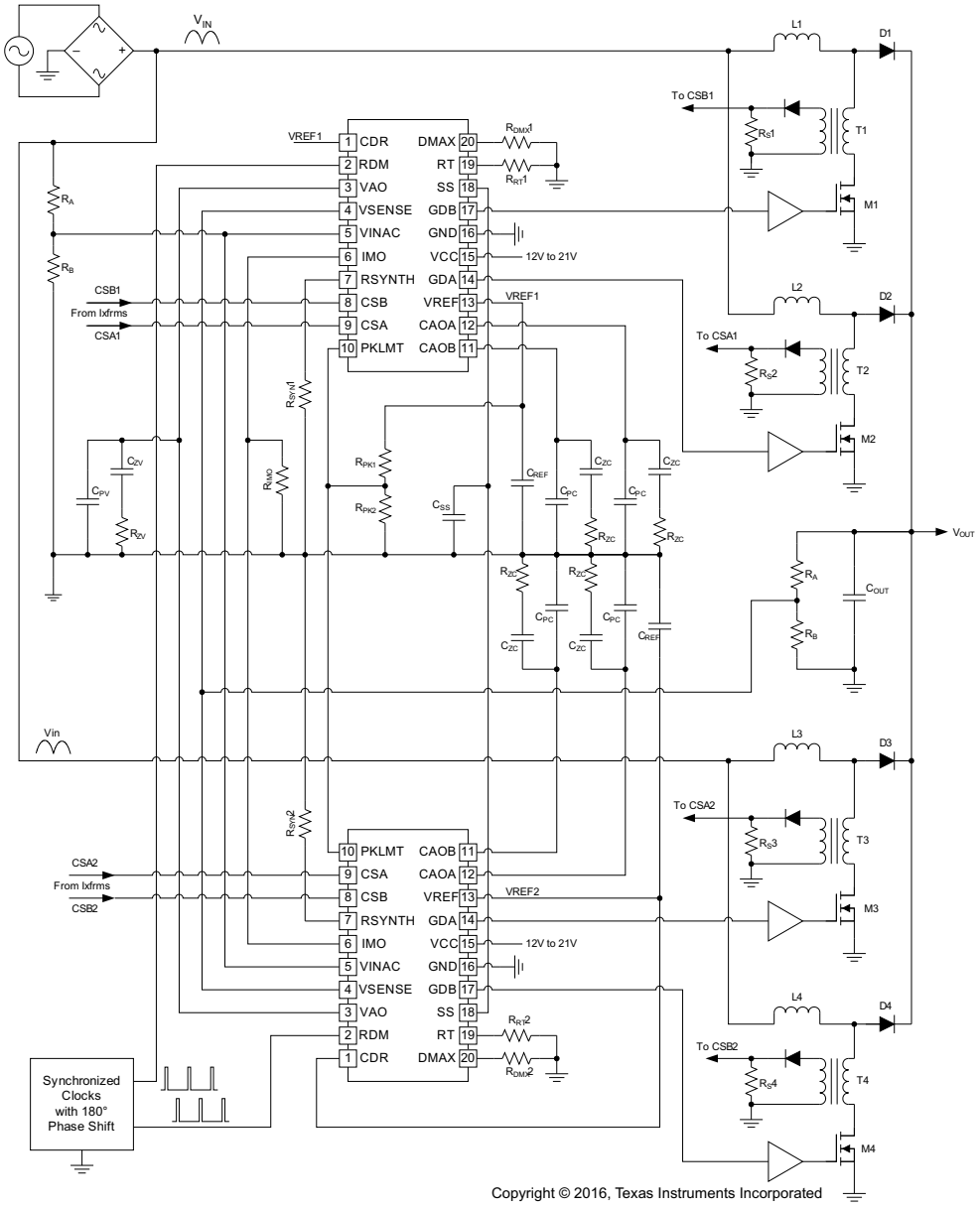


图 6-1. Simplified Four-Phase Application Diagram Using Two UCC28070A Devices

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6.3.8 Current Synthesizer

One of the most prominent innovations in the UCC28070A design is the current synthesizer circuitry that synchronously monitors the instantaneous inductor current through a combination of ON-time sampling and OFF-time down-slope emulation.

During the ON-time of the GDA and GDB outputs, the inductor current is recorded at the CSA and CSB pins, respectively, through the current transformer network in each output phase. Meanwhile, the continuous monitoring of the input and output voltages through the VINAC and VSENSE pins permits the UCC28070A to internally recreate the down-slope of the inductor current during the respective OFF-time of each output. Through the selection of the RSYNTH resistor (R_{SYN}), based on 方程式 12, the internal response may be adjusted to accommodate the wide range of inductances expected across the wide array of applications.

During inrush surge events at power up and AC drop-out recovery, V_{VSENSE} < V_{VINAC}, the synthesized downslope becomes zero. In this case, the synthesized inductor current remains above the IMO reference and the current loop drives the duty cycle to zero. This avoids excessive stress on the MOSFETs during the surge event. Once V_{VINAC} falls below V_{VSENSE}, the duty cycle increases until steady-state operation resumes.

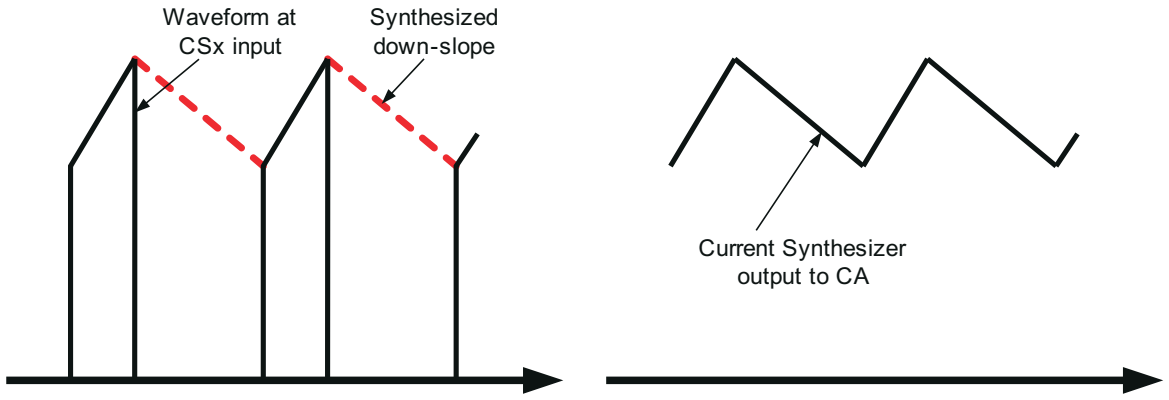


图 6-2. Downslope of the Inductor Current

$$R_{SYN}\left(k\Omega\right)=\frac{\left(10\times N_{CT}\times L_{B}\left(\mu H\right)\times k_{R}\right)}{R_{S}\left(\Omega\right)} \quad (12)$$

where:

- L_B = Nominal Zero-Bias Boost Inductance (μ H)
- R_S = Sense Resistor (Ω)
- N_{CT} = Current-sense Transformer turns ratio
- k_R = R_B / (R_A + R_B) = the resistor-divider attenuation at the VSENSE and VINAC pins

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6.3.9 Programmable Peak Current Limit

The UCC28070A has been designed with a programmable cycle-by-cycle peak current limit dedicated to disabling either the GDA or GDB output whenever the corresponding current-sense input (CSA or CSB, respectively) rises above the voltage established on the PKLMT pin. Once an output has been disabled through the detection of peak current limit, the output remains disabled until the next clock cycle initiates a new PWM period. The programming range of the PKLMT voltage extends to 4V to permit the full use of the 3V average current-sense signal range; however, note that the linearity of the current amplifiers begins to compress above 3.6V.

A resistor-divider network from VREF to GND programs the peak current limit voltage on PKLMT, provided that the total current out of VREF is less than 2mA to avoid drooping of the 6V VREF voltage. TI recommends a load of less than 0.5mA, but if the resistance on PKLMT is very high, TI recommends a small filter capacitor on PKLMT to avoid operational problems in high-noise environments.

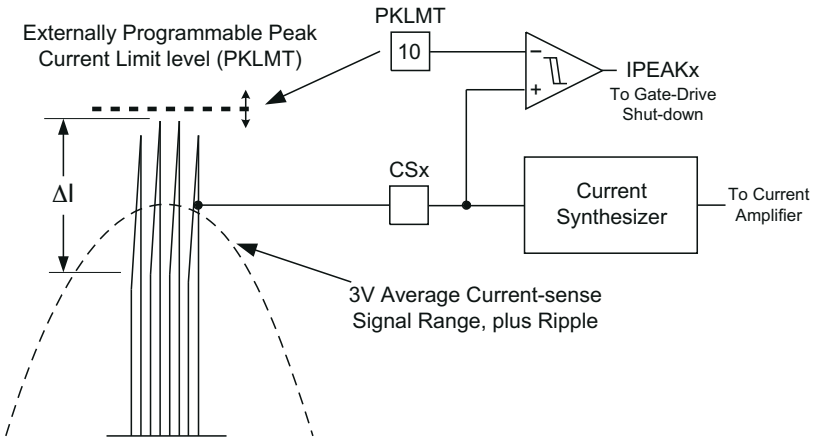


图 6-3. Externally Programmable Peak Current Limit

Peak Current Limit is a protection feature and has no built-in slope-compensation for duty-cycles greater than 0.5. During occurrences of peak limiting, sub-harmonic oscillation will occur with possible audible noise from such oscillation. If the PKLMT feature is re-purposed to implement a steady-state power-limit function, suitable slope compensation should be added by external means.

6.3.10 Linear Multiplier and Quantized Voltage Feed Forward

The UCC28070A multiplier generates a reference current which represents the desired wave shape and proportional amplitude of the AC input current. This current is converted to a reference voltage signal by the R_{IMO} resistor which is scaled in value to match the low-frequency average voltage of the current-sense signals. The instantaneous multiplier current is dependent upon the rectified, scaled input voltage V_{VINAC} and the voltage-error amplifier output V_{VAO}. V_{VINAC} conveys three pieces of information to the multiplier:

- The overall wave-shape of the input voltage (typically sinusoidal).
- The instantaneous input voltage magnitude at any point in the line cycle.
- The rms level of the input voltage (inferred from the peak of the assumed sinusoid).

Maximum V_{VAO} represents the total output power of the PFC preregulator.

A major innovation in the UCC28070A multiplier architecture is the internal quantized V_{RMS} feed-forward (Q_{VFF}) circuitry, which eliminates the requirement for external filtering of the VINAC signal and the subsequent slow response to transient line variations. A unique circuit algorithm detects the transition of the peak of V_{VINAC} through seven thresholds and generates an equivalent VFF level centered within the 8-Q_{VFF} ranges. The boundaries of the ranges expand with increasing V_{IN} to maintain an approximately equal-percentage delta between levels. These 8-Q_{VFF} levels are spaced to accommodate the full universal line range of 85V_{RMS} to 265V_{RMS}.

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A great benefit of the Q_{VFF} architecture is that the constant k_{VFF} factors eliminate any contribution to distortion of the multiplier output, unlike an externally-filtered VINAC signal ripple which unavoidably contains 2nd-harmonic distortion components. Furthermore, the Q_{VFF} algorithm allows for rapid response to both increasing and decreasing changes in input rms voltage so that disturbances transmitted to the PFC output are minimized. 5% hysteresis in the level thresholds help avoid chattering between Q_{VFF} levels for V_{VINAC} voltage peaks near a particular threshold or containing mild ringing or distortion.

The Q_{VFF} architecture requires that the input voltage be largely sinusoidal, and relies on detecting zero-crossings to adjust Q_{VFF} downward on decreasing input voltage. Zero-crossings are defined as V_{VINAC} falling below 0.7V for at least 50 μs, typically. For hysteresis in changing levels, falling threshold voltages are 95% of rising threshold voltages.

表 6-1 shows the relationship between the various V_{VINAC} peak voltages and the corresponding k_{VFF} terms for the multiplier equation.

表 6-1. V_{VINAC} Peak Voltages and Q_{VFF} Levels

LEVEL(1)	V_{VINAC} PEAK VOLTAGE (RISING PEAKS)	V_{VINAC} PEAK VOLTAGE (FALLING PEAKS)	k_{VFF} (V^2)	V_{IN} PEAK VOLTAGE(2)
8	2.6V ≤ $V_{VINAC(pk)}$	2.47V < $V_{VINAC(pk)}$	3.857	>345V
7	2.25V ≤ $V_{VINAC(pk)}$ < 2.6V	2.138V < $V_{VINAC(pk)}$ ≤ 2.47V	2.922	300V to 345V
6	1.95V ≤ $V_{VINAC(pk)}$ < 2.25V	1.853V < $V_{VINAC(pk)}$ ≤ 2.138V	2.199	260V to 300V
5	1.65V ≤ $V_{VINAC(pk)}$ < 1.95V	1.568V < $V_{VINAC(pk)}$ ≤ 1.853V	1.604	220V to 260V
4	1.4V ≤ $V_{VINAC(pk)}$ < 1.65V	1.33V < $V_{VINAC(pk)}$ ≤ 1.568V	1.156	187V to 220V
3	1.2V ≤ $V_{VINAC(pk)}$ < 1.4V	1.14V < $V_{VINAC(pk)}$ ≤ 1.33V	0.839	160V to 187V
2	1V ≤ $V_{VINAC(pk)}$ < 1.2V	0.95V < $V_{VINAC(pk)}$ ≤ 1.14V	0.600	133V to 160V
1	$V_{VINAC(pk)}$ < 1V	$V_{VINAC(pk)}$ ≤ 0.95V	0.398	<133V

(1) The controller always defaults to Level 8 at start-up, so zero-crossings are necessary to detect lower Levels if $V_{VINAC(pk)}$ < 2.47V. Zero-crossings are detected each AC half-cycle when V_{VINAC} falls below 0.7V for at least 50 μs.

(2) The V_{IN} peak voltage boundary values listed above are calculated based on a PFC output voltage of 400V and the use of a matched resistor-divider network (k_R = 3V / 400V = 0.0075) on VINAC and VSENSE (as required for current synthesis). When V_{OUT} is designed to be higher or lower than 400V, k_R = 3V / V_{OUT}, and the V_{IN} peak voltage boundary values for each Q_{VFF} level adjust to $V_{VINAC(pk)}$ / k_R.

The multiplier output current I_{IMO} for any line and load condition can thus be determined using 方程式 13:

$$I_{IMO} = \frac{17\ \mu A \times (V_{VINAC}) \times (V_{VAO} - 1)}{k_{VFF}} \quad (13)$$

Because the k_{VFF} value represents the scaled $(V_{RMS})^2$ at the center of a level, V_{VAO} adjusts slightly upwards or downwards when $V_{VINAC(pk)}$ is either lower or higher than the center of the Q_{VFF} voltage range to compensate for the difference. This is automatically accomplished by the voltage loop control when V_{IN} varies, both within a level and after a transition between levels.

The output of the voltage-error amplifier (V_{VAO}) is clamped at 5V, which represents the maximum PFC output power. This value is used to calculate the maximum reference current at the IMO pin, and sets a limit for the maximum input power allowed (and, as a consequence, limits maximum output power).

Unlike a continuous V_{FF} situation, where maximum input power is a fixed power at any V_{RMS} input, the discrete Q_{VFF} levels permit a variation in maximum input power within limited boundaries as the input V_{RMS} varies within each level.

The lowest maximum power limit occurs at the V_{VINAC} voltage of 0.76V, while the highest maximum power limit occurs at the increasing threshold from level-1 to level-2. This pattern repeats at every level transition threshold, considering that decreasing thresholds are 95% of the increasing threshold values. Below V_{VINAC} = 0.76V, P_{IN} is always less than $P_{IN(max)}$, falling linearly to zero with decreasing input voltage.

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For example, to design for the lowest maximum power allowable, determine the maximum steady-state (average) output power required of the PFC preregulator and add some additional percentage to account for line drop-out recovery power (to recharge C_{OUT} while full load power is drawn) such as 10% or 20% of $P_{OUT(max)}$. Then apply the expected efficiency factor to find the lowest maximum input power allowable:

$$P_{IN(max)} = 1.1 \times P_{OUT(max)} / \eta \quad (14)$$

At the $P_{IN(max)}$ design threshold, V_{VINAC} = 0.76V, hence Q_{VFF} = 0.398 and input V_{AC} = 73V_{RMS} (accounting for 2V bridge-rectifier drop) for a nominal 400V output system.

$$I_{IN(rms)} = P_{IN(max)} / 73V_{RMS} \quad (15)$$

$$I_{IN(pk)} = 1.414 \times I_{IN(rms)} \quad (16)$$

This $I_{IN(pk)}$ value represents the combined average current through the boost inductors at the peak of the line voltage. Each inductor current is detected and scaled by a current-sense transformer (CT). Assuming equal currents through each interleaved phase, the signal voltage at each current-sense input pin (CSA and CSB) is developed across a sense resistor selected to generate approximately 3V based on ½ $I_{IN(pk)}$ × R_S / N_{CT}, where R_S is the current-sense resistor and N_{CT} is the CT turns-ratio.

I_{IMO} is then calculated at that same lowest maximum-power point, as:

$$I_{IMO(max)} = 17\ \mu A \times \frac{(0.76\ V)(5\ V - 1\ V)}{0.398} = 130\ \mu A \quad (17)$$

R_{IMO} is selected such that:

$$I_{IMO(max)} \times R_{IMO} = \left(\frac{\frac{1}{2} \times I_{IN(pk)}}{N_{CT}} \right) \times R_S \quad (18)$$

Therefore:

$$R_{IMO} = \left(\frac{\frac{1}{2} \times I_{IN(pk)} \times R_S}{N_{CT}} \right) / I_{IMO(max)} \quad (19)$$

At the increasing side of the level-1 to level-2 threshold, note that the IMO current would allow higher input currents at low-line:

$$I_{IMO(L1–L2)} = 17\ \mu A \times \frac{(1\ V)(5\ V - 1\ V)}{0.398} = 171\ \mu A \quad (20)$$

However, this current may easily be limited by the programmable peak current limiting (PKLMT) feature of the UCC28070A if required by the power stage design.

The same procedure can be used to find the lowest and highest input power limits at each of the Q_{VFF} level transition thresholds. At higher line voltages, where the average current with inductor ripple is traditionally below the PKLMT threshold, the full variation of maximum input power is seen, but the input currents are inherently below the maximum acceptable current levels of the power stage.

The performance of the multiplier in the UCC28070A has been significantly enhanced when compared to previous generation PFC controllers, with high linearity and accuracy over most of the input ranges. The accuracy is at its worst as V_{VAO} approaches 1V because the error of the (V_{VAO} – 1) subtraction increases and begins to distort the IMO reference current to a greater degree.

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6.3.11 Enhanced Transient Response (VA Slew-Rate Correction)

Due to the low voltage-loop bandwidth required to maintain proper PFC and ignore the slight ripple at twice-line frequency on the output, the response of ordinary PFC controllers to input voltage and load transients are usually slow. In the UCC28070A, however, the Q_{VFF} function effectively handles the line-transient response with the exception of any minor adjustments needed within a Q_{VFF} level.

Load transients on the other hand can only be handled by the voltage loop; therefore, the UCC28070A has been designed to improve its transient response by pulling up on the output of the voltage amplifier (V_{VAO}) with an additional 100 μA of current in the event the voltage on VSENSE drops below 93% of regulation (2.79V).

During a soft-start cycle, when V_{VSENSE} is ramping up from the 0.75V PFC-Enable threshold, the 100 μA slew-rate correction current source is disabled to ensure gradual and controlled ramping of output voltage and input current.

6.3.12 Bias Voltages (VCC and VREF)

The UCC28070A operates within a VCC bias-supply range of 10V to 21V. An undervoltage lockout (UVLO) threshold prevents the PFC from activating until V_{VCC} > 10.2V, and 1V of hysteresis assures reliable start-up from a possibly low-compliance bias source. An internal 25V Zener-like clamp on the VCC pin is intended only to protect the device from brief energy-limited surges from the bias supply, and must not be used as a regulator with a current-limited source.

At minimum, a 0.1 μF ceramic bypass capacitor must be applied from VCC to GND close to the device pins to provide local filtering of the bias supply. Larger values may be required depending on I_{VCC} peak current magnitudes and durations to minimize ripple voltage on VCC.

To provide a smooth transition out of UVLO and to make the 6V voltage reference available as early as possible, the output from VREF is enabled when V_{VCC} exceeds 8V typically.

The VREF circuitry is designed to provide the biasing of all internal control circuits and for limited use externally. At minimum, a 22nF ceramic bypass capacitor must be applied from VREF to GND close to the device pins to ensure stability of the circuit. External load current on the VREF pin must be limited to less than 2mA, or degraded regulation may result.

6.3.13 PFC Enable and Disable

The UCC28070A contains two independent circuits dedicated to disabling the GDx outputs based on the biasing conditions of the VSENSE or SS pins.

The first is a PFC Enable which monitors V_{VSENSE} and holds off soft-start and the overall PFC function until the output has precharged to approximately 25% of the nominal set point. Before V_{VSENSE} reaches 0.75V, almost all of the internal circuitry is disabled. Once V_{VSENSE} exceeds 0.75V and V_{VAO} < 0.75V, the oscillator, multiplier, and current synthesizer are enabled and the SS circuitry begins to ramp up the voltage on the SS pin.

The second circuit provides an external interface to emulate an internal fault condition to disable the GDx outputs without fully disabling the voltage loop and multiplier. By externally pulling the SS pin below 0.6V, the GDx outputs are immediately disabled and held low. Assuming no other fault conditions are present, normal PWM operation resumes when the external SS pulldown is released. The external pulldown must be sized large enough to override the internal 1.5mA adaptive SS pullup once the SS voltage falls below the disable threshold. TI recommends using a MOSFET with $R_{DS(on)}$ < 100Ω to ensure the SS pin is held adequately below the disable threshold.

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6.3.14 Adaptive Soft-Start

To maintain a controlled power up, the UCC28070A has been designed with an adaptive soft-start function that overrides the internal reference voltage with a controlled voltage ramp during power up. On initial power up, once V_{VSENSE} exceeds the 0.75V enable threshold (V_{EN}), the internal pulldown on the SS pin is released, and the 1.5mA adaptive soft-start current source is activated. This 1.5mA pullup almost immediately pulls the SS pin to 0.75V (V_{VSENSE}) to bypass the initial 25% of dead time during a traditional 0V to $V_{REGULATION}$ SS ramp. Once the SS pin has reached the voltage on VSENSE, the 10 μA soft-start current (I_{SS}) takes over. Thus, through the selection of the soft-start capacitor (C_{SS}), the effective soft-start time (t_{SS}) may be easily programmed based on 方程式 21.

$$t_{SS} = C_{SS} \times \left(\frac{2.25\ V}{10\ \mu A} \right) \tag{21}$$

Often, a system restart is desired following a brief shutdown. In such a case, VSENSE may still have substantial voltage if V_{OUT} has not fully discharged or if high line has peak charged C_{OUT}. To eliminate the delay caused by charging C_{SS} from 0V up to the precharged V_{VSENSE} with only the 10 μA current source and minimize any further output voltage sag, the adaptive soft start uses a 1.5mA current source to rapidly charge C_{SS} to V_{VSENSE}, after which time the 10 μA source controls the V_{SS} rise at the desired soft-start ramp rate. In such a case, t_{SS} is estimated as follows:

$$t_{SS} = C_{SS} \times \left(\frac{3\ V - V_{VSENSE0}}{10\ \mu A} \right) \tag{22}$$

where

- $V_{VSENSE0}$ is the voltage at VSENSE at the moment that a soft-start or restart is initiated

备注

For soft-start to be effective and avoid overshoot on V_{OUT}, the SS ramp must be slower than the voltage-loop control response. Choose $C_{SS} \geqslant C_{VZ}$ to ensure this.

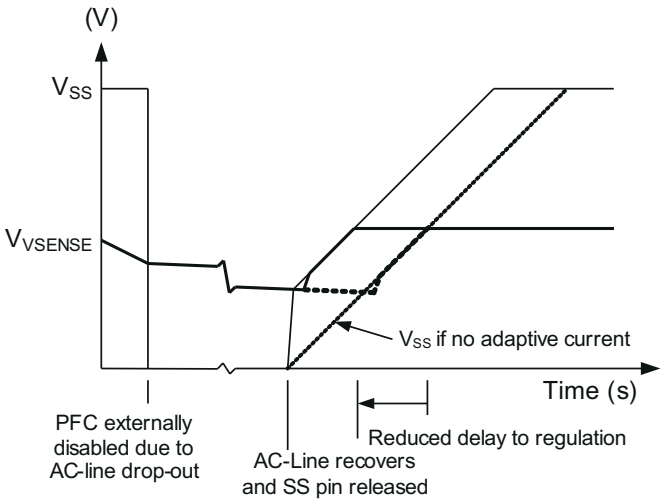


图 6-4. Soft-Start Ramp Rate

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6.3.15 PFC Start-Up Hold Off

An additional feature designed into the UCC28070A is the *Start-Up Hold Off* logic that prevents the device from initiating a soft-start cycle until the VAO pin is below the zero-power threshold (0.75V). This feature ensures that the SS cycle initiates from zero-power and zero duty-cycle while preventing the potential for any significant inrush currents due to stored charge in the VAO compensation network.

6.3.16 Output Overvoltage Protection (OVP)

Because of the high voltage output and a limited design margin on the output capacitor, output overvoltage protection is essential for PFC circuits. The UCC28070A implements OVP through the continuous monitoring of V_{VSENSE}. In the event V_{VSENSE} rises above 106% of regulation (3.18V), the GDx outputs are immediately disabled to prevent the output voltage from reaching excessive levels. Meanwhile the CAOx outputs are pulled low to ensure a controlled recovery starting from 0% duty-cycle after an OVP fault is released. Once V_{VSENSE} has dropped below 3.08V, the PWM operation resumes normal operation.

6.3.17 Zero-Power Detection

To prevent undesired performance under no-load and near no-load conditions, the UCC28070A zero-power detection comparator is designed to disable both GDA and GDB outputs in the event V_{VAO} voltage falls below 0.75V. The 150mV of hysteresis ensures that the outputs remain disabled until V_{VAO} has nearly risen back into the linear range of the multiplier ($V_{VAO} \geqslant 0.9V$).

6.3.18 Thermal Shutdown

To protect the power supplies from silicon failures at excessive temperatures, the UCC28070A has an internal temperature-sensing comparator that shuts down nearly all of the internal circuitry and disables the GDA and GDB outputs if the die temperature rises above 160°C. Once the die temperature falls below 140°C, the device brings the outputs up through a typical soft-start.

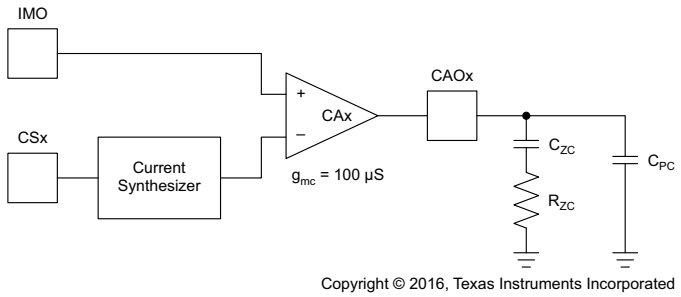
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6.3.19 Current Loop Compensation

The UCC28070A incorporates two identical and independent transconductance-type current-error amplifiers (one for each phase) with which to control the shaping of the PFC input current waveform. The current-error amplifier (CA) forms the heart of the embedded current control loop of the boost PFC preregulator, and is compensated for loop stability using familiar principles [7, 8]. The output of the CA for phase-A is CAOA, and that for phase-B is CAOB. Because the design considerations are the same for both, they are collectively referred to as CAOx, where x is A or B.

In a boost PFC preregulator, the current control loop comprises the boost power plant stage, the current sensing circuitry, the wave-shape reference, the PWM stage, and the CA with compensation components. The CA compares the average boost inductor current sensed with the wave-shape reference from the multiplier stage and generates an output current proportional to the difference.

This CA output current flows through the impedance of the compensation network generating an output voltage, V_{CAO}, which is then compared with a periodic voltage ramp to generate the PWM signal necessary to achieve PFC.



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图 6-5. Current Error Amplifier With Type II Compensation

For frequencies above boost LC resonance and below f_{PWM}, the small-signal model of the boost stage, which includes current sensing, can be simplified to:

$$\frac{v_{RS}}{v_{CA}} = \frac{V_{OUT} \times \frac{R_S}{N_{CT}}}{\Delta V_{RMP} \times k_{SYNC} \times s \times L_B} \quad (23)$$

where:

- L_B = mid-value boost inductance
- R_S = CT sense resistor
- N_{CT} = CT turns ratio
- V_{OUT} = average output voltage of the PFC converter
- $\Delta V_{RMP} = 4V_{pk\text{-}pk}$ amplitude of the PWM voltage ramp
- k_{SYNC} = ramp reduction factor due to external synchronization frequency: $k_{SYNC} = (15000 / R_{RT}(k\Omega)) / f_{SYNC}$, where $R_{RT}(k\Omega)$ is from 方程式 8. When external synchronization is not used, $k_{SYNC} = 1$.
- s = Laplace complex variable

An R_{ZC}-C_{ZC} network is introduced on CAOx to obtain high gain for the low-frequency content of the inductor current signal, but reduced flat gain above the zero frequency out to f_{PWM} to attenuate the high-frequency switching ripple content of the signal (thus averaging it).

The switching ripple voltage on the CAOx outputs must be attenuated to less than 1/10 of the ΔV_{RMP} amplitude so as to be considered negligible ripple.

Thus, CAOx gain at f_{PWM} is:

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$$g_{mc} \times Rzc \le \frac{\frac{\Delta V_{RMP} \times k_{SYNC}}{10}}{\Delta I_{LB} \times \frac{R_S}{N_{CT}}} \tag{24}$$

where:

- ΔI_{LB} is the maximum peak-to-peak ripple current in the boost inductor
- g_{mc} is the transconductance of the CA, 100 μ S

$$R_{ZC} \le \frac{4V \times N_{CT} \times k_{SYNC}}{10 \times 100\mu S \times \Delta I_{LB} \times R_S} \tag{25}$$

The current-loop cross-over frequency is then found by equating the open-loop gain to 1 and solving for f_{CXO}:

$$f_{CXO} = \frac{V_{OUT} \times \frac{R_S}{N_{CT}}}{\Delta V_{RMP} \times k_{SYNC} \times 2\pi \times L_B} \times g_{mc} \times Rzc \tag{26}$$

C_{ZC} is then determined by setting $f_{ZC} = f_{CXO} = 1 / (2\pi \times R_{ZC} \times C_{ZC})$ and solving for C_{ZC}. At $f_{ZC} = f_{CXO}$, a phase margin of 45° is obtained at f_{CXO}. Greater phase margin may be had by placing $f_{ZC} < f_{CXO}$ (increase C_{ZC}).

An additional high-frequency pole is generally added at f_{PWM} or $f_{PWM}/2$ to further attenuate ripple and noise at f_{PWM} and higher. This is done by adding a lower-value capacitor, C_{PC}, across the $R_{ZC}C_{ZC}$network.

$$C_{PC} = \frac{1}{2\pi \times \frac{f_{PWM}}{2} \times R_{ZC}} \tag{27}$$

The procedure above is valid for fixed-value inductors.

备注

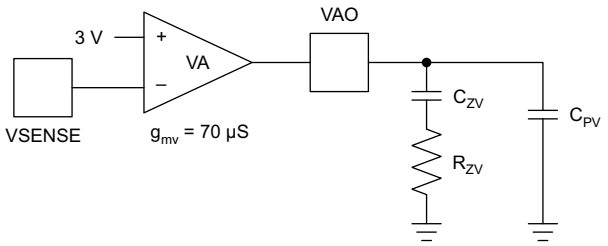
If a "swinging-choke" boost inductor (inductance decreases gradually with increasing current) is used, f_{CXO} varies inversely with inductance, so C_{ZC} must be determined at maximum inductance.

6.3.20 Voltage Loop Compensation

The outer voltage control loop of the dual-phase PFC controller functions the same as with a single-phase controller, and compensation techniques for loop stability are standard [7]. The bandwidth of the voltage-loop must be considerably lower than the twice-line ripple frequency (f_{2LF}) on the output capacitor to avoid distortion-causing correction to the output voltage. The output of the voltage-error amplifier (V_{VAO}) is an input to the multiplier to adjust the input current amplitude relative to the required output power. Variations on VAO within the bandwidth of the current loops influences the wave-shape of the input current. Because the low-frequency ripple on C_{OUT} is a function of input power only, its peak-to-peak amplitude is the same at high-line as at low-line. Any response of the voltage-loop to this ripple has a greater distorting effect on high-line current than on low-line current. Therefore, the allowable percentage of 3rd-harmonic distortion on the input current contributed by VAO must be determined using high-line conditions.

Because the voltage-error amplifier (VA) is a transconductance type of amplifier, the impedance on its input has no bearing on the amplifier gain, which is determined solely by the product of its transconductance (g_{mv}) with its output impedance (Z_{OV}). Thus, the VSENSE input divider-network values are determined separately based on criteria discussed in *VSENSE and VINAC Open-Circuit Protection*. Its output is the VAO pin.

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图 6-6. Voltage Error Amplifier With Type II Compensation

The twice-line ripple voltage component of V_{VSENSE} must be sufficiently attenuated and phase-shifted at VAO to achieve the desired level of 3rd-harmonic distortion of the input current wave-shape [4]. For every 1% of 3rd-harmonic input distortion allowable, the small-signal gain $G_{VEA} = V_{VAOpk} / v_{SENSEpk} = g_{mv} \times Z_{OV}$ at the twice-line frequency must allow no more than 2% ripple over the full V_{VAO} voltage range. In the UCC28070A, V_{VAO} can range from 1V at zero load power to approximately 4.2V at full load power for a ΔV_{VAO} = 3.2V, so 2% of 3.2V is 64mV peak ripple.

备注

Although the maximum V_{VAO} is clamped at 5V, at full load V_{VAO} may vary around an approximate center point of 4.2V to compensate for the effects of the quantized feed-forward voltage in the multiplier stage (see *Linear Multiplier and Quantized Voltage Feed Forward* for details). Therefore, 4.2V is the proper voltage to use to represent maximum output power when performing voltage-loop gain calculations.

The output capacitor maximum low-frequency, zero-to-peak, ripple voltage is closely approximated by:

$$v_{0pk} = \frac{P_{IN(avg)} \times X_{Cout}}{V_{OUT(avg)}} = \frac{P_{IN(avg)}}{V_{OUT(avg)} \times 2\pi \times f_{2LF} \times C_{OUT}} \quad (28)$$

where:

- $P_{IN(avg)}$ is the total maximum input power of the interleaved-PFC preregulator
- $V_{OUT(avg)}$ is the average output voltage
- C_{OUT} is the output capacitance

$$V_{SENSEpk} = V_{0pk} \times k_R \quad (29)$$

where

- k_R is the gain of the resistor-divider network on VSENSE

Thus, for k_{3rd}, the percentage of allowable 3rd-harmonic distortion on the input current attributable to the VAO ripple,

$$Z_{OV(f_{2LF})} = \frac{k_{3rd} \times 64\ mV \times V_{OUT(avg)} \times 2\pi \times f_{2LF} \times C_{OUT}}{g_{mv} \times k_R \times P_{IN(avg)}} \quad (30)$$

This impedance on VAO is set by a capacitor (C_{PV}), where $C_{PV} = 1 / (2\pi f_{2LF} \times Z_{OV}(f_{2LF}))$; therefore:

$$Cpv = \frac{g_{mv} \times k_R \times P_{IN(avg)}}{k_{3rd} \times 64\ mV \times V_{OUT(avg)} \times (2\pi \times f_{2LF})^2 \times C_{OUT}} \quad (31)$$

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The voltage-loop unity-gain cross-over frequency (f_{VXO}) may now be solved by setting the open-loop voltage transfer function gain equal to 1:

$$Tv(f_{VXO}) = G_{BST} \times G_{VEA} \times k_R = \left(\frac{P_{IN(avg)} \times X_{Cout}}{\Delta V_{VAO} \times V_{OUT(avg)}} \right) \times \left(g_{mv} \times X_{Cpv} \right) \times k_R = 1 \quad (32)$$

$$\text{so,} \quad f_{VXO}^{\ 2} = \frac{g_{mv} \times k_R \times P_{IN(avg)}}{\Delta V_{VAO} \times V_{OUT(avg)} \times (2\pi)^2 \times Cpv \times C_{OUT}} \quad (33)$$

The zero-resistor (R_{ZV}) from the zero-placement network of the compensation may now be calculated. Together with C_{PV}, R_{ZV} sets a pole right at f_{VXO} to obtain 45° phase margin at the cross-over.

$$\text{Thus,} \quad Rzv = \frac{1}{2\pi \times f_{VXO} \times Cpv} \quad (34)$$

Finally, a zero is placed at or below f_{VXO} / 6 with capacitor C_{ZV} to provide high gain at DC but with a breakpoint far enough below f_{VXO} so as not to significantly reduce the phase margin. Choosing f_{VXO} / 10 allows one to approximate the parallel combination value of C_{ZV} and C_{PV} as C_{ZV}, and solve for C_{ZV} simply as:

$$Czv = \frac{10}{2\pi \times f_{VXO} \times Rzv} \approx 10 \times Cpv \quad (35)$$

By using a spreadsheet or math program, C_{ZV}, R_{ZV}, and C_{PV} may be manipulated to observe their effects on f_{VXO} and phase margin and the percentage contribution to 3rd-harmonic distortion. Also, phase margin may be checked as $P_{IN(avg)}$ level and system parameter tolerances vary.

备注

The percentage of 3rd-harmonic distortion calculated in this section represents the contribution from the f_{2LF} voltage ripple on C_{OUT} only. Other sources of distortion, such as the current-sense transformer, the current synthesizer stage, excessively-limited D_{MAX}, and so on, can contribute additional 3rd and higher-order harmonic distortion.

6.4 Device Functional Modes

The UCC28070A operates in Average Current Mode. This eliminates the peak-to-average current error inherent in the peak current mode control method and gives lower THD and harmonics on the current drawn from the line. It does not require slope compensation and has better noise immunity than the peak current control method.

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7 Application and Implementation

备注

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7.1 Application Information

The UCC28070A is a switch-mode controller used in interleaved boost converters for power factor correction. The UCC28070A device requires few external components to operate as an active PFC preregulator. It operates at a fixed frequency in continuous conduction mode. The operating switching frequency can be programmed from 10kHz to 300kHz by a single resistor from the RT pin to ground. The magnitude and rate of optional frequency dithering may also be controlled easily.

The internal 6V reference voltage provides for accurate output voltage regulation over the typical world-wide $85V_{AC}$ to $265V_{AC}$ mains input range from zero to full output load. The reference may also be used to set a peak current limit. Regulation is accomplished in two loops. The inner current loop shapes the average input current to match the sinusoidal input voltage under continuous inductor current conditions. A single multiplier output is shared between the two current amplifiers to ensure close matching of the currents in the two phases. A Zero-Power detector disables both the GDA and GDB outputs under light-load conditions.

7.2 Typical Application

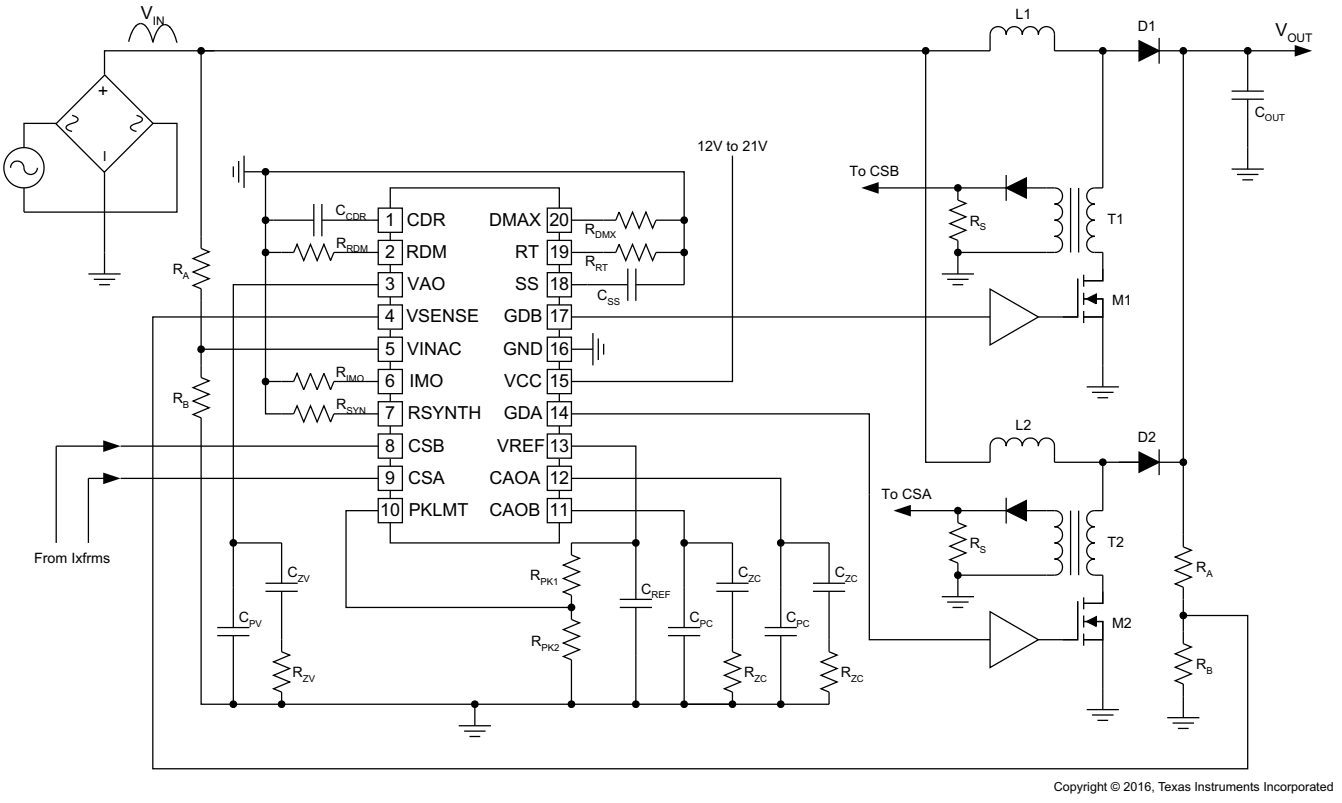


图 7-1. Typical Application Diagram

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7.2.1 Design Requirements

For this design example, use the parameters listed in 表 7-1 as the input parameters.

表 7-1. Design Parameters

DESIGN PARAMETER		MIN	TYP	MAX	UNIT
V_{AC}	Input voltage	85		265	V
V_{OUT}	Output voltage		390		V
f_{LINE}	Line frequency	47		63	Hz
f_{SW}	Switching frequency		200		kHz
P_{OUT}	Output power		300		W
η	Full load efficiency	90%			

7.2.2 Detailed Design Procedure

7.2.2.1 Output Current Calculation

The first step is to determine the maximum load current on the output.

$$I_o = \frac{P_o}{V_o} = \frac{300W}{385V} = 0.78A \tag{36}$$

7.2.2.2 Bridge Rectifier

The maximum RMS input-line current is given by 方程式 37:

$$I_{line_max} = \frac{P_o}{\eta V_{AC_min}} = \frac{300W}{98\%(85V)} = 3.6Arms \tag{37}$$

The peak input current is given by 方程式 38:

$$I_{in_pk} = \sqrt{2} \times I_{line_max} = \sqrt{2} \times 3.6A = 5.1A \tag{38}$$

The maximum average rectified line current is given by 方程式 39:

$$I_{in_avg_max} = \frac{2\sqrt{2}}{\pi} \times I_{line_max} = \frac{2\sqrt{2}}{\pi} \times 3.6A = 3.25A \tag{39}$$

A typical bridge rectifier has a forward voltage drop V_F of 0.95V at I_{in_pk}. The maximum power loss in the rectifier bridge can be conservatively estimated by 方程式 40:

$$P_{BR_max} = 2 \times V_F \times I_{in_avg_max} = 2 \times 0.95V \times 3.25A = 6.2W \tag{40}$$

The bridge rectifier must be rated to carry the full line current plus any anticipated line-surge peaks. The bridge rectifier also carries the full inrush current as the bulk capacitor C_{OUT} charges when the line is connected. The voltage rating of the bridge is recommended to maintain suitable margin to the maximum anticipated peak input voltage including AC-line swells.

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7.2.2.3 PFC Inductor (L_1 and L_2)

The selection of the PFC inductor value is usually based on a number of different considerations. Cost, core size, EMI filter, and inductor ripple current are some of the factors that have an influence. In previous versions of this data sheet, the design method to choose the inductor targetted the peak to peak inductor ripple current (ΔI_L) at the minimum input voltage to have the same amplitude as the peak of AC-line current in each phase. The line current flows equally in the two phases so ΔI_L is half I_{in_pk} calculated in 方程式 38. That method worked well for relatively low minimum input voltages, but was found to generate excessively low inductances for minimum inputs with peak voltages near ½ V_{OUT}.

A new method of calculating boost inductance is presented in this datasheet where low input-current distortion is the main design criterion. In recent years, low distortion at lighter loads and higher input voltages has become a major design requirement in many applications. In a CCM-Boost-PFC, the total harmonic distortion of the input current (THDi) increases greatly when the inductor current operates in DCM over a significant portion of the input AC-line cycle. To maintain low THDi at any given line and load point, it is necessary to maintain CCM in the boost inductors at that operating point. Since a PFC converter is intended to present an equivalent or emulated resistance Re to the AC line, it can be shown [5] that inductor current operates in CCM over the entire line cycle when:

$$R_e < \frac{2 \times L_B}{T_{PWM}}, \text{ where } R_e = \frac{V_{rms}^2}{P_{IN}} \text{ and } T_{PWM} = \frac{1}{f_{PWM}} \tag{41}$$

By rearranging terms and substituting, the minimum boost inductance necessary to maintain CCM is calculated as:

$$L_1 = L_2 = L_B \geq \frac{V_{rms_CCM(max)}^2}{2 \times \left(P_{O_CCM(min)}/\eta\right) \times f_{PWM}} \tag{42}$$

where

- $V_{rms_CCM(max)}$ is the highest rms input voltage at which CCM operation is to be maintained
- $P_{O_CCM(min)}$ is the lowest output power level *per inductor* where CCM is to be maintained
- η is the expected conversion efficiency at $P_{O_CCM(min)}$ and $V_{rms_CCM(max)}$

Lower values of boost inductance than that calculated by 方程式 42 can be used for PFC, but THDi will increase as the amount of DCM increases in the line cycle.

To match the previous data sheet inductor selection, it can be seen that for CCM operation at 100Vrms input, 150W per phase, 95 % efficiency, and 200kHz PWM switching frequency, L_B must be ⩾ 158.333µH.
Select L_1 = L_2 = 160µH.

Given that inductance, ΔI_L at the peak of low-line can be calculated as follows:

$$\Delta I_L = \frac{\left(V_{OUT} - \sqrt{2} \times V_{AC_min}\right)}{L_B} \times \left(\frac{\sqrt{2} \times V_{AC_min}}{V_{OUT}}\right) \times T_{PWM} = \frac{(385\text{ V} - 120\text{ V})}{160\text{ µH}} \times \left(\frac{120\text{ V}}{385\text{ V}}\right) \times 5\text{ µs} = \sim 2.57\text{ A} \tag{43}$$

Then, the peak current in each boost inductor is approximately:

$$I_{L_pk} = \frac{I_{in_pk}}{2} + \frac{\Delta I_L}{2} = \frac{5.1\text{ A}}{2} + \frac{2.57\text{ A}}{2} = \sim 3.8\text{ A} \tag{44}$$

The basic inductor specifications for this application example are:

- Inductance: 160µH
- Peak current: 4A

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7.2.2.4 PFC MOSFETs (M_1 and M_2)

The main specifications for the PFC MOSFETs are:

- B_{VDSS}, drain source breakdown voltage: ⩾650V
- $R_{DS(on)}$, ON-state drain source resistance: 520mΩ at 25 °C, estimate 1Ω at 125°C
- C_{OSS}, output capacitance: 32pF at ~400V
- tr, devise rise time: 12ns
- tf, device fall time: 16ns

The losses in the device are calculated by 方程式 45 and 方程式 46. These calculations are approximations because the losses are dependent on parameters which are not well controlled. For example, the $R_{DS(on)}$ of a MOSFET may increase by a factor of 2 from 25°C to 125°C. Therefore several iterations may be needed to choose an optimum device for an application different than the one discussed here.

Each phase carries half the load power so the conduction losses are estimated by:

$$P_{M_cond} = \left(\frac{0.5 \times P_o}{\sqrt{2} \times V_{IN(min)}} \times \sqrt{2 - \frac{16}{3\pi} \times \frac{\sqrt{2} \times V_{IN(min)}}{V_{OUT}}} \right)^2 \times R_{DS(on)} = \left(\frac{150W}{\sqrt{2} \times 85V} \times \sqrt{2 - \frac{16}{3\pi} \times \frac{\sqrt{2} \times 85V}{385V}} \right)^2 \times 1.0 = 2.25W \quad (45)$$

The switching losses in each MOSFET are estimated by:

$$P_{M_sw} = \frac{1}{2} \times f_{SW} \left(V_o \times \frac{I_{line_max}}{2} \times (t_r + t_f) + C_{oss} \times V_o^2 \right) = \frac{1}{2} \times 200kHz \left(385V \times \frac{3.6A}{2} \times (12ns + 16ns) + 32pF \times 385V^2 \right) = 2.4W \quad (46)$$

The total losses in each MOSFET are then:

$$P_M = P_{M_cond} + P_{M_sw} = 2.25W + 2.4W = 4.9W \quad (47)$$

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7.2.2.5 PFC Diode

Reverse-recovery losses can be significant in a CCM boost converter. A silicon-carbide diode is chosen here because it has no reverse-recovery charge (Q_{RR}) and therefore zero reverse-recovery losses.

$$P_D = V_f \times \frac{I_{OUT}}{2} = 1.5V \times \frac{0.78A}{2} = 580mW \quad (48)$$

7.2.2.6 PFC Output Capacitor

The value of the output capacitor is governed by the required hold-up time and the allowable ripple voltage on the output.

The hold-up time depends on the load current and the minimum acceptable voltage at the output.

The value of the output capacitor must be large enough to provide the required hold-up time and keep the ripple voltage at twice-line frequency within acceptable limits. Normally a capacitance value of about 0.6 μF per Watt of output power (for ~400V output) is a reasonable compromise where hold-up time is not significant. At 300W this would indicate a capacitance of about 200 μF.

The low-frequency (at twice-line frequency) rms voltage ripple on V_{OUT} is given by 方程式 49:

$$V_{O_ripple} = \frac{1}{\sqrt{2}} \times \frac{I_O}{2\pi \times 2f_{line} \times C_O} = \frac{1}{\sqrt{2}} \times \frac{0.78A}{2\pi \times 100Hz \times 200\mu F} = 4.4Vrms \quad (49)$$

The resulting twice-line low-frequency current in the capacitor is:

$$I_{O_ripple} = 2\pi \times 2f_{line} \times C_O \times V_{O_ripple} = 2\pi \times 100Hz \times 200\mu F \times 4.4Vrms = 0.55Arms \quad (50)$$

7.2.2.7 Current-Loop Feedback Configuration (Sizing of the Current-Transformer Turns-Ratio N_{CT} and Current-Sense Resistor R_S)

A current-sense transformer (CT) is typically used in high-power applications to sense inductor current and avoid the losses inherent in the use of a current-sensing resistor. For average current-mode control, the entire inductor current waveform is required; however low-frequency CTs are obviously impracticable. Normally, two high-frequency CTs are used, one in the switching leg to obtain the up-slope current and one in the diode leg to obtain the down-slope current. These two current signals are summed together to form the entire inductor current, but this is not necessary with the UCC28070A.

A major advantage of the UCC28070A design is the current-synthesis function, which internally recreates the inductor current down-slope during the switching period OFF-time. This eliminates the need for the diode-leg CT in each phase, significantly reducing space, cost and complexity. A single resistor programs the synthesizer down-slope, as previously discussed in the *Current Synthesizer* section.

A number of trade-offs must be made in the selection of the CT. Various internal and external factors influence the size, cost, performance, and distortion contribution of the CT.

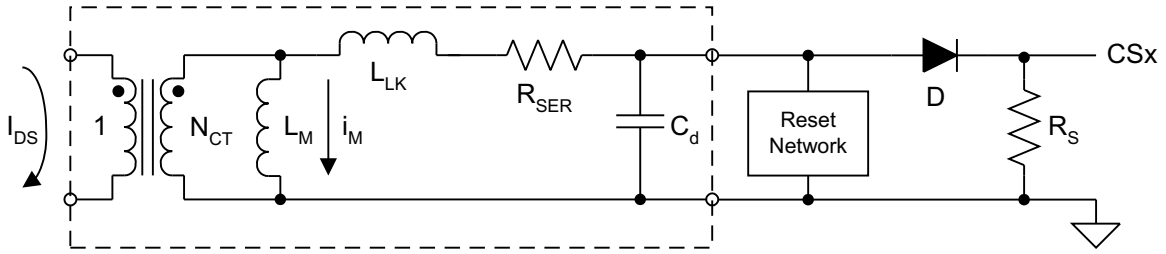
These factors include, but are not limited to:

- Turns-ratio (N_{CT})
- Magnetizing inductance (L_M)
- Leakage inductance (L_{LK})
- Volt-microsecond product (V μ s)
- Distributed capacitance (C_d)
- Series resistance (R_{SER})
- External diode drop (V_D)
- External current-sense resistor (R_S)
- External reset network

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Traditionally, the turns-ratio and the current-sense resistor are selected first. Some iterations may be needed to refine the selection once the other considerations are included.

In general, 50 ⩽ N_{CT} ⩽ 200 is a reasonable range from which to choose. If N_{CT} is too low, there may be high power loss in R_S and insufficient L_M. If too high, there could be excessive L_{LK} and C_d. (A one-turn primary winding is assumed.)



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图 7-2. Current Sense Transformer Equivalent Circuit

A major contributor to distortion of the input current is the effect of magnetizing current on the CT output signal (i_{RS}). A higher turns-ratio results in a higher L_M for a given core size. L_M must be high enough that the magnetizing current (i_M) generated is a very small percentage of the total transformed current. This is an impossible criterion to maintain over the entire current range, because i_M unavoidably becomes a larger fraction of i_{RS} as the input current decreases toward zero. The effect of i_M is to *steal* some of the signal current away from R_S, reducing the CSx voltage and effectively understating the actual current being sensed. At low currents, this understatement can be significant and CAOx increases the current-loop duty-cycle in an attempt to correct the CSx input(s) to match the IMO reference voltage. This unwanted correction results in overstated current on the input wave shape in the regions where the CT understatement is significant, such as near the AC line zero crossings. It can affect the entire waveform to some degree under the high line, light-load conditions.

The sense resistor R_S is chosen, in conjunction with N_{CT}, to establish the sense voltage at CSx to be about 3V at the center of the reflected inductor ripple current under maximum load. The goal is to maximize the average signal within the common-mode input range V_{CMCAO} of the CAOx current-error amplifiers, while leaving room for the peaks of the ripple current within V_{CMCAO}. The design condition must be at the lowest maximum input power limit as determined in *Linear Multiplier and Quantized Voltage Feed Forward*. If the inductor ripple current is so high as to cause V_{CSx} to exceed V_{CMCAO}, then R_S or N_{CT} or both must be adjusted to reduce peak V_{CSx}, which could reduce the average sense voltage center below 3V. There is nothing wrong with this situation; but be aware that the signal is more compressed between full-load and no-load, with potentially greater distortion at light loads.

The matter of volt-second balancing is important, especially with the widely varying duty-cycles in the PFC stage. Ideally, the CT is reset once each switching period; that is, the OFF-time V µ s product equals the ON-time V µ s product. ON-time V µ s is the time-integral of the voltage across L_M generated by the series elements R_{SER}, L_{LK}, D, and R_S. Off-time V µ s is the time-integral of the voltage across the reset network during the OFF-time. With passive reset, V µ s(off) is unlikely to exceed V µ s(on). Sustained unbalance in the on or off V µ s products leads to core saturation and a total loss of the current-sense signal. Loss of V_{CSx} causes V_{CAOx} to quickly rise to its maximum, programming a maximum duty-cycle at any line condition. This, in turn causes the boost inductor current to increase without control, until the system fuse or some component failure interrupts the input current.

It is vital that the CT has plenty of V µ s design-margin to accommodate various special situations where there may be several consecutive maximum duty-cycle periods at maximum input current, such as during peak current limiting.

Maximum V µ s(on) can be estimated by:

$$V\mu s(on)_{max} = (V_{RS} + V_D + V_{RSER} + V_{LK}) \times t_{ON(max)} \quad (51)$$

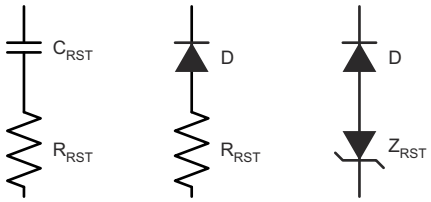
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where

- all factors are maximized to account for worst-case transient conditions
- $t_{ON(max)}$ occurs during the lowest dither frequency, if frequency dithering is enabled

For design margin, a CT rating of approximately 5 × V μs(on)max or higher is suggested. The contribution of V_{RS} varies directly with the line current. However, V_D may have a significant voltage even at near-zero current, so substantial V μs(on) may accrue at the zero-crossings where the duty-cycle is maximum. V_{RSER} is the least contributor, and often can be neglected if $R_{SER} < R_S$. V_{LK} is developed by the di/dt of the sensed current, and is not observable externally. However, its impact is considerable, given the sub-microsecond rise-time of the current signal plus the slope of the inductor current. Fortunately, most of the built-up V μs across L_M during the ON-time is removed during the fall-time at the end of the duty-cycle, leaving a lower net V μs(on) to be reset during the OFF-time. Nevertheless, the CT must, at the very minimum, be capable of sustaining the full internal V μs(on)max built up until the moment of turn-off within a switching period.

To reset the CT, V μs(off) may be generated with a resistor or Zener diode, using the i_M as bias current.



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图 7-3. Possible Reset Networks

To accommodate various CT circuit designs and prevent the potentially destructive result due to CT saturation, the UCC28070A maximum duty-cycle must be programmed such that the resulting minimum OFF-time accomplishes the required worst-case reset. (See *Programming the PWM Frequency and Maximum Duty-Cycle Clamp* for more information on sizing R_{DMX}.) Be aware that excessive C_d in the CT can interfere with effective resetting, because the maximum reset voltage is not reached until after 1/4-period of the CT self-resonant frequency. A higher turns-ratio results in higher C_d [6], so a trade-off between N_{CT} and D_{MAX} must be made.

The selected turns-ratio also affects L_M and L_{LK}, which vary proportionally to the square of the turns. Higher L_M is good, while higher L_{LK} is not. If the voltage across L_M during the ON-time is assumed to be constant (which it is not, but close enough to simplify) then the magnetizing current is an increasing ramp.

This upward ramping current subtracts from i_{RS}, which affects V_{CSx} especially heavily at the zero-crossings and light loads, as stated earlier. With a reduced peak at V_{CSx}, the current synthesizer starts the down-slope at a lower voltage, further reducing the average signal to CAOx and further increasing the distortion under these conditions. If low input current distortion at very light loads is required, special mitigation methods may need to be developed to accomplish that goal.

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7.2.2.8 Current-Sense Offset and PWM Ramp for Improved Noise Immunity

To improve noise immunity at extremely light loads, TI recommends adding a PWM ramp with a DC offset to the current-sense signals. Electrical components R_{TA}, R_{TB}, R_{OA}, R_{OB}, C_{TA}, C_{TB}, D_{PA1}, D_{PA2}, D_{PB1}, D_{PB1} C_{TA}, and C_{TB} form a PWM ramp that is activated and deactivated by the gate drive outputs of the UCC28070A. Resistor R_{OA} and R_{OB} add a DC offset to the CS resistors (R_{SA} and R_{SB}).

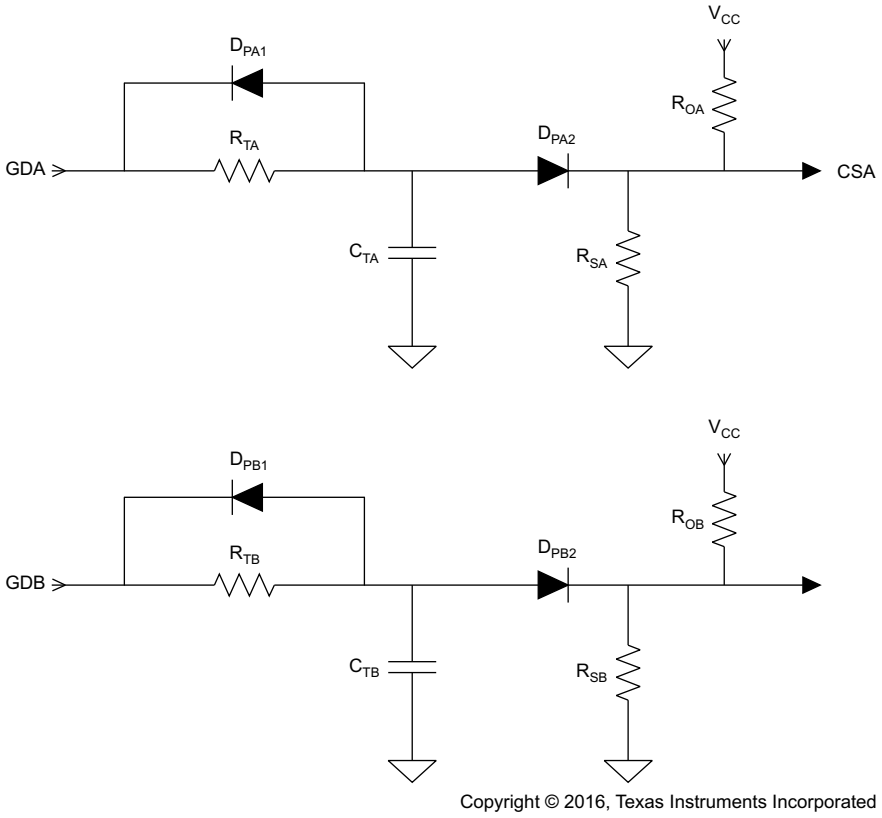


图 7-4. PWM Ramp and Offset Circuit

When the inductor current becomes discontinuous the boost inductors ring with the parasitic capacitances in the boost stages. This inductor current rings through the CTs causing a false current-sense signal. 图 7-5 shows what the current-sense signal looks like when the inductor current becomes discontinuous.

备注

The inductor current (IL1) and V_{Rsa} may vary from this graphical representation depending on how much inductor ringing is in the design when the current becomes discontinuous.

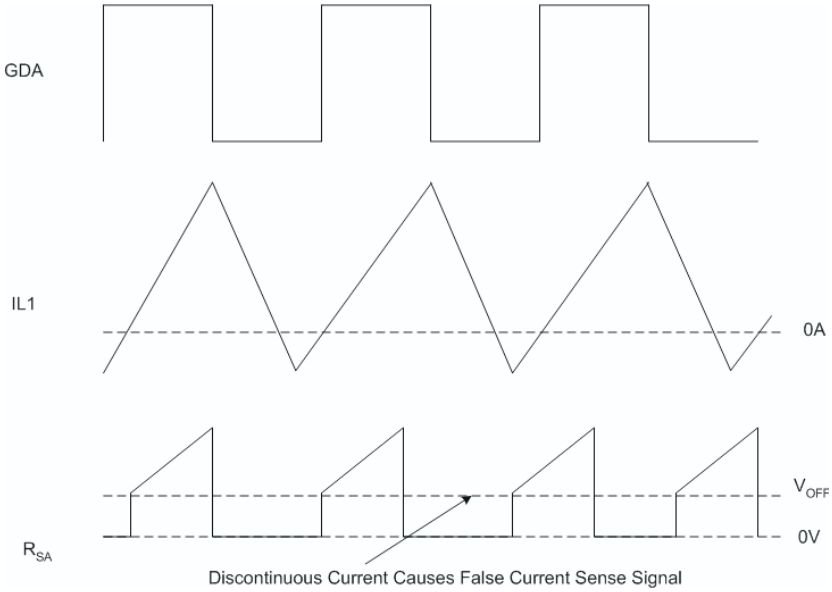


图 7-5. False Current-Sense Signal

To counter for the offset (V_{OFF}) just requires adjusting resistors R_{OA} and R_{OB} to ensure that when the unit goes discontinuous the current-sense resistor is not seeing a positive current when it must be zero. Setting the offset to 100mV is a good initial starting point and can be adjusted down or up based on evaluation of THDi.

$$R_{SA} = R_{SB} \tag{52}$$

$$R_{OA} = R_{OB} = \frac{\left(V_{VCC} - V_{OFF}\right) \times R_{SA}}{V_{OFF}} \tag{53}$$

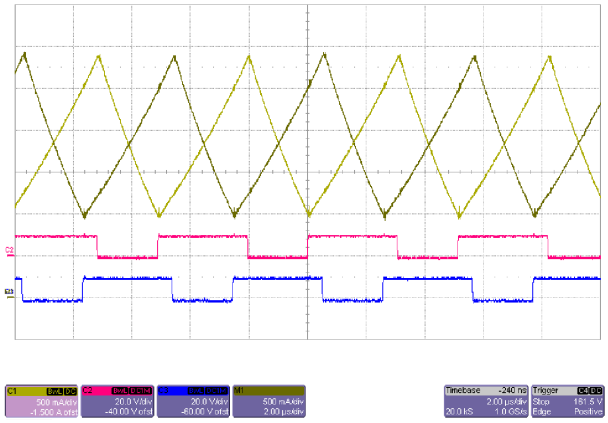
A small ramp with ΔV that is equal to [10% of the maximum current-sense signal (V_S) minus the offset] can also be added by selecting R_{TA}, R_{TB}, C_{TA} and C_{TB} as follows.

$$R_{TA} = R_{TB} = R_{SA} \times \frac{(V_{VCC} - (0.1 \times V_S - V_{OFF}) - V_{DA2})}{0.1 \times V_S - V_{OFF}} \tag{54}$$

$$C_{TA} = C_{TB} = \frac{1}{R_{SA} \times f_{PWM} \times 3} \tag{55}$$

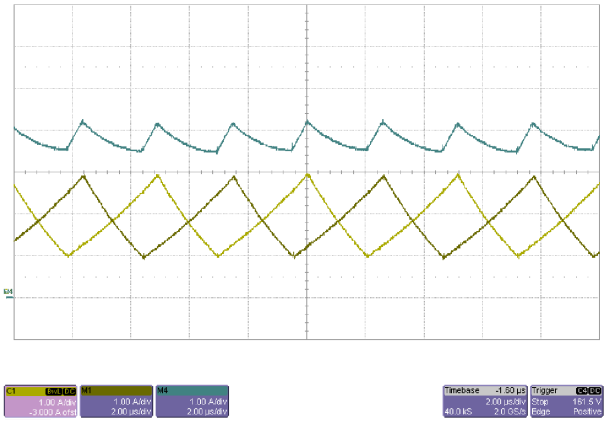
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7.2.3 Application Curves



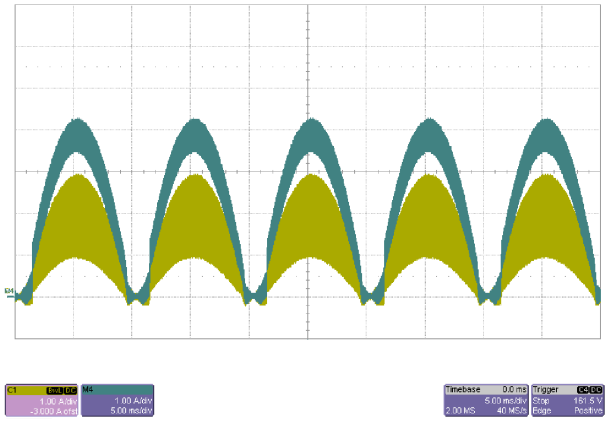
Ch1: Inductor current (I_A) Ch3: GDB Ch2: GDA
M1: Inductor Current (I_B)

图 7-6. Typical Inductor Currents



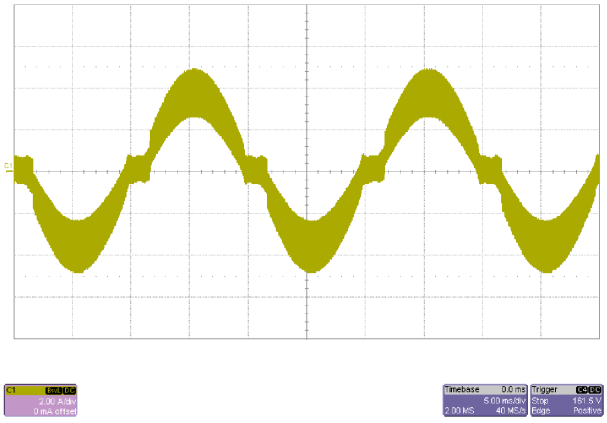
Ch1: Inductor current (I_A) M1: Inductor current (I_B)
M4: Input current (I_A + I_B)

图 7-7. Typical Inductor and Input Ripple Currents



Ch1: Inductor current (I_A) M4: Input current (I_A + I_B)

图 7-8. Typical Inductor and Input Ripple Currents



Ch1: Input current 120V_{AC} PF = 0.98

图 7-9. Typical Input Current

7.3 Power Supply Recommendations

The UCC28070A must be operated from a V_{CC} rail which is within the limits given in *Recommended Operating Conditions*. To avoid the possibility that the device might stop switching, V_{CC} must not be allowed to fall into the UVLO range. Yet, to minimize power dissipation in the device, V_{CC} must not be unnecessarily high. Keeping V_{CC} at or near 12V is a good compromise between these competing constraints.

The gate drive outputs from the UCC28070A can deliver large current pulses into their loads. This indicates the need for a low ESR decoupling capacitor to be connected as directly as possible between the VCC and GND pins. TI recommends ceramic capacitors with a stable dielectric characteristic over temperature, such as X7R. Avoid capacitors which have a large drop in capacitance with applied DC voltage bias and use a part that has a low voltage co-efficient of capacitance. TI recommends a decoupling capacitance of 10 μ F, X7R, with at least a 25V rating. A capacitor of at least 0.1 μ F must be placed as close as possible between the VCC and GND pins.

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7.4 Layout

7.4.1 Layout Guidelines

Interleaved-PFC techniques dramatically reduce input and output ripple current caused by the PFC boost inductor, which allows the circuit to use smaller and less expensive filters. To maximize the benefits of interleaving, the output filter capacitor must be located after the two phases allowing the current of each phase to be combined together before entering the boost capacitor. Similar to other power-management devices, when routing the PCB it is important to use *star grounding* techniques and to keep filter and high frequency bypass capacitors as close to device pins and ground as possible. To minimize the possibility of interference caused by magnetic coupling from the boost inductor, the device must be located at least 1 inch away from the boost inductor. TI recommends not to place the device underneath magnetic elements.

7.4.2 Layout Example

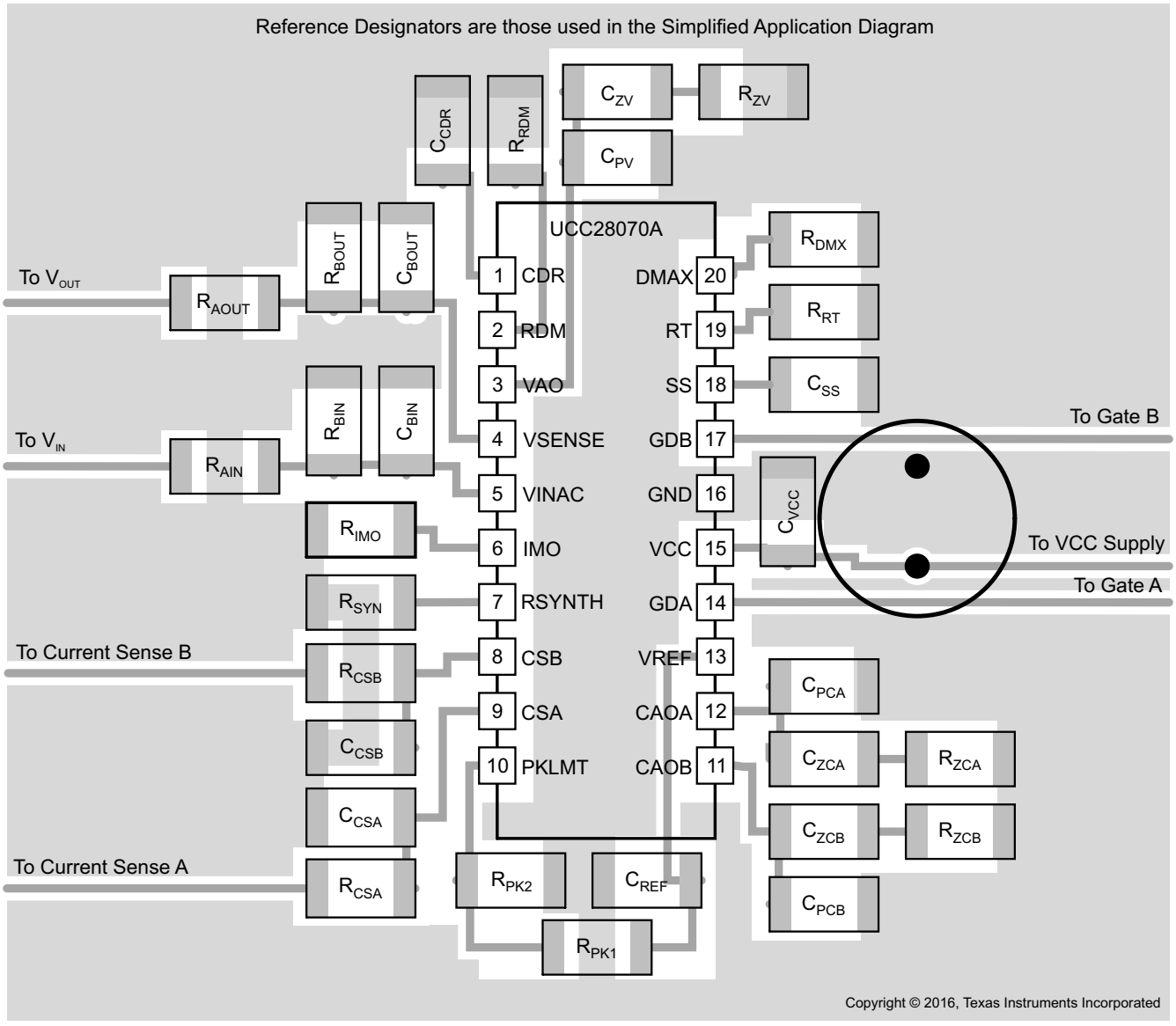


图 7-10. Layout Diagram

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8 器件和文档支持

8.1 文档支持

8.1.1 相关文档

如需帮助进行系统设计的相关文档，请参阅以下内容：

1. 德州仪器 (TI)，*UCC28070 Excel 应用设计工具* 计算程序
2. 德州仪器 (TI)，*UCC28070 300W 交错式 PFC 前置稳压器设计审查* 应用报告，Excel 设计工具的配套文档
3. O’Loughlin, Michael，*用于大功率转换器的交错式 PFC 前置稳压器*，德州仪器 (TI) 2006 Unitrode 电源研讨会，主题 5
4. Erickson, Robert W., *Fundamentals of Power Electronics*, 1st ed., pp. 604-608 Norwell, MA: Kluwer Academic Publishers, 1997
5. Erickson, R. W. & Maksimović, D. (2001), *Fundamentals of Power Electronics* (2nd ed.), Springer Science+Business Media, LLC. pp. 642-643
6. Creel, Kirby *Measuring Transformer Distributed Capacitance* 白皮书，Datatronic Distribution, Inc. 网站：http://www.datatronics.com/pdf/distributed_capacitance_paper.pdf
7. L. H. Dixon，*优化高功率因数开关前置稳压器的设计*，Unitrode 电源设计研讨会手册 SEM700，1990 年。SLUP093
8. L. H. Dixon，*用于离线电源的高功率因数前置稳压器*，Unitrode 电源设计研讨会手册 SEM600，1988 年。SLUP087

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.4 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (December 2023) to Revision C (July 2025)	Page
• 更新了整个文档中的印刷错误并澄清了文本。将 UCC28070 信息并入 UCC28070A 资料表。	1
• 修订了特性和应用要点。添加了超链接。	1
• Added Wide-SOIC package pin-out view for UCC28070	3
• Linked device numbers to respective DW and PW package thermal information	6
• Linked device numbers to respective fPWM limits	7
• Include UCC28070 at all mentions of UCC28070A throughout the data sheet	14
• Updated tSYNC meaning; added reference to minimum allowable pulse width	18
• Added falling thresholds to VINAC levels table	22
• Option in text for using ½ fPWM in Cpc equation. Changed equation to match calculator tool	28
• Remove extra factor of 2 from Io_ripple equation	36
• Corrections to equations for Rta and Cta	39

Changes from Revision A (May 2016) to Revision B (December 2023)	Page
• 更新了整个文档中的印刷错误并澄清了文本。	1
• Moved Absolute Maximum values for Supply voltage and current, Gate-drive currents, and signal-pin Currents from MIN column to MAX column	5
• Updated Y-axis units in several figures	11
• Added SYNC frequency limitation note in External Clock Synchronization section	18
• Added paragraph on PKLMT sub-harmonic oscillation	22
• Added clarifying equation for kSYNC in Current Loop Compensation section; corrected gain in Current Error Amplifier diagram and equation for Rzc.	28
• Updated gain in Voltage Error Amplifier diagram	29
• Updated text to clarify bridge rectifier design considerations	33
• Updated method for calculating boost inductance	34
• 在“相关文档”部分添加了其他参考	43

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC28070APW	Active	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28070A
UCC28070APW.B	Active	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28070A
UCC28070APWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28070A
UCC28070APWR.B	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28070A
UCC28070DW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC28070
UCC28070DW.B	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC28070
UCC28070DWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC28070
UCC28070DWR.B	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC28070
UCC28070DWRG4	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28070
UCC28070DWRG4.B	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28070
UCC28070PW	Active	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28070
UCC28070PW.B	Active	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28070
UCC28070PWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28070
UCC28070PWR.B	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28070
UCC28070PWRG4	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28070
UCC28070PWRG4.B	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28070

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF UCC28070 :

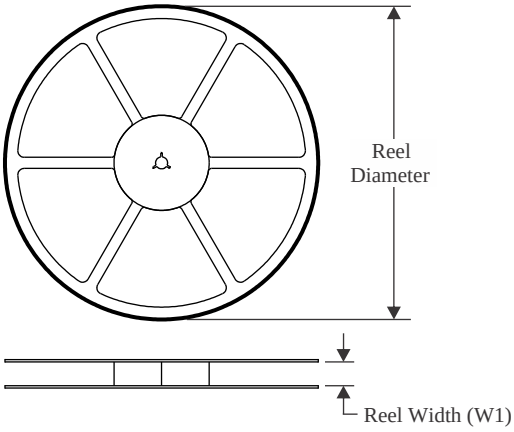
- Automotive : UCC28070-Q1

NOTE: Qualified Version Definitions:

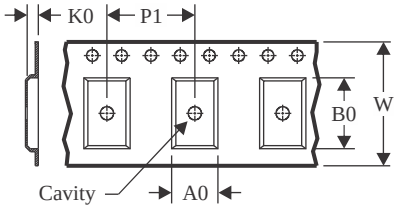
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

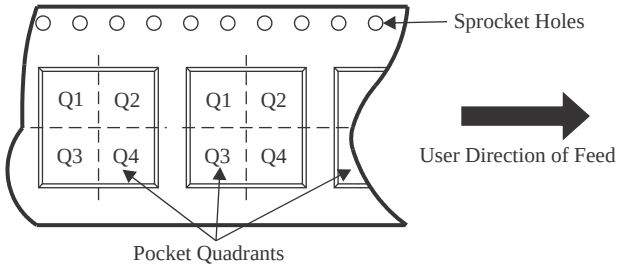


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

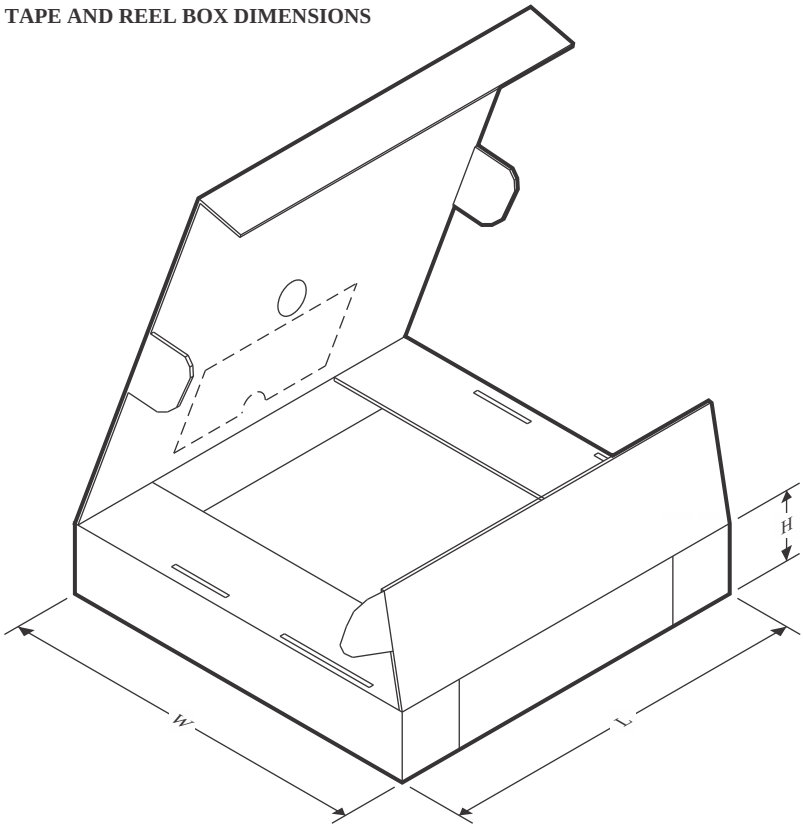
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28070APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
UCC28070DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
UCC28070DWRG4	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
UCC28070PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
UCC28070PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

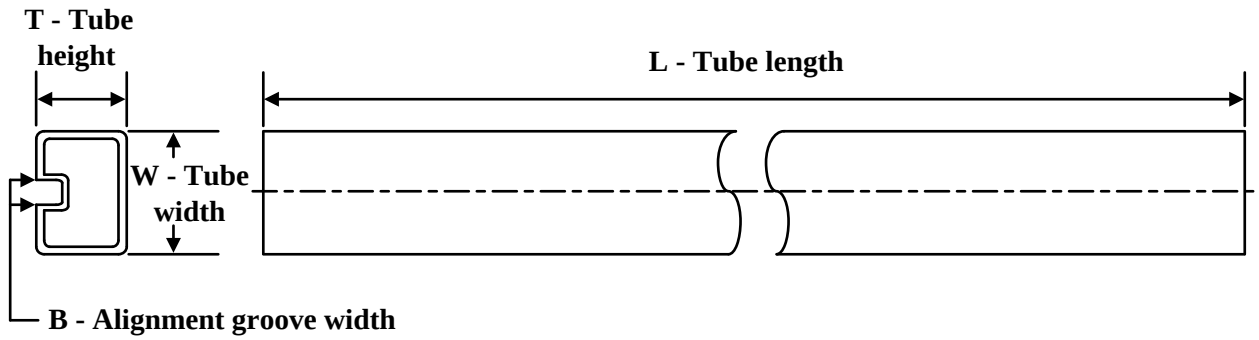
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

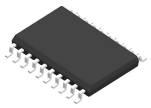
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28070APWR	TSSOP	PW	20	2000	353.0	353.0	32.0
UCC28070DWR	SOIC	DW	20	2000	356.0	356.0	45.0
UCC28070DWRG4	SOIC	DW	20	2000	356.0	356.0	45.0
UCC28070PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
UCC28070PWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC28070APW	PW	TSSOP	20	70	530	10.2	3600	3.5
UCC28070APW.B	PW	TSSOP	20	70	530	10.2	3600	3.5
UCC28070DW	DW	SOIC	20	25	507	12.83	5080	6.6
UCC28070DW.B	DW	SOIC	20	25	507	12.83	5080	6.6
UCC28070PW	PW	TSSOP	20	70	530	10.2	3600	3.5
UCC28070PW.B	PW	TSSOP	20	70	530	10.2	3600	3.5

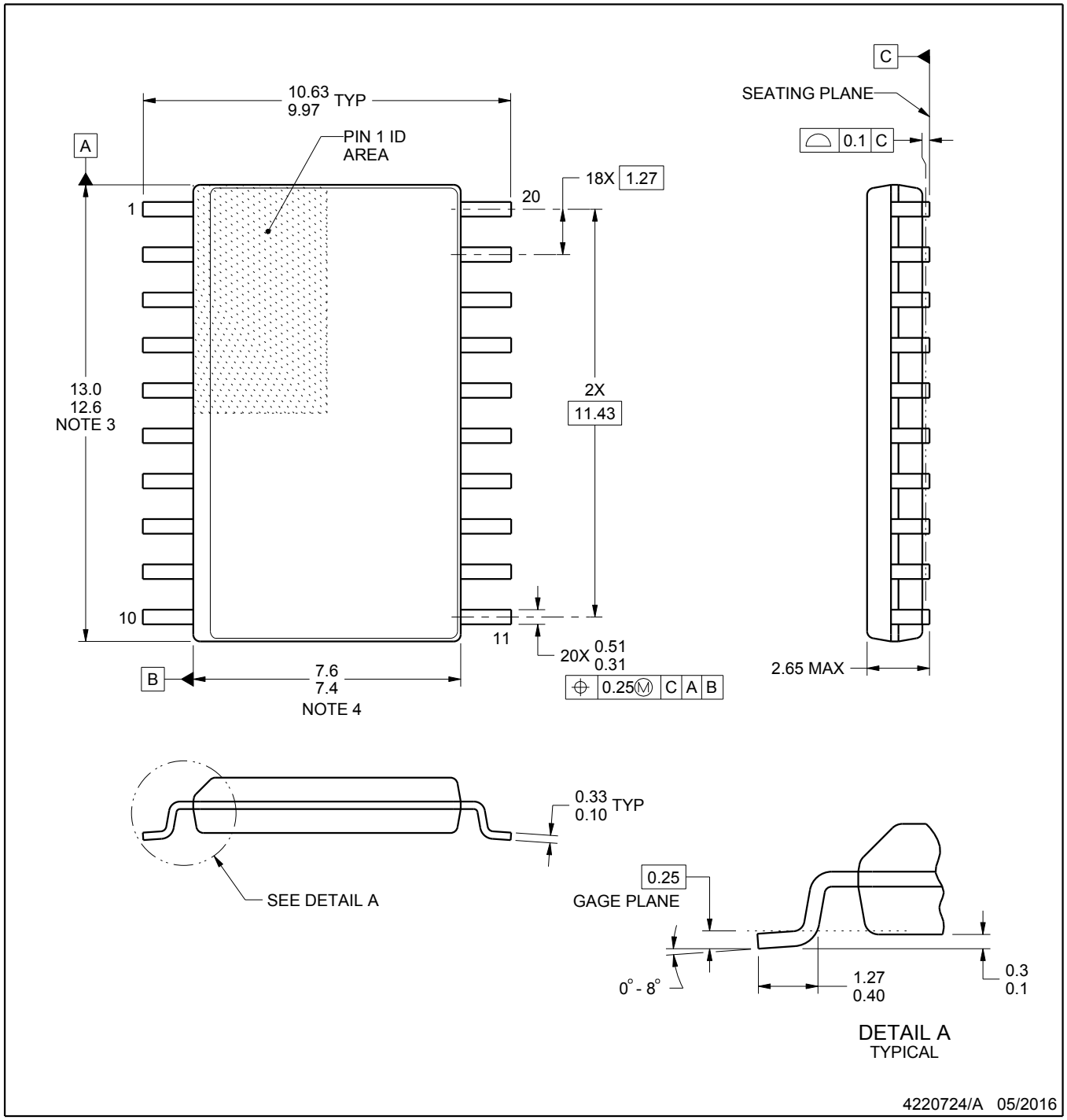


PACKAGE OUTLINE

DW0020A

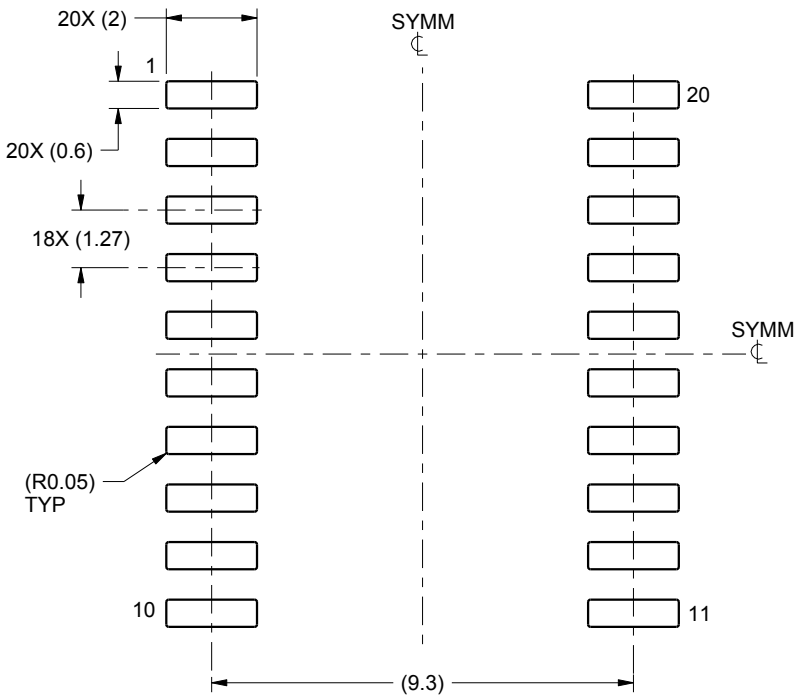
SOIC - 2.65 mm max height

SOIC

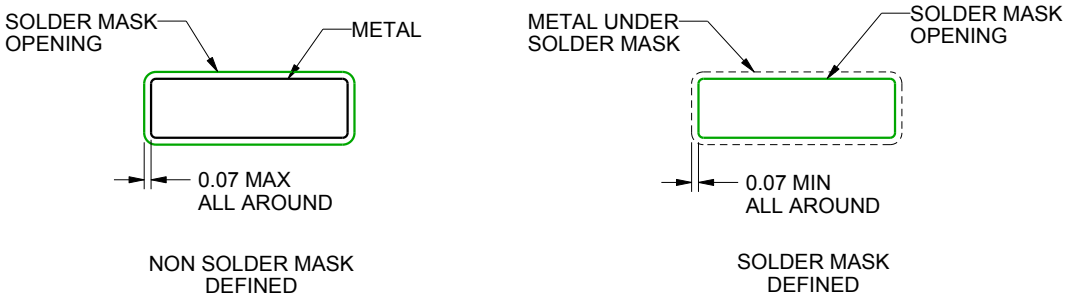


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

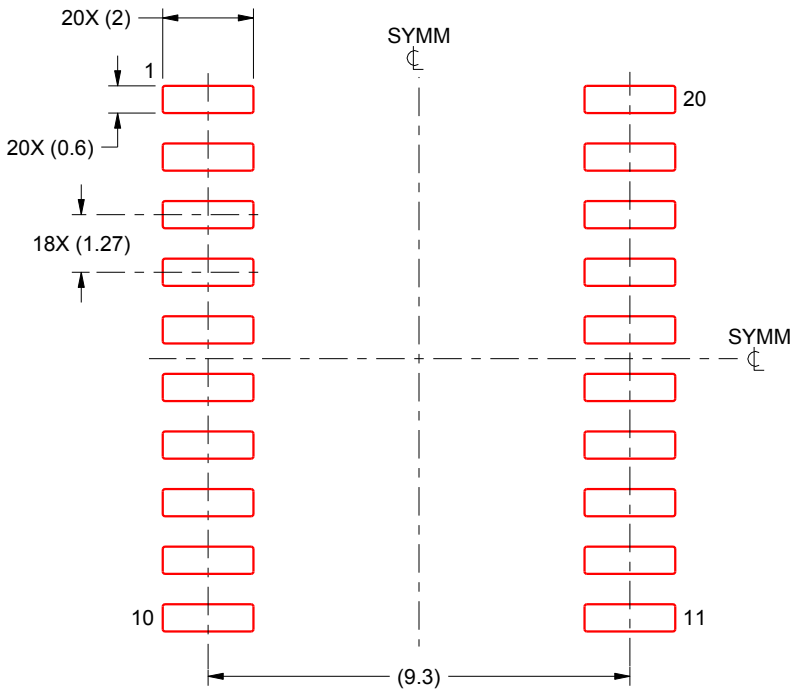


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

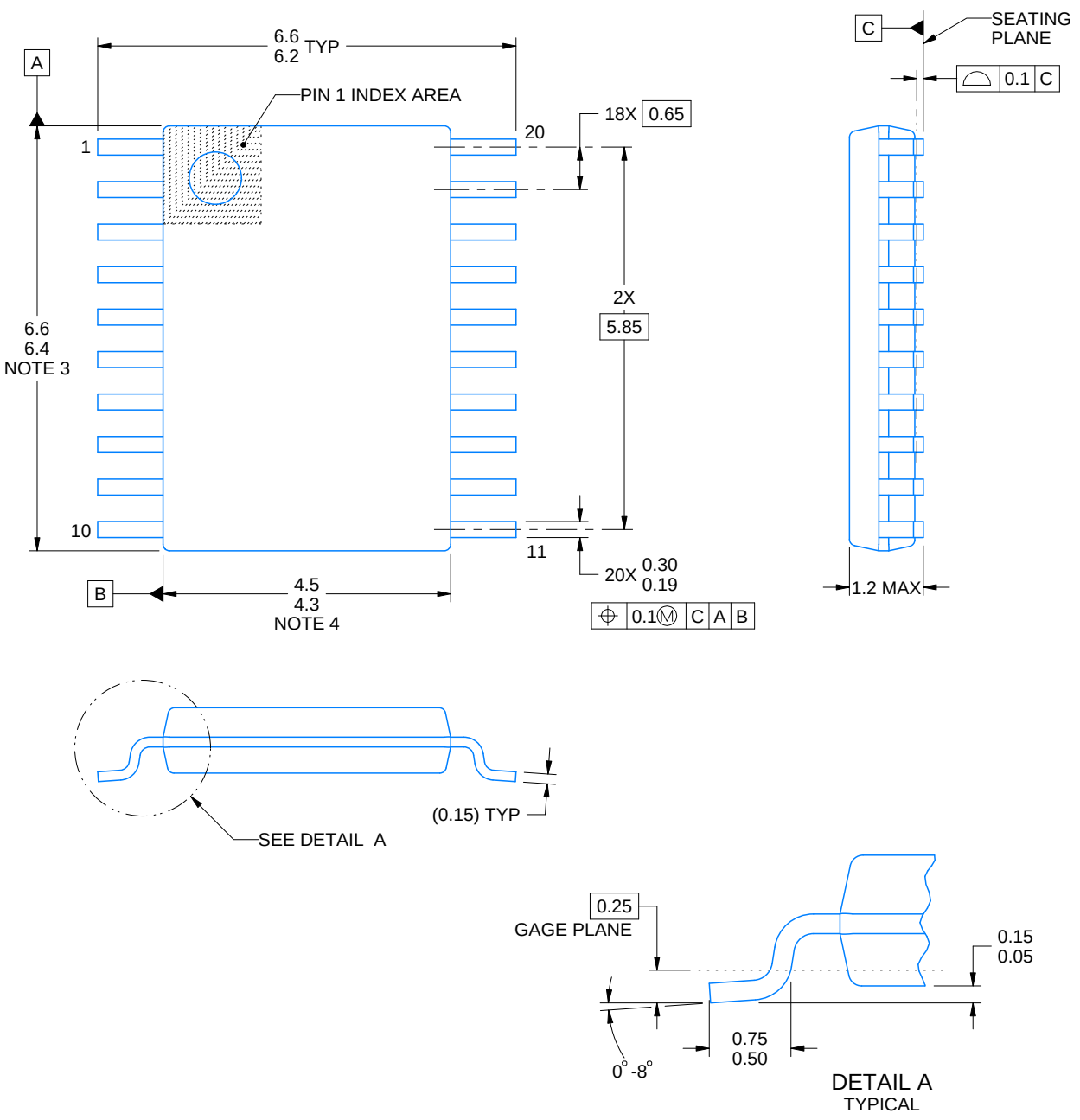
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0020A

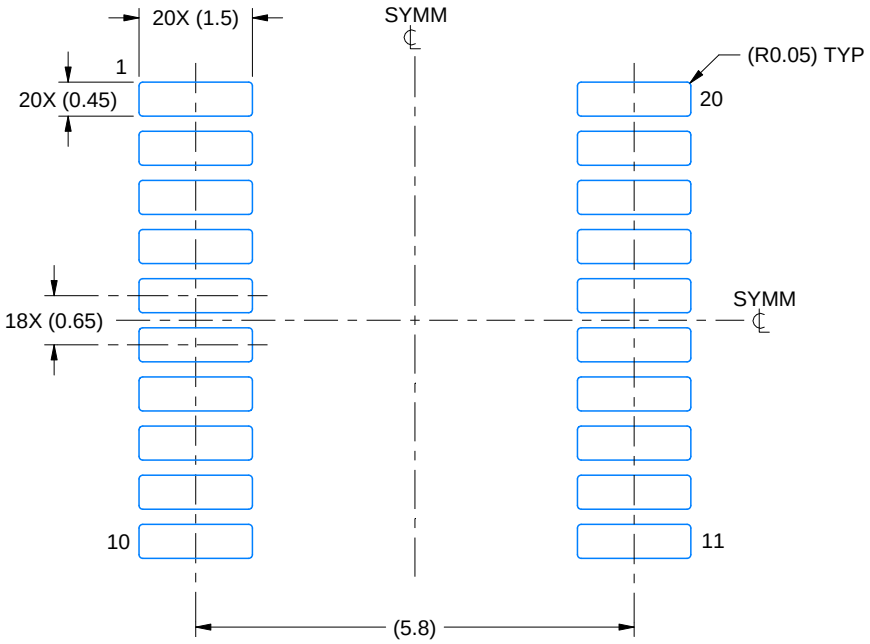
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

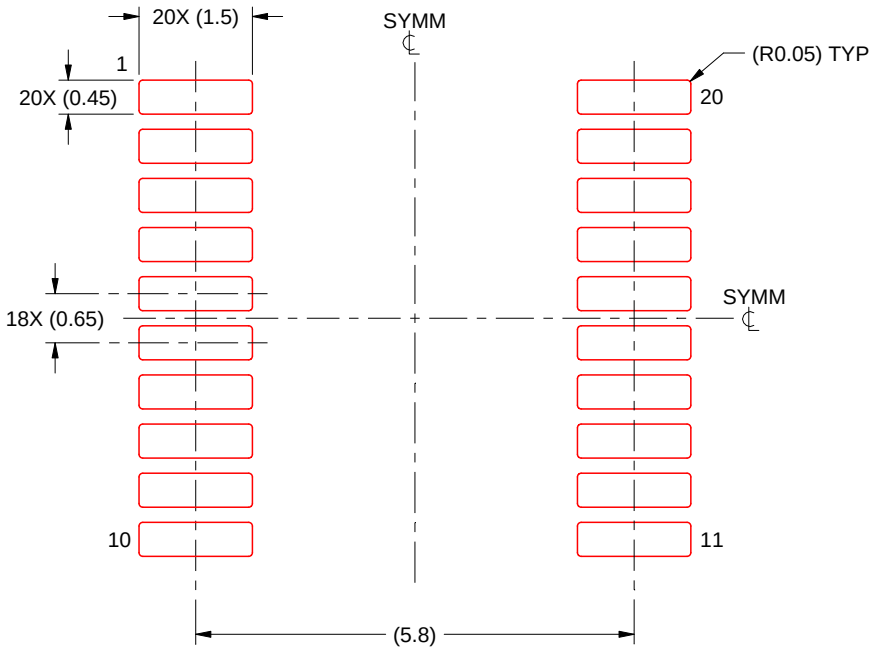


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月