UCC27524A1-Q1 具有负输入电压能力的双路 5A 高速低侧栅极驱动器

1 特性

- 符合汽车应用 要求
- 具有符合 AEC-Q100 标准的下列结果：
  - 器件温度 1 级
  - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 H2
  - 器件组件充电模式 (CDM) ESD 分类等级 C4B
- 工业标准引脚分配
- 两个独立的栅极驱动通道
- 5A 峰值驱动源电流和灌电流
- 针对每个输出的独立支持功能
- 与电源电压无关的 TTL 和 CMOS 兼容逻辑阈值
- 针对高噪声抗扰度的滞后逻辑阈值
- 在输入端处理负电压 (-5V) 的能力
- 输入和允许引脚电压电平不受 V_{DD} 引脚偏置电源电压的限制
- 4.5V 至 18V 单电源供电范围
- V_{DD} 欠压闭锁 (UVLO) 期间输出保持低电平（确保加电和掉电时的无干扰运行）
- 快速传播延迟（典型值 13ns）
- 快速上升和下降时间（典型值 7ns 和 6ns）
- 两通道间的延迟匹配时间典型值为 1ns
- 能够并联两个高驱动电流输出
- 当输入浮动时，输出保持低电平
- MSOP-8 PowerPad™封装
- -40°C 至 +140°C 的运行温度范围

2 应用

- 汽车
- 开关模式电源
- 直流到直流转换器
- 电机控制，太阳能
- 用于诸如 GaN 等新兴宽带隙电源器件的栅极驱动

3 说明

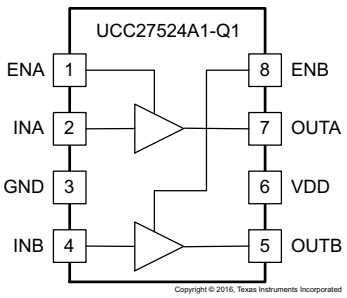
UCC27524A1-Q1 器件是一款双通道、高速、低侧栅极驱动器器件，能够高效地驱动金属氧化物半导体场效应晶体管 (MOSFET) 和绝缘栅双极型功率管 (IGBT) 电源开关。UCC27524A1-Q1 器件是 UCC2752x 系列的一个型号。为了增加稳定耐用性，UCC27524A1-Q1 器件在输入引脚上增加了直接处理 –5V 电压的能力。UCC27524A1-Q1 器件是一款双路非反相驱动器。UCC27524A1-Q1 器件采用的设计方案可最大程度减少击穿电流，从而为电容负载提供高达 5A 的峰值拉/灌电流脉冲，以及轨到轨驱动能力和极小的传播延迟（典型值为 13ns）。除此之外，此驱动器的特性使得两个通道间的内部传播延迟相匹配，这一特性使得此驱动器非常适合于 诸如 同步整流器等对于双栅极驱动有严格时间设置要求的应用。这还使得两个通道可以并联，以有效地增加电流驱动能力或者使用一个单一输入信号驱动两个并联开关。输入引脚阈值基于 TTL 和 CMOS 兼容低压逻辑，此逻辑是固定的并且与 V_{DD} 电源电压无关。高低阈值间的宽滞后提供出色的抗扰度。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
UCC27524A1-Q1	MSOP-PowerPAD（8）	3.00mm x 3.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

Dual Non-Inverting Inputs



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4 修订历史记录

日期	修订版本	注意
2017 年 4 月	*	初始发行版。

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5 说明 （续）

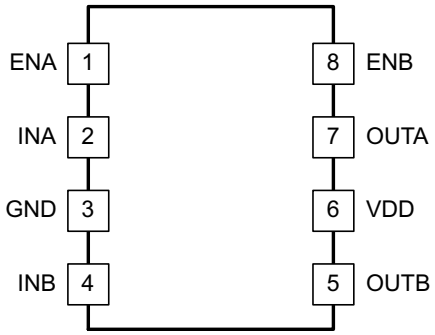
出于保护目的，当输入引脚处于悬空状态时，UCC27524A1-Q1 期间的输入引脚上的内部上拉和下拉电阻器确保输出被保持在低电平。UCC27524A1-Q1 器件 采用 特有使能引脚（ENA 和 ENB）以更好地控制此驱动器的运行 滤波器的理想选择。这些引脚内部上拉至 V_{DD} 电源以实现高电平有效逻辑运行，并且可保持断开连接状态以实现标准运行。

UCC27524A1-Q1 器件采用 MSOP-PowerPAD-8 和暴露焊盘 (DGN) 封装。

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6 Pin Configuration and Functions

DGN Package
8-Pin MSOP-PowerPAD
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ENA	1	I	Enable input for Channel A: ENA is biased LOW to disable the Channel A output regardless of the INA state. ENA is biased HIGH or left floating to enable the Channel A output. ENA is allowed to float; hence the pin-to-pin compatibility with the UCC2732X N/C pin.
ENB	8	I	Enable input for Channel B: ENB is biased LOW to disables the Channel B output regardless of the INB state. ENB is biased HIGH or left floating to enable Channel B output. ENB is allowed to float hence; the pin-to-pin compatibility with the UCC2752A N/C pin.
GND	3	-	Ground: All signals are referenced to this pin.
INA	2	I	Input to Channel A: INA is the non-inverting input in the UCC27524A1-Q1 device. OUTA is held LOW if INA is unbiased or floating.
INB	4	I	Input to Channel B: INB is the non-inverting input in the UCC27524A1-Q1 device. OUTB is held LOW if INB is unbiased or floating.
OUTA	7	O	Output of Channel A
OUTB	5	O	Output of Channel B
VDD	6	I	Bias supply input

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	VDD	–0.3	20	V
OUTA, OUTB voltage	DC	–0.3	VDD + 0.3	V
	Repetitive pulse < 200 ns(2)	–2	VDD + 0.3	V
Output continuous source/sink current	I_{OUT_DC}		0.3	A
Output pulsed source/sink current (0.5 µs)	I_{OUT_pulsed}		5	A
INA, INB, ENA, ENB voltage(3)		–5	20	V
Operating virtual junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Values are verified by characterization on bench.
(3) The maximum voltage on the Input and Enable pins is not restricted by the voltage on the VDD pin.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, VDD	4.5	12	18	V
Operating junction temperature	–40		140	°C
Input voltage, INA, INB	–2		18	V
Enable voltage, ENA and ENB	–2		18	V

7.4 Thermal Information

THERMAL METRIC(1)		UCC27524A1-Q1 HVSSOP (DGN) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	71.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	19.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

V_{DD} = 12 V, T_A = T_J = –40 °C to 140 °C, 1-µF capacitor from V_{DD} to GND. Currents are positive into, negative out of the specified terminal (unless otherwise noted,)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS CURRENTS						
$I_{DD(off)}$	Startup current, (based on UCC27524 Input configuration)	VDD = 3.4 V, INA = VDD, INB = VDD	55	110	175	µA
		VDD = 3.4 V, INA = GND, INB = GND	25	75	145	
UNDER VOLTAGE LOCKOUT (UVLO)						
V_{ON}	Supply start threshold	T_J = 25 °C	3.91	4.2	4.5	V
		T_J = –40 °C to 140 °C	3.7	4.2	4.65	
V_{OFF}	Minimum operating voltage after supply start		3.4	3.9	4.4	V
VDD_H	Supply voltage hysteresis		0.2	0.3	0.5	V
INPUTS (INA, INB, INA+, INA–, INB+, INB–), UCC27524A1-Q1 (DGN)						
V_{IN_H}	Input signal high threshold	Output high for non-inverting input pins Output low for inverting input pins	1.9	2.1	2.3	V
V_{IN_L}	Input signal low threshold	Output low for non-inverting input pins Output high for inverting input pins	1	1.2	1.4	V
V_{IN_HYS}	Input hysteresis		0.7	0.9	1.1	V
OUTPUTS (OUTA, OUTB)						
$I_{SNK/SRC}$	Sink/source peak current(1)	C_{LOAD} = 0.22 µF, F_{SW} = 1 kHz		±5		A
V_{DD}-V_{OH}	High output voltage	I_{OUT} = –10 mA			0.075	V
V_{OL}	Low output voltage	I_{OUT} = 10 mA			0.01	V
R_{OH}	Output pullup resistance(2)	I_{OUT} = –10 mA	2.5	5	7.5	Ω
R_{OL}	Output pulldown resistance	I_{OUT} = 10 mA	0.15	0.5	1	Ω

(1) Ensured by design.
(2) R_{OH} represents on-resistance of only the P-Channel MOSFET device in the pullup structure of the UCC27524A1-Q1 output stage.

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Rise time(1)	C_{LOAD} = 1.8 nF		7	18	ns
t_F	Fall time(1)	C_{LOAD} = 1.8 nF		6	10	ns
t_M	Delay matching between 2 channels	INA = INB, OUTA and OUTB at 50% transition point		1	4	ns
t_{PW}	Minimum input pulse width that changes the output state			15	25	ns
t_{D1}, t_{D2}	Input to output propagation delay(1)	C_{LOAD} = 1.8 nF, 5-V input pulse	6	13	23	ns
t_{D3}, t_{D4}	EN to output propagation delay(1)	C_{LOAD} = 1.8 nF, 5-V enable pulse	6	13	23	ns

(1) See the timing diagrams in Figure 1 and Figure 2

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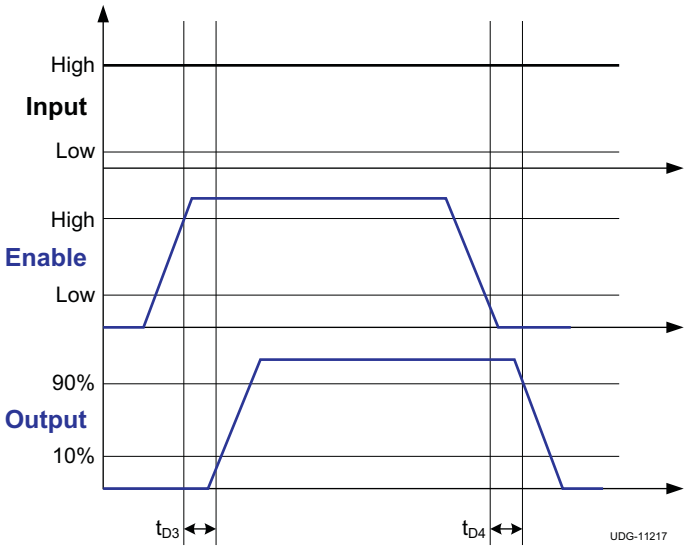


Figure 1. Enable Function

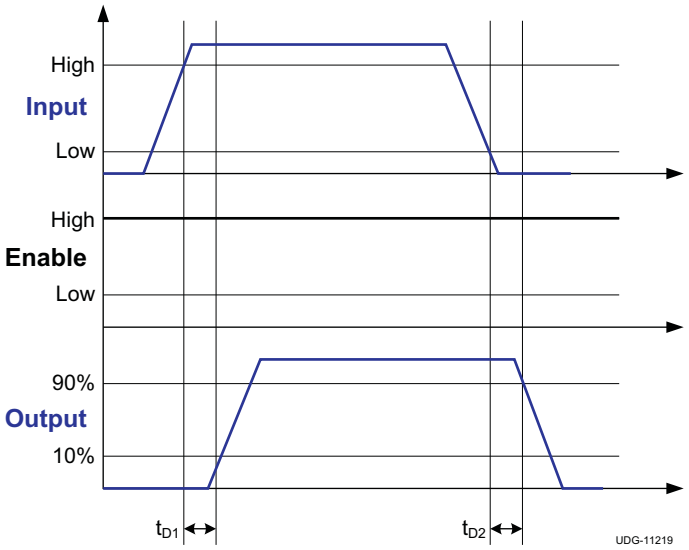


Figure 2. Input-Output Operation

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7.7 Typical Characteristics

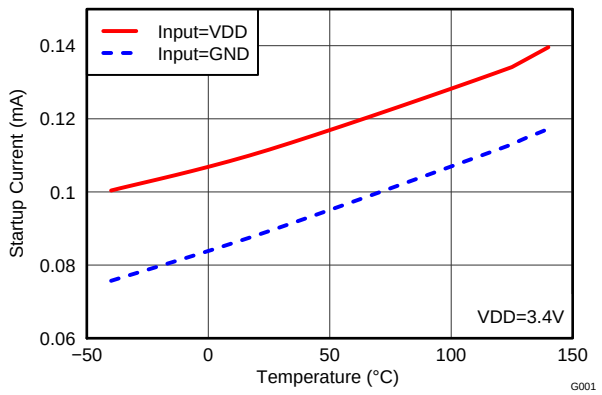


Figure 3. Start-Up Current vs Temperature

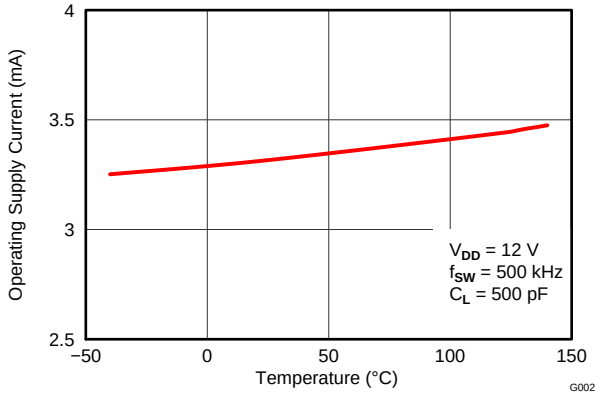


Figure 4. Operating Supply Current vs Temperature (Outputs Switching)

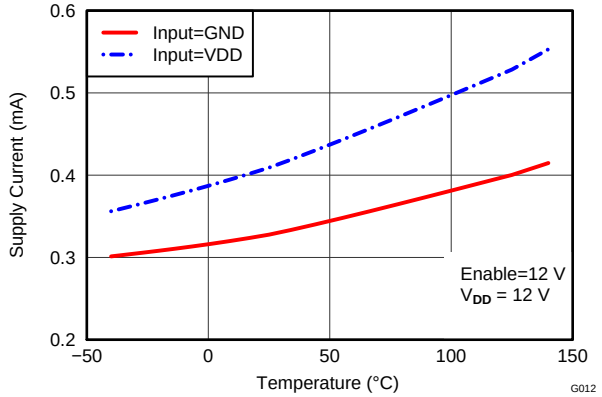


Figure 5. Supply Current vs Temperature (Outputs In DC On/Off Condition)

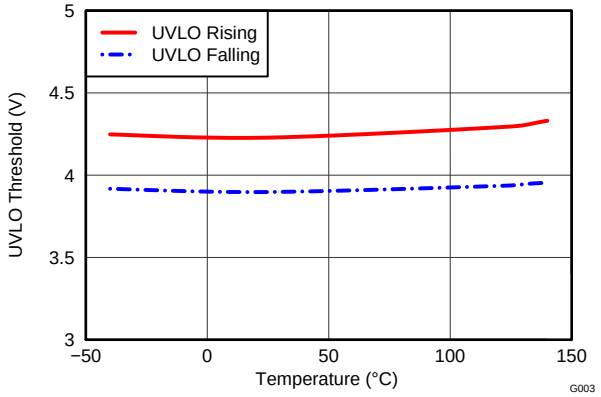


Figure 6. UVLO Threshold vs Temperature

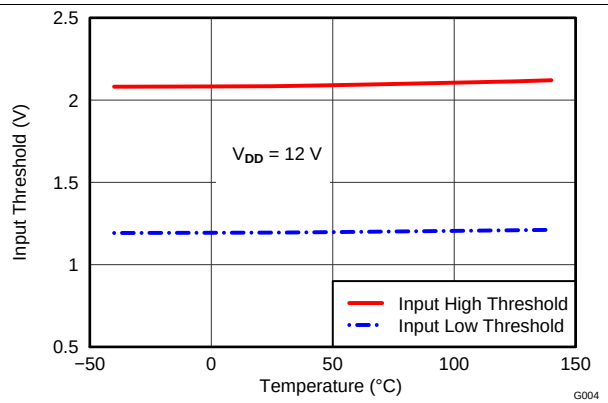


Figure 7. Input Threshold vs Temperature

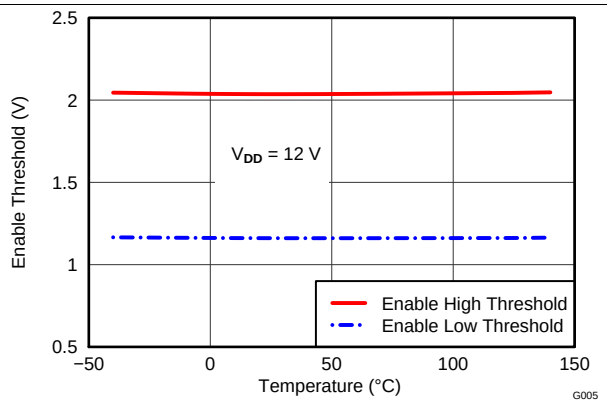


Figure 8. Enable Threshold vs Temperature

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Typical Characteristics (continued)

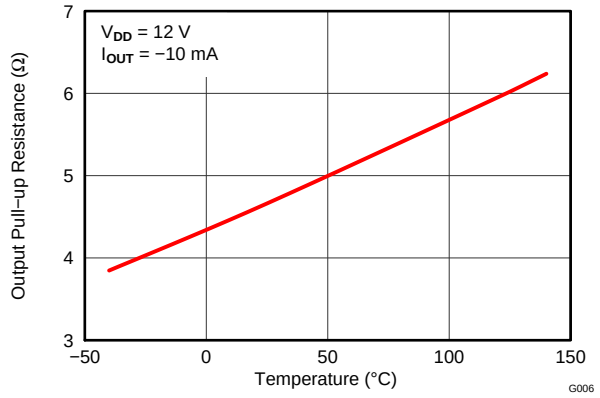


Figure 9. Output Pullup Resistance vs Temperature

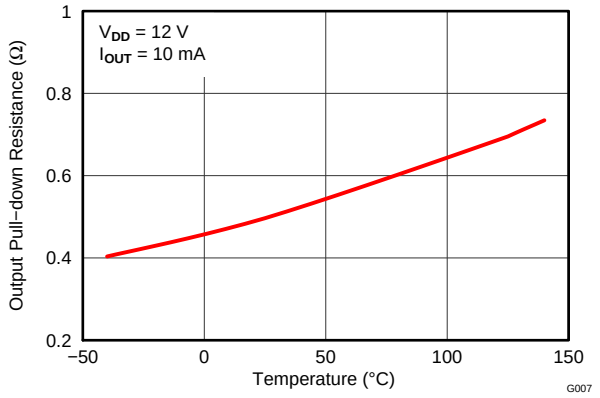


Figure 10. Output Pulldown Resistance vs Temperature

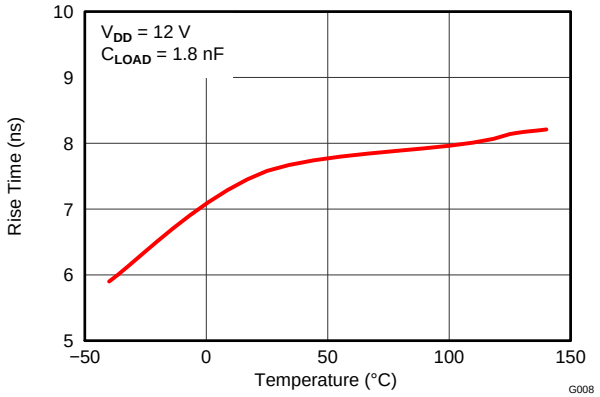


Figure 11. Rise Time vs Temperature

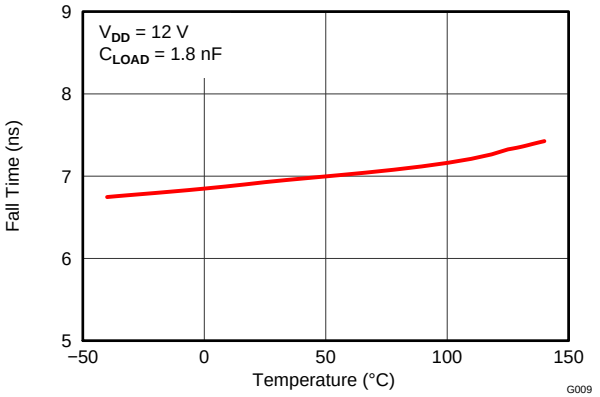


Figure 12. Fall Time vs Temperature

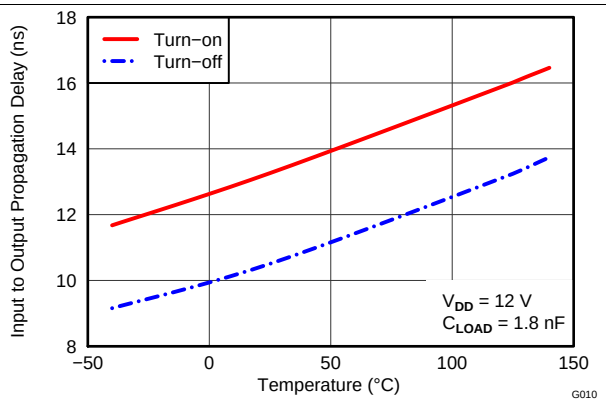


Figure 13. Input to Output Propagation Delay vs Temperature

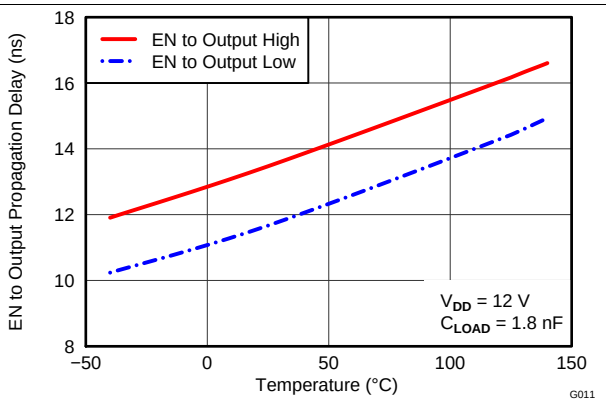


Figure 14. En to Output Propagation Delay vs Temperature

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Typical Characteristics (continued)

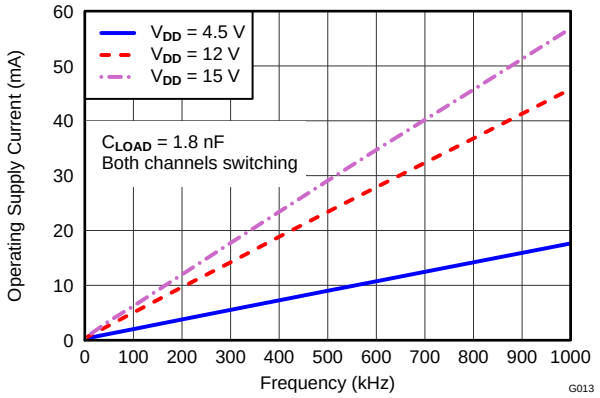


Figure 15. Operating Supply Current vs Frequency

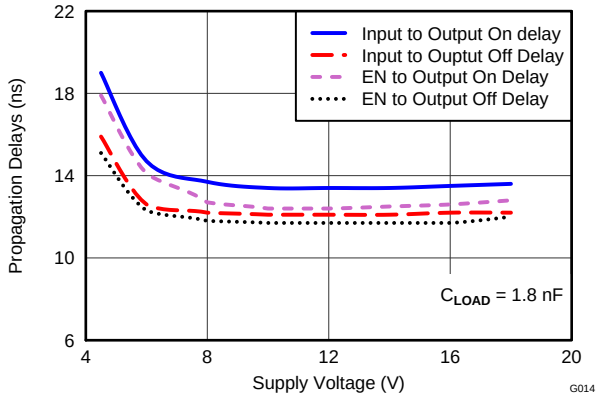


Figure 16. Propagation Delays vs Supply Voltage

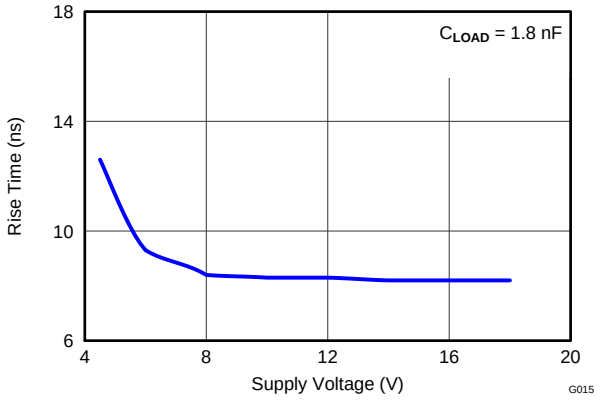


Figure 17. Rise Time vs Supply Voltage

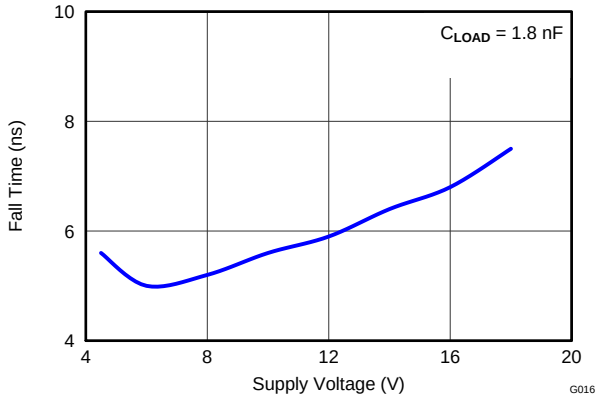


Figure 18. Fall Time vs Supply Voltage

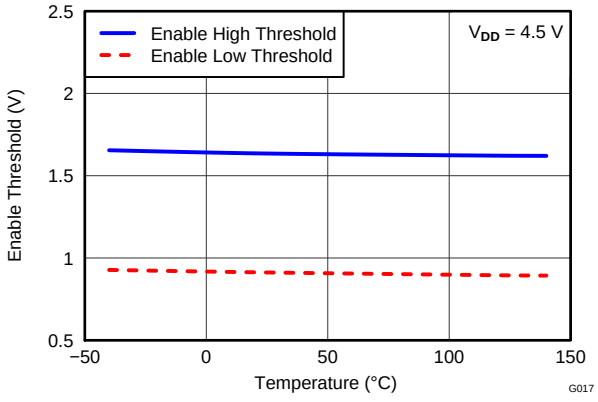


Figure 19. Enable Threshold vs Temperature

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8 Detailed Description

8.1 Overview

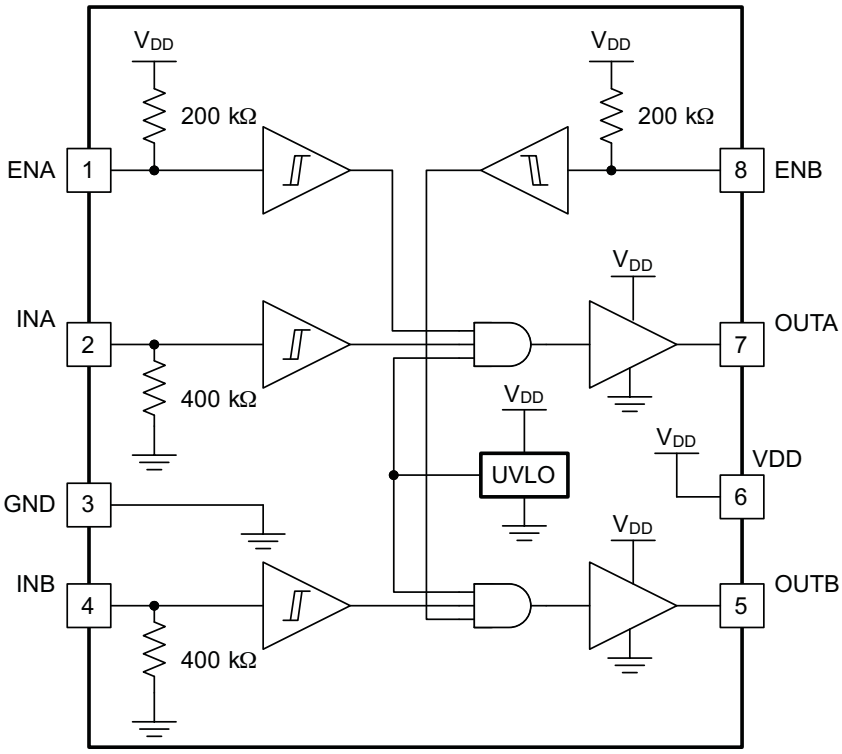
The UCC27524A1-Q1 device represents Texas Instruments' latest generation of dual-channel, low-side, high-speed, gate-driver devices featuring a 5-A source and sink current capability, industry best-in-class switching characteristics, and a host of other features listed in Table 1 all of which combine to ensure efficient, robust, and reliable operation in high-frequency switching power circuits.

Table 1. UCC27524A1-Q1 Features and Benefits

FEATURE	BENEFIT
Best-in-class 13-ns (typ) propagation delay	Extremely low-pulse transmission distortion
1-ns (typ) delay matching between channels	Ease of paralleling outputs for higher (2 times) current capability, ease of driving parallel-power switches
Expanded VDD Operating range of 4.5 to 18 V	Flexibility in system design
Expanded operating temperature range of –40 °C to +140 °C (See *Electrical Characteristics* table)	Flexibility in system design
VDD UVLO Protection	Outputs are held Low in UVLO condition, which ensures predictable, glitch-free operation at power-up and power-down
Outputs held Low when input pins (INx) in floating condition	Protection feature, especially useful in passing abnormal condition tests during safety certification
Outputs enable when enable pins (ENx) in floating condition	Pin-to-pin compatibility with the UCC27324 device from Texas Instruments, in designs where Pin 1 and Pin 8 are in floating condition
CMOS/TTL compatible input and enable threshold with wide hysteresis	Enhanced noise immunity, while retaining compatibility with microcontroller logic-level input signals (3.3 V, 5 V) optimized for digital power
Ability of input and enable pins to handle voltage levels not restricted by VDD pin bias voltage	System simplification, especially related to auxiliary bias supply architecture
Ability to handle –5 V_{DC} (max) at input pins	Increased robustness in noisy environments

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8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Supply Current

The UCC27524A1-Q1 devices feature very low quiescent I_{DD} currents. The typical operating-supply current in UVLO state and fully-on state (under static and switching conditions) are summarized in Figure 3, Figure 4, and Figure 5. The I_{DD} current when the device is fully on and outputs are in a static state (DC high or DC low, see Figure 4) represents lowest quiescent I_{DD} current when all the internal logic circuits of the device are fully operational. The total supply current is the sum of the quiescent I_{DD} current, the average I_{OUT} current because of switching, and finally any current related to pullup resistors on the enable pins (see *Functional Block Diagram*). Knowing the operating frequency (f_{SW}) and the MOSFET gate (Q_G) charge at the drive voltage being used, the average I_{OUT} current can be calculated as product of Q_G and f_{SW}.

A complete characterization of the I_{DD} current as a function of switching frequency at different V_{DD} bias voltages under 1.8-nF switching load in both channels is provided in Figure 15. The strikingly linear variation and close correlation with theoretical value of average I_{OUT} indicates negligible shoot-through inside the gate-driver device attesting to its high-speed characteristics.

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Feature Description (continued)

8.3.2 Input Stage

The input pins of the UCC27524A1-Q1 gate-driver devices are based on a TTL and CMOS compatible input-threshold logic that is independent of the VDD supply voltage. With typically high threshold = 2.1 V and typically low threshold = 1.2 V, the logic level thresholds are conveniently driven with PWM control signals derived from 3.3-V and 5-V digital power-controller devices. Wider hysteresis (typ 0.9 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. UCC27524A1-Q1 devices also feature tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature (refer to Figure 7). The very low input capacitance on these pins reduces loading and increases switching speed.

The UCC27524A1-Q1 device features an important protection feature that holds the output of a channel when the respective pin is in a floating condition. This is achieved using GND pulldown resistors on all of the non-inverting input pins (INA, INB), as shown in the device block diagrams.

The input stage of each driver is driven by a signal with a short rise or fall time. This condition is satisfied in typical power supply applications, where the input signals are provided by a PWM controller or logic gates with fast transition times (<200 ns) with a slow changing input voltage, the output of the driver may switch repeatedly at a high frequency. While the wide hysteresis offered in UCC27524A1-Q1 definitely alleviates this concern over most other TTL input threshold devices, extra care is necessary in these implementations. If limiting the rise or fall times to the power device is the primary goal, then an external resistance is highly recommended between the output of the driver and the power device. This external resistor has the additional benefit of reducing part of the gate-charge related power dissipation in the gate driver device package and transferring it into the external resistor itself.

8.3.3 Enable Function

The enable function is an extremely beneficial feature in gate-driver devices, especially for certain applications such as synchronous rectification where the driver outputs disable in light-load conditions to prevent negative current circulation and to improve light-load efficiency.

The UCC27524A1-Q1 device is equipped with independent enable pins (ENx) for exclusive control of each driver-channel operation. The enable pins are based on a non-inverting configuration (active-high operation). Thus when ENx pins are driven high, the drivers are enabled and when ENx pins are driven low, the drivers are disabled. Like the input pins, the enable pins are also based on a TTL and CMOS compatible, input-threshold logic that is independent of the supply voltage and are effectively controlled using logic signals from 3.3-V and 5-V microcontrollers. The UCC27524A1-Q1 devices also feature tight control of the enable-function threshold-voltage levels which eases system design considerations and ensures stable operation across temperature (refer to Figure 8). The ENx pins are internally pulled up to VDD using pullup resistors as a result of which the outputs of the device are enabled in the default state. Hence the ENx pins are left floating or Not Connected (N/C) for standard operation, where the enable feature is not needed. Essentially, this floating allows the UCC27524A1-Q1 device to be pin-to-pin compatible with TI's previous generation of drivers (UCC27323, UCC27324, and UCC27325 respectively), where Pin 1 and Pin 8 are N/C pins. If the channel A and Channel B inputs and outputs are connected in parallel to increase the driver current capacity, ENA and ENB are connected and driven together.

8.3.4 Output Stage

The UCC27524A1-Q1 device output stage features a unique architecture on the pullup structure which delivers the highest peak-source current when it is most needed during the Miller plateau region of the power-switch turnon transition (when the power switch drain or collector voltage experiences dV/dt). The output stage pullup structure features a P-Channel MOSFET and an additional N-Channel MOSFET in parallel. The function of the N-Channel MOSFET is to provide a brief boost in the peak sourcing current enabling fast turnon. This is accomplished by briefly turning-on the N-Channel MOSFET during a narrow instant when the output is changing state from Low to High.

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Feature Description (continued)

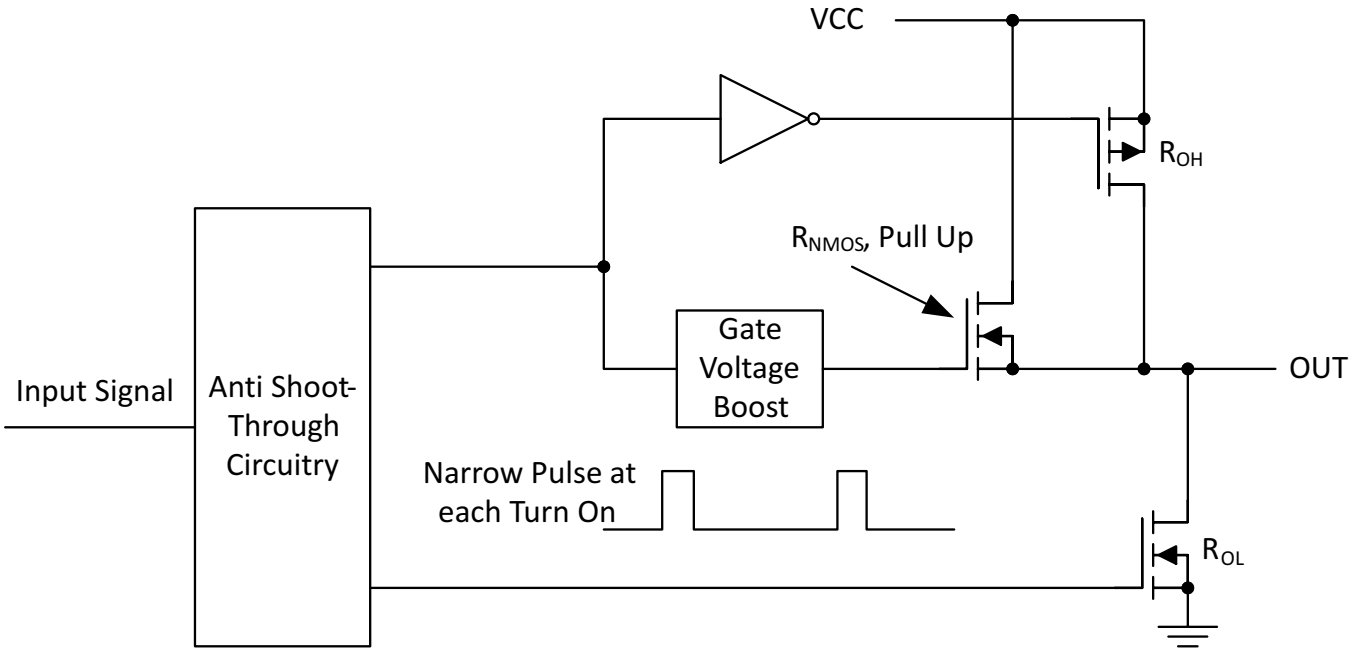


Figure 20. UCC27524A1-Q1 Gate Driver Output Structure

The R_{OH} parameter (see *Electrical Characteristics*) is a DC measurement and it is representative of the on-resistance of the P-Channel device only. This is because the N-Channel device is held in the off state in DC condition and is turned-on only for a narrow instant when output changes state from low to high. Note that effective resistance of the UCC27524A1-Q1 pullup stage during the turnon instant is much lower than what is represented by R_{OH} parameter.

The pulldown structure in the UCC27524A1-Q1 device is simply composed of a N-Channel MOSFET. The R_{OL} parameter (see *Electrical Characteristics*), which is also a DC measurement, is representative of the impedance of the pulldown stage in the device. In the UCC27524A1-Q1 device, the effective resistance of the hybrid pullup structure during turnon is estimated to be approximately 1.5 × R_{OL}, estimated based on design considerations.

Each output stage in the UCC27524A1-Q1 device is capable of supplying 5-A peak source and 5-A peak sink current pulses. The output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the MOS-output stage which delivers very low drop-out. The presence of the MOSFET-body diodes also offers low impedance to switching overshoots and undershoots which means that in many cases, external Schottky-diode clamps may be eliminated. The outputs of these drivers are designed to withstand 500-mA reverse current without either damage to the device or logic malfunction.

The UCC27524A1-Q1 device is particularly suited for dual-polarity, symmetrical drive-gate transformer applications where the primary winding of transformer driven by OUTA and OUTB, with inputs INA and INB being driven complementary to each other. This situation is because of the extremely low drop-out offered by the MOS output stage of these devices, both during high (V_{OH}) and low (V_{OL}) states along with the low impedance of the driver output stage, all of which allow alleviate concerns regarding transformer demagnetization and flux imbalance. The low propagation delays also ensure accurate reset for high-frequency applications.

For applications that have zero voltage switching during power MOSFET turnon or turnoff interval, the driver supplies high-peak current for fast switching even though the miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before power MOSFET is switched on.

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Feature Description (continued)

8.3.5 Low Propagation Delays And Tightly Matched Outputs

The UCC27524A1-Q1 driver device features a best in class, 13-ns (typical) propagation delay between input and output which goes to offer the lowest level of pulse-transmission distortion available in the industry for high frequency switching applications. For example in synchronous rectifier applications, the SR MOSFETs are driven with very low distortion when a single driver device is used to drive both the SR MOSFETs. Further, the driver devices also feature an extremely accurate, 1-ns (typical) matched internal-propagation delays between the two channels which is beneficial for applications requiring dual gate drives with critical timing. For example in a PFC application, a pair of paralleled MOSFETs can be driven independently using each output channel, which the inputs of both channels are driven by a common control signal from the PFC controller device. In this case the 1-ns delay matching ensures that the paralleled MOSFETs are driven in a simultaneous fashion with the minimum of turnon delay difference. Yet another benefit of the tight matching between the two channels is that the two channels are connected together to effectively increase current drive capability, for example A and B channels may be combined into a single driver by connecting the INA and INB inputs together and the OUTA and OUTB outputs together. Then, a single signal controls the paralleled combination.

Caution must be exercised when directly connecting OUTA and OUTB pins together because there is the possibility that any delay between the two channels during turnon or turnoff may result in shoot-through current conduction as shown in Figure 21. While the two channels are inherently very well matched (4-ns Max propagation delay), note that there may be differences in the input threshold voltage level between the two channels which causes the delay between the two outputs especially when slow dV/dt input signals are employed. The following guidelines are recommended whenever the two driver channels are paralleled using direct connections between OUTA and OUTB along with INA and INB:

- Use very fast dV/dt input signals (20 V/µs or greater) on INA and INB pins to minimize impact of differences in input thresholds causing delays between the channels.
- INA and INB connections must be made as close to the device pins as possible.

Wherever possible, a safe practice would be to add an option in the design to have gate resistors in series with OUTA and OUTB. This allows the option to use 0-Ω resistors for paralleling outputs directly or to add appropriate series resistances to limit shoot-through current, should it become necessary.

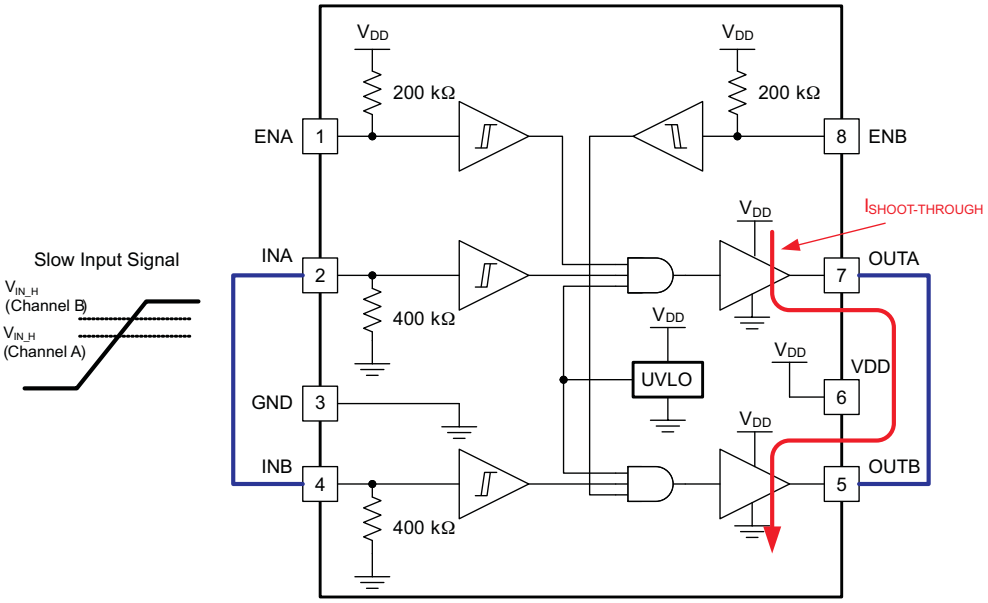


Figure 21. Slow Input Signal Can Cause Shoot-Through Between Channels During Paralleling (Recommended DV/DT is 20 V/Ms or Higher)

Feature Description (continued)

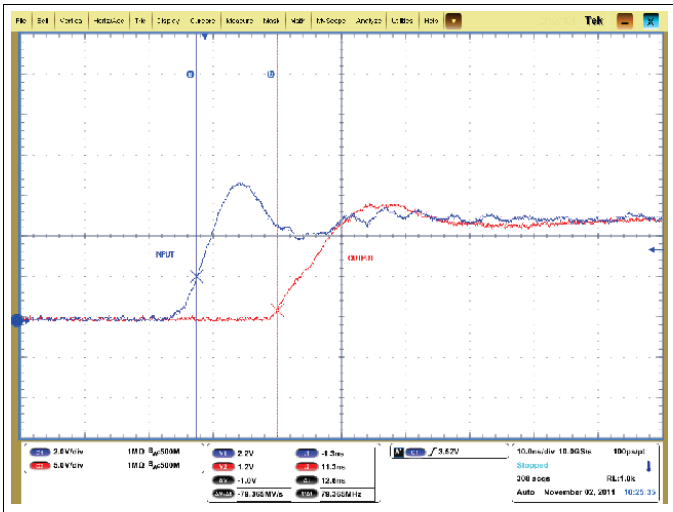


Figure 22. Turnon Propagation Delay (C_L = 1.8 nF, VDD = 12 V)

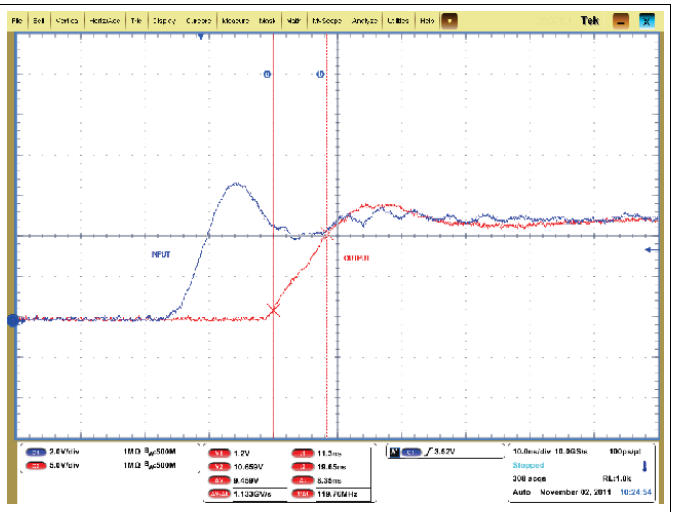


Figure 23. Turnon Rise Time (C_L = 1.8 nF, VDD = 12 V)

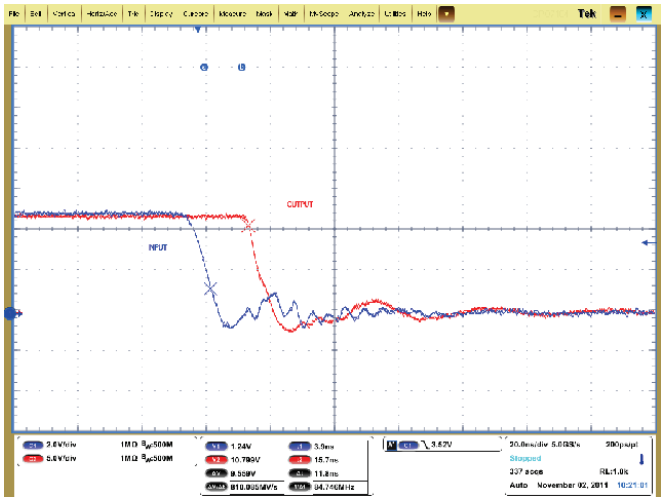


Figure 24. . Turnoff Propagation Delay (C_L = 1.8 nF, VDD = 12 V)

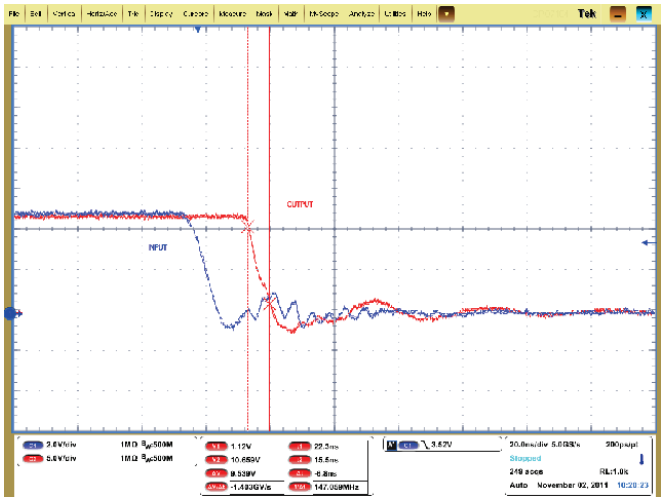


Figure 25. Turnoff Fall Time (C_L = 1.8 nF, VDD = 12 V)

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8.4 Device Functional Modes

Table 2. Device Logic Table

ENA	ENB	INA	INB	UCC27524A1-Q1	
				OUTA	OUTB
H	H	L	L	L	L
H	H	L	H	L	H
H	H	H	L	H	L
H	H	H	H	H	H
L	L	Any	Any	L	L
Any	Any	x(1)	x(1)	L	L
x(1)	x(1)	L	L	L	L
x(1)	x(1)	L	H	L	H
x(1)	x(1)	H	L	H	L
x(1)	x(1)	H	H	H	H

(1) Floating condition.

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9 Application and Implementation

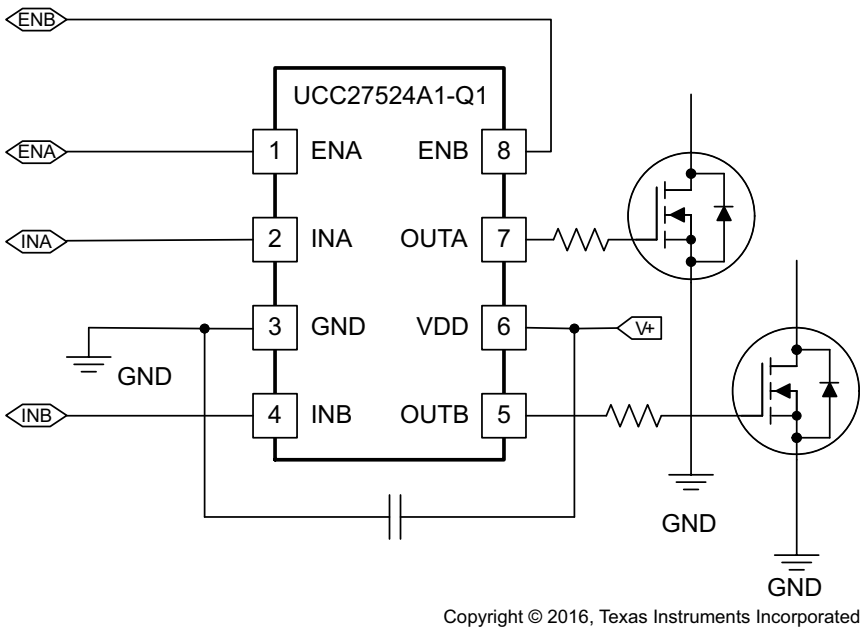
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

High-current gate-driver devices are required in switching power applications for a variety of reasons. In order to effect the fast switching of power devices and reduce associated switching-power losses, a powerful gate-driver device employs between the PWM output of control devices and the gates of the power semiconductor devices. Further, gate-driver devices are indispensable when it is not feasible for the PWM controller device to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which is not capable of effectively turning on a power switch. A level-shifting circuitry is required to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer-drive circuits based on NPN/PNP bipolar transistors in a totem-pole arrangement, as emitter-follower configurations, prove inadequate with digital power because the traditional buffer-drive circuits lack level-shifting capability. Gate-driver devices effectively combine both the level-shifting and buffer-drive functions. Gate-driver devices also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controller devices by moving gate-charge power losses into the controller. Finally, emerging wide band-gap power-device technologies such as GaN based switches, which are capable of supporting very high switching frequency operation, are driving special requirements in terms of gate-drive capability. These requirements include operation at low VDD voltages (5 V or lower), low propagation delays, tight delay matching and availability in compact, low-inductance packages with good thermal capability. In summary, gate-driver devices are an extremely important component in switching power combining benefits of high-performance, low-cost, component-count, board-space reduction, and simplified system design.

9.2 Typical Application



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Figure 26. UCC27524A1-Q1 Typical Application Diagram

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Typical Application (continued)

9.2.1 Design Requirements

When selecting the proper gate driver device for an end application, some desiring considerations must be evaluated first in order to make the most appropriate selection. Among these considerations are VDD, UVLO, Drive current and power dissipation.

9.2.2 Detailed Design Procedure

9.2.2.1 VDD and Undervoltage Lockout

The UCC27524A1-Q1 device has an internal undervoltage-lockout (UVLO) protection feature on the VDD pin supply circuit blocks. When VDD is rising and the level is still below UVLO threshold, this circuit holds the output low, regardless of the status of the inputs. The UVLO is typically 4.25 V with 350-mV typical hysteresis. This hysteresis prevents chatter when low VDD supply voltages have noise from the power supply and also when there are droops in the VDD bias voltage when the system commences switching and there is a sudden increase in I_{DD}. The capability to operate at low voltage levels such as below 5 V, along with best in class switching characteristics, is especially suited for driving emerging GaN power semiconductor devices.

For example, at power up, the UCC27524A1-Q1 driver-device output remains low until the V_{DD} voltage reaches the UVLO threshold if enable pin is active or floating. The magnitude of the OUT signal rises with V_{DD} until steady-state V_{DD} is reached. The operation in Figure 27 shows that the output remains low until the UVLO threshold is reached, and then the output is in-phase with the input.

Because the device draws current from the VDD pin to bias all internal circuits, for the best high-speed circuit performance, two VDD bypass capacitors are recommended to prevent noise problems. The use of surface mount components is highly recommended. A 0.1-μF ceramic capacitor must be located as close as possible to the VDD to GND pins of the gate-driver device. In addition, a larger capacitor (such as 1-μF) with relatively low ESR must be connected in parallel and close proximity, in order to help deliver the high-current peaks required by the load. The parallel combination of capacitors presents a low impedance characteristic for the expected current levels and switching frequencies in the application.

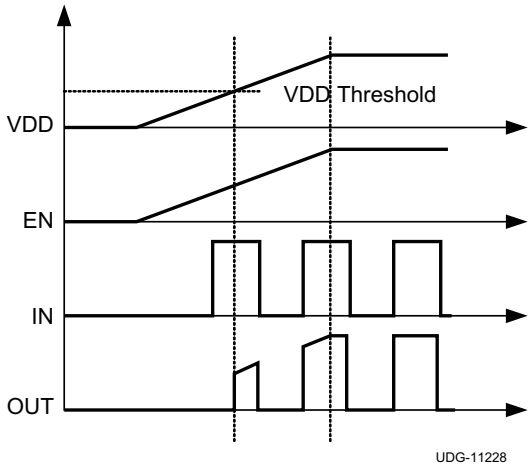


Figure 27. Power-Up Non-Inverting Driver

9.2.2.2 Drive Current and Power Dissipation

The UCC27524A1-Q1 driver is capable of delivering 5-A of current to a MOSFET gate for a period of several-hundred nanoseconds at VDD = 12 V. High peak current is required to turn the device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground which repeats at the operating frequency of the power device. The power dissipated in the gate driver device package depends on the following factors:

- Gate charge required of the power MOSFET (usually a function of the drive voltage V_{GS}, which is very close to input bias supply voltage V_{DD} due to low V_{OH} drop-out)
- Switching frequency

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Typical Application (continued)

- Use of external gate resistors

Because UCC27524A1-Q1 features very low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver can be safely assumed to be negligible.

When a driver device is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly simple. The energy that must be transferred from the bias supply to charge the capacitor is given by Equation 1.

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2 \quad (1)$$

where

- C_{LOAD} is the load capacitor
- V_{DD}^2 is the bias voltage feeding the driver

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Typical Application (continued)

There is an equal amount of energy dissipated when the capacitor is charged. This leads to a total power loss given by Equation 2.

$$P_G = C_{LOAD} V_{DD}^2 f_{SW}$$

where

- f_{SW} is the switching frequency (2)

With V_{DD} = 12 V, C_{LOAD} = 10 nF and f_{SW} = 300 kHz the power loss is calculated with Equation 3.

$$P_G = 10\,nF \times 12\,V^2 \times 300\,kHz = 0.432\,W \quad (3)$$

The switching load presented by a power MOSFET is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, the power that must be dissipated when charging a capacitor is determined which by using the equivalence $Q_g = C_{LOAD} V_{DD}$ to provide Equation 4 for power:

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} = Q_g V_{DD} f_{SW} \quad (4)$$

Assuming that the UCC27524A1-Q1 device is driving power MOSFET with 60 nC of gate charge (Q_g = 60 nC at V_{DD} = 12 V) on each output, the gate charge related power loss is calculated with Equation 5.

$$P_G = 2 \times 60\,nC \times 12\,V \times 300\,kHz = 0.432\,W \quad (5)$$

This power PG is dissipated in the resistive elements of the circuit when the MOSFET turns on or turns off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as follows (see Equation 6):

$$P_{SW} = 0.5 \times Q_G \times VDD \times f_{SW} \times \left(\frac{R_{OFF}}{R_{OFF} + R_{GATE}} + \frac{R_{ON}}{R_{ON} + R_{GATE}} \right)$$

where

- $R_{OFF} = R_{OL}$
- R_{ON} (effective resistance of pullup structure) = 1.5 x R_{OL} (6)

In addition to the above gate-charge related power dissipation, additional dissipation in the driver is related to the power associated with the quiescent bias current consumed by the device to bias all internal circuits such as input stage (with pullup and pulldown resistors), enable, and UVLO sections. As shown in Figure 4, the quiescent current is less than 0.6 mA even in the highest case. The quiescent power dissipation is calculated easily with Equation 7.

$$P_Q = I_{DD} V_{DD} \quad (7)$$

Assuming , I_{DD} = 6 mA, the power loss is:

$$P_Q = 0.6\,mA \times 12\,V = 7.2\,mW \quad (8)$$

Clearly, this power loss is insignificant compared to gate charge related power dissipation calculated earlier.

With a 12-V supply, the bias current is estimated as follows, with an additional 0.6-mA overhead for the quiescent consumption:

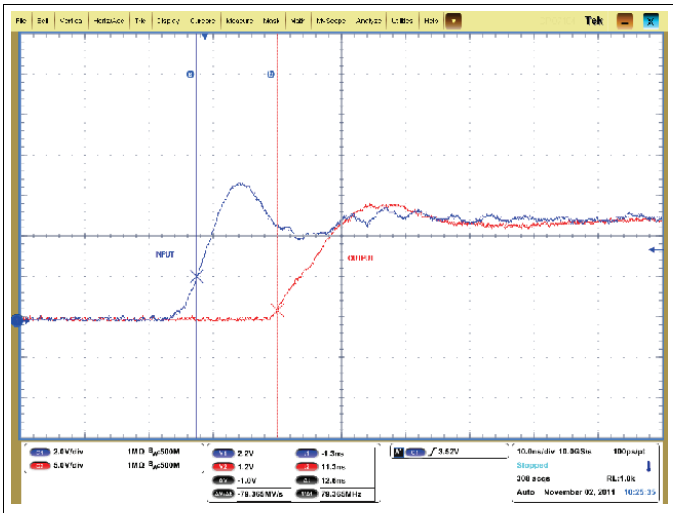
$$I_{DD} \sim \frac{P_G}{V_{DD}} = \frac{0.432\ W}{12\ V} = 0.036\ A \quad (9)$$

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Typical Application (continued)

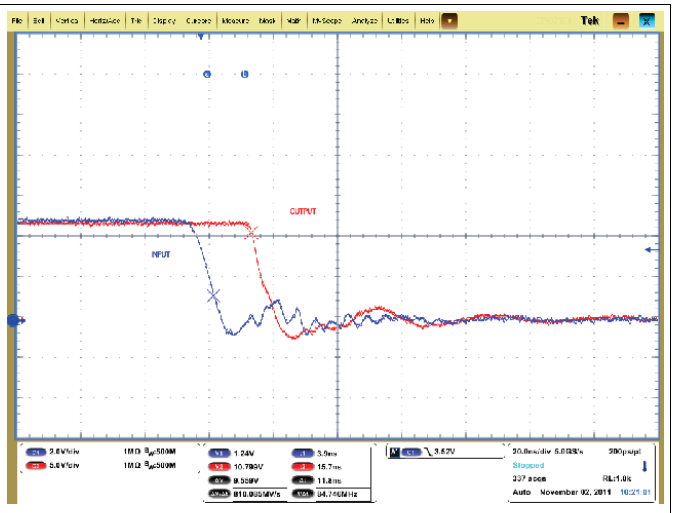
9.2.3 Application Curves

Figure 28 and Figure 29 show the typical switching characteristics of the UCC27524A1-Q1 device.



CL = 1.8 nF, VDD = 12 V

Figure 28. Typical Turnon Waveform



CL = 1.8 nF, VDD = 12 V

Figure 29. Typical Turnoff Waveform

10 Power Supply Recommendations

The bias supply voltage range for which the UCC27524A1-Q1 device is rated to operate is from 4.5 V to 18 V. The lower end of this range is governed by the internal undervoltage-lockout (UVLO) protection feature on the V_{DD} pin supply circuit blocks. Whenever the driver is in UVLO condition when the V_{DD} pin voltage is below the V_{ON} supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20-V absolute maximum voltage rating of the V_{DD} pin of the device (which is a stress rating). Keeping a 2-V margin to allow for transient voltage spikes, the maximum recommended voltage for the V_{DD} pin is 18 V.

The UVLO protection feature also involves a hysteresis function. This means that when the V_{DD} pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification VDD_H. Therefore, ensuring that, while operating at or near the 4.5-V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown. During system shutdown, the device operation continues until the V_{DD} pin voltage has dropped below the V_{OFF} threshold which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system startup, the device does not begin operation until the V_{DD} pin voltage has exceeded above the V_{ON} threshold.

The quiescent current consumed by the internal circuit blocks of the device is supplied through the V_{DD} pin. Although this fact is well known, recognizing that the charge for source current pulses delivered by the OUTA/B pin is also supplied through the same V_{DD} pin is important. As a result, every time a current is sourced out of the output pins, a corresponding current pulse is delivered into the device through the V_{DD} pin. Thus ensuring that local bypass capacitors are provided between the V_{DD} and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low ESR, ceramic surface mount capacitor is a must. TI recommends having 2 capacitors; a 100-nF ceramic surface-mount capacitor which can be nudged very close to the pins of the device and another surface-mount capacitor of few microfarads added in parallel.

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11 Layout

11.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current fast-switching circuit to provide appropriate device operation and design robustness. The UCC27524A1-Q1 gate driver incorporates short propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power MOSFET to facilitate voltage transitions very quickly. At higher V_{DD} voltages, the peak current capability is even higher (5-A peak current is at V_{DD} = 12 V). Very high di/dt causes unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are strongly recommended when designing with these high-speed drivers.

- Locate the driver device as close as possible to power device in order to minimize the length of high-current traces between the output pins and the gate of the power device.
- Locate the V_{DD} bypass capacitors between V_{DD} and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high peak current being drawn from V_{DD} during turnon of power MOSFET. The use of low inductance surface-mounted-device (SMD) components such as chip resistors and chip capacitors is highly recommended.
- The turnon and turnoff current loop paths (driver device, power MOSFET and V_{DD} bypass capacitor) must be minimized as much as possible in order to keep the stray inductance to a minimum. High di/dt is established in these loops at two instances during turnon and turnoff transients which induces significant voltage transients on the output pin of the driver device and Gate of the power MOSFET.
- Wherever possible, parallel the source and return traces to take advantage of flux cancellation
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver is connected to the other circuit nodes such as source of power MOSFET and ground of PWM controller at one, single point. The connected paths must be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well
- Exercise caution when replacing the UCC2732x/UCC2742x devices with the UCC27524A1-Q1 device:
  - The UCC27524A1-Q1 device is a much stronger gate driver (5-A peak current versus 4-A peak current).
  - The UCC27524A1-Q1 device is a much faster gate driver (13-ns/13-ns rise and fall propagation delay versus 25-ns/35-ns rise and fall propagation delay).

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11.2 Layout Example

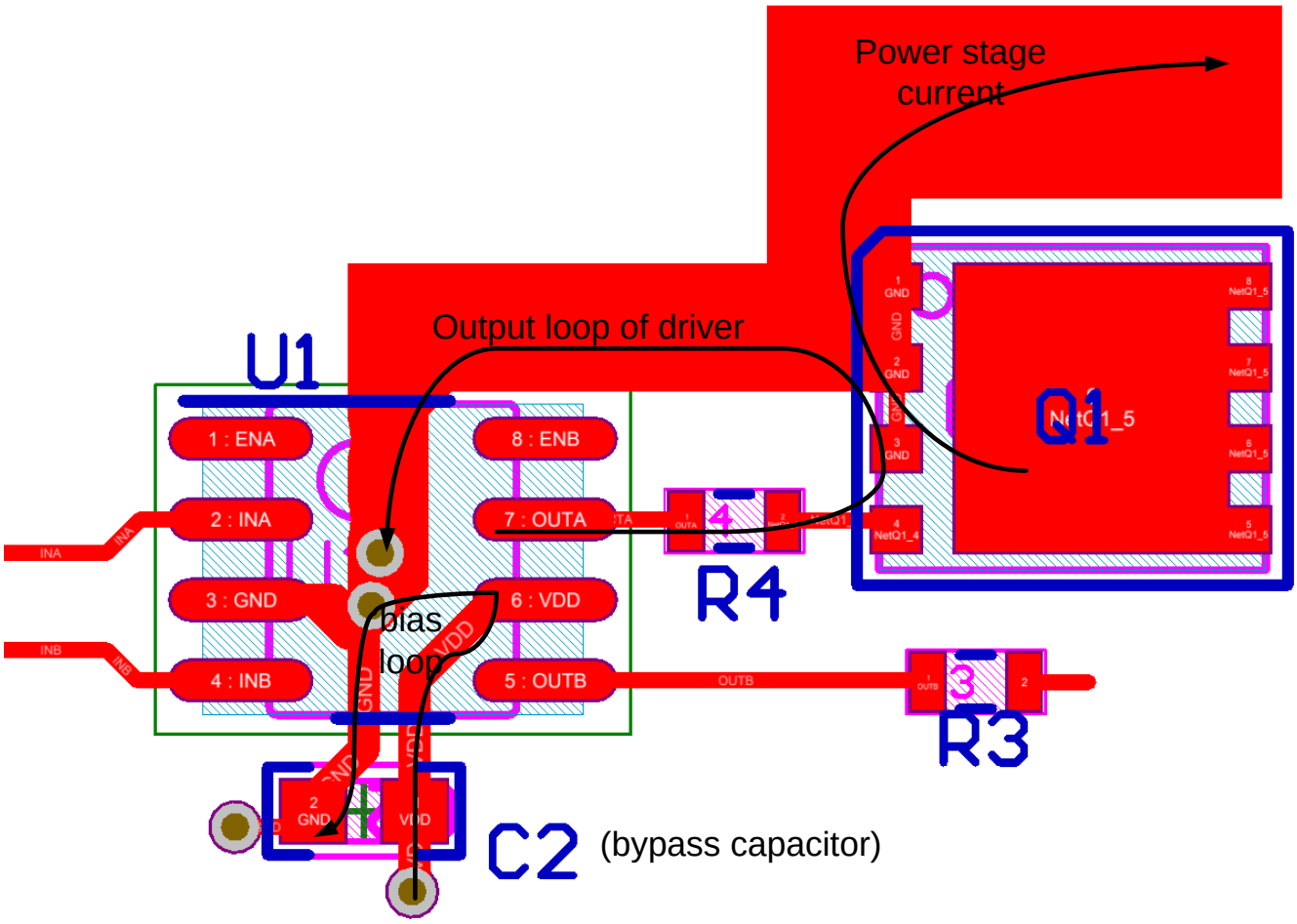


Figure 30. UCC27524A1-Q1 Layout Example

11.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. In order for a gate driver device to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. For detailed information regarding the thermal information table, please refer to Application Note from Texas Instruments entitled, *Semiconductor and IC Package Thermal Metrics* (SPRA953).

Among the different package options available for the UCC27524A1-Q1 device, power dissipation capability of the DGN package is of particular mention. The HVSSOP-8 (DGN) package offers a means of removing the heat from the semiconductor junction through the bottom of the package. This package offers an exposed thermal pad at the base of the package. This pad is soldered to the copper on the printed circuit board directly underneath the device package, reducing the thermal resistance to a very low value. This allows a significant improvement in heat-sinking over that available in the D package. The printed circuit board must be designed with thermal lands and thermal vias to complete the heat removal subsystem. Note that the exposed pads in the HVSSOP-8 package are not directly connected to any leads of the package, however, the PowerPAD is electrically and thermally connected to the substrate of the device which is the ground of the device. TI recommends to externally connect the exposed pads to GND in PCB layout for better EMI immunity.

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12 器件和文档支持

12.1 社区资源

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设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.2 商标

PowerPad, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC27524A1QDGNRQ1	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 140	7524 Q1
UCC27524A1QDGNRQ1.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 140	7524 Q1
UCC27524A1QDGNRQ1.B	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 140	7524 Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

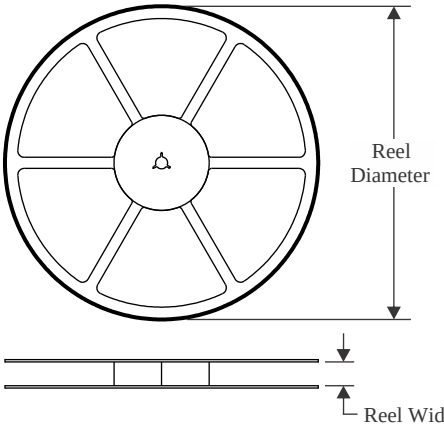
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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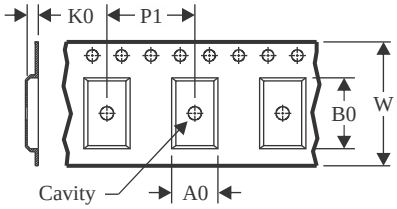
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

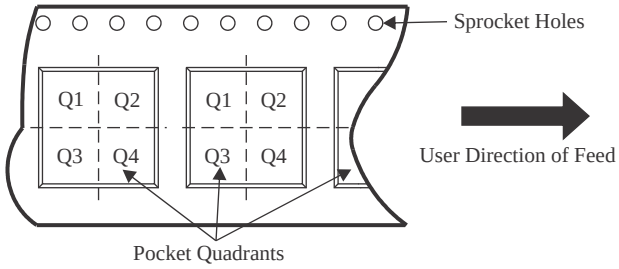


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

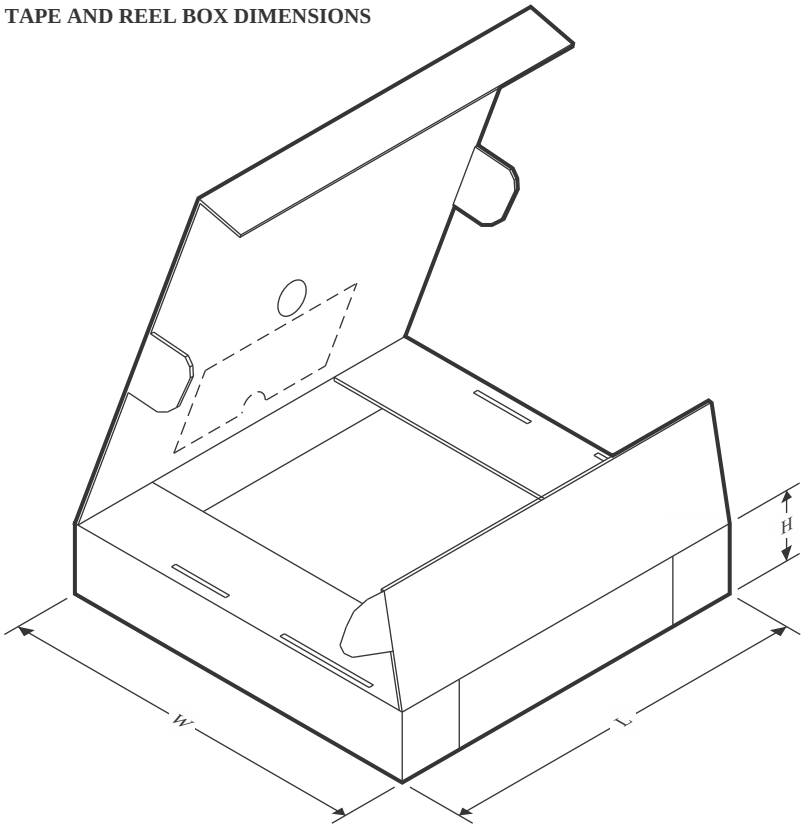
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27524A1QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27524A1QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27524A1QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
UCC27524A1QDGNRQ1	HVSSOP	DGN	8	2500	353.0	353.0	32.0

GENERIC PACKAGE VIEW

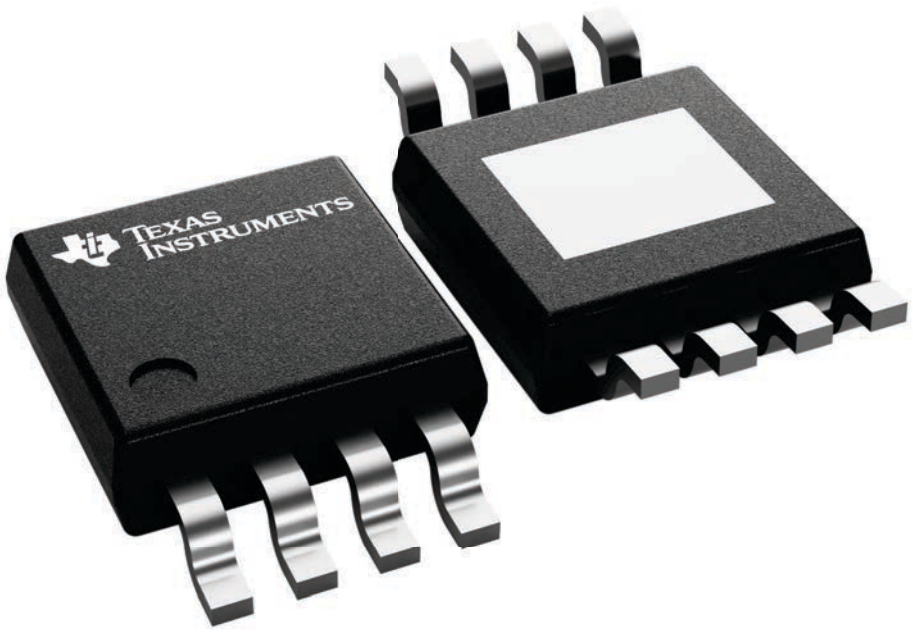
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



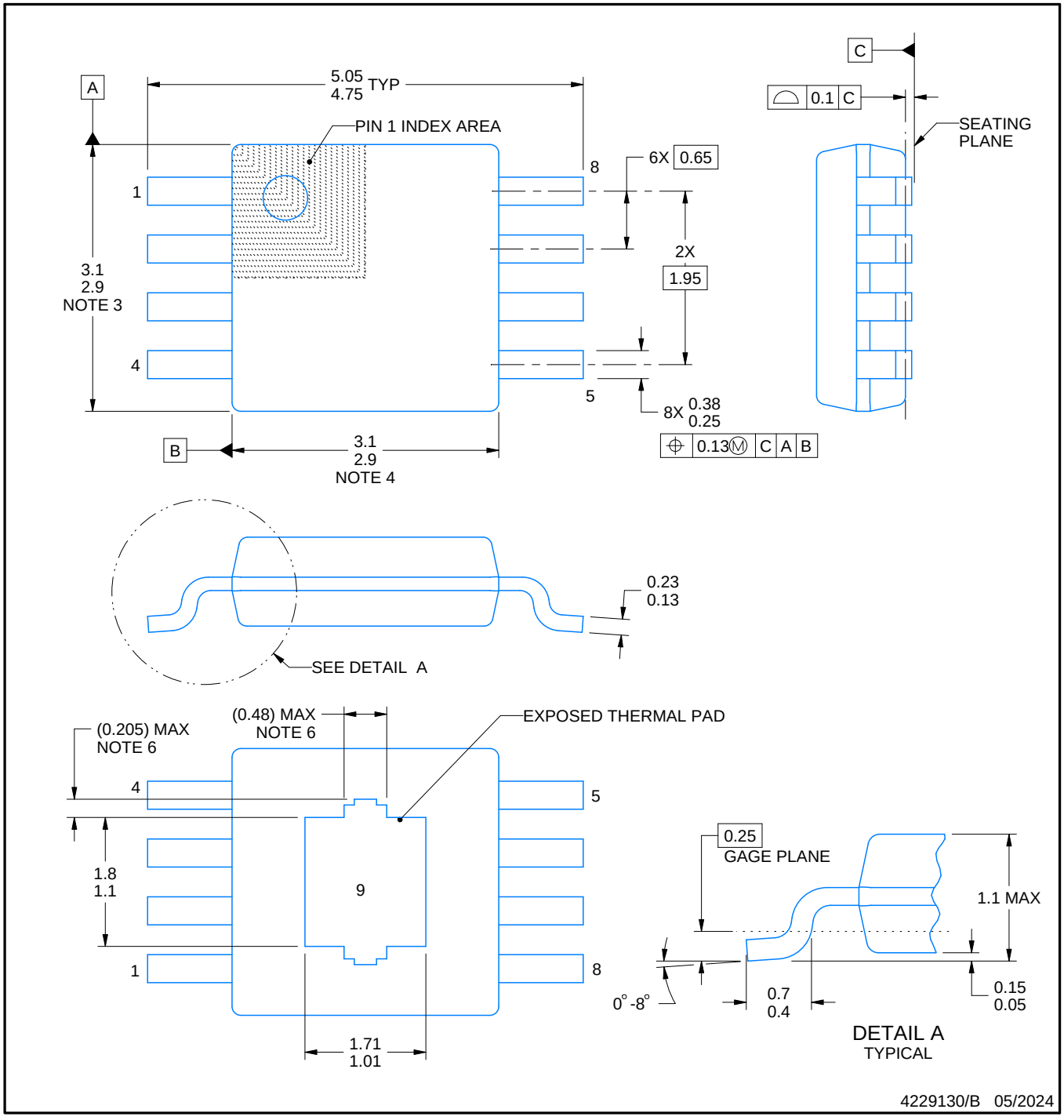
4225482/B

PACKAGE OUTLINE

DGN0008H

PowerPAD™ VSSOP - 1.1 mm max height

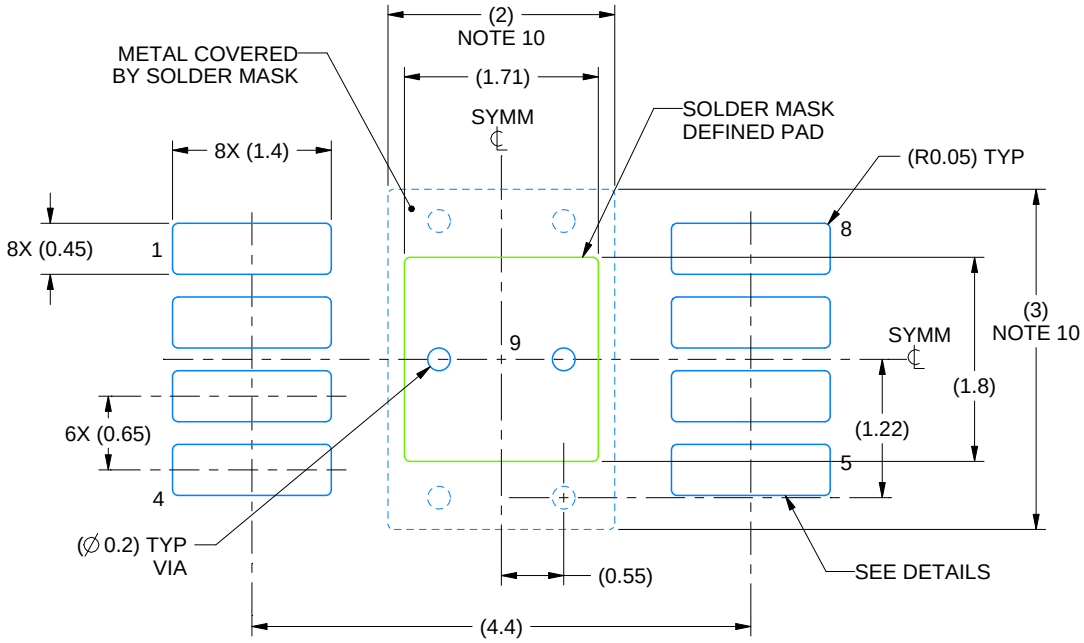
SMALL OUTLINE PACKAGE



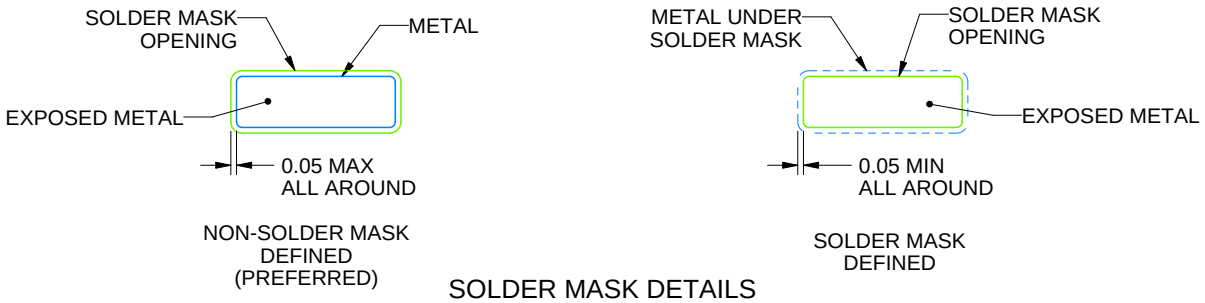
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

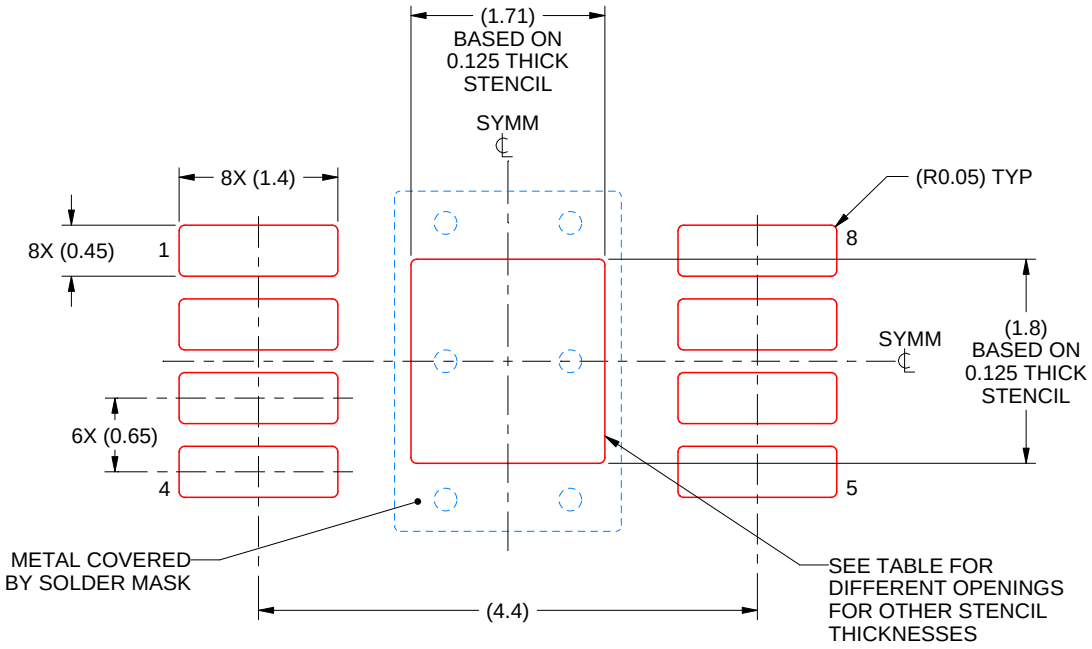


SOLDER MASK DETAILS

4229130/B 05/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.91 X 2.01
0.125	1.71 X 1.80 (SHOWN)
0.15	1.56 X 1.64
0.175	1.45 X 1.52

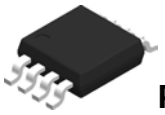
4229130/B 05/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

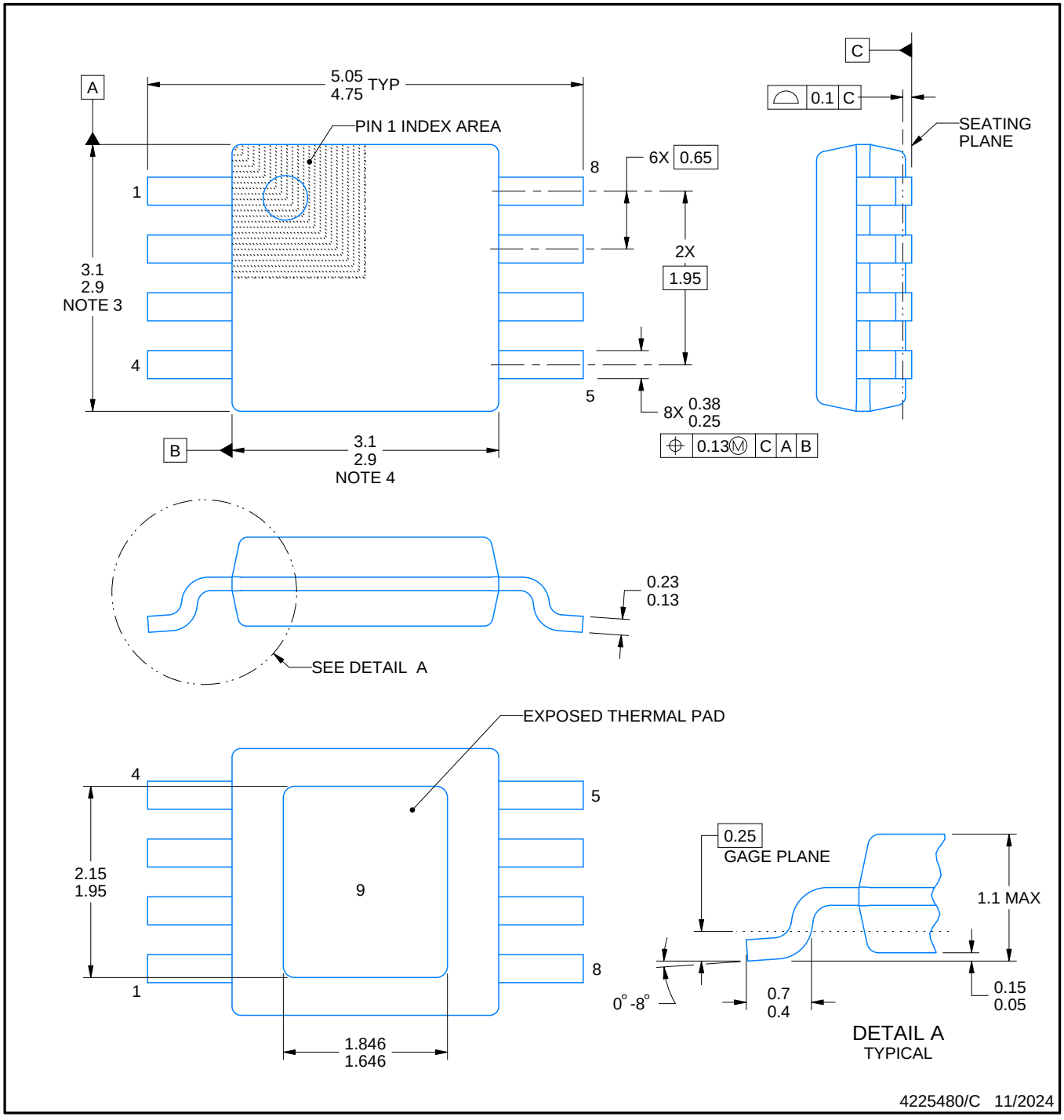
PACKAGE OUTLINE

DGN0008G



PowerPAD™ HVSSOP - 1.1 mm max height

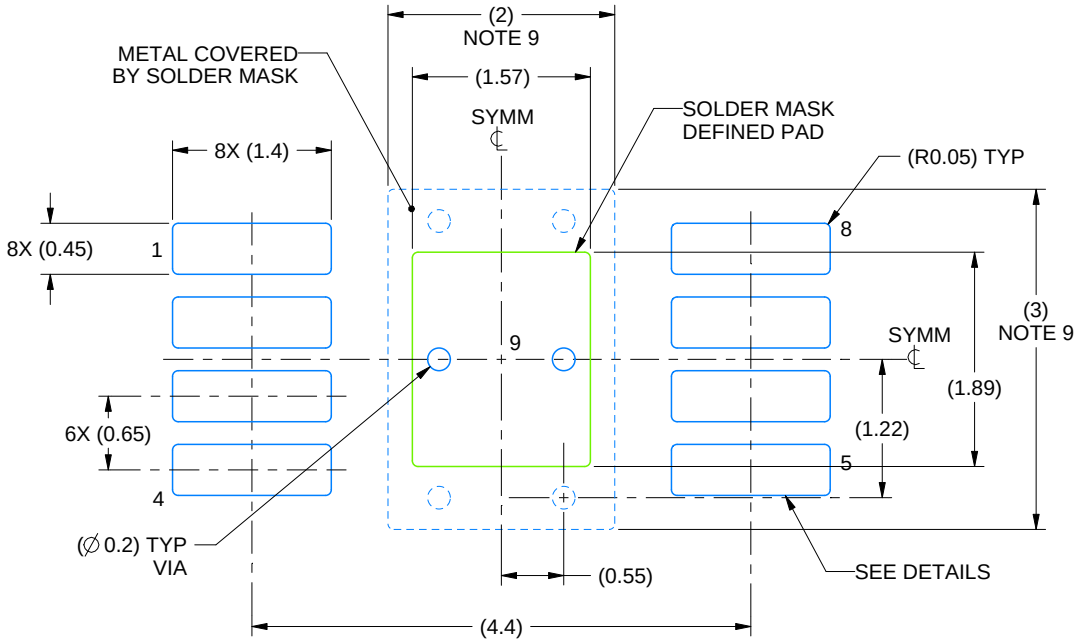
SMALL OUTLINE PACKAGE



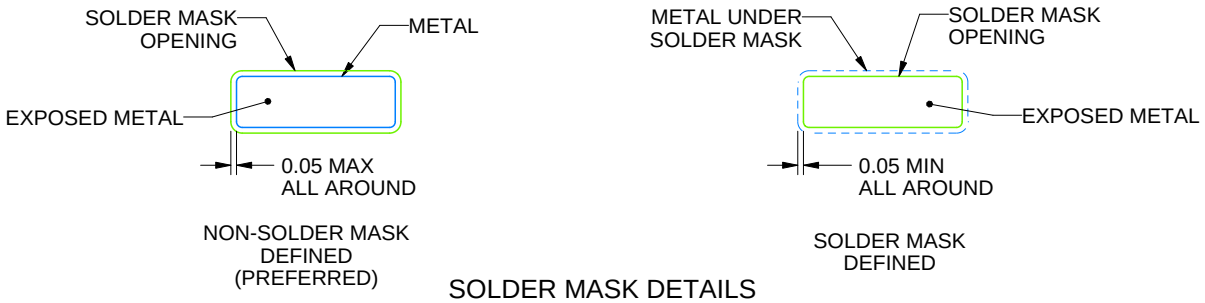
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

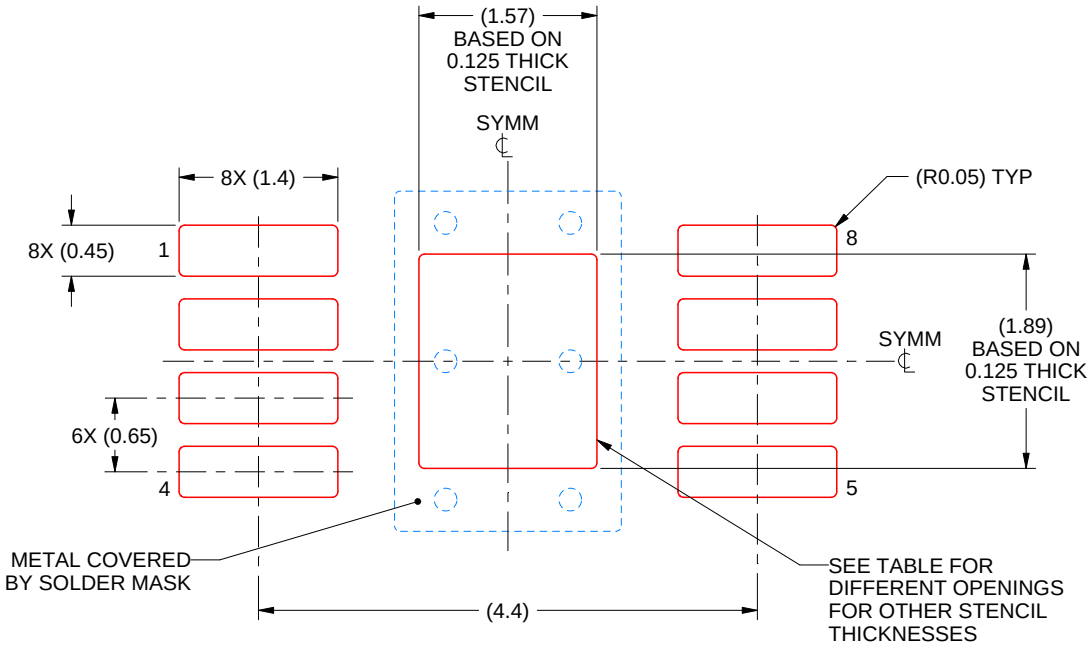


SOLDER MASK DETAILS

4225480/C 11/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/C 11/2024

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月