UCC27517A-Q1 具有负输入电压能力的单通道高速低侧栅极驱动器（具有 4A 峰值拉/灌电流）

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列结果：
  - 符合汽车应用要求的器件温度 1 级：-40°C 至 125°C 的环境运行温度范围
  - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 2
  - 器件组件充电模式 (CDM) ESD 分类等级 C6
- 低成本栅极驱动器器件提供 NPN 和 PNP 离散解决方案的高品质替代产品
- 4A 峰值拉电流和灌电流对称驱动
- 能够在输入上处理负电压 (-5V)
- 快速传播延迟（典型值 13ns）
- 快速上升和下降时间（典型值 9ns 和 7ns）
- 4.5V 至 18V 单电源
- V_{DD} 欠压锁定 (UVLO) 期间输出保持低电平（确保上电和掉电时的无毛刺脉冲运行）
- TTL 和 CMOS 兼容逻辑阈值（与电源电压无关）
- 针对高抗扰度的滞后逻辑阈值
- 双输入设计（选择一个反向（IN- 引脚）或者非反相（IN+ 引脚）驱动器配置）
  - 未使用的输入引脚可被用于启用或者禁用功能
- 当输入引脚悬空时输出保持在低电平
- 输入引脚最大绝对电压电平不受 V_{DD} 引脚偏置电源电压的限制
- -40°C 至 140°C 的运行温度范围
- 5 引脚 DBV（小外形尺寸晶体管 (SOT)-23）封装选项

2 应用范围

- 汽车
- 开关模式电源
- 直流到直流转换器
- 针对数字电源控制器的伴随栅极驱动器器件
- 太阳能、电机控制、不间断电源 (UPS)
- 用于新上市的宽带隙电源器件（例如 GaN）的栅极驱动器

3 说明

UCC27517A-Q1 单通道高速低侧栅极驱动器器件有效地驱动金属氧化物半导体场效应晶体管 (MOSFET) 和绝缘栅双极型晶体管 (IGBT) 开关。 借助于固有的大大减少击穿电流的设计，UCC27517A-Q1 能够灌、拉高峰值电流脉冲进入到电容负载，此电容负载提供了轨到轨驱动能力以及极小传播延迟（典型值为 13ns）。

UCC27517A-Q1 器件在输入上处理 -5V 电压。

当 V_{DD} = 12V 时，UCC27517A-Q1 可提供峰值为 4A 的灌/拉（对称驱动）电流驱动能力。

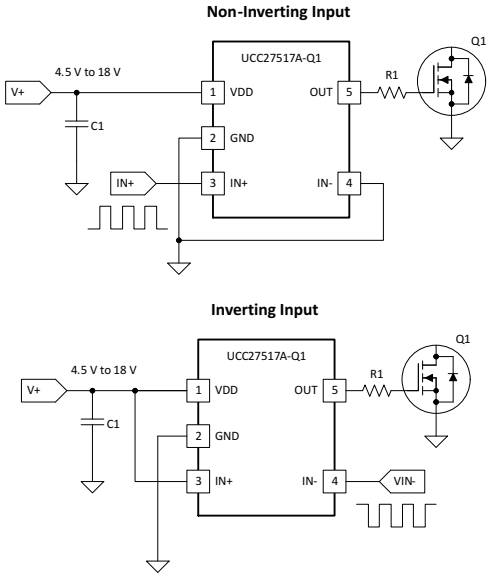
UCC27517A-Q1 在 4.5V 至 18V 的宽 V_{DD} 范围以及 -40°C 至 140°C 的宽温度范围内运行。 V_{DD} 引脚上的内部欠压锁定 (UVLO) 电路可在 V_{DD} 超出运行范围时使输出保持低电平。 此器件能够在低电压（例如低于 5V）下运行，并且拥有同类产品中最佳的开关特性，因此非常适用于驱动诸如 GaN 功率半导体器件等新上市的宽带隙电源开关器件。

器件信息(1)

部件号	封装	封装尺寸（标称值）
UCC27517A-Q1	SOT-23 (5)	2.90mm x 1.60mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用图



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2013) to Revision B **Page**

- 已添加 *ESD 额定值表，特性描述部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分。* ... 1

Changes from Original (August 2013) to Revision A **Page**

- 已更改 文档状态从 *产品预览* 改为*生成数据* ... 1

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5 Description (continued)

UCC27517A-Q1 features a dual-input design which offers flexibility of implementing both inverting (IN– pin) and non-inverting (IN+ pin) configurations with the same device. Either the IN+ or IN– pin are used to control the state of the driver output. The unused input pin is used for the enable and disable functional. For protection purpose, internal pullup and pulldown resistors on the input pins ensure that outputs are held low when input pins are in floating condition. Hence the unused input pin is not left floating and must be properly biased to ensure that driver output is in enabled for normal operation.

The input-pin threshold of the UCC27517A-Q1 device is based on TTL and CMOS compatible low-voltage logic which is fixed and independent of the V_{DD} supply voltage. Wide hysteresis between the high and low thresholds offers excellent noise immunity.

6 Device Comparison Table

The UCC2751x family of gate-driver products (Table 1) represent Texas Instruments' latest generation of single-channel, low-side high-speed gate driver devices featuring high-source and sink current capability, industry best-in-class switching characteristics, and a host of other features (Table 3) all of which combine to ensure efficient, robust, and reliable operation in high-frequency switching power circuits.

Table 1. UCC2751x Product Family Summary

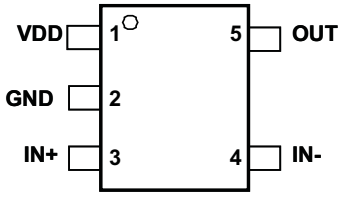
PART NUMBER(1)	PACKAGE	PEAK CURRENT (SOURCE, SINK)	INPUT THRESHOLD LOGIC
UCC27511DBV UCC27511ADBVQ1	SOT-23, 6 pin	4-A, 8-A (Asymmetrical Drive)	CMOS and TTL-Compatible (low voltage, independent of V_{DD} bias voltage)
UCC27512DRS	3-mm × 3-mm WSON, 6 pin		
UCC27516DRS	3-mm × 3-mm WSON, 6 pin	4-A, 4-A (Symmetrical Drive)	
UCC27517DBV UCC27517ADBVQ1 UCC27517ADBV	SOT-23, 5 pin		
UCC27518DBV UCC27518ADBVQ1	SOT-23, 5 pin		CMOS (follows V_{DD} bias voltage)
UCC27519DBV UCC27519ADBVQ1	SOT-23, 5 pin		

(1) Visit www.ti.com for the latest product datasheet.

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7 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{DD}	I	Bias supply input
2	GND	–	Ground. All signals reference to this pin
3	IN+	I	Non-inverting input. Apply PWM control signal to this pin when driver is desired to be operated in non-inverting configuration. When the driver is used in inverting configuration, connect IN+ to V_{DD} in order to enable output, OUT held LOW if IN+ is unbiased or floating
4	IN–	I	Inverting input. Apply PWM control signal to this pin when driver is desired to be operated in inverting configuration. When the driver is used in non-inverting configuration, connect IN– to GND in order to enable output, OUT held LOW if IN– is unbiased or floating
5	OUT	O	Sourcing/Sinking current output of driver

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

		MIN	MAX	UNIT
Supply voltage	V_{DD}	–0.3	20	V
OUT voltage	DC	–0.3	V_{DD} + 0.3	V
	Repetitive pulse less than 200 ns(4)	–2	V_{DD} + 0.3	V
Output continuous current	I_{OUT_DC} (source/sink)		0.3	A
Output pulsed current (0.5 µs)	I_{OUT_pulsed} (source/sink)		4	A
Input voltage	IN+, IN–(5)	–6	20	V
Operating virtual junction temperature, T_J		–40	150	°C
Storage temperature, T_{STG}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Packaging Section of the datasheet for thermal limitations and considerations of packages.
(3) These devices are sensitive to electrostatic discharge; follow proper device-handling procedures.
(4) Values are verified by characterization on bench.
(5) Maximum voltage on input pins is not restricted by the voltage on the V_{DD} pin.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2500	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.5	12	18	V
Operating ambient temperature	–40		140	°C
Input voltage, IN+ and IN–	0		18	V

8.4 Thermal Information

THERMAL METRIC(1)		UCC27517A-Q1 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	216	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	136.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

V_{DD} = 12 V, T_A = –40°C to 140°C, 1-µF capacitor from V_{DD} to GND. Currents are positive into, negative out of the specified terminal.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
BIAS CURRENTS							
$I_{DD(off)}$	Startup current	V_{DD} = 3.4 V	IN+ = V_{DD}, IN– = GND	40	100	160	µA
			IN+ = IN– = GND or IN+ = IN– = V_{DD}	25	75	145	
			IN+ = GND, IN– = V_{DD}	20	60	115	
UNDER VOLTAGE LOCKOUT (UVLO)							
V_{ON}	Supply start threshold	T_A = 25°C		3.91	4.20	4.5	V
		T_A = –40°C to 140°C		3.70	4.20	4.65	
V_{OFF}	Minimum operating voltage after supply start			3.45	3.9	4.35	V
V_{DD}_H	Supply voltage hysteresis			0.2	0.3	0.5	V
INPUTS (IN+, IN–)							
V_{IN_H}	Input signal high threshold	Output high for IN+ pin, Output low for IN– pin			2.2	2.4	V
V_{IN_L}	Input signal low threshold	Output low for IN+ pin, Output high for IN– pin		1	1.2		V
V_{IN_HYS}	Input signal hysteresis				1		V
SOURCE/SINK CURRENT							
$I_{SRC/SNK}$	Source/sink peak current(1)	C_{LOAD} = 0.22 µF, F_{SW} = 1 kHz			±4		A
OUTPUTS (OUT)							
V_{DD}–V_{OH}	High output voltage	V_{DD} = 12 V, I_{OUT} = –10 mA			50	90	mV
		V_{DD} = 4.5 V, I_{OUT} = –10 mA			60	130	
V_{OL}	Low output voltage	V_{DD} = 12, I_{OUT} = 10 mA			5	10	mV
		V_{DD} = 4.5 V, I_{OUT} = 10 mA			6	12	
R_{OH}	Output pullup resistance(2)	V_{DD} = 12 V, I_{OUT} = –10 mA			5	7.5	Ω
		V_{DD} = 4.5 V, I_{OUT} = –10 mA			5	11	
R_{OL}	Output pulldown resistance	V_{DD} = 12 V, I_{OUT} = 10 mA			0.5	1	Ω
		V_{DD} = 4.5 V, I_{OUT} = 10 mA			0.6	1.2	

(1) Ensured by Design.
(2) R_{OH} represents on-resistance of P-Channel MOSFET in pullup structure of the output stage of the UCC27517A-Q1.

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8.6 Switching Characteristics

V_{DD} = 12 V, T_A = –40°C to 140°C, 1-µF capacitor from V_{DD} to GND. Currents are positive into, negative out of the specified terminal.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHING TIME						
t_R	Rise time(1)	V_{DD} = 12 V, C_{LOAD} = 1.8 nF		8	12	ns
		V_{DD} = 4.5 V, C_{LOAD} = 1.8 nF		16	22	
t_F	Fall time(1)	V_{DD} = 12 V, C_{LOAD} = 1.8 nF		7	11	ns
		V_{DD}=4.5V, C_{LOAD} = 1.8 nF		7	11	
t_{D1}	IN+ to output propagation delay(1)	V_{DD} = 12 V, 5-V input pulse, C_{LOAD} = 1.8 nF	4	13	23	ns
		V_{DD} = 4.5 V, 5-V input pulse, C_{LOAD} = 1.8 nF	4	15	26	
t_{D2}	IN– to output propagation delay(1)	V_{DD} = 12 V, C_{LOAD} = 1.8 nF	4	13	23	ns
		V_{DD} = 4.5 V, C_{LOAD} = 1.8 nF	4	19	30	

(1) See timing diagrams in Figure 1, Figure 2, Figure 3 and Figure 4.

PWM Input to IN+ pin (IN– pin tied to GND)

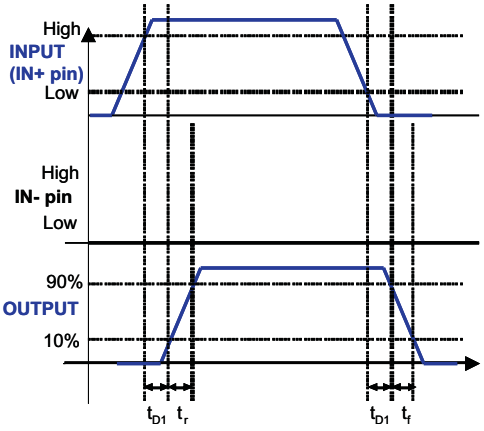


Figure 1. Non-Inverting Configuration

PWM input to IN– pin (IN+ pin tied to V_{DD})

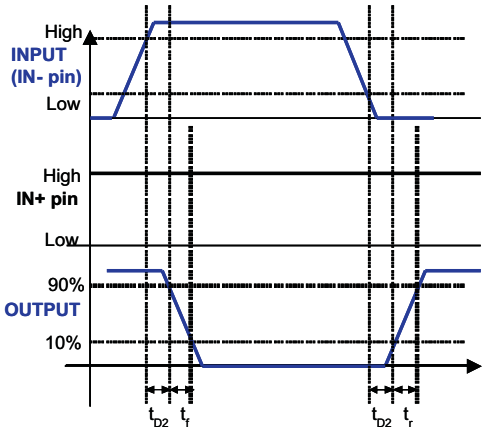


Figure 2. Inverting Configuration

Enable and disable signal applied to IN+ pin, PWM input to IN– pin

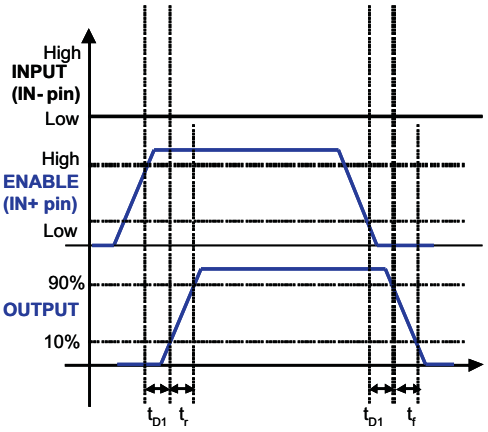


Figure 3. Enable and Disable Function Using IN+ Pin

Enable and disable signal applied to IN– pin, PWM input to IN+ pin

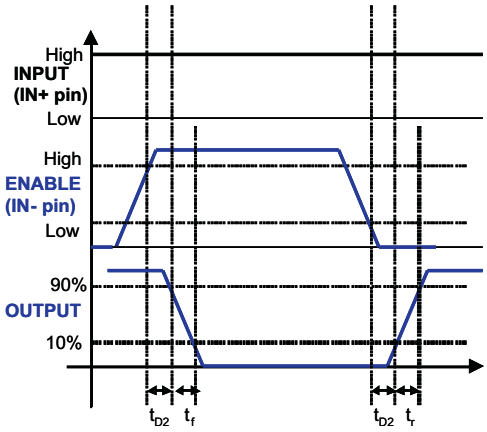


Figure 4. Enable and Disable Function Using IN– Pin

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8.7 Typical Characteristics

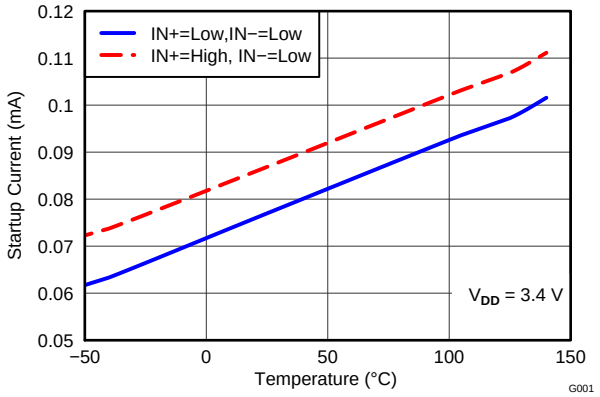


Figure 5. Startup Current vs Temperature

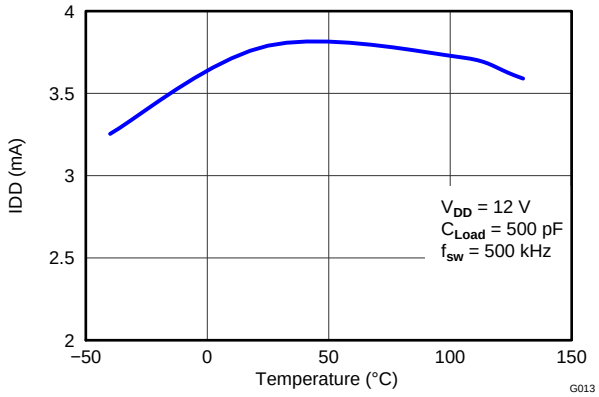


Figure 6. Operating Supply Current vs Temperature (Output Switching)

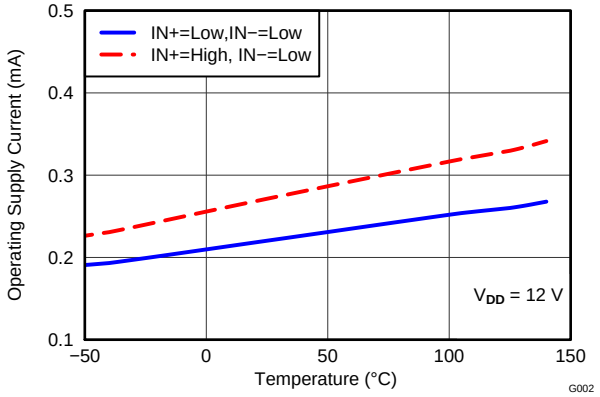


Figure 7. Supply Current vs Temperature (Output in DC On/Off condition)

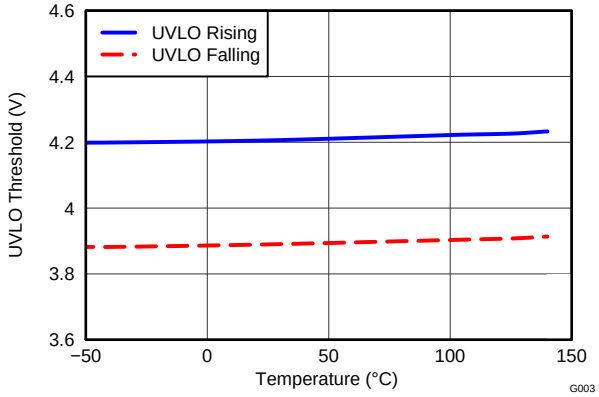


Figure 8. UVLO Threshold Voltage vs Temperature

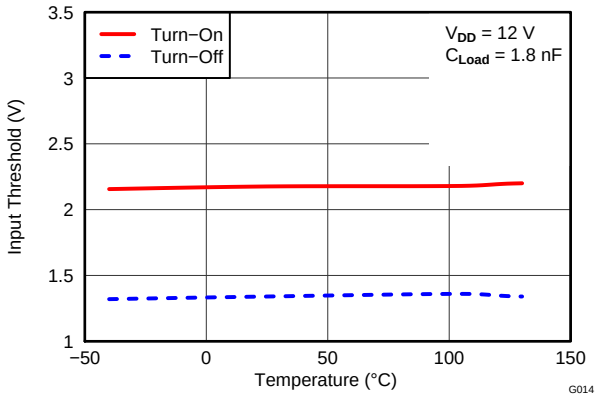


Figure 9. Input Threshold vs Temperature

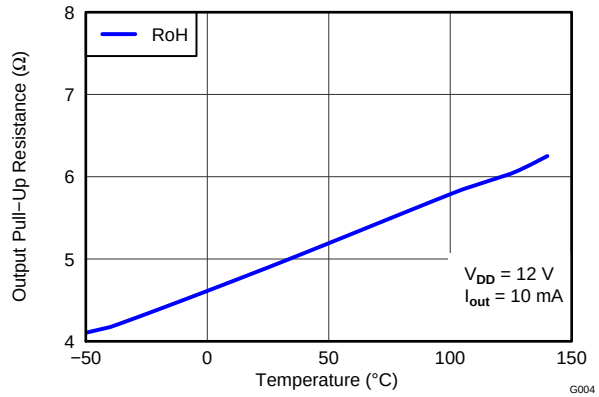


Figure 10. Output Pullup Resistance vs Temperature

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Typical Characteristics (continued)

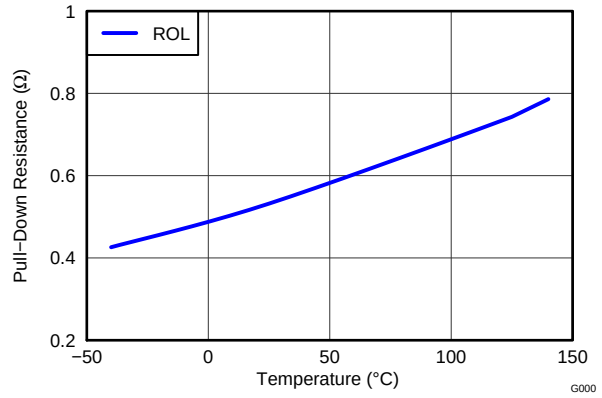


Figure 11. Output Pulldown Resistance vs Temperature

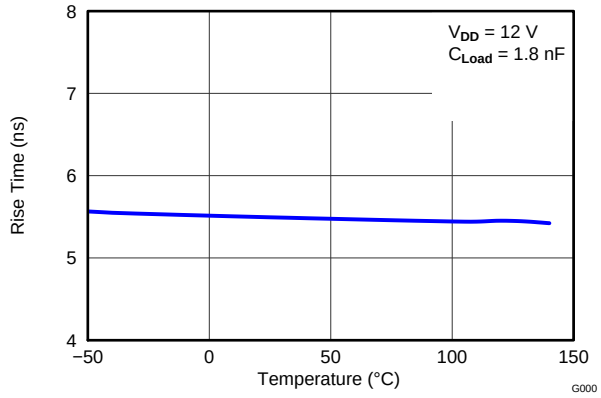


Figure 12. Rise Time vs Temperature

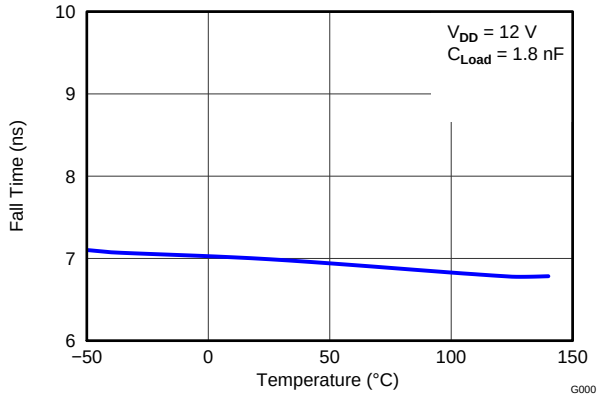


Figure 13. Fall Time vs Temperature

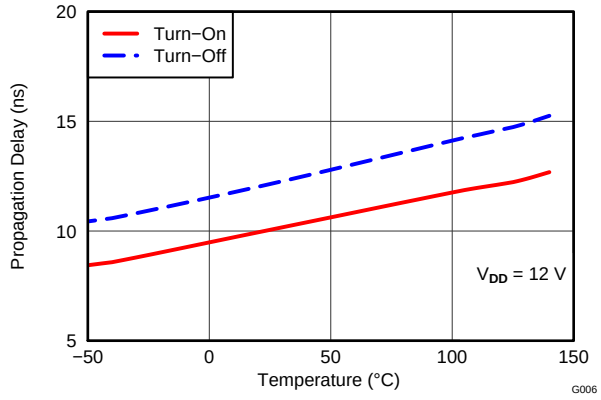


Figure 14. Input to Output Propagation Delay vs Temperature

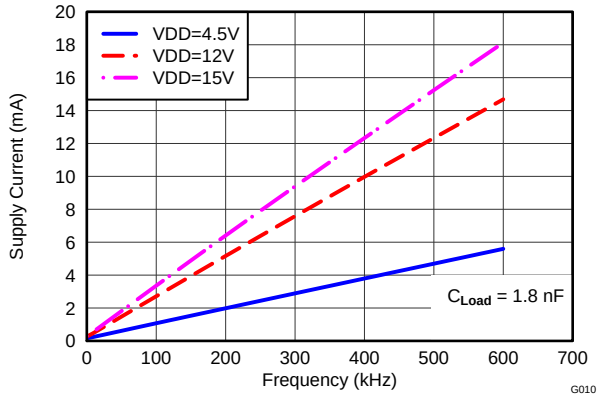


Figure 15. Operating Supply Current vs Frequency

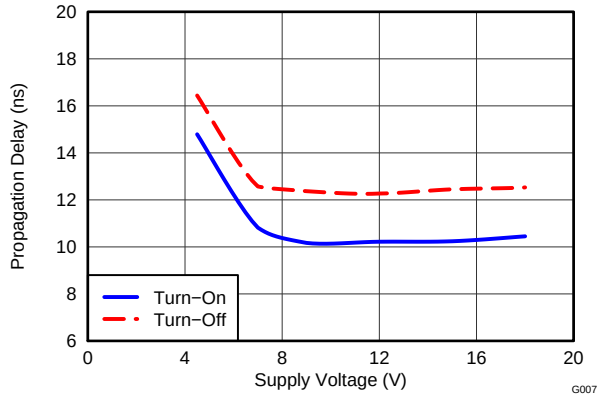


Figure 16. Propagation Delays vs Supply Voltage

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Typical Characteristics (continued)

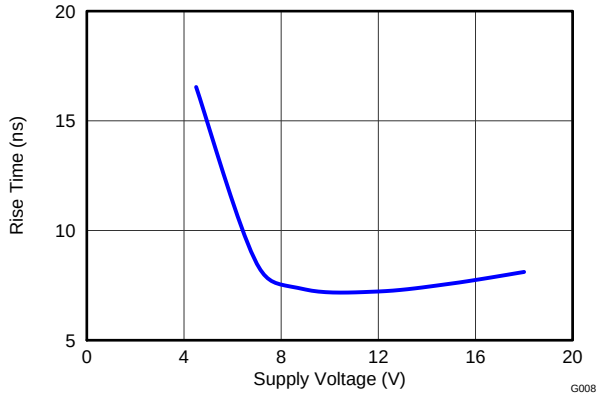


Figure 17. Rise Time vs Supply Voltage

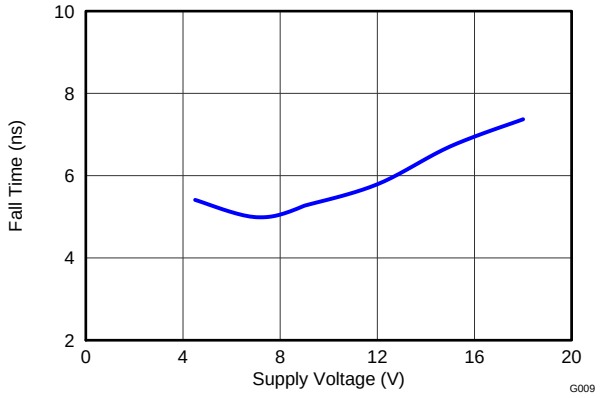


Figure 18. Fall Time Vs Supply Voltage

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9 Detailed Description

9.1 Overview

The UCC2751xA-Q1 single-channel, high-speed, low-side gate-driver device is capable of effectively driving MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, the UCC2751x device is capable of sourcing and sinking high peak-current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay of 13 ns (typical). The UCC2751xA-Q1 family of devices provides 4-A source, 4-A sink (symmetrical drive) peak-drive current capability. The device is designed to operate over a wide V_{DD} range of 4.5 to 18 V, and a wide temperature range of –40°C to 140°C. Internal undervoltage lockout (UVLO) circuitry on the V_{DD} pin holds the output low outside V_{DD} operating range. The capability to operate at low voltage levels, such as below 5 V, along with best-in- class switching characteristics, is especially suited for driving emerging wide bandgap power-switching devices such as GaN power-semiconductor devices.

The UCC27511A-Q1 device features a dual-input design which offers flexibility of implementing both inverting (IN– pin) and non-inverting (IN+ pin) configuration with the same device. Either the IN+ or IN– pin can be used to control the state of the driver output. The unused input pin can be used for enable and disable functions. For system robustness, internal pull-up and pull-down resistors on the input pins ensure that outputs are held low when the input pins are in floating condition. Therefore the unused input pin is not left floating and must be properly biased to ensure that driver output is in enabled for normal operation.

The input pin threshold of the UCC27517A-Q1 device is based on TTL and CMOS-compatible low-voltage logic which is fixed and independent of the V_{DD} supply voltage. Wide hysteresis between the high and low thresholds offers excellent noise immunity.

Table 2. UCC27517A-Q1 Summary

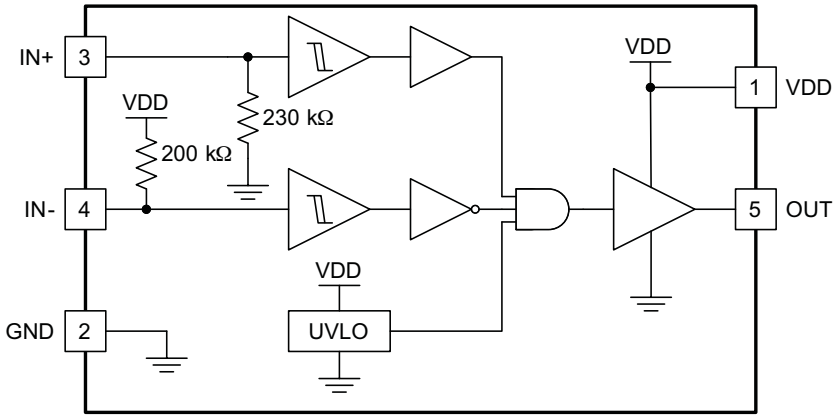
PART NUMBER	PACKAGE	PEAK CURRENT (SOURCE, SINK)	INPUT THRESHOLD LOGIC
UCC27517ADBVQ1	SOT-23, 5 pin	4-A, 4-A (Symmetrical Drive)	CMOS and TTL-Compatible (low voltage, independent of V_{DD} bias voltage)

Table 3. UCC27517A-Q1 Features and Benefits

FEATURE	BENEFIT
High Source, Sink Current Capability 4 A, 4 A (Symmetrical)	High current capability offers flexibility in employing the UCC27517A-Q1 to drive a variety of power switching devices at varying speeds
Best-in-class 13-ns (typ) Propagation delay	Extremely low-pulse transmission distortion
Expanded V_{DD} Operating range of 4.5 V to 18 V	Flexibility in system design Low V_{DD} operation ensures compatibility with emerging wide-bandgap power devices such as GaN
Expanded Operating Temperature range of –40°C to 140°C *(See Recommended Operating Conditions table)*	
V_{DD} UVLO Protection	Outputs are held low in UVLO condition, which ensures predictable glitch-free operation at power up and power down
Outputs held low when input pins (INx) in floating condition	Protection feature, especially useful in passing abnormal condition tests during protection certification
Ability of input pins to handle voltage levels not restricted by V_{DD} pin bias voltage	System simplification, especially related to auxiliary bias supply architecture
CMOS and TTL compatible input threshold logic with wide hysteresis in UCC27517A-Q1	Enhanced noise immunity, while retaining compatibility with microcontroller logic-level input signals (3.3 V, 5 V) optimized for digital power
Ability to handle –5 V_{DC} at input pins	Increased robustness in noisy envirnments

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9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 V_{DD} and Undervoltage Lockout

The UCC27517A-Q1 has internal Undervoltage Lockout (UVLO) protection feature on the V_{DD}-pin supply-circuit blocks. Whenever the driver is in UVLO condition (for example when V_{DD} voltage is less than V_{ON} during power up and when V_{DD} voltage is less than V_{OFF} during power down), this circuit holds all outputs LOW, regardless of the status of the inputs. The UVLO is typically 4.2 V with 300-mV typical hysteresis. This hysteresis helps prevent chatter when low V_{DD} – supply voltages have noise from the power supply and also when there are droops in the V_{DD}-bias voltage when the system commences switching and there is a sudden increase in I_{DD}. The capability to operate at low voltage levels such as below 5 V, along with best-in-class switching characteristics, is especially suited for driving emerging GaN wide-bandgap power-semiconductor devices.

For example, at power up, the UCC27517A-Q1 driver output remains LOW until the V_{DD} voltage reaches the UVLO threshold. The magnitude of the OUT signal rises with V_{DD} until steady-state V_{DD} is reached. In the non-inverting operation (PWM signal applied to IN+ pin) shown in Figure 19, the output remains LOW until the UVLO threshold is reached, and then the output is in-phase with the input. In the inverting operation (PWM signal applied to IN– pin) shown in Figure 20 the output remains LOW until the UVLO threshold is reached, and then the output is out-phase with the input. In both cases, the unused input pin must be properly biased to enable the output. Note that in these devices the output turns to high-state only if IN+ pin is high and IN– pin is low after the UVLO threshold is reached.

Because the driver draws current from the V_{DD} pin to bias all internal circuits, for the best high-speed circuit performance, two V_{DD} bypass capacitors are recommended to prevent noise problems. The use of surface-mount components is highly recommended. A 0.1-µF ceramic capacitor should be located as close as possible to the V_{DD} to GND pins of the gate driver. In addition, a larger capacitor (such as 1 µF) with relatively low ESR should be connected in parallel and close proximity, in order to help deliver the high-current peaks required by the load. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels and switching frequencies in the application.

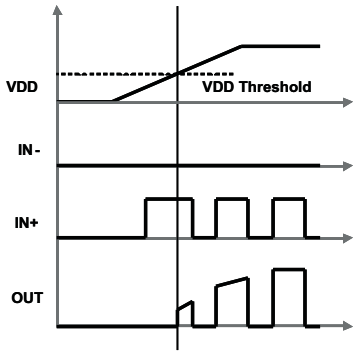


Figure 19. Power-Up (Non-Inverting Drive)

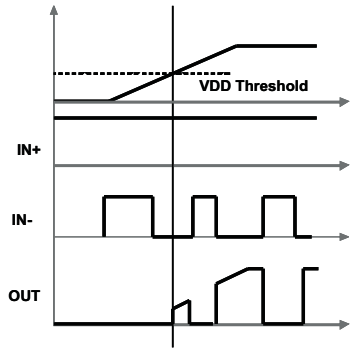


Figure 20. Power-Up (Inverting Drive)

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Feature Description (continued)

9.3.2 Operating Supply Current

The UCC27517A-Q1 features very low quiescent I_{DD} currents. The typical operating-supply current in Undervoltage-Lockout (UVLO) state and fully-on state (under static and switching conditions) are summarized in Figure 5, Figure 6 and Figure 7. The I_{DD} current when the device is fully on and outputs are in a static state (DC high or DC low, refer Figure 7) represents lowest quiescent I_{DD} current when all the internal logic circuits of the device are fully operational. The total supply current is the sum of the quiescent I_{DD} current, the average I_{OUT} current due to switching and finally any current related to pullup resistors on the unused input pin. For example when the inverting input pin is pulled low additional current is drawn from V_{DD} supply through the pull-up resistors (refer to *Detailed Description* for the device Block Diagram). Knowing the operating frequency (f_{SW}) and the MOSFET gate (Q_G) charge at the drive voltage being used, the average I_{OUT} current can be calculated as product of Q_G and f_{SW}.

A complete characterization of the I_{DD} current as a function of switching frequency at different V_{DD} bias voltages under 1.8-nF switching load is provided in Figure 15. The strikingly-linear variation and close correlation with theoretical value of average I_{OUT} indicates negligible shoot-through inside the gate-driver device attesting to the high-speed characteristics of I_{OUT}.

9.3.3 Input Stage

The input pins of the UCC27517A-Q1 are based on a TTL and CMOS compatible input-threshold logic that is independent of the V_{DD} supply voltage. With typical high threshold = 2.2 V and typ low threshold = 1.2 V, the logic-level thresholds can be conveniently driven with PWM-control signals derived from 3.3-V and 5-V digital-power controllers. Wider hysteresis (typically 1 V) offers enhanced noise immunity compared to traditional TTL-logic implementations, where the hysteresis is typically less than 0.5 V. These devices also feature tight control of the input-pin threshold-voltage levels which eases system-design considerations and ensures stable operation across temperature. The very low input capacitance on these pins reduces loading and increases switching speed.

The device features an important protection function wherein, whenever any of the input pins are in a floating condition, the output of the respective channel is held in the low state. This is achieved using V_{DD}-pullup resistors on all the inverting inputs (IN– pin) or GND-pulldown resistors on all the non-inverting input pins (IN+ pin), (refer to the device *Functional Block Diagram*).

The device also features a dual-input configuration with two input pins available to control the state of the output. The user has the flexibility to drive the device using either a non-inverting input pin (IN+) or an inverting input pin (IN–). The state of the output pin is dependent on the bias on both the IN+ and IN– pins. Refer to the input/output logic truth table (Table 4) and the Typical Application Diagrams, (Figure 22 and Figure 23), for additional clarification.

Once an input pin has been chosen for PWM drive, the other input pin (the *unused* input pin) must be properly biased in order to enable the output. As mentioned earlier, the *unused* input pin cannot remain in a floating condition because, whenever any input pin is left in a floating condition, the output is disabled for protection purposes. Alternatively, the *unused* input pin can effectively be used to implement an enable/disable function, as explained below.

- In order to drive the device in a non-inverting configuration, apply the PWM-control input signal to IN+ pin. In this case, the *unused* input pin, IN–, must be biased low (eg. tied to GND) in order to enable the output.
  - Alternately, the IN– pin can be used to implement the enable/disable function using an external logic signal. OUT is disabled when IN– is biased high and OUT is enabled when IN– is biased low.
- In order to drive the device in an inverting configuration, apply the PWM-control input signal to IN– pin. In this case, the *unused* input pin, IN+, must be biased high (eg. tied to V_{DD}) in order to enable the output.
  - Alternately, the IN+ pin can be used to implement the enable/disable function using an external logic signal. OUT is disabled when IN+ is biased low and OUT is enabled when IN+ is biased high.
- Finally, note that the output pin is driven into a high state *only* when IN+ pin is biased high and IN– input is biased low.

The input stage of the driver should preferably be driven by a signal with a short rise or fall time. Caution must be exercised whenever the driver is used with slowly-varying input signals, especially in situations where the device is located in a mechanical socket or PCB layout is not optimal:

- High dI/dt current from the driver output coupled with board layout parasitics causes ground bounce. Because

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Feature Description (continued)

the device features just one GND pin, which may be referenced to the power ground, the differential voltage between input pins and GND is modified and triggers an unintended change of output state. Because of fast 13-ns propagation delay, high-frequency oscillations ultimately occur, which increases power dissipation and poses risk of damage.

- 1-V input-threshold hysteresis boosts noise immunity compared to most other industry-standard drivers.
- In the worst case, when a slow input signal is used and PCB layout is not optimal, adding a small capacitor (1 nF) between input pin and ground very close to the driver device is necessary. This helps to convert the differential mode noise with respect to the input-logic circuitry into common-mode noise and avoid unintended change of output state.

If limiting the rise or fall times to the power device is the primary goal, then an external resistance is highly recommended between the output of the driver and the power device instead of adding delays on the input signal. This external resistor has the additional benefit of reducing part of the gate charge related power dissipation in the gate-driver device package and transferring the gate driver into the external resistor.

9.3.4 Enable Function

As mentioned earlier, an enable or disable function is easily implemented in the UCC27517A-Q1 using the *unused* input pin. When IN+ is pulled down to GND or IN– is pulled down to V_{DD}, the output is disabled. Thus IN+ pin is used like an enable pin that is based on active-high logic, while IN– can be used like an enable pin that is based on active-low logic.

9.3.5 Output Stage

The UCC27517A-Q1 is capable of delivering 4-A source, 4-A sink (symmetrical drive) at V_{DD} = 12 V. The output stage of the UCC27517A-Q1 device is illustrated in Figure 21. The UCC27517A-Q1 features a unique architecture on the output stage which delivers the highest peak-source current when most needed during the Miller-plateau region of the power-switch turnon transition (when the power-switch drain/collector voltage experiences dV/dt). The device output stage features a hybrid pullup structure using a parallel arrangement of N-Channel and P-Channel MOSFET devices. By turning on the N-Channel MOSFET during a narrow instant when the output changes state from low to high, the gate-driver device delivers a brief boost in the peak-sourcing current enabling fast turnon.

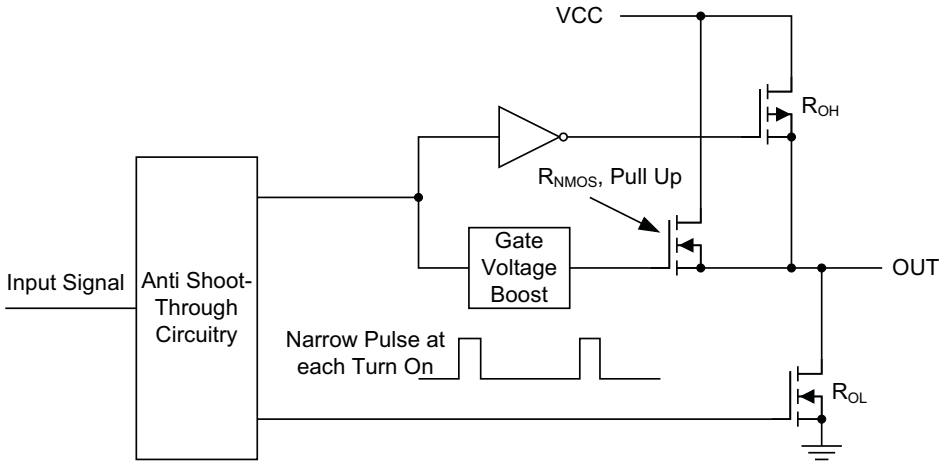


Figure 21. UCC27517A-Q1 Gate Driver Output Structure

The R_{OH} parameter (see *Electrical Characteristics*) is a DC measurement and is representative of the on-resistance of the P-Channel device only, since the N-Channel device is turned on only during output change of state from low to high. Thus the effective resistance of the hybrid pullup stage is much lower than what is represented by R_{OH} parameter. The pulldown structure is composed of a N-Channel MOSFET only. The R_{OL} parameter (see *Electrical Characteristics*), which is also a DC measurement, is representative of true impedance of the pulldown stage in the device. In the UCC27517A-Q1, the effective resistance of the hybrid pullup structure is approximately 1.4 × R_{OL}.

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Feature Description (continued)

The driver-output voltage swings between V_{DD} and GND providing rail-to-rail operation because of the MOS output stage which delivers very low dropout. The presence of the MOSFET-body diodes also offers low impedance to switching overshoots and undershoots. This means that in many cases, external Schottky-diode clamps may be eliminated. The outputs of these drivers are designed to withstand 500-mA reverse current without either damage to the device or logic malfunction.

9.3.6 Low Propagation Delays

The UCC27517A-Q1 features best-in-class input-to-output propagation delay of 13 ns (typ) at V_{DD} = 12 V. This promises the lowest level of pulse-transmission distortion available from industry-standard gate-driver devices for high-frequency switching applications. As seen in Figure 14, there is very little variation of the propagation delay with temperature and supply voltage as well, offering typically less than 20-ns propagation delays across the entire range of application conditions.

9.4 Device Functional Modes

The device operates in normal mode and UVLO mode. See the *V_{DD} and Undervoltage Lockout* section for information on UVLO operation mode. In the normal mode the output state is dependent on states of the IN+ and IN– pins. Table 4 below lists the output states for different input pin combinations.

Table 4. Device Logic Table

IN+ PIN	IN– PIN	OUT PIN
L	L	L
L	H	L
H	L	H
H	H	L
x(1)	Any	L
Any	x(1)	L

(1) x = Floating Condition

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

High-current gate-driver devices are required in switching power applications for a variety of reasons. In order to effect fast switching of power devices and reduce associated switching power losses, a powerful gate driver is employed between the PWM output of controllers and the gates of the power-semiconductor devices. Further, gate drivers are indispensable when there are times that the PWM controller cannot directly drive the gates of the switching devices. With advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal, which is not capable of effectively turning on a power switch. A level-shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Because traditional buffer-drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter-follower configurations, lack level-shifting capability, the circuits prove inadequate with digital power. Gate drivers effectively combine both the level-shifting and buffer-drive functions.

Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate-charge power losses into itself. Finally, emerging wide-bandgap power-device technologies, such as GaN based switches, which are capable of supporting very high switching frequency operation, are driving very special requirements in terms of gate-drive capability. These requirements include operation at low V_{DD} voltages (5 V or lower), low propagation delays and availability in compact, low-inductance packages with good thermal capability. In summary gate-driver devices are extremely important components in switching power combining benefits of high-performance, low cost, component count and board space reduction with a simplified system design.

10.2 Typical Application

Typical application diagrams for the UCC27517A-Q1 device are shown in Figure 22 and Figure 23 to illustrate use in non-inverting and inverting driver configurations.

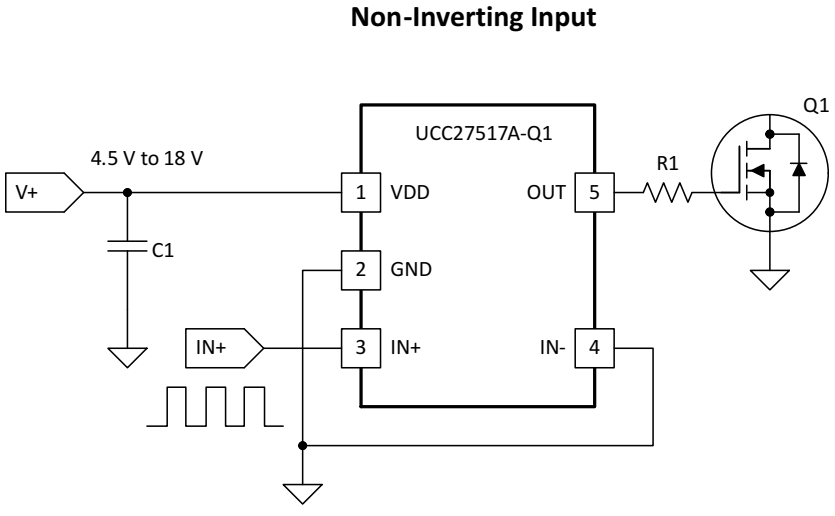


Figure 22. Using Non-Inverting Input (IN– is grounded to the enable output)

Typical Application (continued)

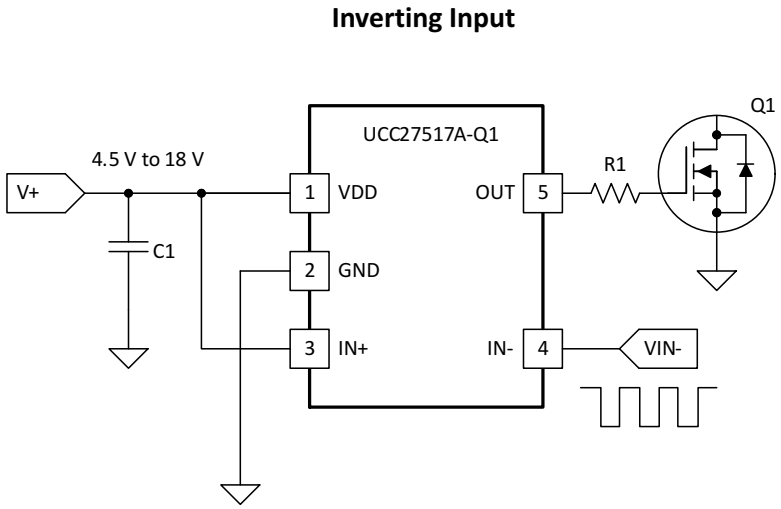


Figure 23. Using Inverting Input (IN+ is tied to V_{DD} enable output)

10.2.1 Design Requirements

When selecting the proper gate driver device for an end application, some design considerations must be evaluated first to make the most appropriate selection. Among these considerations are input-to-output configuration, the input threshold type, bias supply voltage levels, peak source and sink currents, availability of independent enable and disable functions, propagation delay, power dissipation, and package type.

Table 5. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input-to-Output Logic	Non-Inverting
Input Threshold Type	Logic Level
V_{DD} Bias Supply Voltage	10 V (minimum), 13 V (nominal), 15 V (peak)
Peak Source and Sink Currents	Minimum 3 A Source, Minimum 3 A Sink
Enable and Disable Function	Yes, Needed
Propagation Delay	Maximum 40 ns or Less

10.2.2 Detailed Design Procedure

10.2.2.1 Input-to-Output Logic

The design should specify which type of input-to-output configuration should be used. If turning on the power MOSFET or IGBT when the input signal is in high state is preferred, then the noninverting configuration must be selected. If turning off the power MOSFET or IGBT when the input signal is in high state is preferred, the inverting configuration must be chosen. The UCC27517-Q1 device can be configured in either an inverting or noninverting input-to-output configuration, using the IN– or IN+ pins, respectively. To configure the device for use in inverting mode, tie the IN+ pin to V_{DD} and apply the input signal to the IN– pin. For the non inverting configuration, tie the IN– pin to GND and apply the input signal to the IN+ pin

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10.2.2.2 Input Threshold Type

The type of input voltage threshold determines the type of controller used with the gate driver device. The UCC27517-Q1 device featureS a TTL and CMOS-compatible input threshold logic, with wide hysteresis. The threshold voltage levels are low voltage and independent of the V_{DD} supply voltage, which allows compatibility with both logic-level input signals from microcontrollers, as well as higher-voltage input signals from analog controllers. See *Electrical Characteristics* for the actual input threshold voltage levels and hysteresis specifications for the UCC27517-Q1 device.

10.2.2.3 V_{DD} Bias Supply Voltage

The bias supply voltage to be applied to the V_{DD} pin of the device should never exceed the values listed in the *Recommended Operating Conditions* table. However, different power switches demand different voltage levels to be applied at the gate terminals for effective turnon and turnoff. With certain power switches, a positive gate voltage may be required for turnon and a negative gate voltage may be required for turnoff, in which case the V_{DD} bias supply equals the voltage differential. With a wide operating range from 4.5 V to 18 V, the UCC27517-Q1 device can be used to drive a variety of power switches, such as Si MOSFETs (for example, VGS = 4.5 V, 10 V, 12 V), IGBTs (VGE = 15 V, 18 V), and wide-band gap power semiconductors (such as GaN, certain types of which allow no higher than 6 V to be applied to the gate terminals).

10.2.2.4 Peak Source and Sink Currents

Generally, the switching speed of the power switch during turnon and turnoff should be as fast as possible, to minimize switching power losses. The gate driver device must be able to provide the required peak current for achieving the targeted switching speeds for the targeted power MOSFET.

Using the example of a power MOSFET, the system requirement for the switching speed is typically described in terms of the slew rate of the drain-to-source voltage of the power MOSFET (such as dV DS /dt). For example, the system requirement might state that a SPP20N60C3 power MOSFET must be turned-on with a dV DS /dt of 20V/ns or higher, under a DC bus voltage of 400 V in a continuous-conduction-mode (CCM) boost PFC-converter application. This type of application is an inductive hard-switching application and reducing switching power losses is critical. This requirement means that the entire drain-to-source voltage swing during power MOSFET turnon event (from 400 V in the OFF state to V DS(on) in on state) must be completed in approximately 20 ns or less.

When the drain-to-source voltage swing occurs, the Miller charge of the power MOSFET (QGD parameter in SPP20N60C3 power MOSFET data sheet = 33 nC typical) is supplied by the peak current of gate driver. According to the power MOSFET inductive switching mechanism, the gate-to-source voltage of the power MOSFET at this time is the Miller plateau voltage, which is typically a few volts higher than the threshold voltage of the power MOSFET, VGS(TH). To achieve the targeted dV DS /dt, the gate driver must be capable of providing the QGD charge in 20 ns or less. In other words, a peak current of 1.65 A (= 33 nC / 20 ns) or higher must be provided by the gate driver. The UCC27517-Q1 gate driver is capable of providing 4-A peak sourcing current, which exceeds the design requirement and has the capability to meet the switching speed needed.

The 2.4x overdrive capability provides an extra margin against part-to-part variations in the QGD parameter of the power MOSFET, along with additional flexibility to insert external gate resistors and fine tune the switching speed for efficiency versus EMI optimizations. However, in practical designs the parasitic trace inductance in the gate drive circuit of the PCB will have a definitive role to play on the power MOSFET switching speed. The effect of this trace inductance is to limit the dI/dt of the output current pulse of the gate driver.

To illustrate this, consider output current pulse waveform from the gate driver to be approximated to a triangular profile, where the area under the triangle (½ × I PEAK × time) would equal the total gate charge of the power MOSFET (QG parameter in SPP20N60C3 power MOSFET datasheet = 87 nC typical).

If the parasitic trace inductance limits the dI/dt, then a situation may occur in which the full peak current capability of the gate driver is not fully achieved in the time required to deliver the QG required for the power MOSFET switching. In other words, the time parameter in the equation would dominate and the I PEAK value of the current pulse would be much less than the true peak current capability of the device, while the required QG is still delivered. Because of this, the desired switching speed may not be realized, even when theoretical calculations indicate the gate driver is capable of achieving the targeted switching speed. Thus, placing the gate driver device very close to the power MOSFET and designing a tight gate drive-loop with minimal PCB trace inductance is important to realize the full peak-current capability of the gate driver.

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10.2.2.5 Enable and Disable Runction

Certain applications demand independent control of the output state of the driver, without involving the input signal. A pin offering an enable and disable function achieves this requirement. The UCC27517-Q1 device offers two input pins, IN+ and IN – , both of which control the state of the output as listed in Table 4. Based on whether an inverting or non inverting input signal is provided to the driver, the appropriate input pin can be selected as the primary input for controlling the gate driver. The other unused input pin can be used for the enable and disable functionality. If the design does not require an enable function, the unused input pin can be tied to either the V_{DD} pin (in case IN+ is the unused pin), or GND (in case IN – is unused pin) to ensure it does not affect the output status.

10.2.2.6 Propagation Delay

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used, and the acceptable level of pulse distortion to the system. The UCC27517-Q1 device featureS industry best-in-class 13-ns (typical) propagation delays, which ensure very little pulse distortion and allow operation at very high-frequencies. See *Switching Characteristics* for the propagation and switching characteristics of the UCC27517-Q1 device.

10.2.3 Application Curves

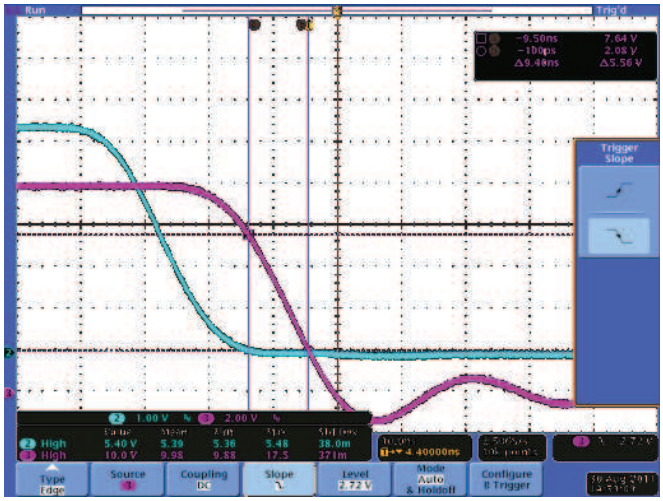


Figure 24. Typical Turnon Waveform

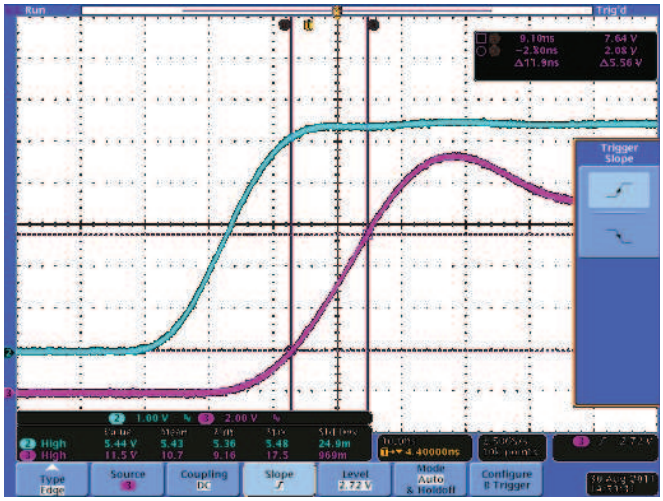


Figure 25. Typical Turnoff Waveform

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11 Power Supply Recommendations

The bias supply voltage range for which the UCC27517-Q1 device is rated to operate is from 4.5 V to 18 V. The lower end of this range is governed by the internal UVLO protection feature on the V_{DD} pin supply circuit blocks. Whenever the driver is in UVLO condition when the V_{DD} pin voltage is below the V(ON) supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20-V absolute maximum voltage rating of the V_{DD} pin of the device (which is a stress rating). Keeping a 2-V margin to allow for transient voltage spikes, the maximum recommended voltage for the V_{DD} pin is 18 V.

The UVLO protection feature also involves a hysteresis function. This means that when the V_{DD} pin bias voltage has exceeded the threshold voltage and the device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification $V_{DD(hys)}$. While operating at or near the 4.5 V range, ensure that the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device, to avoid triggering a device shutdown.

During system shutdown, the device operation continues until the V_{DD} pin voltage has dropped below the $V_{(OFF)}$ threshold, which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system startup the device does not begin operation until the V_{DD} pin voltage has exceeded above the $V_{(ON)}$ threshold. The quiescent current consumed by the internal circuit blocks of the device is supplied through the V_{DD} pin. Keep in mind that the charge for source current pulses delivered by the OUT pin is also supplied through the same V_{DD} pin. As a result, every time a current is sourced out of the output pin (OUT), a corresponding current pulse is delivered into the device through the V_{DD} pin. Therefore, ensure that local bypass capacitors are provided between the V DD and GND pins, and located as close to the device as possible for the purpose of decoupling. A low ESR, ceramic surface mount capacitor is necessary. TI recommends using 2 capacitors; a 100-nF ceramic surface-mount capacitor which can be nudged very close to the pins of the device, and another surface-mount capacitor of few microfarads added in parallel.

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12 Layout

12.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current fast-switching circuit to provide appropriate device operation and design robustness. The UCC27517A-Q1 gate driver incorporates short-propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of the power switch to facilitate voltage transitions very quickly. At higher V_{DD} voltages, the peak-current capability is even higher (4-A, 4-A peak current is at V_{DD} = 12 V). Very high di/dt causes unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are strongly recommended when designing with these high-speed drivers.

- Locate the driver device as close as possible to the power device in order to minimize the length of high-current traces between the output pins and the gate of the power device.
- Locate the V_{DD} bypass capacitors between V_{DD} and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high-peak current being drawn from V_{DD} during turnon of power MOSFET. The use of low inductance SMD components such as chip resistors and chip capacitors is highly recommended.
- The turnon and turnoff current-loop paths (driver device, power MOSFET and V_{DD} bypass capacitor) should be minimized as much as possible in order to keep the stray inductance to a minimum. High dI/dt is established in these loops at two instances — during turnon and turnoff transients, which will induce significant voltage transients on the output pin of the driver device and gate of the power switch.
- Wherever possible parallel the source and return traces, taking advantage of flux cancellation.
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as source of power switch or the ground of PWM controller at one, single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.
- In noisy environments, tying the unused input pin of the UCC27517A-Q1 to V_{DD} (in case of IN+) or GND (in case of IN–) using short traces in order to ensure that the output is enabled and to prevent noise from causing malfunction in the output is necessary.

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12.2 Layout Example

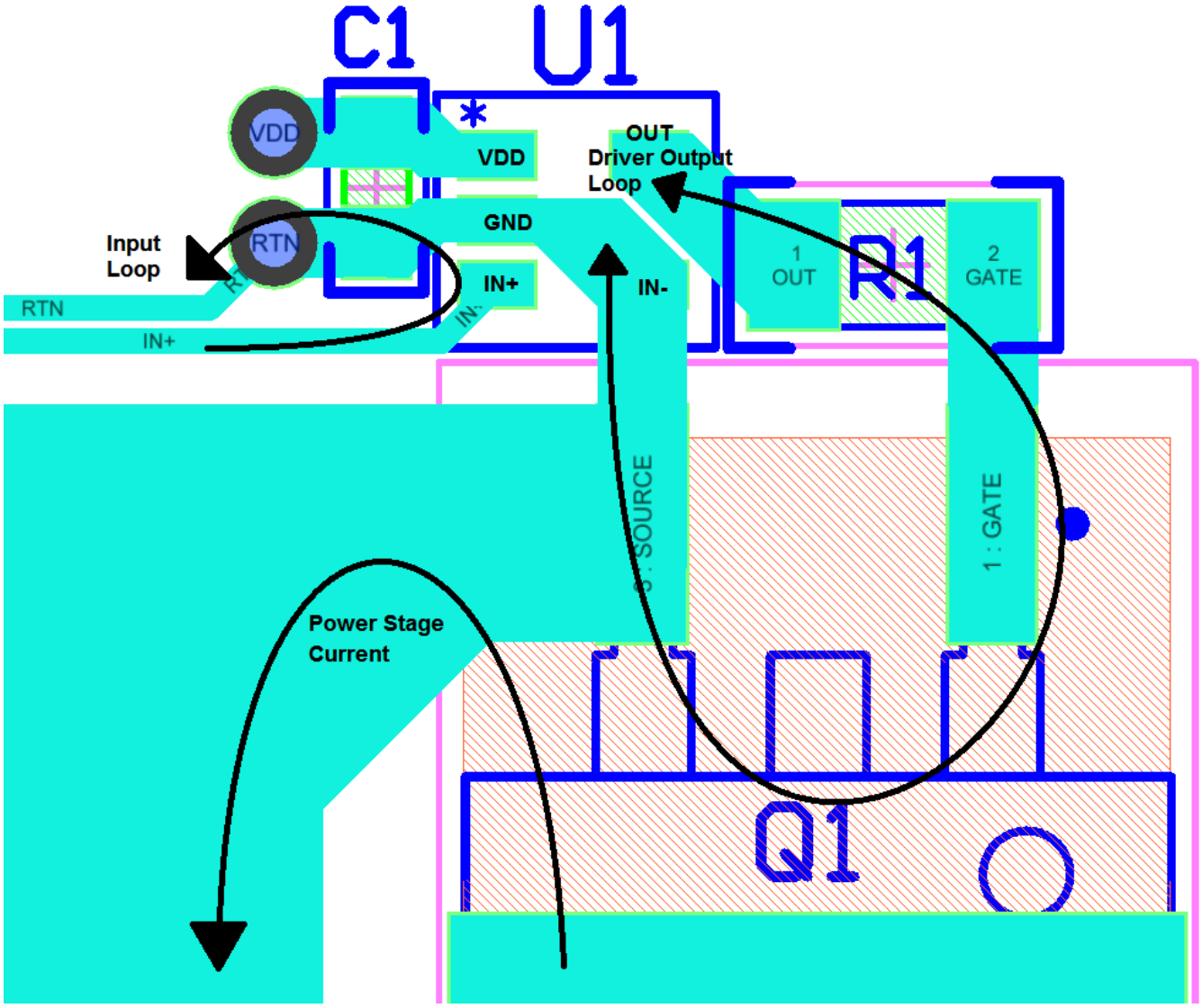


Figure 26. UCC27517ADBVQ1 in Noninverting Configuration

12.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive-power requirements of the load and the thermal characteristics of the package. In order for a gate driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package is summarized in the *Specifications* section of the datasheet. For detailed information regarding the thermal information table, refer to the Application Note from Texas Instruments entitled *Semiconductor and IC Package Thermal Metrics* (SPRA953).

The UCC27517A-Q1 is offered in SOT-23, 5-pin package (DBV). The *Thermal Information* table summarizes the thermal performance metrics related to the package. θ_{JA} metric should be used for comparison of power dissipation between different packages. The ψ_{JT} and ψ_{JB} metrics should be used when estimating the die temperature during actual application measurements.

The DBV package heat removal occurs primarily through the leads of the device and the PCB traces connected to the leads.

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12.4 Power Dissipation

Power dissipation of the gate driver has two portions as shown in Equation 1.

$$P_{DISS} = P_{DC} + P_{SW} \quad (1)$$

The DC portion of the power dissipation is $P_{DC} = I_Q \times V_{DD}$ where I_Q is the quiescent current for the driver. The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections, and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through etc). The UCC27517-Q1 device features very-low quiescent currents (less than 1 mA, refer Figure 7) and contains internal logic to eliminate any shoot-through in the output-driver stage. Thus the effect of the P_{DC} on the total power dissipation within the gate driver can be safely assumed to be negligible.

The power dissipated in the gate-driver package during switching (P_{SW}) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage V_G, which is very close to input bias supply voltage V_{DD} due to low V_{OH} drop-out).
- Switching frequency.
- Use of external-gate resistors.

When a driver device is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly easy. The energy that must be transferred from the bias supply to charge the capacitor is given by Equation 2.

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2$$

Where

- C_{LOAD} is load capacitor
- V_{DD} is bias voltage feeding the driver

(2)

There is an equal amount of energy dissipated when the capacitor is charged. This leads to a total power loss given by Equation 3.

$$P_G = C_{LOAD} V_{DD}^2 f_{SW}$$

where

- f_{SW} is the switching frequency

(3)

The switching load presented by a power MOSFET/IGBT is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Qg, determine the power that must be dissipated when charging a capacitor. This is done by using the equation, $Q_G = C_{LOAD} \times V_{DD}$, to provide Equation 4 for power:

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} = Q_g V_{DD} f_{SW} \quad (4)$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET/IGBT is being turned on or turned off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate-drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated in Equation 5.

$$P_{SW} = 0.5 \times Q_G \times VDD \times f_{SW} \times \left(\frac{R_{OFF}}{R_{OFF} + R_{GATE}} + \frac{R_{ON}}{R_{ON} + R_{GATE}} \right)$$

where

- $R_{OFF} = R_{OL}$
- R_{ON} (effective resistance of pullup structure) = 1.4 x R_{OL}

(5)

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13 器件和文档支持

13.1 社区资源

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 要获得这份数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC27517AQDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EAGQ
UCC27517AQDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EAGQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF UCC27517A-Q1 :

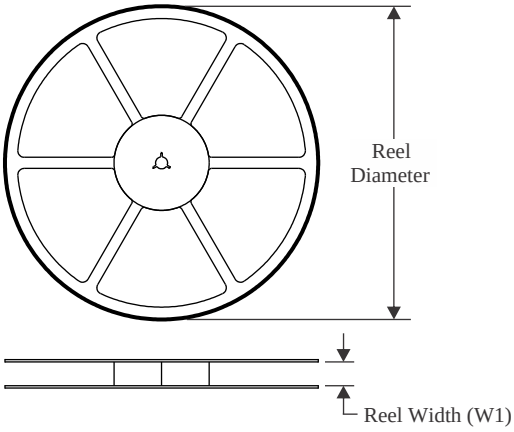
- Catalog : UCC27517A

NOTE: Qualified Version Definitions:

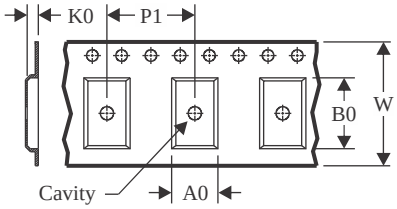
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

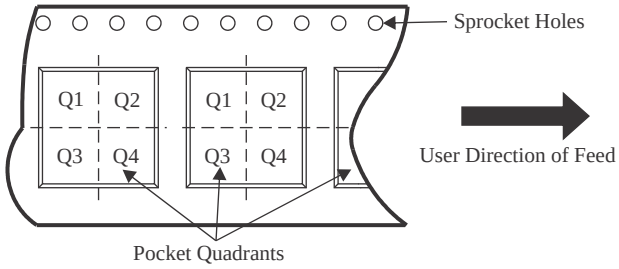


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

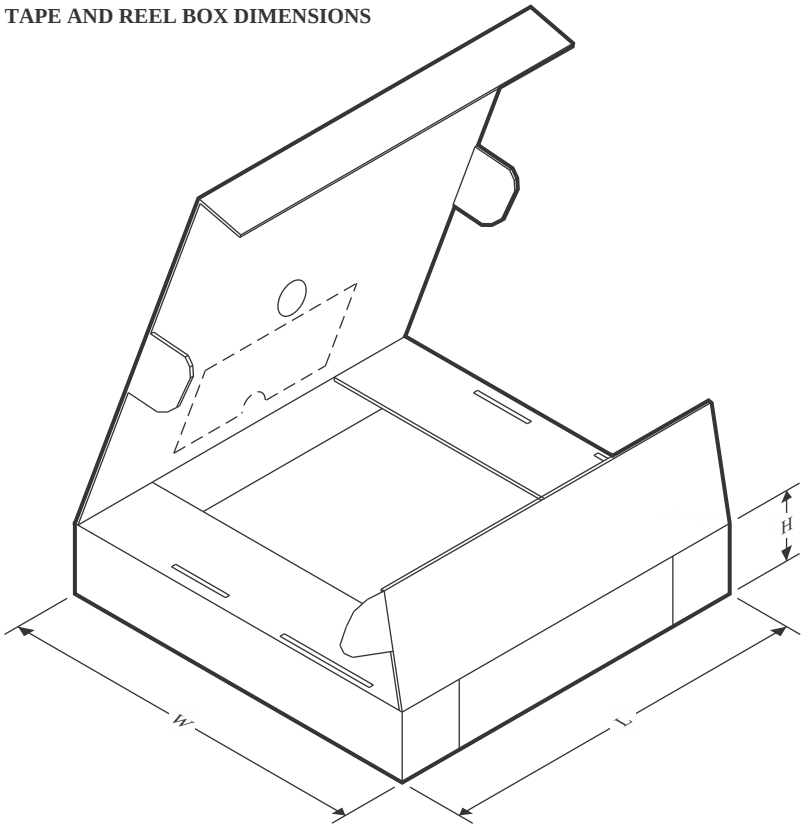
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27517AQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27517AQDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC27517AQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

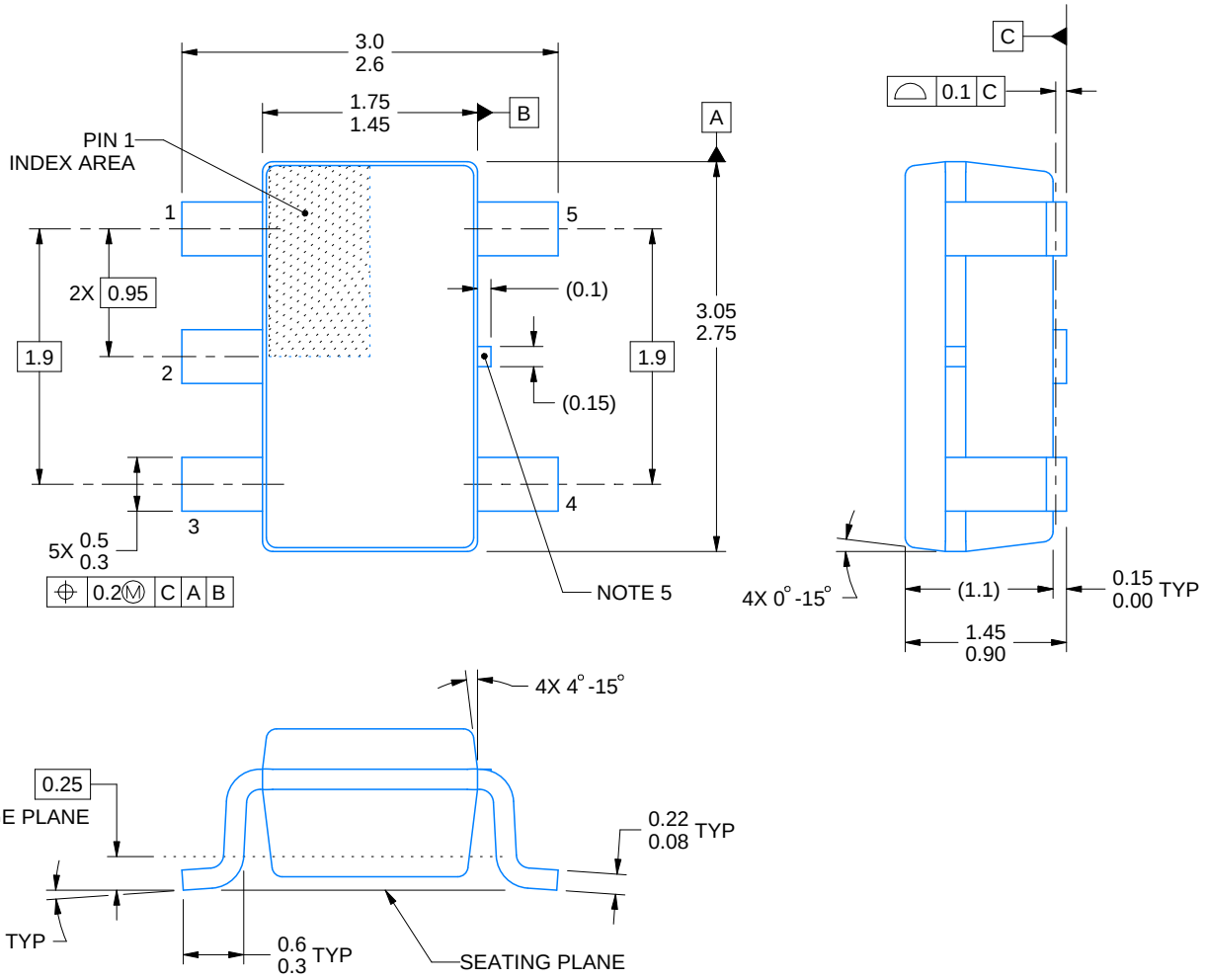
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27517AQDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
UCC27517AQDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
UCC27517AQDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

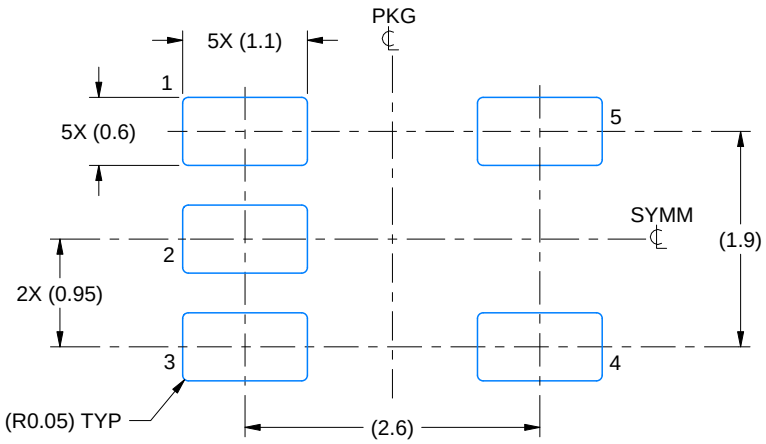
SMALL OUTLINE TRANSISTOR



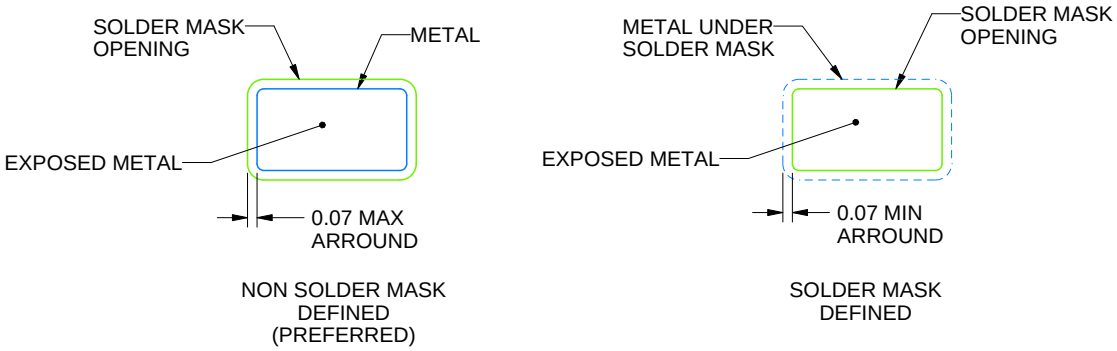
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

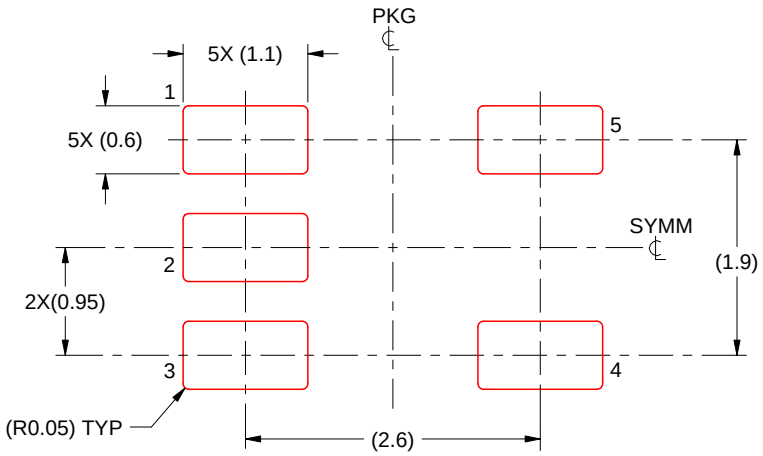


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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