适用于多串 **LED** 照明的 **UCC25710 LLC** 半桥控制器

1 特性

- 闭环 LED 灯串电流控制
- 脉宽调制 (PWM) 调光输入
- 可调 F_{MIN}（精度为 3%）和 F_{MAX}（精度为 7.5%）
- LLC 和串联 LED 调光开关控制
- 可编程的调光 LLC 开/关变化，消除可闻噪声
- 在低调光占空比时进行闭环电流控制
- 可编程软启动
- 精准的 V_{REF}，可实施严格的输出调节
- 具有自动重启响应的过压、低压和输入过流保护
- 具有闭锁响应的二级过流阈值
- 400mA/800mA 栅极驱动电流
- 低启动和工作电流
- 无铅 (Pb)、20 引脚、SOIC 封装

2 应用

- 适用于 LCD 电视和监视器的 LED 背光
- LED 通用照明

3 说明

UCC25710 器件是一款 LLC 半桥控制器，可精准控制多串 LED 背光 应用。该器件针对多变压器、多串 LED 架构进行了优化。借助该控制器和架构，可在多灯串中实现出色 LED 电流匹配。与现有的 LED 背光解决方案相比，该多变压器架构可提供从交流输入到 LED 负载的优异整体效率。

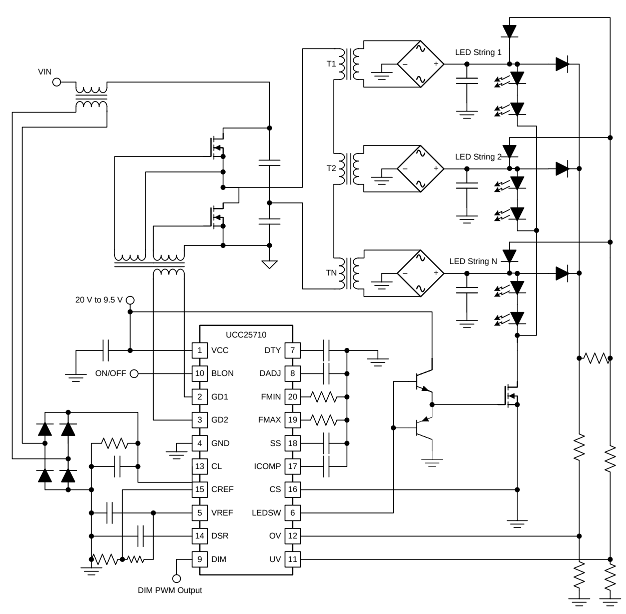
LLC 控制器功能包括具有可编程 F_{MIN} 和 F_{MAX} 的电压控制晶体振荡器 (VCO)、具有 500ns 固定死区时间的半桥栅极驱动器和 GM 电流放大器。LLC 功率传输由控制器的 VCO 频率进行调制。VCO 具有一个精确的可编程频率范围。在极低功耗水平下，VCO 频率由 F_{MAX} 转为零，从而最大限度地提升小 LED 电流下的效率。

器件信息(1)

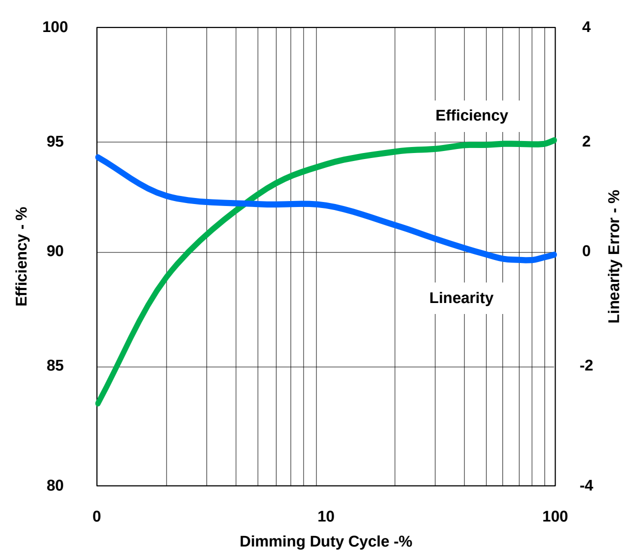
器件型号	封装	封装尺寸（标称值）
UCC25710	SOIC (20)	12.80mm x 7.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化应用示意图



效率和线性结果（**45W** 双灯串）



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (May 2011) to Revision B **Page**

- *已添加 ESD 额定值 表、特性 说明 部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分* ... 1

5 说明 （续）

LED 电流环路基准电压由分压器以 V_{REF} 5V 输出进行设定。该基准电压范围为 0.5V 至 2.6V，可将模拟调光与 PWM 调光相结合。

PWM 调光用于控制外部 LED 串联开关，还可导通和断开 LLC 功率级。LEDSW 输出借助一个简单的驱动器电路可用于接通和断开 LED 灯串电流。此输出可直接对调光输入 (DIM) 的输入信号作出响应。LLC 还可以随调光 PWM 输入而开启和关闭。开启和关闭的 LLC 调光边缘以可编程转换率改变，以便控制可闻噪声。调光功能包括占空比补偿，从而可优化最大范围内的整体效率和调光线性。

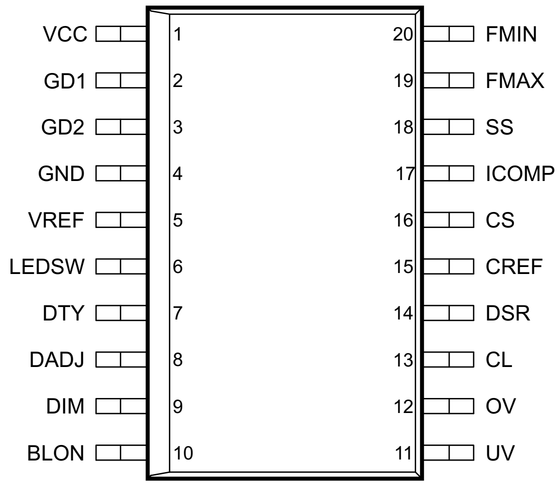
VCO 的控制电压由 ICOMP（电流放大器输出）在 LED 开启期间进行设定。在启动期间，软启动引脚 SS 会控制 VCO 响应，直至响应超出 ICOMP。在调光期间，VCO 输入的上升和下降速率由电压根据调光转换率、DSR 和引脚进行控制，而 VCO 控制消隐脉冲电平继续由 ICOMP 控制。电流放大器输出仅在命令的调光 LED 开启期间连接至 ICOMP。在低调光占空比期间，LLC 开启时间延长至超过 LED 电流接通时间，从而维持 LED 电流的闭环控制。

LED 灯串过压和欠压条件下的保护阈值由外部电阻分压器和精确的内部阈值设定。流入转换器的输入电流通过重启和闭锁响应进行监控，具体取决于过流级别。控制器还包括热关断保护。

针对任何故障的自动重启响应包括一个 10ms 重置周期和后续的软启动。如果出现严重的输入过流，则输入电源在其 UVLO 阈值内开启后才可启用重启。

6 Pin Configuration and Functions

DW Package
20-Pin SOIC
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VCC	P	Connect a DC power voltage to VCC. Bypass VCC to GND with a 0.47-µF or larger ceramic capacitor using short PC-board traces. VCC directly supplies power to the gate drivers and VREF which biases all circuit blocks in the UCC25710. Undervoltage lockout (UVLO) comparator prevents operation until VCC rises above V_{VCCON}.
2, 3	GD1&2	O	Gate drive outputs operate 180° out of phase with a fixed 500 ns of dead time. They typically drive either primary end of a gate drive transformer. At start-up or during a fault recovery, initiating the LLC converter begins with GD2 turning on first.
4	GND	P	The ground pin is both the reference pin for the controller and the low-side return for the gate drive signals. Take special care to return all AC decoupling as close as possible to this pin and avoid any common trace length with analog signal return paths.
5	VREF	O	The internal 5-V supply and reference rail is brought out to this pin. A small decoupling capacitor to ground of 1 µF is required. VREF can support up to 10-mA current external to the device. VREF is enabled when VCC is above V_{VCCON} and BLON is above V_{BLON}.
6	LEDSW	O	The LED switch output is a control signal to a series LED switch. This output is low during a low level at the DIM input and whenever the LLC converter is disabled. PWM dimming is disabled during soft start, and the LEDSW output is high independent of the DIM input. A simple gate drive circuit is generally required at this output to drive the external FET.
7	DTY	I/O	The duty-cycle pin is averaged with a capacitor to ground to form a 1-D proportional voltage that is compared to the D_{ADJ} saw tooth voltage. The average voltage at this pin is 2.5 V(1-D)+0.1 V, where D is the dimming PWM duty-cycle the DIM input.
8	DADJ	I/O	A capacitor to ground at the duty-cycle adjust input sets the positive slope of a saw tooth waveform that is compared to a voltage proportional to 1-D where D is the dimming PWM duty-cycle of the DIM input. At the falling edge of the DIM input this comparison is used to extend the LLC ON-time beyond the ON-time of the LED series switch.
9	DIM	I	A PWM input signal at the dimming pin controls the average load current by cycling on and off both an external series LED switch and the gate drives to the LLC converter. A high on this pin corresponds to an ON condition. The controller ignores a low condition at this input during start-up or fault recovery until after the completion of a soft-start sequence.
10	BLON	I	Backlight ON is an enable signal for the control device. The signal is active high with a threshold of approx 1.2 V. The 5-V reference (VREF) is enabled with BLON which is the bias supply for many of the internal blocks of the device.

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
11	UV	I	This pin is used to monitor for an undervoltage condition on the load. A level below V_{UVTH} on this pin causes the converter to disable the gate drive outputs as well as the LEDSW output. Immediately, a T_{RSTDLY} (10 ms) reset delay and soft-start sequence is initiated. The reset delay and soft-start sequence is repeated as long at the UV pin is low at the end of the sequence.
12	OV	I	This pin is used to monitor for an overvoltage condition on an LED string. A level above V_{OVTH} on this pin causes the converter to disable the gate drive outputs as well as the LEDSW output. If the OV input falls below its trip threshold the converter responds with a T_{RSTDLY} (10 ms) reset delay and soft start.
13	CL	I	Current limit input connects to a signal that represents the power converter’s input current. Dual thresholds provide a shutdown retry or latch-off response.
14	DSR	I/O	The dimming slew rate pin is used to limit the rate of the VCO frequency change at the LLC on or off edges of a dimming PWM cycle. A capacitor to ground at this pin programs the maximum positive and negative slew rates that appear at the control input to the VCO. Pulling this pin below about 0.8 V disables the GD outputs.
15	CREF	I	Current Reference is used to set the regulating voltage for the LED current feedback signal at the CS input. This voltage input is set using a resistor divider from VREF. A nominal level of around 0.7 V is recommended although a range of 0.6 V to 2.7 V is accommodated. Internal reference levels of 0.5 V and 2.8 V replace the CREF input voltage at the current amplifier when the CREF pin voltage is respectively below or above these levels. The 0.5-V internal reference can be achieved by shorting CREF to ground, the internal 2.8-V reference can be achieved by shorting CREF to VREF.
16	CS	I	Current sense input monitors the LED current. This signal is compared to V_{CREF} by the current amplifier to regulate the total LED current.
17	ICOMP	O	This output pin is used to compensate the current regulating loop. A capacitor, or capacitor resistor series combination is typically used. During current regulation the voltage into the VCO is slaved to this pin. Pulling this pin below about 0.8 V disables the GD outputs. During PWM dimming OFF-time this pin is tri-stated and the compensation network is meant to hold the proper LLC control voltage until the LLC converter is turned back on. To optimize this operation any DC loading on this pin must be avoided.
18	SS	I/O	The soft-start pin is used to control the rate of change of the VCO frequency during start-up. At start-up a low value pullup current source, I_{SS}, is applied to this pin. A soft-start sequence is initiated at start-up and during any fault recovery. The SS pin must charge to 4.2 V before the controller allows PWM dimming to take place.
19	FMAX	I/O	The maximum frequency of the LLC converter is set by a resistor to ground at this pin. It is actually the difference between the maximum and minimum frequency that is set by this resistor.
20	FMIN	I/O	The minimum frequency of the LLC converter is set by a resistor to ground at this pin.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_{CC}		20	V
LEDSW output current	I_{LEDSW}		±2	mA
VREF output current	I_{VREF}		–20	
Gate drive RMS current continuous GD1, GD2	I_{GD1}, I_{DG2}		25	
Gate drive voltage, GD1 GD2	V_{GD1}, V_{GD2}	–0.5	V_{CC} + 0.5	V
Voltage	CS, CL, OV, UV, BLON, DIM, CREF	–0.5	7	
Lead temperature 1.60 mm (1/16 inch) from case for 10 s			260	°C
Operating junction temperature, T_J		–55	150	
Storage temperature, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

all voltages are with respect to GND; currents are positive into and negative out of the specified terminal. -40°C < T_J = T_A < 125°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Operating input voltage	11		18	V
C_{VCC}	VCC bypass capacitor	0.47			µF
	Operating junction temperature	–40		125	°C
	Switching frequency at gate drive outputs	25		350	kHz
V_{CREF}	Input voltage (linear range)	0.6	1.65	2.7	V
V_{CREF}	Input voltage (using internal clamps)	0		V_{VREF}	
C_{VREF}	VREF bypass capacitor	0.22	1	2.2	µF
C_{SS}	SS capacitor	10		250	nF
C_{ICOMP}	ICOMP capacitor	0.5		47	
C_{DTY}	DTY capacitor	0.22		6.8	µF
C_{DSR}	DSR capacitor	0		2500	pF

7.4 Thermal Information

THERMAL METRIC[1]		UCC25710 DW (SOIC) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	79	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16	°C/W
ψ_{JB}	Junction-to-board characterization parameter	44	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

T_A = –40°C to 125°C, $T_A = T_J$, V_{VCC} = 12 V, V_{BLON} = 3 V, V_{UV} = 3 V, V_{OV} = 2 , V_{CL} = 0 V, R_{MIN} = 100 kΩ, R_{MAX} = 4.99 kΩ, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY INPUT						
V_{VCCMAX}	VCC operating voltage				18	V
I_{OFF}	Supply current, off	V_{VCC} = 8 V		160	250	µA
I_{ON}	Supply current, on	Switching frequency = F_{MIN} (30 KHz)		1.4	2.1	mA
$I_{DISABLE}$	Supply current, disabled	V_{VCC} = 12 V, V_{BLON} = 0 V		240	350	µA
$I_{LATCHOFF}$	Supply current, latched off	Fault latch set		600	900	µA
UNDERVOLTAGE LOCKOUT						
V_{VCCON}	VCC turnon threshold	V_{VCC} low-to-high	8.6	9.3	10.1	V
V_{VCCOFF}	VCC turnoff threshold	V_{VCC} high-to-low	8.3	9	9.6	V
V_{VCCHYS}	Hysteresis		0.2	0.35	0.5	V
5-V REFERENCE OUTPUT						
V_{VREF}	5-V Reference	I_{VREF} = 0 to 10 mA, T_J = 25°C	4.95	5	5.05	V
V_{VREF}	5-V Reference	I_{VREF} = 0 to 10 mA, T_J = –40°C to 125°C	4.85	5	5.15	V
CURRENT AMPLIFIER						
$V_{ICOMPIOS}$	Input offset voltage	V_{CREF} = 1.65 V, I_{COMP} tied to CS	–15		15	mV
I_{CS}	Input bias current at CS input	V_{CREF} = 1.65 V, V_{CS} = 1.65 V	–0.25		0.25	µA
I_{CR}	Input bias current at CREF input	V_{CREF} = 1.65 V, V_{CS} = 1.65 V	–0.25		0.25	µA
$V_{ICOMPHI}$	ICOMP high	V_{CS} = 0 V, V_{CREF} = 1.65 V, I_{ICOMP} = 50 µA	4.6	4.85		V
$V_{ICOMPLO}$	ICOMP low	V_{CS} = 3 V, V_{CREF} = 1.65 V, I_{ICOMP} = –50 µA		0.35	0.65	V
GM_{ICOMP}	ICOMP transconductance	I_{COMP} tied to C_S, I_{ICOMP} = –100 µA to 100 µA	440	510	600	µs
$I_{ICOMPSRC}$	Source current ICOMP	V_{CS} = 0.65 V, V_{CREF} = 1.65 V, V_{ICOMP} = 2.5 V	120	150	180	µA
$I_{ICOMPSNK}$	Sink current ICOMP	V_{CS} = 2.65 V, V_{CREF} = 1.65 V, V_{ICOMP} = 2.5 V	195	245	295	µA
$I_{ICOMPLGK}$	LED off leakage current at ICOMP	V_{DIM} = 0 V, V_{ICOMP} = 2.5 V, T_J = –40°C to 85°C	–0.1		0.1	µA
$V_{CREFCLO}$	CREF low Clamp	V_{CREF} = 0 V, ICOMP tied to CS, regulating voltage at ICOMP	0.475	0.5	0.535	V
$V_{CREFCHI}$	CREF high Clamp	V_{CREF} = 3 V, ICOMP tied to CS, regulating voltage at ICOMP	2.65	2.8	2.95	V

Electrical Characteristics (continued)

T_A = –40°C to 125°C, T_A = T_J, V_{VCC} = 12 V, V_{BLON} = 3 V, V_{UV} = 3 V, V_{OV} = 2 , V_{CL} = 0 V, R_{MIN} = 100 kΩ, R_{MAX} = 4.99 kΩ, (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOFT START						
I_{SS}	Soft-start charging current	V_{SS} = 2.25 V	2	2.5	3	µA
R_{SSDC}	Soft-start discharge resistance	V_{SS} = 1 V		3.4	5	kΩ
V_{SSTH}	Soft-start threshold	SS clamp released	3.95	4.15	4.4	V
T_{RSTDLY}	Reset delay	From UVLO turnon to start of soft start	7	10	13	ms
VOLTAGE CONTROLLED OSCILLATOR						
F_{MIN}	F_{MIN} GD1, GD2	R_{MIN} = 100 kΩ, V_{ICOMP} = 5 V	29.5	30.5	31.5	kHz
F_{MAX}	F_{MAX} GD1, GD2	R_{MIN} = 100 kΩ, R_{MAX} = 4.99 kΩ, V_{ICOMP} = 0.95 V	275	300	320	
T_{DT}	Dead-time GD1, GD2	R_{MIN} = 100 kΩ, V_{ICOMP} = 3 V	400	500	600	ns
T_{MATCH}	ON-time mismatching	R_{MIN} = 100 kΩ, V_{ICOMP} = 3 V	–50		50	
$V_{VCOTHLO}$	V_{ICOMP} VCO Threshold Low	Disable GD1, GD2, V_{ICOMP} high to low	0.8	0.9	0.95	V
V_{VCOMAX}	V_{ICOMP} for F_{MIN}	Frequency reaches F_{MIN}	3.8	4	4.2	
GATE DRIVERS						
V_{GDHI}	GD1, GD2 V_{OUT} high	I_{GD1}, I_{GD2} = –20 mA, below VCC		1.8	3	V
$R_{GDHSRES}$	GD1, GD2 ON-resistance high	I_{GD1}, I_{GD2} = –20 mA		14	30	Ω
V_{GDLO}	GD1, GD2 V_{OUT} low	I_{GD1}, I_{GD2} = 20 mA		0.08	0.2	V
$R_{GDLSRES}$	GD1, GD2 ON-resistance low	I_{GD1}, I_{GD2} = 20 mA		4	10	Ω
T_{GDRISE}	GD1, GD2 output rise time	C_{GD} = 1 nF, 1 V to 9 V		25	35	ns
T_{GDFALL}	GD1, GD2 output fall time	C_{GD} = 1 nF, 9 V to 1 V		20	30	
UNDERVOLTAGE PROTECTION						
V_{UVTH}	Undervoltage threshold	High-to-low on UV input	2.27	2.4	2.53	V
V_{UVHY}	Undervoltage threshold hysteresis		190	240	300	mV
I_{UV}	UV input bias current	V_{UV} = 2.7 V	–0.25		0.25	µA
OVERVOLTAGE PROTECTION						
V_{OVTH}	Overvoltage threshold	Low-to-high on OV input	2.46	2.6	2.74	V
V_{OVHY}	Overvoltage threshold hysteresis		190	240	300	mV
I_{OV}	OV input bias current	V_{OV} = 2.3 V	–0.25		0.25	µA
CURRENT LIMIT PROTECTION						
V_{CLTH}	Current limit threshold	Low-to-high on CL input	0.9	0.95	1	V
V_{CLHY}	Current limit threshold hysteresis		375	475	525	mV
V_{CLLTH}	Current limit latching threshold	Low-to-high on CL input	1.75	1.9	2.05	V
I_{CL}	CL input bias current	V_{CL} = 2.2 V	–0.25		0.25	µA
THERMAL SHUTDOWN						
t_{TSD}	Junction temperature at thermal shutdown	Temperature rising	135	160	185	°C
t_{HYS}	Thermal hysteresis			25	45	
BACKLIGHT ON INPUT						
R_{BLON}	RBLON pulldown resistance	Pull down to GND	100	200	350	kΩ
V_{BLON}	Enable threshold		0.8	1.2	1.6	V

Electrical Characteristics (continued)

T_A = –40°C to 125°C, T_A = T_J, V_{VCC} = 12 V, V_{BLON} = 3 V, V_{UV} = 3 V, V_{OV} = 2 , V_{CL} = 0 V, R_{MIN} = 100 kΩ, R_{MAX} = 4.99 kΩ, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM DIMMING						
V_{DIM}	Dimming input threshold		1.2	1.5	1.8	V
R_{DIM}	DIM pullup resistance	Pullup resistance to VREF, V_{DIM} = 0 V – 4.5 V	140	180	240	kΩ
$V_{LEDSWHI}$	High-level at LEDSW output	I_{LEDSW} = –100 µA, below VCC, V_{DIM} = 3 V		0.4	1	V
$V_{LEDSWLO}$	Low-level at LEDSW output	I_{LEDSW} = 100 µA, V_{DIM} = 0 V		0.2	0.5	V
$R_{LEDSWHI}$	High-level output resistance	I_{LEDSW} = –500 µA – 0 µA, V_{DIM} = 3 V		4	6	kΩ
$R_{LEDSWLO}$	Low-level output resistance	I_{LEDSW} = 500 µA – 0 µA, V_{DIM} = 0 V		2	3	kΩ
R_{DTY}	DTY output resistance	V_{DTY} = 0 V – 2.5 V , V_{DIM} = 0 V	30	40	50	kΩ
V_{DTYH}	DTY max level	V_{DIM} = 0 V	2.45	2.6	2.7	V
V_{DTYL}	DTY min level	V_{DIM} = 3 V	0.05	0.1	0.15	V
I_{DADJCH}	DADJ charging current	V_{DADJ} = 2.5 V, V_{DIM} = 0 V	16	20	25	µA
R_{DADJDC}	DADJ discharge resistance	V_{DADJ} = 0.5 V, V_{DIM} = 3 V		1	1.5	kΩ
T_{DADJ}	DADJ delay	C_{ADJ} = 2.2 nF, V_{DTY} = 2.6 V, delay from DIM high-to-low to DSR discharge	225	275	330	µs
I_{DSRCH}	DSR slew rate charge current	V_{DSR} = 2.5 V, V_{ICOMP} = 4 V, V_{DIM} = 3 V	38	44	50	µA
I_{DSRDC}	DSR slew rate discharge current	V_{DSR} = 2.5 V, V_{ICOMP} = 4 V, V_{DIM} = 0 V	38	44	50	µA
V_{DSRCL}	DSR clamp above ICOMP	V_{ICOMP} = 2 V, level above V_{ICOMP}	0.45	0.7	0.95	V

7.6 Typical Characteristics

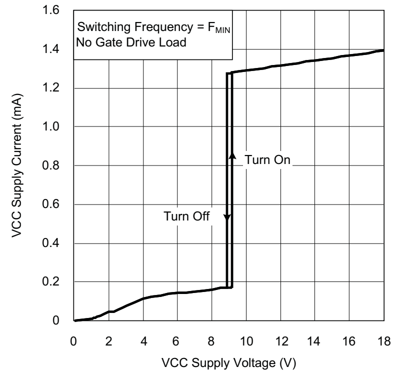


Figure 1. Supply Current vs Dimming Duty Cycle

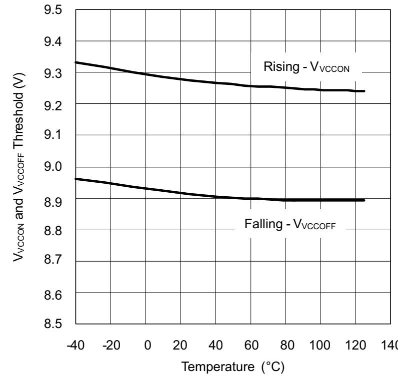


Figure 2. VVCCON and VVCOFF Threshold vs Temperature

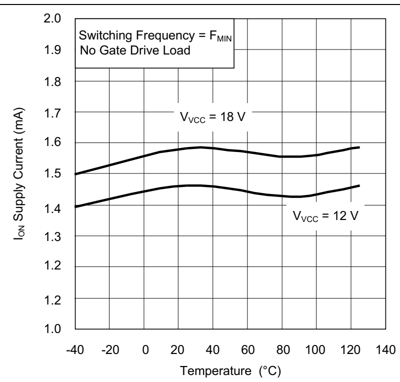


Figure 3. Supply Current vs Temperature

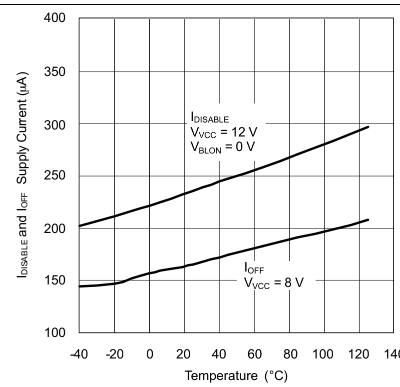


Figure 4. IDISABLE and IOFF Supply Current vs Temperature

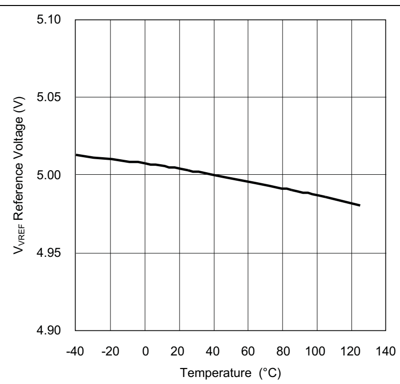


Figure 5. Reference Voltage vs Temperature

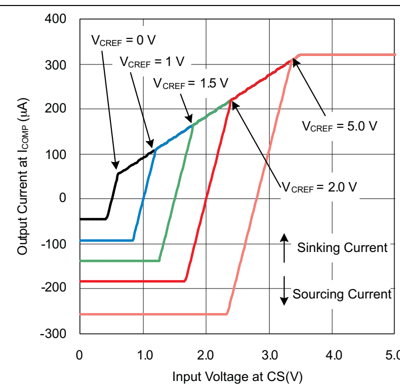


Figure 6. Output Current (ICOMP) vs Input Voltage (CS)

Typical Characteristics (continued)

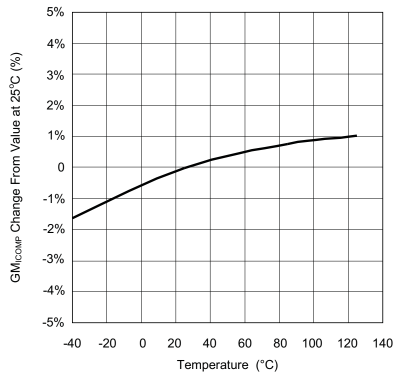


Figure 7. GMICOMP vs Temperature

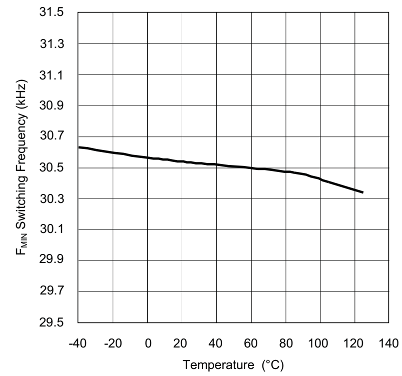


Figure 8. Minimum Switching Frequency vs Temperature

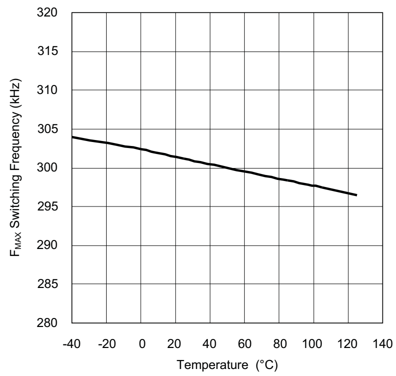


Figure 9. Maximum Switching Frequency vs Temperature

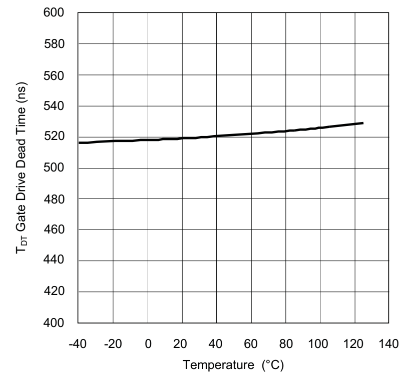


Figure 10. Gate Drive Dead Time vs Temperature

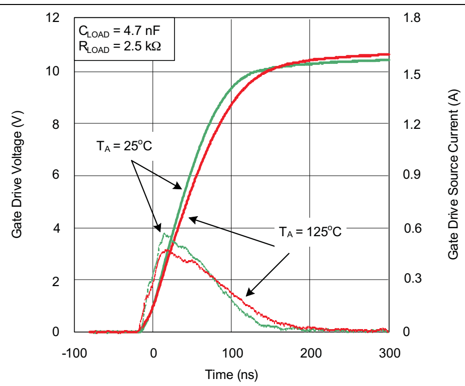


Figure 11. Gate Driver Outputs (Rising Edge) vs Time

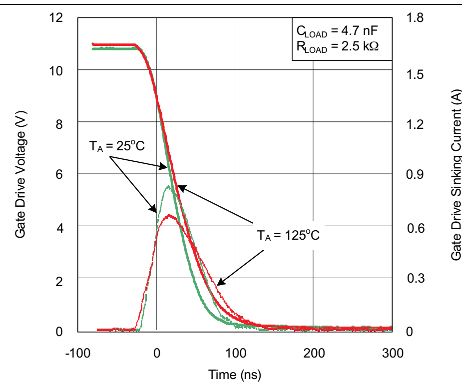


Figure 12. Gate Driver Outputs (Falling Edge) vs Time

Typical Characteristics (continued)

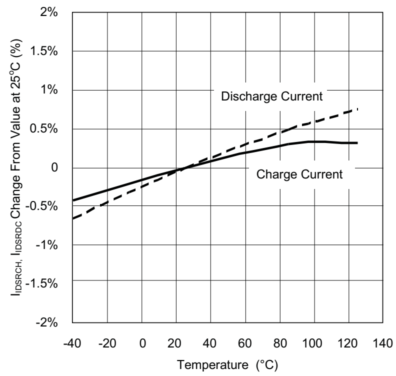


Figure 13. DSR Currents vs Temperature

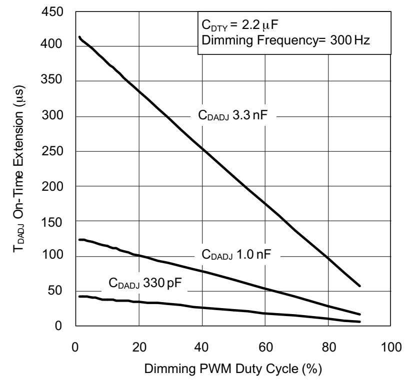


Figure 14. LLC ON-Time Extension vs Dimming Duty Cycle

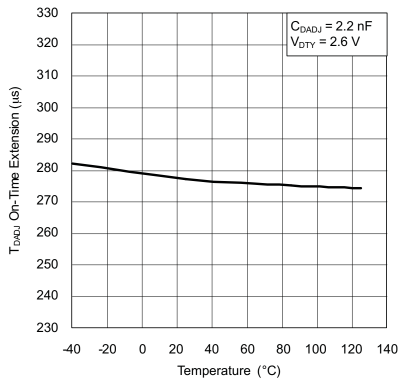


Figure 15. LLC ON-Time Extension vs Temperature

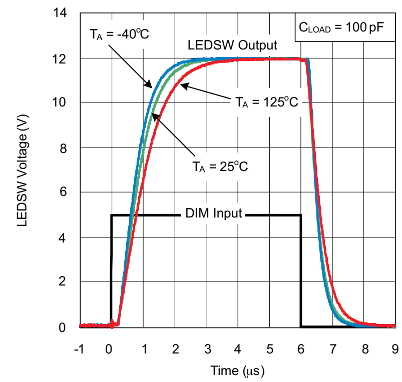


Figure 16. LEDSW Rise and Fall vs Time

8 Detailed Description

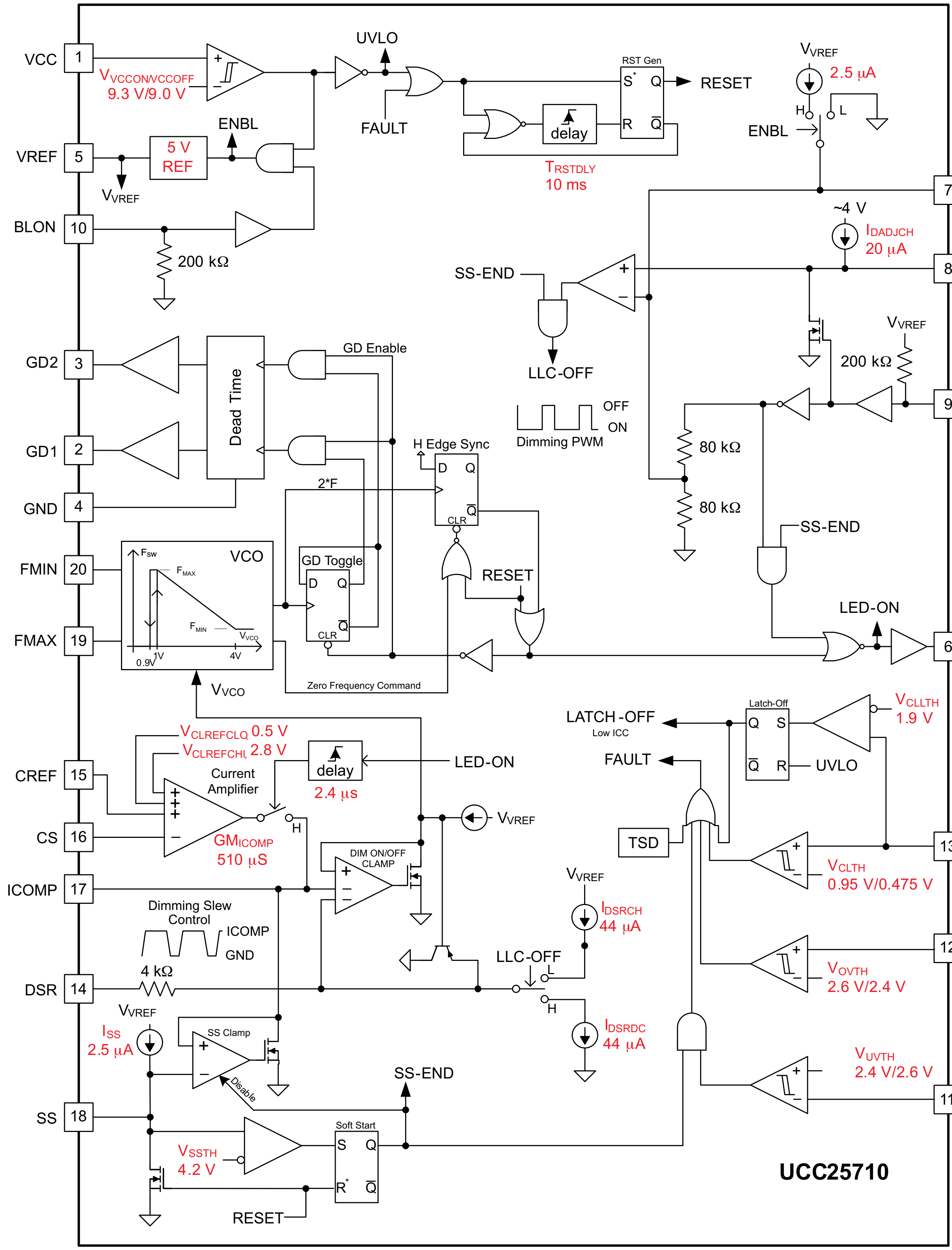
8.1 Overview

The UCC25710 is a highly integrated LLC controller designed specifically for multi-string LED lighting applications. The half-bridge LLC control is combined with independent PWM dimming or non-dimming of the LED current for control of the light output.

The UCC25710 is designed to provide power from a high voltage DC bus, such as the output from a PFC stage. Input over current-sensing protects the system in the event of a fault and gate drive outputs provide the drive signals to the LLC stage. Output overvoltage and undervoltage provide additional protection. LED current is sensed with a resistor in series with the LED’s. The UCC25710 has separate enable and dimming inputs.

This arrangement of a multi-transformer architecture, as shown in Figure 25, results in a highly efficient power supply.

8.2 Functional Block Diagram



8.3 Feature Description

Signal names and pin functions are depicted in *Functional Block Diagram*.

8.3.1 Multi-transformer Architecture

The multi-transformer LED driver architecture is a very attractive solution for driving multiple LED strings at the same current using a single power train and control device. Excellent LED string current matching from string to string (<1%) excellent LED current linearity from 1% to 100% dimming (<2%), and high efficiency can be achieved (>94%). Because this architecture is intended to use the 400-V output of the PFC stage, there is a significant cost advantage over typical LED backlight implementations because a power stage can be eliminated.

The architecture and UCC25710 control device are based on the LLC resonant half-bridge topology. The controller feedback loop is configured to regulate the total LED current typically with a current-sense resistor. The arrangement of the transformers with the primaries in series provides excellent LED string current matching. Because the primaries are in series, the current in each transformer primary is the same. The secondary current is the primary current times the turns ratio. The net primary magnetizing current is circulated in the primary side of the half bridge and does not affect the current transferred to the outputs. In each transformer, differences in magnetizing current caused by different magnetizing inductance or winding voltage will cause a difference in current transferred to the LED outputs, although the difference in transferred current is minimal with typical transformer tolerances and following the guidance in the *Determining Transformer and Resonant Circuit Parameters* below.

The UCC25710 includes all of the functions necessary to implement a total LED backlight driver including GM current amplifier, VCO, reference regulator, soft start, dimming duty cycle compensation and protection for OV, UV, current limit, and thermal shutdown. There are additional features to minimize audible noise during dimming and provide fast LED current rise and fall times.

8.3.2 Start-Up and Non-Dimming Operation

The UCC27510 is enabled when V_{CC} exceeds the V_{VCCON} threshold and BLON is high. At this time the soft-start cycle is initiated following a 10-ms reset delay. A 2.5-µA current source charges the capacitor connected to the SS pin to generate the soft-start ramp. During the soft-start cycle the current amplifier output (ICOMP) is clamped to be equal to or less than SS voltage. The voltage on ICOMP controls the VCO. V_{ICOMP} achieves the steady state operating point to regulate the total LED current during the soft-start rise time. The DIM input and the UV input are disabled during soft start to allow the output capacitors to charge to the steady-state operating voltage. When the SS pin reaches the V_{SSTH} threshold the SS-END signal transitions high indicating the end of the soft-start cycle. At this time the UV comparator and DIM input are enabled. See Figure 17 for the timing relationship during soft start.

Feature Description (continued)

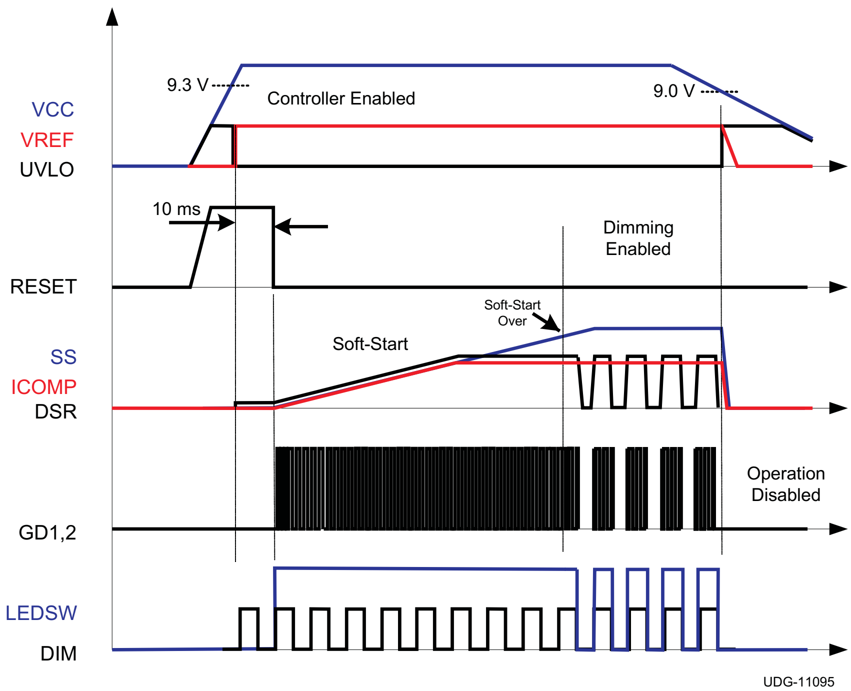


Figure 17. Start-Up Timing Diagram

8.3.3 Dimming Operation

Once the soft-start cycle is complete, the LEDSW output and control of the VCO depend on the DIM input. The dimming input signal controls the LEDSW output maintaining an accurate ON-time relationship between the DIM pulse width and LED current pulse width; the internal control signal is LED-ON. The LED-ON signal also controls a switch between the GM current amplifier output and the ICOMP pin. On the DIM rising edge the switch from the amplifier to the ICOMP pin is turned on after a 2.4-µs delay. The small delay time allows time to turn on the LED switch MOSFET. On the DIM falling edge the switch between the GM amplifier is turned off. During the DIM OFF-time the compensation capacitor at the ICOMP pin holds the correct steady-state operating voltage for the current loop. It is important that any DC loading of this pin is kept to an absolute minimum or current errors results as the dimming duty-cycle is reduced.

The LLC power stage is gated on and off during dimming with the dimming input signal. The UCC25710 allows control of the slew rate of the LLC power delivery at the rising and falling edges of a dim cycle allowing potentially audible electro-mechanically induced noise to be minimized. In addition, the falling, or turnoff, edge of a dimming cycle can be delayed, allowing the current loop to maintain control at low dimming duty-cycles even when the ramp rates have been slowed. See Figure 18.

Feature Description (continued)

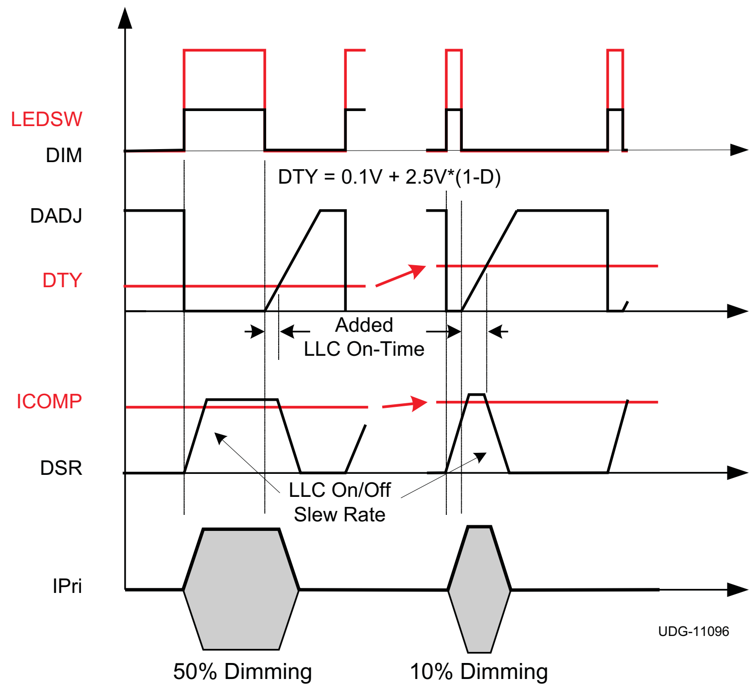


Figure 18. Dimming Timing Diagram

The power through the LLC converter is inversely proportional to the frequency of the VCO. The VCO frequency, in turn, is inversely proportional to the VCO control signal. See Figure 19 for details of this relationship. The dimming input generates an LLC-OFF signal that is used to select either a charging or discharging state for a capacitor applied to the DSR pin. The ±44 µA of current and associated capacitor set a ramp rate for the rise and fall of the DSR voltage. The control voltage to the VCO is dominated by the DSR voltage when the DSR voltage is less than the ICOMP pin – allowing the falling ramp on the DSR pin to softly turnoff the LLC power stage and softly return it to the same operating state as it rises.

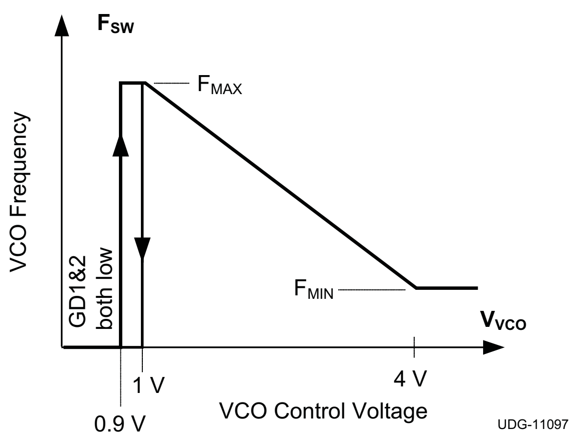


Figure 19. VCO Characteristics

The LLC-OFF signal is an inverted version of the dimming input signal. The falling edge of LLC-OFF is synchronized with the rising edge of the DIM signal. At a negative DIM edge the DADJ and DTY signals are combined to delay the rising edge of LLC-OFF providing a duty-cycle compensation time that is a function of the dimming duty cycle.

Feature Description (continued)

Averaged by a capacitor at the DTY pin, the voltage on DTY is inversely proportional to the dimming duty cycle; the voltage is

$$0.1\text{ V} + 2.5\text{ V} \times (1\text{-D}) \tag{1}$$

where

- D is the dimming PWM duty-cycle

The DTY voltage range is 100 mV at 100% DIM duty-cycle, or LED current continuously on, to 2.6 V at 0% DIM duty cycle, or LED current continuously off. The DADJ pin 20-µA current source is allowed to charge the pin capacitor after a DIM falling edge. The LLC-OFF signal transitions high when the capacitor on DADJ charges to the voltage on DTY. See Figure 18 for the timing relationship during dimming. The scope plots in Figure 20 and Figure 21 below show an example LED driver at 10% and 50% DIM duty cycle.

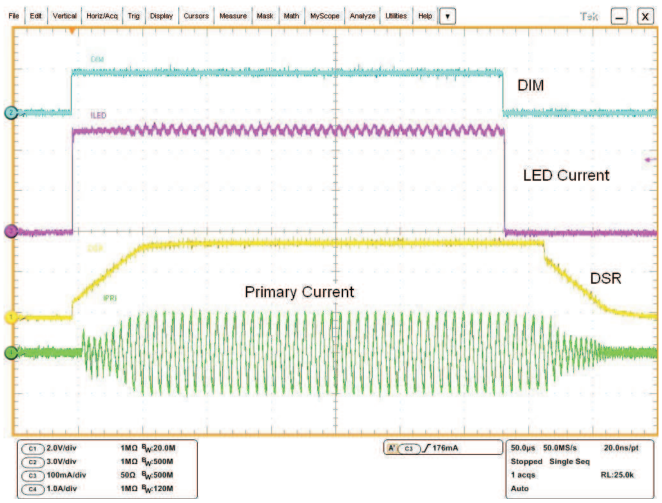


Figure 20. DIM 10% at 300 Hz

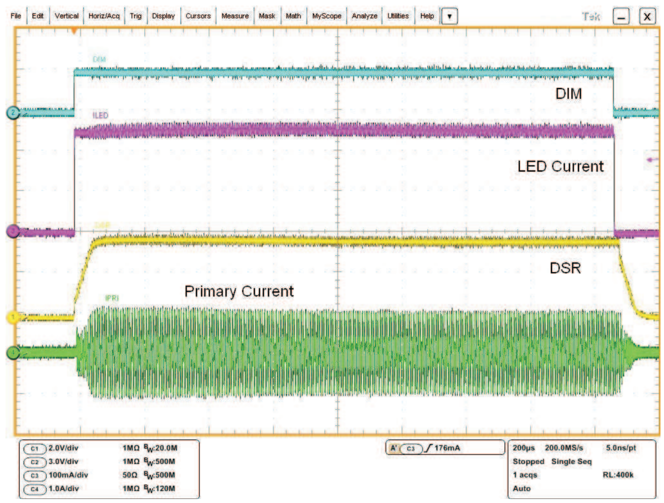


Figure 21. DIM 50% at 300 Hz

8.3.4 Fault Condition Operation

The UCC25710 has a similar response to overvoltage, thermal shutdown and current limit faults. Figure 22 shows the fault response. The OV input has a 2.6-V threshold and 240 mV of hysteresis. When OV is above 2.6 V the internal FAULT signal is active which results in the RESET signal going high. With RESET high the gate drivers are disabled, the SS pin is discharged to ground, and the LEDSW output is turned off. When OV is below 2.36 V the FAULT signal is inactive which starts the 10-ms SS clamp timer.

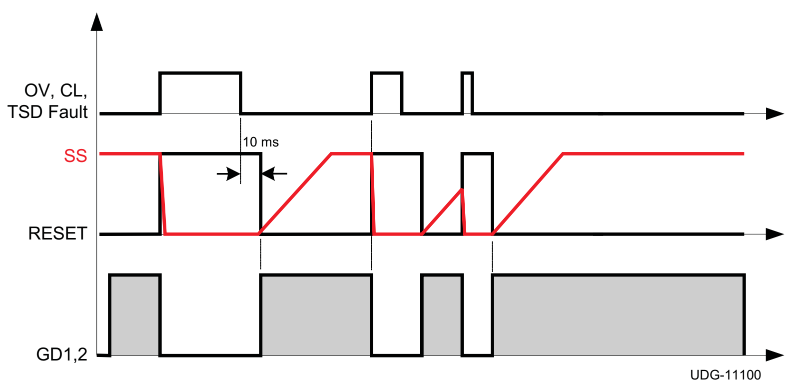


Figure 22. OV, CL(1 V) and TSD Fault Timing Diagram

Feature Description (continued)

RESET is extended 10 ms beyond FAULT going low. After the 10-ms soft-start timer the normal soft-start sequence begins. Thermal shutdown generates the same internal FAULT signal when the internal temperature reaches 160°C and a restart sequence begins after the junction temperature drops by the 25°C of threshold hysteresis.

The current limit comparator has two thresholds. The lower threshold of 0.95 V results in a shutdown and restart as described for OVP, the OC pin has 0.475 V of hysteresis. The second current limit threshold of 1.9 V results in a latch-off fault. VCC must be recycled below the V_{CCOFF} threshold to reset the latched OC fault.

The undervoltage fault has a different response to allow the converter to charge the output capacitors in a normal start-up condition. Because UV is disabled during soft start, a sustained UV fault results in a 10-ms soft-start clamp time plus the time required for the SS pin to charge to V_{SSTH} which is 4.15 V. See Figure 23 for UV fault condition timing diagrams.

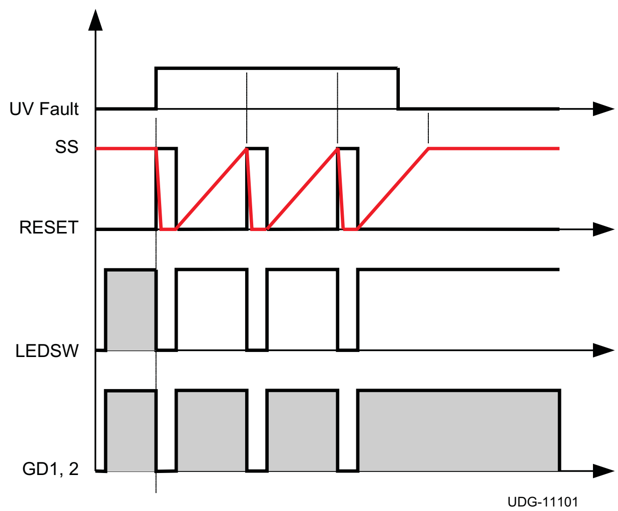


Figure 23. UV Fault Timing Diagram

8.4 Device Functional Modes

The device has two functional modes: non-dimming and dimming.

In the non-dimming mode the DIM input pin is held high (above 1.5 V typically)

In the dimming mode the DIM pin is switched between high and low levels.

The dimming slew rate controls the rate of change between the high and low LED currents.

This is set with a capacitor on the DSR input pin.

Additionally, a capacitor on the DADJ input pin extends the falling edges of the dimming cycle.

This allows for control at very low dimming ratios.

9 Application and Implementation

NOTE

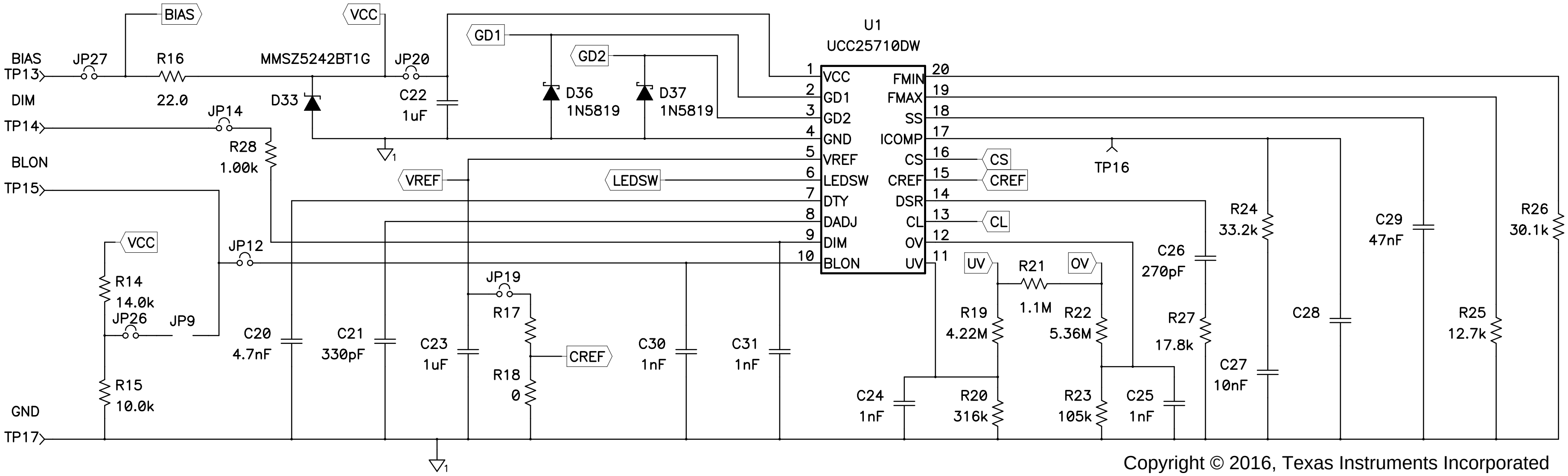
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The UCC25710 offers a highly integrated solution for LLC control of LED lighting. To the part easier to use, TI has prepared an extensive set of materials to demonstrate the features of the device. The UCC25710 offers a highly integrated feature-set and excellent accuracy to control the LED current in highly efficient LLC type power supplies with dimming or without dimming requirements.

9.2 Typical Application

To take advantage of all the benefits integrated in this controller, the following procedure simplifies the setup to avoid unnecessary iterations in the design procedure. See Figure 24 setup for component names.



▲ Note parts with no value are populated

Figure 24. UCC25710 Controller Setup

9.2.1 Design Requirements

Table 1 lists the design parameters of this example.

Table 1. Design Parameters

PARAMETER		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
V_{IN}	Input voltage	370	390	410	V
I_{IN}	Input current		0.275		A
OUTPUT1, OUTPUT2, OUTPUT3, OUTPUT 4 CHARACTERISTICS					
V_{LED1}, V_{LED2}, V_{LED3}, V_{LED4}	Output voltage set by LED load	96	98	100	V
I_{LED1}, I_{LED2}, I_{LED3}, I_{LED4}	Output current ripple			0.0125	A_{P-P}
I_{LED1}, I_{LED2}, I_{LED3}, I_{LED4}	Output current	0.245	0.25	0.255	A
I_{LED1}, I_{LED2}, I_{LED3}, I_{LED4}	Line regulation	0.245	0.25	0.255	
I_{LED1}, I_{LED2}, I_{LED3}, I_{LED4}	Load regulation	0.245	0.25	0.255	
V_{OVP}	Single output OVP		136		V
V_{UV}	Single output undervoltage		43		
	Dimming range	1%		100%	
	Dimming frequency	270	300	330	Hz
	Current matching between strings (10% to 100% dimming)	–2%		2%	
	Output power single output			24.5	W
	Full output power				
SYSTEM CHARACTERISTICS					
F_{SW}		84		156	kHz
η		91%	93%		

9.2.2 Detailed Design Procedure

9.2.2.1 Determining Transformer and Resonant Circuit Parameters

The muti-transformer architecture is similar to conventional LLC converter design with a few exceptions that are described in this section. Typical LLC voltage output converters are designed to operate nominally close to resonance and have the minimum switching frequency below resonance and maximum frequency above resonance. TI recommends operating above resonance at the nominal input voltage range of the converter to achieve good transient response during dimming and improved LED current matching. The transformer turns ratio equation shown is to target operation above resonance.

Use Equation 2 to calculate the turns ratio of the transformers in the multi-transformer architecture.

$$N = \frac{N_P}{N_S} = \frac{V_{IN}}{2 \times N_T \times V_{LED}}$$

where

- N is the primary to secondary turns ratio
- N_P is the primary turns
- N_S is the secondary turns
- V_{IN} is the input voltage to the LLC converter, typically the output of the PFC boost converter
- N_T is the number of transformers
- V_{LED} is the LED string voltage (2)

Another important consideration for the multi-transformer LED driver is to set the total magnetizing inductance of the transformers as high as possible to minimize the primary magnetizing current and it's effect on LED current matching. TI recommends targeting the total magnetizing inductance of the transformers to a value just low enough to achieve ZVS operation during nominal frequency operation. Equation 3 and Equation 4 determine the magnetizing inductance target. Reduce the calculated L_M to accommodate L_M and C_{OSS} tolerances.

$$I_{MPk} = \frac{2 \times C_{OSS} \times V_{IN}}{400\,ns} \tag{3}$$

$$L_m = \frac{V_{IN} \times \left(\frac{0.5}{F_{SW}} - 500\,ns \right)}{4 \times I_{MPk} \times N_T}$$

where

- I_{MPk} is the peak magnetizing current
- C_{OSS} is the MOSFET equivalent time related drain to source capacitance
- V_{IN} is the nominal input voltage to the half bridge, normally the PFC output voltage
- F_{SW} is the switching frequency at the regulation operating point
- L_M is the magnetizing inductance of each transformer
- N_T is the number of transformers with the primaries in series (4)

To use standard LLC converter design process and available tools such as SLUC253 design calculator available on the TI website, the multiple transformers and reflected loads can be combined into one equivalent transformer and load as shown in Figure 25. Once Lr and Lm are determined based on a single transformer circuit, simply divide by the number of transformers for each transformer specification target.

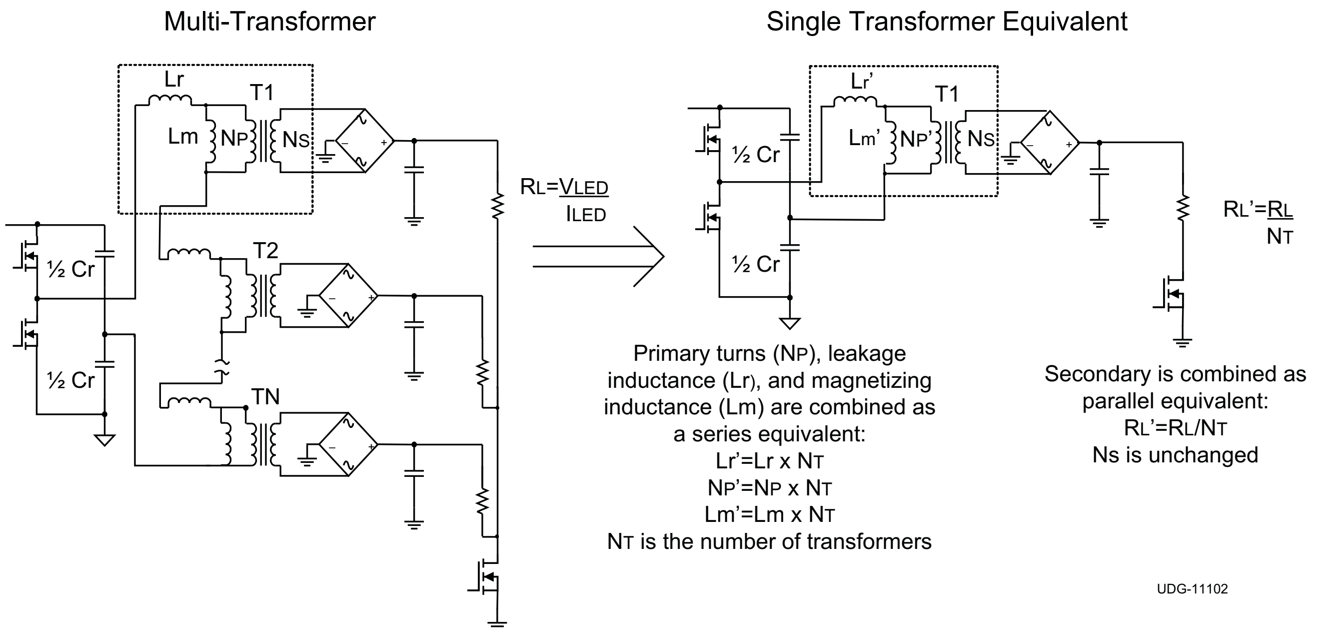


Figure 25. Multiple Transformers Combined With Reflected Loads

9.2.2.2 CS (Output Current Sense)

The CS pin is connected to the output current-sense resistor and is the feedback signal for the current amplifier. The regulation range is limited by the 0.5-V to 2.8-V internal current amplifier reference clamp. The LED current sense resistor value is determined by Equation 5.

$$R_{CS} = \frac{V_{CREF}}{I_{LEDTotal}}$$

where

- V_{CREF} is voltage on CREF pin determined by divider from VREF $I_{LEDTotal}$.
- $I_{LEDTOTAL}$ is the total LED string current during the DIM on time. (5)

9.2.2.3 ICOMP (Current Amplifier Compensation)

Connect a capacitor or series resistor capacitor combination to ground to compensate the 510-µS GM current amplifier control loop. The current amplifier is designed to maintain the steady-state operating voltage point of the current amplifier during dimming operation. This is accomplished by switching on and off the GM current amplifier to the ICOMP pin with the same control signal that controls the LEDSW output. The GM amplifier is disconnected from the ICOMP pin during the DIM OFF-time, and connected during the DIM ON-time. This feature is compromised if there is a leakage path on the ICOMP pin, such as resistance to ground. The re-connection of the ICOMP pin to the current amplifier output is delayed by about 2.4 µs to allow time for the external LED switch to be turned on prior to allowing the ICOMP pin voltage to be driven.

The optimum ICOMP capacitor value is determined based on desired LED current and primary current response during dimming. Because the LLC converter has a highly nonlinear transfer function, a gain phase analyzer is recommended to optimize the component values on ICOMP. The recommended bandwidth target is from 800 Hz to 5 kHz. The trade-off of too low bandwidth is increased line frequency ripple on the LED string current. The trade-off of high bandwidth is voltage variation on ICOMP during the DSR rise time which can result in primary current peaking during the start of the DIM period, this may result in audible noise if excessive. Either an integrator (capacitor to ground) or type II compensation (capacitor in parallel with resistor and series capacitor) is recommended.

9.2.2.4 SS (Soft Start)

Connect a capacitor to ground to program the desired soft-start time. When VCC exceeds the V_{CCON} threshold and BLON is high, a 2.5-µA current source charges the soft-start capacitor after a 10-ms delay. The voltage on SS dominates the VCO control voltage when lower than V_{ICOMP} or V_{DSR}. The device is in a soft-start condition until V_{SS} reaches the 4.2-V soft start over threshold. During the soft-start cycle DIM is disabled and the UV protection is disabled. The soft-start cycle is initiated by UVLO, BLON, OV fault clear, or UV fault clear after the soft-start cycle.

$$C_{SS} = \frac{2.5\ \mu A \times T_{SS}}{V_{ICOMP\_REG} - 0.9\ V}$$

where

- T_{SS} is the target SS time.
- V_{ICOMP_REG} is the ICOMP voltage at the regulation point, which can be derived based on LLC switching frequency. (6)

9.2.2.5 FMAX (Maximum VCO Frequency)

Terminate FMAX to ground with a resistor to program the frequency delta from desired maximum to minimum operating frequency range. The recommended resistor value range is 4.22 kΩ to 53.6 kΩ. V_{ICOMP} which is the VCO control signal determines the voltage on FMAX; the programming resistor determines the voltage to current conversion ratio that programs the oscillator frequency at a given V_{ICOMP} voltage level. The device is designed to accommodate a maximum frequency of 350 kHz and a minimum frequency delta of 25 kHz. To provide controlled rise and fall time of the primary current during dimming, a maximum frequency of 2 to 3 times the nominal switching frequency is recommended as an initial value. The resistor value can be determined by Equation 7.

$$R_{MAX} = \frac{0.0664}{49.2\,pF \times F_{SW}(Delta)}$$

where

- $F_{SW}(Delta) = F_{SW(max)} - F_{SW(min)}$ (7)

9.2.2.6 FMIN (Minimum VCO Frequency)

Terminate FMIN to ground with a resistor to program the desired minimum operating frequency. The recommended resistor range is 9.53 kΩ to 102 kΩ. The device is designed to accommodate a minimum frequency of 30 KHz. The resistor value can be determined by Equation 8.

$$R_{MIN} = \frac{0.15}{49.2\,pF \times F_{SW(min)}} \quad (8)$$

Use Equation 9 to determine F_{SW} for given V_{ICOMP}, R_{FMAX}, and R_{FMIN} values.

$$F_{SW} = \frac{\dfrac{0.15}{R_{MIN}} + \dfrac{(4\,V - V_{ICOMP})}{R_{MAX} \times 45.2\,V}}{49.2\,pF}$$

where from Equation 7 to Equation 9

- F_{SW} is in Hz, R is in Ω
- V_{ICOMP} is in V (9)

9.2.2.7 GD1 and GD2 (Gate Drive 1 and 2)

Connect the primary of the gate-drive transformer to GD1 and GD2 through a small series resistance. The high-side driver resistance is 12 Ω and low-side driver resistance is 4 Ω typical. The drivers are limited to 25-mA RMS maximum current, so there is a magnetizing current limitation of the gate-drive transformer shown in the Equation 10. If the magnetizing current exceeds 25 mA with the specified gate-drive transformer and nominal operating frequency, a simple NPN-PNP buffer on GD1 and GD2 may be required. The minimum gate drive transformer inductance can be determined from Equation 10.

$$L_{GD} = \frac{V_{CC}}{2 \times F_{SW} \times 87\,mA}$$

where

- L_{GD} is the gate drive transformer L_{PRI}
- F_{SW} is the nominal switching frequency
- V_{CC} is the V_{CC} supply voltage (10)

9.2.2.8 LEDSW (LED Switch Drive)

The LEDSW is the output to control the LED switch MOSFET in series with the LED string returns. The LEDSW is controlled by the DIM input during normal operation to provide LED string current pulse widths that corresponds to the DIM signal. During soft start, the LEDSW signal is high regardless of the DIM signal to allow the output capacitors to charge. The LEDSW is low during an OV, UV or CL fault to provide additional protection to the LED's. This output is 0 V to VCC but has limited drive current ability, a simple NPN or PNP buffer is required to drive the LED switch MOSFET. The LEDSW high resistance is 4 kΩ and low side is 2 kΩ, so avoid any DC load on this pin.

The turnon and turnoff delay of the LED switch MOSFET relative to DIM rising and falling edge must be well matched to achieve excellent LED current linearity especially at low DIM duty-cycles. As an example, consider a 1% dimming duty-cycle at dimming PWM frequency of 300 Hz where a delay mismatch of 667 ns represents a 2% linearity error. A gate-drive resistor and parallel resistor diode combination to drive the LED switch MOSFET can be used to match edge delays. Refer to Figure 26 for a recommended LED switch MOSFET drive circuit.

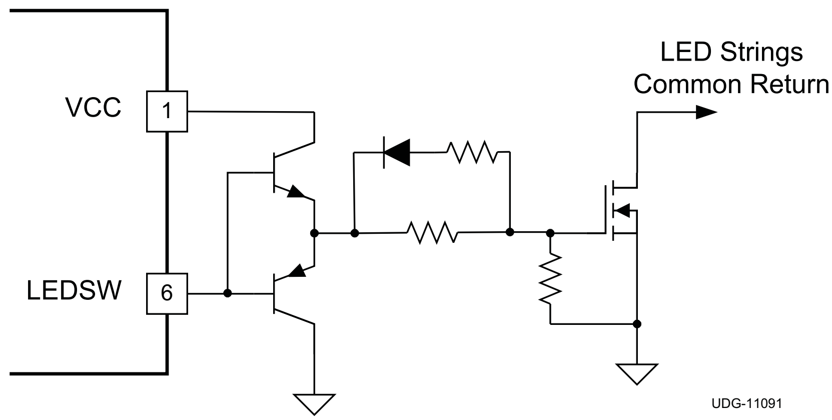


Figure 26. Recommended LED Switch MOSFET Drive Circuit

9.2.2.9 DSR (Dimming Slew Rate)

The DSR pin is used to control the rise and fall time of the VCO control voltage. The DSR capacitor value can be determined by Equation 11. The effective rise time of the LLC primary current is when VDSR is between the 0.9-V gate-drive enable voltage and the VICOMP operating point.

$$C_{DSR} = \frac{44\,\mu A \times T_{SLEW}}{V_{ICOMP\_REG} - 0.9\,V}$$

where

- T_{SLEW} is the desired LLC current rise and fall time
- V_{ICOMP_REG} is the ICOMP voltage regulation point (11)

Because the DSR voltage starts at 0 V and the LLC gate-drive enable is typically 0.9 V, there is a delay from the DIM rising edge and LEDSW rising edge until the LLC gate drivers are enabled. An easy solution to eliminate a majority of the delay is to use a resistor in series with C_{DSR}. Because DSR is clamped at a Vbe above V_{ICOMP}, the recommended resistance is 15 kΩ to 17 kΩ to provide a 640-mV to 720-mV initial voltage delta.

9.2.2.10 DTY (Dimming Duty-Cycle Average)

The DTY pin generates a voltage inversely proportional to the DIM duty-cycle with a 100-mV offset. The voltage range is 100 mV to 2.6 V corresponding to 100% dimming and 0% dimming. This voltage is compared to the DADJ rising ramp to determine the dimming duty-cycle compensation delay time.

The capacitor value is selected to provide low ripple voltage at the DIM frequency. A good guideline is to target 100 V or less peak-to-peak ripple voltage. There is a trade-off of DTY capacitor value and response to DIM duty-cycle transients. For faster response time to significant changes in DIM duty-cycle select a lower value capacitance. Equation 12 can be used to select a DTY capacitor based on maximum ripple voltage and DIM frequency.

$$C_{DTY} = \frac{15.65\,\mu A}{V_{DTY(pp)} \times F_{DIM}}$$

where

- F_{DIM} is the dimming frequency
- $V_{DTY(pp)}$ is the maximum peak to peak ripple voltage. (12)

Equation 13 can be used to determine the average of V_{DTY} at any given DIM duty-cycle.

$$V_{DTY} = \left[(1 - D_{DIM}) \times 2.5\,V\right] + 0.1V$$

where D_{DIM} is the DIM duty-cycle. (13)

9.2.2.11 DADJ (Dimming Duty-Cycle Adjust)

The DADJ pin is a 20-µA current source enabled at the DIM falling edge. The capacitor connected to this pin determines the slope of V_{DADJ}. LLC-OFF is the internal signal that controls the turnon and turnoff of the LLC power stage. The rising edge of LLC-OFF corresponds to a falling edge at the DIM input. The falling edge of the LLC-OFF signal is delayed until the rising edge of the DADJ voltage crosses the voltage on DTY. See *Dimming Operation* discussion for more details.

An initial value DADJ capacitor can be determined by Equation 14. The dimming performance at lowest DIM on time must be evaluated as described in the following paragraph.

$$C_{DADJ} = \frac{20\,\mu A \times \left(\sqrt{\frac{DIM_{DMIN} \times T_{RISE}}{F_{DIM}}} - \frac{DIM_{DMIN}}{F_{DIM}} \right)}{\left[\left(1 - DIM_{DMIN}\right) \times 2.5\,V \right] + 0.1\,V}$$

where

- DIM_{DMIN} is the minimum dimming duty cycle
- F_{DIM} is the dimming frequency
- T_{RISE} is the effective DSR rise time (14)

To ensure consistent LED current regulation during DIM duty-cycle transients, it is important to confirm that ICOMP achieves the steady-state operating voltage at the lowest DIM duty-cycle. Because DSR is clamped a V_{BE} (approximately 0.7 V) above ICOMP, this signal can be inspected to confirm a steady-state operating point is achieved after the programmed DSR rise time. Confirm that the DSR signal achieves a relatively flat voltage during the lowest DIM duty-cycle condition. Figure 27 and Figure 28 below are scope plots of 1% DIM duty-cycle where DSR reaches the steady-state operating point, and 0.5% DIM where DSR is still rising and ICOMP is open loop. If DSR is still rising during the lowest DIM duty cycle, increase the DADJ capacitor value until DSR achieves a relatively flat response as shown in Figure 27, the 1% DIM duty-cycle scope plot below.

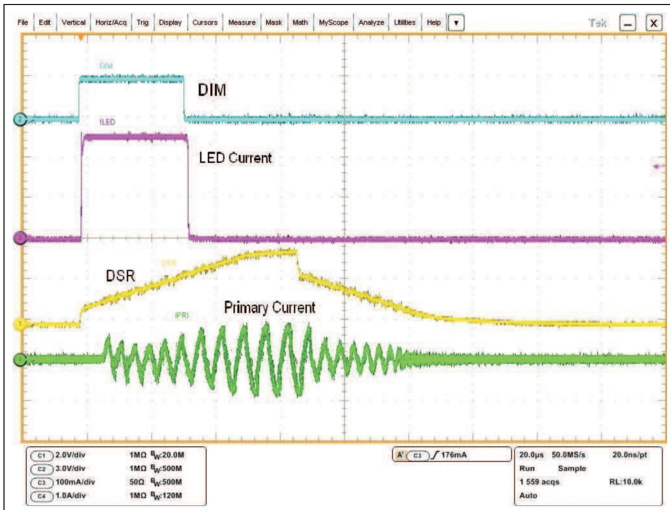


Figure 27. 1% DIM duty-cycle

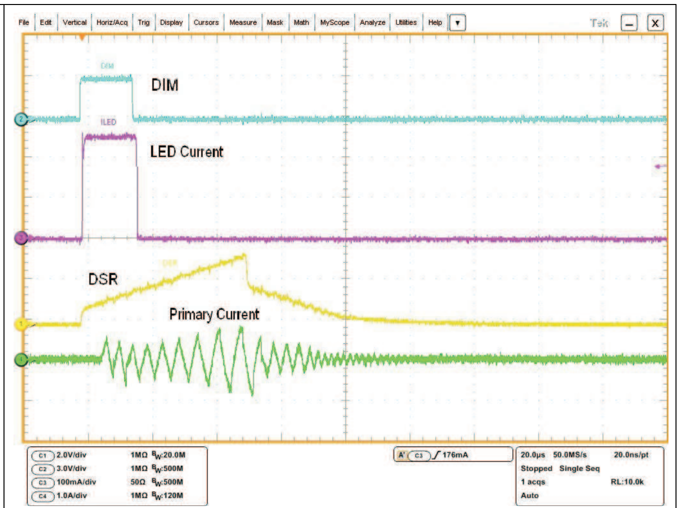


Figure 28. 0.5% DIM duty-cycle

9.2.2.12 OV (Output Overvoltage)

The OV pin is connected to an output-voltage sense resistor divider with oring diodes to all of the LED outputs. The OV threshold is 2.6 V with 240-mV hysteresis. During an OV fault the GD1 and GD2 gate drivers are disabled and the LEDSW goes low (off). When the OV fault clears, the soft-start cycle is initiated.

A configuration is shown in Figure 29 below that allows for summing of multiple LED string outputs into common UV and OV dividers. Consider the total resistance of the divider networks because the divider bias current is provided by the highest voltage LED string. Equation 15 and Equation 16 can be used to determine total divider resistance and each component values.

$$R_{OV1} = \frac{2 \times V_{OUT} \times 1.5}{I_{OUT} \times D_{MIN} \times I_{MATCH}}$$

where

- V_{OUT} is LED string voltage
- I_{OUT} is LED DC output current
- D_{MIN} is minimum dimming duty-cycle
- I_{MATCH} is LED current matching target
- OV and UV dividers are approximately equal resistance (15)

$$R_{OV2} = \frac{R_{OV1} \times 2.6\,V}{V_{OVLO} - 2.6\,V - V_D}$$

where

- V_{OVLO} is the OVP threshold
- V_D is the summing diode voltage drop (16)

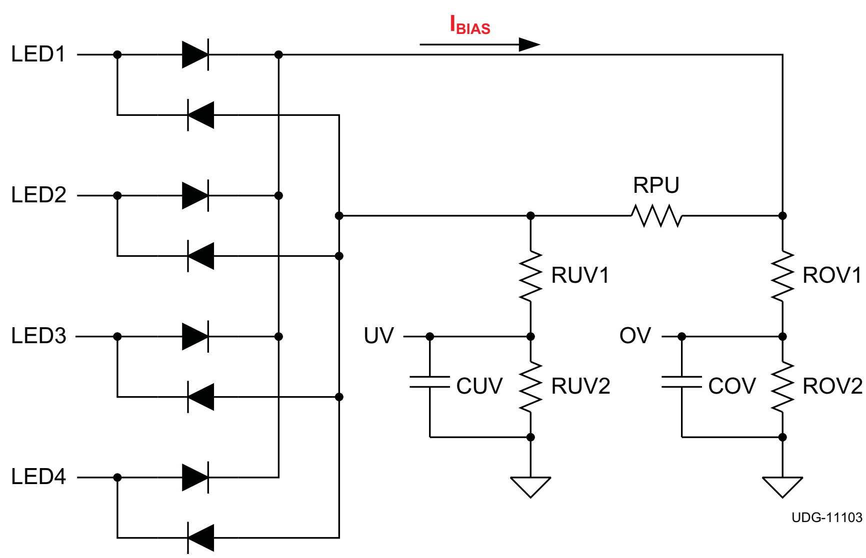


Figure 29. Application of Overvoltage and Undervoltage

9.2.2.13 UV (Output Undervoltage)

UV is connected to an output-voltage sample of the converter. The UV threshold is 2.4 V with 240-mV hysteresis. UV below 2.4 V is considered an undervoltage fault which disables the GD1 and GD2 gate drivers, LEDSW output goes low, the 10-ms soft-start clamp and soft-start cycle are initiated. The UV comparator is disabled until SS voltage is 4.2 V to allow the output capacitors to charge to the normal operating voltage during start-up of the converter.

See the OV and UV divider diagram above for a typical configuration that allows for summing of multiple LED string outputs into common UV and OV dividers. Consider the value of RPU to avoid a current path from the highest voltage LED string to the lowest voltage LED string. Equation 17, Equation 18, and Equation 19 assume a 2× V_{OUT} delta as the maximum UVLO voltage.

$$R_{PU} = \frac{R_{OV1}}{5}$$

where

- LED voltage total tolerance is ±5%

- OV and UV dividers are approximately equal resistance (17)

$$R_{UV1} = R_{OV1} - R_{PU} \quad (18)$$

$$R_{UV2} = \frac{(R_{UV1} + R_{PU}) \times 2.4\,V}{V_{UVLO} - 2.4\,V - V_D}$$

where

- V_{UVLO} is the UVP threshold
- V_D is the summing diode voltage drop (19)

9.2.2.14 CL (Current Limit)

The CL pin is typically connected to the rectified and filtered output of a primary current sense transformer. There are two levels of current limit protection: restart and latching. When CL exceeds 0.95 V the gate drivers are disabled and LEDSW goes low, when the CL voltage reduces to 475 mV the soft-start cycle is initiated. If CL exceeds a 1.9-V threshold, the gate drivers are disabled and LEDSW goes low, this condition is latched until VCC is recycled below the UVLO threshold.

9.2.3 Application Curves

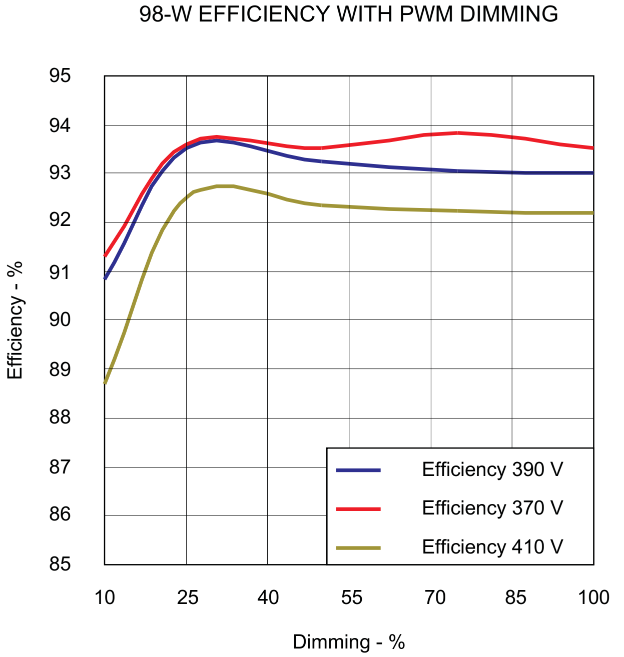


Figure 30. Efficiency 10% to 100% PWM Dimming

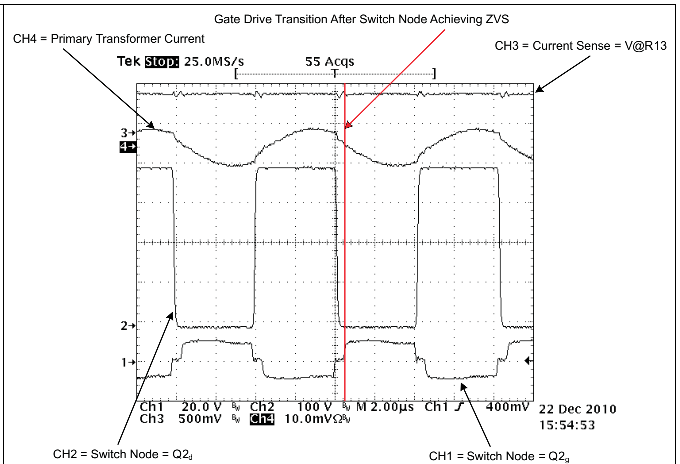


Figure 31. V_{IN} = 390 V, Outputs Loaded With 32, Cree XLamp CR-E , LEDs

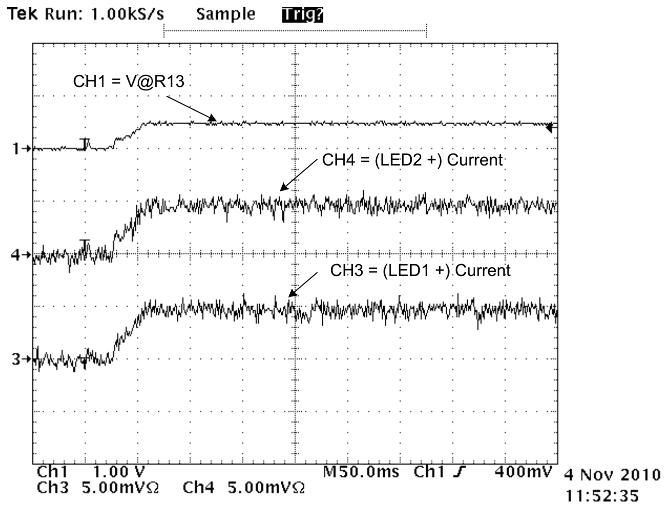


Figure 32. Current LED1 (CH3) and LED2 (CH4)

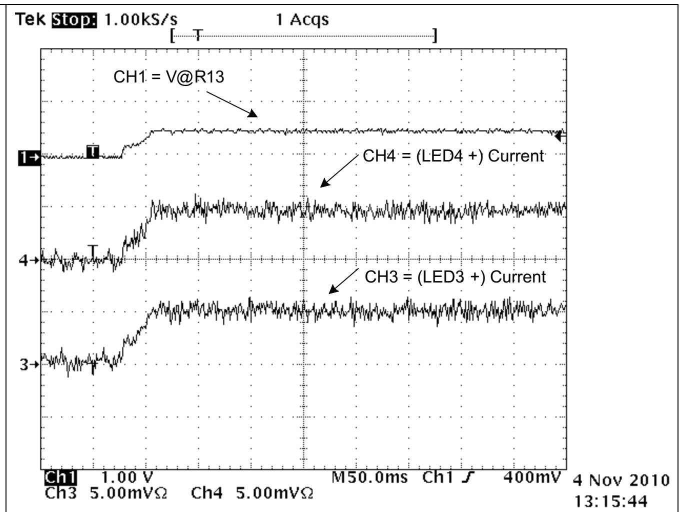


Figure 33. Current LED3 (CH3) and LED4 (CH4)

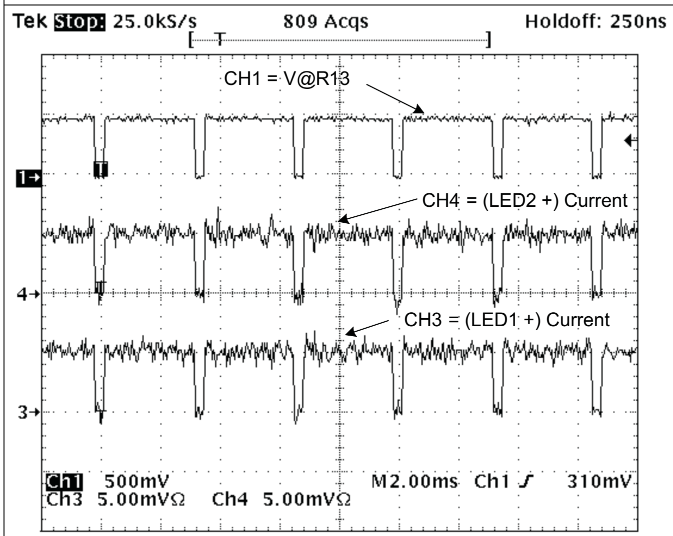


Figure 34. Current LED1 (CH3) and LED2 (CH4)

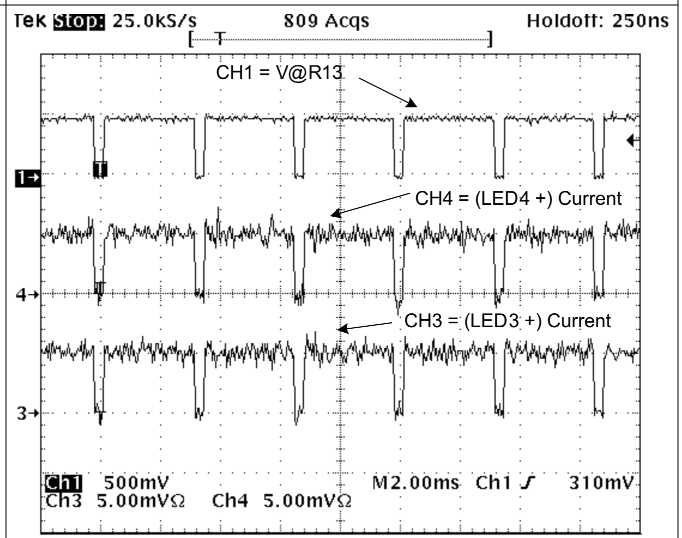


Figure 35. Current LED3 (CH3) and LED4 (CH4)

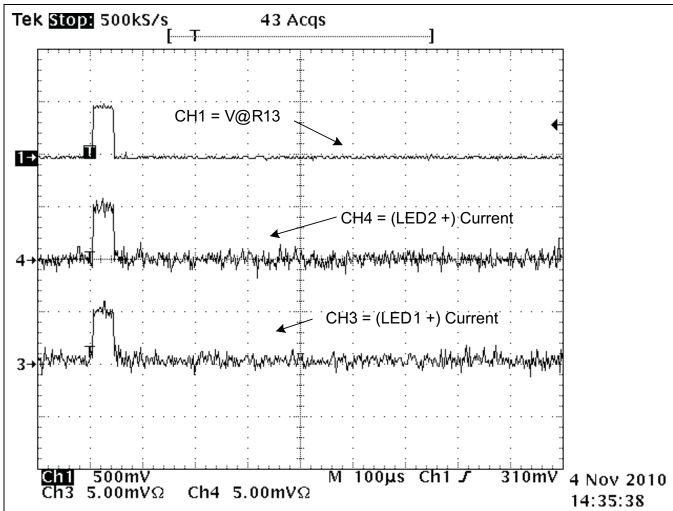


Figure 36. Current LED1 (CH3) and LED2 (CH4)

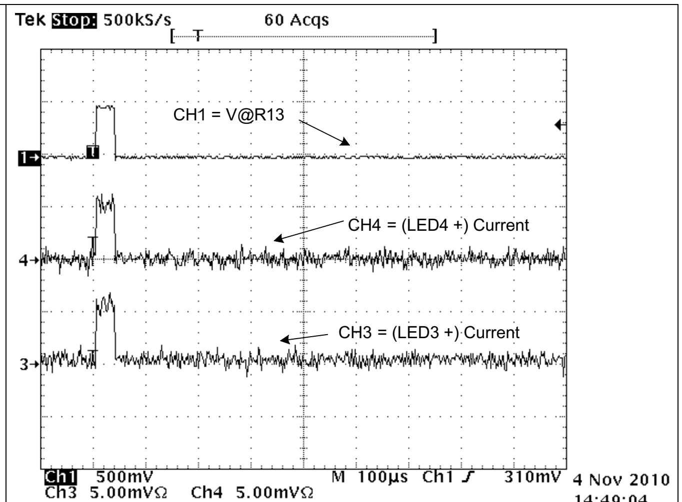


Figure 37. Current LED3 (CH3) and LED4 (CH4)

10 Power Supply Recommendations

The UCC25710 is designed to operate from an external bias supply connected to the VCC input. It has an operating voltage range between 11 V and 18 V with an absolute maximum input voltage rating of 18 V.

In most applications, the high voltage input range of the LLC controller is normally set at about 370 V to 410 V with 390-V nominal. This narrow range of DC input voltage is a constraint of the LLC topology. Setting the maximum and minimum switching frequencies limits the regulation range to these input voltages.

11 Layout

11.1 Layout Guidelines

As with all PWM controllers, the effectiveness of the filter capacitors on the signal pins depends upon the integrity of the ground signal. Separating the high di/dt induced noise on the power ground from the low current quiet signal ground is required for adequate noise immunity. As shown Figure 38, the bypass capacitors on VCC and VREF have one end located in close proximity to their associated pins and the other ends are returned directly to the GND pin or to the portion of the ground plane associated with the low level GND signal and not to the high current power return. Low-ESR type ceramic capacitors are recommended as bypass capacitors.

The gate-drive output signals (GD1 and GD2) can cause interference on the low-level inputs (CL and CS) and for this reason must be routed as far as possible away from them and have short direct paths to the gate-drive transformer. In general any slow-changing analog signals must be routed away from high-speed digital signals.

Timing resistors FMIN and FMAX must be placed as close as possible to the pins on the UCC25710.

11.2 Layout Example

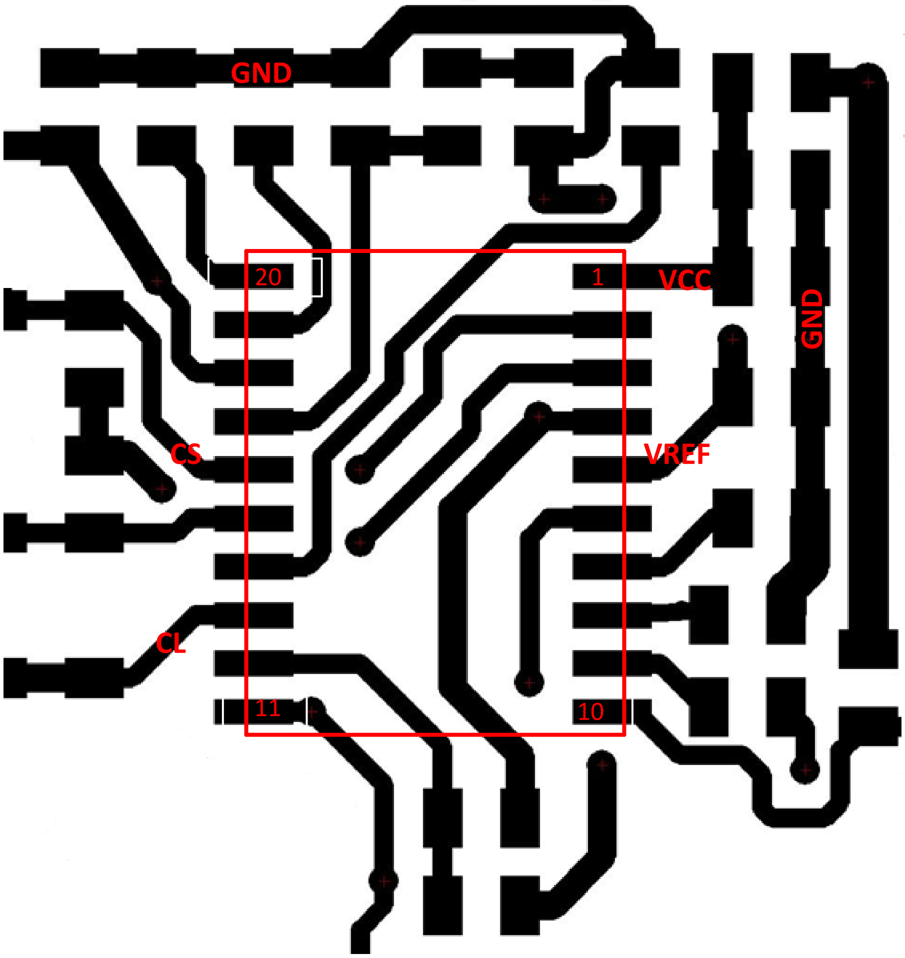


Figure 38. Layout Example for UCC25710

12 器件和文档支持

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要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。请单击右上角的*通知我* 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

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12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC25710DW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC25710
UCC25710DW.A	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC25710
UCC25710DWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC25710
UCC25710DWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC25710

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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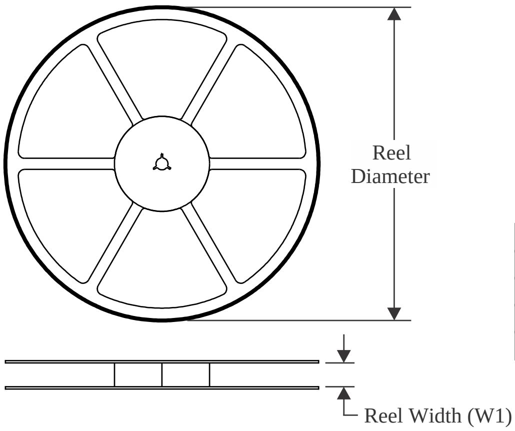
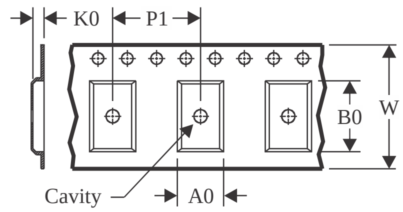
TAPE AND REEL INFORMATION

REEL DIMENSIONS

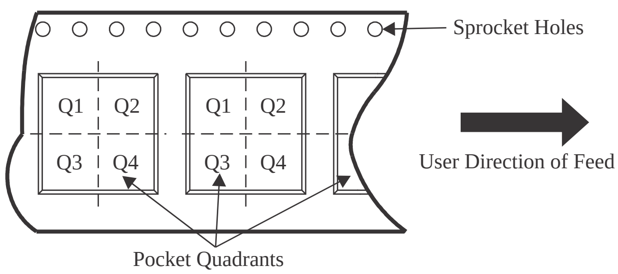


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

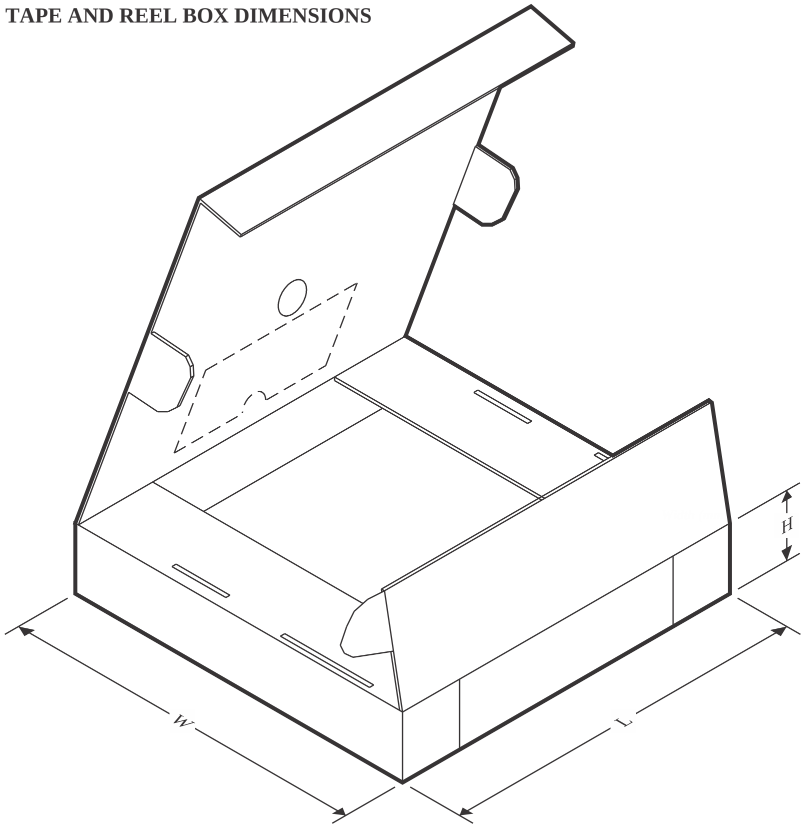
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC25710DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

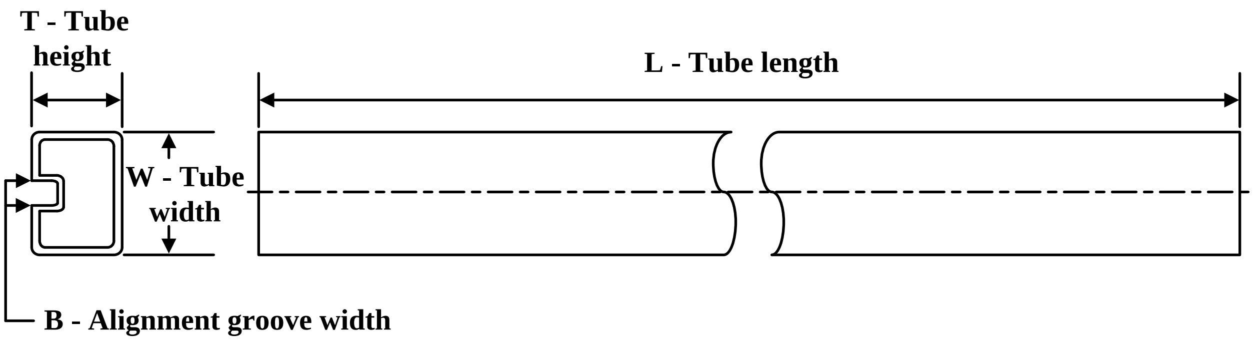
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

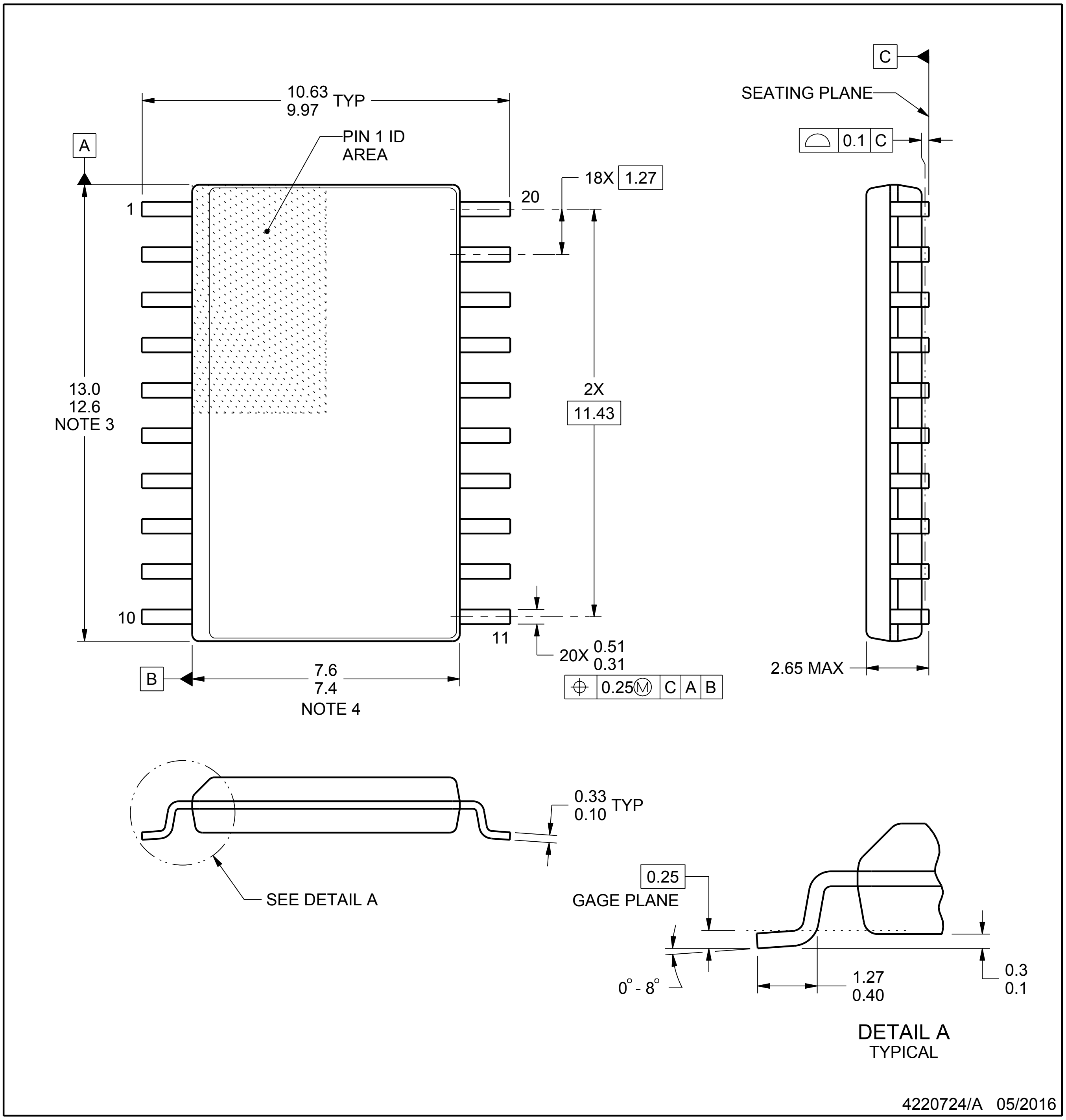
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC25710DWR	SOIC	DW	20	2000	350.0	350.0	43.0

TUBE



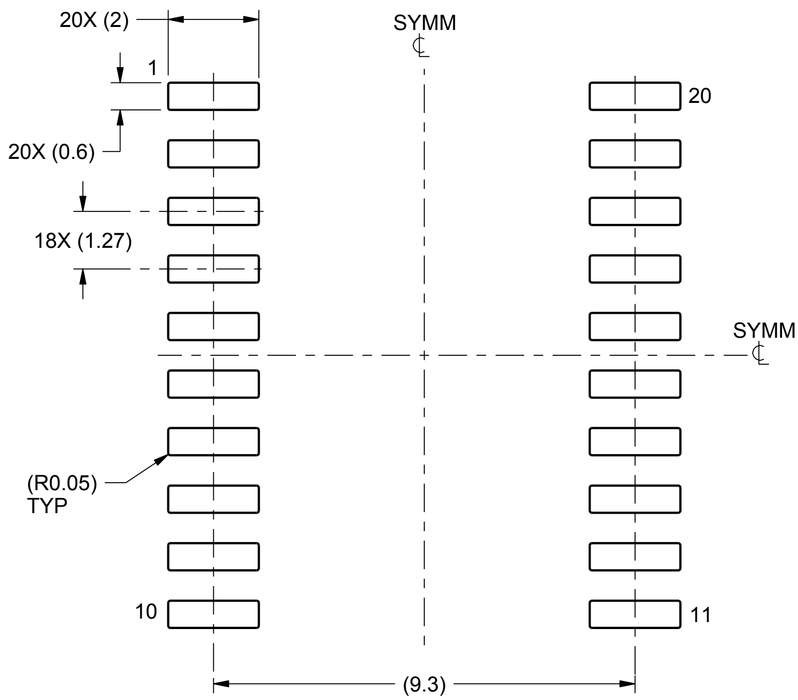
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC25710DW	DW	SOIC	20	25	506.98	12.7	4826	6.6
UCC25710DW.A	DW	SOIC	20	25	506.98	12.7	4826	6.6

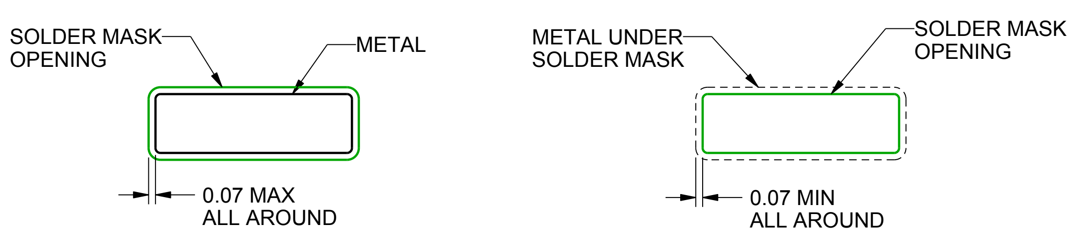


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



NON SOLDER MASK DEFINED

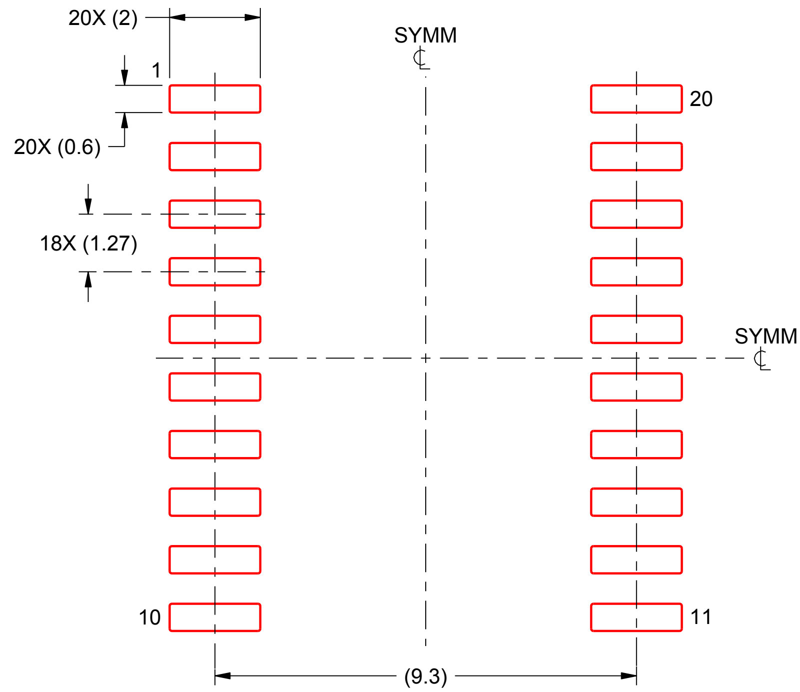
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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