# 具有单输入的 UCC205204A/6A、5.7 $kV_{RMS}$ 隔离式双通道栅极驱动器

## 1 特性

- 单输入、双输出
- 工作温度范围：–40 至 125° C
- 开关参数：
  - 19ns 典型传播延迟
  - 10ns 最小脉冲宽度
  - 5ns 最大延迟匹配
  - 6ns 最大脉宽失真
- 共模瞬态抗扰度 (CMTI) 大于 100V/ns
- 浪涌抗扰度高达 12.8kV
- 隔离栅寿命大于 40 年
- 4A 峰值拉电流、6A 峰值灌电流输出
- TTL 和 CMOS 兼容输入
- 3V 至 18V 输入 VCCI 范围，可与数字控制器和模拟控制器连接
- 高达 25V 的 VDD 输出驱动电源
- 可编程死区时间
- 抑制短于 5ns 的输入脉冲和噪声瞬态
- 快速禁用电源定序
- 业界通用的宽体 SOIC-16 (DW) 封装
- 安全相关及监管批准：
  - 符合 DIN V VDE V 0884-11:2017-01 标准的 8000$V_{PK}$ 隔离
  - 符合 UL 1577 标准且长达 1 分钟的 5700$V_{RMS}$ 隔离
  - 获得 CSA 认证，符合 IEC 60950-1、IEC 62368-1、IEC 61010-1 和 IEC 60601-1 终端设备标准
  - 获得 CQC 认证，符合 GB4943.1-2011 标准

## 2 应用

- 隔离式交流/直流电源转换器
- 服务器、电信、IT 和工业基础设施
- 电机驱动和直流/交流光伏逆变器
- LED 照明
- 感应加热
- 不间断电源 (UPS)
- HEV 和 BEV 电池充电器

## 3 说明

UCC20520 是一款隔离式单输入、双通道栅极驱动器，其峰值拉电流为 4A，峰值灌电流为 6A。该器件设计用于驱动高达 5MHz 的功率 MOSFET、IGBT 和 SiC MOSFET，具有一流的传播延迟和脉宽失真度。

输入侧通过 5.7$kV_{RMS}$ 增强型隔离层与两个输出驱动器隔离，具有最少 100V/ns 的共模瞬态抗扰度 (CMTI)。两个次级侧驱动器之间的内部功能隔离，支持的工作电压高达 1500 $V_{DC}$。

该驱动器可用于具有可编程死区时间 (DT) 的半桥驱动器。禁用引脚在设为高电平时可同时关断两个输出，并在开路或接地时允许正常运行。作为一种故障安全措施，初级侧逻辑故障强制两个输出均为低电平。

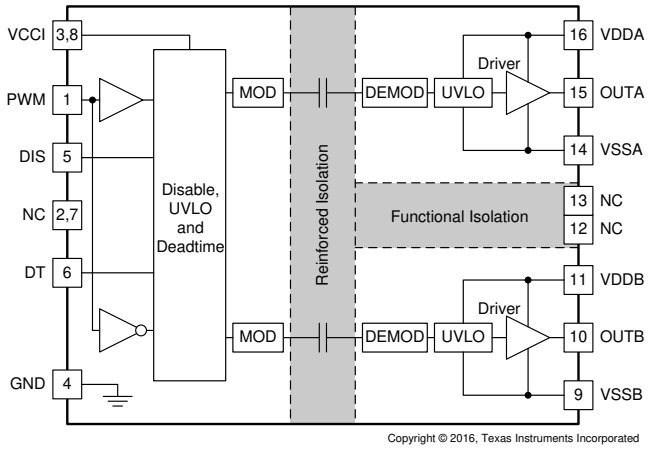
此器件接受高达 25V 的 VDD 电源电压。3V 到 18V 的宽输入电压 VCCI 范围使得该驱动器适用于与模拟和数字控制器连接。所有电源电压引脚都具有欠压锁定 (UVLO) 保护功能。

凭借所有这些高级特性，UCC20520 能够在各种各样的电源应用中实现高效率、高电源密度和稳健性。

**器件信息**

| 零件编号 | 封装(1) | 封装尺寸（标称值） |
|---|---|---|
| UCC20520 | DW SOIC (16) | 10.30mm × 7.50mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。




**功能框图**

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

# Table of Contents

**1 特性** ..... 1
**2 应用** ..... 1
**3 说明** ..... 1
**4 Revision History** ..... 2
**5 Pin Configuration and Functions** ..... 3
**6 Specifications** ..... 4
6.1 Absolute Maximum Ratings ..... 4
6.2 ESD Ratings ..... 4
6.3 Recommended Operating Conditions ..... 4
6.4 Thermal Information ..... 5
6.5 Power Ratings ..... 5
6.6 Insulation Specifications ..... 6
6.7 Safety-Related Certifications ..... 7
6.8 Safety-Limiting Values ..... 7
6.9 Electrical Characteristics ..... 8
6.10 Switching Characteristics ..... 9
6.11 Insulation Characteristics Curves ..... 10
6.12 Typical Characteristics ..... 11
**7 Parameter Measurement Information** ..... 15
7.1 Propagation Delay and Pulse Width Distortion ..... 15
7.2 Rising and Falling Time ..... 15
7.3 PWM Input and Disable Response Time ..... 15
7.4 Programable Dead Time ..... 16
7.5 CMTI Testing ..... 16
**8 Detailed Description** ..... 17
8.1 Overview ..... 17
8.2 Functional Block Diagram ..... 17
8.3 Feature Description ..... 18
8.4 Device Functional Modes ..... 21
**9 Application and Implementation** ..... 23
9.1 Application Information ..... 23
9.2 Typical Application ..... 23
**10 Layout** ..... 35
10.1 Layout Guidelines ..... 35
10.2 Layout Example ..... 36
**11 Device and Documentation Support** ..... 38
11.1 Documentation Support ..... 38
11.2 接收文档更新通知 ..... 38
11.3 支持资源 ..... 38
11.4 Trademarks ..... 38
11.5 Electrostatic Discharge Caution ..... 38
11.6 术语表 ..... 38

## 4 Revision History

| Changes from Revision * (November 2016) to Revision A (January 2022) | Page |
|---|---|
| • 更新了整个文档中的表格、图和交叉参考的编号格式 | 1 |
| • 将*特性* 中的最大脉宽失真值从“5ns”更改为“6ns” | 1 |
| • Changed maximum pulse width distortion specification in 节 6.10 from "5 ns" to "6 ns" | 9 |
| • Updated bench test waveform colors for better readability only. No data or measurment changes. | 33 |


Copyright © 2022 Texas Instruments Incorporated

# 5 Pin Configuration and Functions

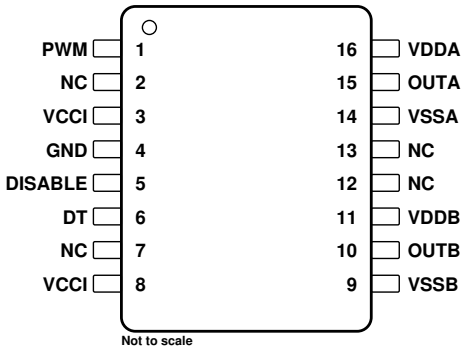



**图 5-1. DW Package, 16-Pin SOIC (Top View)**

**表 5-1. Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| DISABLE | 5 | I | Disables both driver outputs if asserted high, enables if set low or left open. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity. |
| DT | 6 | I | Programmable dead time function.<br>Tying DT to VCCI disables the DT function with dead time ≅ 0 ns. Leaving DT open sets the dead time to <15 ns. Placing a 500-Ω to 500-kΩ resistor ($R_{DT}$) between DT and GND adjusts dead time according to: DT (in ns) = 10 × $R_{DT}$ (in kΩ). It is recommended to parallel a ceramic capacitor, ⩾2.2-nF, with $R_{DT}$ to achieve better noise immunity. |
| GND | 4 | P | Primary-side ground reference. All signals in the primary side are referenced to this ground. |
| NC | 2 | – | No connection. |
| NC | 7 | – | No connection. |
| NC | 12 | – | No connection. |
| NC | 13 | – | No connection. |
| OUTA | 15 | O | Output of driver A. Connect to the gate of the A channel FET or IGBT. Output A is in phase with PWM input with a propagation delay |
| OUTB | 10 | O | Output of driver B. Connect to the gate of the B channel FET or IGBT. Output B is always complementary to output A with a programmed dead time. |
| PWM | 1 | I | PWM input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. |
| VCCI | 3 | P | Primary-side supply voltage. Locally decoupled to GND using a low ESR/ESL capacitor located as close to the device as possible. |
| VCCI | 8 | P | Primary-side supply voltage. This pin is internally shorted to pin 3. |
| VDDA | 16 | P | Secondary-side power for driver A. Locally decoupled to VSSA using a low ESR/ESL capacitor located as close to the device as possible. |
| VDDB | 11 | P | Secondary-side power for driver B. Locally decoupled to VSSB using a low ESR/ESL capacitor located as close to the device as possible. |
| VSSA | 14 | P | Ground for secondary-side driver A. Ground reference for secondary side A channel. |
| VSSB | 9 | P | Ground for secondary-side driver B. Ground reference for secondary side B channel. |

1. I = input, O = output, I/O = input or output, FB = feedback, G = ground, P = power

Copyright © 2022 Texas Instruments Incorporated

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| VCCI to GND | –0.3 | 20 | V |
| VDDA-VSSA, VDDB-VSSB | –0.3 | 30 | V |
| OUTA to VSSA, OUTB to VSSB | –0.3 | $V_{VDDA}$+0.3, $V_{VDDB}$+0.3 | V |
| OUTA to VSSA, OUTB to VSSB, Transient for 200 ns | –2 | $V_{VDDA}$+0.3, $V_{VDDB}$+0.3 | V |
| PWM, DIS, DT to GND | –0.3 | $V_{VCCI}$+0.3 | V |
| PWM Transient for 50 ns | –5 | $V_{VCCI}$+0.3 | V |
| VSSA-VSSB, VSSB-VSSA | | 1500 | V |
| Junction temperature, $T_J$ (2) | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) To maintain the recommended operating conditions for $T_J$, see the 节 6.4.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±4000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| VCCI | VCCI Input supply voltage | 3 | 18 | V |
| VDDA, VDDB | Driver output bias supply | 9.2 | 25 | V |
| $T_A$ | Ambient Temperature | –40 | 125 | °C |
| $T_J$ | Junction Temperature | –40 | 130 | °C |


Copyright © 2022 Texas Instruments Incorporated

## 6.4 Thermal Information

| THERMAL METRIC(1) | | UCC20520 | UNIT |
|---|---|---|---|
| | | DW-16 (SOIC) | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 78.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 11.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 48.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 12.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 48.4 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Power Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $P_D$ | Power dissipation by UCC20520DW | VCCI = 18 V, VDDA/B = 12 V, PWM = 3.3 V, 3 MHz 50% duty cycle square wave 1-nF load | 1.05 | W |
| $P_{DI}$ | Power dissipation by primary side of UCC20520DW | | 0.05 | W |
| $P_{DA}$, $P_{DB}$ | Power dissipation by secondary driver side of UCC20520DW | | 0.5 | W |

Copyright © 2022 Texas Instruments Incorporated

## 6.6 Insulation Specifications

| PARAMETER | | TEST CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| CLR | External clearance(1) | Shortest terminal to terminal distance through air | > 8 | mm |
| CPG | External creepage(1) | Shortest terminal to terminal distance across the package surface | > 8 | mm |
| DTI | Distance through insulation | Distance through internal isolation (internal clearance) | >21 | µm |
| CTI | Comparative tracking index | DIN EN 60112 (VDE 0303-11); IEC 60112 | > 600 | V |
| | Material group | According to IEC 60664-1 | I | |
| | Overvoltage category per IEC 60664-1 | Rated mains voltage ⩽ 600 $V_{RMS}$ | I-IV | |
| | | Rated mains voltage ⩽ 1000 $V_{RMS}$ | I-III | |
| **DIN V VDE 0884-10 (VDE V 0884-10): 2006-2012(2)** | | | | |
| $V_{IORM}$ | Maximum repetitive peak isolation voltage | AC voltage (bipolar) | 2121 | $V_{PK}$ |
| $V_{IOWM}$ | Maximum isolation working voltage | Time dependent dielectric breakdown (TDDB) test, (See 图 6-1) | 1500 | $V_{RMS}$ |
| | | | 2121 | $V_{DC}$ |
| $V_{IOTM}$ | Maximum transient isolation voltage | $V_{TEST}$ = $V_{IOTM}$<br>t = 60 sec (qualification)<br>t = 1 sec (100% production) | 8000 | $V_{PK}$ |
| $V_{IOSM}$ | Maximum surge isolation voltage(3) | Test method per IEC 60065, 1.2/50 µs waveform, $V_{TEST}$ = 1.6 × $V_{IOSM}$ = 12800 $V_{PK}$ (qualification) | 8000 | $V_{PK}$ |
| $q_{pd}$ | Apparent charge(4) | Method a, After Input/Output safety test subgroup 2/3. $V_{ini}$ = $V_{IOTM}$, $t_{ini}$ = 60s;<br>$V_{pd(m)}$ = 1.2 X $V_{IORM}$ = 2545 $V_{PK}$, $t_m$ = 10s | <5 | pC |
| | | Method a, After environmental tests subgroup 1. $V_{ini}$ = $V_{IOTM}$, $t_{ini}$ = 60s;<br>$V_{pd(m)}$ = 1.6 X $V_{IORM}$ = 3394 $V_{PK}$, $t_m$ = 10s | <5 | |
| | | Method b1; At routine test (100% production) and preconditioning (type test)<br>$V_{ini}$ = $V_{IOTM}$; $t_{ini}$ = 1s;<br>$V_{pd(m)}$ = 1.875 * $V_{IORM}$ = 3977 $V_{PK}$ , $t_m$ = 1s | <5 | |
| $C_{IO}$ | Barrier capacitance, input to output(5) | $V_{IO}$ = 0.4 sin (2 π ft), f =1 MHz | 1.2 | pF |
| $R_{IO}$ | Isolation resistance, input to output | $V_{IO}$ = 500 V at $T_A$ = 25°C | > $10^{12}$ | Ω |
| | | $V_{IO}$ = 500 V at 100°C ⩽ $T_A$ ⩽ 125°C | > $10^{11}$ | |
| | | $V_{IO}$ = 500 V at $T_S$ =150°C | > $10^9$ | |
| | Pollution degree | | 2 | |
| | Climatic category | | 40/125/21 | |
| **UL 1577** | | | | |
| $V_{ISO}$ | Withstand isolation voltage | $V_{TEST}$ = $V_{ISO}$ = 5700 $V_{RMS}$, t = 60 sec. (qualification),<br>$V_{TEST}$ = 1.2 × $V_{ISO}$ = 6840$V_{RMS}$, t = 1 sec (100% production) | 5700 | $V_{RMS}$ |

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for basic electrical insulation only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device.


Copyright © 2022 Texas Instruments Incorporated

## 6.7 Safety-Related Certifications

| VDE | CSA | UL | CQC |
|---|---|---|---|
| Certified according to DIN VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 60950-1 (VDE 0805 Teil 1):2011-01 | Approved under CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 60601-1 | Certified according to UL 1577 component recognition program | Certified according to GB 4943.1-2011 |
| Reinforced insulation maximum transient isolation voltage, 8000 $V_{PK}$; maximum repetitive peak isolation voltage, 2121 $V_{PK}$; maximum surge isolation voltage, 8000 $V_{PK}$ | Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed. | Single protection, 5700 $V_{RMS}$ | Reinforced insulation, Altitude ≤ 5000 m, Tropical climate, 400 $V_{RMS}$ maximum working voltage |
| Certification number: 40040142 | Agency qualification planned | File number: E181974 | Certification number: CQC16001155011 |

## 6.8 Safety-Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

| PARAMETER | | TEST CONDITIONS | SIDE | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_S$ | Safety output supply current | $R_{\theta JA}$ = 78.1°C/W, VDDA/B = 12 V, $T_A$ = 25°C, $T_J$ = 150°C See 图 6-2 | DRIVER A, DRIVER B | | | 64 | mA |
| | | $R_{\theta JA}$ = 78.1°C/W, VDDA/B = 25 V, $T_A$ = 25°C, $T_J$ = 150°C | DRIVER A, DRIVER B | | | 31 | mA |
| $P_S$ | Safety supply power | $R_{\theta JA}$ = 78.1°C/W, $T_A$ = 25°C, $T_J$ = 150°C See 图 6-3 | INPUT | | | 50 | mW |
| | | | DRIVER A | | | 775 | |
| | | | DRIVER B | | | 775 | |
| | | | TOTAL | | | 1600 | |
| $T_S$ | Safety temperature | | | | | 150 | °C |

The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the 节 6.4 table is that of a device installed on a High-K test board for leaded surface mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

Copyright © 2022 Texas Instruments Incorporated

## 6.9 Electrical Characteristics

$V_{VCCI}$ = 3.3 V or $V_{VCCI}$ = 5 V, 0.1-µF capacitor from VCCI to GND, $V_{VDDA}$ = $V_{VDDB}$ = 12 V, 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, $T_A$ = – 40°C to +125°C, (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENTS** | | | | | | |
| $I_{VCCI}$ | VCCI quiescent current | DISABLE = VCCI | | 1.5 | 2.0 | mA |
| $I_{VDDA}$, $I_{VDDB}$ | VDDA and VDDB quiescent current | DISABLE = VCCI | | 1.0 | 1.8 | mA |
| $I_{VCCI}$ | VCCI operating current | (f = 500 kHz) current per channel, $C_{OUT}$ = 100 pF | | 2.5 | | mA |
| $I_{VDDA}$, $I_{VDDB}$ | VDDA and VDDB operating current | (f = 500 kHz) current per channel, $C_{OUT}$ = 100 pF | | 2.5 | | mA |
| **VCCI SUPPLY UNDERVOLTAGE LOCKOUT THRESHOLDS** | | | | | | |
| $V_{VCCI_ON}$ | Rising threshold VCCI_ON | | 2.55 | 2.7 | 2.85 | V |
| $V_{VCCI_OFF}$ | Falling threshold VCCI_OFF | | 2.35 | 2.5 | 2.65 | V |
| $V_{VCCI_HYS}$ | Threshold hysteresis | | | 0.2 | | V |
| **VDDA/VDDB SUPPLY UNDERVOLTAGE LOCKOUT THRESHOLDS** | | | | | | |
| $V_{VDDA_ON}$, $V_{VDDB_ON}$ | Rising threshold VDDA_ON, VDDB_ON | | 8 | 8.5 | 9 | V |
| $V_{VDDA_OFF}$, $V_{VDDB_OFF}$ | Falling threshold VDDA_OFF, VDDB_OFF | | 7.5 | 8 | 8.5 | V |
| $V_{VDDA_HYS}$, $V_{VDDB_HYS}$ | Threshold hysteresis | | | 0.5 | | V |
| **PWM AND DISABLE** | | | | | | |
| $V_{PWMH}$, $V_{DISH}$ | Input high voltage | | 1.6 | 1.8 | 2 | V |
| $V_{PWML}$, $V_{DISL}$ | Input low voltage | | 0.8 | 1 | 1.2 | V |
| $V_{PWM_HYS}$, $V_{DIS_HYS}$ | Input hysteresis | | | 0.8 | | V |
| $V_{PWM}$ | Negative transient, ref to GND, 50 ns pulse | Not production tested, bench test only | – 5 | | | V |


Copyright © 2022 Texas Instruments Incorporated

$V_{VCCI}$ = 3.3 V or $V_{VCCI}$ = 5 V, 0.1-µF capacitor from VCCI to GND, $V_{VDDA}$ = $V_{VDDB}$ = 12 V, 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, $T_A$ = –40°C to +125°C, (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OUTPUT** | | | | | | |
| $I_{OA+}$, $I_{OB+}$ | Peak output source current | $C_{VDD}$ = 10 µF, $C_{LOAD}$ = 0.18 µF, f = 1 kHz, bench measurement | | 4 | | A |
| $I_{OA-}$, $I_{OB-}$ | Peak output sink current | $C_{VDD}$ = 10 µF, $C_{LOAD}$ = 0.18 µF, f = 1 kHz, bench measurement | | 6 | | A |
| $R_{OHA}$, $R_{OHB}$ | Output resistance at high state | $I_{OUT}$ = –10 mA, $T_A$ = 25°C, $R_{OHA}$, $R_{OHB}$ do not represent drive pull-up performance. See $t_{RISE}$ in 节 6.10 and 节 8.3.4 for details. | | 5 | | Ω |
| $R_{OLA}$, $R_{OLB}$ | Output resistance at low state | $I_{OUT}$ = 10 mA, $T_A$ = 25°C | | 0.55 | | Ω |
| $V_{OHA}$, $V_{OHB}$ | Output voltage at high state | $V_{VDDA}$, $V_{VDDB}$ = 12 V, $I_{OUT}$ = –10 mA, $T_A$ = 25°C | | 11.95 | | V |
| $V_{OLA}$, $V_{OLB}$ | Output voltage at low state | $V_{VDDA}$, $V_{VDDB}$ = 12 V, $I_{OUT}$ = 10 mA, $T_A$ = 25°C | | 5.5 | | mV |
| **DEADTIME AND OVERLAP PROGRAMMING** | | | | | | |
| Dead time | | Pull DT pin to VCCI | | 0 | | ns |
| | | DT pin is left open, min spec characterized only, tested for outliers | | 8 | 15 | ns |
| | | $R_{DT}$ = 20 kΩ | 160 | 200 | 240 | ns |

## 6.10 Switching Characteristics

$V_{VCCI}$ = 3.3 V or 5 V, 0.1-µF capacitor from VCCI to GND, $V_{VDDA}$ = $V_{VDDB}$ = 12 V, 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, $T_A$ = –40°C to +125°C, (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{RISE}$ | Output rise time, 20% to 80% measured points | $C_{OUT}$ = 1.8 nF | | 6 | 16 | ns |
| $t_{FALL}$ | Output fall time, 90% to 10% measured points | $C_{OUT}$ = 1.8 nF | | 7 | 12 | ns |
| $t_{PWmin}$ | Minimum pulse width | Output off for less than minimum, $C_{OUT}$ = 0 pF | | | 20 | ns |
| $t_{PDHL}$ | Propagation delay from INx to OUTx falling edges | | | 19 | 30 | ns |
| $t_{PDLH}$ | Propagation delay from INx to OUTx rising edges | | | 19 | 30 | ns |
| $t_{PWD}$ | Pulse width distortion $\lvert t_{PDLH} - t_{PDHL} \rvert$ | | | | 6 | ns |
| $t_{DM}$ | Propagation delays matching between VOUTA, VOUTB | f = 100 kHz | | | 5 | ns |
| CMTI | Static common-mode transient immunity (See 节 7.5) | Slew rate of GND versus VSSA and VSSB, PWM is tied to GND or VCCI | 100 | | | V/ns |

Copyright © 2022 Texas Instruments Incorporated

## 6.11 Insulation Characteristics Curves

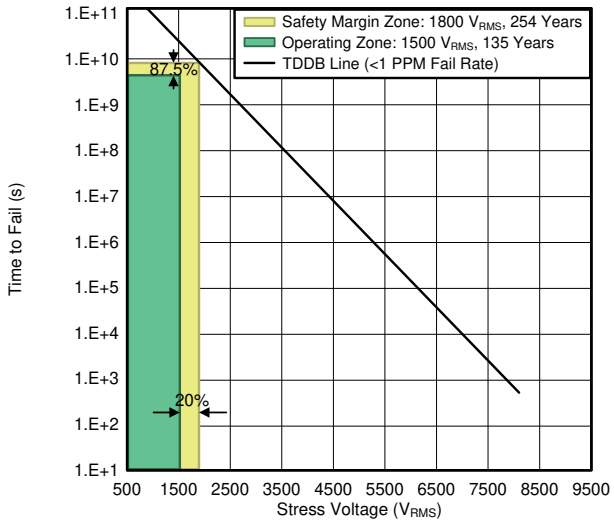



**图 6-1. Reinforced Isolation Capacitor Life Time Projection**

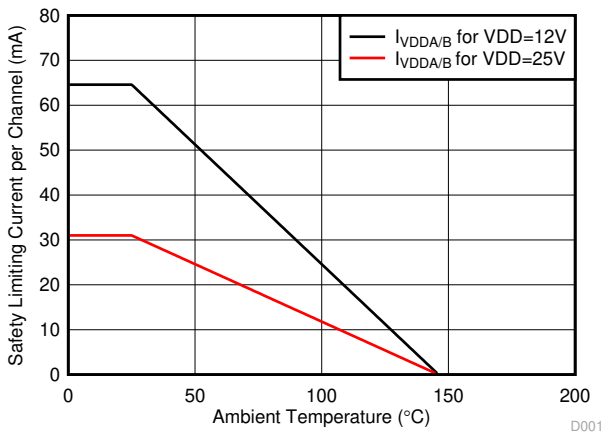



**图 6-2. Thermal Derating Curve for Safety-Related Limiting Current (Current in Each Channel with Both Channels Running Simultaneously)**

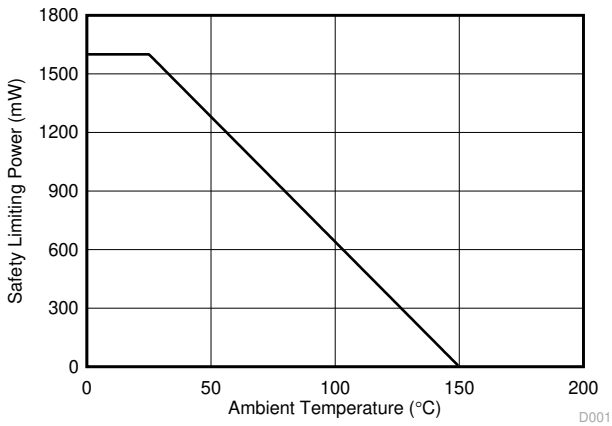
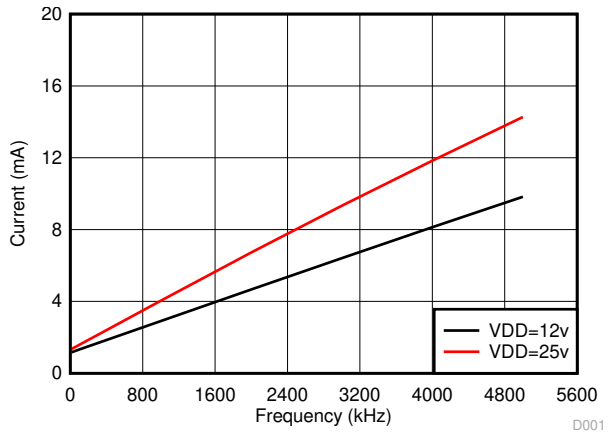



**图 6-3. Thermal Derating Curve for Safety-Related Limiting Power**


Copyright © 2022 Texas Instruments Incorporated

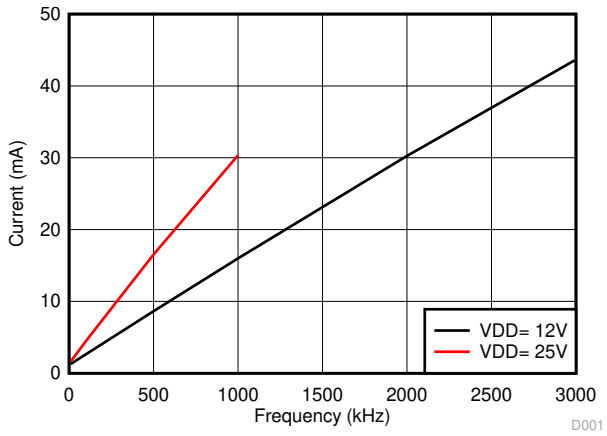
## 6.12 Typical Characteristics

VDDA = VDDB= 12 V, VCCI = 3.3 V, $T_A$ = 25°C, No load unless otherwise noted.



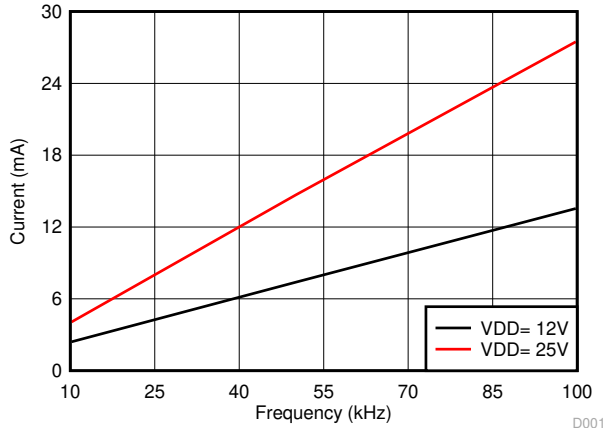

No load

**图 6-4. Per Channel Current Consumption vs. Frequency**



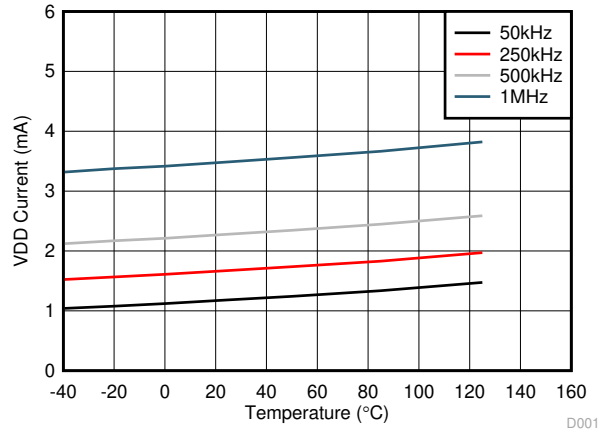

$C_{LOAD}$ = 1 nF

**图 6-5. Per Channel Current Consumption ($I_{VDDA/B}$) vs. Frequency**




$C_{LOAD}$ = 10 nF

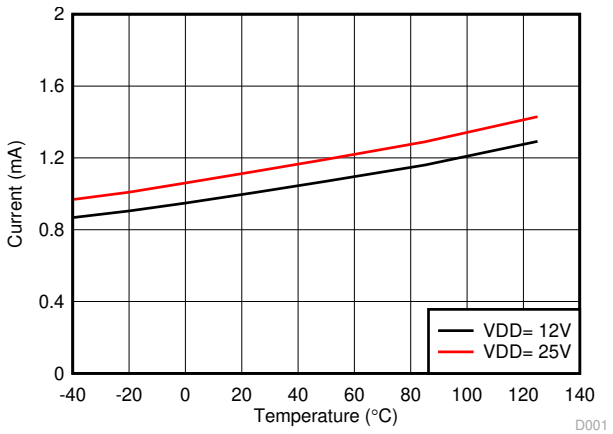
**图 6-6. Per Channel Current Consumption ($I_{VDDA/B}$) vs. Frequency**




No load

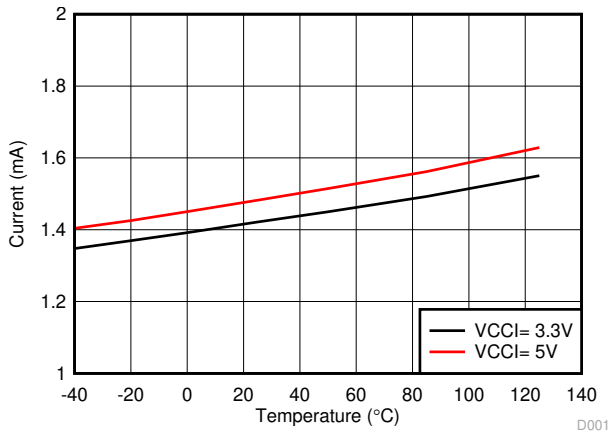
**图 6-7. Per Channel ($I_{VDDA/B}$) Supply Current Vs. Temperature**

Copyright © 2022 Texas Instruments Incorporated



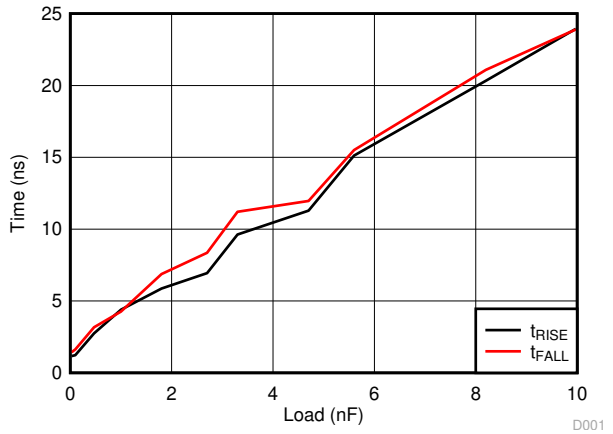

No load Input low No switching

**图 6-8. Per Channel ($I_{VDDA/B}$) Quiescent Supply Current vs Temperature**




No load DIS is high No switching

**图 6-9. $I_{VCCI}$ Quiescent Supply Current vs Temperature**




VDD = 12 V

**图 6-10. Rising and Falling Times vs. Load**

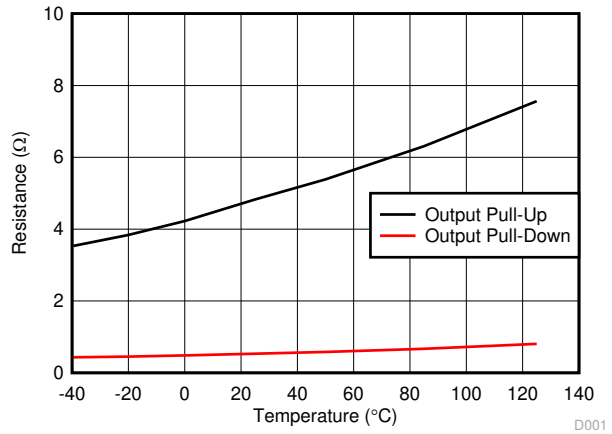



**图 6-11. Output Resistance vs. Temperature**

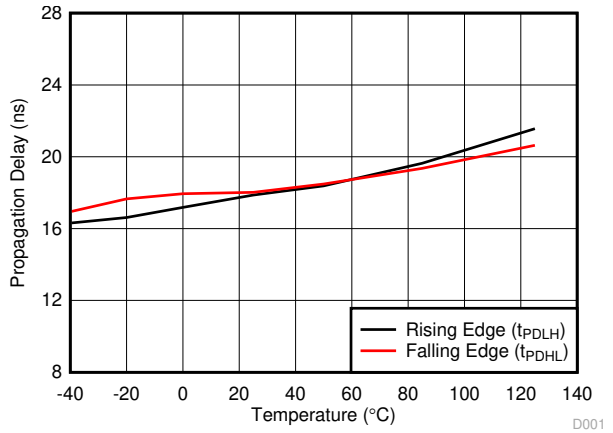



**图 6-12. Propagation Delay vs. Temperature**

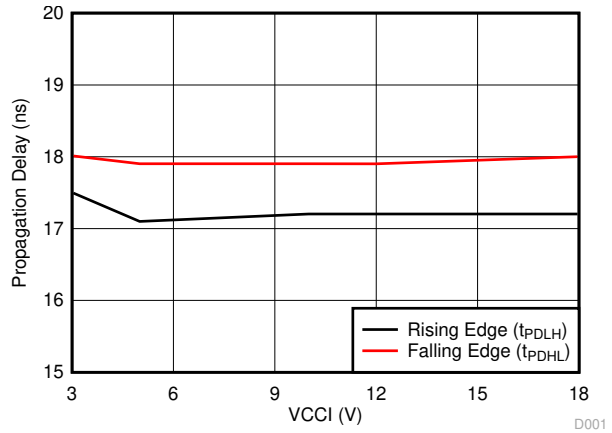



**图 6-13. Propagation Delay vs. VCCI**


Copyright © 2022 Texas Instruments Incorporated

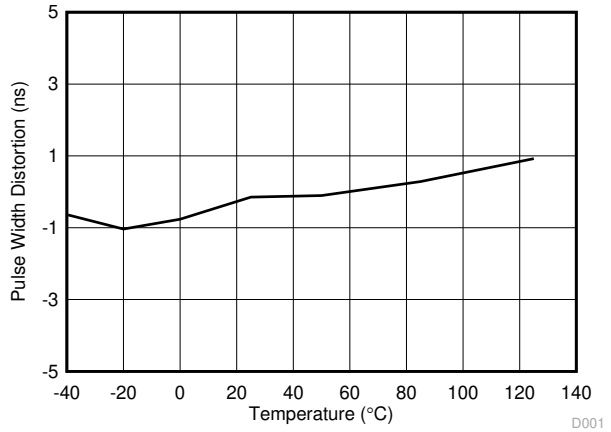



图 6-14. Pulse Width Distortion vs. Temperature

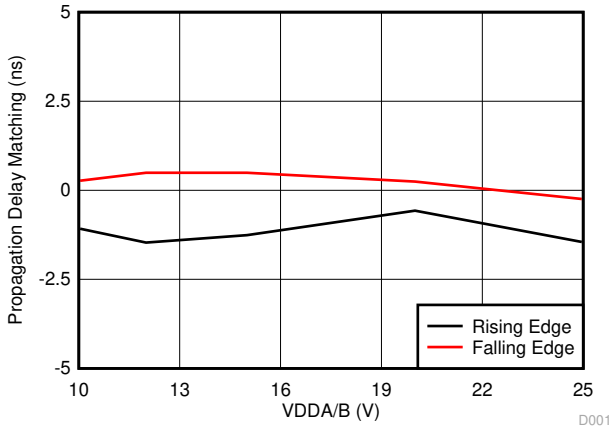



图 6-15. Propagation Delay Matching ($t_{DM}$) vs. VDD

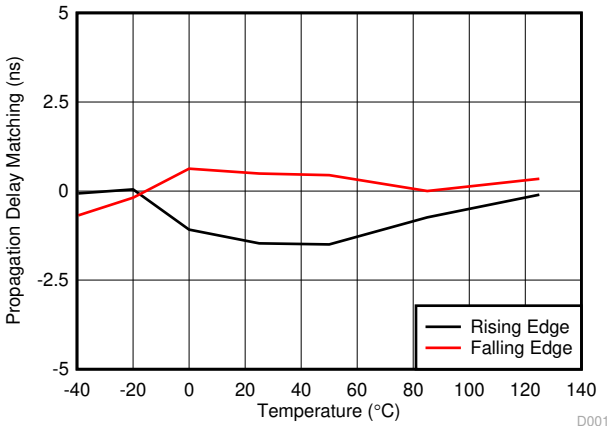



图 6-16. Propagation Delay Matching ($t_{DM}$) vs. Temperature

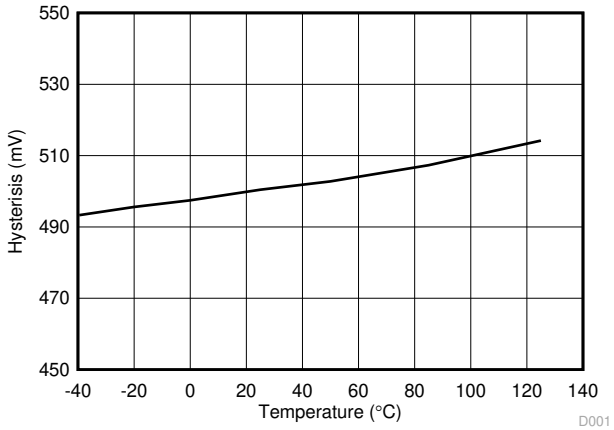



图 6-17. VDD UVLO Hysteresis vs. Temperature

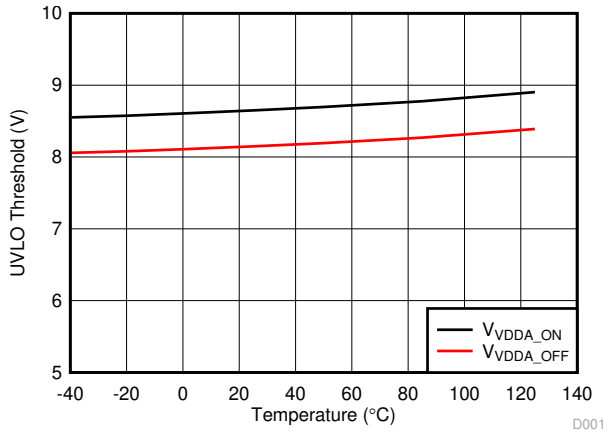



图 6-18. VDD UVLO Threshold vs. Temperature

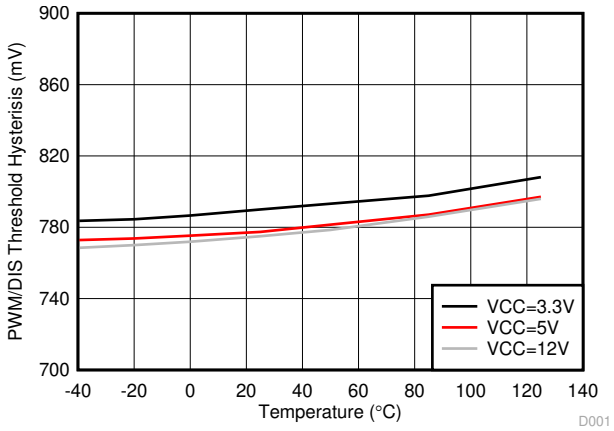



图 6-19. PWM/DIS Hysteresis vs. Temperature

Copyright © 2022 Texas Instruments Incorporated

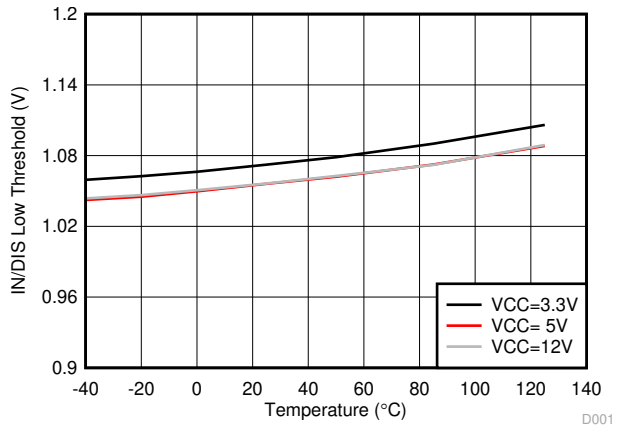



图 6-20. PWM/DIS Low Threshold

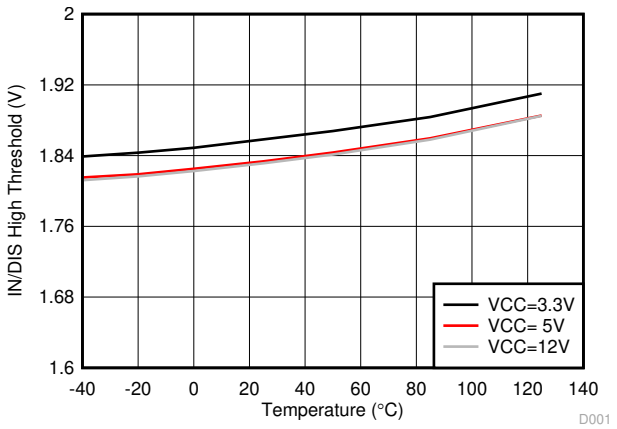



图 6-21. PWM/DIS High Threshold

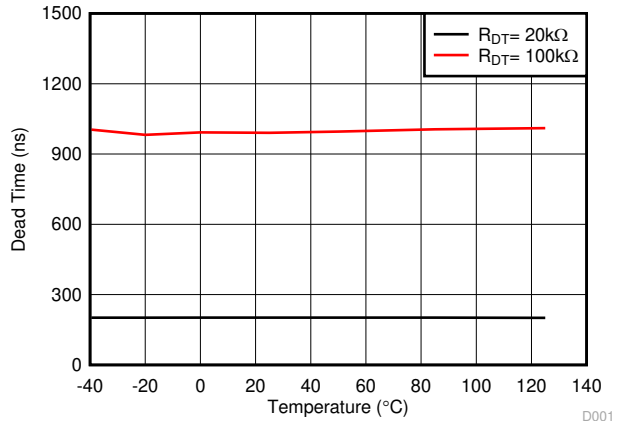



图 6-22. Dead Time vs. Temperature

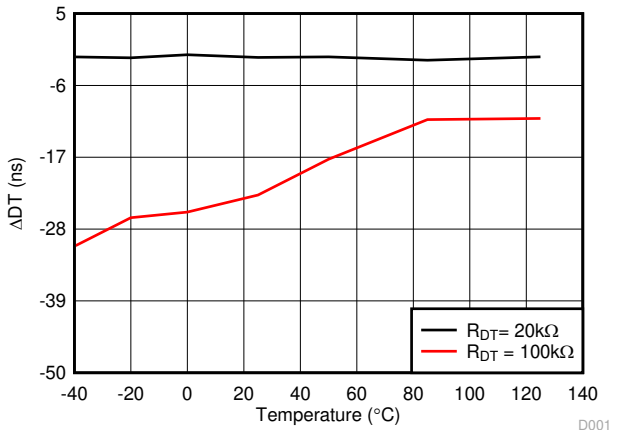



图 6-23. Dead Time Matching vs. Temperature

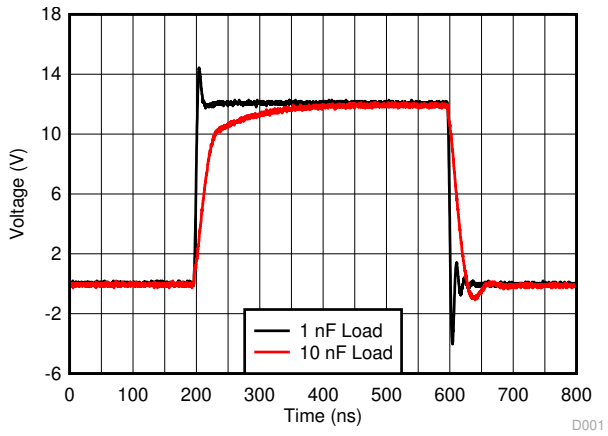



图 6-24. Typical Output Voltage


Copyright © 2022 Texas Instruments Incorporated

# 7 Parameter Measurement Information

## 7.1 Propagation Delay and Pulse Width Distortion

图 7-1 shows how one calculates pulse width distortion ($t_{PWD}$) and delay matching ($t_{DM}$) from the propagation delays of channels A and B. It can be measured by disabling the dead time function by shorting the DT Pin to VCC.

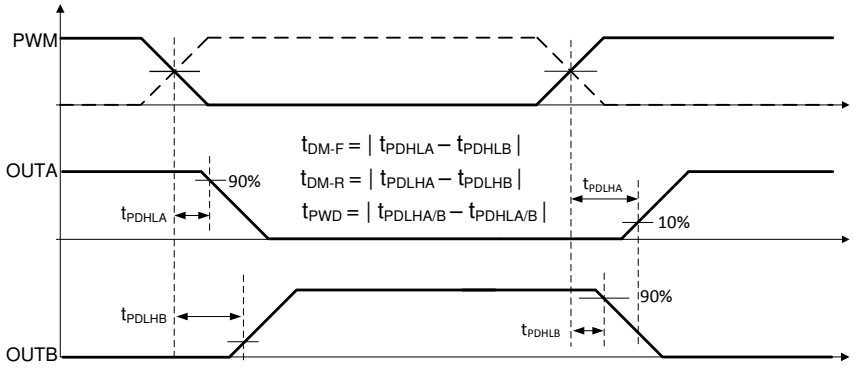



**图 7-1. Propagation Delay Matching and Pulse Width Distortion**

## 7.2 Rising and Falling Time

图 7-2 shows the criteria for measuring rising ($t_{RISE}$) and falling ($t_{FALL}$) times. For more information on how short rising and falling times are achieved see 节 8.3.4

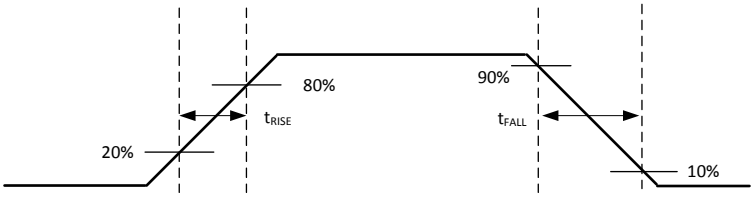



**图 7-2. Rising and Falling Time Criteria**

## 7.3 PWM Input and Disable Response Time

图 7-3 shows the response time of the disable function. For more information, see 节 8.4.1 .

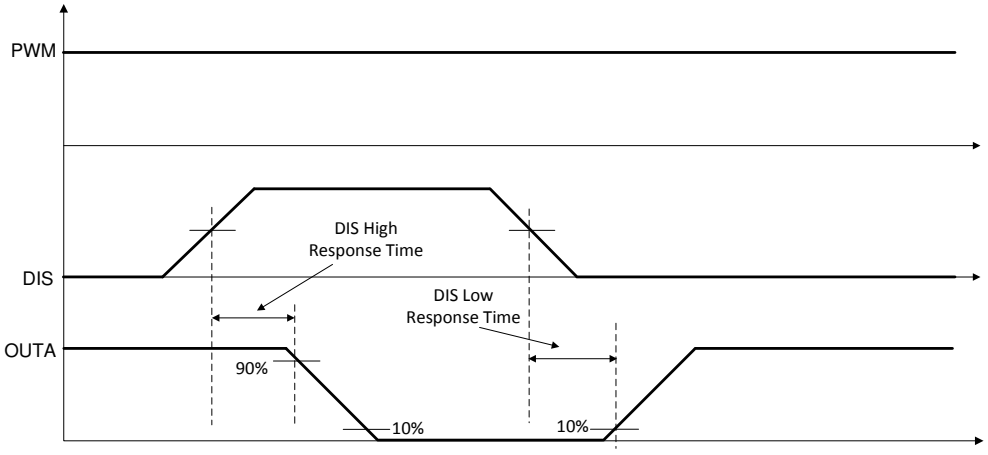



**图 7-3. Disable Pin Timing**

## 7.4 Programable Dead Time

Leaving the DT pin open or tying it to GND through an appropriate resistor ($R_{DT}$) sets a dead-time interval. For more details on dead time, refer to 节 8.4.2 .

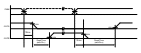


**图 7-4. Dead-Time Switching Parameters**

## 7.5 CMTI Testing

图 7-5 is a simplified diagram of the CMTI testing configuration.

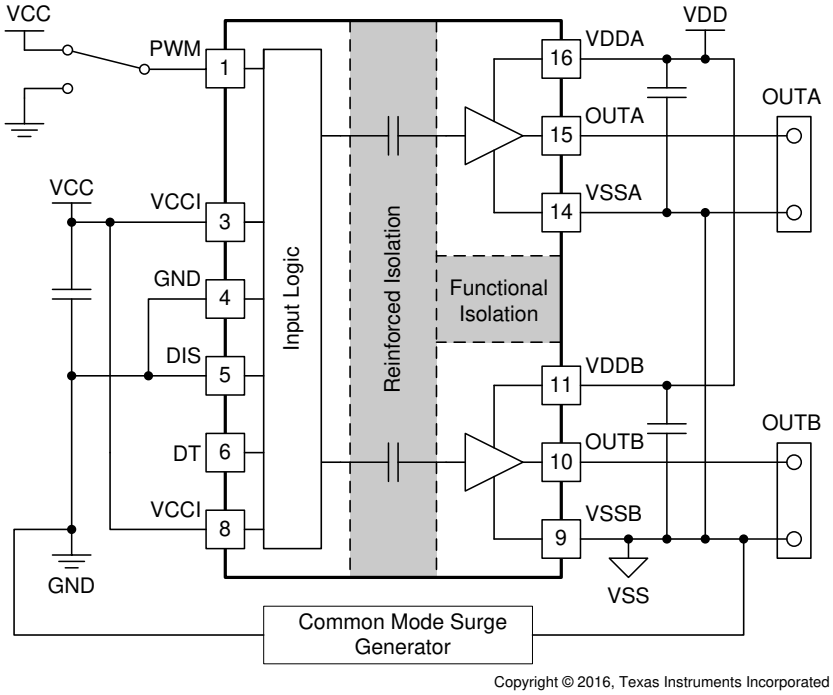



**图 7-5. Simplified CMTI Testing Setup**


Copyright © 2022 Texas Instruments Incorporated

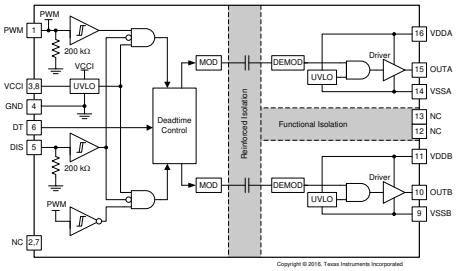
# 8 Detailed Description

## 8.1 Overview

In order to switch power transistors rapidly and reduce switching power losses, high-current gate drivers are often placed between the output of control devices and the gates of power transistors. There are several instances where controllers are not capable of delivering sufficient current to drive the gates of power transistors. This is especially the case with digital controllers, since the input signal from the digital controller is often a 3.3-V logic signal capable of only delivering a few mA.

The UCC20520 is a flexible dual gate driver which can be configured to fit a variety of power supply and motor drive topologies, as well as drive several types of transistors, including SiC MOSFETs. UCC20520 has many features that allow it to integrate well with control circuitry and protect the gates it drives such as: resistor-programmable dead time (DT) control, a DISABLE pin, and under voltage lock out (UVLO) for both input and output voltages. The UCC20520 also holds its OUTA low when the PWM is left open or when the PWM pulse is not wide enough. The driver input PWM is CMOS and TTL compatible for interfacing to digital and analog power controllers alike. Importantly, Channel A is in phase with PWM input and Channel B is always complimentary with Channel A with programmed deadtime.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 VDD, VCCI, and Under Voltage Lock Out (UVLO)

The UCC20520 has an internal under voltage lock out (UVLO) protection feature on the supply circuit blocks between the VDD and VSS pins for both outputs. When the VDD bias voltage is lower than $V_{VDD_ON}$ at device start-up or lower than $V_{VDD_OFF}$ after start-up, the VDD UVLO feature holds the effected outputs low, regardless of the status of the input pin (PWM).

When the output stages of the driver are in an unbiased or UVLO condition, the driver outputs are held low by an active clamp circuit that limits the voltage rise on the driver outputs (Illustrated in 图 8-1 ). In this condition, the upper PMOS is resistively held off by $R_{Hi-Z}$ while the lower NMOS gate is tied to the driver output through $R_{CLAMP}$. In this configuration, the output is effectively clamped to the threshold voltage of the lower NMOS device, typically less than 1.5V, when no bias power is available.

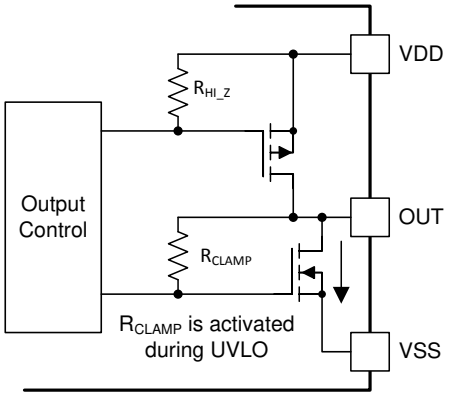



**图 8-1. Simplified Representation of Active Pull Down Feature**

The VDD UVLO protection has a hysteresis feature ($V_{VDD_HYS}$). This hysteresis prevents chatter when there is ground noise from the power supply. Also this allows the device to accept small drops in bias voltage, which is bound to happen when the device starts switching and operating current consumption increases suddenly.

The input side of the UCC20520 also has an internal under voltage lock out (UVLO) protection feature. The device isn't active unless the voltage, VCCI, is going to exceed $V_{VCCI_ON}$ on start up. And a signal will cease to be delivered when that pin receives a voltage less than $V_{VCCI_OFF}$. And, just like the UVLO for VDD, there is hystersis ($V_{VCCI_HYS}$) to ensure stable operation.


Copyright © 2022 Texas Instruments Incorporated

All versions of the UCC20520 can withstand an absolute maximum of 30 V for VDD, and 20 V for VCCI.

**表 8-1. UCC20520 VCCI UVLO Feature Logic**

| CONDITION | INPUT | OUTPUTS | |
|---|---|---|---|
| | PWM | OUTA | OUTB |
| VCCI-GND < $V_{VCCI_ON}$ during device start up | H | L | L |
| VCCI-GND < $V_{VCCI_ON}$ during device start up | L | L | L |
| VCCI-GND < $V_{VCCI_OFF}$ after device start up | H | L | L |
| VCCI-GND < $V_{VCCI_OFF}$ after device start up | L | L | L |

**表 8-2. UCC20520 VDD UVLO Feature Logic**

| CONDITION | INPUT | OUTPUTS | |
|---|---|---|---|
| | PWM | OUTA | OUTB |
| VDD-VSS < $V_{VDD_ON}$ during device start up | H | L | L |
| VDD-VSS < $V_{VDD_ON}$ during device start up | L | L | L |
| VDD-VSS < $V_{VDD_OFF}$ after device start up | H | L | L |
| VDD-VSS < $V_{VDD_OFF}$ after device start up | L | L | L |

### 8.3.2 Input and Output Logic Table

**表 8-3. INPUT/OUTPUT Logic Table(1)**

Assume VCCI, VDDA, VDDB are powered up. See 节 8.3.1 for more information on UVLO operation modes.

| INPUT | DISABLE | OUTPUTS | | NOTE |
|---|---|---|---|---|
| PWM | | OUTA | OUTB | |
| L or Left Open | L or Left Open | L | H | Output transitions occur after the dead time expires. See 节 8.4.2 |
| H | L or Left Open | H | L | |
| X | H | L | L | - |

(1) "X" means L, H or left open.

### 8.3.3 Input Stage

The input pins (PWM and DIS) of UCC20520 are based on a TTL and CMOS compatible input-threshold logic that is totally isolated from the VDD supply voltage. The input pins are easy to drive with logic-level control signals (Such as those from 3.3-V micro-controllers), since UCC20520 has a typical high threshold ($V_{PWMH}$) of 1.8 V and a typical low threshold of 1 V, which vary little with temperature (see 图 6-20, 图 6-21). A wide hysteresis ($V_{PWM_HYS}$) of 0.8 V makes for good noise immunity and stable operation. If any of the inputs are ever left open, internal pull-down resistors force the pin low. These resistors are typically 200 kΩ (See 节 8.2). However, it is still recommended to ground an input if it is not being used.

Since the input side of UCC20520 is isolated from the output drivers, the input signal amplitude can be larger or smaller than VDD, provided that it doesn’t exceed the recommended limit. This allows greater flexibility when integrating with control signal sources, and allows the user to choose the most efficient VDD for their chosen gate. That said, the amplitude of any signal applied to PWM must *never* be at a voltage higher than VCCI.

Copyright © 2022 Texas Instruments Incorporated

### 8.3.4 Output Stage

The UCC20520’s output stages features a pull-up structure which delivers the highest peak-source current when it is most needed, during the Miller plateau region of the power-switch turn on transition (when the power switch drain or collector voltage experiences dV/dt). The output stage pull-up structure features a P-channel MOSFET and an additional *Pull-Up* N-channel MOSFET in parallel. The function of the N-channel MOSFET is to provide a brief boost in the peak-sourcing current, enabling fast turn on. This is accomplished by briefly turning on the N-channel MOSFET during a narrow instant when the output is changing states from low to high. The on-resistance of this N-channel MOSFET ($R_{NMOS}$) is approximately 1.47 Ω when activated.

The $R_{OH}$ parameter is a DC measurement and it is representative of the on-resistance of the P-channel device only. This is because the *Pull-Up* N-channel device is held in the off state in DC condition and is turned on only for a brief instant when the output is changing states from low to high. Therefore the effective resistance of the UCC20520 pull-up stage during this brief turn-on phase is much lower than what is represented by the $R_{OH}$ parameter. Therefore, the value of $R_{OH}$ belies the fast nature of the UCC20520's turn-on time.

The pull-down structure in UCC20520 is simply composed of an N-channel MOSFET. The $R_{OL}$ parameter, which is also a DC measurement, is representative of the impedance of the pull-down state in the device. Both outputs of the UCC20520 are capable of delivering 4-A peak source and 6-A peak sink current pulses. The output voltage swings between VDD and VSS provides rail-to-rail operation, thanks to the MOS-out stage which delivers very low drop-out.

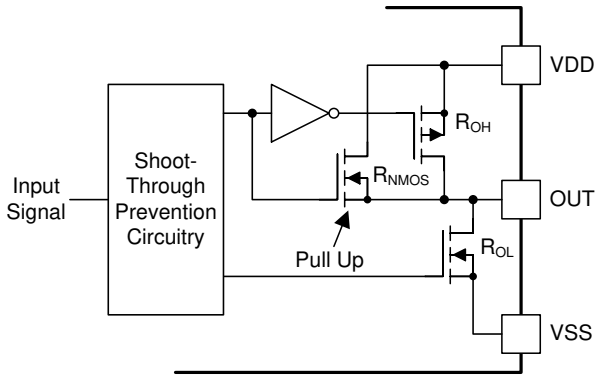



**图 8-2. Output Stage**


Copyright © 2022 Texas Instruments Incorporated

### 8.3.5 Diode Structure in UCC20520

图 8-3 illustrates the multiple diodes involved in the ESD protection components of the UCC20520. This provides a pictorial representation of the absolute maximum rating for the device.

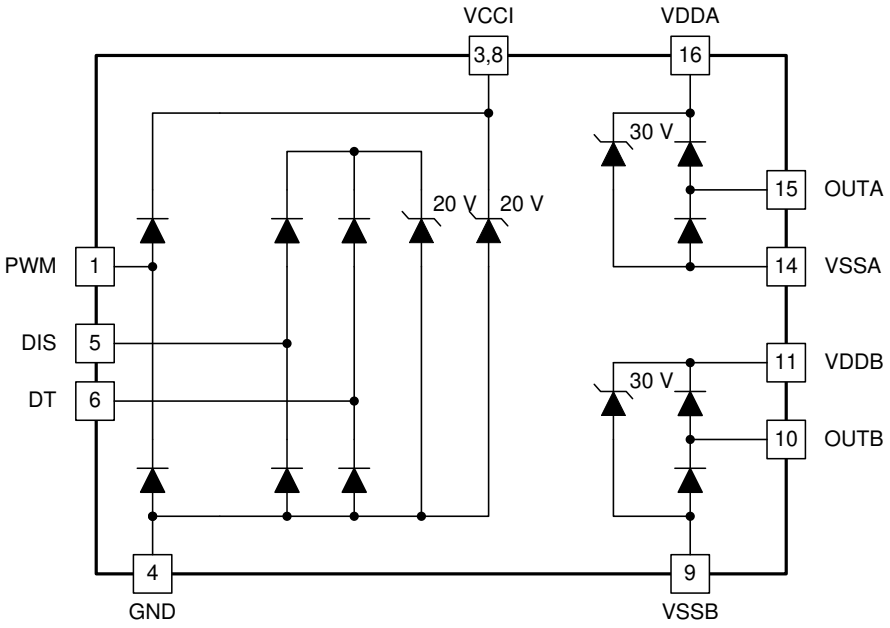



**图 8-3. ESD Structure**

## 8.4 Device Functional Modes

### 8.4.1 Disable Pin

Setting the DISABLE pin high shuts down both outputs simultaneously. Grounding (or left open) the DISABLE pin allows UCC20520 to operate normally. The DISABLE response time is in the range of 20ns and quite responsive, which is as fast as propagation delay. The DISABLE pin is only functional (and necessary) when VCCI stays above the UVLO threshold. It is recommended to tie this pin to ground if the DISABLE pin is not used to achieve better noise immunity.

### 8.4.2 Programmable Dead Time (DT) Pin

UCC20520 allows the user to adjust dead time (DT) in the following ways:

#### *8.4.2.1 Tying the DT Pin to VCC*

If DT pin is tied to VCC, dead time function between OUTA and OUTB is disabled and the deadtime between the two output channels is around 0ns.

Copyright © 2022 Texas Instruments Incorporated

#### 8.4.2.2 DT Pin Left Open or Connected to a Programming Resistor between DT and GND Pins

If the DT pin is left open, the dead time duration ($t_{DT}$) is set to <15 ns. One can program $t_{DT}$ by placing a resistor, $R_{DT}$, between the DT pin and GND. The appropriate $R_{DT}$ value can be determined from 方程式 1, where $R_{DT}$ is in kΩ and $t_{DT}$ in ns:

#### 8.4.2.3

$$t_{DT} \approx 10 \times R_{DT} \quad (1)$$

The steady state voltage at DT pin is around 0.8V, and the DT pin current will be less than 10uA when $R_{DT}$=100kΩ. Therefore, It is recommended to parallel a ceramic capacitor, 2.2nF or above, with $R_{DT}$ to achieve better noise immunity and better deadtime matching between two channels, especially when the dead time is larger than 300ns. The major consideration is that the current through the $R_{DT}$ is used to set the dead time, and this current decreases as $R_{DT}$ increases.

PWM input signal’s falling edge activates the programmed dead time for the other signal. The output signals’ dead time is always set to the driver’s programmed dead time. Various driver dead time logic operating conditions are illustrated and explained in 图 8-4:

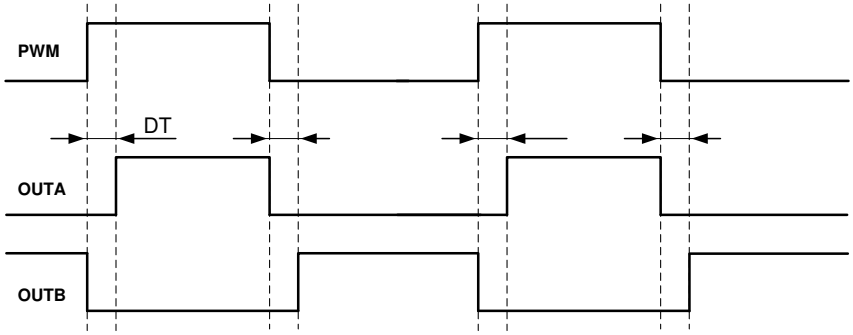



**图 8-4. Input and Output Logic Relationship with Dead Time**


Copyright © 2022 Texas Instruments Incorporated

# 9 Application and Implementation

**备注**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

The UCC20520 effectively combines both isolation and buffer-drive functions. The flexible, universal capability of the UCC20520 (with up to 18-V VCCI and 25-V VDDA/VDDB) allows the device to be used as a low-side, high-side, high-side/low-side or half-bridge driver for MOSFETs, IGBTs or SiC MOSFETs. With integrated components, advanced protection features (UVLO, dead time, and disable) and optimized switching performance; the UCC20520 enables designers to build smaller, more robust designs for enterprise, telecom, automotive, and industrial applications with a faster time to market.

## 9.2 Typical Application

图 9-1 shows a reference design with UCC20520 driving a typical half-bridge configuration which can be used in several popular power converter topologies such as synchronous buck, synchronous boost, half-bridge/full bridge isolated topologies, and three-phase motor drive applications.

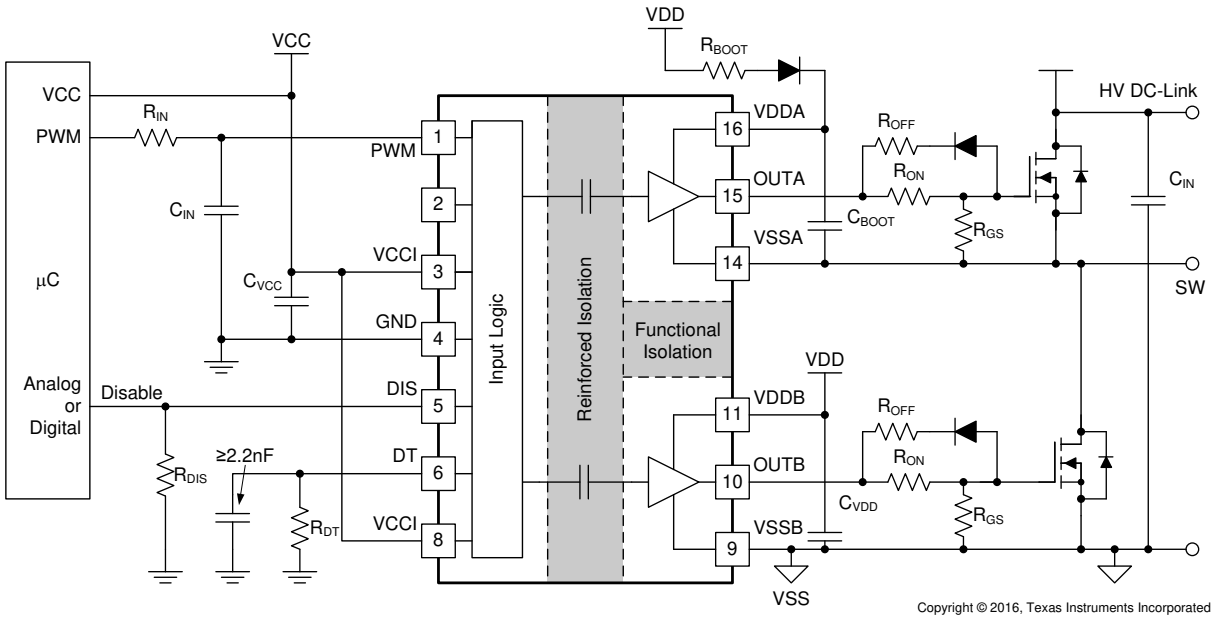



**图 9-1. Typical Application**

### 9.2.1 Design Requirements

表 9-1 lists reference design parameters for the example application: UCC20520 driving 1200-V SiC-MOSFETs in a high side-low side configuration.

**表 9-1. UCC20520 Design Requirements**

| PARAMETER | VALUE | UNITS |
|---|---|---|
| Power transistor | C2M0080120D | - |
| VCC | 5.0 | V |
| VDD | 20 | V |
| Input signal amplitude | 0 ↔ 3.3 | V |
| Switching frequency ($f_s$) | 100 | kHz |
| DC link voltage | 800 | V |

### 9.2.2 Detailed Design Procedure

#### *9.2.2.1 Designing PWM Input Filter*

It is recommended that users avoid shaping the signals to the gate driver in an attempt to slow down (or delay) the signal at the output. However, a small input $R_{IN}$-$C_{IN}$ filter can be used to filter out the ringing introduced by non-ideal layout or long PCB traces.

Such a filter should use an $R_{IN}$ in the range of 0 Ω to100 Ω and a $C_{IN}$ between 10 pF and 100 pF. In the example, an $R_{IN}$ = 51 Ω and a $C_{IN}$ = 33 pF are selected, with a corner frequency of approximately 100 MHz.

When selecting these components, it is important to pay attention to the trade-off between good noise immunity and propagation delay.

#### *9.2.2.2 Select External Bootstrap Diode and its Series Resistor*

The bootstrap capacitor is charged by VDD through an external bootstrap diode every cycle when the low side transistor turns on. Charging the capacitor involves high-peak currents, and therefore transient power dissipation in the bootstrap diode may be significant. Conduction loss also depends on the diode’s forward voltage drop. Both the diode conduction losses and reverse recovery losses contribute to the total losses in the gate driver circuit.

When selecting external bootstrap diodes, it is recommended that one chose high voltage, fast recovery diodes or SiC Schottky diodes with a low forward voltage drop and low junction capacitance in order to minimize the loss introduced by reverse recovery and related grounding noise bouncing. In the example, the DC-link voltage is 800 $V_{DC}$. The voltage rating of the bootstrap diode should be higher than the DC-link voltage with a good margin. Therefore, a 1200-V SiC diode, C4D02120E, is chosen in this example.

A bootstrap resistor, $R_{BOOT}$, is used to reduce the inrush current in $D_{BOOT}$ and limit the ramp up slew rate of voltage of VDDA-VSSA during each switching cycle, especially when the VSSA(SW) pin has an excessive negative transient voltage. The recommended value for $R_{BOOT}$ is between 1 Ω and 20 Ω depending on the diode used. In the example, a current limiting resistor of 2.2 Ω is selected to limit the inrush current of bootstrap diode. The estimated worst case peak current through $D_{Boot}$ is,

$$I_{DBoot(pk)} = \frac{V_{DD} - V_{BDF}}{R_{Boot}} = \frac{20V - 2.5V}{2.2\Omega} \approx 8A \quad (2)$$

where

- $V_{BDF}$ is the estimated bootstrap diode forward voltage drop at 8 A.


Copyright © 2022 Texas Instruments Incorporated

#### 9.2.2.3 Gate Driver Output Resistor

The external gate driver resistors, $R_{ON}$/$R_{OFF}$, are used to:

1. Limit ringing caused by parasitic inductances/capacitances.
2. Limit ringing caused by high voltage/current switching dv/dt, di/dt, and body-diode reverse recovery.
3. Fine-tune gate drive strength, i.e. peak sink and source current to optimize the switching loss.
4. Reduce electromagnetic interference (EMI).

As mentioned in 节 8.3.4, the UCC20520 has a pull-up structure with a P-channel MOSFET and an additional *pull-up* N-channel MOSFET in parallel. The combined peak source current is 4 A. Therefore, the peak source current can be predicted with:

$$I_{OA+} = \min\left(4A, \frac{V_{DD} - V_{BDF}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET_Int}}\right) \tag{3}$$

$$I_{OB+} = \min\left(4A, \frac{V_{DD}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET_Int}}\right) \tag{4}$$

where

- $R_{ON}$: External turn-on resistance.
- $R_{GFET_INT}$: Power transistor internal gate resistance, found in the power transistor datasheet.
- $I_{O+}$ = Peak source current – The minimum value between 4 A, the gate driver peak source current, and the calculated value based on the gate drive loop resistance.

In this example:

$$I_{OA+} = \frac{V_{DD} - V_{BDF}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET_Int}} = \frac{20V - 0.8V}{1.47\Omega \,||\, 5\Omega + 2.2\Omega + 4.6\Omega} \approx 2.4A \tag{5}$$

$$I_{OB+} = \frac{V_{DD}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET_Int}} = \frac{20V}{1.47\Omega \,||\, 5\Omega + 2.2\Omega + 4.6\Omega} \approx 2.5A \tag{6}$$

Therefore, the high-side and low-side peak source current is 2.4 A and 2.5 A respectively. Similarly, the peak sink current can be calculated with:

$$I_{OA-} = \min\left(6A, \frac{V_{DD} - V_{BDF} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET_Int}}\right) \tag{7}$$

$$I_{OB-} = \min\left(6A, \frac{V_{DD} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET_Int}}\right) \tag{8}$$

where

- $R_{OFF}$: External turn-off resistance;
- $V_{GDF}$: The anti-parallel diode forward voltage drop which is in series with $R_{OFF}$. The diode in this example is an MSS1P4.
- $I_{O-}$: Peak sink current – the minimum value between 6 A, the gate driver peak sink current, and the calculated value based on the gate drive loop resistance.

Copyright © 2022 Texas Instruments Incorporated

In this example,

$$I_{OA-} = \frac{V_{DD} - V_{BDF} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET_Int}} = \frac{20V - 0.8V - 0.75V}{0.55\Omega + 0\Omega + 4.6\Omega} \approx 3.6A \quad (9)$$

$$I_{OB-=} \frac{V_{DD} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET_Int}} = \frac{20V\text{-}0.75V}{0.55\Omega + 0\Omega + 4.6\Omega} \approx 3.7A \quad (10)$$

Therefore, the high-side and low-side peak sink current is 3.6 A and 3.7 A respectively.

Importantly, the estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate driver loop can slow down the peak gate drive current and introduce overshoot and undershoot. Therefore, it is strongly recommended that the gate driver loop should be minimized. On the other hand, the peak source/sink current is dominated by loop parasitics when the load capacitance ($C_{ISS}$) of the power transistor is very small (typically less than 1 nF), because the rising and falling time is too small and close to the parasitic ringing period.

#### *9.2.2.4 Estimate Gate Driver Power Loss*

The total loss, $P_G$, in the gate driver subsystem includes the power losses of the UCC20520 ($P_{GD}$) and the power losses in the peripheral circuitry, such as the external gate drive resistor. Bootstrap diode loss is not included in $P_G$ and not discussed in this section.

$P_{GD}$ is the key power loss which determines the thermal safety-related limits of the UCC20520, and it can be estimated by calculating losses from several components.

The first component is the static power loss, $P_{GDQ}$, which includes quiescent power loss on the driver as well as driver self-power consumption when operating with a certain switching frequency. $P_{GDQ}$ is measured on the bench with no load connected to OUTA and OUTB at a given VCCI, VDDA/VDDB, switching frequency and ambient temperature. 图 6-4 shows the per output channel current consumption vs. operating frequency with no load. In this example, $V_{VCCI}$ = 5 V and $V_{VDD}$ = 20 V. The current on each power supply, with PWM switching from 0 V to 3.3 V at 100 kHz is measured to be $I_{VCCI}$ = 2.5 mA, and $I_{VDDA}$ = $I_{VDDB}$ = 1.5 mA. Therefore, the $P_{GDQ}$ can be calculated with

$$P_{GDQ} = V_{VCCI} \times I_{VCCI} + V_{VDDA} \times I_{DDA} + V_{VDDB} \times I_{DDB} \approx 72mW \quad (11)$$

The second component is switching operation loss, $P_{GDO}$, with a given load capacitance which the driver charges and discharges the load during each switching cycle. Total dynamic loss due to load switching, $P_{GSW}$, can be estimated with

$$P_{GSW} = 2 \times V_{DD} \times Q_G \times f_{SW} \quad (12)$$

where

- $Q_G$ is the gate charge of the power transistor.

If a split rail is used to turn on and turn off, then VDD is going to be equal to difference between the positive rail to the negative rail.

So, for this example application:

$$P_{GSW} = 2 \times 20V \times 60nC \times 100kHz = 240mW \quad (13)$$


Copyright © 2022 Texas Instruments Incorporated

$Q_G$ represents the total gate charge of the power transistor switching 800 V at 20 A, and is subject to change with different testing conditions. The UCC20520 gate driver loss on the output stage, $P_{GDO}$, is part of $P_{GSW}$. $P_{GDO}$ will be equal to $P_{GSW}$ if the external gate driver resistances are zero, and all the gate driver loss is dissipated inside the UCC20520. If there are external turn-on and turn-off resistance, the total loss will be distributed between the gate driver pull-up/down resistances and external gate resistances. Importantly, the pull-up/down resistance is a linear and fixed resistance if the source/sink current is not saturated to 4 A/6 A, however, it will be non-linear if the source/sink current is saturated. Therefore, $P_{GDO}$ is different in these two scenarios.

**Case 1 - Linear Pull-Up/Down Resistor:**

$$P_{GDO} = P_{GSW} \times \left( \frac{R_{OH} \,||\, R_{NMOS}}{R_{OH} \,||\, R_{NMOS} + R_{ON} + R_{GFET_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET_Int}} \right) \tag{14}$$

In this design example, all the predicted source/sink currents are less than 4 A/6 A, therefore, the UCC20520 gate driver loss can be estimated with:

$$P_{GDO} = 240\text{mW} \times \left( \frac{5\Omega \,||\, 1.47\Omega}{5\Omega \,||\, 1.47\Omega + 2.2\Omega + 4.6\Omega} + \frac{0.55\Omega}{0.55\Omega + 0\Omega + 4.6\Omega} \right) \approx 60\text{mW} \tag{15}$$

**Case 2 - Nonlinear Pull-Up/Down Resistor:**

$$P_{GDO} = 2 \times f_{SW} \times \left[ 4\text{A} \times \int_0^{T_{R_Sys}} \left( V_{DD} - V_{OUTA/B}(t) \right) dt + 6\text{A} \times \int_0^{T_{F_Sys}} V_{OUTA/B}(t)\, dt \right] \tag{16}$$

where

- $V_{OUTA/B}(t)$ is the gate driver OUTA and OUTB pin voltage during the turn on and off transient, and it can be simplified that a constant current source (4 A at turn-on and 6 A at turn-off) is charging/discharging a load capacitor. Then, the $V_{OUTA/B}(t)$ waveform will be linear and the $T_{R_Sys}$ and $T_{F_Sys}$ can be easily predicted.

For some scenarios, if only one of the pull-up or pull-down circuits is saturated and another one is not, the $P_{GDO}$ will be a combination of Case 1 and Case 2, and the equations can be easily identified for the pull-up and pull-down based on the above discussion. Therefore, total gate driver loss dissipated in the gate driver UCC20520, $P_{GD}$, is:

$$P_{GD} = P_{GDQ} + P_{GDO} \tag{17}$$

which is equal to 127 mW in the design example.

#### *9.2.2.5 Estimating Junction Temperature*

The junction temperature ($T_J$) of the UCC20520 can be estimated with:

$$T_J = T_C + R_{\theta JC} \times P_{GD} \tag{18}$$

where

- $T_C$ is the UCC20520 case-top temperature measured with a thermocouple or some other instrument, $R_{\theta JC}$ is the Junction-to-case-top thermal resistance from the 节 6.4 table. Importantly, $R_{\theta JA}$, the junction to ambient thermal impedance provided in the Thermal Information table, is developed based on JEDEC standard PCB board and it is subject to change when the PCB board layout is different.

Copyright © 2022 Texas Instruments Incorporated

#### 9.2.2.6 Selecting VCCI, VDDA/B Capacitor

Bypass capacitors for VCCI, VDDA, and VDDB are essential for achieving reliable performance. It is recommended that one choose low ESR and low ESL surface-mount multi-layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients and capacitance tolerances. Importantly, DC bias on an MLCC will impact the actual capacitance value. For example, a 25-V, 1-µF X7R capacitor is measured to be only 500 nF when a DC bias of 15 $V_{DC}$ is applied.

##### 9.2.2.6.1 Selecting a VCCI Capacitor

A bypass capacitor connected to VCCI supports the transient current needed for the primary logic and the total current consumption, which is only a few mA. Therefore, a 50-V MLCC with over 100 nF is recommended for this application. If the bias power supply output is a relatively long distance from the VCCI pin, a tantalum or electrolytic capacitor, with a value over 1 µF, should be placed in parallel with the MLCC.

##### 9.2.2.6.2 Selecting a VDDA (Bootstrap) Capacitor

A VDDA capacitor, also referred to as a *bootstrap capacitor* in bootstrap power supply configurations, allows for gate drive current transients up to 6 A, and needs to maintain a stable gate drive voltage for the power transistor.

The total charge needed per switching cycle can be estimated with

$$Q_{Total} = Q_G + \frac{I_{VDD}@100kHz(\text{No Load})}{f_{SW}} = 60nC + \frac{1.5mA}{100kHz} = 75nC \quad (19)$$

where

- $Q_G$: Gate charge of the power transistor.
- $I_{VDD}$: The channel self-current consumption with no load at 100kHz.

Therefore, the absolute minimum $C_{Boot}$ requirement is:

$$C_{Boot} = \frac{Q_{Total}}{\Delta V_{VDDA}} = \frac{75nC}{0.5V} = 150nF \quad (20)$$

where

- $\Delta V_{VDDA}$ is the voltage ripple at VDDA, which is 0.5 V in this example.

In practice, the value of $C_{Boot}$ is greater than the calculated value. This allows for the capacitance shift caused by the DC bias voltage and for situations where the power stage would otherwise skip pulses due to load transients. Therefore, it is recommended to include a safety-related margin in the $C_{Boot}$ value and place it as close to the VDD and VSS pins as possible. A 50-V 1-µF capacitor is chosen in this example.

$$C_{Boot} = 1\mu F \quad (21)$$

To further lower the AC impedance for a wide frequency range, it is recommended to have bypass capacitor with a low capacitance value, in this example a 100 nF, in parallel with $C_{Boot}$ to optimize the transient performance.

备注

Too large $C_{BOOT}$ is not good. $C_{BOOT}$ may not be charged within the first few cycles and $V_{BOOT}$ could stay below UVLO. As a result, the high-side FET does not follow input signal command. Also during initial $C_{BOOT}$ charging cycles, the bootstrap diode has highest reverse recovery current and losses.


Copyright © 2022 Texas Instruments Incorporated

#### 9.2.2.6.3 Select a VDDB Capacitor

Chanel B has the same current requirements as Channel A, Therefore, a VDDB capacitor (Shown as $C_{VDD}$ in 图 9-1) is needed. In this example with a bootstrap configuration, the VDDB capacitor will also supply current for VDDA through the bootstrap diode. A 50-V, 10-µF MLCC and a 50-V, 220-nF MLCC are chosen for $C_{VDD}$. If the bias power supply output is a relatively long distance from the VDDB pin, a tantalum or electrolytic capacitor, with a value over 10 µF, should be used in parallel with $C_{VDD}$.

### *9.2.2.7 Dead Time Setting Guidelines*

For power converter topologies utilizing half-bridges, the dead time setting between the top and bottom transistor is important for preventing shoot-through during dynamic switching.

The UCC20520 dead time specification in the electrical table is defined as the time interval from 90% of one channel’s falling edge to 10% of the other channel’s rising edge (see 图 7-4). This definition ensures that the dead time setting is independent of the load condition, and guarantees linearity through manufacture testing. However, this dead time setting may not reflect the dead time in the power converter system, since the dead time setting is dependent on the external gate drive turn-on/off resistor, DC-Link switching voltage/current, as well as the input capacitance of the load transistor.

Here is a suggestion on how to select an appropriate dead time for UCC20520:

$$DT_{Setting} = DT_{Req} + T_{F_Sys} + T_{R_Sys} - T_{D(on)} \tag{22}$$

where

- $DT_{setting}$: UCC20520 dead time setting in ns, $DT_{Setting}$ = 10 × RDT(in kΩ).
- $DT_{Req}$: System required dead time between the real $V_{GS}$ signal of the top and bottom switch with enough margin, or ZVS requirement.
- $T_{F_Sys}$: In-system gate turn-off falling time at worst case of load, voltage/current conditions.
- $T_{R_Sys}$: In-system gate turn-on rising time at worst case of load, voltage/current conditions.
- $T_{D(on)}$: Turn-on delay time, from 10% of the transistor gate signal to power transistor gate threshold.

In the example, $DT_{Setting}$ is set to 250 ns.

It should be noted that the UCC20520 dead time setting is decided by the DT pin configuration (See 节 8.4.2), and it cannot automatically fine-tune the dead time based on system conditions, i.e. zero voltage switching conditions. It is recommended to parallel a ceramic capacitor, 2.2nF or above, with $R_{DT}$ to achieve better noise immunity and deadtime matching.

Copyright © 2022 Texas Instruments Incorporated

### 9.2.2.8 Application Circuits with Output Stage Negative Bias

When parasitic inductances are introduced by non-ideal PCB layout and long package leads (e.g. TO-220 and TO-247 type packages), there could be ringing in the gate-source drive voltage of the power transistor during high di/dt and dv/dt switching. If the ringing is over the threshold voltage, there is the risk of unintended turn-on and even shoot-through. Applying a negative bias on the gate drive is a popular way to keep such ringing below the threshold. Below are a few examples of implementing negative gate drive bias.

图 9-2 shows the first example with negative bias turn-off on the channel-A driver using a Zener diode on the isolated power supply output stage. The negative bias is set by the Zener diode voltage. If the isolated power supply, $V_A$, is equal to 25 V, the turn-off voltage will be – 5.1 V and turn-on voltage will be 25 V - – 5.1 V ≈ 20 V. The channel-B driver circuit is the same as channel-A, therefore, this configuration needs two power supplies for a half-bridge configuration, and there will be steady state power consumption from $R_Z$.

### 9.2.2.9

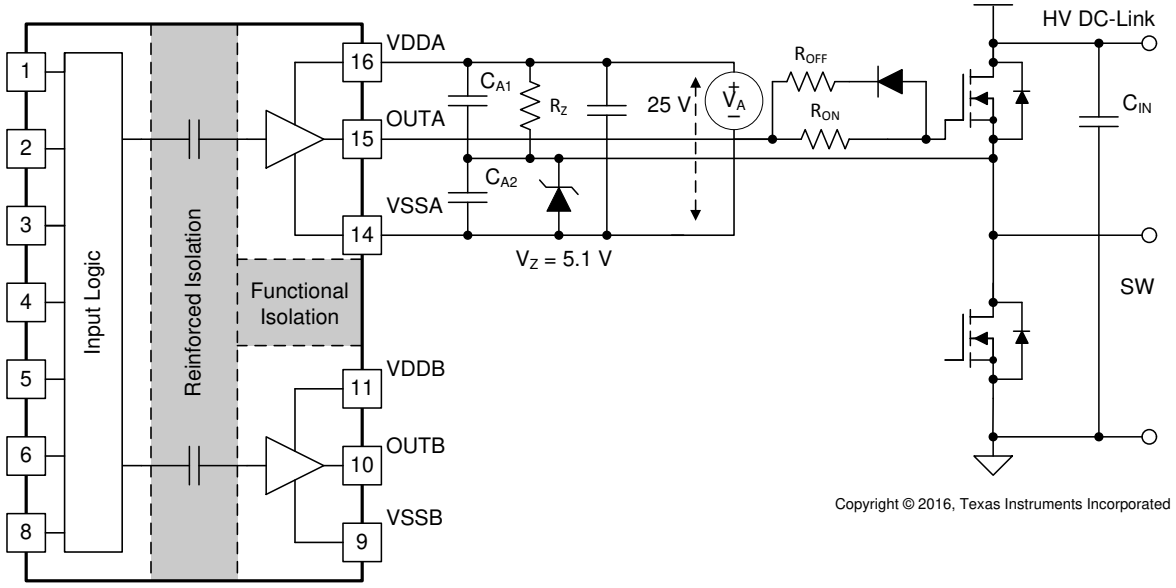



**图 9-2. Negative Bias with Zener Diode on Iso-Bias Power Supply Output**


Copyright © 2022 Texas Instruments Incorporated

图 9-3 shows another example which uses two supplies (or single-input-double-output power supply). Power supply $V_{A+}$ determines the positive drive output voltage and $V_{A-}$ determines the negative turn-off voltage. The configuration for channel B is the same as channel A. This solution requires more power supplies than the first example, however, it provides more flexibility when setting the positive and negative rail voltages.

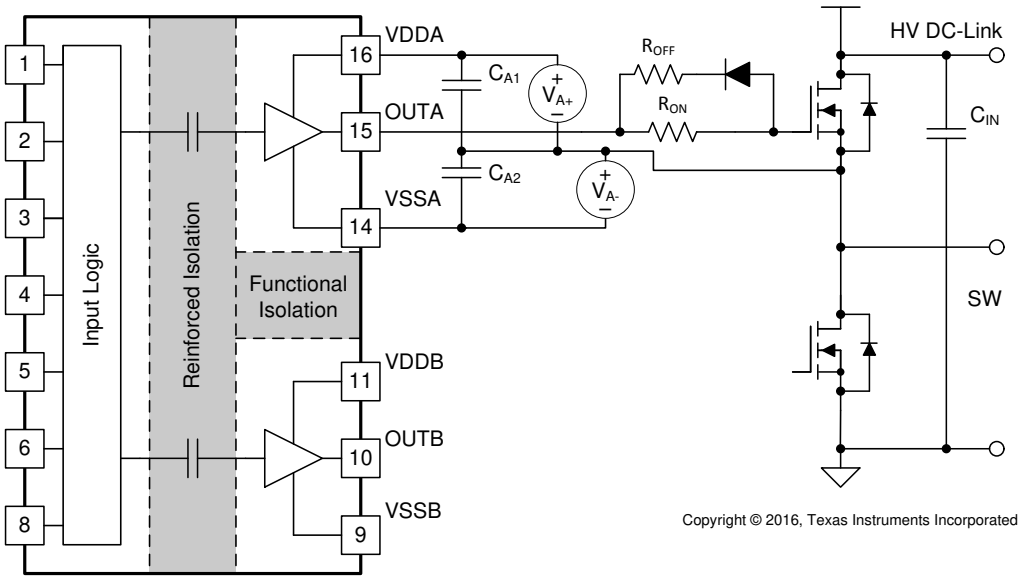



**图 9-3. Negative Bias with Two Iso-Bias Power Supplies**

The last example, shown in 图 9-4, is a single power supply configuration and generates negative bias through a Zener diode in the gate drive loop. The benefit of this solution is that it only uses one power supply and the bootstrap power supply can be used for the high side drive. This design requires the least cost and design effort among the three solutions. However, this solution has limitations:

1. The negative gate drive bias is not only determined by the Zener diode, but also by the duty cycle, which means the negative bias voltage will change when the duty cycle changes. Therefore, converters with a fixed duty cycle (~50%) such as variable frequency resonant convertors or phase shift convertors which favor this solution.
2. The high side VDDA-VSSA must maintain enough voltage to stay in the recommended power supply range, which means the low side switch must turn-on or have free-wheeling current on the body (or anti-parallel) diode for a certain period during each switching cycle to refresh the bootstrap capacitor. Therefore, a 100% duty cycle for the high side is not possible unless there is a dedicated power supply for the high side, like in the other two example circuits.

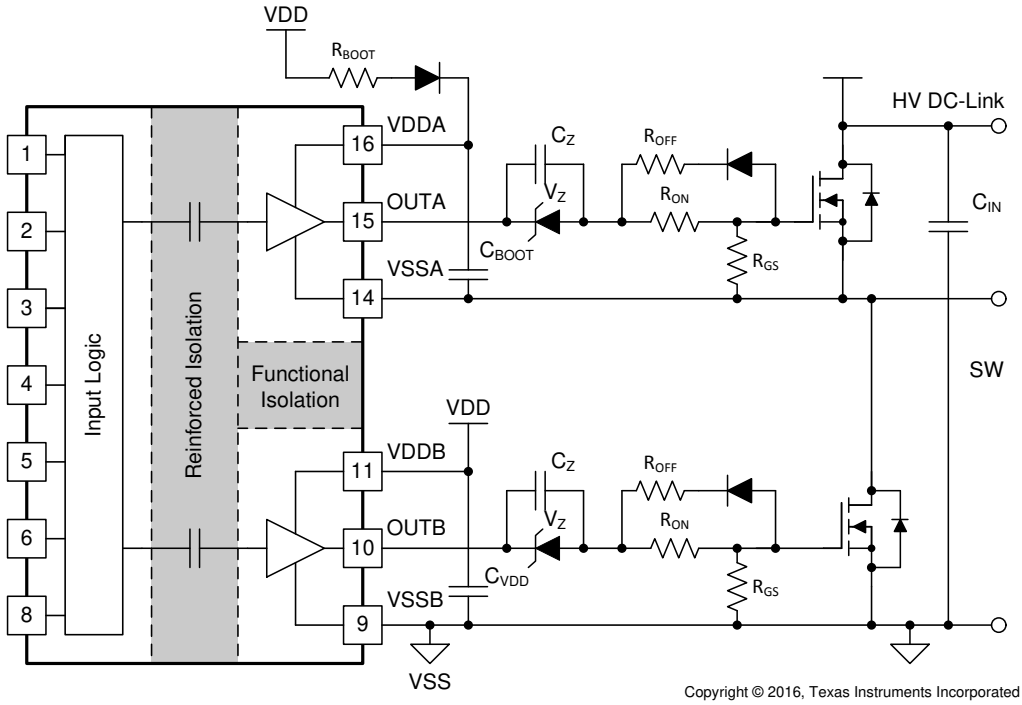



**图 9-4. Negative Bias with Single Power Supply and Zener Diode in Gate Drive Path**


Copyright © 2022 Texas Instruments Incorporated

### 9.2.3 Application Curves

图 9-5 and 图 9-6 shows the bench test waveforms for the design example shown in 图 9-1 under these conditions: VCC = 5 V, VDD = 20 V, $f_{SW}$ = 100 kHz, $V_{DC-Link}$ = 0 V.

**Channel 1 (Blue):** UCC20520 PWM pin signal.

**Channel 2 (Red):** Gate-source signal on the high side power transistor.

**Channel 3 (Green):** Gate-source signal on the low side power transistor.

In 图 9-5, PWM is sent with 50% duty-cycle signals. The gate drive signals on the power transistor have a 250-ns dead time, shown in the measurement section of 图 9-5.

图 9-6 shows a zoomed-in version of the waveform of 图 9-5, with measurements for propagation delay and rising/falling time. Cursors are also used to measure dead time. Importantly, the output waveform is measured between the power transistors' gate and source pins, and is not measured directly from the driver OUTA and OUTB pins. Due to the split on and off resistors ($R_{ON}$,$R_{OFF}$) and different sink and source currents, different rising (16 ns) and falling time (9 ns) are observed in 图 9-6.

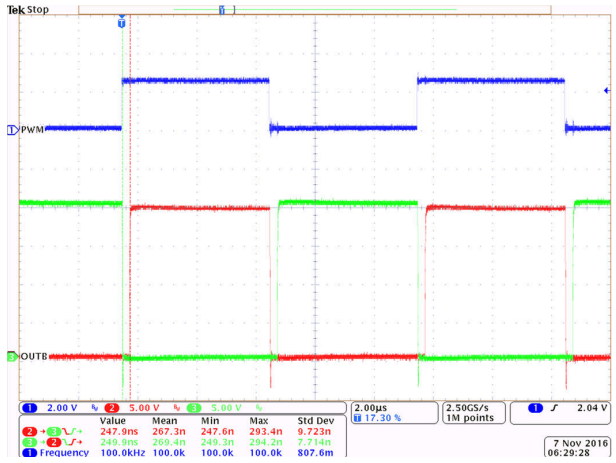



图 9-5. Bench Test Waveform for PWM and OUTA/B

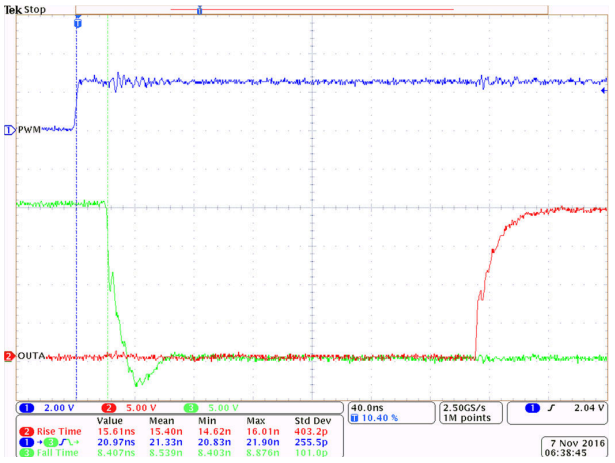



图 9-6. Zoomed-In bench-test waveform

Copyright © 2022 Texas Instruments Incorporated

## Power Supply Recommendations

The recommended input supply voltage (VCCI) for UCC20520 is between 3-V and 18-V. The recommended output bias supply voltage (VDDA/VDDB) range is between 9.2-V to 25-V. The lower end of this bias supply range is governed by the internal under voltage lockout (UVLO) protection feature of each device. One mustn't let VDD or VCCI fall below their respective UVLO thresholds (For more information on UVLO see 节 8.3.1). The upper end of the VDDA/VDDB range depends on the maximum gate voltage of the power device being driven by UCC20520.

A local bypass capacitor should be placed between the VDD and VSS pins. This capacitor should be positioned as close to the device as possible. A low ESR, ceramic surface mount capacitor is recommended. It is further suggested that one place two such capacitors: one with a value of between 220 nF and 10 µF for device biasing, and an additional 100-nF capacitor in parallel for high frequency filtering.

Similarly, a bypass capacitor should also be placed between the VCCI and GND pins. Given the small amount of current drawn by the logic circuitry within the input side of UCC20520, this bypass capacitor has a minimum recommended value of 100 nF.


Copyright © 2022 Texas Instruments Incorporated

# 10 Layout

## 10.1 Layout Guidelines

To achieve optimum performance for the UCC20520, pay close attention to PCB layout in order.

**Component Placement:**

- Low-ESR and low-ESL capacitors must be connected close to the device between the VCCI and GND pins and between the VDD and VSS pins to support high peak currents when turning on the external power transistor.
- To avoid large negative transients on the switch node VSSA (HS) pin, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.
- It is recommended to place the dead time setting resistor, $R_{DT}$, and its bypassing capacitor close to DT pin of UCC20520.

**Grounding Considerations:**

- It is essential to confine the high peak currents that charge and discharge the transistor gates to a minimal physical area. This will decrease the loop inductance and minimize noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- Pay attention to high current path that includes the bootstrap capacitor, bootstrap diode, local VSSB-referenced bypass capacitor, and the low-side transistor body/anti-parallel diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode by the VDD bypass capacitor. This recharging occurs in a short time interval and involves a high peak current. Minimizing this loop length and area on the circuit board is important for ensuring reliable operation.

**High-Voltage Considerations:**

- To ensure isolation performance between the primary and secondary side, one should avoid placing any PCB traces or copper below the driver device. A PCB cutout is recommended in order to prevent contamination that may compromise the UCC20520’s isolation performance.
- For half-bridge, or high-side/low-side configurations, where the channel A and channel B drivers could operate with a DC-link voltage up to 1500 $V_{DC}$, one should try to increase the creepage distance of the PCB layout between the high and low-side PCB traces.

**Thermal Considerations:**

- A large amount of power may be dissipated by the UCC20520 if the driving voltage is high, the load is heavy, or the switching frequency is high (Refer to 节 9.2.2.4 for more details). Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction to board thermal impedance ( $\theta_{JB}$).
- Increasing the PCB copper connecting to VDDA, VDDB, VSSA and VSSB pins is recommended (See 图 10-2 and 图 10-3). However, high voltage PCB considerations mentioned above must be maintained.
- If there are multiple layers in the system, it is also recommended to connect the VDDA, VDDB, VSSA and VSSB pins to internal ground or power planes through multiple vias of adequate size. However, keep in mind that there shouldn’t be any traces/coppers from different high voltage planes overlapping.

Copyright © 2022 Texas Instruments Incorporated

## 10.2 Layout Example

图 10-1 shows a 2-layer PCB layout example with the signals and key components labeled.

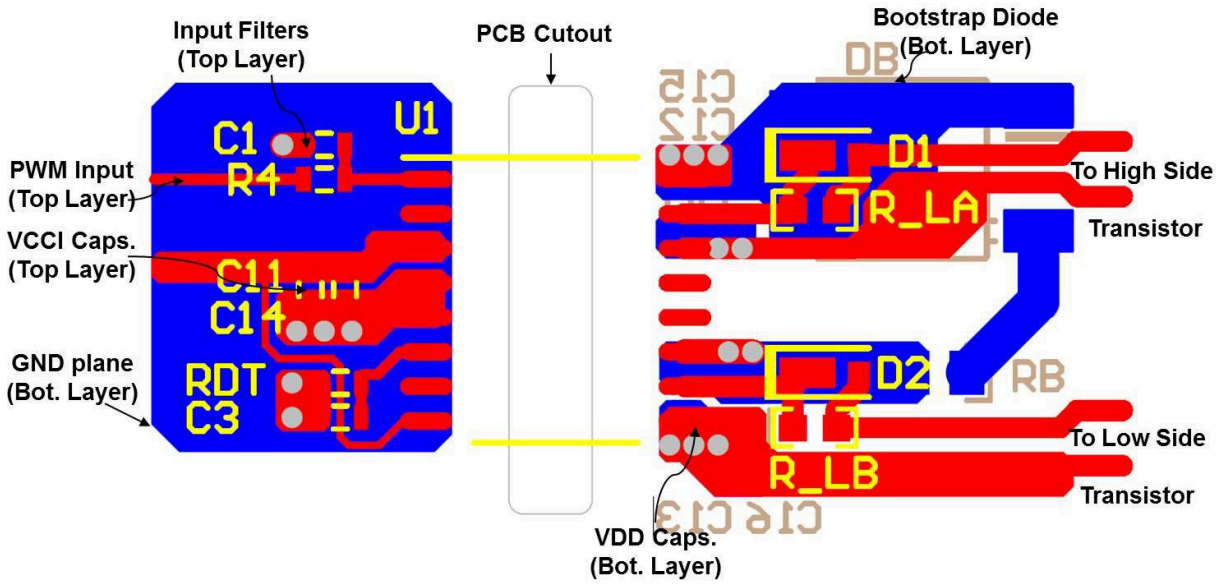



**图 10-1. Layout Example**

图 10-2 and 图 10-3 shows top and bottom layer traces and copper.

**备注**

There are no PCB traces or copper between the primary and secondary side, which ensures isolation performance.


Copyright © 2022 Texas Instruments Incorporated

PCB traces between the high-side and low-side gate drivers in the output stage are increased to maximize the creepage distance for high-voltage operation, which will also minimize cross-talk between the switching node VSSA (SW), where high dv/dt may exist, and the low-side gate drive due to the parasitic capacitance coupling.

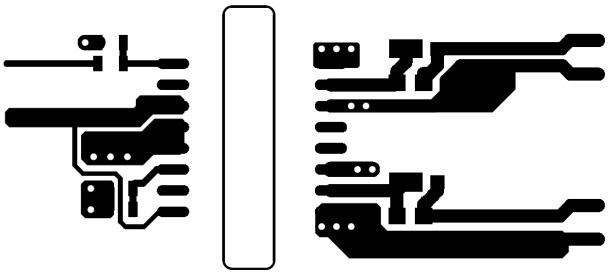


图 10-2. Top Layer Traces and Copper

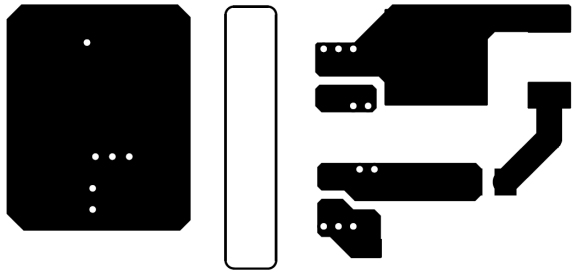


图 10-3. Bottom Layer Traces and Copper

图 10-4 and 图 10-5 are 3D layout pictures with top view and bottom views.

**备注**

The location of the PCB cutout between the primary side and secondary sides, which ensures isolation performance.

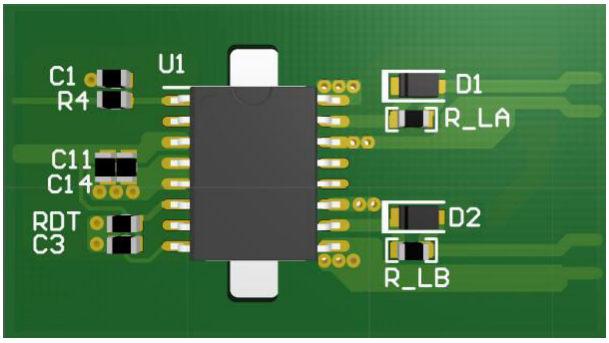



图 10-4. 3-D PCB Top View

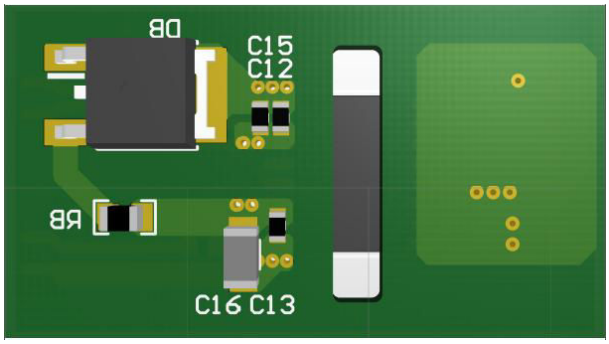



图 10-5. 3-D PCB Bottom View

# 11 Device and Documentation Support

## 11.1 Documentation Support

### 11.1.1 Related Documentation

For related documentation see the following:

- Isolation Glossary

## 11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

### 11.3.1 Certifications

UL Online Certifications Directory, *"FPPT2.E181974 Nonoptical Isolating Devices - Component"* Certificate Number: 20160516-E181974, (SLUQ001)

VDE Online Certifications Directory, *"Certificate of Conformity with Factory Surveillance"* Certificate Number: 40040142

CQC Online Certifications Directory, "GB4943.1-2011, Digital Isolator Certificate" Certificate Number: CQC16001155011

## 11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

## 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

# Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


Copyright © 2022 Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| UCC20520DW | Obsolete | Production | SOIC (DW) \| 16 | - | - | Call TI | Call TI | -40 to 125 | UCC20520 |
| UCC20520DWR | Active | Production | SOIC (DW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | UCC20520 |
| UCC20520DWR.A | Active | Production | SOIC (DW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | UCC20520 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# GENERIC PACKAGE VIEW

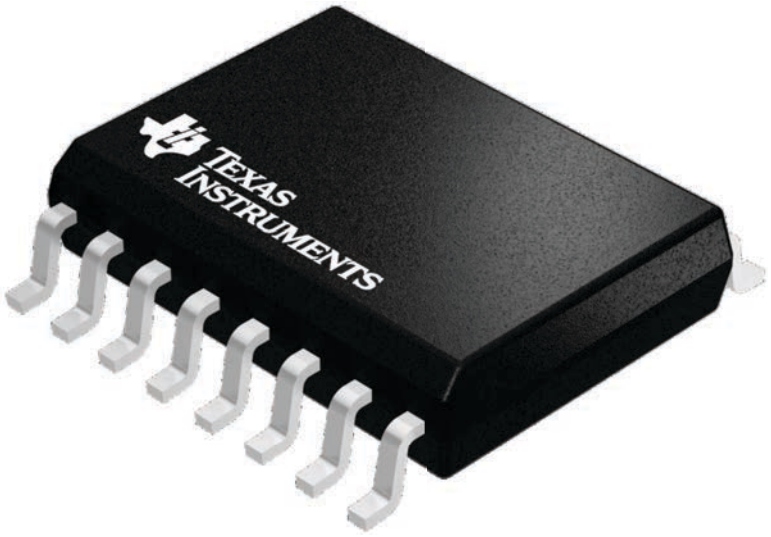
## DW 16

## SOIC - 2.65 mm max height

**7.5 x 10.3, 1.27 mm pitch**

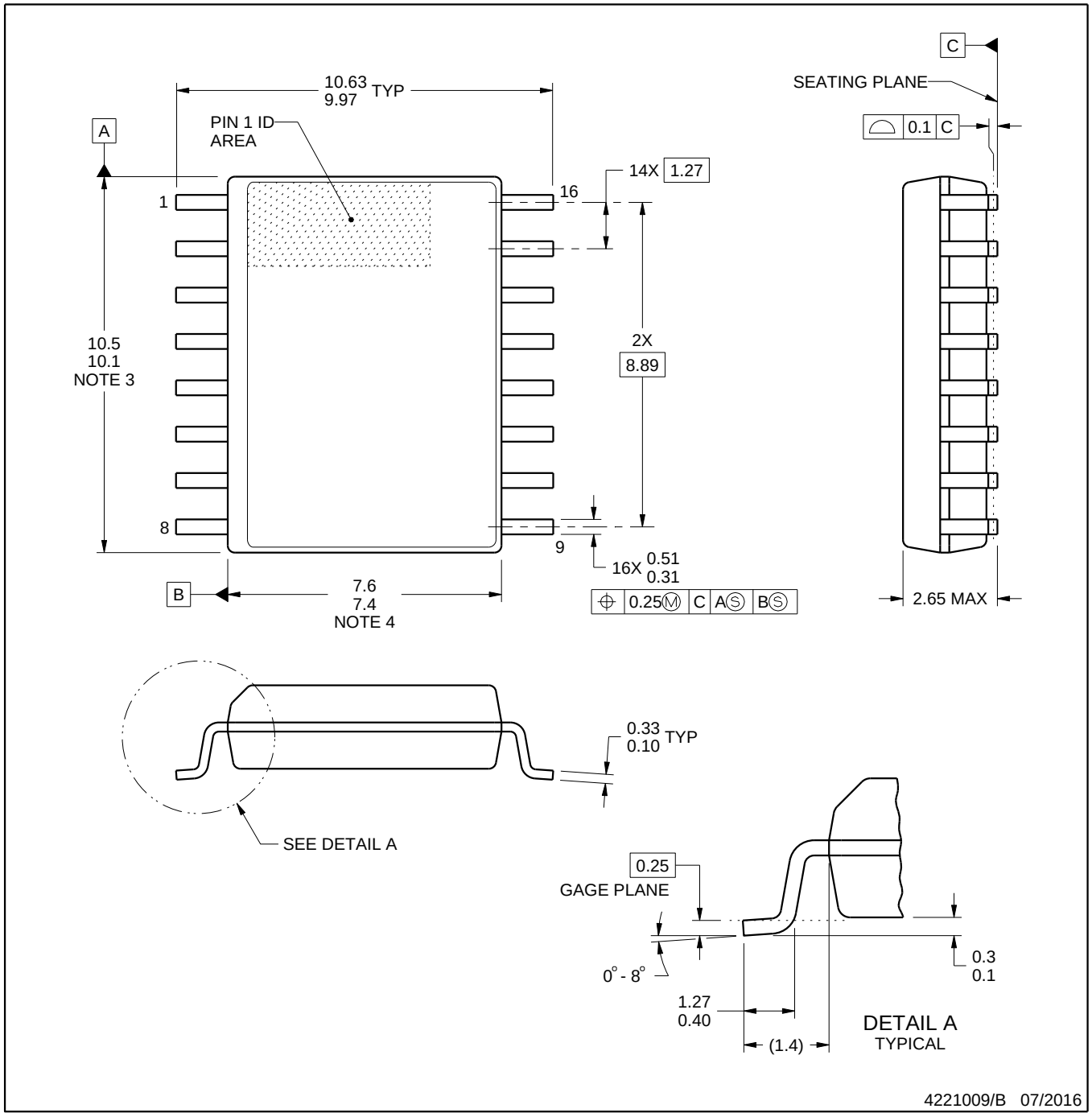
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



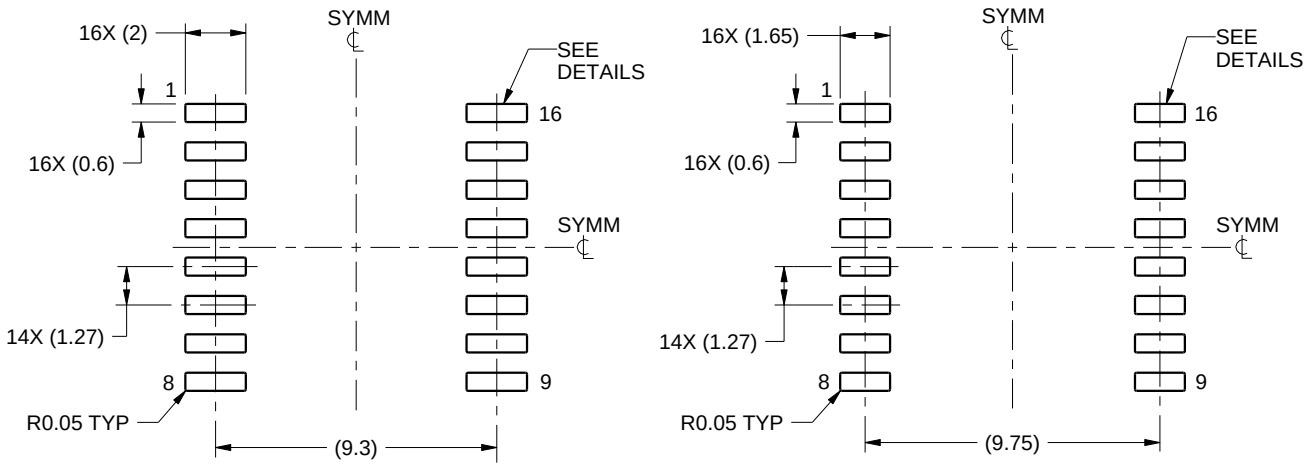

4224780/A

SOIC




NOTES:

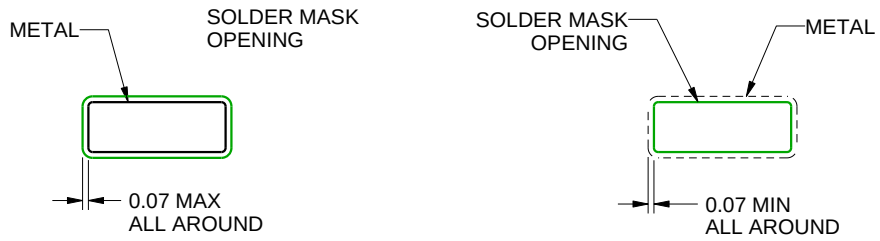
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.




IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X




NON SOLDER MASK DEFINED

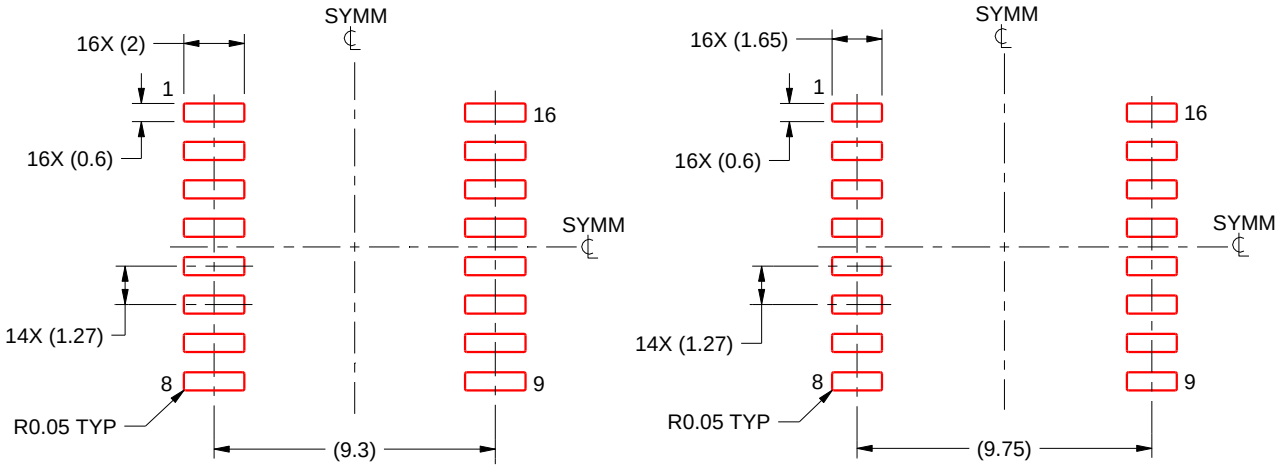
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# 重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2026，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月