抗辐射 V 类，移相谐振控制器

查询样片: UC1875-SP

特性

- 符合 **QML-V，SMD 5962-94555** 标准
- 抗辐射：**50kRad (Si)** 总电离辐射剂量 **(TID)** (1)
- 零到 **100%** 占空比控制
- 可编程输出接通延迟
- 与电压或者电流模式拓扑兼容
- 在**1MHz**开关频率下实际运行
- **4** 个 **2A** 推拉输出电路输出
- **10MHz**误差放大器
- 欠压闭锁
- 低启动电流 **- 150μA**
- 在欠压闭锁 **(UVLO)** 期间输出低电平有效
- 软启动控制
- 具有全周期重启动功能的闩锁过流比较器
- 可调基准

(1) 抗辐射是基于初始器件限定剂量率 = 10mrad/s 的一个典型值，并且被施加到 5962-9455502 器件。 提供辐射批次验收测试 — 联系工厂了解详细信息。

应用范围

- 电源现场可编程门阵列 **(FPGA)**

说明

UC1875-SP 根据另外一个半桥，通过一个半桥上的相位移动来控制一个桥电源级，在高频率下，为了获得高效性能，允许持续频率脉宽调制与谐振，零电压开关相组合。 此电路可被配置为在电压或者电源模式下提供控制功能，此分离的过流关断以实现快速故障保护。

提供一个可编程时间延迟，在每个输出级接通时插入一个死区时间。 此延迟，为谐振开关动作提供了时间，并可被每个输出对 (A-B，C-D) 单独控制。

借助于工作频率超过 2MHz 的振荡器，实际总开关频率可达到 1MHz。
除了标准自由模式，通过使用时钟同步 (CLOCLSYNC) 引脚，用户可以配置这些器件以接收一个外部时钟同步信号，或者也可以在最快器件决定的运行频率上锁定最多 5 个单位。.

保护特性包括一个欠压闭锁，此特性将所有输出保持在一个低电平有效的状态直到电源达到 10.75V 的阀值。为了获得可靠、自举芯片电源，内置 1.5 滞后。 还提供过载保护功能，在故障时，将会在 70ns 内把此输出锁定在关闭 (OFF) 状态。 此电流故障电路执行满周期重启操作。

额外的特性包括一个带宽超过 7MHz 的误差放大器，一个 5V 基准，提供软启动，和灵活的斜坡生成和斜率补偿电路。

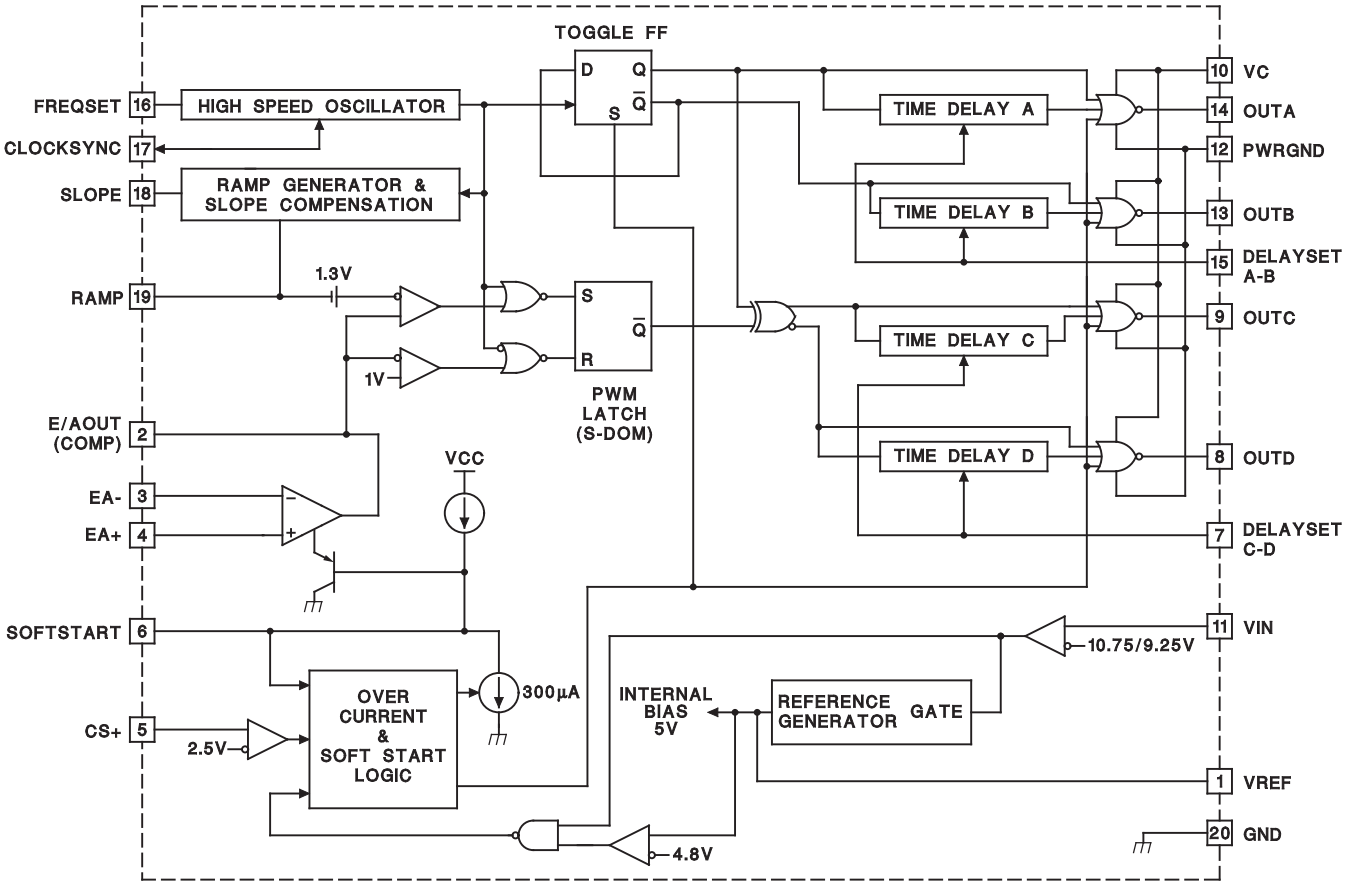
此器件采用玻璃密封陶瓷双列直插式，表面贴装，和陶瓷无引线芯片载体封装，额定温度范围 -55°C 至 +125°C。

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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方框图



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	CDIP (J)	5962-9455501VRA	5962-9455501VRA
		5962-9455502VRA	5962-9455502VRA
	LCCC (FK)	5962-9455501V3A	5962-9455501V3A
	CFP (W)	5962-9455502VKA	5962-9455502VKA

ABSOLUTE MAXIMUM RATINGS(1)

PARAMETER	VALUE		UNIT
	MIN	MAX	
Supply voltage (VC, VIN)		20	V
Output current, source or sink			
DC		0.5	A
Pulse (0.5 µs)		3	A
Analog inputs			
(Pins 1, 2, 3, 4, 5, 6, 7, 15, 16, 17, 18, 19)	–0.3	5.3	V
Storage temperature range	–65	150	°C
Maximum junction temperature, J_{Tmax}		150	
Thermal Resistance T_{JC}			
J package		7	°C/W
W package		5.4	
FK package		5.6	

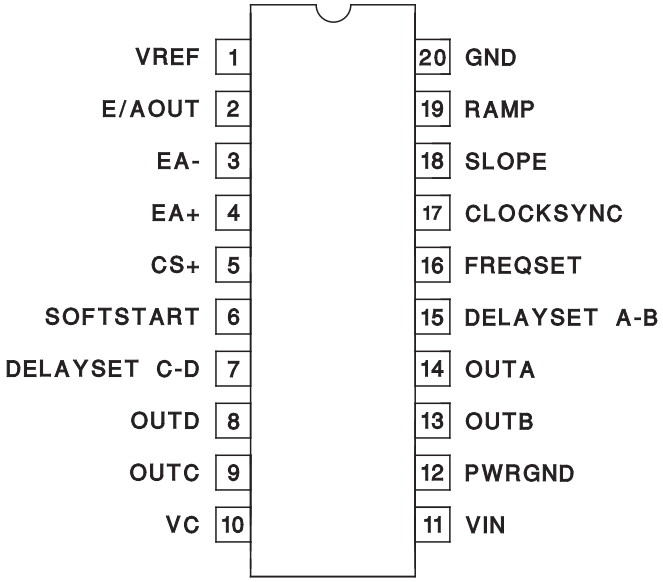
(1) Pin references are to 20-pin packages. All voltages are with respect to ground. Currents are positive into, negative out of the device terminals.

DEVICE INFORMATION

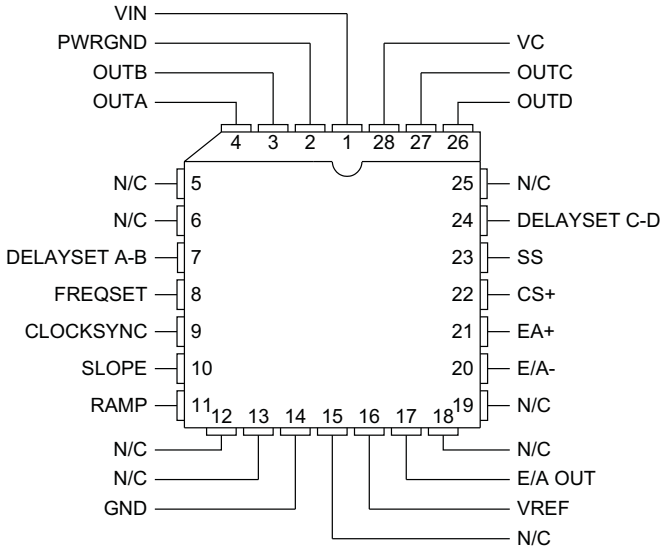
	UVLO Turn-On	UVLO Turn-Off	Delay Set
UCC1875-SP	10.75V	9.25V	Yes

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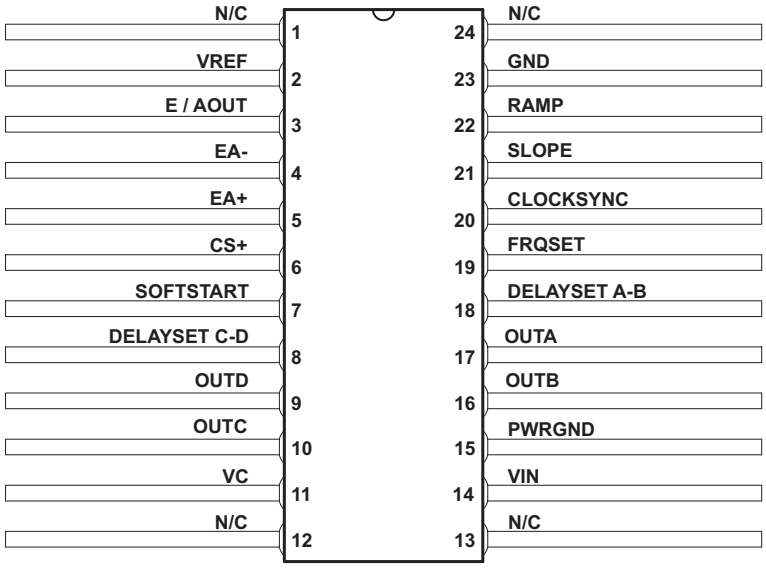
DIL - 20 Pin
J Package
(TOP VIEW)



LCCC - 28 Pin
FK Package
(TOP VIEW)



CFP - 24 Pin
W Package
(TOP VIEW)



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ELECTRICAL CHARACTERISTICS

–55°C < T_A < 125°C. VC = VIN = 12 V, $R_{(FREQSET)}$ = 12 kΩ, $C_{(FREQSET)}$ = 330 pF, $R_{(SLOPE)}$ = 12 kΩ, $C_{(RAMP)}$ = 200 pF, $C_{(DELAYSET\ A-B)}$ = $C_{(DELAYSET\ C-D)}$ = 0.01 µF, $I_{(DELAYSET\ A-B)}$ = $I_{(DELAYSET\ C-D)}$ = –500 µA, T_A = T_J, unless otherwises stated.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Undervoltage Lockout						
Start threshold				10.75	11.75	V
UVLO hysteresis			0.5	1.25	2	V
Supply Current						
I_{IN} Startup	VIN = 8 V, VC = 20 V, $R_{(SLOPE)}$ open, $I_{(DELAY)}$ = 0			150	600	µA
I_C Startup	VIN = 8 V, VC = 20 V, $R_{(SLOPE)}$ open, $I_{(DELAY)}$ = 0			10	100	µA
I_{IN}				30	44	mA
I_C				15	30	mA
Voltage Reference						
Output voltage	T_J = 25°C		4.92	5	5.08	V
Line regulation	11 V < VIN < 20 V			1	10	mV
Load regulation	I_{VREF} = –10 mA			5	20	mV
Total variation	Line, Load, Temperature		4.9		5.1	V
Noise Voltage	10 Hz to 10 kHz			50		µVrms
Long Term Stability	T_J = 125°C, 1000 hours			2.5		mV
Short circuit current	VREF = 0 V, T_J = 25°C			60		mA
Error Amplifier						
Offset voltage				5	15	mV
Input bias current				0.6	3	µA
AVOL	1 V < $V_{(E/AOUT)}$ < 4 V		60	90		dB
CMMR	1.5 V < V_{CM} < 5.5 V		75	95		dB
PSRR	11 V < VIN < 20 V		85	100		dB
Output sink current	$V_{(E/AOUT)}$ = 1 V		1	2.5		mA
Output source current	$I_{(E/AOUT)}$ = 4 V			–1.3	–0.5	mA
Output voltage high	$I_{(E/AOUT)}$ = –0.5 mA		4	4.7	5	V
Output voltage low	$I_{(E/AOUT)}$ = 1 mA		0	0.5	1	V
Unity Gain BW	See (1)	01 device	5			MHz
		02 device	7			MHz
Slew rate	See (1)		6	11		V/µsec
PWM Comparator						
RAMP offset voltage	T_J = 25°C (2)			1.3		V
Zero phase shift voltage	See (3)		0.55	0.9		V
PWM phase shift (4) (5)	$V_{(E/AOUT)}$ > (Ramp Peak + Ramp Offset)	01 device	98	99.5	102	%
		02 device	96	100	104	%
	$V_{(E/AOUT)}$ < Zero Phase Shift Voltage		0	0.5	2	%
Output skew (4) (5)	$V_{(E/AOUT)}$ > 1 V			5	±20	nsec
Ramp to output delay (6) (1)				65	125	nsec

(1) Not production tested.
(2) Ramp offset voltage has a temperature coefficient of about –4 mV/°C.
(3) The zero phase shift voltage has a temperature coefficient of about –2 mV/°C.

(4) Phase shift percentage (0% = 0 , 100% = 180) is defined as $\theta = \frac{200}{T}\phi\%$ where is the phase shift, and and T are defined in Figure 1. At 0% phase shift, is the output skew.
(5) Not production tested at –55·C.
(6) Ramp delay to output time is defined in Figure 1

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ELECTRICAL CHARACTERISTICS (continued)

–55°C < T_A < 125°C. VC = VIN = 12 V, $R_{(FREQSET)}$ = 12 kΩ, $C_{(FREQSET)}$ = 330 pF, $R_{(SLOPE)}$ = 12 kΩ, $C_{(RAMP)}$ = 200 pF, $C_{(DELAYSET\ A-B)}$ = $C_{(DELAYSET\ C-D)}$ = 0.01 µF, $I_{(DELAYSET\ A-B)}$ = $I_{(DELAYSET\ C-D)}$ = –500 µA, T_A = T_J, unless otherwises stated.

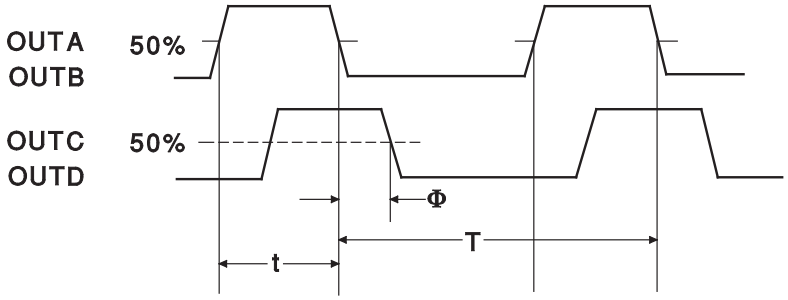
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Oscillator						
Initial accuracy	T_A = 25°C	01 device	0.85	1	1.15	MHz
		02 device	0.85	1	1.19	
Voltage stability	11 V < VIN < 20 V			0.2	2	%
Total variation	Line, Temperature		0.8		1.2	MHz
Sync pin threshold	T_J = 25°C			3.8		V
Clock out peak	T_J = 25°C			4.3		
Clock out low	T_J = 25°C			3.3		
Clock out pulse width	$R_{(CLOCKSYNC)}$ = 3.9 kΩ			30	100	nsec
Maximum frequency (7)	$R_{(FREQUEST)}$ = 5 kΩ		2			MHz
Ramp Generator/Slope Compensation						
Ramp current, minimum	$I_{(SLOPE)}$ = 10 µA, $V_{(FREQSET)}$ = VREF			–11	–14	µA
Ramp current, maximum	$I_{(SLOPE)}$ = 1 mA, $V_{(FREQSET)}$ = VREF		–0.8	–0.95		mA
Ramp valley				0		V
Ramp peak - clamping level	$R_{(FREQSET)}$ = 100 kΩ		3.8	4.1	5	V
Current Limit						
Input bias	V_{CS+} = 3 V			2	5	µA
Threshold voltage			2.4	2.5	2.6	V
Delay to output (8)				85	150	nsec
Soft Start/Reset Delay						
Charge current	$V_{(SOFTSTART)}$ = 0.5 V		–20	–9	–3	µA
Discharge current	$V_{(SOFTSTART)}$ = 1 V		120	230		
Restart threshold			4.3	4.7		V
Discharge level				300		mV
Output Drivers						
Output low level	I_{OUT} = 50 mA			0.2	0.4	V
Output high level	I_{OUT} = –50 mA			1.5	2.5	
Delay Set						
Delay set voltage	$I_{(DELAY)}$ = –500 µA		2.3	2.4	2.6	V
Delay time (8)	$I_{(DELAY)}$ = –250 µA (9)		150	250	600	nsec

(7) Not production tested at –55·C.
(8) Not production tested.

(9) Delay time can be programmed via resistors from the delay set pins to ground. Delay time = $\frac{62.5 \times 10^{-12}}{I_{(DELAY)}}$.

Where $I_{(DELAY)} = \frac{\text{Delay set voltage}}{R_{(DELAY)}}$. The Recommended range for $I_{(DELAY)}$ is 25 µA ≤ $I_{(DELAY)}$ ≤ 1 mA.

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Duty Cycle = t/T, Period = T

T_{DHL} (A to C) = T_{DHL} (B to D) = Φ

Figure 1. Phase Shift, Output Skew and Delay Time Definitions

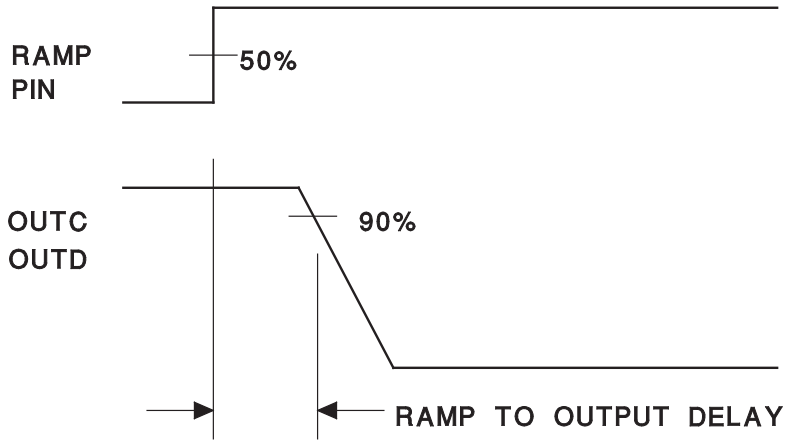


Figure 2. Ramp to Delay Output

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PIN DESCRIPTIONS

CLKSYNC (bi-directional clock and synchronization pin): Used as an output, this pin provides a clock signal. As an input, this pin provides a synchronization point. In its simplest usage, multiple devices, each with their own local oscillator frequency, may be connected together by the CLOCKSYNC pin and will synchronize on the fastest oscillator. This pin may also be used to synchronize the device to an external clock, provided the external signal is of higher frequency than the local oscillator. A resistor load may be needed on this pin to minimize the clock pulse width.

E/AOUT (Error Amplifier Output): This is is the gain stage for overall feedback control. Error amplifier output voltage levels below 1 volt will force 0° phase shift. Since the error amplifier has a relatively low current drive capability, the output may be overridden by driving with a sufficiently low impedance source.

CS+ (Current Sense): The non-inverting input to the current-fault comparator whose reference is set internally to a fixed 2.5 V (separate from VREF). When the voltage at this pin exceeds 2.5 V the current-fault latch is set, the outputs are forced OFF and a SOFT-START cycle is initiated. If a constant voltage above 2.5 V is applied to this pin the outputs are disabled from switching and held in a low state until the CS+ pin is brought below 2.5 V. The outputs may begin switching at 0 degrees phase shift before the SOFTSTART pin begins to rise -- this condition will not prematurely deliver power to the load.

FREQSET (Oscillator Frequency Set pin): A resistor and a capacitor from FREQSET to GND will set the oscillator frequency.

DELSETA-B, DELSETC-D (Output Delay Control): The user programmed current flowing from these pins to GND set the turn-on delay for the corresponding output pair. This delay is introduced between turn-off of one switch and turn-on of another in the same leg of the bridge to provide a dead time in which the resonant switching of the external power switches takes place. Separate delays are provided for the two half-bridges to accommodate differences in the resonant capacitor charging currents.

EA– (Error Amplifier Inverting Input): This is normally connected to the voltage divider resistors which sense the power supply output voltage level.

EA+ (Error Amplifier Non-Inverting Input): This is normally connected to a reference voltage used for comparison with the sensed power supply output voltage level at the EA+ pin.

GND (Signal Ground): All voltages are measured with respect to GND. The timing capacitor, on the FREQSET pin, any bypass capacitor on the VREF pin, bypass capacitors on VIN and the ramp capacitor, on the RAMP pin, should be connected directly to the ground plane near the signal ground pin.

OUTA – OUTD (Outputs A-D): The outputs are 2 A totem-pole drivers optimized for both MOSFET gates and level-shifting transformers. The outputs operate as pairs with a nominal 50% duty-cycle. The A-B pair is intended to drive one half-bridge in the external power stage and is syncronized with the clock waveform. The C-D pair will drive the other half-bridge with switching phase shifted with respect to the A-B outputs.

PWRGND (Power Ground): VC should be bypassed with a ceramic capacitor from the VC pin to the section of the ground plane that is connected to PWRGND. Any required bulk reservoir capacitor should parallel this one. Power ground and signal ground may be joined at a single point to optimize noise rejection and minimize DC drops.

RAMP (Voltage Ramp): This pin is the input to the PWM comparator. Connect a capacitor from here to GND. A voltage ramp is developed at this pin with a slope:

$$\frac{dV}{dT} = \frac{\text{Sense Voltage}}{R_{(SLOPE)} \times C_{(RAMP)}}$$

Current mode control may be achieved with a minimum amount of external circuitry, in which case this pin provides slope compensation.

Because of the 1.3 V offset between the ramp input and the PWM comparator, the error amplifier output voltage can not exceed the effective ramp peak voltage and duty cycle clamping is easily achievable with appropriate values of $R_{(SLOPE)}$ and $C_{(RAMP)}$.

SLOPE (Set Ramp Slope/Slope Compensation): A resistor from this pin to VCC will set the current used to generate the ramp. Connecting this resistor to the DC input line voltage will provide voltage feed-forward.

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SOFTSTART:(soft start): SOFTSTART will remain at GND as long as VIN is below the UVLO threshold. SOFTSTART will be pulled up to about 4.8 V by an internal 9 µA current source when VIN becomes valid (assuming a non-fault condition). In the event of a current-fault (CS+ voltage exceeding 2.5 V), SOFTSTART will be pulled to GND and them ramp to 4.8 V. If a fault occurs during the SOFTSTART cycle, the outputs will be immediately disabled and SOFTSTART must charge fully prior to resetting the fault latch.

For paralleled controllers, the SOFTSTART pins may be paralled to a single capacitor, but the charge currents will be additive.

VC (Output Switch Supply Voltage): This pin supplies power to the output drivers and their associated bias circuitry. Connect VC to a stable source above 3 V for normal operation, above 12 V for best performance. This supply should be bypassed directly to the PWRGND pin with low ESR, low ESL capacitors

VIN (Primary Chip Supply Voltage): This pin supplies power to the logic and analog circuitry on the integrated circuit that is not directly associated with driving the output stages. Connect VIN to a stable source above 12 V for normal operation. To ensure proper chip functionality, these devices will be inactive until VIN exceeds the upper undervoltage lockout threshold. This pin should by bypassed directly to the GND pin with low ESR, low ESL capacitors.

NOTE

When VIN exceeds the UVLO threshold the supply current (I_{IN}) will jump from about 100 µA to a current in excess of 20 µA. If the UC1875-SP is not connected to a well bypassed supply, it may immediately enter UVLO again.

VREF: This pin is an accurate 5 V voltage reference. This output is capable of delivering about 60 mA to peripheral circuitry and is internally short circuit current limited. VREF is disabled while VIN is low enough to force the chip into UVLO. The circuit is also in UVLO until VREF reaches approximately 4.75 V. For best results bypass VREF with a 0.1 µF, low ESR, low ESL, capacitor to the GND pin.

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APPLICATION INFORMATION

Undervoltage Lockout Section

When power is applied to the circuit and VIN is below the upper UVLO threshold, I_{IN} will be below 600 µA, the reference generator will be off, the fault latch is reset, the soft-start pin is discharged, and the outputs are actively held low. When VIN exceeds the upper UVLO threshold, the reference generator turns on. All else remains in the shut-down mode until the output of the reference, VREF, exceeds 4.75 V.

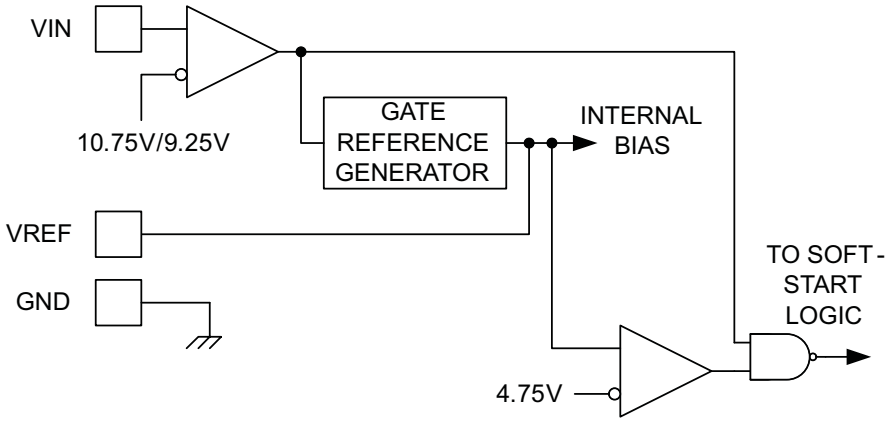
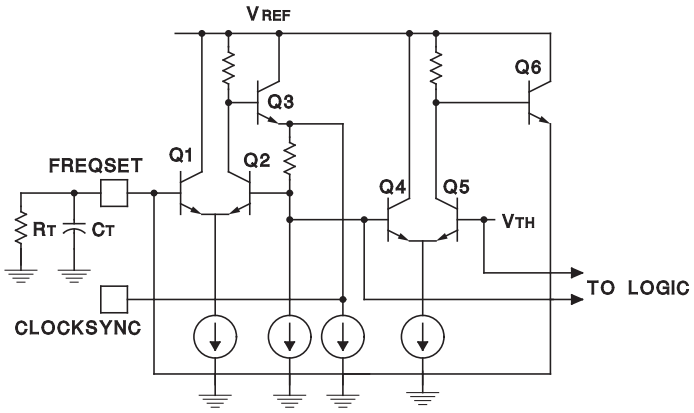
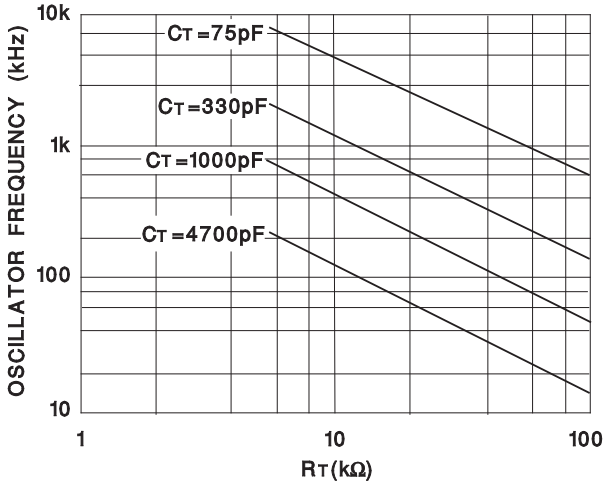


Figure 3. Undervoltage Circuit

The high frequency oscillator may be either free-running or externally synchronized. For free-running operation, the frequency is set via an external resistor and capacitor to ground from the FREQSET pin.





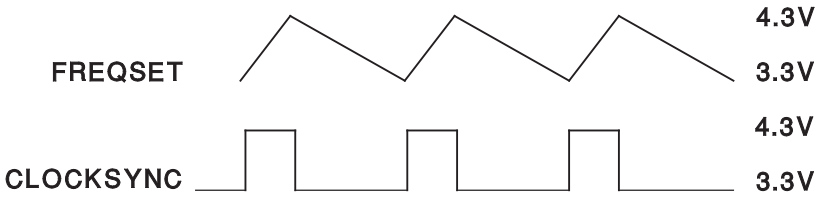


Figure 4. Simplified Oscillator Schematic

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Synchronizing The Oscillator

The CLOCKSYNC pin of the oscillator may be used to synchronize multiple UC1875-SP device by connecting the CLOCKSYNC of each UC1875-SP to the others:

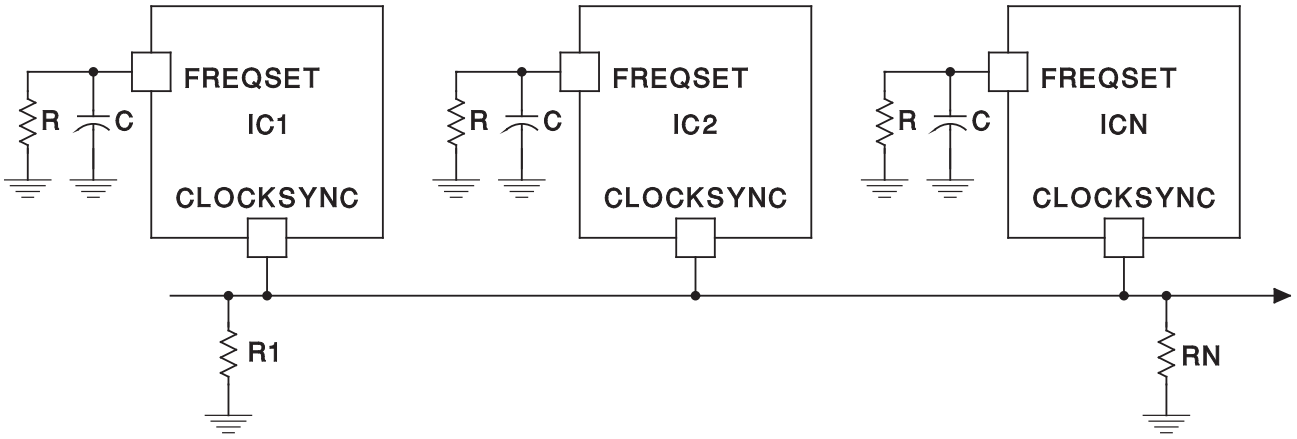


Figure 5.

ALL ICs will sync to the chip with the fastest local oscillator.

R1 and RN may be needed to keep sync pulse narrow due to capacitance on line.

R1 and RN may also be needed to properly terminate $R_{(SYNC)}$ line.

Syncing to External TTL/CMOS

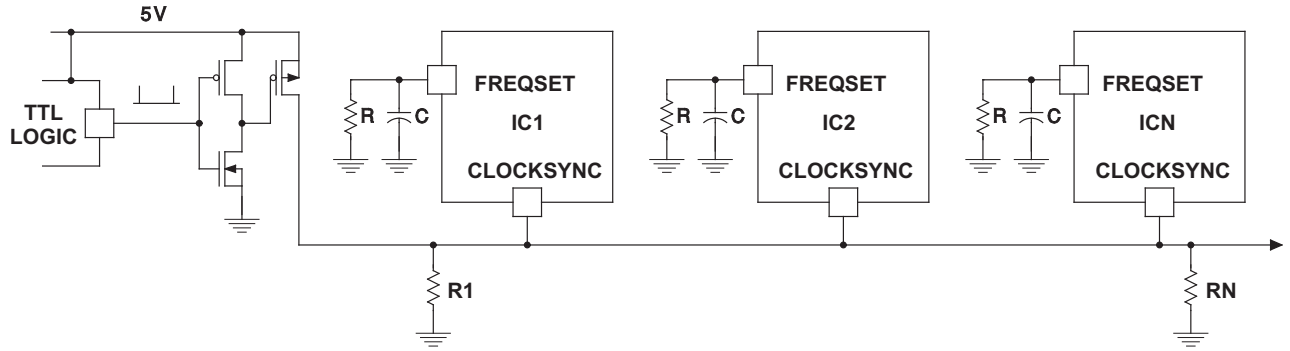


Figure 6.

ICs will sync to the fastest chip or TTL clock if it is higher frequency.

R1 and RN may be needed to keep sync pulse narrow due to capacitance on line.

R1 and RN may also be needed to properly terminate $R_{(SYNC)}$ line.

Although the UC1875-SP has a local oscillator frequency, the device will synchronize to the fastest oscillator driving the CLOCKSYNC pin. This arrangement allows the synchronizing connection between ICs to be broken without any local loss of functionality.

Synchronizing the device to an external clock signal may be accomplished with a minimum of external circuitry, as shown in Figure 6.

Capacitive loading on the CLOCKSYNC pin will increase the clock pulse width, and may adversely effect system performance. Therefore, a resistor to ground from the CLOCKSYNC pin is optional, but may be required to offset capacitive loading on this pin. These resistors are shown in the oscillator schematics as R1, RN.

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Delay Blocks and Output Stages

In each of the output stages, transistors Q3 through Q6 form a high-speed totem-pole driver which will source or sink more than one amp peak with a total delay of approximately 30 nanoseconds. To ensure a low output level prior to turn-on, transistors Q7 through Q9 form a self-biased driver to hold Q6 on prior to the supply reaching its turn-on threshold. This circuit is operable when the chip supply is zero. Q6 is also turned on and held low with a signal from the fault logic portion of the chip.

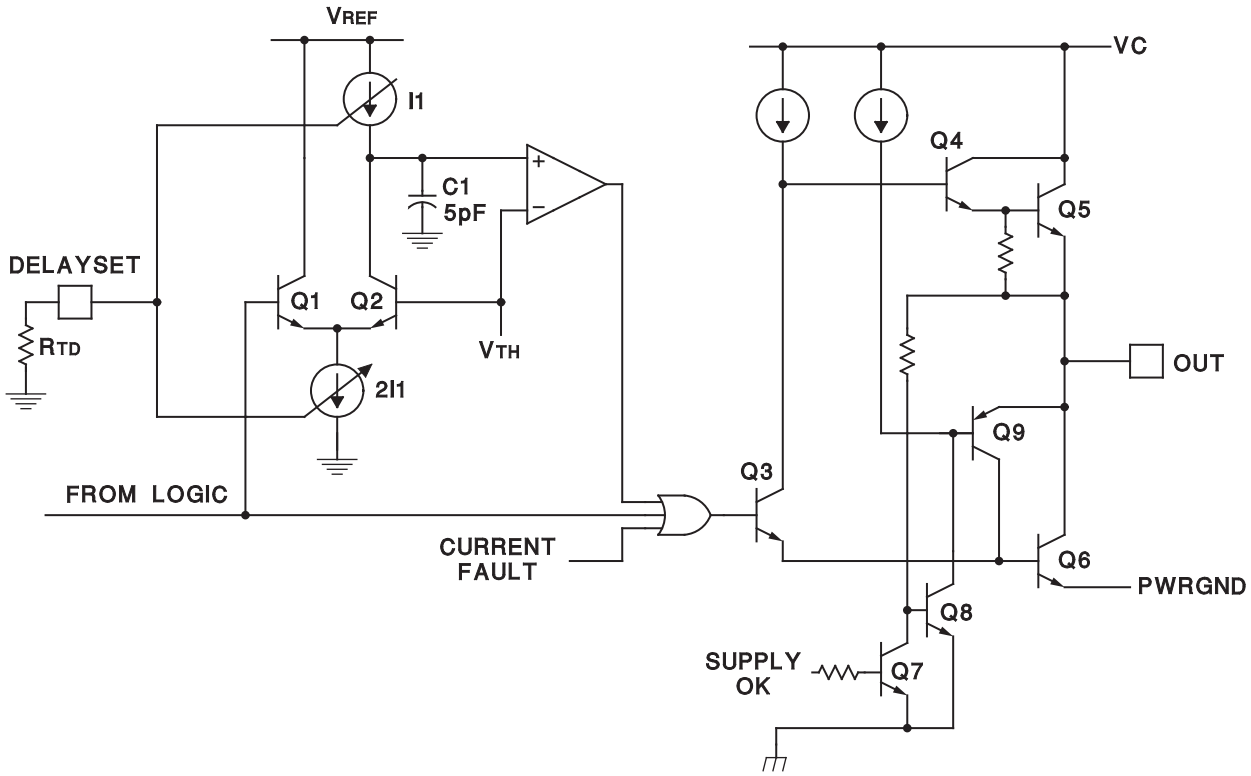


Figure 7.

The delay providing the dead-time is accomplished with C1 which must discharge to V_{TH} before the output can go high. The time is defined by the current sources, I1, which is programmed by an external resistor, R_{TD}. The voltage on the Delay Set pins is internally regulated to 2.5 V and the range of dead time control is from 50 to 200 nanoseconds.

NOTE

There is no way to disable the delay circuitry, and the delay time must be programmed.

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Output Switch Orientation

The four outputs of the UC1875-SP interfaces to the full bridge converter switches as shown in Figure 8

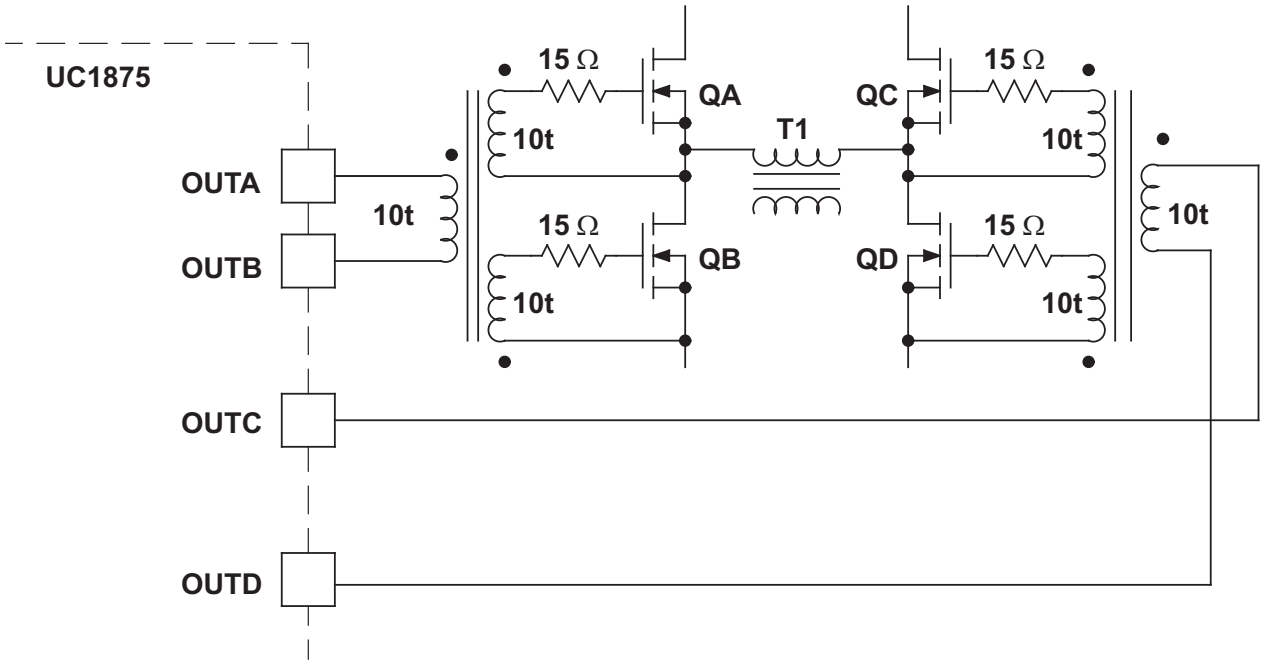


Figure 8. 3 Winding Bifilar, AWG 30 Kynar Insulation

Fault/SoftStart

The fault control circuitry provides two forms of power shutdown:

- Complete turn-off of all four output power stages.
- Clamping the phase shift command to zero.

Complete turn-off is ordered for an over-current fault or a low supply voltage. When the SOFTSTART pin reaches its low threshold, switching is allowed to proceed while the phase-shift is advanced from zero to its nominal value with the time constant of the SOFT-START capacitor.

The fault logic insures that a continuous fault will institute a low frequency “hiccup” retry cycle by forcing the SOFT-START capacitor to charge through its full cycle between each restart attempt.

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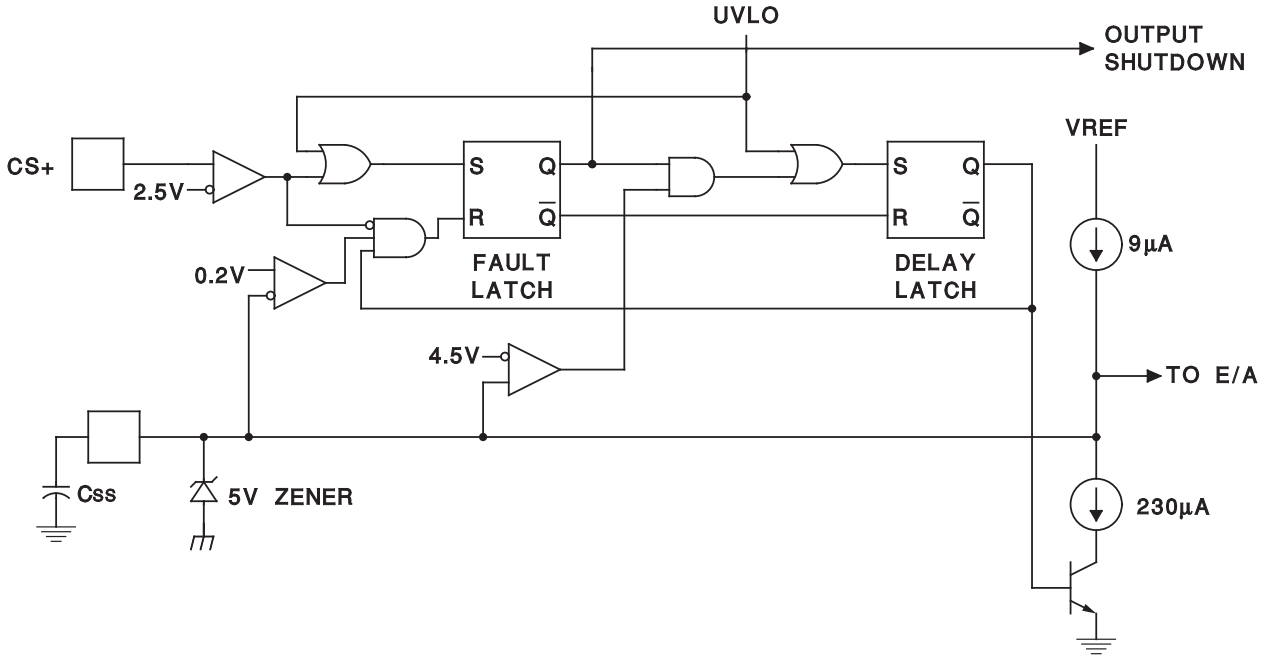


Figure 9.

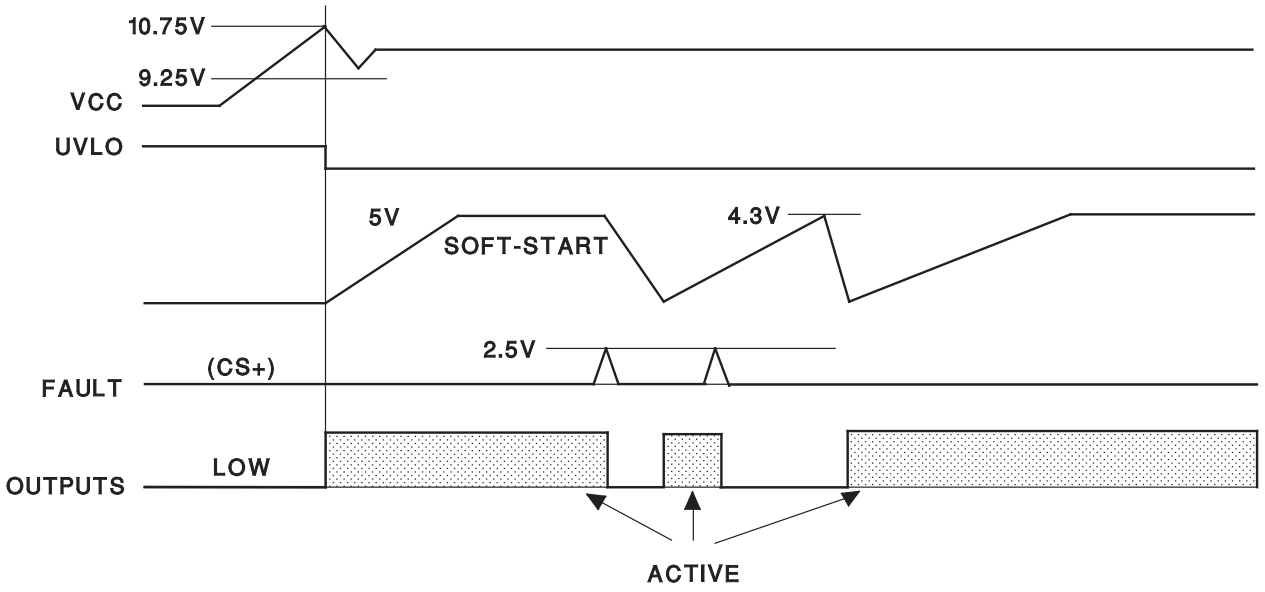


Figure 10.

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Slope/Ramp Pins

The ramp generator may be configured for the following control methods:

- Voltage Mode
- Voltage Feedforward
- Current Mode
- Current Mode with Slope Compensation

Figure 11 shows a voltage-mode configuration. With $R_{(SLOPE)}$ tied to a stable voltage source, the waveform on $C_{(RAMP)}$ will be a constant-slope ramp, providing conventional voltage-mode control. If $R_{(SLOPE)}$ is connected to the power supply input voltage, a variable-slope ramp will provide voltage feedforward.

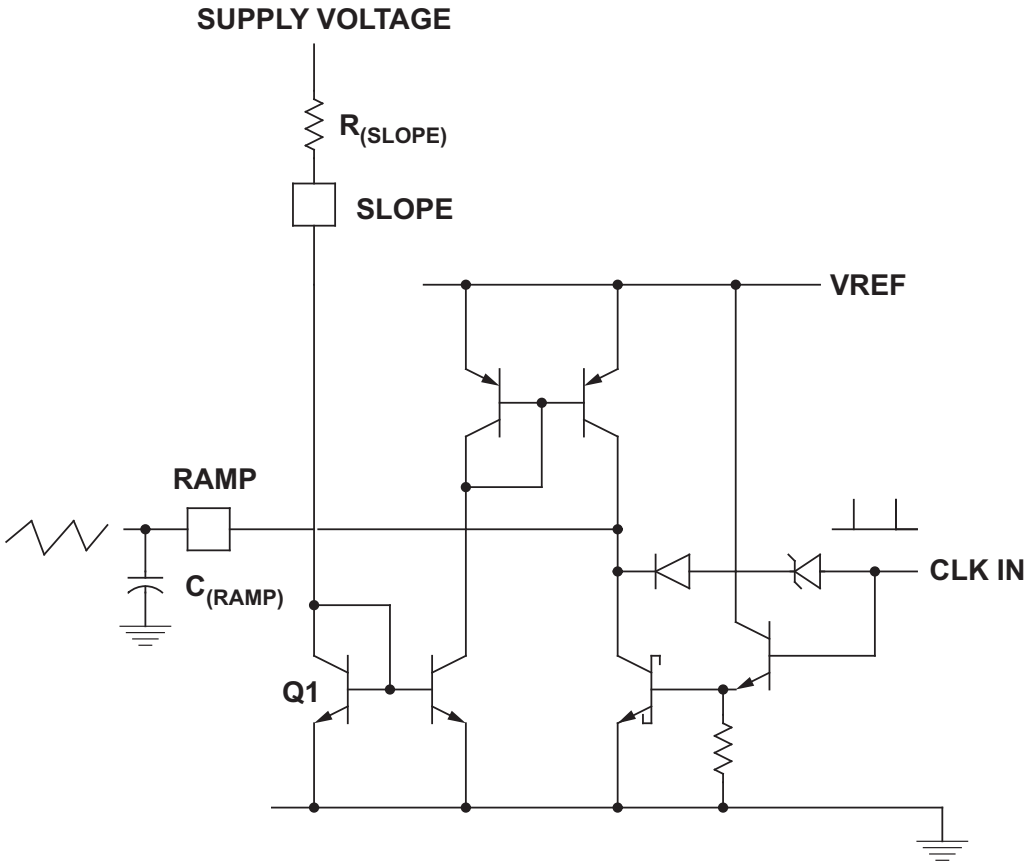


Figure 11. Voltage Mode Operation

1. Simple voltage mode operation achieved by placing $R_{(SLOPE)}$ between VIN and SLOPE
2. Voltage Feedforward achieved by placing $R_{(SLOPE)}$ between supply voltage and SLOPE pin of UC1875-SP.

RAMP:

$$\frac{dV}{dT} = \frac{V_{Rslope}}{R_{SLOPE} \times C_{RAMP}}$$

For current-mode control the ramp generator may be disabled by grounding the slope pin and using the ramp pin as a direct current sense input to the PWM comparator.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9455501VRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9455501VRA UC1875JQMLV
5962-9455501VRA.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9455501VRA UC1875JQMLV
5962-9455502VKA	Active	Production	CFP (W) | 24	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9455502VKA UC1875W-SP
5962-9455502VKA.A	Active	Production	CFP (W) | 24	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9455502VKA UC1875W-SP
5962-9455502VRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9455502VRA UC1875J-SP
5962-9455502VRA.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9455502VRA UC1875J-SP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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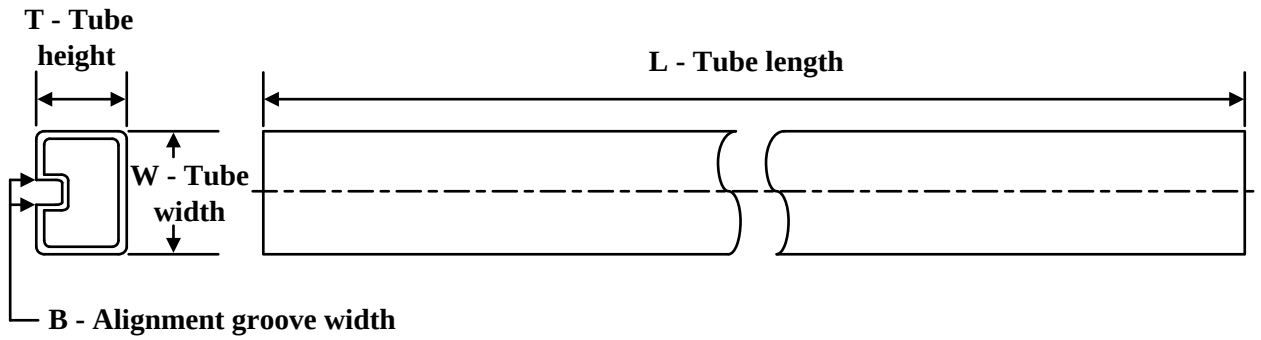
OTHER QUALIFIED VERSIONS OF UC1875-SP :

- Catalog : UC1875

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

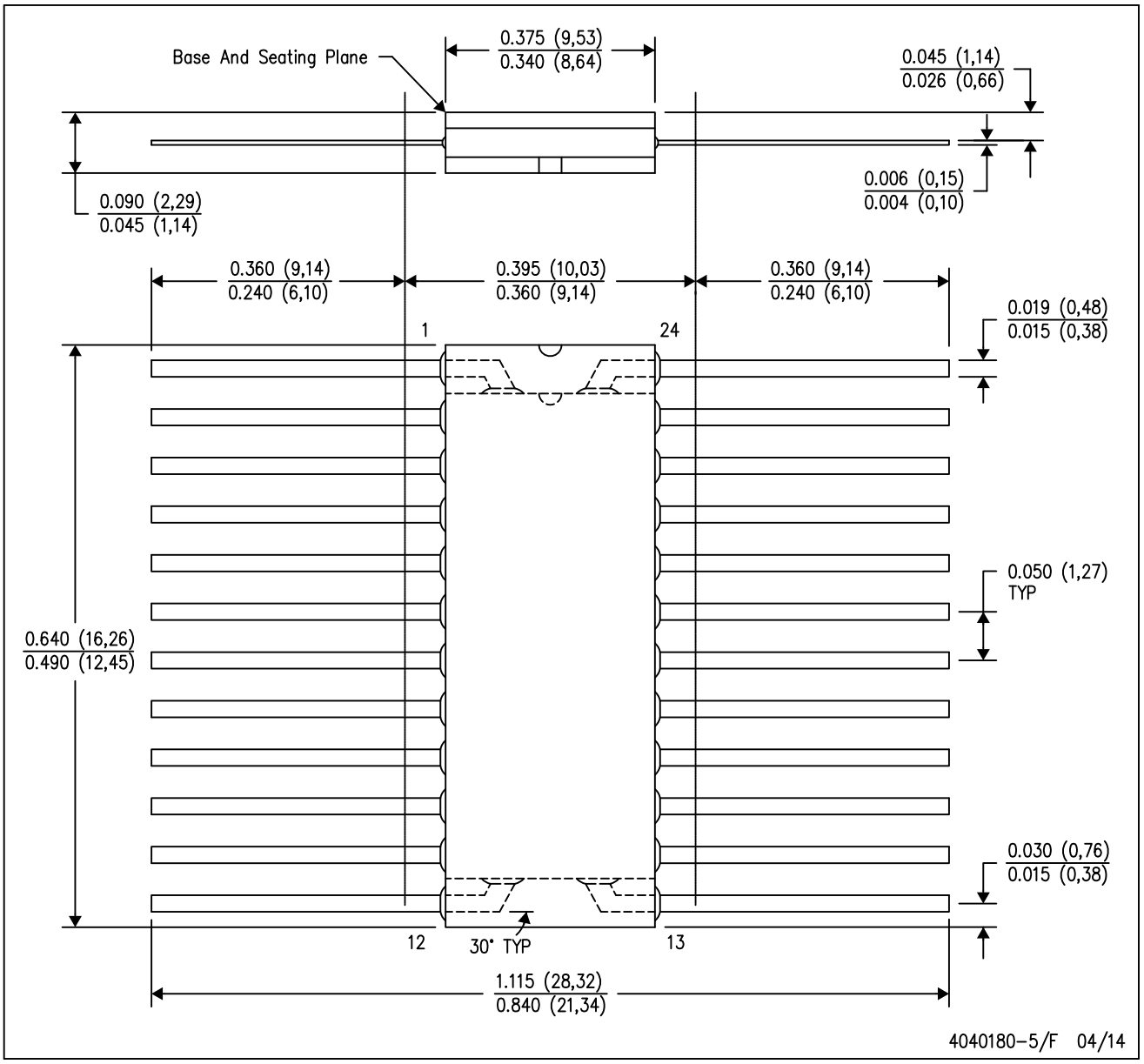
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9455502VKA	W	CFP	24	25	506.98	26.16	6220	NA
5962-9455502VKA.A	W	CFP	24	25	506.98	26.16	6220	NA
5962-9455502VRA	J	CDIP	20	20	506.98	15.24	13440	NA
5962-9455502VRA.A	J	CDIP	20	20	506.98	15.24	13440	NA

W (R–GDFP–F24) CERAMIC DUAL FLATPACK

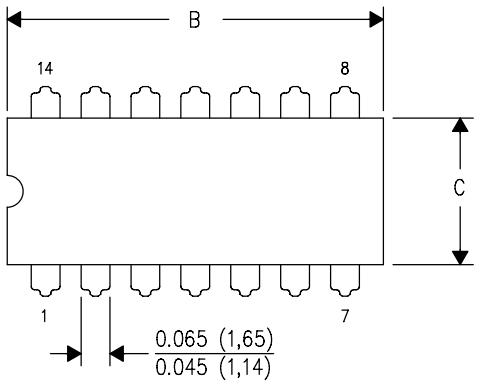


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

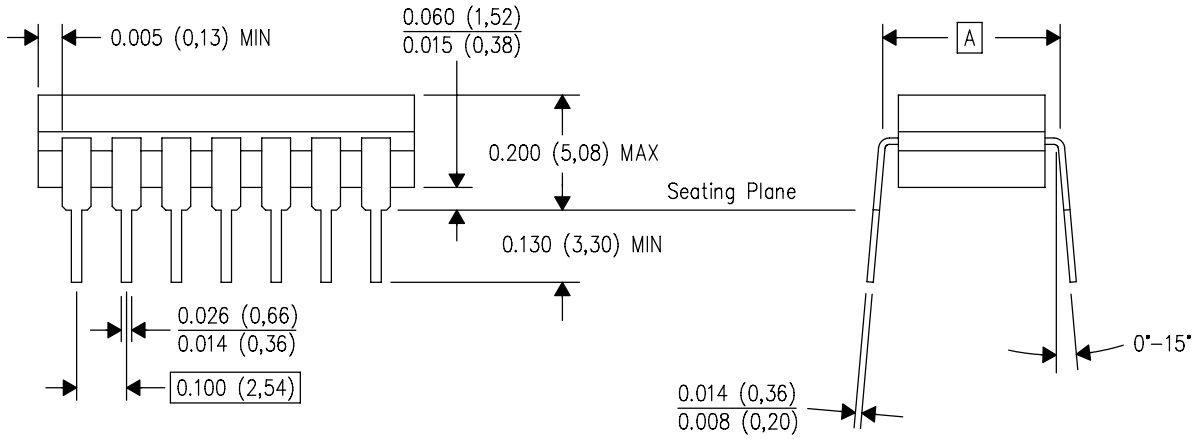
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

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