TUSB213-Q1 USB 2.0 高速信号调节器

1 特性

- 符合汽车应用 要求
- 具有符合 AEC-Q100 标准的下列结果
  - 器件温度等级 2 级：环境工作温度范围为 –40°C 至 105°C
  - 器件 HBM 分类等级 H1C
  - 器件 CDM 分类等级 C3
- 与 USB 2.0、OTG 2.0 和 BC 1.2 兼容
- 引脚搭接或可通过 I^2C 进行配置
- 支持 LS、FS 和 HS 信号传输
- 超低 USB 断开和关断功耗
- 可扩展解决方案 - 用于高损耗应用的菊花链 器件
- D1P/M 和 D2P/M 可互换且主机/设备不可知
- 支持长达 5 米的通道前或 2 米的通道后电缆长度
  - 通过外部下拉电阻器实现四种可选交流升压设置
  - 直流升压与交流升压，可实现最佳信号完整性

2 应用

- 车用信息娱乐
- 笔记本电脑
- 台式机
- 扩展坞
- 平板电脑
- 手机
- 有源电缆、电缆扩展器
- 背板
- 电视

3 说明

TUSB213-Q1 是一款 USB 高速 (HS) 信号调节器，专为补偿传输通道中的 ISI 信号损失而设计， 这有助于通过 USB 电气合规性测试。

TUSB213-Q1 采用了对 USB 低速 (LS) 和全速 (FS) 信号无感知的设计，该设计正在申请专利。LS 和 FS 信号特征不受 TUSB213-Q1 的影响，但该器件会对 HS 信号进行补偿。

借助可编程信号交流升压和直流升压，可精调器件性能，从而优化连接器上的高速信号，这可用于多种不同的 应用。

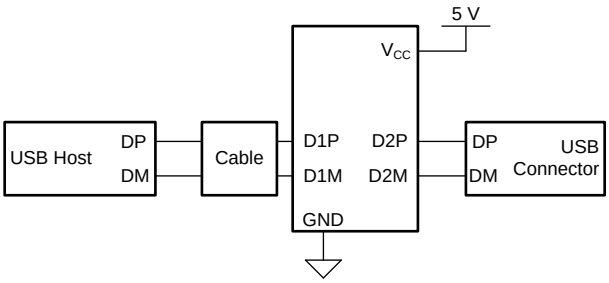
此外，TUSB213-Q1 符合 USB On-The-Go (OTG) 和电池充电 (BC) 协议。

器件信息 (1)

器件型号	封装	封装尺寸（标称值）
TUSB213-Q1	VQFN (14)	3.50mm x 3.50mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化电路原理图



Copyright © 2017, Texas Instruments Incorporated

显示屏



Copyright © 2017, Texas Instruments Incorporated

目录

1 特性 1
2 应用 1
3 说明 1
4 修订历史记录 2
5 **Pin Configuration and Functions** 3
6 **Specifications** 4
6.1 Absolute Maximum Ratings 4
6.2 ESD Ratings 4
6.3 Recommended Operating Conditions 4
6.4 Thermal Information 5
6.5 Electrical Characteristics 5
6.6 Switching Characteristics 6
6.7 Typical Characteristics 7
7 **Detailed Description** 8
7.1 Overview 8
7.2 Functional Block Diagram 8
7.3 Feature Description 8
7.4 Device Functional Modes 8
8 **Application and Implementation** 10
8.1 Application Information 10
8.2 Typical Application 10
9 **Power Supply Recommendations** 17
10 **Layout** 18
10.1 Layout Guidelines 18
10.2 Layout Example 18
11 器件和文档支持 19
11.1 接收文档更新通知 19
11.2 社区资源 19
11.3 商标 19
11.4 静电放电警告 19
11.5 Glossary 19
12 机械、封装和可订购信息 20

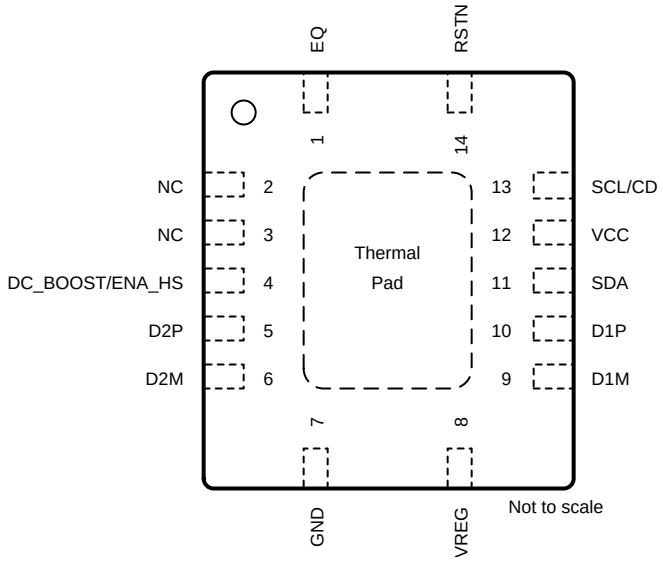
4 修订历史记录

日期	修订版本	说明
2017 年 9 月	*	初始发行版。

Copyright © 2017, Texas Instruments Incorporated

5 Pin Configuration and Functions

RGY Package
14 Pin (VQFN)
Top View



Pin Functions

PIN		I/O	INTERNAL PULLUP/PULLDOWN	DESCRIPTION
NAME	NO.			
EQ	1	I	N/A	USB High Speed AC boost select via external pull down resistor. Sampled upon de-assertion of RSTN. Does not recognize real time adjustments. See application section for details. Auto selects maximum AC boost level when left floating.
NC	2, 3	N/A	N/A	Leave unconnected.
DC_BOOST(1)/ENA_HS	4	I/O		In I2C mode: Reserved for TI test purpose. In non-I2C mode: At reset: 3-level input signal DC_BOOST. USB High Speed DC signal boost selection. H (pin is pulled high) – 80 mV M (pin is left floating) – 60 mV L (pin is pulled low) – 40 mV After reset: Output signal ENA_HS. Flag indicating that channel is in High Speed mode. Asserted upon: 1. Detection of USB-IF High Speed test fixture from an unconnected state followed by transmission of USB TEST_PACKET pattern. 2. Squelch detection following USB reset with a successful HS handshake [HS handshake is declared to be successful after single chirp J chirp K pair where each chirp is within 18 μs – 128 μs].
D2P	5	I/O	N/A	USB High Speed positive port.
D2M	6	I/O	N/A	USB High Speed negative port.
GND	7	PWR	N/A	Ground
VREG	8	O	N/A	1.8-V LDO output. Only enabled when operating in High Speed mode. Requires 0.1-μF external capacitor to GND to stabilize the core.
D1M	9	I/O	N/A	USB High Speed negative port..
D1P	10	I/O	N/A	USB High Speed positive port.
SDA(2)	11	I/O	RSTN asserted: 500 kΩ PD	I2C Mode: Bidirectional I2C data pin [I2C address = 0x2C]. In non I2C mode: Reserved for TI test purpose.

(1) Pull-down and pull-up (to 3.3 V) resistors for DC_BOOST pins must be between 22 kΩ to 47 kΩ in non I^2C mode.
(2) Pull-up resistors for SDA and SCL pins in I^2C mode should be 4.7 kΩ (5%). If both SDA and SCL are pulled up at reset the device enters into I^2C mode.

Copyright © 2017, Texas Instruments Incorporated

Pin Functions (continued)

PIN		I/O	INTERNAL PULLUP/PULLDOWN	DESCRIPTION
NAME	NO.			
VCC	12	PWR	N/A	Supply power
SCL(2)/CD	13	I/O	RSTN asserted: 500 kΩ PD	In I2C mode: I2C clock pin [I2C address = 0x2C]. Non I2C mode: After reset: Output CD. Flag indicating that a USB device is attached (connection detected). Asserted from an unconnected state upon detection of DP or DM pull-up resistor. De-asserted upon detection of disconnect.
RSTN	14	I	500 kΩ PU	Device disable/enable. Low – Device is at reset and in shutdown, and High – Normal operation. Recommend 0.1-µF external capacitor to GND to ensure clean power on reset if not driven. If the pin is driven, it must be held low until the supply voltage for the device reaches within specifications.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature and voltage range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage Range	VCC	-0.3	6	V
Voltage Range on I/O pins	DxP, DxM, RSTN, EQ, SCL, SDA, DC_BOOST, VREG	-0.3	3.8	V
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature and voltage range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.4	5	5.5	V
T_A	Ambient temperature	TUSB213Q1	-40		105	°C
T_J	Junction temperature	TUSB213Q1	-40		125	°C

版权 © 2017, Texas Instruments Incorporated

6.4 Thermal Information

THERMAL METRIC(1)		RGY (VQFN) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
I_{ACTIVE_HS}	High-speed active curent	USB channel = HS mode; 480 Mbps traffic; V_{CC} = 5V; V_{CC} supply stable; DC Boost = 60 mV		18	30	mA
I_{IDLE_HS}	High-speed idle current	USB channel = HS mode; no traffic; V_{CC} = 5V; V_{CC} supply stable; DC Boost = 60 mV		13	22	mA
$I_{SUSPEND_HS}$	High-speed suspend current	USB channel = HS suspend mode; V_{CC} = 5V; V_{CC} supply stable		0.76	1.5	mA
I_{FS_LS}	Full/Low speed current	USB channel = FS mode or LS mode; V_{CC} = 5V		0.77	1.5	mA
$I_{DISCONNECT}$	Disconnect current	Host side application; No device attachment; V_{CC} = 5V		0.86	1.5	mA
I_{RSTN}	Disable current	RSTN driven low; V_{CC} supply stable; V_{CC} = 5V		22	80	µA
I_{LKG_FS}	Pin fail-safe leakage current for SDA, SCL, DC_BOOST, DxP/N, RSTN	V_{CC} = 0 V; Pin at 3.6 V			40	µA
RSTN						
V_{IH}	High-level input voltage	V_{CC} = 4.4V	2		3.6	V
V_{IL}	Low-level input voltage	V_{CC} = 5.5V	0		0.8	V
I_{IH}	High-level input current	V_{IH} = 3.6 V	-4		4	µA
I_{IL}	Low-level input current	V_{IL} = 0 V	-11		11	µA
EQ						
R_{EQ}	External pull-down resistor on EQ pin.	AC Boost Level 0			160	Ω
		AC Boost Level 1	1.4		2	kΩ
		AC Boost Level 2	3.7		3.9	kΩ
		AC Boost Level 3	6			kΩ
CD, ENA_HS						
V_{OH}	High-level output voltage	I_O = -50µA	2.4			V
V_{OL}	Low-level output voltage	I_O = 50µA			0.4	V
SCL, SDA						
C_{I2CBUS}	I2C Bus capacitance		4		150	pF
V_{IH}	SDA and SCL input high level voltage	V_{CC} = 4.4V	2		3.6	V
V_{IL}	SDA and SCL input Low level voltage	V_{CC} = 5.5V			0.8	V
V_{SDA_OL}	SDA low-level output voltage	4.7kΩ pullup to 3.6V; V_{CC} = 4.4V			0.4	V
I_{SDA_OL}	SDA Low level output current	V_{CC} = 5.5V; I^2C pulled up to 3.6V	1.1			mA
DC_BOOST						

Copyright © 2017, Texas Instruments Incorporated

Electrical Characteristics (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	V_{CC} = 5V	2.4		3.6	V
V_{IM}	Mid-level input voltage	V_{CC} = 5V		1.6		V
V_{IL}	Low-level input voltage	V_{CC} = 5V	0		0.4	V
DxP, DxM						
C_{IO_DXX}	Capacitance to GND	Measured with LCR meter and device powered down. 1 MHz sinusoid, 30 mVpp ripple		2.7		pF

6.6 Switching Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{BR_DXX}	DxP/M Bit Rate	USB channel = HS mode; 480 Mbps traffic; VCC supply stable			480.24	Mbps
t_{RISE_DXX}	DxP/M rise time	10% - 90%; V_{CC} = 5.5V; Max AC Gain;	100			ps
t_{FALL_DXX}	DxP/M fall time	90% - 10%; V_{CC} = 5.5V; Max AC Gain;	100			ps
$t_{RSTN_PULSE_WIDTH}$	Minimum width to detect a valid RSTN signal assert when the pin is actively driven	V_{CC} = 4.4 V; Refer to 图 1	20			µs
t_{STABLE}	VCC stable before RSTN de-assertion	Refer to 图 1	100			µs
t_{VCC_RAMP}	VCC ramp time		0.2		100	ms

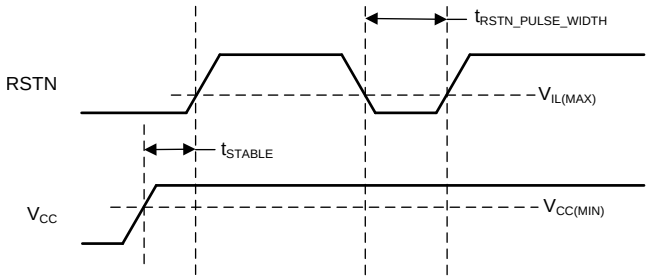


图 1. Power On and Reset Timing

版权 © 2017, Texas Instruments Incorporated

6.7 Typical Characteristics

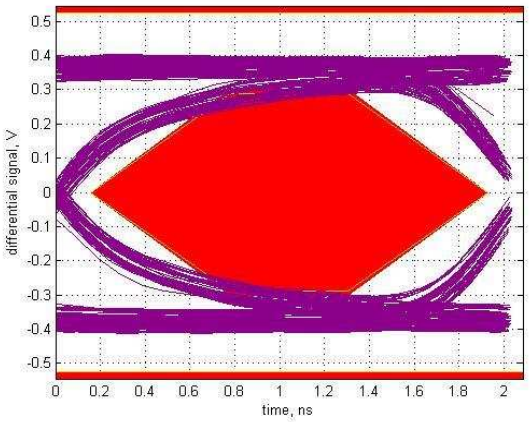


图 2. USB2.0 HS Eye diagram, Host far-end with 2m cable post-channel loss without TUSB213-Q1

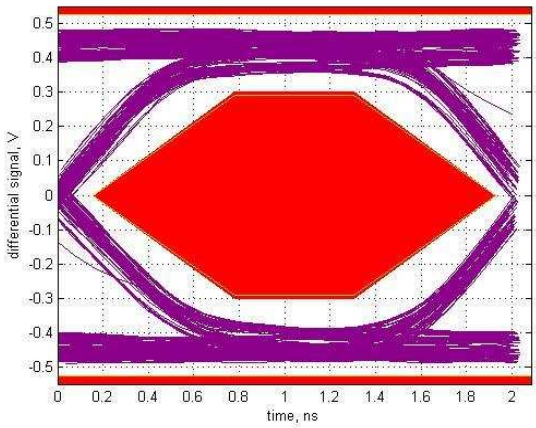


图 3. USB2.0 HS Eye diagram, Host far-end with 2m cable post-channel loss with TUSB213-Q1

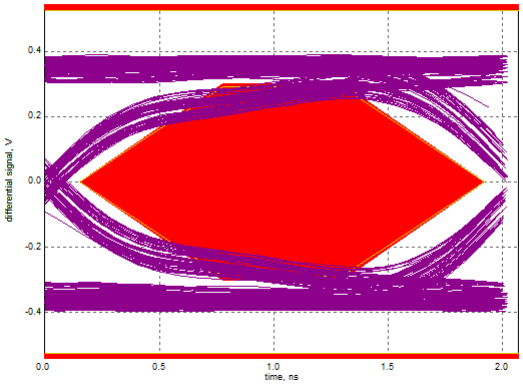


图 4. USB2.0 HS Eye diagram, Host far-end with 5m cable pre-channel loss without TUSB213-Q1

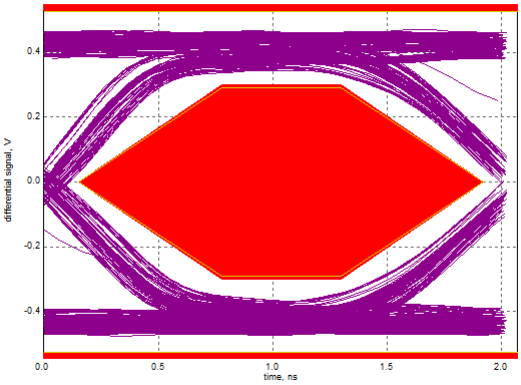


图 5. USB2.0 HS Eye diagram, Host far-end with 5m cable pre-channel loss with TUSB213-Q1

版权 © 2017, Texas Instruments Incorporated

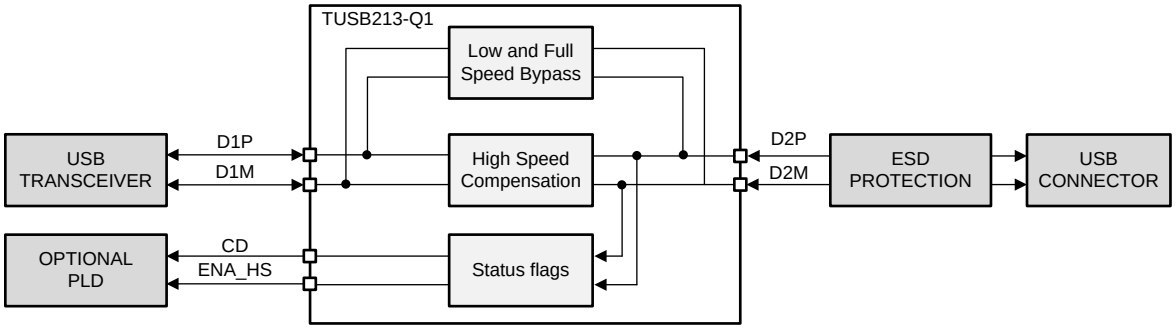
7 Detailed Description

7.1 Overview

The TUSB213-Q1 is a USB High-Speed (HS) signal conditioner, designed to compensate for ISI signal loss in a transmission channel. TUSB213-Q1 has a patent-pending design which is agnostic to USB Low Speed (LS) and Full Speed (FS) signals and does not alter their signal characteristics, while HS signals are compensated. In addition, the design is compatible with USB On-The-Go (OTG) and Battery Charging (BC) specifications.

Programmable signal AC boost through an external resistor on EQ pin permits fine tuning device performance to optimize signals helping to pass USB HS electrical compliance tests at the connector. Additional DC Boost configurable by three level input DC_BOOST pin helps overcoming the cable losses.

7.2 Functional Block Diagram



Copyright © 2017, Texas Instruments Incorporated

7.3 Feature Description

7.3.1 EQ

The EQ pin of the TUSB213-Q1 is used to configure the AC boost of the device. The four levels of AC boost are set through different values of an external pulldown resistor at this pin.

7.3.2 DC BOOST

The DC_BOOST pin of the TUSB213-Q1 is a tri-level pin, used to set the DC gain of the device according to 表 1.

表 1. DC Boost Settings

DC BOOST SETTING VIA PIN STRAP	
DC_BOOST	**DC Boost Setting (mV)**
V_{IL}	40
V_{IM}	60
V_{IH}	80

7.4 Device Functional Modes

7.4.1 Low Speed (LS) Mode

TUSB213-Q1 automatically detects a LS connection and does not enable signal compensation. CD pin is asserted high.

7.4.2 Full Speed (FS) Mode

TUSB213-Q1 automatically detects a FS connection and does not enable signal compensation. CD pin is asserted high.

版权 © 2017, Texas Instruments Incorporated

Device Functional Modes (接下页)

7.4.3 High Speed (HS) Mode

TUSB213-Q1 automatically detects a HS connection and will enable signal compensation as determined by the configuration of the DC_BOOST pin and the external pulldown resistance on its EQ pin. CD pin asserted high.

7.4.4 Shutdown Mode

TUSB213-Q1 is disabled when its RSTN pin is asserted low. In shutdown mode, the USB channel is still fully operational but there is neither signal compensation nor any indication from the CD pin as to the status of the channel.

7.4.5 I^2C Mode

TUSB213-Q1 support 100 kHz I^2C for device configuration, status readback and test purposes. This controller is enabled after SCL and SDA pins are sampled high shortly after de-assertion of RSTN. In this mode, the register as described in 表 2 can be accessed by I^2C read/write transaction to 7-bit slave address 0x2C. It is necessary to set CFG_ACTIVE bit and reset it to zero after making changes to the EQ and DC Boost level registers to restart the state machine.

注

All registers or fields in 表 2 which are not specifically mentioned are considered reserved. The default value of these reserved registers or fields must not be changed. It is suggested to perform a read-modify-write operation to maintain the default value of the reserved fields.

表 2. Register definition

Offset	Bit(s)	Name	Type	Default	Description
0x01	6:4	ACB_LVL	RW	XXX (Sampled from EQ pin at reset)	Sets the level of AC boost 000 :Level 0 AC boost programmed [MIN] 001 : Level 1 AC boost programmed 011 : Level 2 AC boost programmed 111 : Level 3 AC boost programmed [MAX]
0x03	0	CFG_ACTIVE	RW	1b	Configuration mode 0 : Normal mode. State machine enabled. 1 : Configuration mode: State machine disabled. After reset, if I2C mode is true (SCL and SDA are both pulled high) it is maintained until it is cleared by an I2C write, but, if I2C mode is not true, it is cleared automatically.
0x0E	2:0	DCB_LVL	RW	XXX (Sampled from DC_BOOST pin at reset)	Sets the level of DC Boost 011 : 40mV (DC_Boost = L) 101 : 60mV (DC_Boost = M, default) 111 : 80mV (DC_Boost = H)

版权 © 2017, Texas Instruments Incorporated

8 Application and Implementation

> **注**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

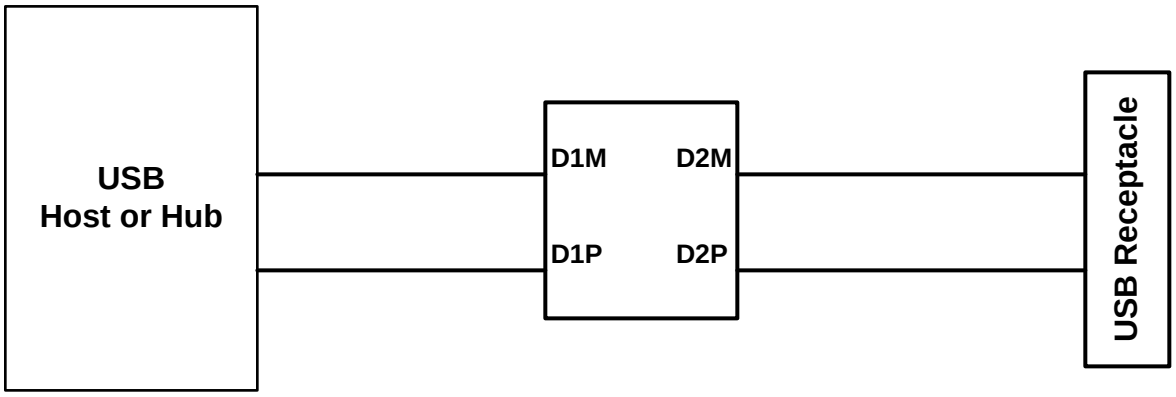
8.1 Application Information

The primary purpose of the TUSB213-Q1 is to re-store the signal integrity of a USB High Speed channel up to the USB connector. The loss in signal quality stems from reduced channel bandwidth due to high loss PCB trace and other components that contribute a capacitive load. This can cause the channel to fail the USB near end eye mask. Proper use of the TUSB213-Q1 can help to pass this eye mask. Additionally the DC Boost helps overcoming DC losses from cables and traces.

A secondary purpose is to use the CD pin of the TUSB213-Q1 to control other blocks on the customer platform if so desired.

8.2 Typical Application

A typical application is shown in 图 6. In this setup, D2P and D2M face the USB connector while D1P and D1M face the USB host or hub. If desired, the orientation may be reversed [that is, D2 faces transceiver and D1 faces connector].



Copyright © 2017, Texas Instruments Incorporated

图 6. Typical Application

版权 © 2017, Texas Instruments Incorporated

Typical Application (接下页)

8.2.1 Design Requirements

For this design example, use the parameters shown in the table below.

表 3. Design Parameters

PARAMETER				VALUE
V_{CC} (4.4 V to 5.5 V)				5 V
I^2C support required in system (Yes/No)				No
AC Boost		R_{EQ}	Level	AC Boost Level 2: R_{EQ} = 3.83 k
		0-Ω	0	
		1.69 k ±1%	1	
		3.83 k ± 1%	2	
		DNI	3	
DC Boost	R_{DC1}	R_{DC2}	Level	Mid DC Level: R_{DC1} = DNI R_{DC2} = DNI
	22 kΩ - 47 kΩ	Do Not Install (DNI)	40 mV Low DC boost	
	DNI	DNI	60 mV Mid DC boost	
	47 kΩ	24 kΩ	80 mV High DC boost	

8.2.2 Detailed Design Procedure

TUSB213-Q1 requires a valid reset signal as described in the power supply recommendations section. The capacitor at RSTN pin is not required if a microcontroller drives the RSTN pin according to recommendations.

VREG pin is the internal LDO output that requires a 0.1-μF external capacitor to GND to stabilize the core.

The ideal AC boost setting is dependent upon the signal chain loss characteristics of the target platform. The general recommendation is to start with AC boost level 0, and then increment to AC boost level 1, etc. if permissible. Same applies to the DC Boost setting where it is recommended to plan for the required pads or connections to change boost settings, but to start with DC boost level 1.

In order for the TUSB213-Q1 to recognize any change to the AC and DC Boost settings, the RSTN pin must be toggled. This is because the configuration is latched on power up and the inputs are ignored thereafter.

注

The TUSB213-Q1 compensates for DC attenuation in the signal path according to the configuration of the DC_BOOST pin. This pin is not 5V tolerant and therefore when selecting the highest DC boost level, the voltage level at DC_BOOST pin must be less than 3.6V.

Placement of the device is also dependent on the application goal. 表 4 summarizes our recommendations.

表 4. Platform Placement Guideline

PLATFORM GOAL	SUGGESTED DEVICE PLACEMENT
Pass USB Near End Mask	Close to measurement point
Pass USB Far End Eye Mask	Close to USB PHY
Cascade multiple devices to improve device enumeration	Midway between each USB interconnect

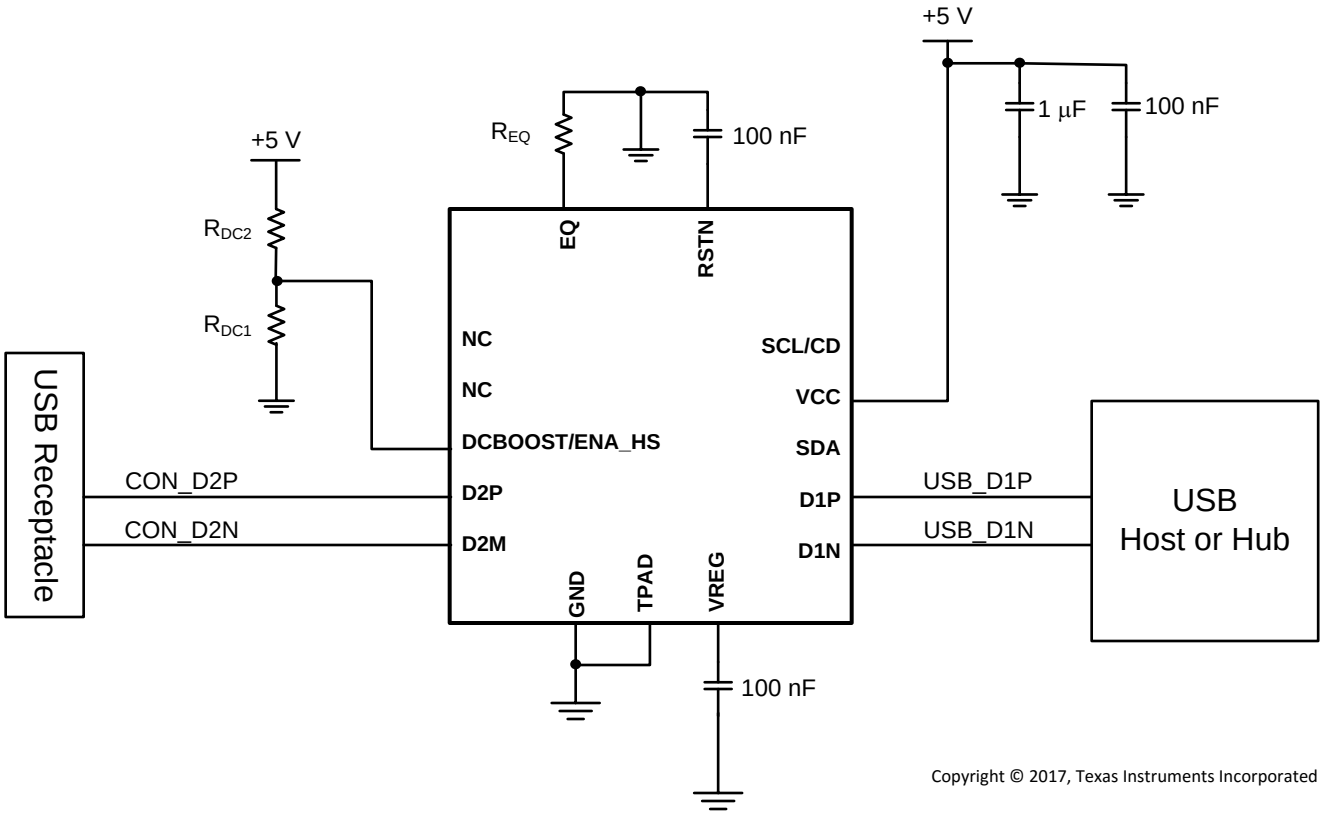


图 7. Reference Schematic

版权 © 2017, Texas Instruments Incorporated

8.2.2.1 Test Procedure to Construct USB High Speed Eye Diagram

注

USB-IF certification tests for High Speed eye masks require the *mandated use* of the USB-IF developed test fixtures. These test fixtures do not require the use of oscilloscope probes. Instead they use SMA cables. More information can be found at the USB-IF Compliance Updates Page. It is located under the 'Electricals' section, ID 86 dated March 2013.

The following procedure must be followed before using any oscilloscope compliance software to construct a USB High Speed Eye Mask:

8.2.2.1.1 For a Host Side Application

1. Configure the TUSB213-Q1 to the desired AC and DC Boost settings
2. Power on (or toggle the RSTN pin if already powered on) the TUSB213-Q1
3. Using SMA cables, connect the oscilloscope and the USB-IF host-side test fixture to the TUSB213-Q1
4. Enable the host to transmit USB TEST_PACKET
5. Execute the oscilloscope USB compliance software.
6. Repeat the above steps in order to re-test TUSB213-Q1 with a different settings

8.2.2.1.2 For a Device Side Application

1. Configure the TUSB213-Q1 to the desired AC and DC Boost settings
2. Power on (or toggle the RSTN pin if already powered on) the TUSB213-Q1
3. Connect a USB host, the USB-IF device-side test fixture, and USB device to the TUSB213-Q1. Ensure that the USB-IF device test fixture is configured to the 'INIT' position
4. Allow the host to enumerate the device
5. Enable the device to transmit USB TEST_PACKET
6. Using SMA cables, connect the oscilloscope to the USB-IF device-side test fixture and ensure that the device-side test fixture is configured to the 'TEST' position.
7. Execute the oscilloscope USB compliance software.
8. Repeat the above steps in order to re-test TUSB213-Q1 with a different settings

版权 © 2017, Texas Instruments Incorporated

8.2.3 Application Curves

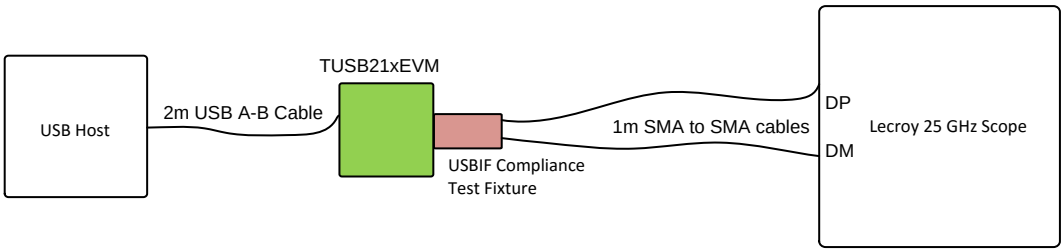


图 8. Eye Diagram Bench Setup

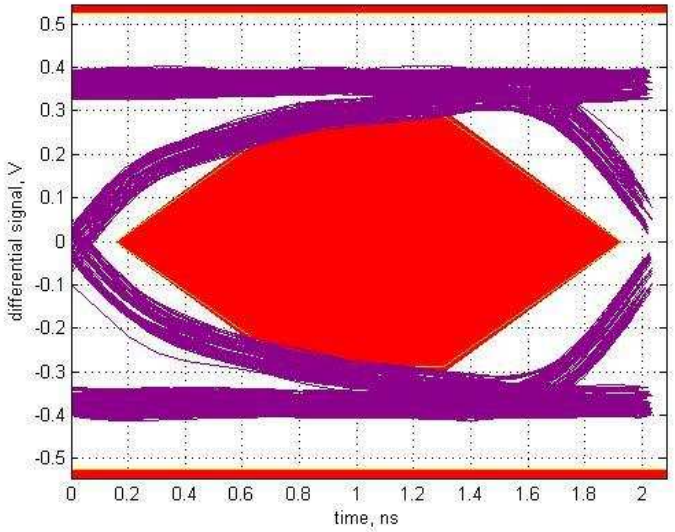


图 9. No TUSB213-Q1

版权 © 2017, Texas Instruments Incorporated

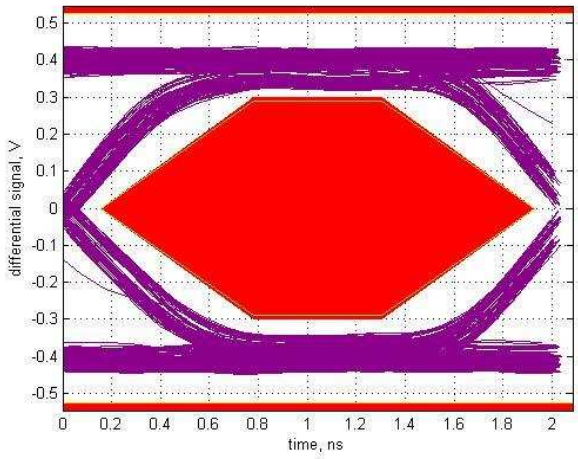


图 10. Low DC Boost, AC Boost Level 0

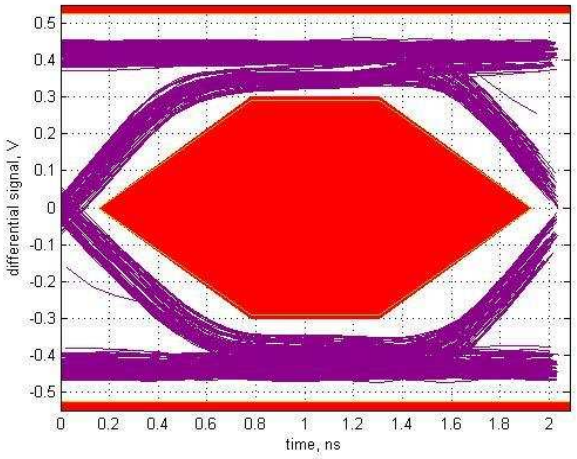


图 11. Mid DC Boost, AC Boost Level 0

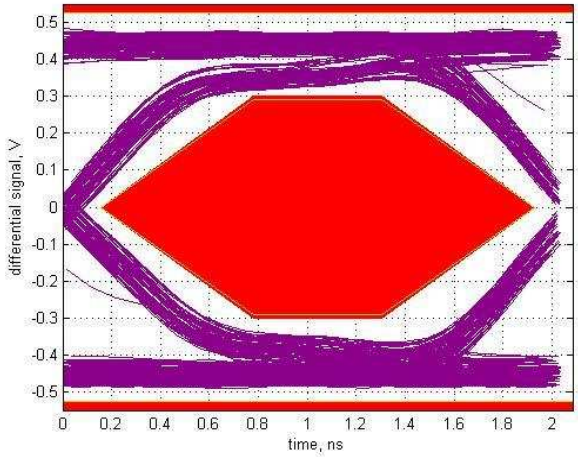


图 12. High DC Boost, AC Boost Level 0

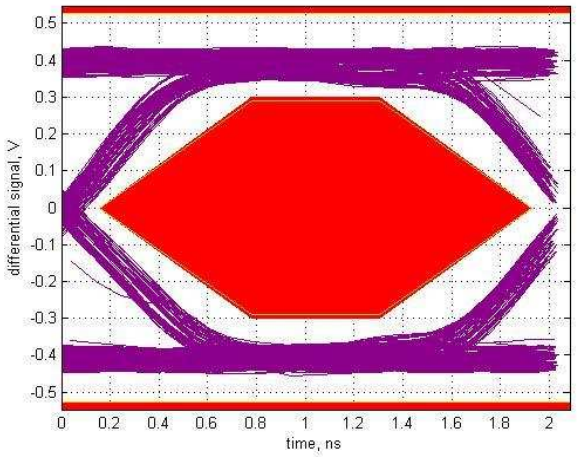


图 13. Low DC Boost, AC Boost Level 1

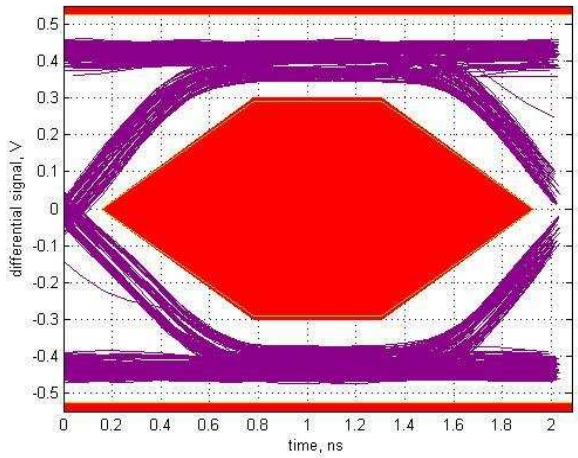


图 14. Mid DC Boost, AC Boost Level 1

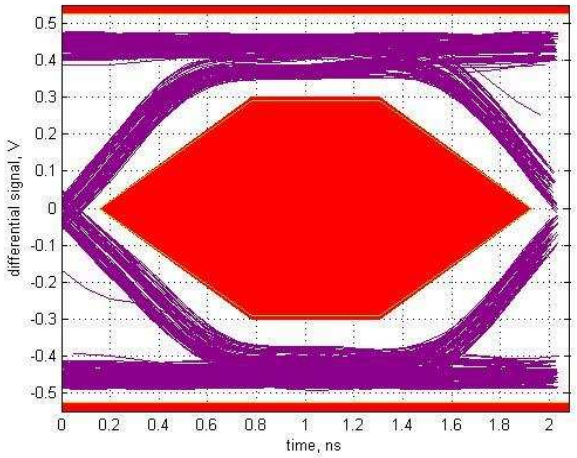


图 15. High DC Boost, AC Boost Level 1

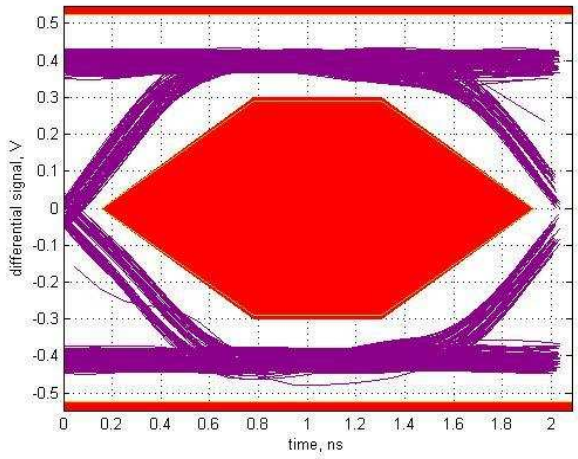


图 16. Low DC Boost, AC Boost Level 2

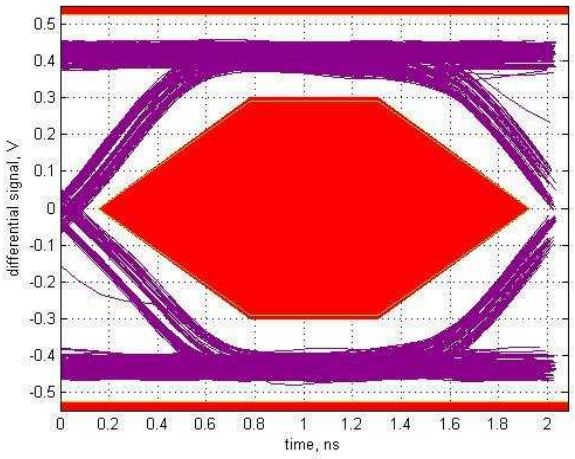


图 17. Mid DC Boost, AC Boost Level 2

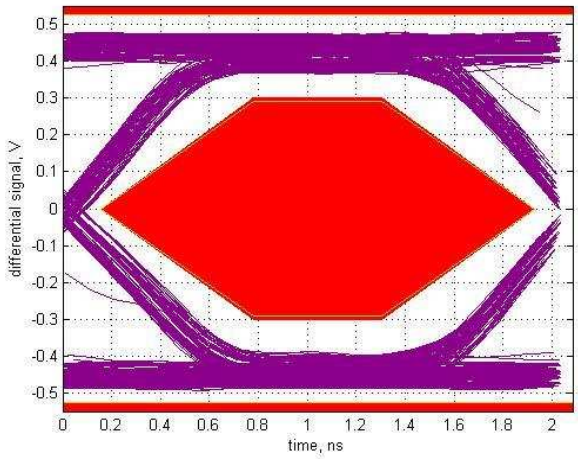


图 18. High DC Boost, AC Boost Level 2

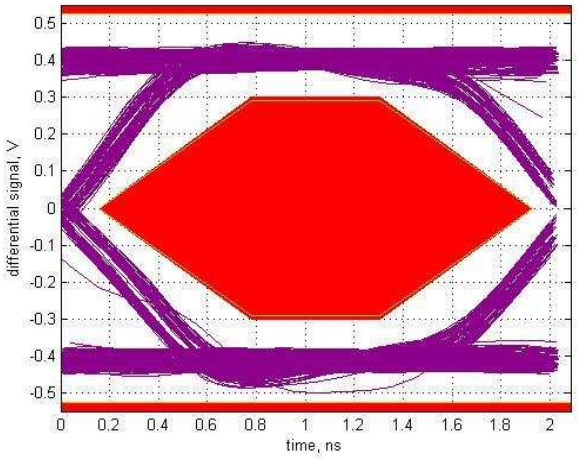


图 19. Low DC Boost, AC Boost Level 3

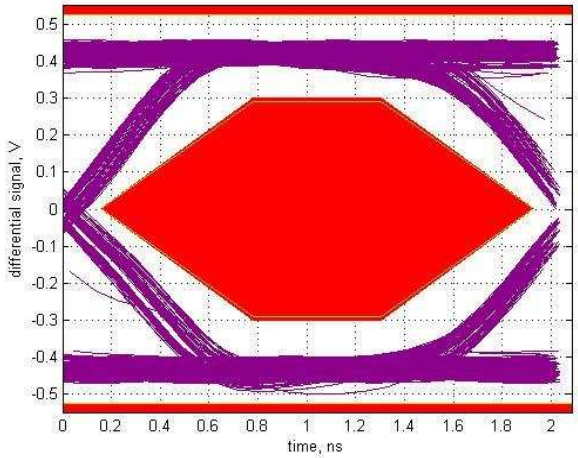


图 20. Mid DC Boost, AC Boost Level 3

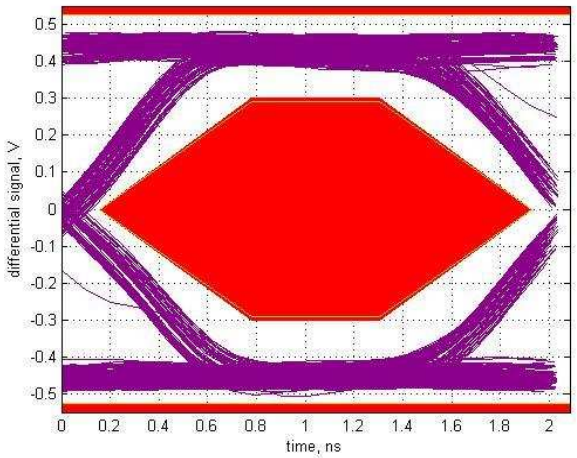


图 21. High DC Boost, AC Boost Level 3

版权 © 2017, Texas Instruments Incorporated

9 Power Supply Recommendations

On power up, the interaction of the RSTN pin and power on ramp could result in digital circuits not being set correctly. The device should not be enabled until the power on ramp has settled to 4.4 V or higher to ensure a correct power on reset of the digital circuitry. If RSTN cannot be held low by microcontroller or other circuitry until the power on ramp has settled, then an external capacitor from the RSTN pin to GND is required to hold the device in the low power reset state.

The RC time constant should be larger than five times of the power on ramp time (0 to V_{CC}). With a typical internal pullup resistance of 500 kΩ, the recommended minimum external capacitance is calculated as:

$$C_{RSTN} = [\text{Ramp Time} \times 5] \div [500\ k\Omega] \quad (1)$$

版权 © 2017, Texas Instruments Incorporated

10 Layout

10.1 Layout Guidelines

To avoid the need for signal vias, it is highly recommend to route the High Speed traces on the same surface layer than the TUSB213-Q1 is placed. shows an example how one could layout the PCB for TUSB213-Q1.

The layout should use impedance controlled traces to maintain 90 Ω differential impedance for the whole signal path as required per USB 2.0 specification. General guidelines for highspeed signal routing apply.

10.2 Layout Example

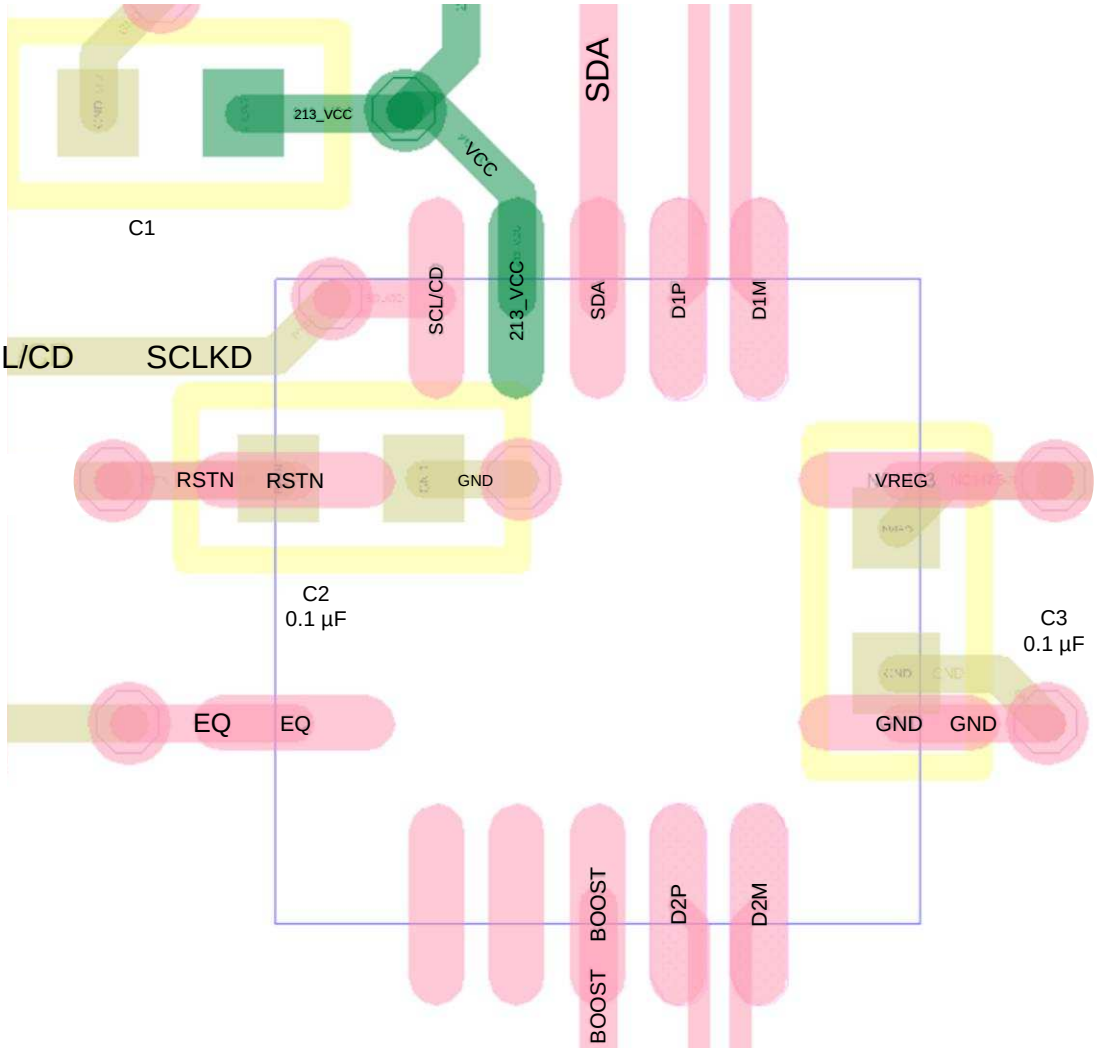


图 22. Layout Example

版权 © 2017, Texas Instruments Incorporated

11 器件和文档支持

11.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

版权 © 2017, Texas Instruments Incorporated

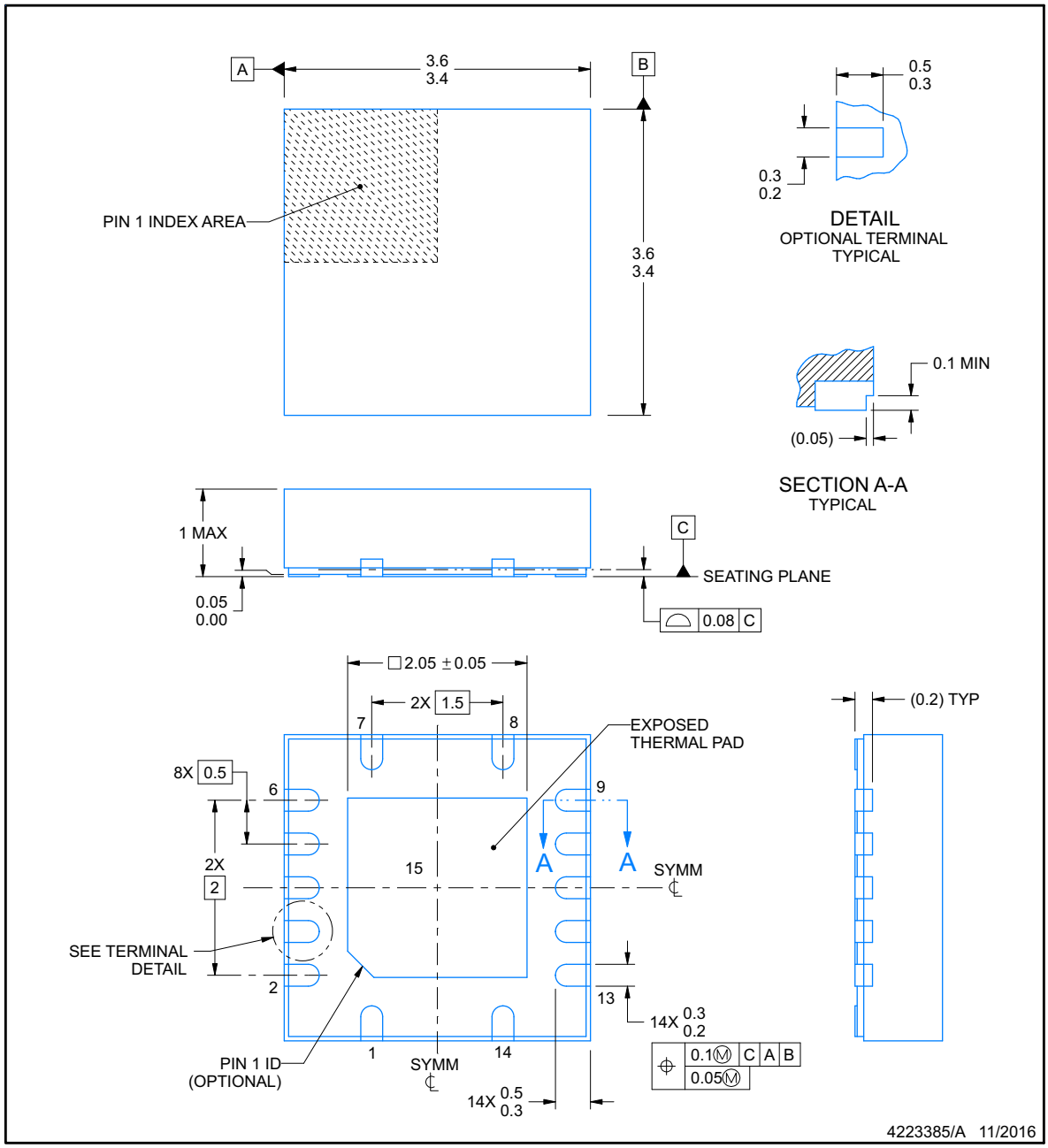
PACKAGE OUTLINE

RGY0014B



VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

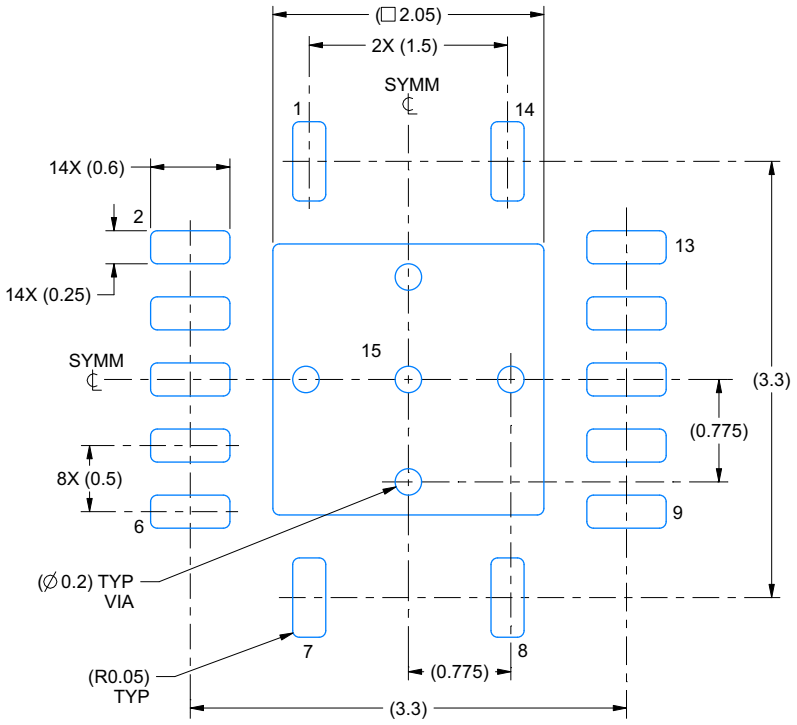
版权 © 2017, Texas Instruments Incorporated

EXAMPLE BOARD LAYOUT

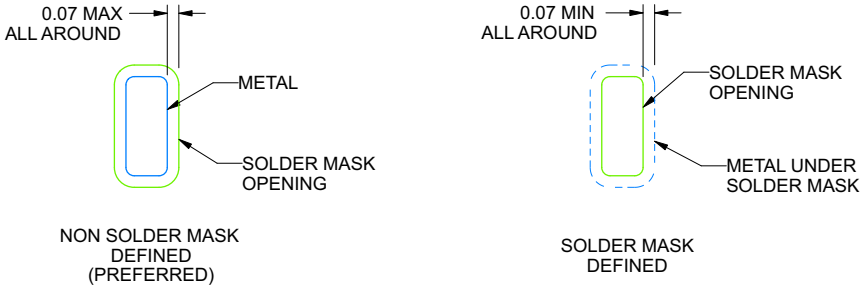
RGY0014B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4223385/A 11/2016

NOTES: (continued)

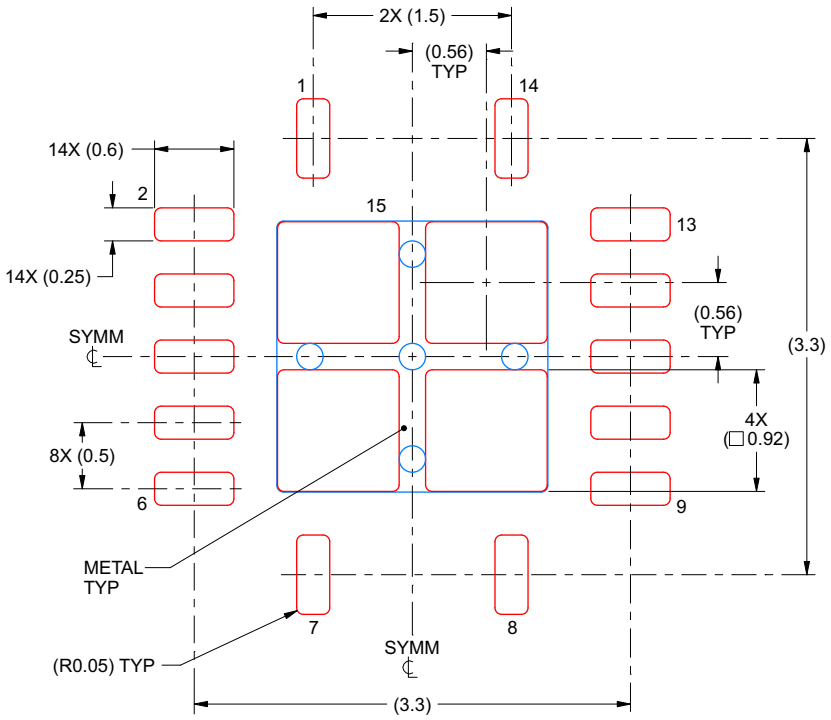
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

版权 © 2017, Texas Instruments Incorporated

EXAMPLE STENCIL DESIGN

RGY0014B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223385/A 11/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

版权 © 2017, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TUSB213QRGYRQ1	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 105	USB213
TUSB213QRGYRQ1.A	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 105	USB213
TUSB213QRGYTQ1	Active	Production	VQFN (RGY) | 14	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 105	USB213
TUSB213QRGYTQ1.A	Active	Production	VQFN (RGY) | 14	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 105	USB213

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TUSB213-Q1 :

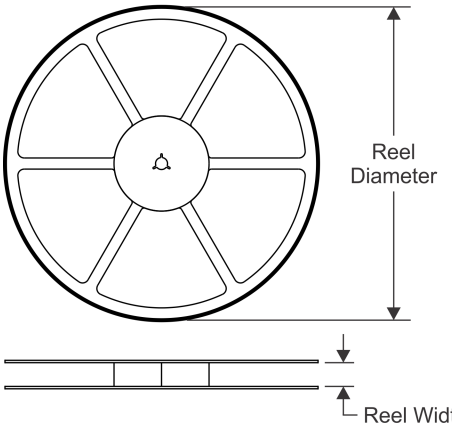
- Catalog : TUSB213

NOTE: Qualified Version Definitions:

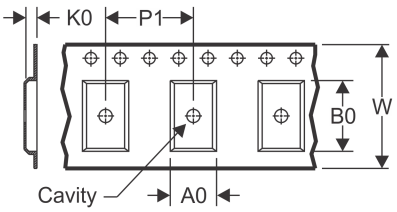
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

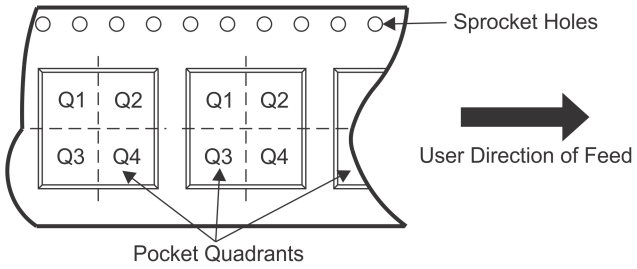


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

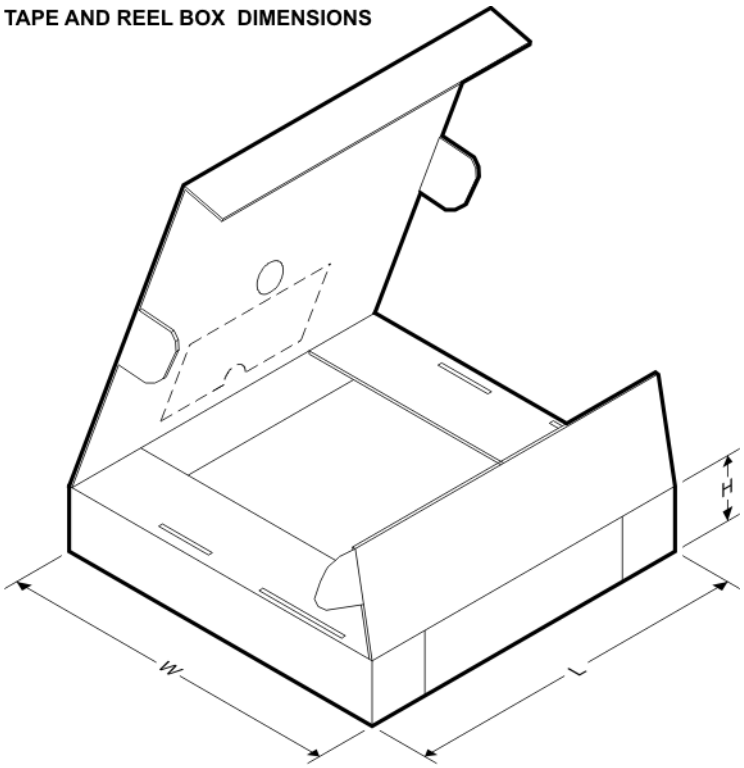
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB213QRGYRQ1	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2
TUSB213QRGYTQ1	VQFN	RGY	14	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB213QRGYRQ1	VQFN	RGY	14	3000	367.0	367.0	38.0
TUSB213QRGYTQ1	VQFN	RGY	14	250	213.0	191.0	35.0

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2025，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月