TS5A22364-Q1 具有负信号功能的 0.65Ω 双路 SPDT 模拟开关

1 特性

- 适用于汽车电子 应用
- 指定的先断后合 (BBM) 开关
- 负信号摆幅功能：最大摆幅范围为 –2.75V 到 2.75V (V_{CC} = 2.75V)
- 内部分流开关，可防止在切换电源时出现喀哒声和噼啪声
- 低导通状态电阻（0.65Ω 典型值）
- 低电荷注入
- 出色的通道间导通状态电阻匹配
- 2.25V 至 5.5V 电源 (V_{CC})
- 锁断性能达 100mA，符合 AEC Q100-004
- 静电放电 (ESD) 性能
  - 通过 2500V 人体模型测试，符合 AEC Q100-002
  - 通过 1500V 带电器件模型测试，符合 AEC Q100-011

2 应用

- 车用信息娱乐
- 音频路由
- 工业自动化
- 医疗成像

3 说明

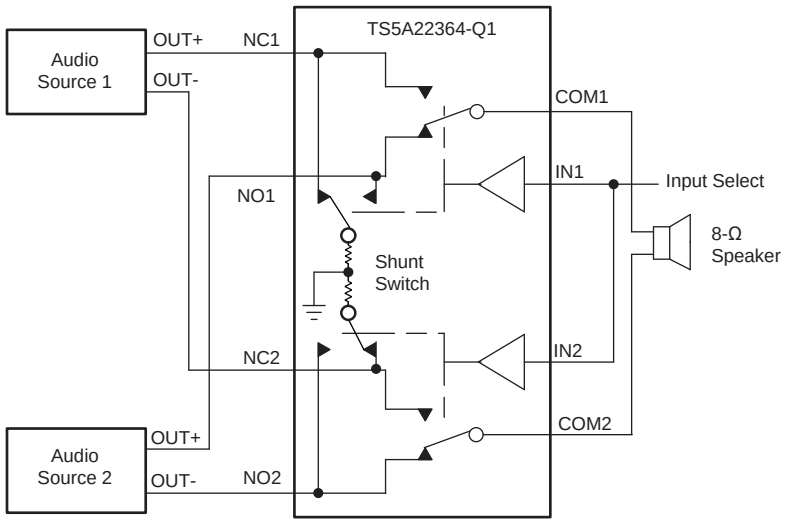
TS5A22364-Q1 是一款双通道单刀双掷 (SPDT) 模拟开关，设计用于 2.3V 至 5.5V 电源。该器件 支持 负信号摆幅，允许低于接地电平的信号通过开关，同时不发生失真。此外，TS5A22364-Q1 还包含一个内部分流开关，能够在常闭或常开引脚未连接至 COM 时使其电容放电。此开关可降低在切换电源时出现的喀哒声和噼啪声。先断后合特性可防止信号在跨路径传输时出现失真。该器件同时拥有低导通电阻、出色的通道间导通状态电阻匹配以及最小总谐波失真 (THD) 性能，是音频应用的 理想选择。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TS5A22364-Q1	VSSOP (10)	3.00mm x 3.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

LP38690 的



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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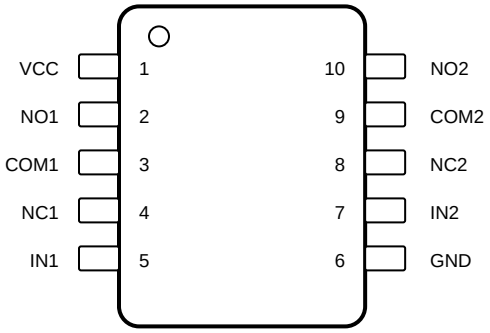
Changes from Original (October 2014) to Revision A **Page**

- 器件状态从*产品预览*改为*量产数据* ... 1

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5 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VCC	I	Supply power
2	NO1	I/O	Normally open (NO) signal path, switch 1
3	COM1	I/O	Common signal path, switch 1
4	NC1	I/O	Normally closed (NC) signal path, switch 1
5	IN1	I	Digital control pin to connect COM1 to NO1, switch 1
6	GND	—	Ground
7	IN2	I	Digital control pin to connect COM2 to NO2, switch 2
8	NC2	I/O	Normally closed (NC) signal path, switch 2
9	COM2	I/O	Common signal path, switch 2
10	NO2	I/O	Normally open (NO) signal path, switch 2

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(3)		–0.5	6	V
V_{NC}	Analog voltage on NC1-NC2 pin(3) (4) (5)		V_{CC} – 6	V_{CC} + 0.5	V
V_{NO}	Analog voltage on NO1-NO2 pin(3) (4) (5)				
V_{COM}	Analog voltage on COM1-COM2 pin(3) (4) (5)				
$I_{I/OK}$	Analog port diode input clamp current	V_{NC}, V_{NO}, V_{COM} < 0 or V_{NC}, V_{NO}, V_{COM} > V_{CC}	–50	50	mA
I_{NC} I_{NO} I_{COM}	On-state switch continuous current	V_{NC}, V_{NO}, V_{COM} = 0 to V_{CC}	–150	150	mA
	On-state switch peak current(6)		–300	300	
I_{RSH}	Off-state switch shunt resistor current		–20	20	mA
V_{IN}	Digital input voltage		–0.5	6.5	V
I_{IK}	Digital input clamp current(3) (4)	V_{IN} < 0	–50	50	mA
I_{CC} I_{GND}	Continuous current through V_{CC} or GND		–100	100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Pulse at 1-ms duration <10% duty cycle.

6.2 ESD Ratings

				MIN	MAX	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		–2500	2500	V
		Charged device model (CDM), per AEC Q100-011	all pins	–1500	1500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.3	5.5	V
V_{NC}	Signal path voltage	V_{CC} – 5.5	V_{CC}	V
V_{NO}				
V_{COM}				
V_{IN}	Digital control	GND	V_{CC}	V

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6.4 Thermal Information

THERMAL METRIC[1] [2]		TS5A22364-Q1 DGS (VSSOP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	163.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	81.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics—2.5-V Supply

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to +125°C (unless otherwise noted) [1]

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
Analog signal	V_{COM} V_{NO} V_{NC}					V_{CC} – 5.5		V_{CC}	V
On-state resistance	R_{on}	V_{NC} or V_{NO} = V_{CC}, 1.5 V, V_{CC} – 5.5 V I_{COM} = –100 mA	COM to NO or NC, See Figure 14	25°C	2.7 V		0.65	0.94	Ω
				–40°C to +125°C				1.3	
On-state resistance match between channels	ΔR_{on}	V_{NC} or V_{NO} = 1.5 V, I_{COM} = –100 mA	COM to NO or NC, See Figure 14	25°C	2.7 V		0.023	0.11	Ω
				–40°C to +125°C				0.15	
On-state resistance flatness	$R_{on(flat)}$	V_{NC} or V_{NO} = V_{CC}, 1.5 V, V_{CC} – 5.5 V I_{COM} = –100 mA	COM to NO or NC, See Figure 14	25°C	2.7 V		0.18	0.46	Ω
				–40°C to +125°C				0.56	
Shunt switch resistance	R_{SH}	I_{NO} or I_{NC} = 10 mA		–40°C to +125°C	2.7 V		25	55	Ω
On-state leakage current	$I_{COM(ON)}$	V_{NC} and V_{NO} = floating, V_{COM} = V_{CC} , V_{CC} – 5.5 V	See Figure 16	25°C	2.7 V	–200		200	nA
				–40°C to +125°C		–2500		2500	
DIGITAL CONTROL INPUTS (IN)[2]									
Input logic high	V_{IH}			–40°C to +125°C		1.4		V_{CC}	V
Input logic low	V_{IL}			–40°C to +125°C				0.4	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = V_{CC} or 0		25°C	2.7 V	–250		250	nA
				–40°C to +125°C		–250		250	
DYNAMIC									
Turnon time	t_{ON}	V_{COM} = V_{CC}, R_L = 300 Ω	C_L = 35 pF, See Figure 18	25°C	2.5 V		44	80	ns
				–40°C to +125°C	2.3 V to 2.7 V			120	
Turnoff time	t_{OFF}	V_{COM} = V_{CC}, R_L = 300 Ω	C_L = 35 pF, See Figure 18	25°C	2.5 V		22	70	ns
				–40°C to +125°C	2.3 V to 2.7 V			70	
Break-before-make time	t_{BBM}		See Figure 19	25°C	2.5 V	1	7		ns
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 23	25°C	2.5 V		215		pC
On-State NC, NO, COM capacitance	$C_{COM(ON)}$	V_{COM} = V_{CC} or GND, Switch ON, f = 10 MHz	See Figure 17	25°C	2.5 V		370		pF
Digital input capacitance	C_I	V_{IN} = V_{CC} or GND	See Figure 17	25°C	2.5 V		2.6		pF
Bandwidth	BW	R_L = 50 Ω, –3 dB	See Figure 20	25°C	2.5 V		17		MHz

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the *Implications of Slow or Floating CMOS Inputs* application report, SCBA004.

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Electrical Characteristics—2.5-V Supply (continued)

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to +125°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Off-state isolation	O_{ISO}	R_L = 50 Ω	f = 100 kHz, See Figure 21	25°C	2.5 V		–66		dB
Crosstalk	X_{TALK}	R_L = 50 Ω	f = 100 kHz, See Figure 22	25°C	2.5 V		–75		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 35 pF	f = 20 Hz to 20 kHz, See Figure 24	25°C	2.5 V		0.01		%
SUPPLY									
Positive supply current	I_{CC}	V_{COM} and V_{IN} = V_{CC} or GND, V_{NC} and V_{NO} = floating		25°C	2.7 V		0.2	1.1	µA
				–40°C to +125°C				1.3	
		V_{COM} = V_{CC} – 5.5 V, V_{IN} = V_{CC} or GND, V_{NC} and V_{NO} = floating		–40°C to +125°C	2.7 V			3.3	µA

6.6 Electrical Characteristics—3.3-V Supply

V_{CC} = 3 V to 3.6 V, T_A = –40°C to +125°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
Analog signal	V_{COM} V_{NO} V_{NC}					V_{CC} – 5.5		V_{CC}	V
On-state resistance	R_{on}	V_{NC} or V_{NO} ≤ V_{CC}, 1.5 V, V_{CC} – 5.5 V, I_{COM} = –100 mA	COM to NO or NC, See Figure 14	25°C	3 V		0.61	0.87	Ω
				–40°C to +125°C				0.97	
On-state resistance match between channels	ΔR_{on}	V_{NC} or V_{NO} = 1.5 V, I_{COM} = –100 mA	COM to NO or NC, See Figure 14	25°C	3 V		0.024	0.13	Ω
				–40°C to +125°C				0.13	
On-state resistance flatness	$R_{on(flat)}$	V_{NC} or V_{NO} ≤ V_{CC}, 1.5 V, V_{CC} – 5.5 V, I_{COM} = –100 mA	COM to NO or NC, See Figure 14	25°C	3 V		0.12	0.46	Ω
				–40°C to +125°C				0.5	
Shunt switch resistance	R_{SH}	I_{NO} or I_{NC} = 10 mA		–40°C to +125°C	3 V		25	40	Ω
On-state leakage current	$I_{COM(ON)}$	V_{NC} and V_{NO} = floating, V_{COM} = V_{CC},V_{CC} – 5.5 V	COM to NO or NC, See Figure 16	25°C	3.6 V	–200		200	nA
				–40°C to +125°C		–2500		2500	
DIGITAL CONTROL INPUTS (IN)(2)									
Input logic high	V_{IH}			–40°C to +125°C		1.4		V_{CC}	V
Input logic low	V_{IL}			–40°C to +125°C				0.6	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = V_{CC} or 0		25°C	3.6 V	–250		250	nA
				–40°C to +125°C		–250		250	
DYNAMIC									
Turnon time	t_{ON}	V_{COM} = V_{CC}, R_L = 300 Ω	C_L = 35 pF, See Figure 18	25°C	3.3 V		34	80	ns
				–40°C to +125°C	3 V to 3.6 V			80	
Turnoff time	t_{OFF}	V_{COM} = V_{CC}, R_L = 300 Ω	C_L = 35 pF, See Figure 18	25°C	3.3 V		19	70	ns
				–40°C to +125°C	3 V to 3.6 V			70	
Break-before-make time	t_{BBM}		See Figure 19	25°C	3.3 V	1	7		ns
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 23	25°C	3.3 V		300		pC
On-State NC, NO, COM capacitance	$C_{COM(ON)}$	V_{COM} = V_{CC} or GND, f = 10 MHz	See Figure 17	25°C	3.3 V		370		pF

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the *Implications of Slow or Floating CMOS Inputs* application report, SCBA004.

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Electrical Characteristics—3.3-V Supply (continued)

V_{CC} = 3 V to 3.6 V, T_A = –40°C to +125°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Digital input capacitance	C_I	V_{IN} = V_{CC} or GND	See Figure 17	25°C	3.3 V		2.6		pF
Bandwidth	BW	R_L = 50 Ω, –3 dB	Switch ON, See Figure 20	25°C	3.3 V		17.5		MHz
Off-state isolation	O_{ISO}	R_L = 50 Ω	f = 100 kHz, See Figure 21	25°C	3.3 V		–68		dB
Crosstalk	X_{TALK}	R_L = 50 Ω	f = 100 kHz, See Figure 22	25°C	3.3 V		–76		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 35 pF	f = 20 Hz to 20 kHz, See Figure 24	25°C	3.3 V		0.008		%
SUPPLY									
Positive supply current	I_{CC}	V_{COM} and V_{IN} = V_{CC} or GND, V_{NC} and V_{NO} = floating		25°C	3.6 V		0.1	1.2	µA
				–40°C to +125°C				1.3	
		V_{COM} = V_{CC} – 5.5 V, V_{IN} = V_{CC} or GND, V_{NC} and V_{NO} = floating		–40°C to +125°C	3.6 V			3.4	µA

6.7 Electrical Characteristics—5-V Supply(1)

V_{CC} = 4.5 V to 5.5 V, T_A = –40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
Analog signal	V_{COM}, V_{NO}, V_{NC}					V_{CC} – 5.5		V_{CC}	V
On-state resistance	R_{on}	V_{NC} or V_{NO} = V_{CC}, 1.6 V, V_{CC} = –5.5 V, I_{COM} = –100 mA	COM to NO or NC, See Figure 14	25°C	4.5 V		0.52	0.74	Ω
				–40°C to +125°C				0.83	
On-state resistance match between channels	ΔR_{on}	V_{NC} or V_{NO} = 1.6 V, I_{COM} = –100 mA	COM to NO or NC, See Figure 14	25°C	4.5 V		0.04	0.23	Ω
				–40°C to +125°C				0.30	
On-state resistance flatness	$R_{on(flat)}$	V_{NC} or V_{NO} = V_{CC}, 1.6 V, V_{CC} = –5.5 V, I_{COM} = –100 mA	COM to NO or NC, See Figure 14	25°C	4.5 V		0.076	0.46	Ω
				–40°C to +125°C				0.5	
Shunt switch resistance	R_{SH}	I_{NO} or I_{NC} = 10 mA		–40°C to +125°C	4.5 V		16	36	Ω
On-state leakage current	$I_{COM(ON)}$	V_{NC} and V_{NO} = Floating, V_{COM} = VCC, V_{CC} – 5.5 V	See Figure 16	25°C	5.5 V	–200		200	nA
				–40°C to +125°C		–2500		2500	
DIGITAL CONTROL INPUTS (IN)(2)									
Input logic high	V_{IH}			–40°C to +125°C		2.4		V_{CC}	V
Input logic low	V_{IL}			–40°C to +125°C				0.8	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = V_{CC} or 0		25°C	5.5 V	–250		250	nA
				–40°C to +125°C		–250		250	
DYNAMIC									
Turnon time	t_{ON}	V_{COM} = V_{CC}, R_L = 300 Ω	C_L = 35 pF, See Figure 18	25°C	5 V		27	80	ns
				–40°C to +125°C	4.5 V to 5.5 V			80	
Turnoff time	t_{OFF}	V_{COM} = V_{CC}, R_L = 300 Ω	C_L = 35 pF, See Figure 18	25°C	5 V		13	70	ns
				–40°C to +125°C	4.5 V to 5.5 V			70	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_{CC}/2 R_L = 300 Ω	C = 35 pF, See Figure 19	25°C	5 V	1	3.5		ns
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0	C_L = 1$_L$ nF, See Figure 23	25°C	5 V		500		pC

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the *Implications of Slow or Floating CMOS Inputs* application report, SCBA004.

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Electrical Characteristics—5-V Supply(1) (continued)

V_{CC} = 4.5 V to 5.5 V, T_A = –40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ON-State NC, NO, COM capacitance	$C_{COM(ON)}$	V_{COM} = V_{CC} or GND	See Figure 17	25°C	5 V		370		pF
Digital input capacitance	C_I	V_{IN} = V_{CC} or GND	See Figure 17	25°C	5 V		2.6		pF
Bandwidth	BW	R_L = 50 Ω	See Figure 20	25°C	5 V		18.3		MHz
Off-state isolation	O_{ISO}	R_L = 50 Ω	f = 100 kHz, See Figure 21	25°C	5 V		–70		dB
Crosstalk	X_{TALK}	R_L = 50 Ω	f = 100 kHz, See Figure 22	25°C	5 V		–78		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 35 pF	f = 20 Hz to 20 kHz, See Figure 24	25°C	5 V		0.009		%
SUPPLY									
Positive supply current	I_{CC}	V_{COM} and V_{IN} = V_{CC} or GND, V_{NC} or V_{NO} = floating		25°C	5.5 V		0.2	1.3	μA
				–40°C to +125°C				3.5	
		V_{COM} = V_{CC} – 5.5 V, V_{IN} = V_{CC} or GND, V_{NC} or V_{NO} = floating		–40°C to +125°C				5	

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6.8 Typical Characteristics

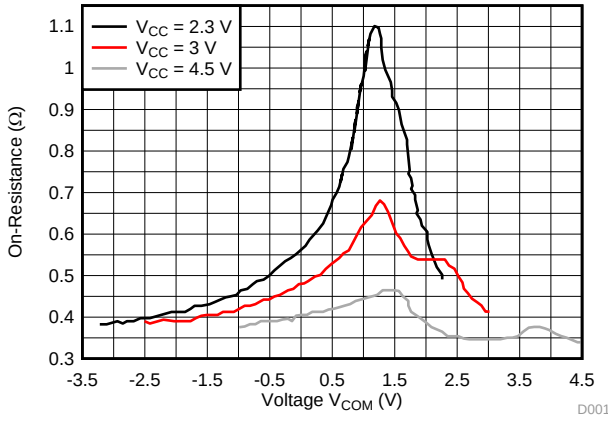


Figure 1. On-Resistance vs Voltage V_{COM}

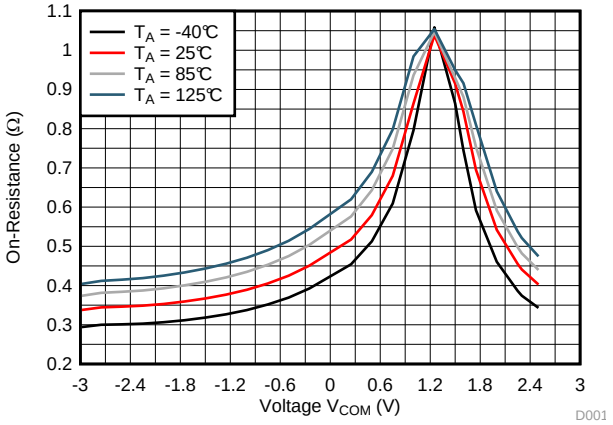


Figure 2. On-Resistance vs Voltage V_{COM} (V_{CC} = 2.3 V)

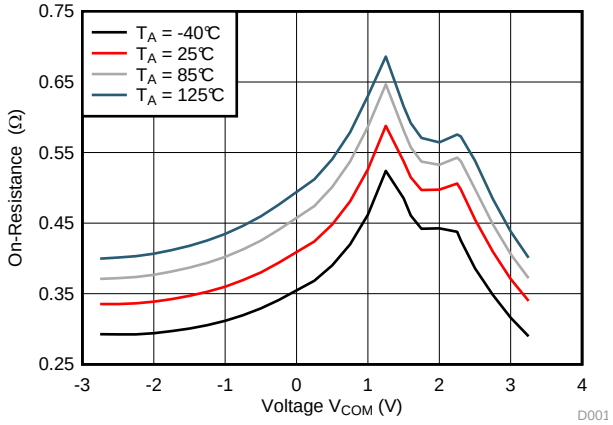


Figure 3. On-Resistance vs Voltage V_{COM} (V_{CC} = 3 V)

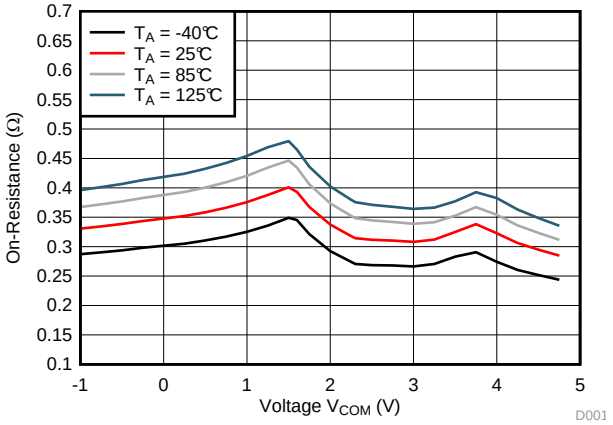


Figure 4. On-Resistance vs Voltage V_{COM} (V_{CC} = 4.5 V)

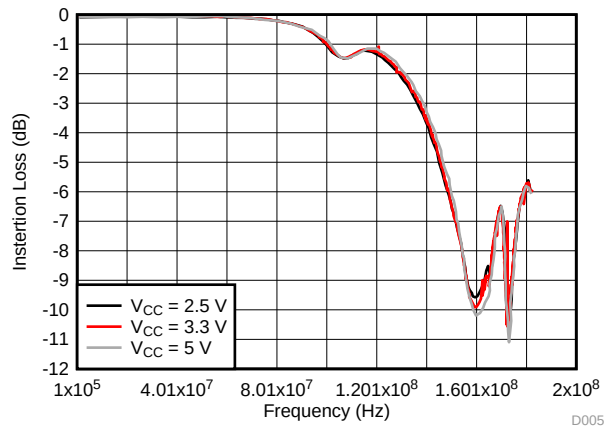


Figure 5. Insertion Loss vs Frequency for Varying V_{CC}

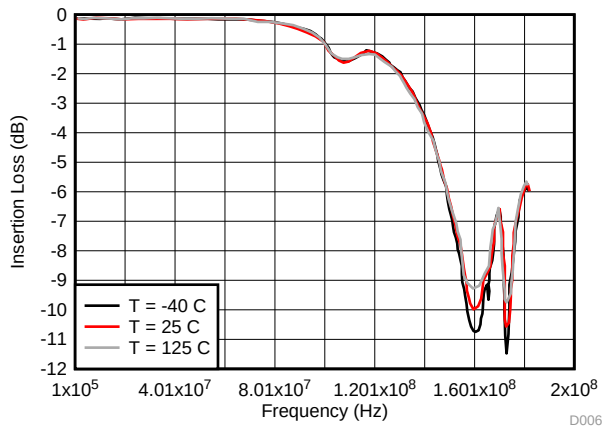


Figure 6. Insertion Loss vs Frequency for Varying Temperature

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Typical Characteristics (continued)

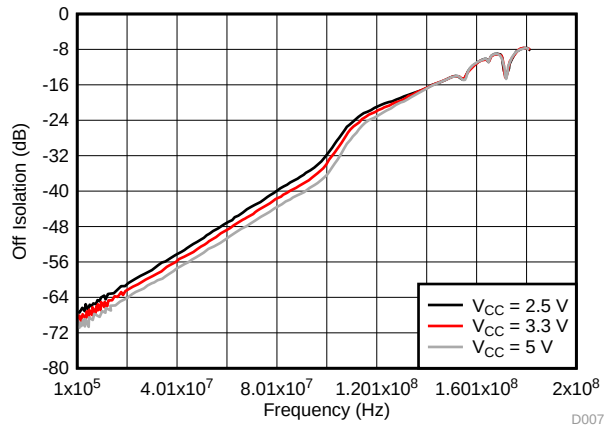


Figure 7. Off Isolation vs Frequency for Varying V_{CC}

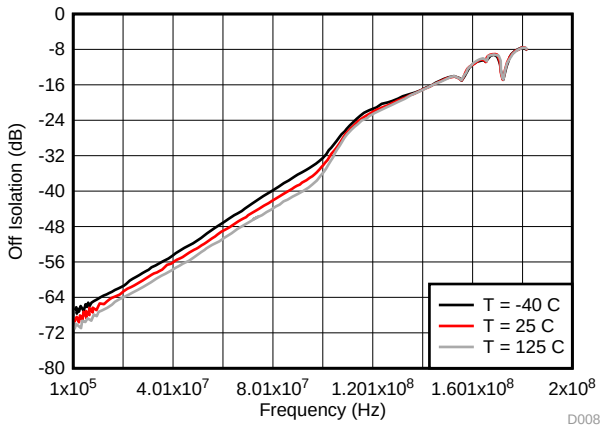


Figure 8. Off Isolation vs Frequency for Varying Temperature

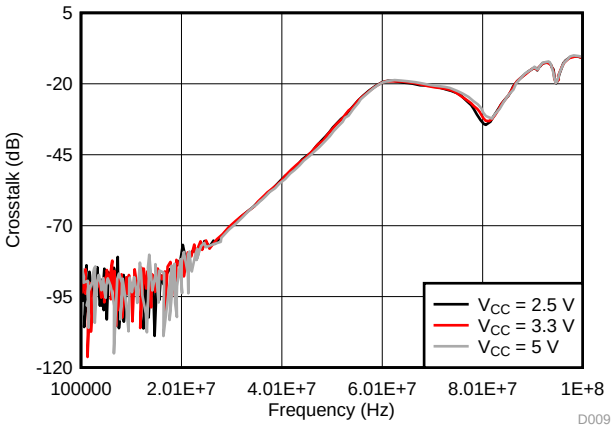


Figure 9. Crosstalk vs Frequency for Varying V_{CC}

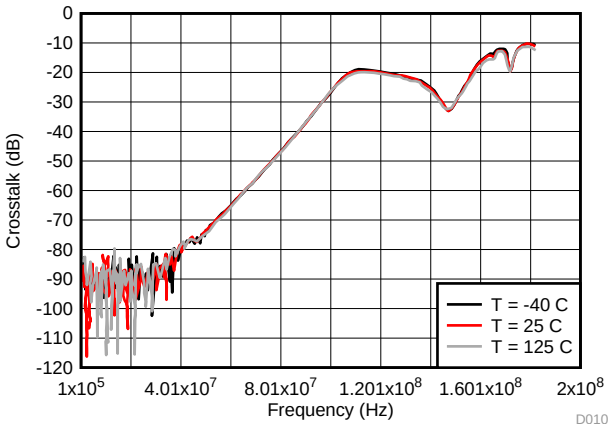


Figure 10. Crosstalk vs Frequency (V_{CC} = 3.3 V)

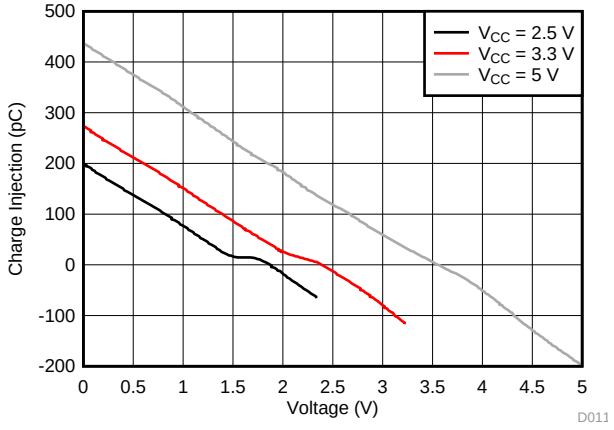


Figure 11. Charge Injection vs Voltage V_{COM}

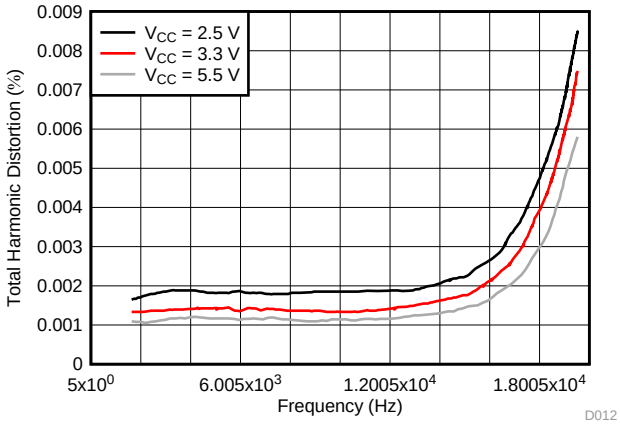
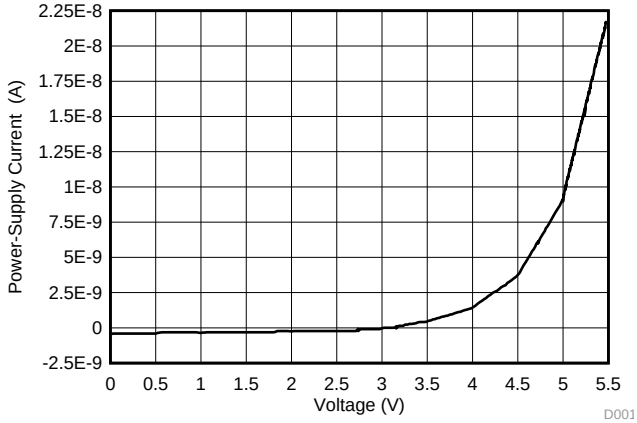


Figure 12. Total Harmonic Distortion vs Frequency

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Typical Characteristics (continued)



T = 25°C V_{NC} and V_{NO} = Floating V_{COM} and V_{IN} = GND

Figure 13. Power-Supply Current vs Voltage

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7 Parameter Measurement Information

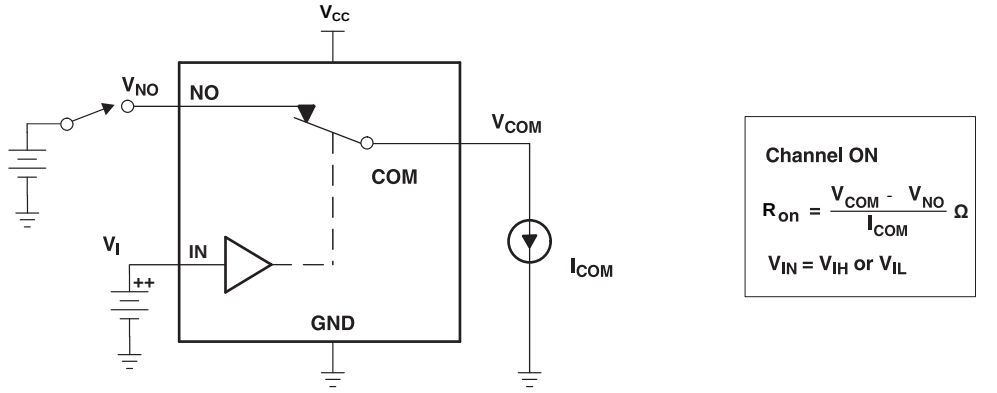


Figure 14. On-State Resistance (R_{on})

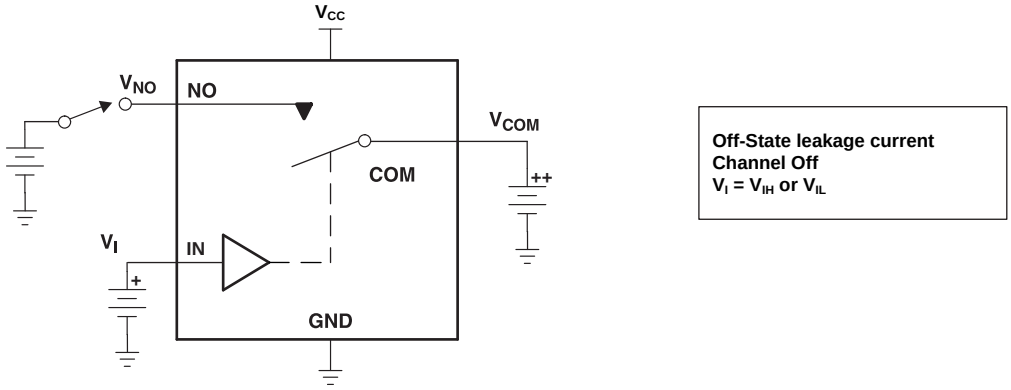


Figure 15. Off-State Leakage Current ($I_{COM(OFF)}$, $I_{NO(OFF)}$)

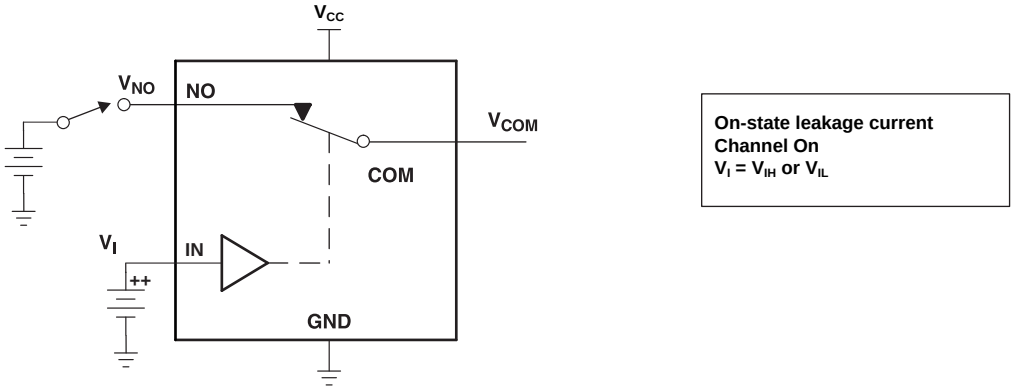


Figure 16. On-State Leakage Current ($I_{COM(ON)}$, $I_{NO(ON)}$)

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Parameter Measurement Information (continued)

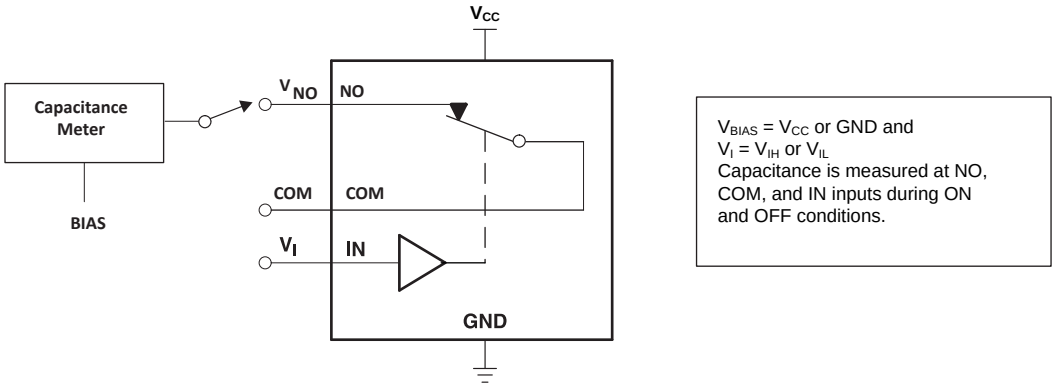
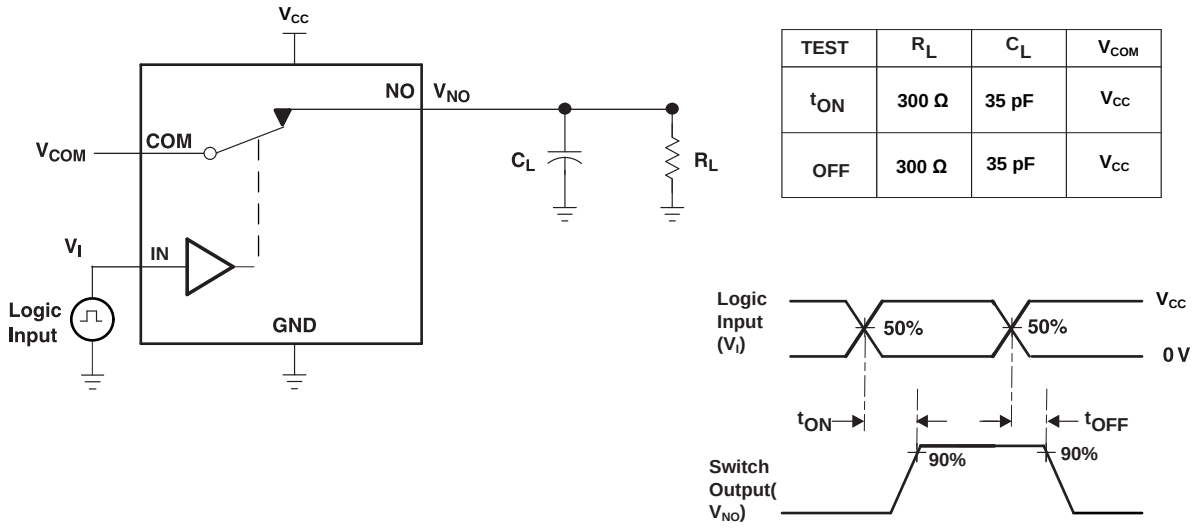


Figure 17. Capacitance (C_I, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NO(OFF)}$, $C_{NO(ON)}$)



TEST	R_L	C_L	V_{COM}
t_{ON}	300 Ω	35 pF	V_{CC}
OFF	300 Ω	35 pF	V_{CC}

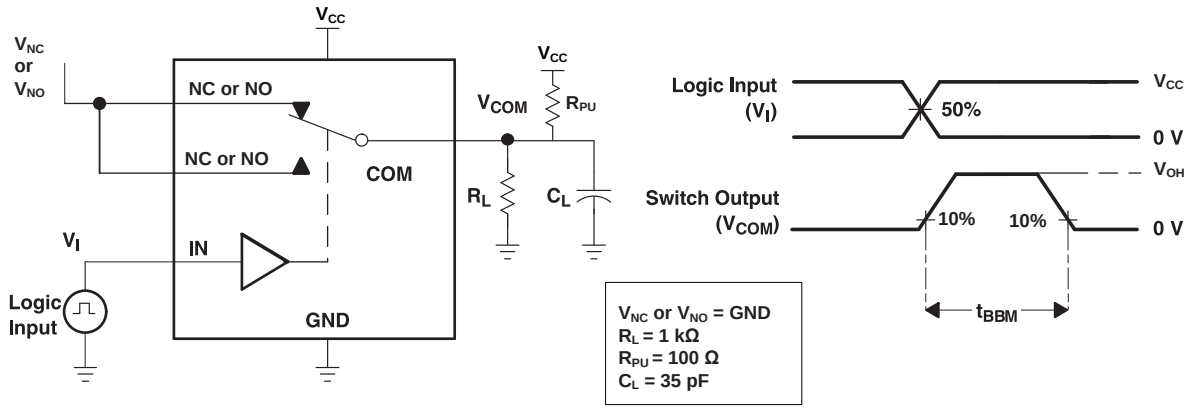
A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

Figure 18. Turnon (t_{ON}) and Turnoff time (t_{OFF})

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Parameter Measurement Information (continued)



A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

Figure 19. Break-Before-Make Time (t_{BBM})

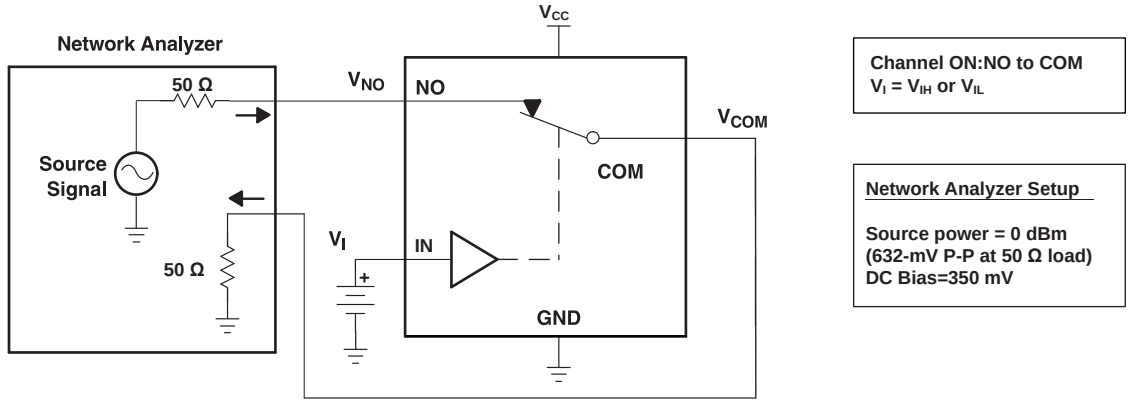


Figure 20. Bandwidth (BW)

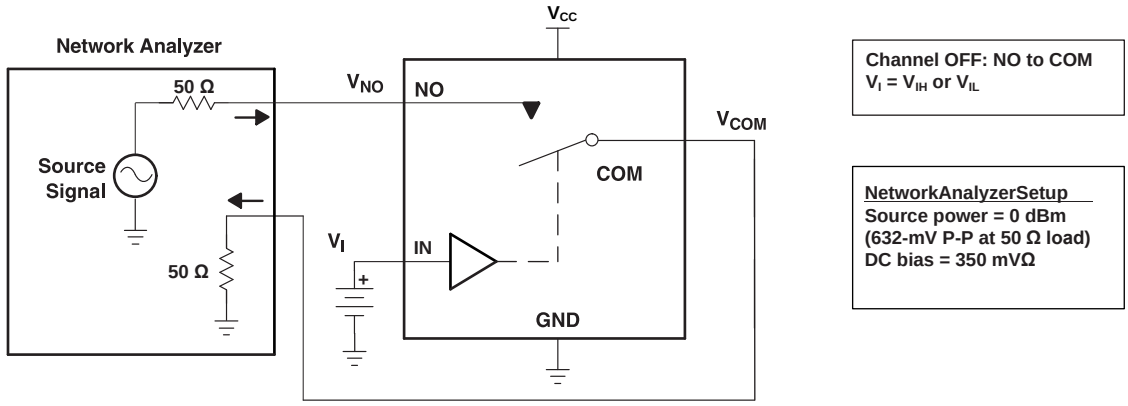


Figure 21. Off Isolation (O_{ISO})

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Parameter Measurement Information (continued)

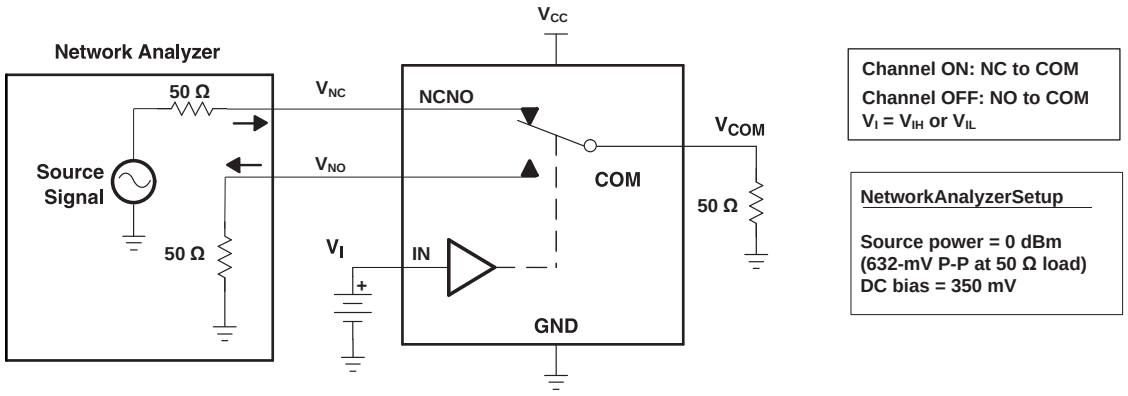
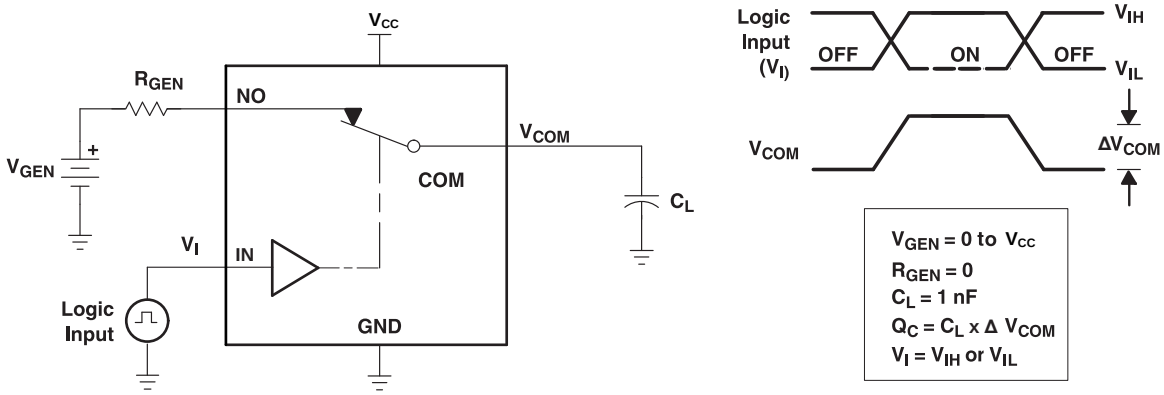


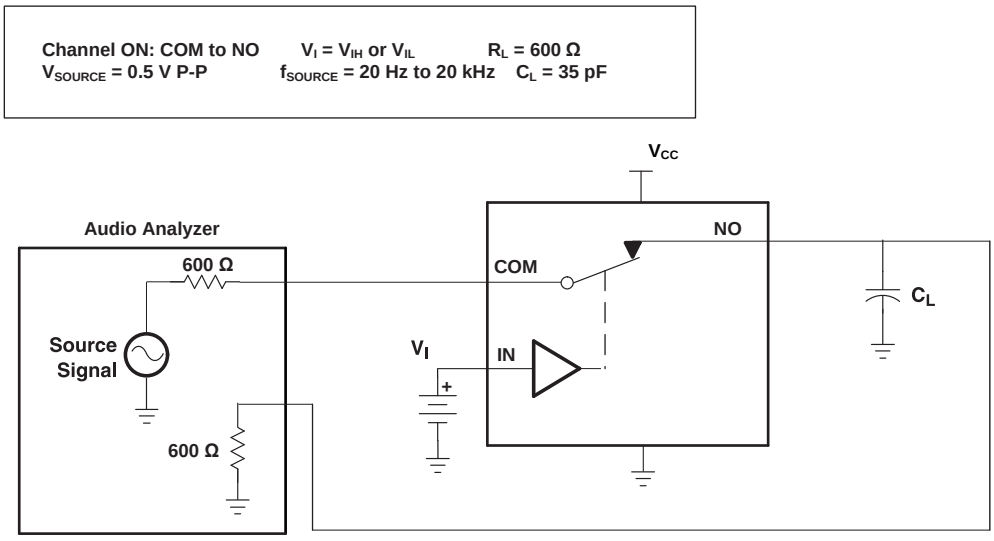
Figure 22. Crosstalk (X_{TALK})



A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

Figure 23. Charge Injection (Q_C)



A. C_L includes probe and jig capacitance.

Figure 24. Total Harmonic Distortion (THD)

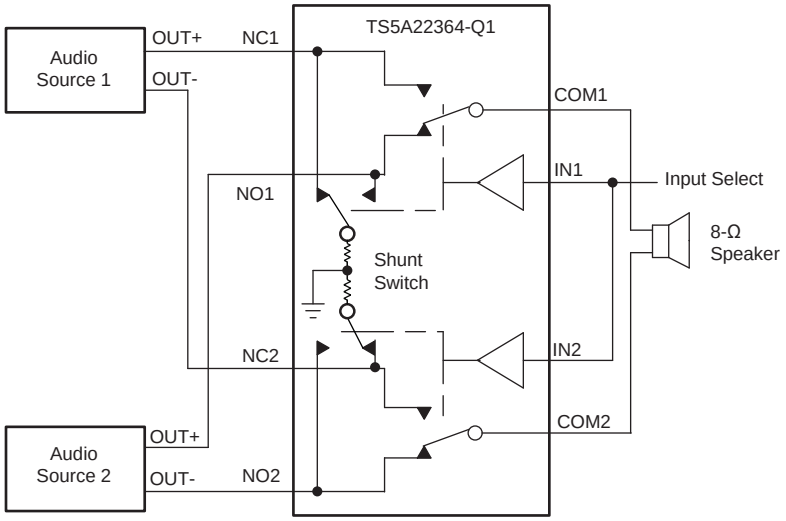
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8 Detailed Description

8.1 Overview

The TS5A22364-Q1 is a 2-channel single-pole double-throw (SPDT) analog switch designed to operate from 2.3-V to 5.5-V power supply. The device features negative signal swing capability that allows signals below ground to pass through the switch without distortion. Additionally, the TS5A22364-Q1 includes an internal shunt switch, which automatically discharges any capacitance at the NC or NO terminals when they are not connected to COM. This reduces the audible click-and-pop noise when switching between two sources. The break-before-make feature prevents signal distortion during the transferring of a signal from one path to another. Low On-state resistance, excellent channel-to-channel On-state resistance matching, and minimal total harmonic distortion (THD) performance are ideal for audio applications.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Click-and-Pop Reduction

The 50-Ω shunt switches on the TS5A22364-Q1 automatically discharge any capacitance at the NC or NO terminals when they are not connected to COM. This reduces the audible click-and-pop sounds that occur when switching between audio sources. Audible clicks and pops are caused when a step DC voltage is switched into the speaker. By automatically discharging the side that is not connected, any residual DC voltage is removed, thereby reducing the clicks and pops.

8.4 Device Functional Modes

Table 1 shows the function table for the TS5A22364-Q1.

Table 1. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Negative Signal Swing Capability

The TS5A22364-Q1 dual SPDT switches feature negative signal capability that allows signals below ground to pass through without distortion. These analog switches operate from a single 2.3-V to 5.5-V supply. The input and output signal swing of the device is dependant on the supply voltage V_{CC}: the device can pass signals as high as V_{CC} and as low as V_{CC} – 5.5 V, including signals below ground with minimal distortion. The Off state signal path (either NC or NO) during the operation of the TS5A22364-Q1 cannot handle negative DC voltage.

Table 2 shows the input-output signal swing the user can get with different supply voltages.

Table 2. Input-Output Signal Swing

SUPPLY VOLTAGE, VCC	MINIMUM (V_{NC}, V_{NO}, V_{COM}) = V_{CC} – 5.5	MAXIMUM (V_{NC}, V_{NO}, V_{COM}) = V_{CC}	MINIMUM (V_{NC}, V_{NO}, V_{COM}) = V_{CC} – 5.5	MAXIMUM (V_{NC}, V_{NO}, V_{COM}) = V_{CC}
	ON State signal path		OFF state signal path	
5.5 V	0 V	5.5 V	0 V	5.5 V
4.2 V	–1.3 V	4.2 V	0 V	4.2 V
3.3 V	–2.2 V	3.3 V	0 V	3.3 V
3 V	–2.5 V	3 V	0 V	3 V
2.5 V	–3 V	2.5 V	0 V	2.5 V

9.2 Typical Application

The 50-Ω shunt switches on the TS5A22364-Q1 automatically discharge any capacitance at the NC or NO terminals when they are unconnected to COM. This reduces audible click-and-pop sounds that occur when switching between audio sources. Audible clicks and pops are caused when a step DC voltage is switched into the speaker. By automatically discharging the side that is not connected, any residual DC voltage is removed, thereby reducing the clicks and pops. See Figure 25.

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Typical Application (continued)

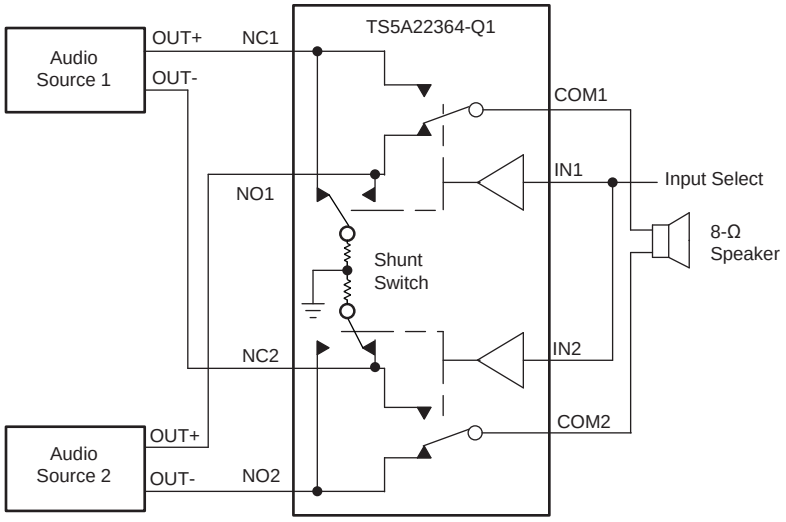


Figure 25. Shunt Switch Block Diagram

9.2.1 Design Requirements

Tie the digitally controlled input select pins IN1 and IN2 to V_{CC} or GND to avoid unwanted switch states that could result if the logic control pins are left floating.

9.2.2 Detailed Design Procedure

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the TS5A22364-Q1 operates from a single 2.3-V to 5.5-V supply and the input-output signal swing of the device is dependant of the supply voltage V_{CC}. The device passes signals as high as V_{CC} and as low as V_{CC} – 5.5 V. Use Table 2 as a guide for selecting supply voltage based on the signal passing through the switch.

Limit the current through the shunt resistor so as not to exceed the ±20 mA.

Ensure that the device is powered up with a supply voltage on VCC before a voltage can be applied to the signal paths NC and NO.

9.2.3 Application Curve

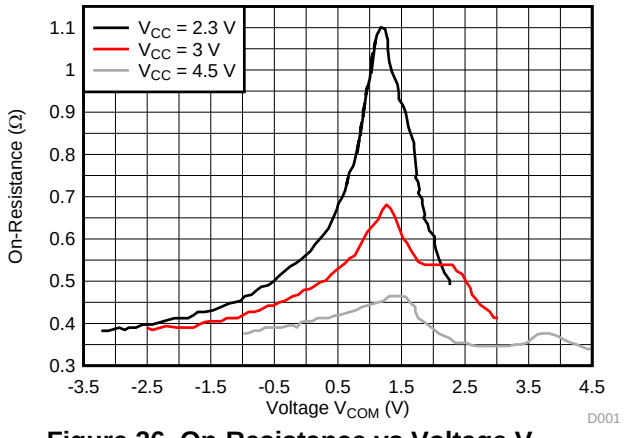


Figure 26. On-Resistance vs Voltage V_{COM}

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10 Power Supply Recommendations

The TS5A22364-Q1 operates from a single 2.3-V to 5.5-V supply. The device must be powered up with a supply voltage on VCC before a voltage can be applied to the signal paths NC and NO. It is recommended to include a 100 μs delay after VCC is at voltage before applying a signal on NC and NO paths.

It is also good practice to place a 0.1-μF bypass capacitor on the supply pin VCC to GND to smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

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11 Layout

11.1 Layout Guidelines

It is recommended to place a bypass capacitor as close to the supply pin VCC as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

Minimize trace lengths and vias on the signal paths in order to preserve signal integrity.

11.2 Layout Example

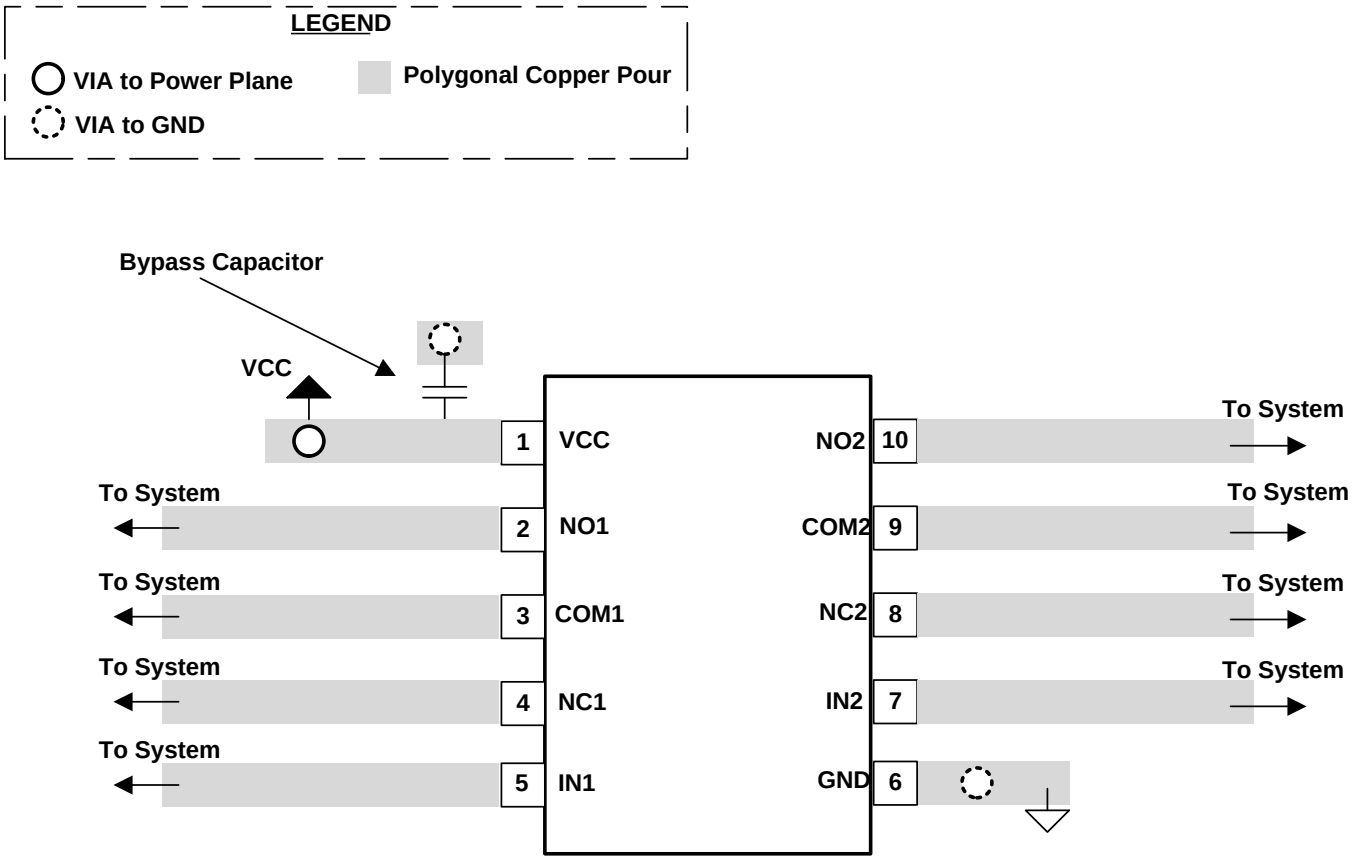


Figure 27. Layout Example of TS5A22364-Q1

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12 器件和文档支持

12.1 接收文档更新通知

如需接收文档更新通知，请访问 ti.com 上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。要获得这份数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS5A22364QDGSRQ1	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SJN
TS5A22364QDGSRQ1.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SJN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TS5A22364-Q1 :

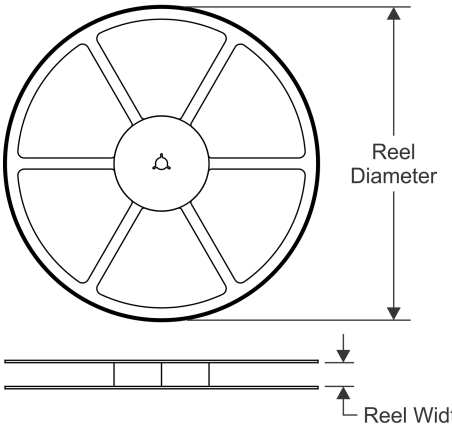
- Catalog : TS5A22364

NOTE: Qualified Version Definitions:

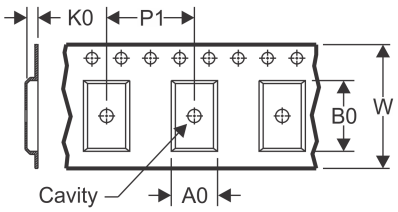
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

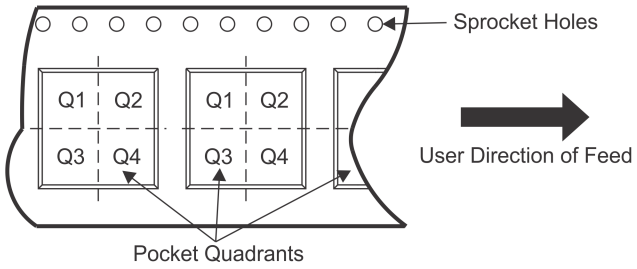


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

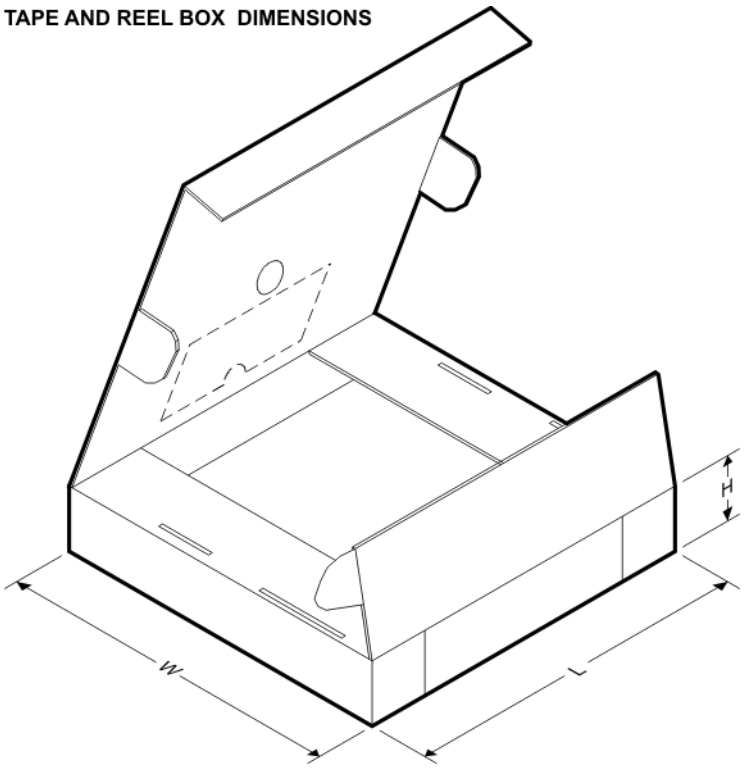
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A22364QDGSRQ1	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

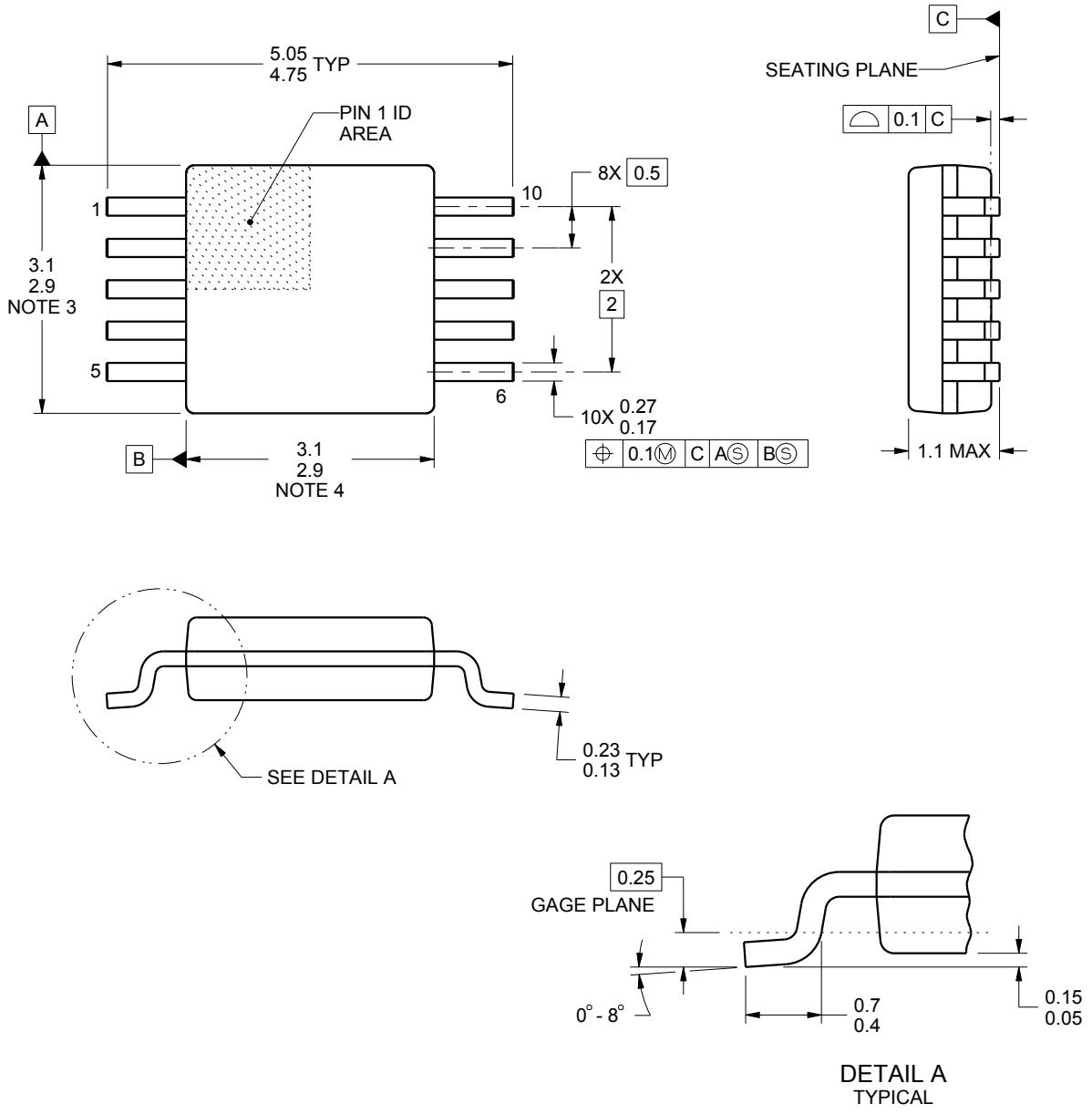
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A22364QDGSRQ1	VSSOP	DGS	10	2500	366.0	364.0	50.0

PACKAGE OUTLINE

DGS0010A

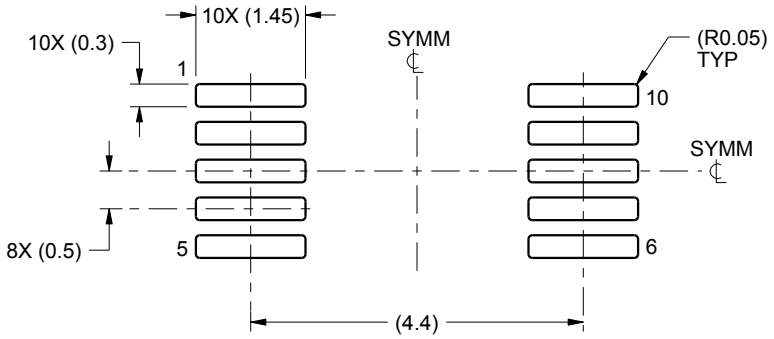
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

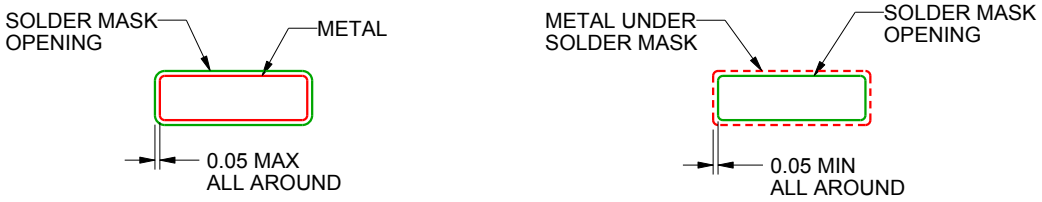


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

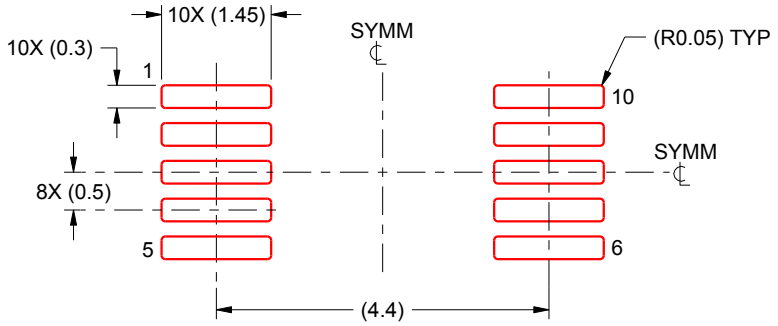


SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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