TS3USB3031 双通道、1:3、USB 2.0 高速 (480Mbps) 和移动高清链路 (MHL) 或移动显示端口 (MyDP) 开关

1 特性

- V_{CC} 范围：2.5V 至 4.3V
- 移动高清链路 (MHL) 或移动显示端口 (MyDP) 开关：
  - 带宽（–3dB）：6.5GHz
  - R_{ON}（典型值）：5.5Ω
  - C_{ON}（典型值）：1.3pF
- USB 开关（2 组）：
  - 带宽（–3dB）：6.5GHz
  - R_{ON}（典型值）：4.5Ω
  - C_{ON}（典型值）：1pF
- 电流消耗：28μA（典型值）
- 专有特性：
  - I_{OFF} 保护可防止在断电状态 (V_{CC} = 0V) 下产生漏电流
  - 1.8V 兼容控制输入 (SEL)
  - 所有 I/O 引脚上的过压容限 (OVT) 高达 5.5V，而且无需使用外部元件
- ESD 性能：
  - 2kV 人体放电模型（A114B，II 类）
  - 1kV 充电器件模型 (C101)
- 封装：
  - 12 引脚 VQFN 封装（1.8mm × 1.8mm，0.4mm 间距）

2 应用

- 智能手机
- 平板电脑
- 手机
- 便携式仪器
- 数码相机 USB 2.0 MHL

3 说明

TS3USB3031 器件为双通道、1:3 多路复用器，其中包括高速移动高清链路 (MHL)、移动显示端口 (MyDP) 开关和 USB 2.0 高速 (480Mbps) 开关。这些配置允许系统设计人员针对 MHL/MyDP 信号和两组 USB 数据使用通用 USB 或 Mico-USB 连接器，从而节省电路板空间且无需再使用多个连接器。MHL/MyDP 路径支持最新的 MHL 3.0 修订版本技术规格。

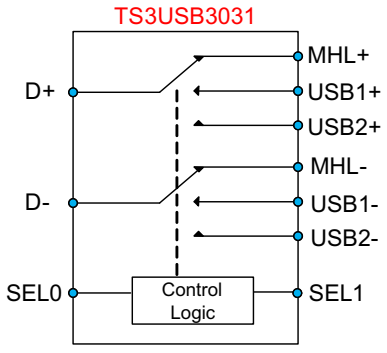
TS3USB3031 的 V_{CC} 范围为 2.5V 至 4.3V，支持过压容限 (OVT) 功能，允许 I/O 引脚承受过压条件（最高可达 5.5V）。断电保护特性在未加电时强制所有 I/O 引脚处于高阻抗模式，从而实现此类情况下信号线路的完全隔离而又不产生过多的漏电流。TS3USB3031 的选择引脚与 1.8V 控制电压兼容，允许它们直接与移动处理器的通用 I/O (GPIO) 相连，而无需额外的电压电平转换电路。

TS3USB3031 采用小型 1.8mm × 1.8mm 12 引脚 VQFN 封装，专为移动应用而设计。

封装信息

器件型号	封装(1)	封装大小(2)
TS3USB3031	RMG（VQFN，12）	1.8mm × 1.8mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



开关图

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4 Pin Configuration and Functions

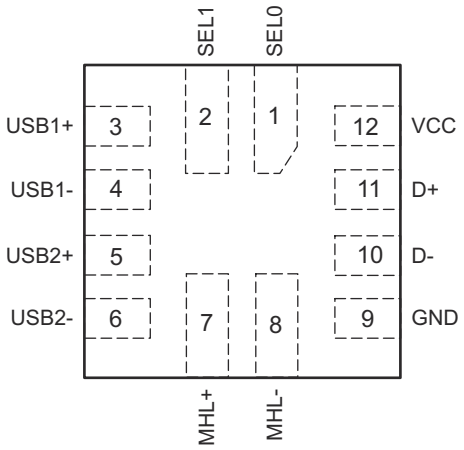


图 4-1. RMG Package, 12-Pin VQFN (Top View)

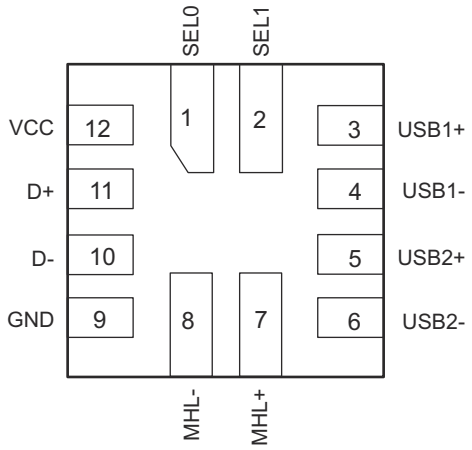


图 4-2. RMG Package, 12-Pin VQFN (Bottom View)

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
SEL0	1	I	Digital control Input
SEL1	2	I	Digital control Input
USB1+	3	I/O	Differential signal path 1
USB1 –	4	I/O	Differential signal path 1
USB2+	5	I/O	Differential signal path 2
USB2 –	6	I/O	Differential signal path 2
MHL+	7	I/O	Differential signal path 3
MHL –	8	I/O	Differential signal path 3
GND	9	G	Ground
D –	10	I/O	Common Differential signal path
D+	11	I/O	Common Differential signal path
VCC	12	P	Power Supply

(1) G = Ground, I = Input, O = Output, P = Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(3)	– 0.3	5.5	V
$V_{I/O}$	Input/Output DC voltage(3)	– 0.3	5.5	V
I_K	Input/Output port diode current (VI/O < 0)	– 50		mA
V_I	Digital input voltage (SEL0, SEL1)	– 0.3	5.5	
I_{IK}	Digital logic input clamp current (VI < 0)(3)	– 50		mA
$I_{I/O}$	Continuous switch DC output current (USB and MHL)		60	mA
T_{stg}	Storage temperature	– 65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±1000 V may actually have higher performance.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.5	4.3	V
$V_{I/O\ (USB)}$, $V_{I/O\ (MHL)}$	Analog voltage	0	3.6	V
V_I	Digital input voltage (SEL0, SEL1)	0	V_{CC}	V
$T_{RAMP\ (VCC)}$	Power supply ramp time requirement (VCC)	100	1000	µs/V
$I_{I/O,\ PEAK}$	Peak switch DC output current (1-ms duration pulse at <10% duty cycle)		150	mA
T_A	Operating free-air temperature	– 40	85	°C

5.4 Thermal Information

THERMAL METRIC(1)		TS3USB3031 RMG (VQFN) 12 PINS	UNIT
$R_{\theta\ JA}$	Junction-to-ambient thermal resistance	160.8	°C/W
$R_{\theta\ JC(top)}$	Junction-to-case (top) thermal resistance	95.5	°C/W
$R_{\theta\ JB}$	Junction-to-board thermal resistance	91.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.4	°C/W

THERMAL METRIC(1)		TS3USB3031 RMG (VQFN) 12 PINS	UNIT
ψ_{JB}	Junction-to-board characterization parameter	91.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

T_A = –40°C to 85°C, typical values are at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MHL SWITCH						
R_{ON}	ON-state resistance	V_{CC} = 2.5 V, $V_{I/O}$ = 1.5V, I_{ON} = –8 mA (see 图 6-1)		5.5	7	Ω
ΔR_{ON}	ON-state resistance match between + and – paths	V_{CC} = 2.5 V, $V_{I/O}$ = 1.5 V, I_{ON} = –8 mA		0.1		Ω
$R_{ON (FLAT)}$	ON-state resistance flatness	V_{CC} = 2.5 V, $V_{I/O}$ = 1.5 V to 3.3 V, I_{ON} = –8 mA		1		Ω
I_{OZ}	OFF leakage current	V_{CC} = 4.3 V, Switch OFF, $V_{MHL+/MHL-}$ = 1.5 V to 3.3 V, $V_{D+/D-}$ = 0 V (see 图 6-2)	–2		2	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0 V, Power off, $V_{MHL+/MHL-}$ = 1.5 V to 3.3 V, $V_{D+/D-}$ = NC	–10		10	µA
I_{ON}	ON leakage current	V_{CC} = 4.3 V, Switch ON, $V_{MHL+/MHL-}$ = 1.5 V to 3.3 V, $V_{D+/D-}$ = NC	–2		2	µA
USB SWITCH (USB1 and USB2)						
R_{ON}	ON-state resistance	V_{CC} = 2.5 V, $V_{I/O}$ = 0.4 V, I_{ON} = –8 mA (see 图 6-1)		4.5	6	Ω
ΔR_{ON}	ON-state resistance match between + and – paths	V_{CC} = 2.5 V, $V_{I/O}$ = 0.4 V, I_{ON} = –8 mA		0.1		Ω
$R_{ON (FLAT)}$	ON-state resistance flatness	V_{CC} = 2.5 V, $V_{I/O}$ = 0 V to 0.4 V, I_{ON} = –8 mA		1		Ω
I_{OZ}	OFF leakage current	V_{CC} = 4.3 V, Switch OFF, $V_{USB+/USB-}$ = 0 V to 0.4 V, $V_{D+/D-}$ = 0 V (see 图 6-2)	–2		2	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0 V, Switch ON or OFF, $V_{USB+/USB-}$ = 0 V to 0.4 V, $V_{D+/D-}$ = NC	–10		10	µA
I_{ON}	ON leakage current	V_{CC} = 4.3 V, Switch ON, $V_{USB+/USB-}$ = 0 V to 0.4 V, $V_{D+/D-}$ = NC	–2		2	µA
DIGITAL CONTROL INPUTS (SEL)						
V_{IH}	Input logic high	V_{CC} = 2.5 V to 4.3 V	1.3			V
V_{IL}	Input logic low	V_{CC} = 2.5 V to 4.3 V			0.6	V
I_{IN}	Input leakage current	V_{CC} = 4.3 V, $V_{I/O}$ = 0 V to 3.6 V, V_{IN} = 0 V to 4.3 V	–10		10	µA

5.6 Dynamic Characteristics

T_A = –40°C to 85°C, Typical values are at V_{CC} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay	R_L = 50 Ω, CL = 5 pF, V_{CC} = 2.5 V to 4.3 V, $V_{I/O(USB)}$ = 0.4 V, $V_{I/O(MHL)}$ = 3.3 V		50		ps
t_{switch}	Switching time between USB/MHL channels in active modes	R_L = 50 Ω, CL = 5 pF, V_{CC} = 2.5 V to 4.3 V, $V_{I/O(USB)}$ = 0.4 V, $V_{I/O(MHL)}$ = 3.3 V			400	ns
t_{ON}	Switch turnon time (from disabled to active mode)	R_L = 50 Ω, CL = 5 pF, V_{CC} = 2.5 V to 4.3 V, $V_{I/O(USB)}$ = 0.4 V, $V_{I/O(MHL)}$ = 3.3 V			100	µs
t_{OFF}	Switch turnoff time (from active to disabled mode)	R_L = 50 Ω, CL = 5 pF, V_{CC} = 2.5 V to 4.3 V, $V_{I/O(USB)}$ = 0.4 V, $V_{I/O(MHL)}$ = 3.3 V			100	µs
$C_{ON(MHL)}$	MHL path, ON capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 V or 3.3 V, f = 240 MHz, Switch ON		1.3		pF

T_A = –40°C to 85°C, Typical values are at V_{CC} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{ON(USB)}$	USB1 and USB2 paths, ON capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 V or 3.3 V, f = 240 MHz, Switch ON		1		pF
$C_{OFF(MHL)}$	MHL path, OFF capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 V or 3.3 V, f = 240 MHz, Switch OFF		1		pF
$C_{OFF(USB)}$	USB1 and USB2 paths, OFF capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 V or 3.3 V, f = 240 MHz, Switch OFF		0.8		pF
C_I	Digital input capacitance	V_{CC} = 3.3 V, V_I = 0 V or 2 V		2.2		pF
$O_{ISO\ (MHL)}$	MHL path, OFF isolation	V_S = –10 dBm, V_{DC_BIAS} = 2.4 V, RT = 50 Ω, f = 240 MHz (see 图 6-3), Switch OFF		–38		dB
$O_{ISO\ (USB)}$	USB path, OFF isolation	V_S = –10 dBm, V_{DC_BIAS} = 0.2 V RT = 50 Ω, f = 240 MHz (see 图 6-3), Switch OFF		–38		dB
$X_{TALK\ (MHL)}$	MHL channel crosstalk	V_S = –10 dBm, V_{DC_BIAS} = 2.4 V, RT = 50 Ω, f = 240 MHz (see 图 6-4), Switch ON		–41		dB
$X_{TALK\ (USB)}$	USB channel crosstalk	V_S = –10 dBm, V_{DC_BIAS} = 0.2 V, RT = 50 Ω, f = 240 MHz (see 图 6-4), Switch ON		–38		dB
$BW_{(MHL)}$	MHL path, –3-dB bandwidth	V_{CC} = 2.5 V to 4.3 V, R_L = 50 Ω (see 图 6-5), Switch ON		6.5		GHz
$BW_{(USB)}$	USB path, –3-dB bandwidth	V_{CC} = 2.5 V to 4.3 V, R_L = 50Ω (See 图 6-5), Switch ON		6.5		GHz
SUPPLY						
V_{CC}	Power supply voltage		2.5		4.3	V
I_{CC}	Positive supply current	V_{CC} = 4.3 V, V_{IN} = V_{CC} or GND, $V_{I/O}$ = 0 V, Switch ON or OFF		28	40	µA

5.7 Typical Characteristics

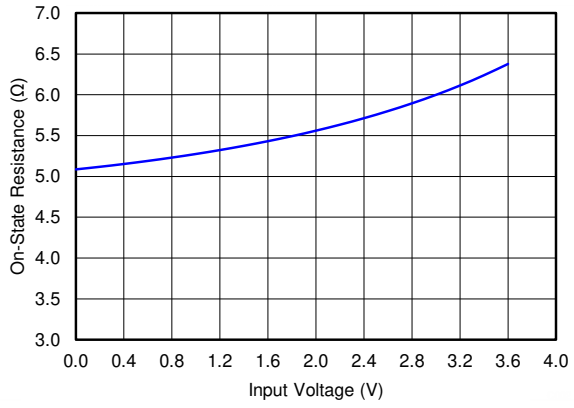


图 5-1. ON-Resistance vs $V_{I/O}$ for MHL Switch

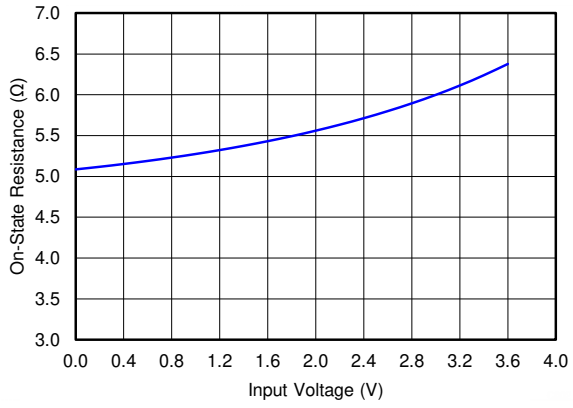


图 5-2. ON-Resistance vs $V_{I/O}$ for USB Switch

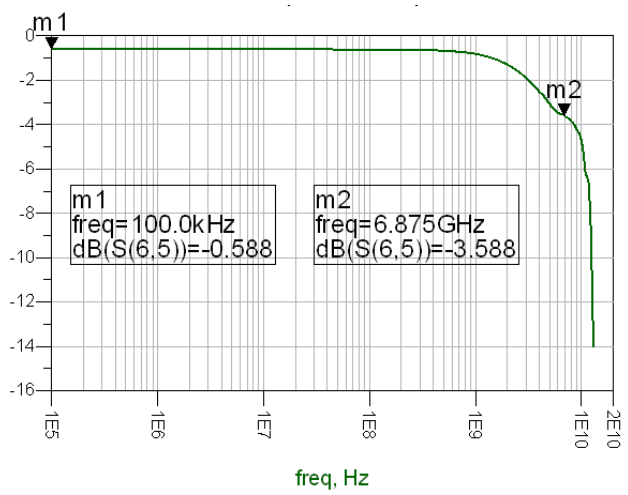


图 5-3. Bandwidth for MHL Switch

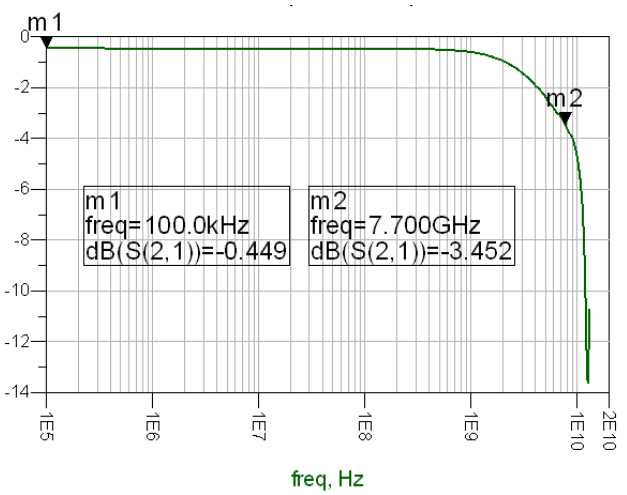


图 5-4. Bandwidth for USB Switch

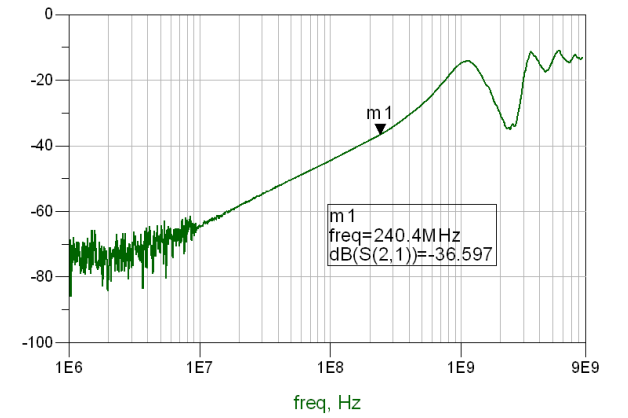


图 5-5. OFF Isolation vs Frequency for MHL Path

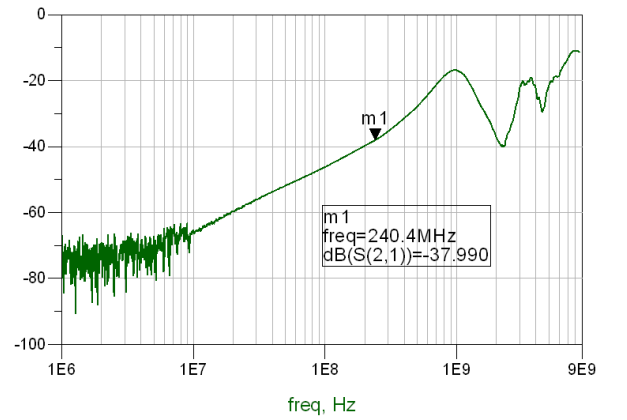


图 5-6. OFF Isolation vs Frequency for USB Path

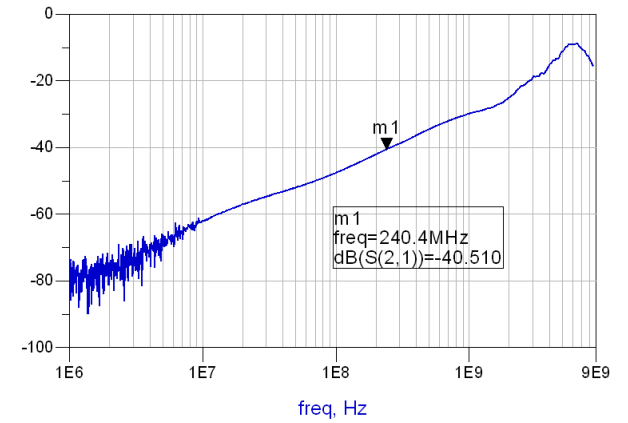


图 5-7. Cross Talk vs Frequency for MHL Path

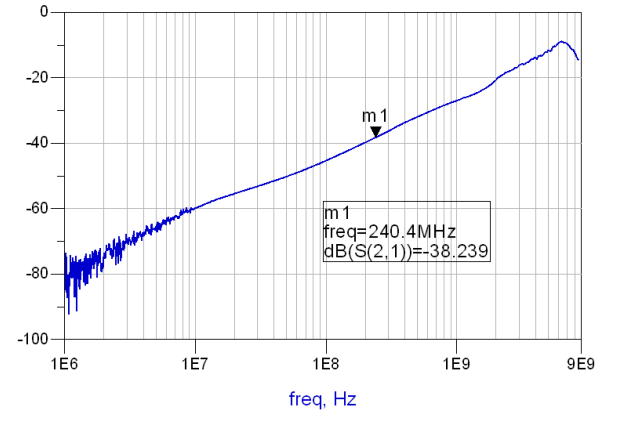


图 5-8. Cross Talk vs Frequency for USB Path

Parameter Measurement Information

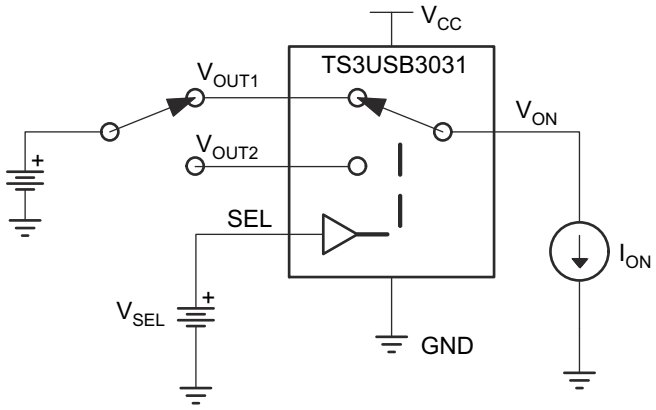


图 6-1. ON-State Resistance (R_{ON})

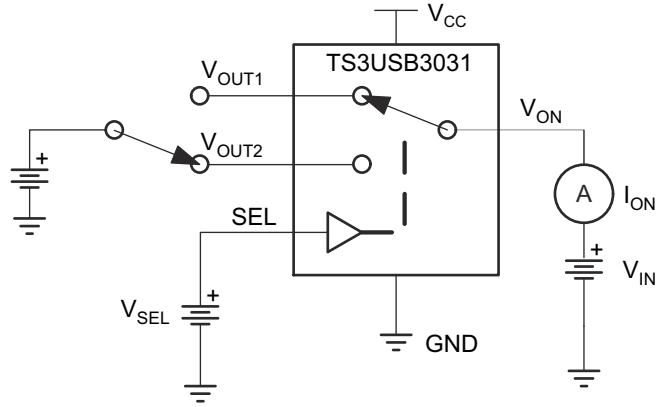


图 6-2. OFF Leakage Current (I_{OZ})

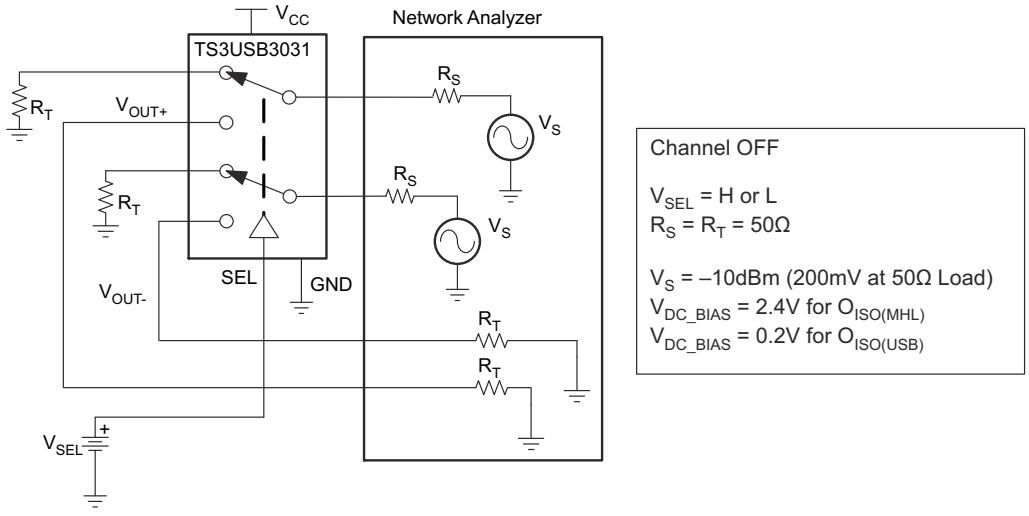


图 6-3. Differential Off-Isolation (O_{ISO})

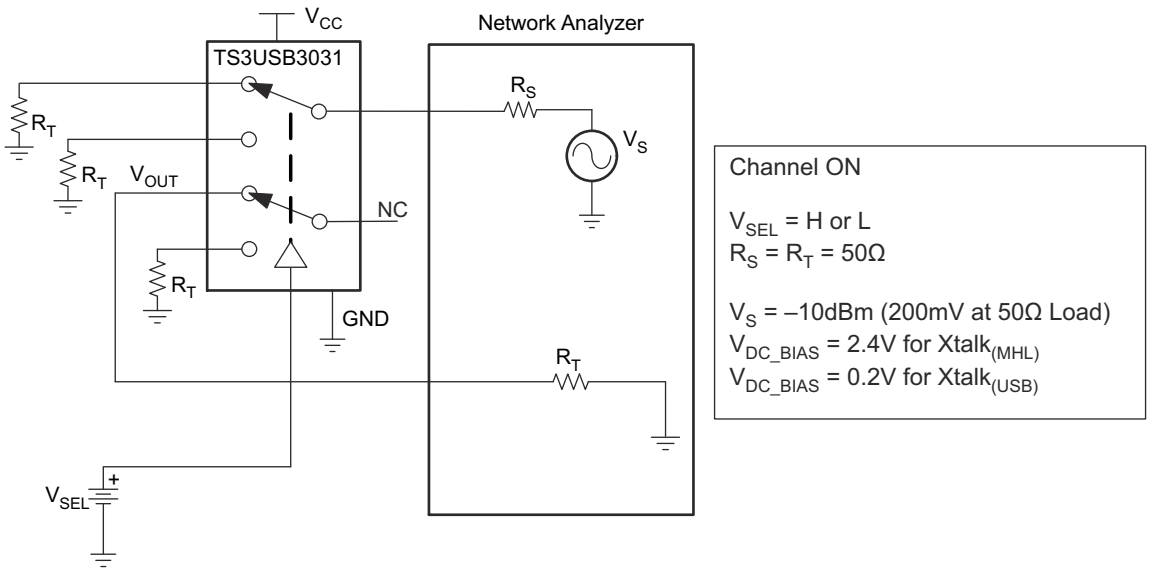


图 6-4. Crosstalk (Xtalk)

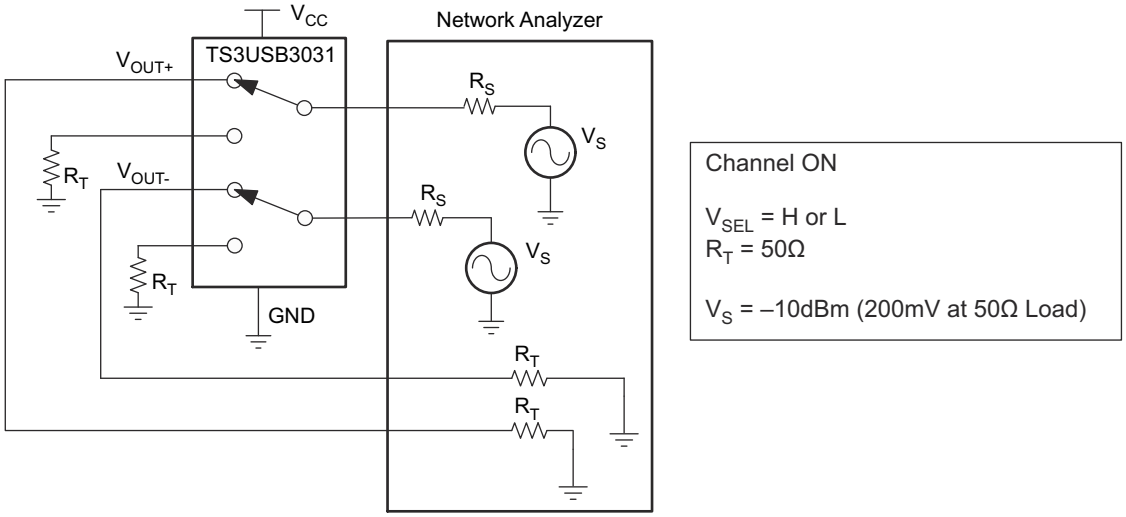


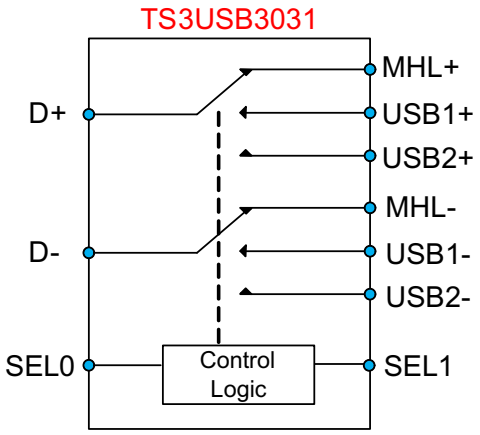
图 6-5. Differential Bandwidth (BW)

6 Detailed Description

6.1 Overview

The TS3USB3031 device is a 2-channel, 1:3 multiplexer that includes a high-speed Mobile High-Definition Link (MHL) or Mobility Display Port (MyDP) switch and USB 2.0 High-Speed (480 Mbps) switches in the same package. This device is used in many high-speed differential 1:3 mux applications.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 I_{OFF} Protection

I_{OFF} protection prevents current leakage through the device when V_{cc} = 0 V This allows signals to be present on the D± and USB/MHL± pins before the device is powered up without damaging the device or system.

6.3.2 1.8-V Compatible Logic

The TS3USB3031 device supports 1.8-V logic irrespective to the supply voltage applied to the IC.

6.3.3 Overvoltage Tolerant (OVT)

The D± and USB/MHL± pins of the device can support signals up to 5.5 V without damaging the device. This protects the TS3USB3031 in case the VBUS pin of the USB connector is shorted to the signal path without additional components added.

6.4 Device Functional Modes

表 6-1 lists the functional modes of the TS3USB3031.

表 6-1. Function Table

SEL1	SEL0	SWITCH STATUS
Low	Low	D+/D – connected to USB1+/USB1 –
Low	High	D+/D – connected to USB2+/USB2 –
High	Low	D+/D – connected to MHL+/MHL –
High	High	USB and MHL switches in High-Z

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

The TS3USB3031 is a passive, bidirectional, 2-channel 1:3 switch that can be used in many high speed 1:3 switching applications. This device was designed originally for USB 2.0 and Mobile High-Definition Link applications but can be used for general signal switching applications such as I^2C, UART, LVDS, and so forth.

7.2 Typical Application

图 7-1 represents a typical application of the TS3USB3031 MHL switch. The TS3USB3031 is used to switch signals between the two sets of USB paths, which go to either the baseband or application processor, and the MHL path, which goes to the HDMI to MHL bridge. The TS3USB3031 has internal 6-MΩ pulldown resistors on SEL0 and SEL1. The pulldown on SEL0 and SEL1 ensure the USB1 channel is selected by default. The TS5A3157 is a separate SPDT switch that is used to switch between the MHL CBUS and the USB ID line that is required for USB OTG (USB On-The-Go) application.

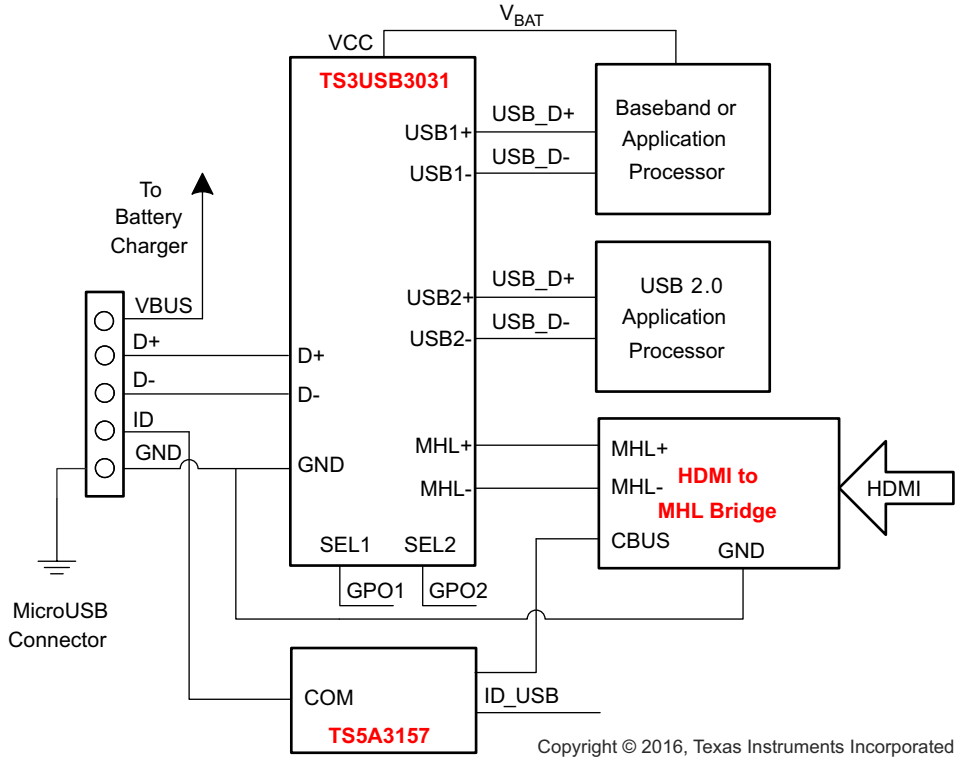


图 7-1. Typical TS3USB3031 Application

7.2.1 Design Requirements

Design requirements of the MHL and USB 1.0,1.1, and 2.0 standards must be followed.

The TS3USB3031 has internal 6-MΩ pulldown resistors on SEL0 and SEL1 so no external resistors are required on the logic pins. The pulldown on SEL0 and SEL1 ensure the USB1 channel is selected by default.

The TS5A3157 is a separate SPDT switch that is used to switch between the CBUS of the MHL and the USB ID line that is required for USB OTG (USB On-The-Go) application.

7.2.2 Detailed Design Procedure

The TS3USB3031 can be properly operated without any external components. However, TI recommends that unused signal I/O pins must be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device.

7.2.3 Application Curves

7.2.3.1 MHL Eye Pattern

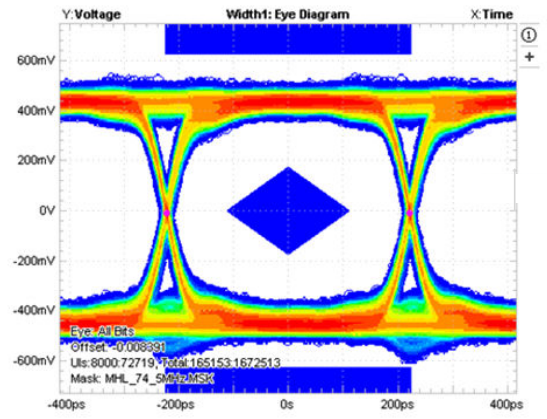


图 7-2. Eye Pattern Error Histogram: 2.25 Gbps With No Device

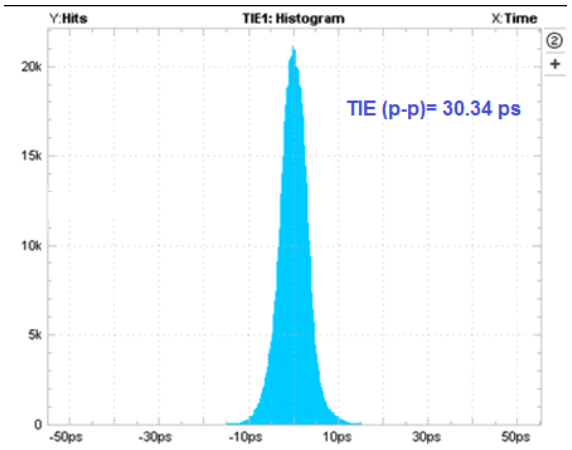


图 7-3. Time Interval Error Histogram: 2.25 Gbps With No Device

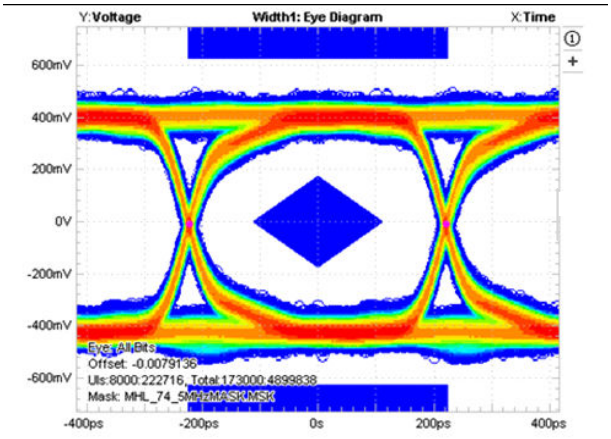


图 7-4. Eye Pattern Error Histogram: 2.25 Gbps With TS3USB3031 (Added Jitter = 5.04 ps)

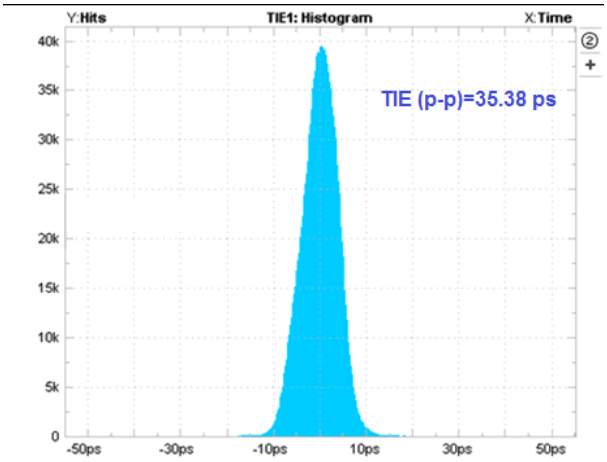


图 7-5. Time Interval Error Histogram: 2.25 Gbps With TS3USB3031 (Added Jitter = 5.04 ps)

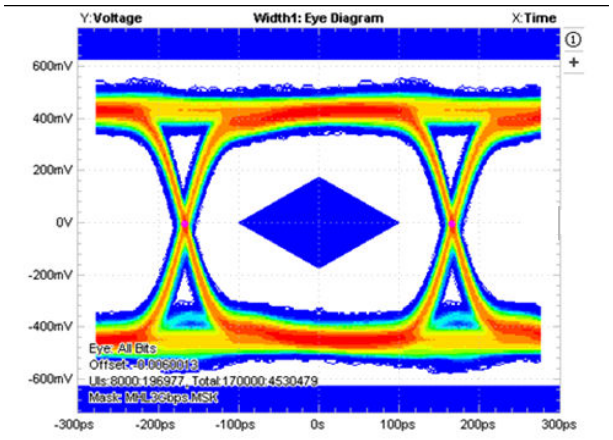


图 7-6. Eye Pattern Error Histogram: 3.0 Gbps With No Device

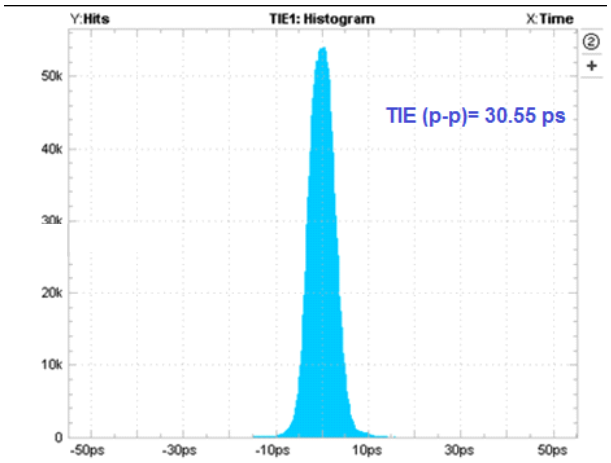


图 7-7. Time Interval Error Histogram: 3.0 Gbps With No Device

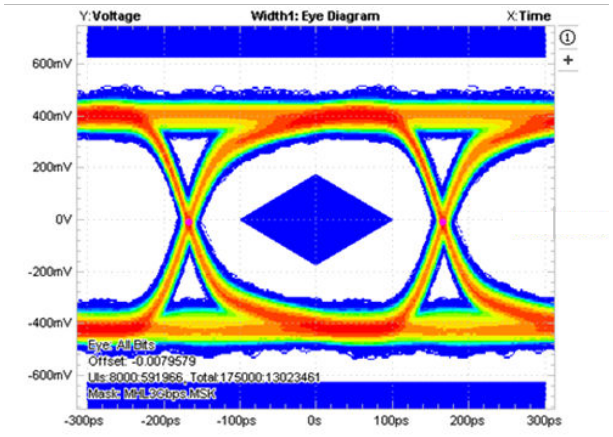


图 7-8. Eye Pattern Error Histogram: 3.0 Gbps With TS3USB3031 (Added Jitter = 2.57 ps)

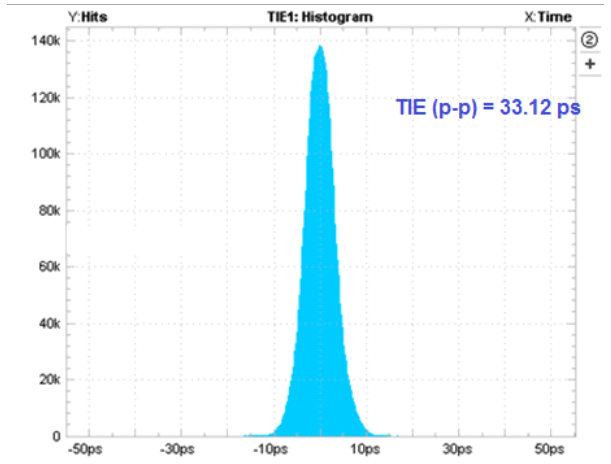


图 7-9. Time Interval Error Histogram: 3.0 Gbps With TS3USB3031 (Added Jitter = 2.57 ps)

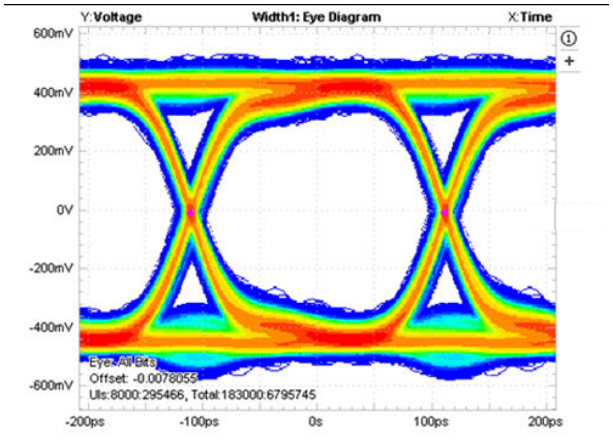


图 7-10. Eye Pattern Error Histogram: 4.5 Gbps With No Device

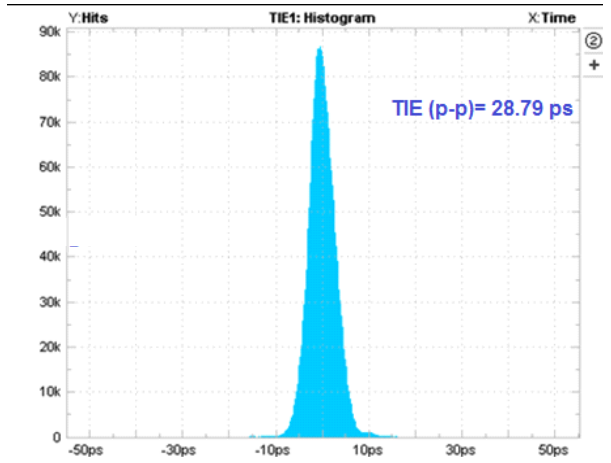


图 7-11. Time Interval Error Histogram: 4.5 Gbps With No Device

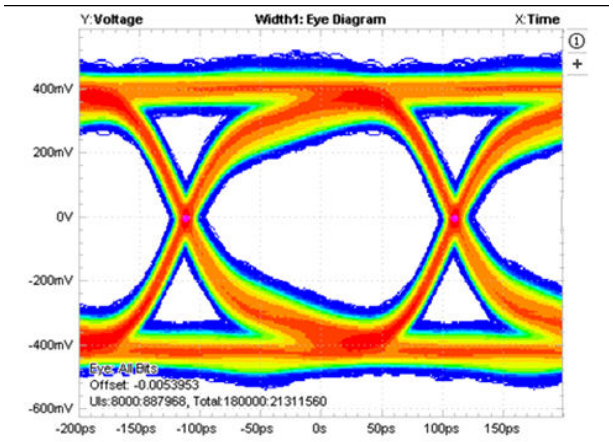


图 7-12. Eye Pattern Error Histogram: 4.5 Gbps With TS3USB3031 (Added Jitter = 1.13 ps)

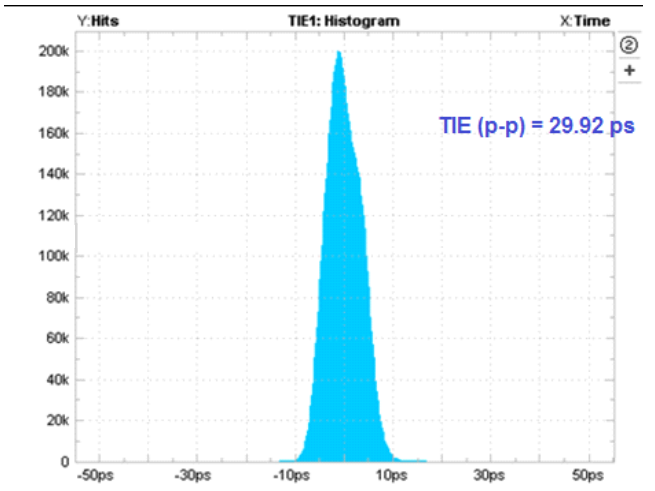


图 7-13. Time Interval Error Histogram: 4.5 Gbps With TS3USB3031 (Added Jitter = 1.13 ps)

7.2.3.2 USB EYE Pattern

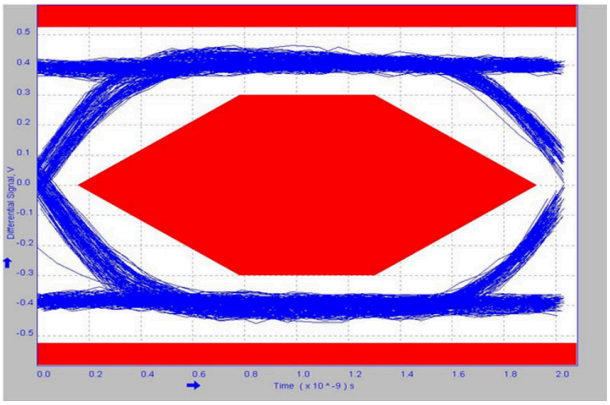


图 7-14. 480-Mbps USB 2.0 Eye Pattern With No Device

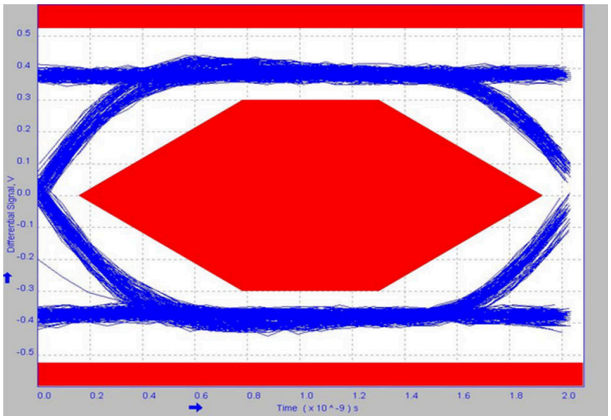


图 7-15. 480-Mbps USB 2.0 Eye Pattern for USB Switch

7.3 Power Supply Recommendations

Power to the device is supplied through the V_{CC} pin. TI recommends placing a bypass capacitor as close as possible to the supply pin V_{CC} to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

This device does not require any power sequencing with respect to other devices in the system due to the power off isolation feature. The power off isolation feature allows signals to be present on the signal path pins before the device is powered up without damaging the device.

7.4 Layout

7.4.1 Layout Guidelines

Place supply bypass capacitors as close to the V_{CC} pin as possible and avoid placing the bypass caps near the D+ and D – traces.

The high-speed D+ and D – traces must always be of equal length and must be no more than four inches; otherwise, the eye diagram performance may degrade. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In the layout, the impedance of D+ and D – traces must match the cable characteristic differential impedance for optimal performance.

Route the high-speed USB signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around the via to minimize the capacitance. Each via introduces discontinuities in the transmission line of the signal and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices, or ICs that use or duplicate clock signals.

Avoid stubs on the high-speed USB signals because the stubs cause signal reflections. If a stub is unavoidable, then the stub must be less than 200 mm.

Route all high-speed USB signal traces over continuous GND planes, with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended: two signal layers separated by a ground layer and a power layer. The majority of signal traces must run on a single layer, preferably top layer. Immediately next to this layer must be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies. For more information on layout guidelines, see *High Speed Layout Guidelines* and *USB 2.0 Board Design and Layout Guidelines* .

7.4.2 Layout Example

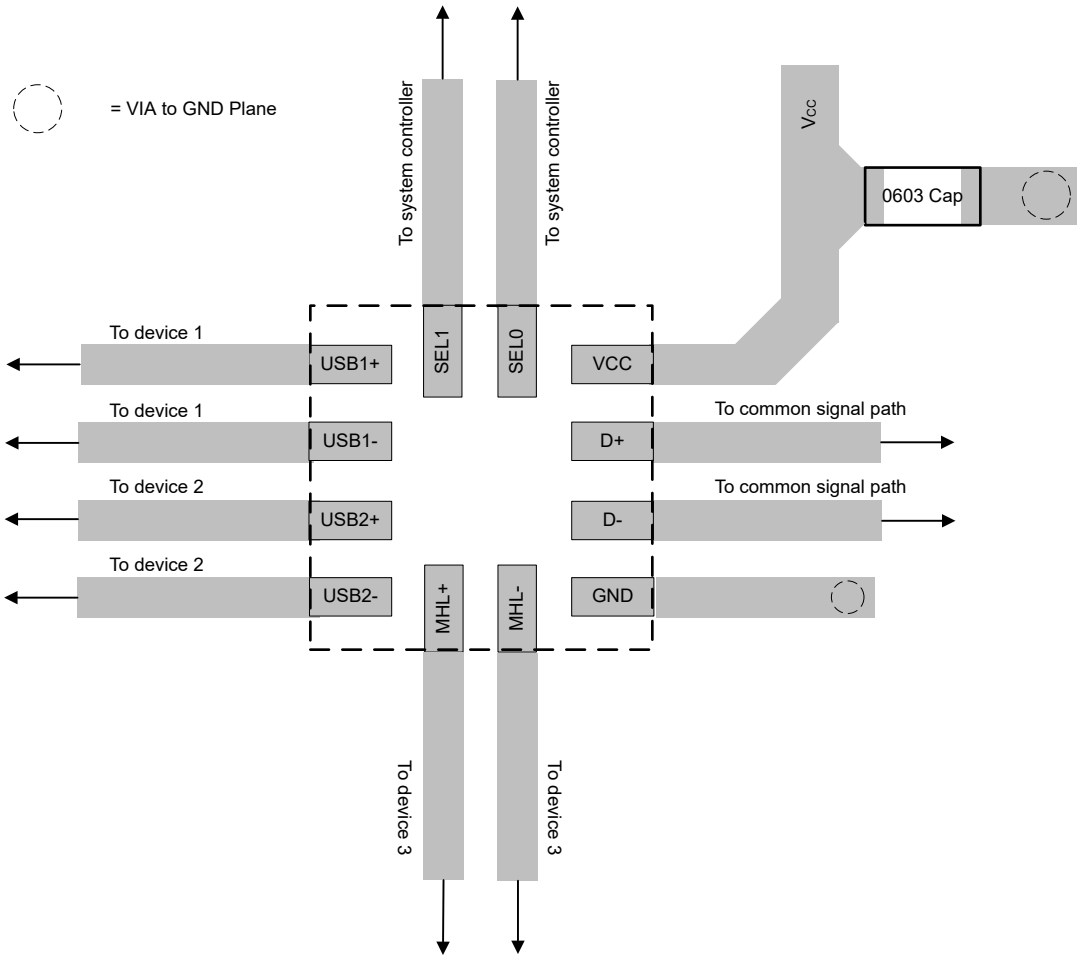


图 7-16. Layout Recommendation

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *High Speed Layout Guidelines*
- Texas Instruments, *USB 2.0 Board Design and Layout Guidelines*

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.4 Trademarks

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8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (March 2017) to Revision D (August 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 将间距尺寸从“0.5mm”更改为“0.4mm”	1
• Changed the *480-Mbps USB 2.0 Eye Pattern for USB Switch* graph.	14
• Changed SEL2 pin name to SEL0 in the *Layout Example* image to keep consistency across the data sheet	16

Changes from Revision B (December 2016) to Revision C (March 2017)	Page
• 将“特性”中的“1.8V 兼容控制输入（SEL，$\overline{OE}$）”更改为：“1.8V 兼容控制输入 (SEL)”	1
• 将第二个引脚 D+ 更改为：D-（在*开关方框图* 中）	1
• Changed DIGITAL CONTROL INPUTS (SEL, $\overline{OE}$) To: DIGITAL CONTROL INPUTS (SEL) in the *Electrical Characteristics* table	5
• Changed second pin D+ To: D- in the *Functional Block Diagram*	10

- Deleted sentence: "The internal pulldown resistor on OE enables the switch when power is applied to VCC" from the *Design Requirements* section 12

Changes from Revision A (September 2013) to Revision B (December 2016) **Page**

- 添加了*应用* 列表、*ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分。 1
- 删除了*订购信息* 表，请参阅数据表末尾的*封装选项附录* 1
- Moved Peak switch DC output current parameter From: *Absolute Maximum Ratings* To: *Recommended Operating Conditions* 4

Changes from Revision * (June 2013) to Revision A (September 2013) **Page**

- Added TYPICAL CHARACTERISTICS section 6

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS3USB3031RMGR	Active	Production	WQFN (RMG) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DY
TS3USB3031RMGR.A	Active	Production	WQFN (RMG) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DY
TS3USB3031RMGRG4	Active	Production	WQFN (RMG) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DY
TS3USB3031RMGRG4.A	Active	Production	WQFN (RMG) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DY

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

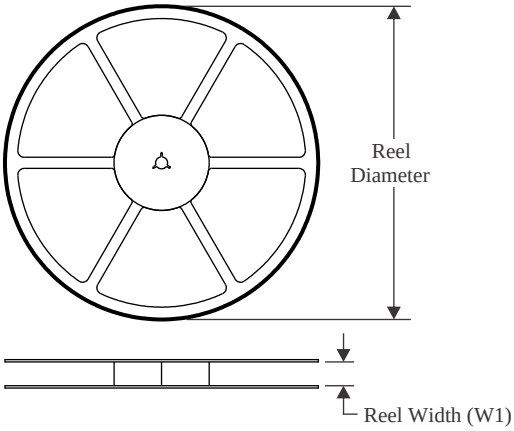
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

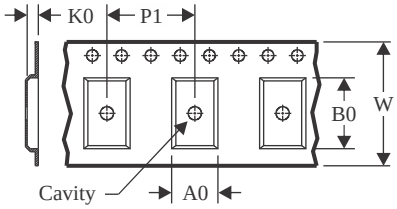
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

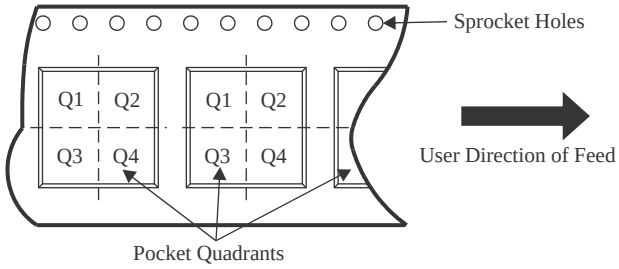


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

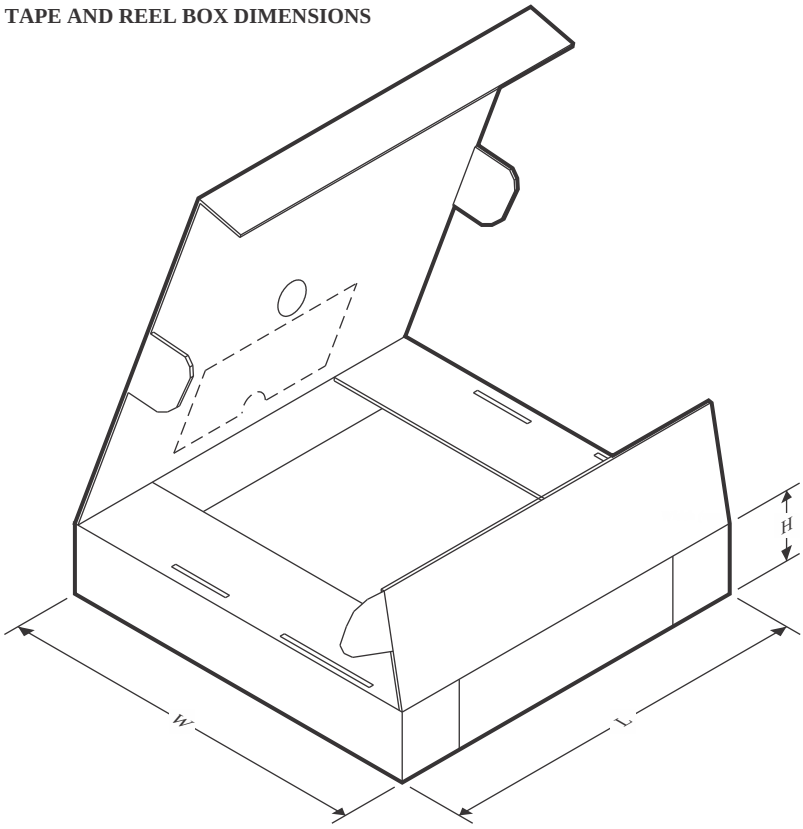
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3USB3031RMGR	WQFN	RMG	12	3000	180.0	8.4	2.05	2.05	1.0	4.0	8.0	Q2
TS3USB3031RMGRG4	WQFN	RMG	12	3000	180.0	8.4	2.05	2.05	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

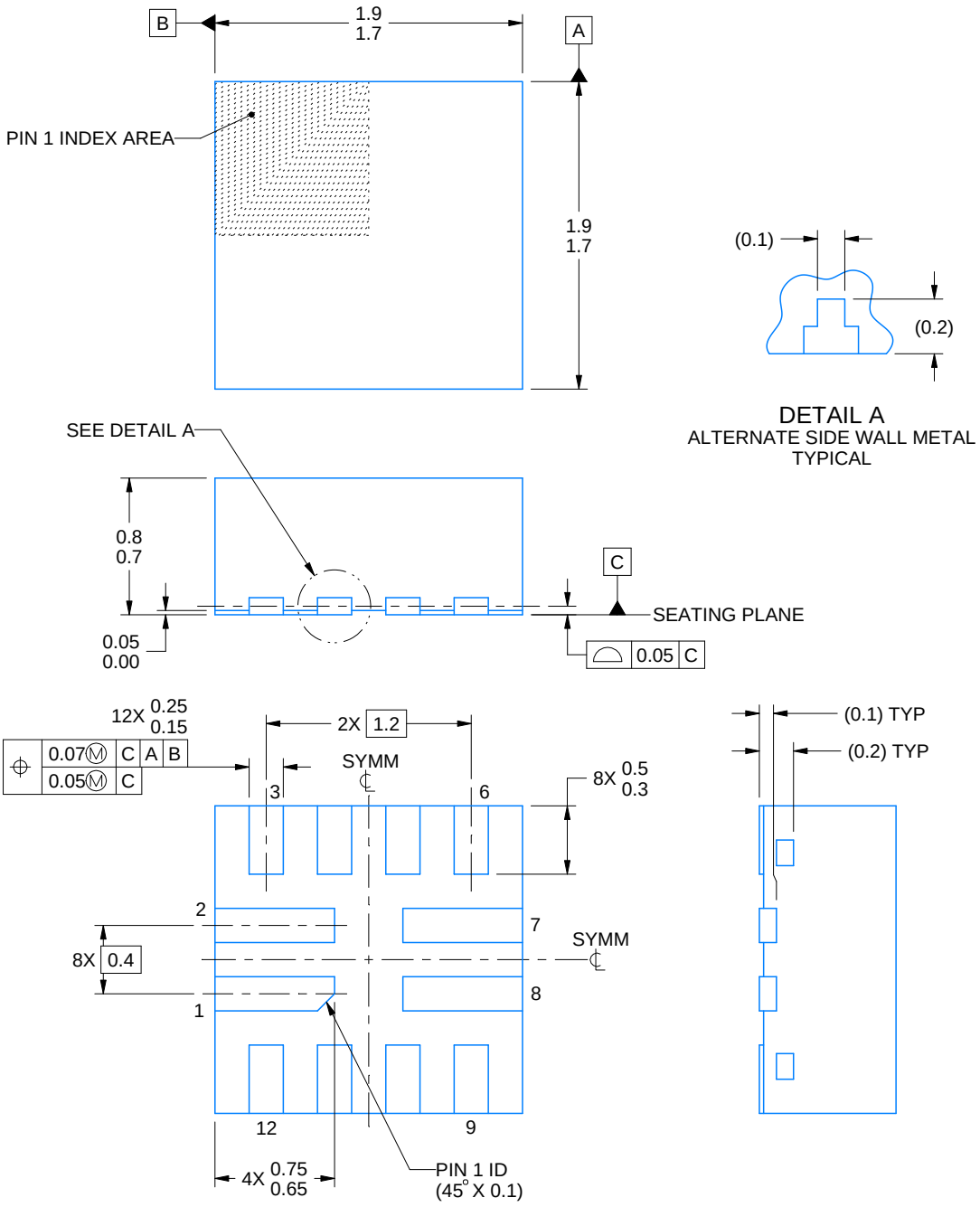
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3USB3031RMGR	WQFN	RMG	12	3000	182.0	182.0	20.0
TS3USB3031RMGRG4	WQFN	RMG	12	3000	182.0	182.0	20.0

PACKAGE OUTLINE

RMG0012A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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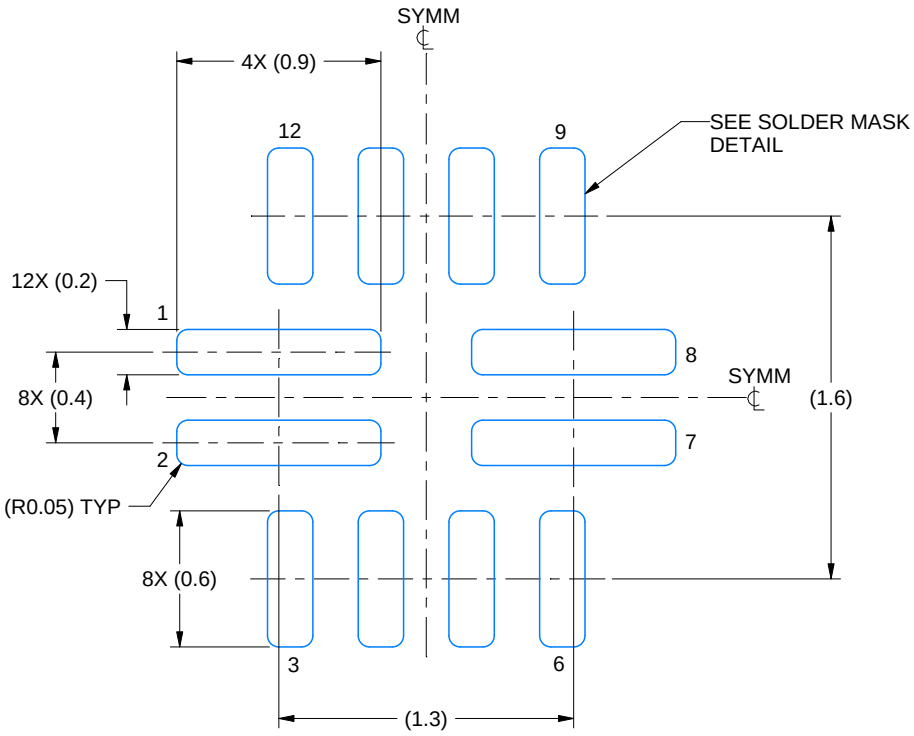
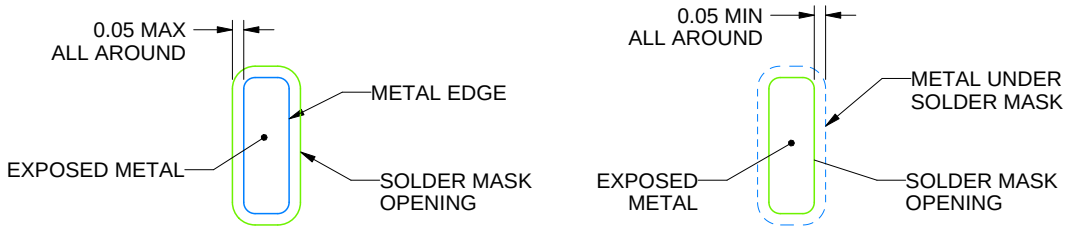
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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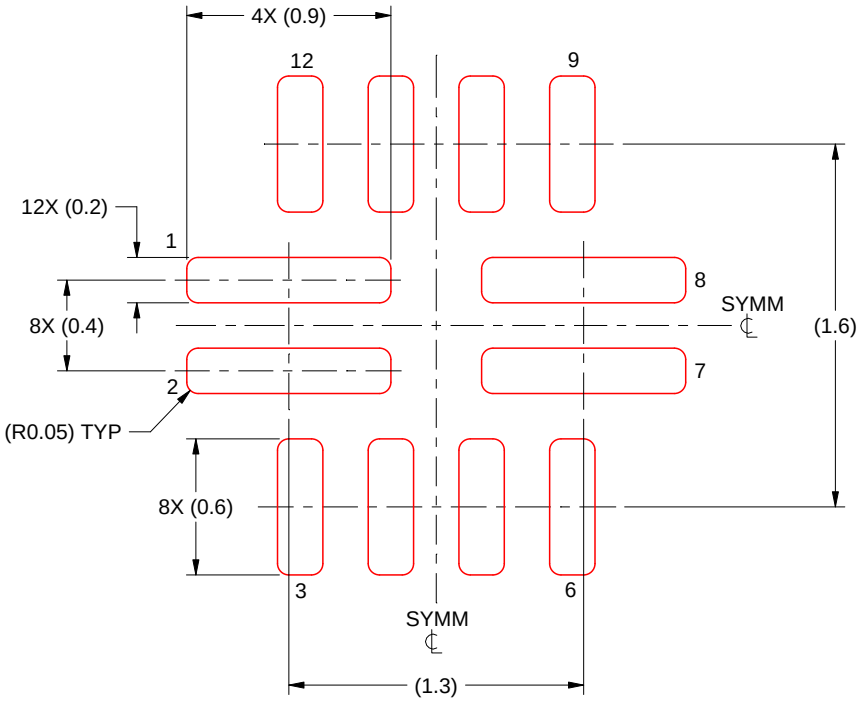
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月