适用于汽车的 TS3A5017-Q1 双通道 4:1 模拟开关 转换器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 器件温度范围：–40°C 至 125°C，T_A
  - 器件 HBM 分类等级：±1500V
  - 器件 CDM 分类等级：±1000V
- 支持关断保护，当 V_{CC} = 0V 时，I/O 引脚处于高阻抗状态
- 低导通状态电阻
- 低电荷注入
- 1Ω 通态电阻匹配
- 0.25% 总谐波失真 (THD+N)
- 2.3V 至 3.6V 单电源运行
- 锁断性能超过 100mA，符合 JESD 78 II 类规范的要求

2 应用

- 采样和保持电路
- 信息娱乐音频和视频信号路由
- 远程信息处理控制单元

3 说明

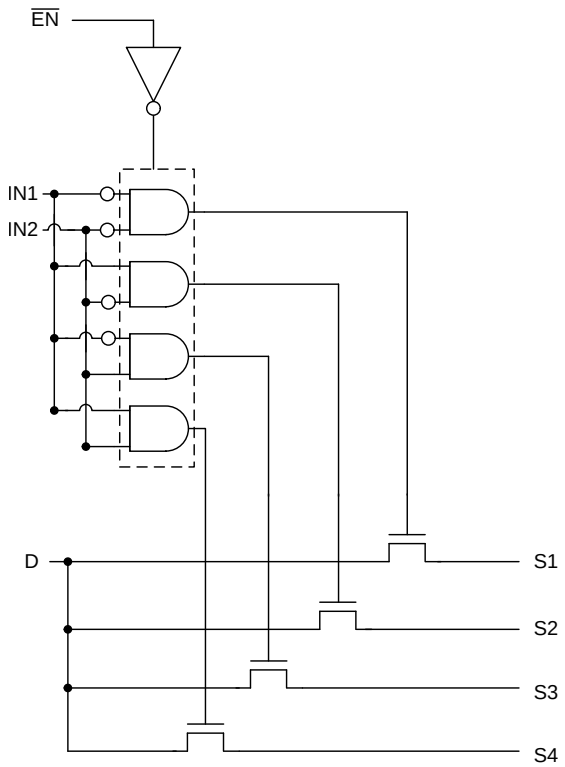
TS3A5017-Q1 器件是一款双通道 4:1 多路复用器，其设计工作电压为 2.3V 至 3.6V。该器件是一款双向器件，可以处理数字和模拟信号。该器件的断电保护功能可确保 V_{CC} = 0V 时信号路径为高阻抗，从而简化了电源定序，并提高了系统可靠性。

器件信息(1)

器件编号	封装	封装尺寸（标称值）
TS3A5017-Q1	VQFN (16)	4.00mm × 3.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

方框图



目录

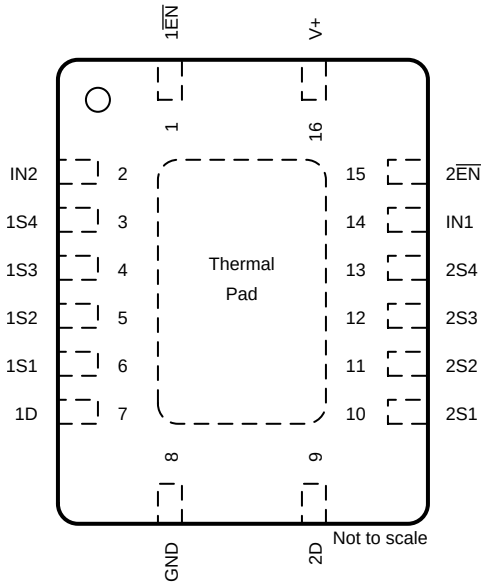
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2018 年 10 月	*	最初发布版本

5 Pin Configuration and Functions

RGY Package
16-Pin VQFN
(Top View)



If exposed thermal pad is used, it must be connected as a secondary ground or left electrically open.

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
7	1D	I/O	Common path for switch 1
1	1$\overline{EN}$	I	Active-low enable for switch 1
6	1S1	I/O	Switch 1 channel 1
5	1S2	I/O	Switch 1 channel 2
4	1S3	I/O	Switch 1 channel 3
3	1S4	I/O	Switch 1 channel 4
9	2D	I/O	Common path for switch 2
15	2$\overline{EN}$	I	Active-low enable for switch 2
10	2S1	I/O	Switch 2 channel 1
11	2S2	I/O	Switch 2 channel 2
12	2S3	I/O	Switch 2 channel 3
13	2S4	I/O	Switch 2 channel 4
8	GND	–	Ground
14	IN1	I	Switch 1 input select
2	IN2	I	Switch 2 input select
16	V+	–	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
V_+	Supply voltage(3)		–0.5	4.6	V
V_S, V_D	Analog voltage(3) (4)		–0.5	4.6	V
I_{SK}, I_{DK}	Analog port clamp current	V_S, V_D < 0	–50		mA
I_S, I_D	ON-state switch current	V_S, V_D = 0 to 7 V	–128	128	mA
V_I	Digital input voltage		–0.5	4.6	V
I_{IK}	Digital input clamp current(3) (4)	V_I < 0	–50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		–100		mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under*Absolute Maximum Ratings* may cause permanent damage to thedevice. These are stress ratings only, and functional operation of the device at these or any otherconditions beyond those indicated under *Recommended OperatingConditions* is not implied. Exposure to absolute-maximum-rated conditions for extendedperiods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is aminimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwisespecified.
(4) The input and output voltage ratings may be exceeded if theinput and output clamp-current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Switch input/output voltage range	0	3.6	V
V+	Supply voltage range	2.3	3.6	V
V_I	Control input voltage range	0	3.6	V
T_A	Operating Temperature Range	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TS3A5017-Q1 RGY (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24.0	°C/W

(1) For more information about traditional and new thermalmetrics, see the *IC Package ThermalMetrics* application report .

6.5 Electrical Characteristics for 3.3-VSupply

V_+ = 2.7 V to 3.6 V, T_A = –40°C to125°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Analog Switch								
V_D, V_S	Analog signal range				0		V_+	V
r_{on}	ON-state resistance	0 ≤ V_S ≤ V_+, I_D = –32 mA,	Switch ON, see 图 12	T_A = 25°C V_+ = 3 V		11		Ω
				T_A = Full V_+ = 3 V			16	
Δr_{on}	ON-state resistance match between channels	V_S = 2.1 V, I_D = –32 mA,	Switch ON, see 图 12	T_A = 25°C V_+ = 3 V		1		Ω
				T_A = Full V_+ = 3 V			5	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_S ≤ V_+, I_D = –32 mA,	Switch ON, see 图 12	T_A = 25°C V_+ = 3 V		7		Ω
				T_A = Full V_+ = 3 V			12	
$I_{S(OFF)}$	S OFF leakage current	V_S = 1 V, V_D = 3 V, or V_S = 3 V, V_D = 1 V,	Switch OFF, see 图 13	T_A = 25°C V_+ = 3.6 V		0.05		µA
				T_A = Full V_+ = 3.6 V	–0.3		0.3	
$I_{SPWR(OFF)}$		V_S = 0 to 3.6 V, V_D = 3.6 V to 0,		T_A = 25°C V_+ = 0 V		0.5		
				T_A = Full V_+ = 0 V	–10		10	
$I_{D(OFF)}$	D OFF leakage current	V_S = 1 V, V_D = 3 V, or V_S = 3 V, V_D = 1 V,	Switch OFF, see 图 13	T_A = 25°C V_+ = 3.6 V		0.05		µA
				T_A = Full V_+ = 3.6 V	–0.3		0.3	
$I_{DPWR(OFF)}$		V_D = 0 to 3.6 V, V_S = 3.6 V to 0,		T_A = 25°C V_+ = 0 V		0.5		
				T_A = Full V_+ = 0 V	–20		20	
$I_{S(ON)}$	S ON leakage current	V_S = 1 V, V_D = Open, or V_S = 3 V, V_D = Open,	Switch ON, see 图 14	T_A = 25°C V_+ = 3.6 V		0.05		µA
				T_A = Full V_+ = 3.6 V	–0.3		0.3	
$I_{D(ON)}$	D ON leakage current	V_D = 1 V, V_S = Open, or V_D = 3 V, V_S = Open,	Switch ON, see 图 14	T_A = 25°C V_+ = 3.6 V		0.05		µA
				T_A = Full V_+ = 3.6 V	–0.3		0.3	
Digital Control Inputs (IN1, IN2, $\overline{EN}$)(2)								
V_{IH}	Input logic high			T_A = Full	2		V_+	V
V_{IL}	Input logic low			T_A = Full	0		0.8	V
I_{IH}, I_{IL}	Input leakage current	V_I = V_+ or 0		T_A = 25°C V_+ = 3.6 V		0.05		µA
				T_A = Full V_+ = 3.6 V	–1		1	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0, C_L = 0.1 nF,	See 图 21	T_A = 25°C V_+ = 3.3 V		5		pC
$C_{S(OFF)}$	S OFF capacitance	V_S = V_+ or GND, Switch OFF,	See 图 15	T_A = 25°C V_+ = 3.3 V		4.5		pF
$C_{D(OFF)}$	D OFF capacitance	V_D = V_+ or GND, Switch OFF,	See 图 15	T_A = 25°C V_+ = 3.3 V		19		pF
$C_{S(ON)}$	S ON capacitance	V_S = V_+ or GND, Switch ON,	See 图 15	T_A = 25°C V_+ = 3.3 V		27		pF

(1) The algebraic convention, whereby the most negative value is aminimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held atV_+ or GND to ensure proper device operation. Refer to the TI applicationreport, *Implications of Slow or Floating CMOS Inputs*, literaturenumber SCBA004.

Electrical Characteristics for 3.3-VSupply (continued)

V_+ = 2.7 V to 3.6 V, T_A = –40°C to125°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$C_{D(ON)}$	D ON capacitance	V_D = V_+ or GND, Switch ON,	See 图 15	T_A = 25°C V_+ = 3.3 V		27		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See 图 15	T_A = 25°C V_+ = 3.3 V		3		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See 图 17	T_A = 25°C V_+ = 3.3 V		165		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	See 图 18	T_A = 25°C V_+ = 3.3 V		–69		dB
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 10 MHz,	See 图 18	T_A = 25°C V_+ = 3.3 V		–49		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	See 图 19	T_A = 25°C V_+ = 3.3 V		–69		dB
$X_{TALK(ADJ)}$	Crosstalk adjacent	R_L = 50 Ω, f = 1 MHz,	See 图 20	T_A = 25°C V_+ = 3.3 V		–80		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see 图 22	T_A = 25°C V_+ = 3.3 V		0.25		%
Supply								
I_+	Positive supply current	V_I = V_+ or GND,	Switch ON or OFF	T_A = 25°C V_+ = 3.6 V		2.5	7	μA
				T_A = Full V_+ = 3.6 V			10	

6.6 Electrical Characteristics for 2.5-VSupply

V_+ = 2.3 V to 2.7 V, T_A = –40°C to125°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Analog Switch								
V_D, V_S	Analog signal range				0		V_+	V
r_{on}	ON-state resistance	0 ≤ V_S ≤ V_+, I_D = –24 mA,	Switch ON, see 图 12	T_A = 25°C V_+ = 2.3 V		22		Ω
				T_A = Full V_+ = 2.3 V			28	
Δr_{on}	ON-state resistance match between channels	V_S = 1.6 V, I_D = –24 mA,	Switch ON, see 图 12	T_A = 25°C V_+ = 2.3 V		1		Ω
				T_A = Full V_+ = 2.3 V			5	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_S ≤ V_+, I_D = –24 mA,	Switch ON, see 图 12	T_A = 25°C V_+ = 2.3 V		18		Ω
				T_A = Full V_+ = 2.3 V			24	
$I_{S(OFF)}$	S OFF leakage current	V_S = 0.5 V, V_D = 2.2 V, or V_S = 2.2 V, V_D = 0.5 V,	Switch OFF, see 图 13	T_A = 25°C V_+ = 2.7 V		0.05		μA
				T_A = Full V_+ = 2.7 V	–0.3		0.3	
$I_{SPWR(OFF)}$		V_S = 0 to 2.7 V, V_D = 2.7 V to 0,		T_A = 25°C V_+ = 0 V		0.5		
				T_A = Full V_+ = 0 V	-15		15	

(1) The algebraic convention, whereby the most negative value is aminimum and the most positive value is a maximum

Electrical Characteristics for 2.5-VSupply (continued)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to125°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$I_{D(OFF)}$	D OFF leakage current	V_S = 0.5 V, V_D = 2.2 V, or V_S = 2.2 V, V_D = 0.5V,	Switch OFF, see 图 13	T_A = 25°C V_+ = 2.7 V		0.05		μA
				T_A = Full V_+ = 2.7 V	–0.3		0.3	
$I_{DPWR(OFF)}$		V_D = 0 to 2.7 V, V_S = 2.7 V to 0,		T_A = 25°C V_+ = 0 V		0.5		
				T_A = Full V_+ = 0 V	-20		20	
$I_{S(ON)}$	S ON leakage current	V_S = 0.5 V, V_D = Open, or V_S = 2.2 V, V_D = Open,	Switch ON, see 图 14	T_A = 25°C V_+ = 2.7 V		0.05		μA
				T_A = Full V_+ = 2.7 V	–0.3		0.3	
$I_{D(ON)}$	D ON leakage current	V_D = 0.5 V, V_S = Open, or V_D = 2.2 V, V_S = Open,	Switch ON, see 图 14	T_A = 25°C V_+ = 2.7 V		0.05		μA
				T_A = Full V_+ = 2.7 V	–0.3		0.3	
Logic Inputs (IN1, IN2, $\overline{EN}$)(2)								
V_{IH}	Input logic high			T_A = Full	1.7		V_+	V
V_{IL}	Input logic low			T_A = Full	0		0.7	V
I_{IH}, I_{IL}	Input leakage current	V_I = V_+ or 0		T_A = 25°C V_+ = 2.7 V		0.05		μA
				T_A = Full V_+ = 2.7 V	–1		1	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0, C_L = 0.1 nF,	See 图 21	T_A = Full V_+ = 2.5 V		3		pC
$C_{S(OFF)}$	S OFF capacitance	V_S = V_+ or GND, Switch OFF,	See 图 15	T_A = Full V_+ = 2.5 V		4.5		pF
$C_{D(OFF)}$	D OFF capacitance	V_D = V_+ or GND, Switch OFF,	See 图 15	T_A = Full V_+ = 2.5 V		18.5		pF
$C_{S(ON)}$	S ON capacitance	V_S = V_+ or GND, Switch ON,	See 图 15	T_A = Full V_+ = 2.5 V		26		pF
$C_{D(ON)}$	D ON capacitance	V_D = V_+ or GND, Switch ON,	See 图 15	T_A = Full V_+ = 2.5 V		26		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See 图 15	T_A = Full V_+ = 2.5 V		3		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See 图 17	T_A = Full V_+ = 2.5 V		165		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	See 图 18	T_A = Full V_+ = 2.5 V		–69		dB
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 10 MHz,	See 图 18	T_A = Full V_+ = 2.5 V		–49		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	See 图 19	T_A = Full V_+ = 2.5 V		–69		dB
$X_{TALK(ADJ)}$	Crosstalk adjacent	R_L = 50 Ω, f = 1 MHz,	See 图 20	T_A = Full V_+ = 2.5 V		–85		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see 图 22	T_A = Full V_+ = 2.5 V		0.3		%
Supply								

(2) All unused digital inputs of the device must be held atV_+ or GND to ensure proper device operation. Refer to the TI applicationreport, *Implications of Slow or Floating CMOS Inputs*, literaturenumber SCBA004.

Electrical Characteristics for 2.5-VSupply (continued)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to125°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_+	Positive supply current	V_I = V_+ or GND,	Switch ON or OFF	T_A = Full V_+ = 2.7 V		2.5	7	µA
				T_A = Full V_+ = 2.7 V			10	

6.7 Switching Characteristics for 3.3-VSupply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{ON}	Turnon time(1)	V_D = 2 V, R_L = 300 Ω,	C_L = 35 pF, see 图 16	T_A = 25°C V_+ = 3.3 V		5	9.5	ns
				T_A = Full V_+ = 3 V to 3.6 V			10.5	
t_{OFF}	Turnoff time(1)	V_D = 2 V, R_L = 300 Ω,	C_L = 35 pF, see 图 16	T_A = 25°C V_+ = 3.3 V		1.5	3.5	ns
				T_A = Full V_+ = 3 V to 3.6 V			4.5	

(1) Specified by design, not tested in production

6.8 Switching Characteristics for 2.5-VSupply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{ON}	Turnon time(1)	V_{COM} = 2 V, R_L = 300 Ω,	C_L = 35 pF, see 图 16	T_A = 25°C V_+ = 2.5 V		5	8	ns
				T_A = Full V_+ = 2.3 V to 2.7 V			10	
t_{OFF}	Turnoff time(1)	V_{COM} =2 V, R_L = 300 Ω,	C_L = 35 pF, see 图 16	T_A = 25°C V_+ = 2.5 V		2	4.5	ns
				T_A = Full V_+ = 2.3 V to 2.7 V			6	

(1) Specified by design, not tested in production.

6.9 Typical Characteristics

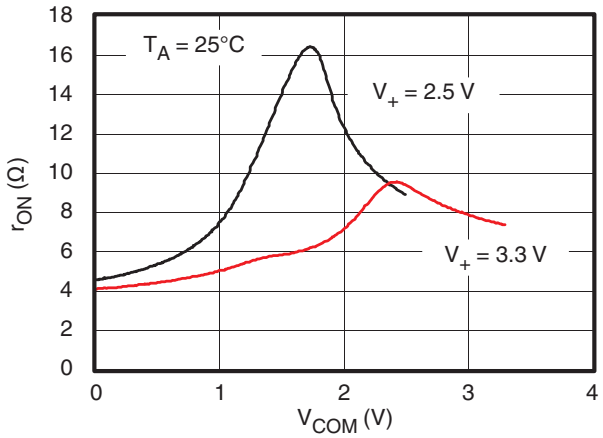


图 1. r_{on} vs V_{COM}

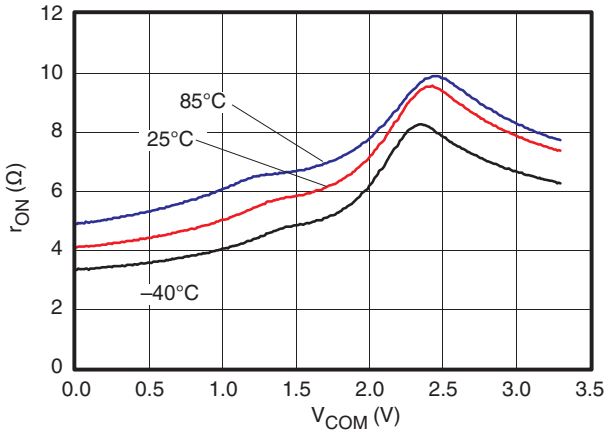


图 2. r_{on} vs V_{COM} (V_+ = 3.3 V)

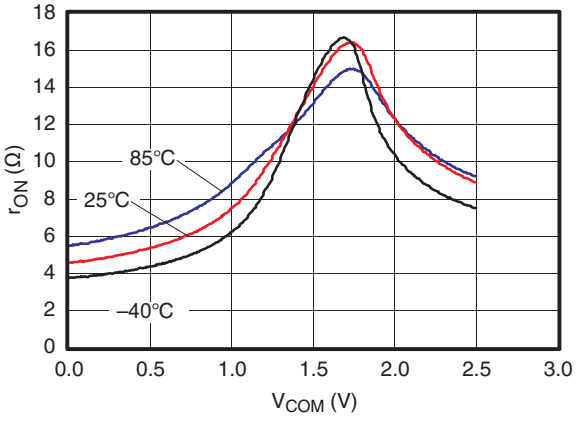


图 3. r_{on} vs V_{COM} (V_+ = 2.5 V)

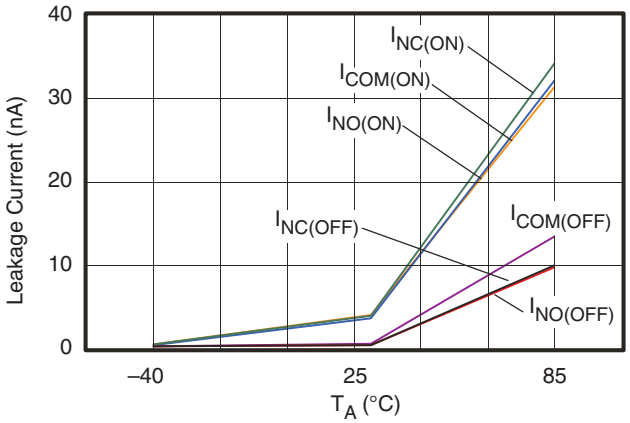


图 4. Leakage Current vs Temperature (V_+ = 3.6 V)

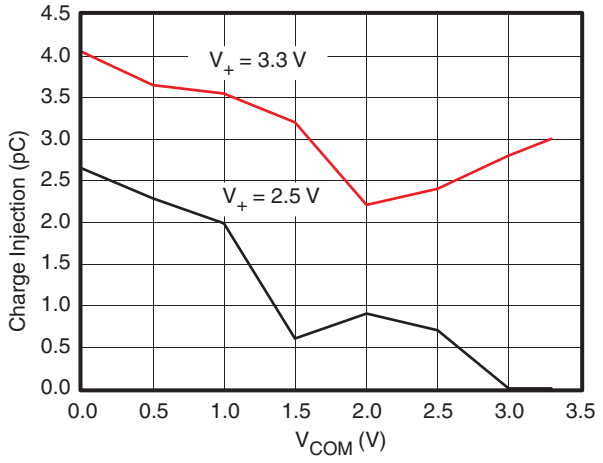


图 5. Charge Injection (Q_C) vs V_{COM}

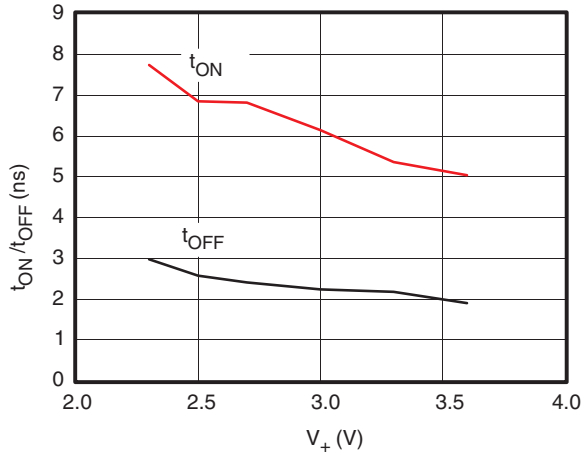


图 6. t_{ON} and t_{OFF} vs Supply Voltage

Typical Characteristics (接下页)

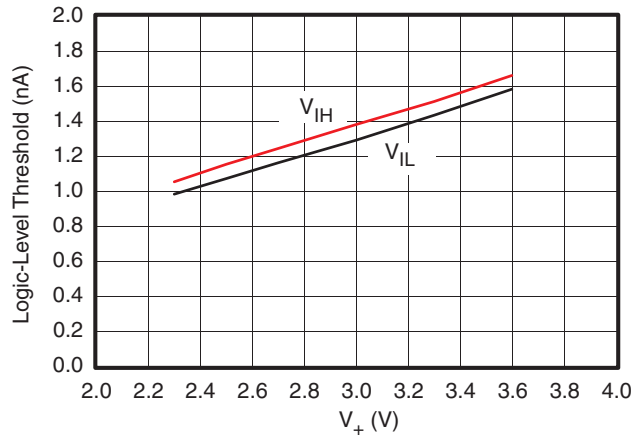


图 7. Logic-Level Threshold vs V_+

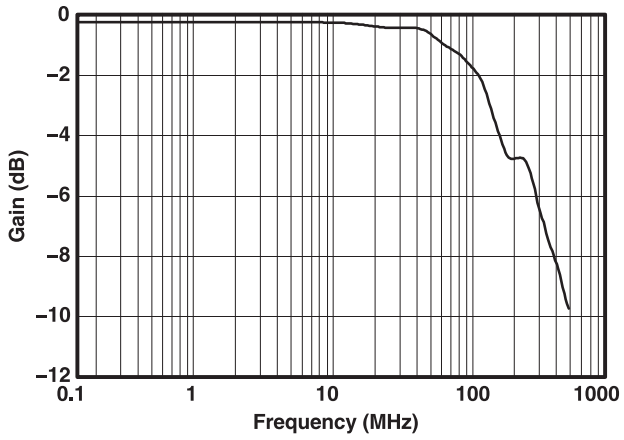


图 8. Bandwidth (Gain vs Frequency) (V_+ = 3.3 V)

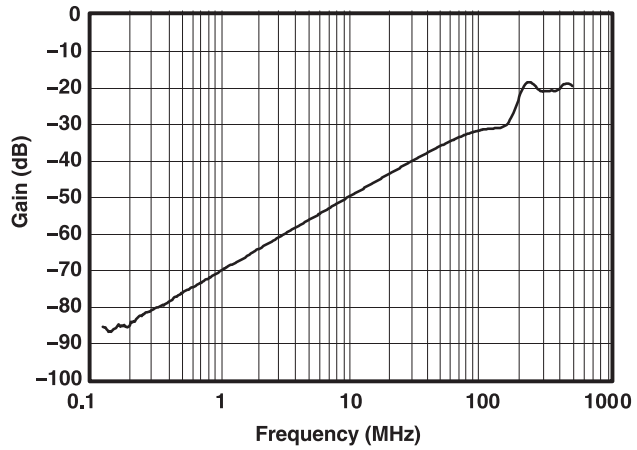


图 9. OFF Isolation and Crosstalk vs Frequency (V_+ = 3.3 V)

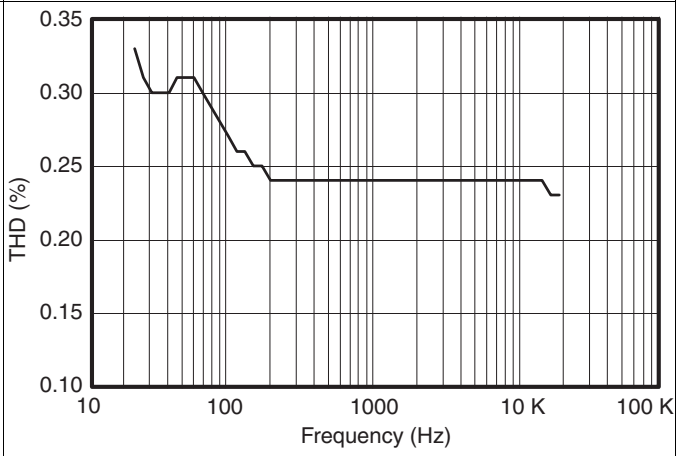


图 10. Total Harmonic Distortion vs Frequency

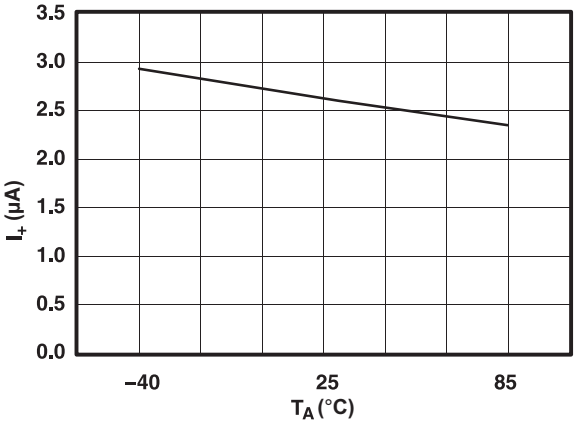


图 11. Power-Supply Current vs Temperature (V_+ = 3.6 V)

7 Parameter Measurement Information

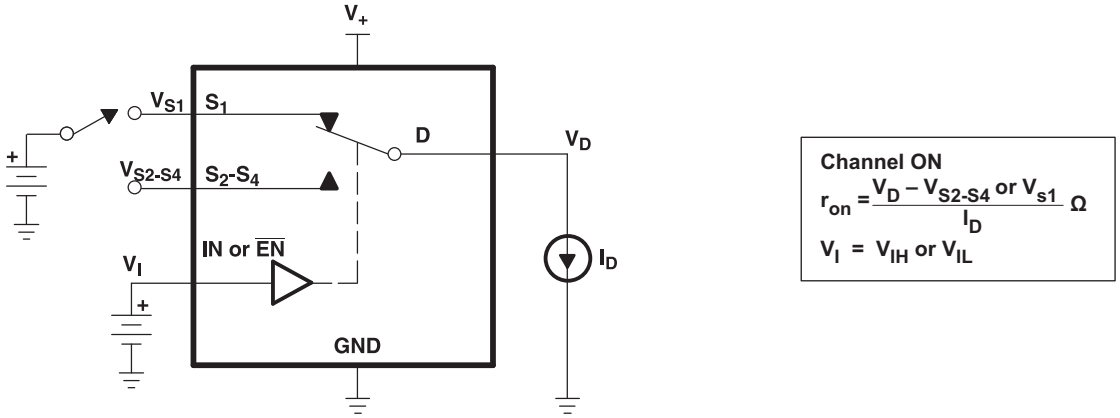


图 12. ON-State Resistance (r_{on})

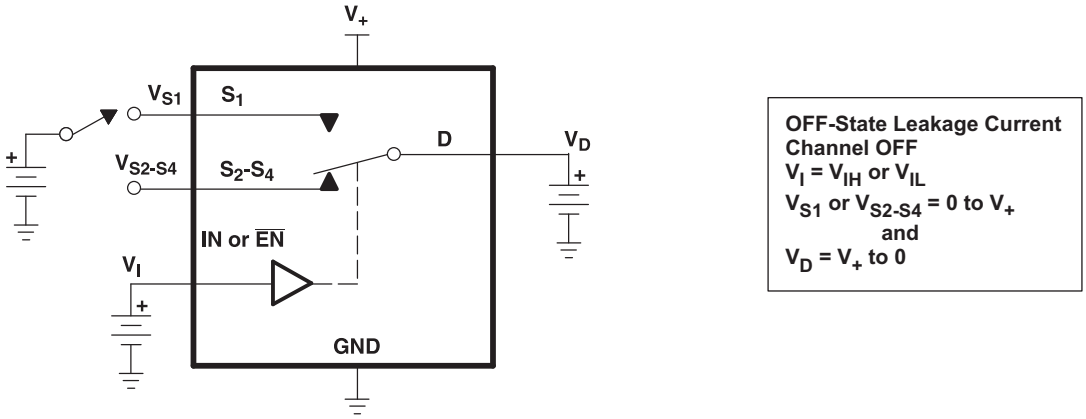


图 13. OFF-State Leakage Current ($I_{D(OFF)}$, $I_{S(OFF)}$)

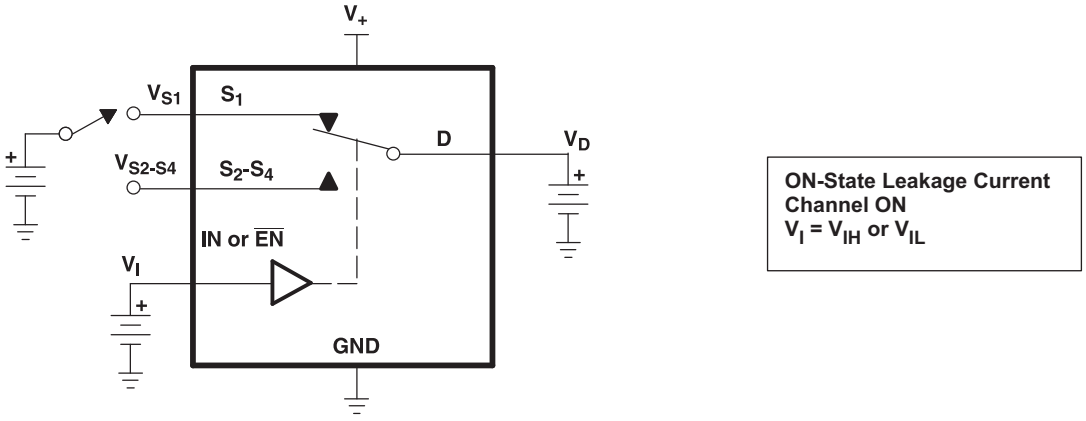


图 14. ON-State Leakage Current ($I_{D(ON)}$, $I_{S(ON)}$)

Parameter Measurement Information (接下页)

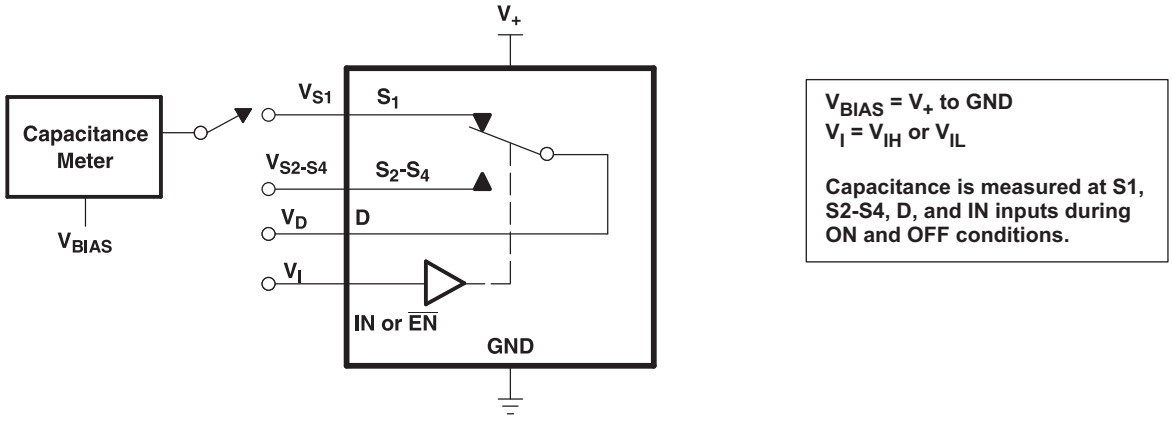
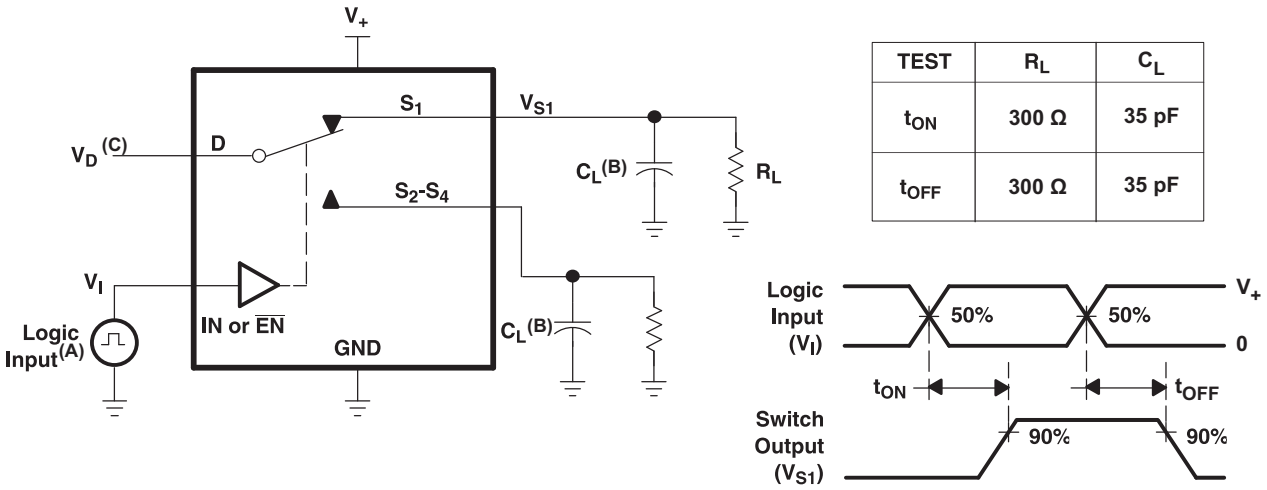


图 15. Capacitance (C_I, $C_{D(OFF)}$, $C_{D(ON)}$, $C_{S(OFF)}$, $C_{S(ON)}$)



A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

C. See Electrical Characteristics for V_D.

图 16. Turnon (t_{ON}) and Turnoff Time (t_{OFF})

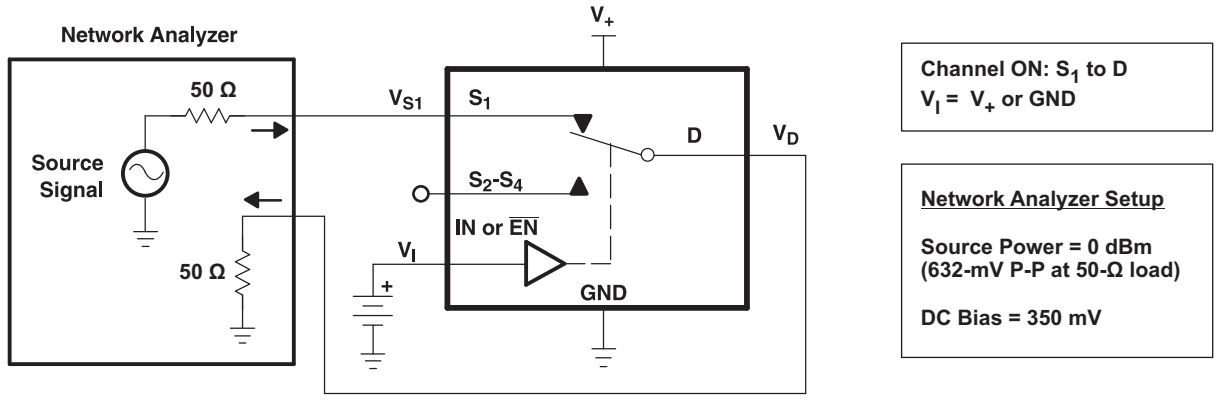


图 17. Bandwidth (BW)

Parameter Measurement Information (接下页)

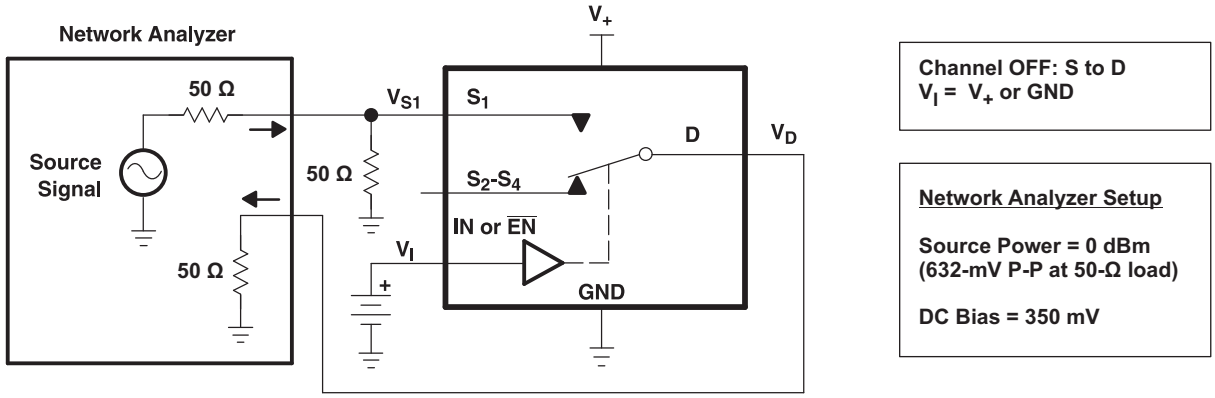


图 18. OFF Isolation (O_{ISO})

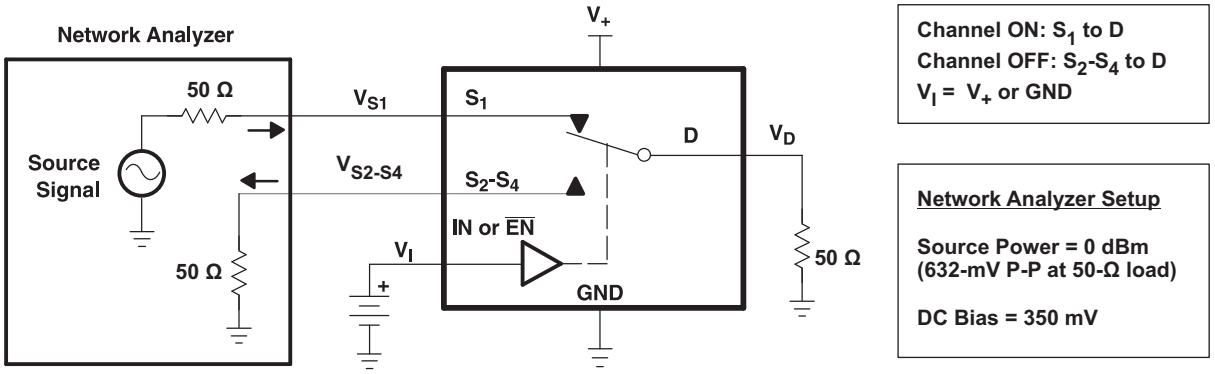


图 19. Crosstalk (X_{TALK})

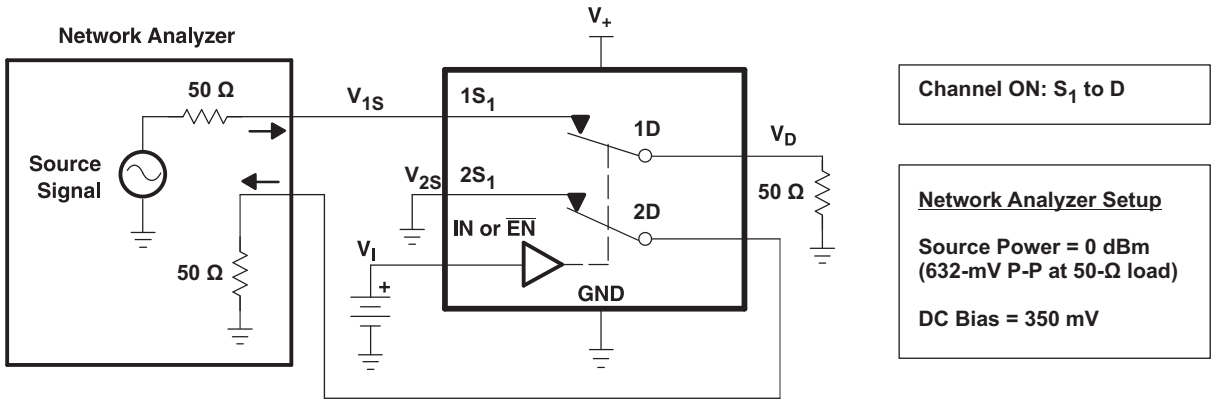
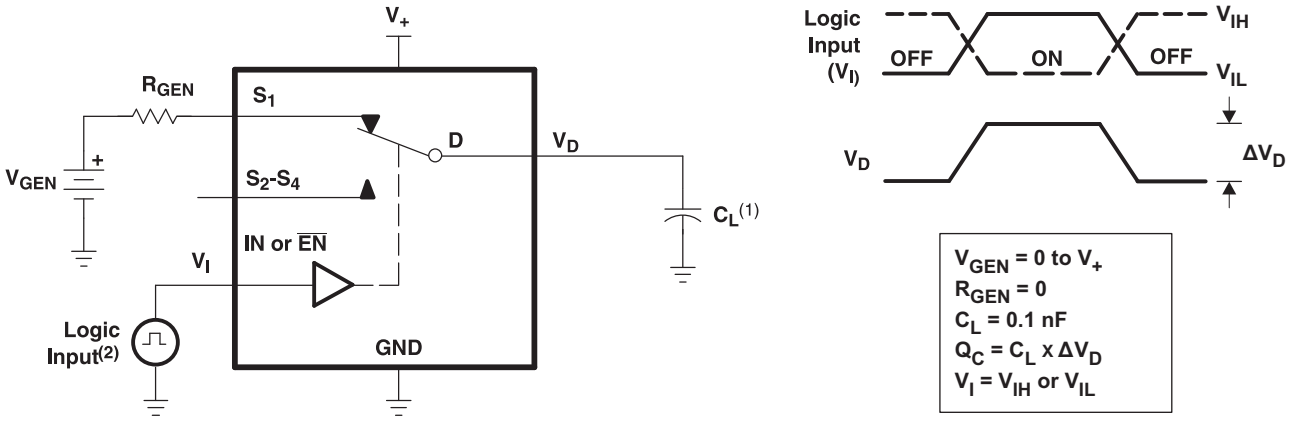


图 20. Adjacent Crosstalk (X_{TALK})

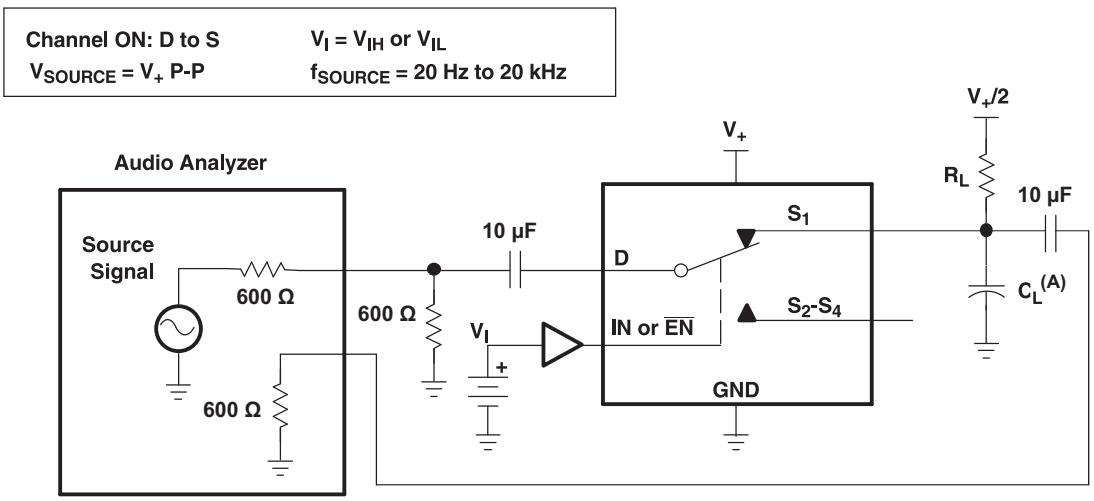
Parameter Measurement Information (接下页)



A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

图 21. Charge Injection (Q_C)



A. C_L includes probe and jig capacitance.

图 22. Total Harmonic Distortion (THD)

8 Detailed Description

8.1 Overview

The TS3A5017-Q1 is a dual Single-Pole-4-Throw (SP4T) solid-state analog switch. The TS3A5017-Q1, like all analog switches, is bidirectional. Each D pin connects to its four respective S pins, with the switch connection dependent on the status of $\overline{EN}$, IN2, and IN1. See 表 1 for the switch configuration truth table.

8.2 Functional Block Diagram

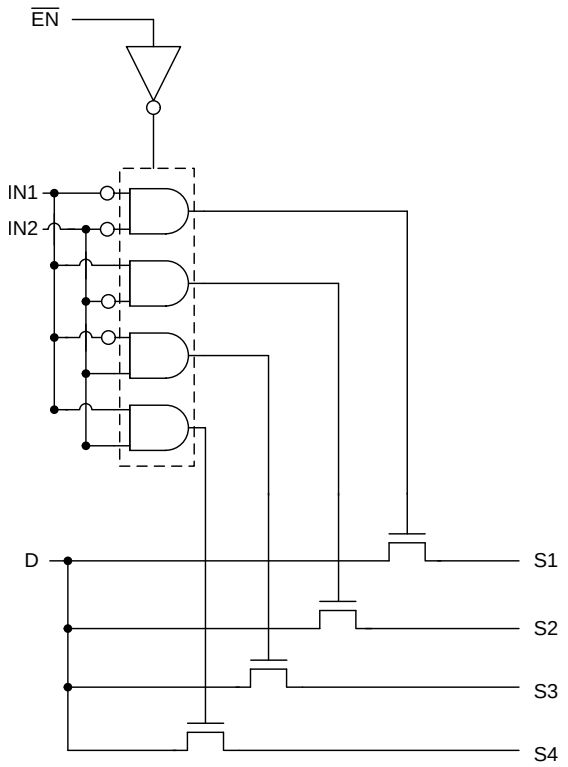


图 23. Functional Block Diagram (Each Switch)

8.3 Feature Description

Isolation in powered-down mode allows signals to be present at the inputs while the switch is powered off without causing damage to the device. The low ON-state resistance and low charge injection give the TS3A5017-Q1 better performance at higher speeds.

8.4 Device Functional Modes

表 1. Function Table

$\overline{EN}$	IN2	IN1	D TO S, S TO D
L	L	L	D = S_1
L	L	H	D = S_2
L	H	L	D = S_3
L	H	H	D = S_4
H	X	X	OFF

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS3A5017-Q1 can be used in a variety of customer systems. The TS3A5017-Q1 can be used anywhere multiple analog or digital signals must be selected to pass across a single line.

9.2 Typical Application

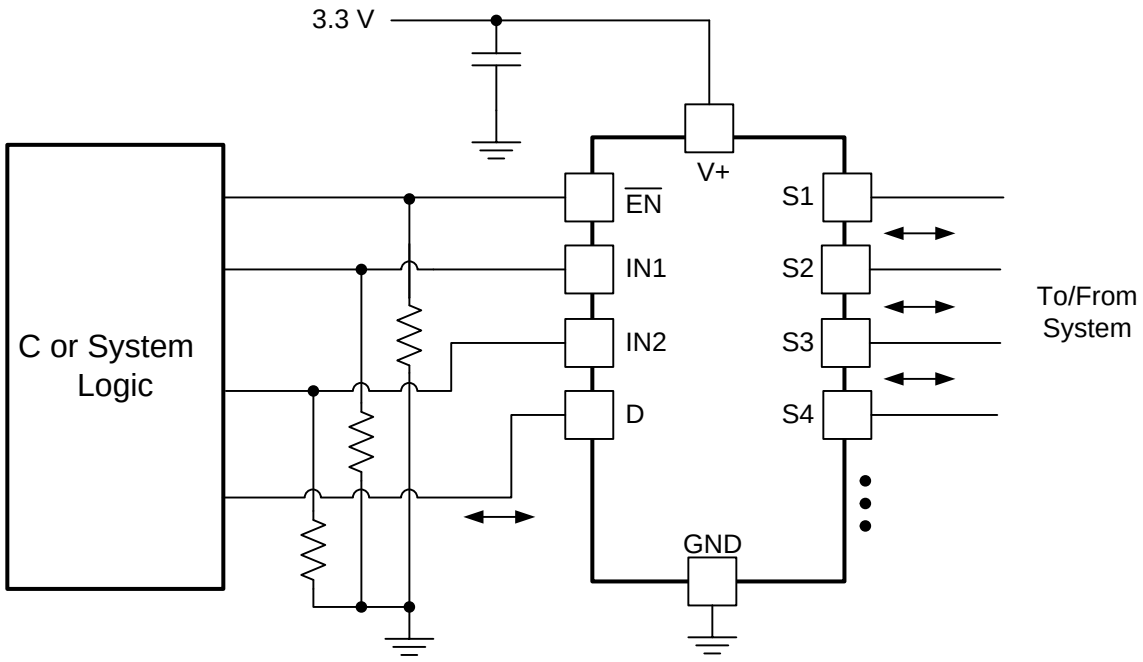


图 24. System Schematic for TS3A5017-Q1

9.2.1 Design Requirements

In this particular application, V+ was 3.3 V, although V+ is allowed to be any voltage specified in *Recommended Operating Conditions*. A decoupling capacitor is recommended on the V+ pin. See *Power Supply Recommendations* for more details.

9.2.2 Detailed Design Procedure

In this application, $\overline{EN}$, IN1, and IN2 are, by default, pulled low to GND. Choose these resistor sizes based on the current driving strength of the GPIO, the desired power consumption, and the switching frequency (if applicable). If the GPIO is open-drain, use pullup resistors instead.

Typical Application (接下页)

9.2.3 Application Curve

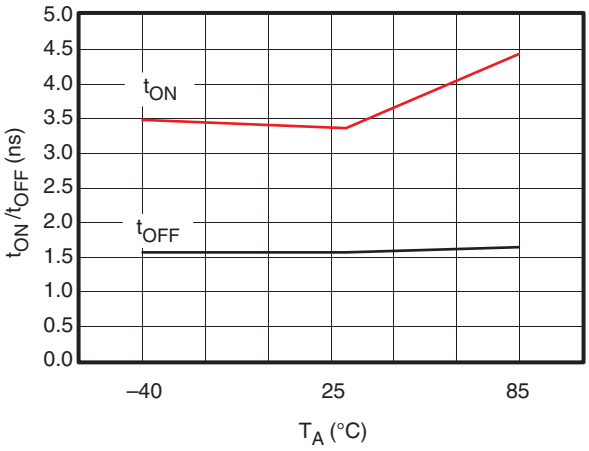


图 25. t_{ON} and t_{OFF} vs Temperature (V_+ = 3.3 V)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operation Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-µF or 0.022-µF capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-µF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and the traces will turn corners. 图 26 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

Unused switch I/Os, such as NO, NC, and COM, can be left floating or tied to GND. However, the IN1, IN2, and $\overline{EN}$ pins must be driven high or low. Due to partial transistor turnon when control inputs are at threshold levels, floating control inputs can cause increased I_{CC} or unknown switch selection states. See *Implications of Slow or Floating CMOS Inputs,* SCBA004 for more details.

11.2 Layout Example

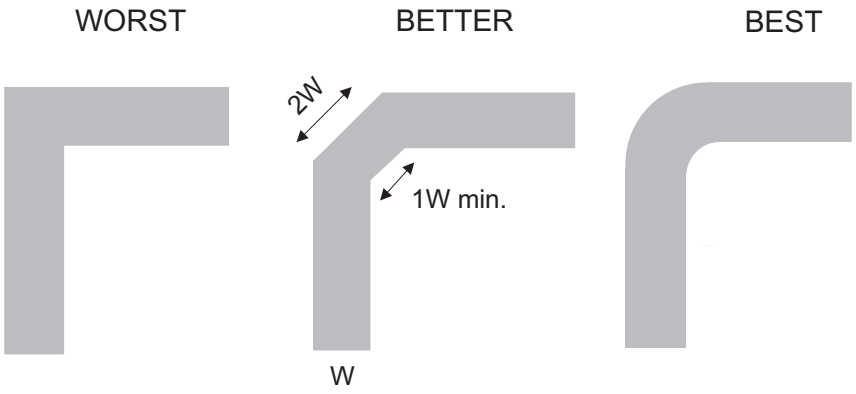


图 26. Trace Example

12 器件和文档支持

12.1 器件支持

12.1.1 器件命名规则

表 2. 参数 说明

符号	说明
V_{COM}	COM 处的电压
V_{NC}	NC 处的电压
V_{NO}	NO 处的电压
r_{on}	通道打开时 COM 和 NC 或 NO 端口之间的电阻
Δr_{on}	特定器件中通道间 r_{on} 的差值
$r_{on(flat)}$	额定条件范围下，同一通道内 r_{on} 最大值与最小值之间的差值
$I_{NC(OFF)}$	相应通道（NC 到 COM）处于关断状态时，在 NC 端口测得的泄漏电流
$I_{NC(ON)}$	相应通道（NC 到 COM）处于导通状态且输出 (COM) 处于开路状态时，在 NC 端口测得的泄漏电流
$I_{NO(OFF)}$	相应通道（NO 到 COM）处于关断状态时，在 NO 端口测得的泄漏电流
$I_{NO(ON)}$	相应通道（NO 到 COM）处于导通状态且输出 (COM) 处于开路状态时，在 NO 端口测得的泄漏电流
$I_{COM(OFF)}$	相应通道（COM 到 NC 或 NO）处于关断状态时，在 COM 端口测得的泄漏电流
$I_{COM(ON)}$	相应通道（COM 到 NC 或 NO）处于导通状态且输出 (NC 或 NO) 处于开路状态时，在 COM 端口测得的泄漏电流
V_{IH}	控制输入 (IN, $\overline{EN}$) 逻辑高电平的最小输入电压
V_{IL}	控制输入 (IN, $\overline{EN}$) 逻辑低电平的最大输入电压
V_I	控制输入 (IN, $\overline{EN}$) 处的电压
I_{IH}、I_{IL}	控制输入 (IN, $\overline{EN}$) 处测量的泄漏电流
t_{ON}	开关开通时间。此参数是在特定条件范围下，开关开通时，通过数字控制 (IN) 信号和模拟输出 NC 或 NO）信号之间的传播延迟测量得出。
t_{OFF}	开关关断时间。此参数是在特定条件范围下，开关开通时，通过数字控制 (OFF) 信号和模拟输出（NC 或 NO）信号之间的传播延迟测量得出。
Q_C	电荷注入是测量从控制 (IN) 输入到模拟（NC 或 NO）输入产生的不需要的信号耦合的方法。电荷注入以库仑为单位，可通过测量开关控制输入产生的总感应电荷得出该值。电荷注入，$Q_C = C_L \times \Delta V_{COM}$，$C_L$ 是负载电容，ΔV_{COM} 是模拟输出电压的变化。
$C_{NC(OFF)}$	相应通道（NC 到 COM）关闭时 NC 端口的电容
$C_{NC(ON)}$	相应通道（NC 到 COM）开启时 NC 端口的电容
$C_{NO(OFF)}$	相应通道（NO 到 COM）关闭时 NC 端口的电容
$C_{NO(ON)}$	相应通道（NO 到 COM）开启时 NC 端口的电容
$C_{COM(OFF)}$	相应通道（COM 到 NC）关闭时 COM 端口的电容
$C_{COM(ON)}$	相应通道（COM 到 NC）开启时 COM 端口的电容
C_I	控制输入 (IN, $\overline{EN}$) 电容
O_{ISO}	开关关断隔离用于衡量关断状态开关阻抗的大小。关断隔离以 dB 为单位，当相应通道（NC 到 COM）处于关断状态时，在额定频率下测量得出。
X_{TALK}	串扰是测量从开启状态的通道到关断状态的通道（NC1 到 NO1）产生的不必要信号耦合的方法。相邻串扰是测量从一条开启状态的通道到相邻开启状态的通道（NC1 到 NC2）产生的不必要信号耦合的方法。相邻串扰在额定频率下测量得出且以 dB 为单位。
BW	开关带宽。这是导通通道增益低于直流增益 -3dB 时的频率。
THD	总谐波失真用于描述由模拟开关导致的信号失真。其定义为二次、三次和更高次谐波与基波绝对幅度之比的均方根 (RMS) 值。
I_+	静态电源电流，以及 V_+ 或 GND 的控制 (IN) 引脚

12.2 文档支持

12.2.1 相关文档

- 《*慢速或浮点 CMOS 输入的影响*》，SCBA004

12.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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12.5 商标

E2E is a trademark of Texas Instruments.

12.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS3A5017QRGYRQ1	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5017Q
TS3A5017QRGYRQ1.B	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5017Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TS3A5017-Q1 :

- Catalog : TS3A5017

NOTE: Qualified Version Definitions:

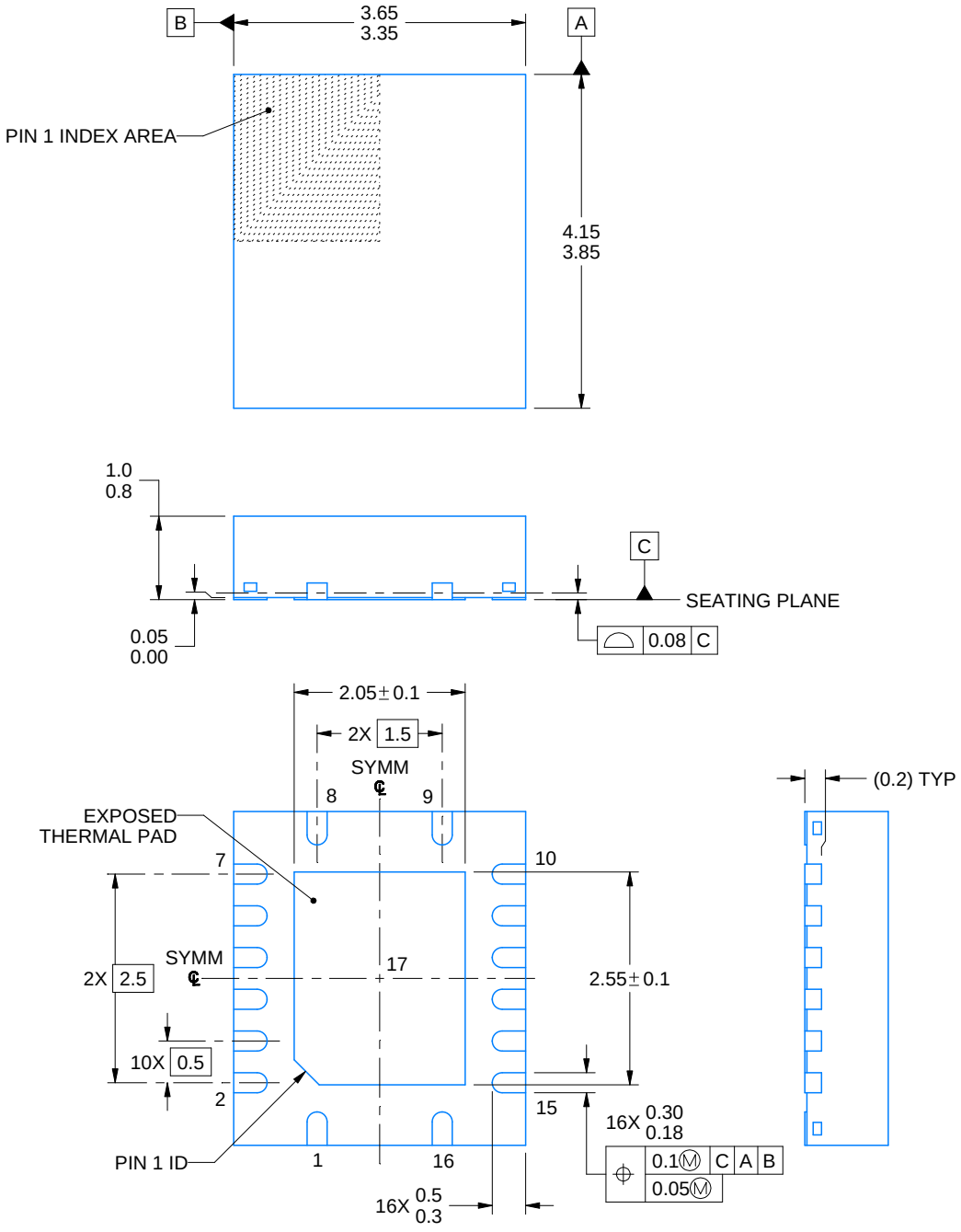
- Catalog - TI's standard catalog product

RGY0016A

PACKAGE OUTLINE

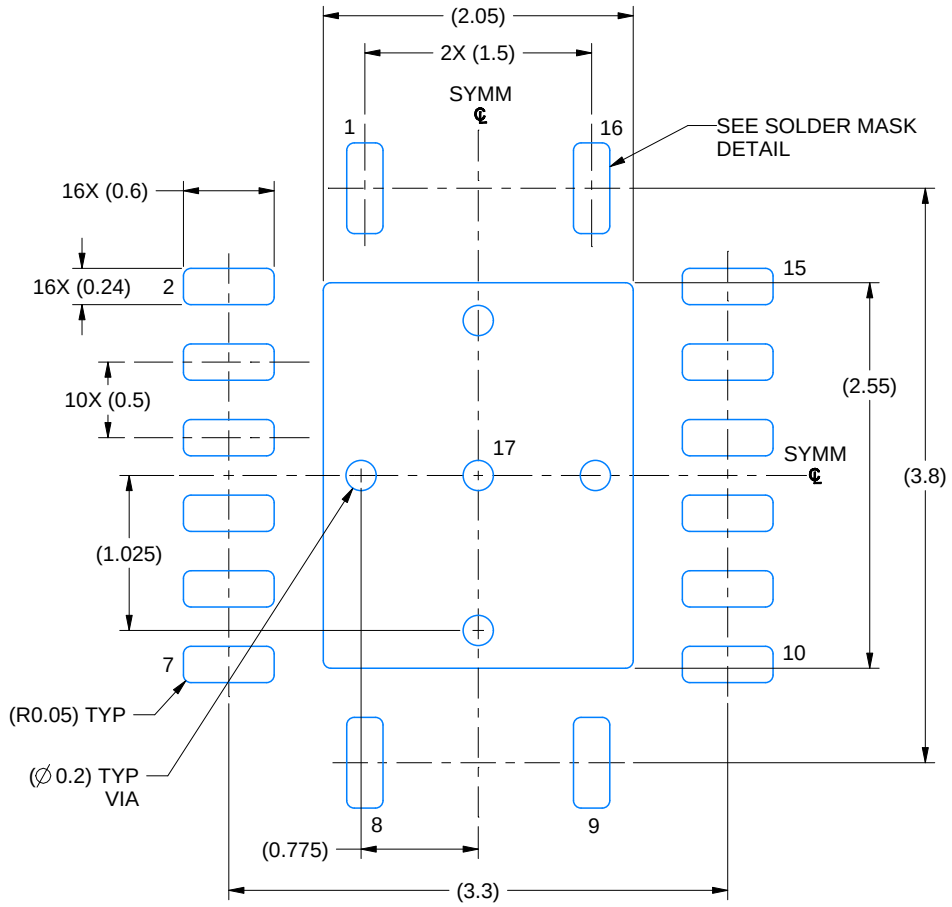
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

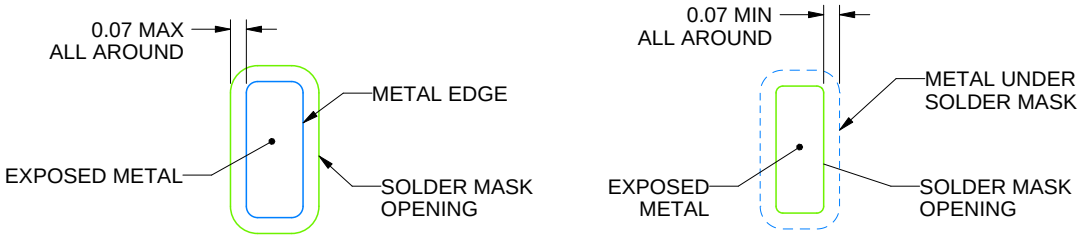


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

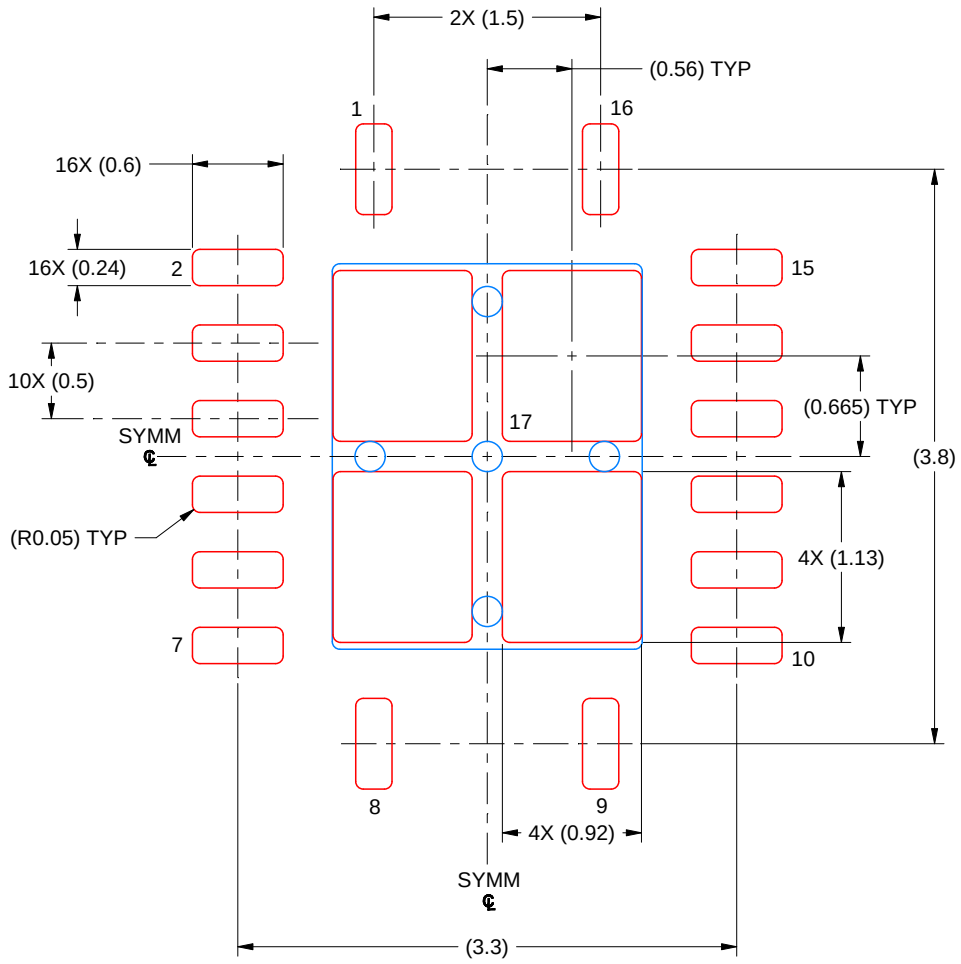


SOLDER MASK DETAILS

4225140/A 07/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225140/A 07/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

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