自主音频头戴式耳机开关

查询样品: **TS3A225E**

特性

- **V_{DD}范围 = 2.7V 至 4.5V**
- 打开立体声插孔开关前断开
- 针对接地场效应晶体管 **(FET)** 开关的 **Ron**
  - 晶圆级芯片封装 **(WCSP)**：**70mΩ**
  - 四方扁平无引线 **(QFN)** 封装：**100mΩ**
- **GND** 和麦克风连接的自主检测
- 由 **I^2C** 或外部触发引脚触发的检测
- **HDA** 兼容麦克风插入指示器
- **1.8V** 兼容 **I^2C** 开关控制
- 静电放电 **(ESD)** 性能测试符合 **JESD 22** 标准：
  - **2000V** 人体模型（**A114-B**，**II** 类）
  - **500V** 充电器件模型 **(C101)**
- **ESD** 性能 **(SLEEVE**，**RING2**，**TIP)**
  - **±8kV** 接触放电 **(IEC 61000-4-2)**

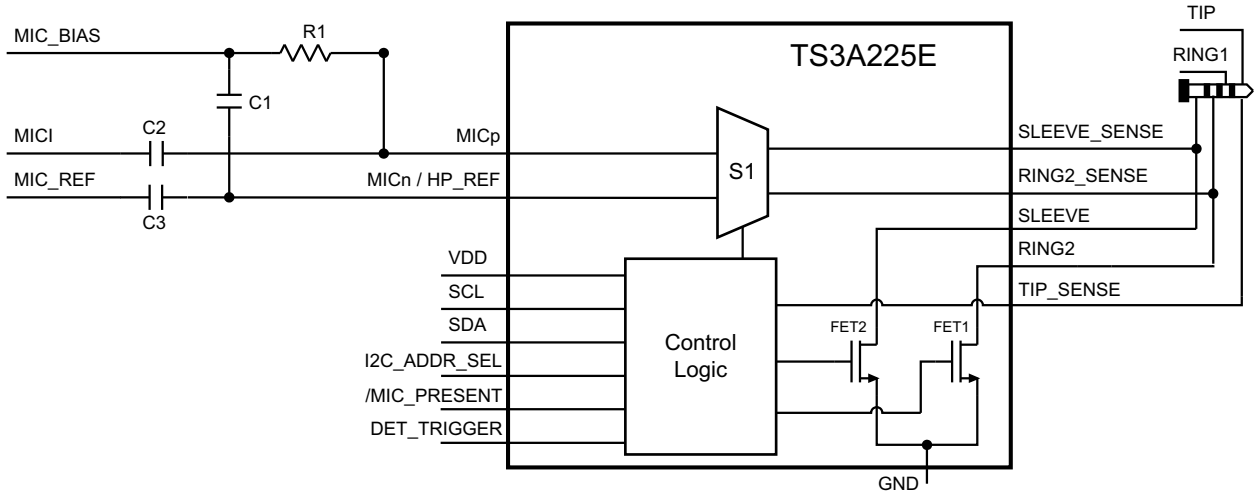
应用范围

- 手机/平板电脑
- 笔记本电脑

说明

TS3A225E 是一个音频头戴式耳机开关器件。 此器件可检测模拟麦克风是否存在，并在音频立体声插孔中的不同接头之间切换系统模拟麦克风引脚。 立体声接头中的麦克风连接可与接地连接互换，具体取决于制造商。 当 TAS3A225E 检测到一个特定配置时，器件会自动将麦克风线路连接到适当的引脚。 此器件还报告音频立体声插孔上插入的模拟麦克风。

在某些系统中，需要将立体声插孔引脚接地。 TS3A225E 提供用于接地短路的两个内部低电阻 (<100mΩ) FET 开关。



ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	RTE - QFN	Tape and reel	TS3A225ERTER	ZTL
	YFF - WCSP	Tape and reel	TS3A225EYFFR	YP225E

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

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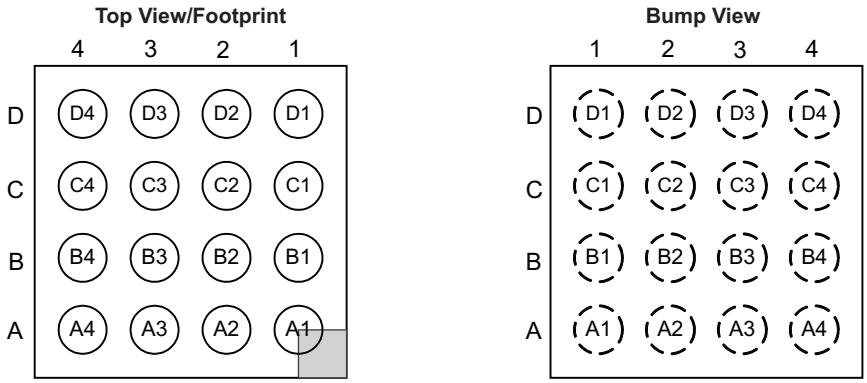
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PACKAGE OPTION #1: YFF- WCSP



Die Size: 1.56mm x 1.56mm (± 0.03mm)
Bump Size: 0.25mm
Bump Pitch: 0.4mm

Table 1. TS3A225E Pin Mapping (Top View)

	4	3	2	1
D	/MIC_PRESENT	TIP_SENSE	MICp	MICn
C	RING2	GND (1)	VDD (1)	RING2_SENSE
B	SLEEVE	GND (1)	VDD (1)	SLEEVE_SENSE
A	DET_TRIGGER	ADDR_SEL	SDA	SCL

(1) To ensure proper operation at least 1 of the VDD balls and at least 1 of the GND balls must be pad-connected.

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PIN DESCRIPTION – WCSP

PIN #	PIN		
WCSP	**NAME**	**TYPE**	**DESCRIPTION**
A1	SCL	I/O	Clock from I^2C bus. This can be connected to VDD if I^2C is not used.
A2	SDA	I/O	Bidirectional data from/to I^2C bus. This can be connected to VDD if I^2C is not used.
A3	ADDR_SEL	I/O	This pin is used to change the device I2C address in an I^2C system to avoid address conflict. Please see the External Pin Connection section for more details. This pin can be grounded if not needed.
A4	DET_TRIGGER	I/O	A rising edge from low to high on this pin triggers the detection. This pin can be connected to the headset jack to allow automatic pull-up to supply after headset insertion to initialize detection sequence. The detection trigger can be disabled or activated in I^2C
B1	SLEEVE_SENSE	I/O	Connected to the SLEEVE segment of the jack. If SLEEVE segment on plug is MIC signal, this is connected to MICp. If not, this is connected to MICn and becomes the remote sensing feedback for the headphone.
B2	VDD	Supply	Power supply
B3	GND	Ground	Headphone ground connection (Current return path to headphone amplifier), switch ground reference.
B4	SLEEVE	I/O	Headphone current return path if SLEEVE is GND for headset. Connect to SLEEVE with low DCR trace.
C1	RING2_SENSE	I/O	Connected to the RING2 segment of the jack. If RING2 segment on plug is MIC signal, this is connected to MICp. If not, this is connected to MICn and becomes the remote sensing feedback for the headphone.
C2	VDD	Supply	Power supply
C3	GND	Ground	Headphone ground connection (Current return path to headphone amplifier), switch ground reference.
C4	RING2	I/O	Headphone current return path if RING2 is GND for headset. Connect to RING2 with low DCR trace.
D1	MICn	I/O	Microphone signal reference connection to codec.
D2	MICp	I/O	Microphone signal connection to codec. Microphone bias should be fed into this pin.
D3	TIP_SENSE	I/O	Connected to the TIP segment of the headphone jack
D4	/MIC_PRESENT	Output	Open Drain output. When pulled-low, it indicate that a mic is detected on the headset (switch for HDA sense resistor or INT output in an I2S based system. Default behavior is a hardware pulldown for HDA resistor. Programmable through I2C into an interrupt.)

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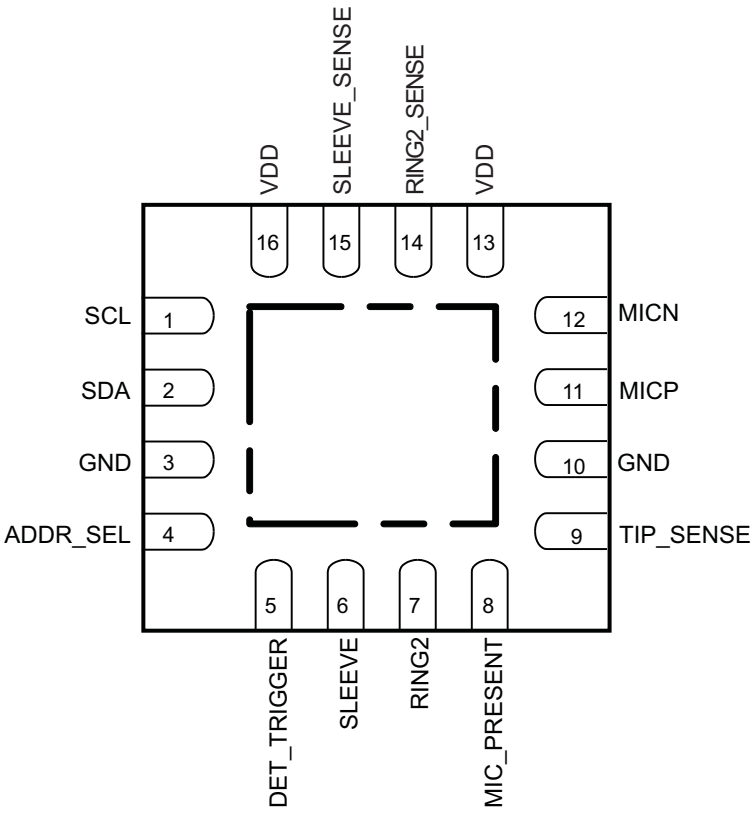
PACKAGE OPTION #2: RTE- QFN



Top View
Package Size: 3 mm x 3 mm
Pitch: 0.5 mm

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PIN DESCRIPTION – QFN

PIN #	PIN		
QFN	**NAME**	**TYPE**	**DESCRIPTION**
1	SCL	I/O	Clock from I^2C bus. This can be connected to VDD if I^2C is not used.
2	SDA	I/O	Bidirectional data from/to I^2C bus. This can be connected to VDD if I^2C is not used.
3	GND	Ground	Headphone ground connection (Current return path to headphone amplifier), switch ground reference.
4	ADDR_SEL	I/O	This pin is used to change the device I2C address in an I^2C system to avoid address conflict. Please see the External Pin Connection section for more details. This pin can be grounded if not needed.
5	DET_TRIGGER	I/O	A rising edge from low to high on this pin triggers the detection. This pin can be connected to the headset jack to allow automatic pull-up to supply after headset insertion to initialize detection sequence. The detection trigger can be disabled or activated in I^2C
6	SLEEVE	I/O	Headphone current return path if SLEEVE is GND for headset. Connect to SLEEVE with low DCR trace.
7	RING2	I/O	Headphone current return path if RING2 is GND for headset. Connect to RING2 with low DCR trace.
8	/MIC_PRESENT	Output	Open Drain output. When pulled-low, it indicate that a mic is detected on the headset (switch for HDA sense resistor or INT output in an I2S based system. Default behavior is a hardware pulldown for HDA resistor. Programmable through I2C into an interrupt.)
9	TIP_SENSE	I/O	Connected to the TIP segment of the headphone jack
10	GND	Ground	Headphone ground connection (Current return path to headphone amplifier), switch ground reference.
11	MICp	I/O	Microphone signal connection to codec. Microphone bias should be fed into this pin.
12	MICn	I/O	Microphone signal reference connection to codec.
13	VDD	Supply	Power supply
14	RING2_SENSE	I/O	Connected to the RING2 segment of the jack. If RING2 segment on plug is MIC signal, this is connected to MICp. If not, this is connected to MICn and becomes the remote sensing feedback for the headphone.
15	SLEEVE_SENSE	I/O	Connected to the SLEEVE segment of the jack. If SLEEVE segment on plug is MIC signal, this is connected to MICp. If not, this is connected to MICn and becomes the remote sensing feedback for the headphone.
16	VDD	Supply	Power supply

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FUNCTIONAL BLOCK DIAGRAM

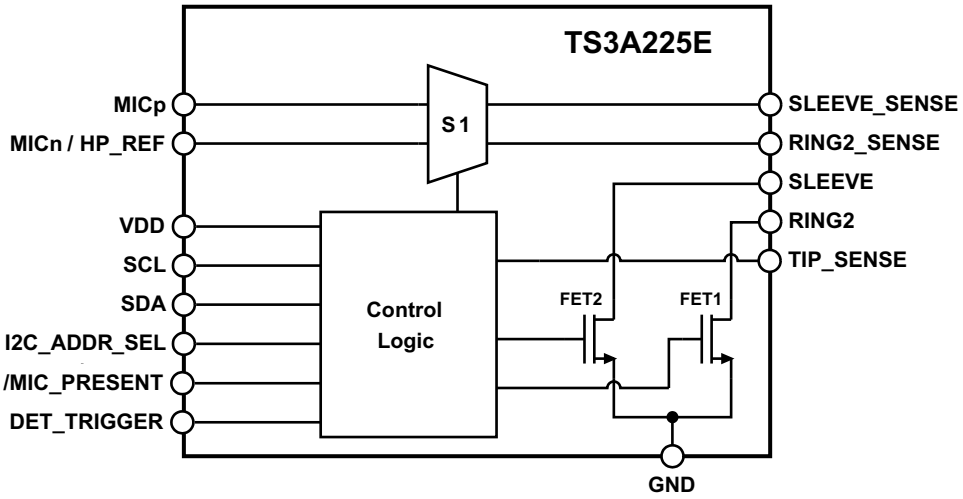

Figure 1. Functional Block Diagram

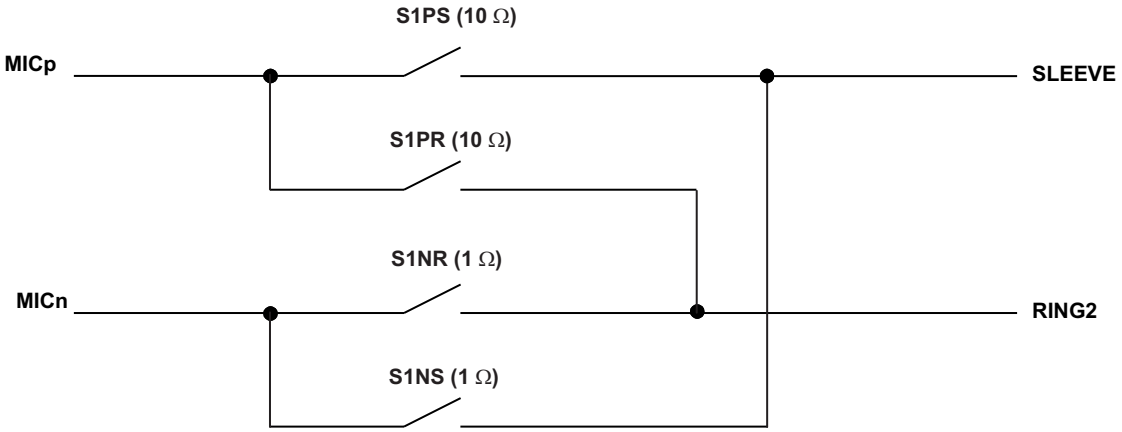

Figure 2. S1 Mux Details

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ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_I	Voltage range on V_{DD} (3)	–0.3 to 5	V
	Voltage range on SCL, SDA, ADDR_SEL, DET_TRIGGER, MICP, MICN, SLEEVE_SENSE, RING2_SENSE, RING2, SLEEVE(3)	–0.3 to V_{DD}+0.5	V
T_A	Operating ambient temperature range	-40 to 85	°C
$T_{J\ (MAX)}$	Maximum operating junction temperature	125	°C
T_{stg}	Storage temperature range	–65 to 150	°C
ESD rating	Machine model (JESD 22 A115)	100	V
	Charge device model (JESD 22 C101)	500	V
	Human body model (JESD 22 A114)	2	kV
	Contact discharge on SLEEVE_SENSE, RING2_SENSE, RING2, SLEEVE, TIP_SENSE (IEC 61000-4-2)	8	kV

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application (Ω_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$
(3) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{DD}	Supply voltage range		2.7	4.5	V
V_{IN}	Digital input voltage range (SDA, SCL, ADDR_SEL, DET_TRIGGER)		0	V_{DD}	V
V_{IO}	Input/Output voltage range (SLEEVE, SLEEVE_SENSE, RING2, RING2_SENSE, MICP, MICN)		0	V_{DD}	V
$V_{IO(TIP)}$	Input/Output voltage range for TIP		–2	V_{DD}	V
V_{IH}	Input logic high	SDA, SCL, ADDR_SEL	1.2	4.5	V
		DET_TRIGGER	$V_{DD} \times 0.65$	V_{DD}	V
V_{IL}	Input logic low	SDA, SCL, ADDR_SEL	0	0.4	V
		DET_TRIGGER	0	$V_{DD} \times 0.40$	V
T_A	Operating temperature range		–40	85	°C

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ELECTRICAL CHARACTERISTICS

Unless otherwise noted the specification applies over the V_{DD} range and operating junction temp –40°C ≤ T_A ≤ 70°C. Typical values are for V_{DD} = 3.3V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Input voltage range		2.7	3.3	4.5	V
I_{DD}	Quiescent current	V_{MIC} = 1.8 V to V_{DD}		8	10	µA
V_{OL}	SDA output high voltage	I_{OL} = 3 mA			0.3	V
I_{IN-I2C}	SCL, SDA input leakage	V_{MIC} = 1.8 V to V_{DD}		0.1	1	µA
$I_{IN-ADDR}$	ADDR input leakage	V_{MIC} = 0 V		0.1	1	µA
SWITCH RESISTANCE						
$R_{F1\ (WCSP)}$	FET1 on resistance (WCSP Package)	V_{DD} = 2.7 V, V_{GND} = 0 V, I_{GND} = 10 mA (see Figure 3)		70		mΩ
$R_{F1\ (QFN)}$	FET1 on resistance (QFN Package)			100		mΩ
$R_{F2\ (WCSP)}$	FET2 on resistance (WCSP Package)			70		mΩ
$R_{F2\ (QFN)}$	FET2 on resistance (QFN Package)			100		mΩ
R_{S1PS}	S1PS on resistance	V_{DD} = 2.7 V, $V_{SLEEVE_SENSE/RING2_SENSE}$ = 0 V to 2.7 V, I_{MIC} = ±10 mA (see Figure 4)			10	Ω
R_{S1PR}	S1PR on resistance				10	Ω
R_{S1NS}	S1NS on resistance				1	Ω
R_{S1NR}	S1NR on resistance				1	Ω
$R_{MIC_PRESENT}$	/MIC_PRESENT pin output resistance	V_{DD} = 2.7 V			25	Ω
SWITCH LEAKAGE CURRENT						
$I_{OFF-0.1}$	FET1 and FET2 off leakage	V_{IN} = 0 V to 2.7 V, V_{OUT} = 0 V, V_{DD} = 4.5V (see Figure 5)			1	µA
I_{OFF-1}	S1NS, S1NR off leakage				1	µA
I_{OFF-10}	S1PS, S1PR off leakage				1	µA
I_{ON-1}	S1NS, S1NR on leakage	V_{IN} = 0 V to 2.7 V, V_{OUT} = 0 V, V_{DD} = 4.5 V (see Figure 6)			1	µA
I_{ON-10}	S1PS, S1PR on leakage				1	µA
SWITCH DYNAMIC CHARACTERISTICS						
PSR_{217}	Power supply rejection, R_L = 5 Ω (see Figure 7)	V = 200 mV_{PP}, f = 217 Hz		–100		dB
PSR_{1k}		V = 200 mV_{PP}, f = 1 kHz		–80		dB
PSR_{20k}		V = 200 mV_{PP}, f = 20 kHz		–50		dB
ISO_{S1}	SLEEVE_SENSE or RING2_SENSE to MICP Isolation (see Figure 8)	V = 200 mV_{PP}, f = 20 kHz, R_L = 50Ω		–100		dB
SEP_{S1}	SLEEVE_SENSE to RING2_SENSE Separation	V = 200 mV_{PP}, f = 20 kHz, $_{RL}$ = 50Ω (see Figure 9)		–60		dB
THD_{200}	Total Harmonic Distortion (see Figure 10)	V = 200mV_{PP}, f = 20-20 kHz, R_S = 600Ω		0.003 %		
THD_{500}		V = 500mV_{PP}, f = 20-20kHz, R_S = 600Ω		0.002 %		
t_{BBM}	Break-Before-Make Off Time	Default		30		µs
		BBM register bit = 1'b1		60		µs
t_{DETC}	Detection sequence duration			360	500	ms

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I2C INTERFACE TIMING REQUIREMENTS

Unless otherwise noted the specification applies over the V_{DD} range and operating junction temp –40°C ≤ T_J ≤ 70°C.

PARAMETER		STANDARD MODE I^2C BUS		FAST MODE I^2C BUS		UNIT
		MIN	MAX	MIN	MAX	
f_{scl}	I^2C clock frequency	0	100	0	400	kHz
t_{sch}	I^2C clock high time	4		0.6		µs
t_{scl}	I^2C clock low time	4.7		1.3		µs
t_{sp}	I^2C spike time		50		50	ns
t_{sds}	I^2C serial-data setup time	250		100		ns
t_{sdh}	I^2C serial-data hold time	0		0		ns
t_{icr}	I^2C input rise time		1000	21	300	ns
t_{icf}	I^2C input fall time		300	21	300	ns
t_{ocf}	I^2C output fall time (C_L = 10 pF to 400 pF)		300	$20+0.1C_b$ (1)	300	ns
t_{bus}	I^2C bus free time between Start and Stop conditions	4.7		1.3		µs
t_{sts}	I^2C Start or repeat Start condition setup	4.7		0.6		µs
t_{sth}	I^2C Start or repeat Start condition hold	4		0.6		µs
t_{sps}	I^2C Stop condition setup	4		0.6		µs
$t_{vd(data)}$	SCL low to SDA output valid		1		1	µs
$t_{vd(ack)}$	Valid-data time, ACK from SCL low to SDA low		1		1	µs
c_b	I^2C bus load	0	400	0	400	pF

(1) C_b = total capacitance of one bus line in pF.

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PARAMEER MEASUREMENT INFORMATION

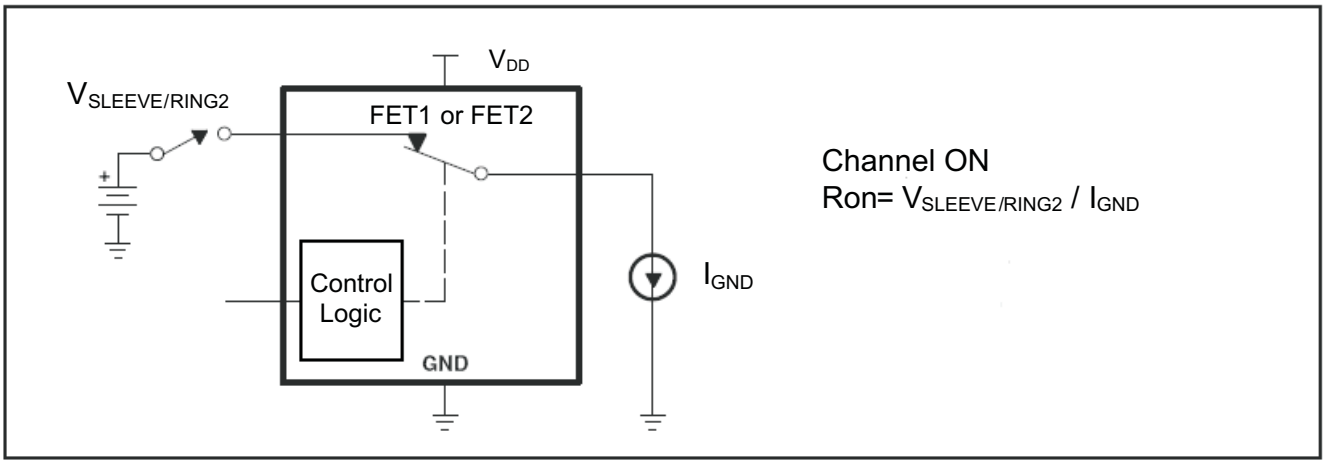

Figure 3. FET1/FET2 On Resistance Measurement

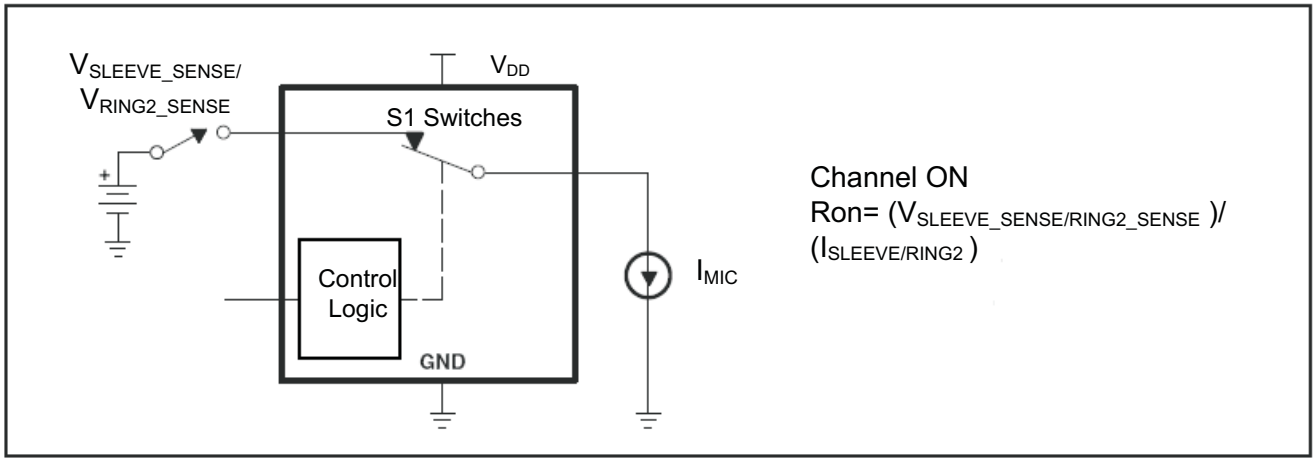

Figure 4. S1 Switch On Resistance Measurement

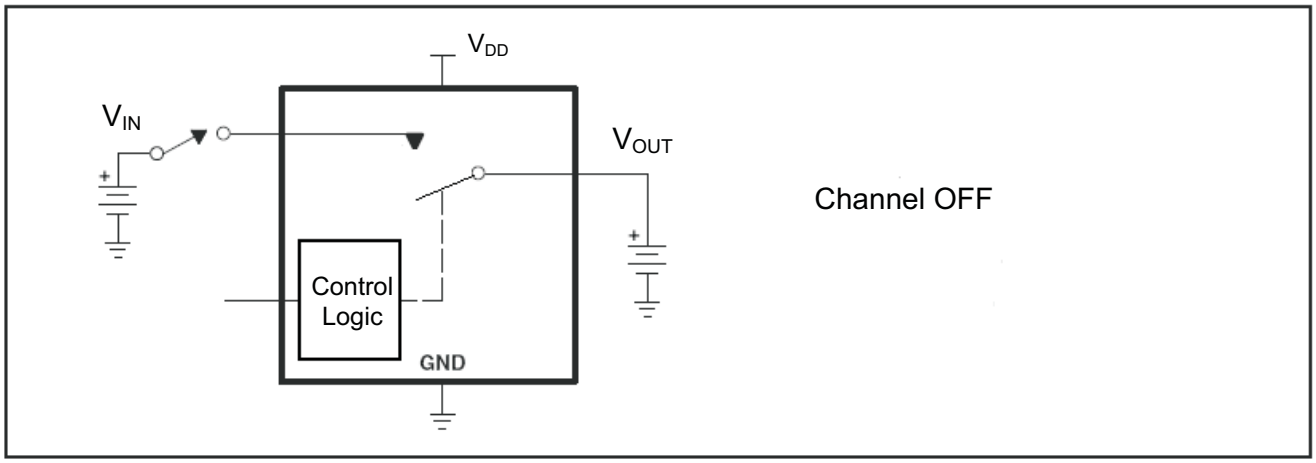

Figure 5. Switch Off Leakage Current Measurement

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PARAMEER MEASUREMENT INFORMATION (continued)

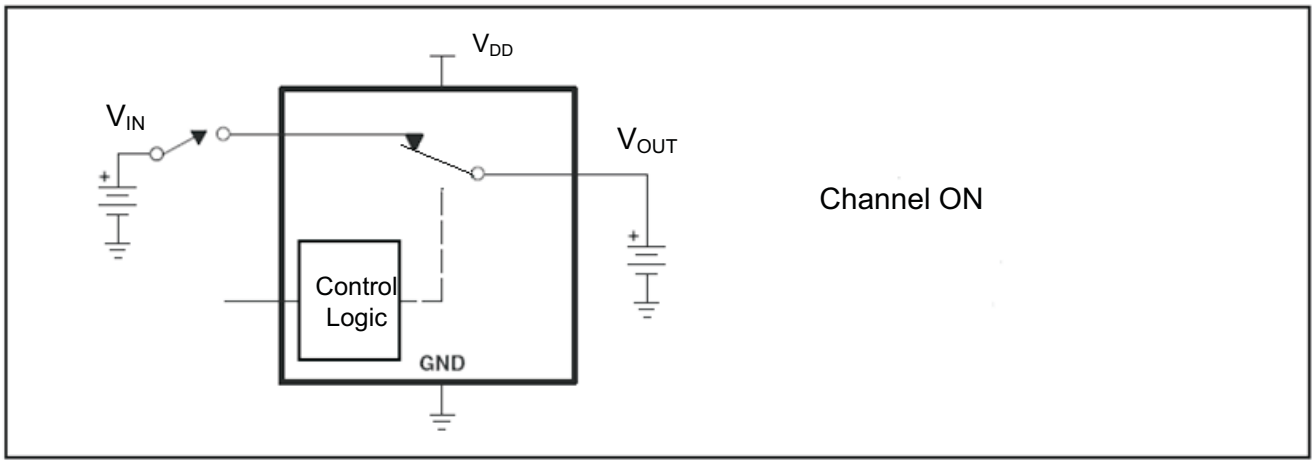


Figure 6. Switch On Leakage Current Measurement

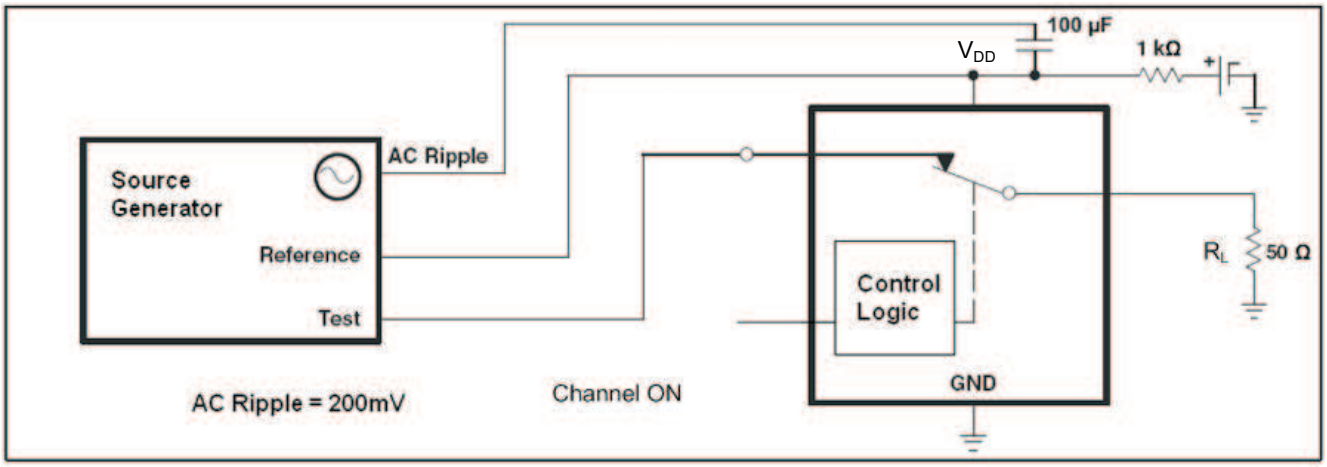


Figure 7. Power Supply Rejection Ratio (PSRR)

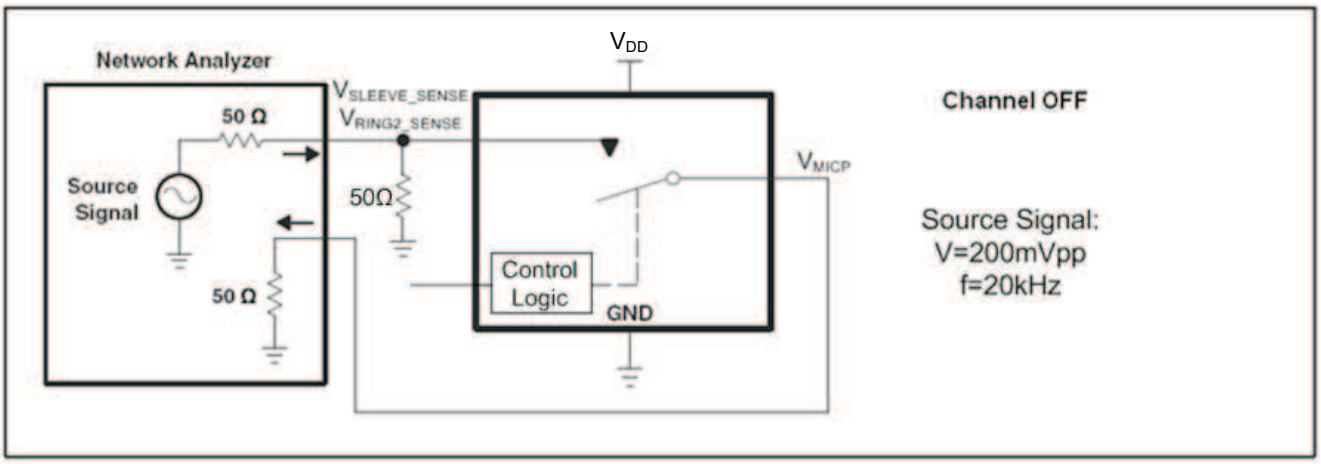


Figure 8. OFF-Isolation

PARAMEER MEASUREMENT INFORMATION (continued)

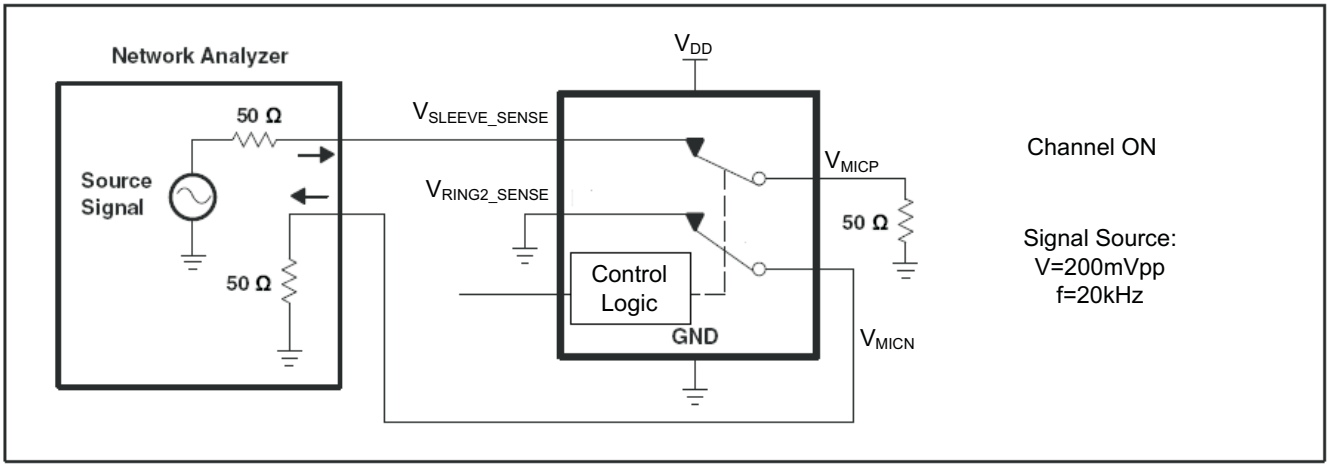
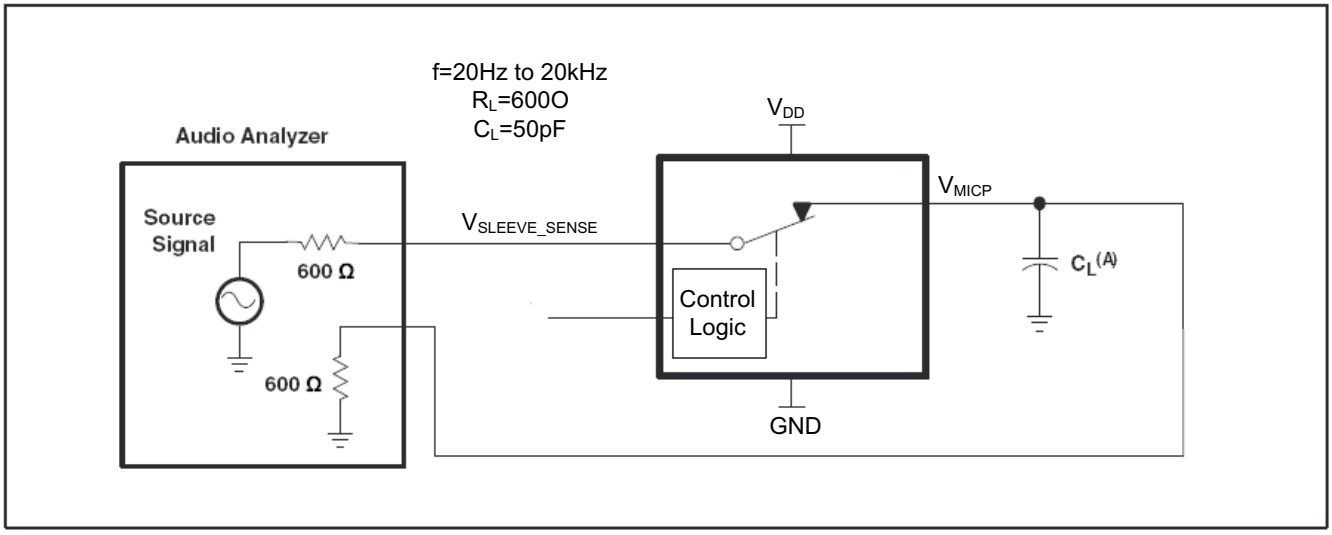


Figure 9. Channel Separation



A. C_L includes probe and jig capacitance.

Figure 10. Total Harmonic Distortion (THD)

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PARAMEER MEASUREMENT INFORMATION (continued)

GND FET On Resistance

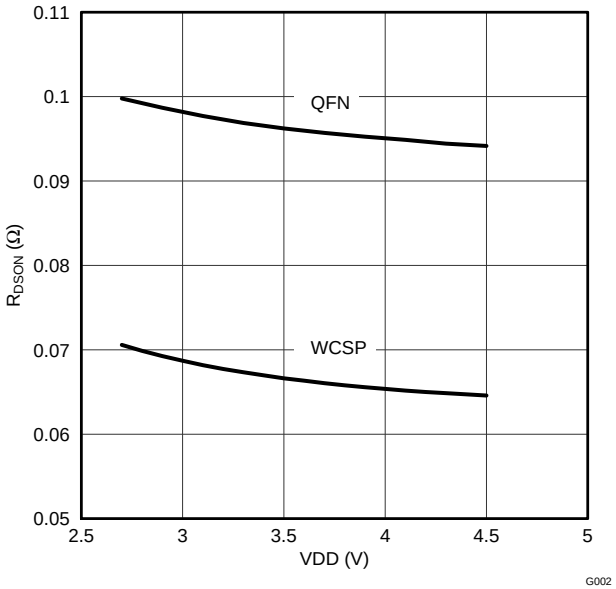

Figure 11. GND FET On Resistance

DESCRIPTION OF OPERATION

GENERAL OPERATION

The TS3A225E is an audio headset switch device that detects the existence and polarity of a microphone connected to a headset. Upon detection of a microphone the TS3A225E automatically connects a system analog microphone pin to the appropriate audio jack connection. The device also routes the system microphone GND to the proper jack connection.

The detection sequence is initiated via I^2C command or the external trigger detection (DET_TRIGGER) pin. The automatic routing feature can be disabled by I^2C command. Additionally, all the switches of TS3A225E can be manually controlled by I^2C register. See the I^2C register usage section for details.

EXTERNAL PIN CONNECTION

(1) HARDWARE MODE

The TS3A225E can be used in a non- I2C system in which the controls are performed via external pins. The following table summarizes how the external pins should be connected in a non- I^2C system:

PIN	CONNECT TO	DETAILED DESCRIPTION
SCL/SDA	V_{DD}	In a non- I^2C system, these two pins should be tied directly to V_{DD} to emulate the default state in an I^2C commutation protocol.
I2C_ADDR_SEL	V_{DD} or GND	In a non- I^2C system this pin has no use and should be grounded.
/MIC_Present	None	This is an output pin and can be read to check whether microphone is detected. This pin will be driven low upon microphone detection.
DET_TRIGGER	Rising edge initiates detection	In a non- I^2C system, this pin needs to be manually asserted to initiate a headset detection sequence. A rising edge on this pin triggers the detection.

(2) I^2C Mode

In an I^2C system, the external pins should be connected as follows:

PIN	CONNECT TO	NOTE
SCL/SDA	I^2C buses	SCL/SDA pins should be connected to the corresponding I2C buses in an I2C system
I2C_ADDR_SEL	V_{DD} or GND	This pin is used to modify the device I2C address in an I2C system to avoid address conflict. The address can be changed as follows:

I2C_ADDR_SEL Pin	Address	Read/Write
0*	8'h76	Write
	8'h77	Read
1	8'h78	Write
	8'h79	Read

*This is the factory programmed value

/MIC_Present	None	By default, this is an output pin. This pin will be driven low upon microphone detection and will remain low until another detection event. In an I^2S system, this pin can also serve as interrupt for I2C register update. See the I^2C register usage section for more details.
DET_TRIGGER	Rising edge initiates detection	In an I^2C system, detection sequence can be initiated via the I2C DET_TRIGGER register or this DET_TRIGGER external pin. A rising edge on this pin triggers the detection.

MICROPHONE PRESENT INDICATOR

The TS3A225E detects whether or not a microphone is present on an inserted audio stereo jack. If a microphone is detected, the TS3A225E pulls the /MIC_PRESENT pin low and also indicates the presence of the microphone in an I^2C register. The /MIC_PRESENT connection is an open-drain output with a maximum on resistance of 25 Ω. This makes the /MIC_PRESENT pin compatible with HDA standards (if /MIC_PRESENT is asserted low when connected to an external 5.1 kΩ pull-up resistor, the effective series resistance of the MIC_PRESENT transistor + pull-up resistor will be changed by less than 0.5%).

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The /MIC_PRESENT pin can also be used as an interrupt flag in I2S based systems. The pin can be programmed via I^2C to pull low when a microphone is present (the pin's default function), to act as an I^2C interrupt when a microphone is detected, or it can be completely disabled.

MICROPHONE POLARITY DETECTION

Microphone polarity is automatically detected by the TS3A225E when running the diagnostic sequence. Microphone polarity is accurately detected under all common connection scenarios for the TIP_SENSE pin including a GND centered amplifier, a non-GND centered (AC-coupled) amplifier, or an amplifier with a tri-stated output.

Microphone detection is not guaranteed if either TIP or RING1 are transmitting audio signals during the detection sequence. To assure proper detection, do not output audio from the headphone amplifier until detection sequence is complete (500 ms after insertion).

It should also be noted that this device is backward compatible with headsets that include send/end functions. However, it should be specified that the user not to hold down the send/end button while the headset is being plugged since it may cause inaccurate microphone detection and the headset may need to be re-plugged.

Microphone polarity is defined by impedance to system GND as noted in the table below in a 4-prong headset:

Connection	Impedance to GND (Ω)
R (Ring1)	16 ~ 1500
L (Tip)	16 ~ 1500
Mic (Ring2 or Sleeve)	600 ~ 3000

SWITCH MANUAL CONTROL

In addition to fully automatic switching (the default mode), the TS3A225E's switches can also be manually controlled for increased flexibility. All switches are open by default, and each switch can be controlled individually via the CTRL2 register setting or based on one of the preset modes used in the CTRL1 register. The following outline the proper steps to perform manual switching:

Step 1: Disable auto switching by setting AUTO_SW_DIS in CTRL3 to 1.

Step 2: Change /Mic_present bit to I^2C interrupt by setting I2C_INT register in CTRL3 to 1.

Step 3: Initialize detection by asserting the DET_TRIGGER register or the DET_TRIGGER external pin. After detection, the DAT1 registers store the detection result and they can be read to get the headset information. CTRL1 will stay in isolation mode '000' after detection since auto switching has been disabled.

Step 4: Manually control the switches by using one of the preset modes in CTRL1 ('010' to '110') or change the mode of CTRL1 to '111' to control each switch individually based on CTRL2 register settings. The /MIC_PRESENT pin can be manually pulled down by setting **b4** of the CTRL3 register to '1'.

STANDARD I2C INTERFACE DETAILS

The bidirectional I2C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I2C communication with this device is initiated by the master sending a START condition, a high-to-low transition on the SDA input/output while the SCL input is high (see). After the start condition, the device address byte is sent, MSB first, including the data direction bit (R/W). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse.

The data byte follows the address ACK. The R/W bit is kept low for transfer from the master to the slave. The data byte is followed by an ACK sent from this device. Data are output only if complete bytes are received and acknowledged. The output data is valid at time (tpv) after the low-to-high transition of SCL, during the clock cycle for the ACK.

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On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (START or STOP) (see).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure). The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

A slave receiver that is addressed must generate an ACK after the reception of each byte. The device that acknowledges has to pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 12). Setup and hold times must be taken into account.

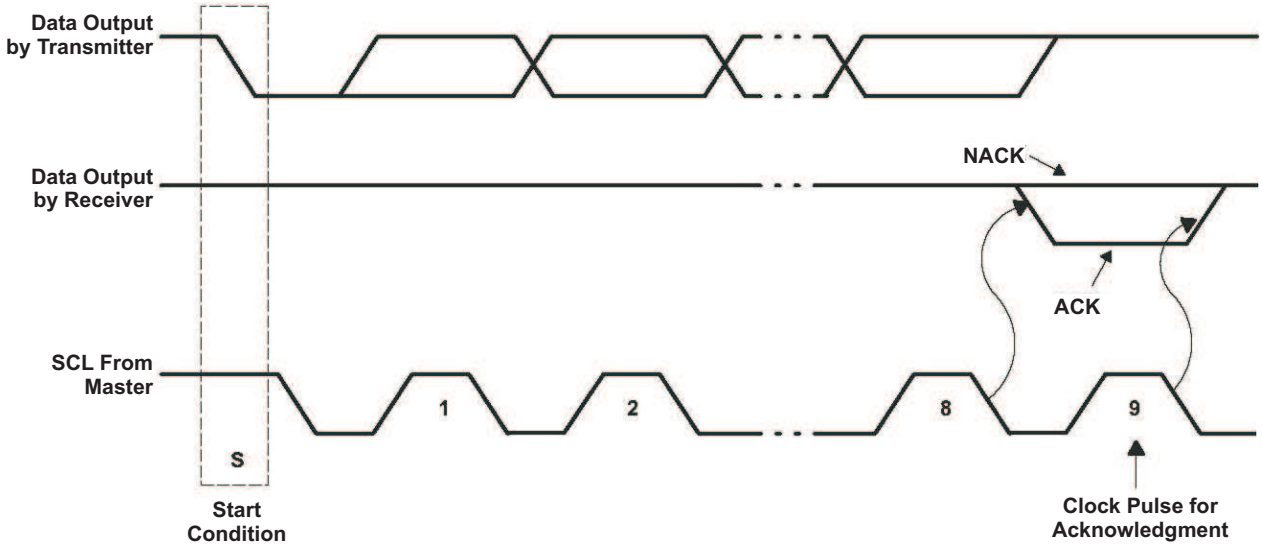

Figure 12. Acknowledgment on I²C Bus

WRITES OPERATION

Data is transmitted to the TS3A225E by sending the device slave address and setting the LSB to a logic 0 The command byte is sent after the address and determines which register receives the data that follows the command byte. The next byte is written to the specified register on the rising edge of the ACK clock pulse. See Figure 13 and Figure 14 for the two modes of Write operations.

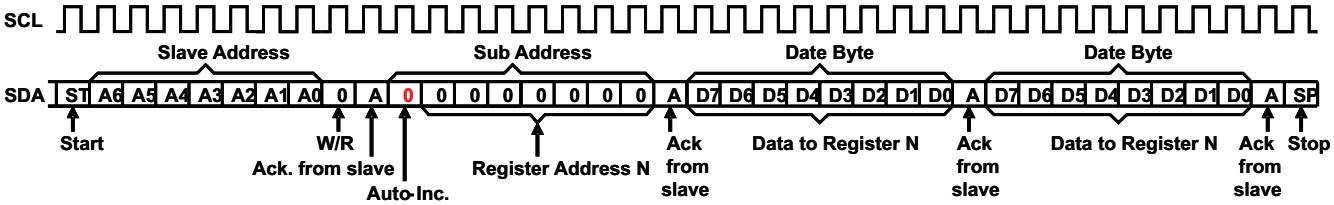

Figure 13. Repeated Data Write to a Single Register

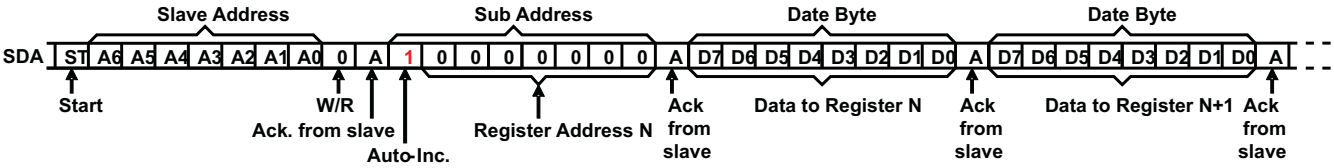

Figure 14. Burst Data Write to Multiple Registers

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READS OPERATION

The bus master first must send the TS3A225E slave address with the LSB set to logic 0. The command byte is sent after the address and determines which register is accessed. After a restart, the device slave address is sent again but, this time, the LSB is set to logic 1. Data from the register defined by the command byte then is sent by the TS3A225E. Data is clocked into the SDA output shift register on the rising edge of the ACK clock pulse. See Figure 15Figure 18 to Figure 18 for different modes of Reads Operation.

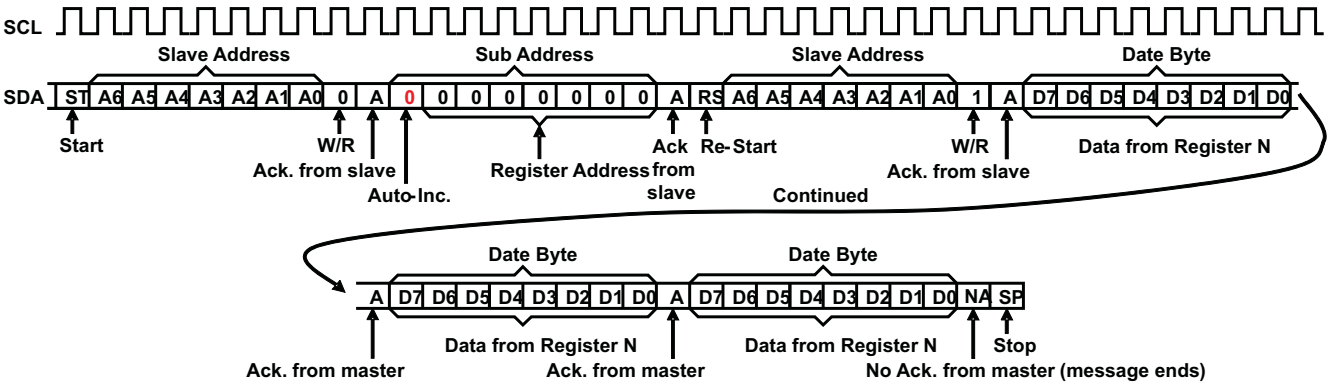

Figure 15. Repeated Data Read from a Single Register – Combined Mode

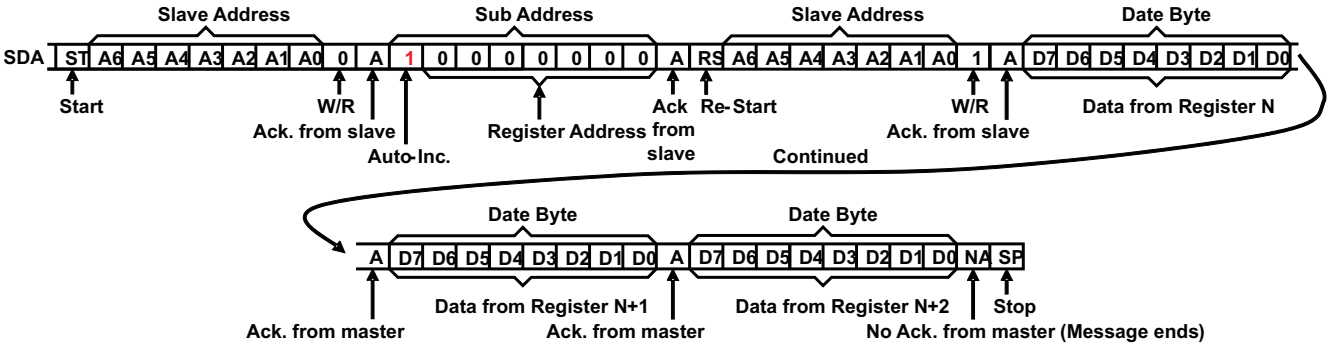

Figure 16. Burst Data Read from Multiple Registers – Combined Mode

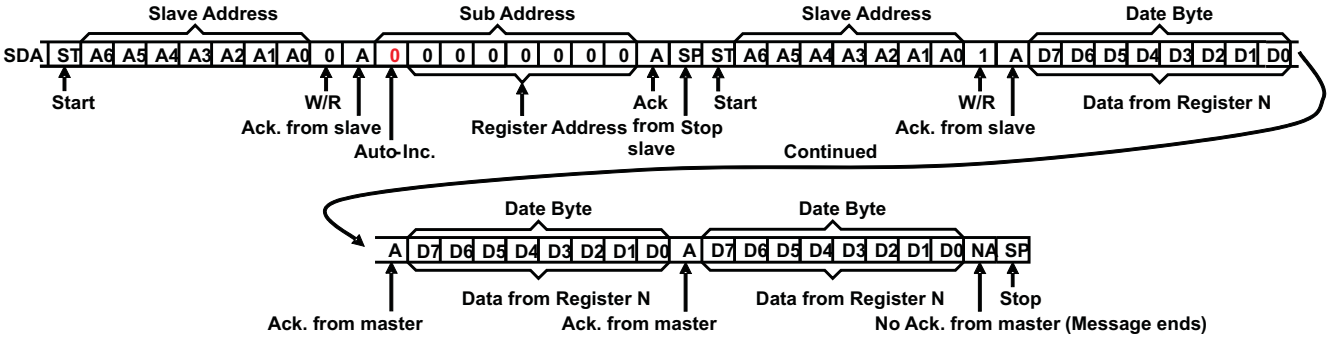

Figure 17. Repeated Data Read from a Single Register – Split Mode

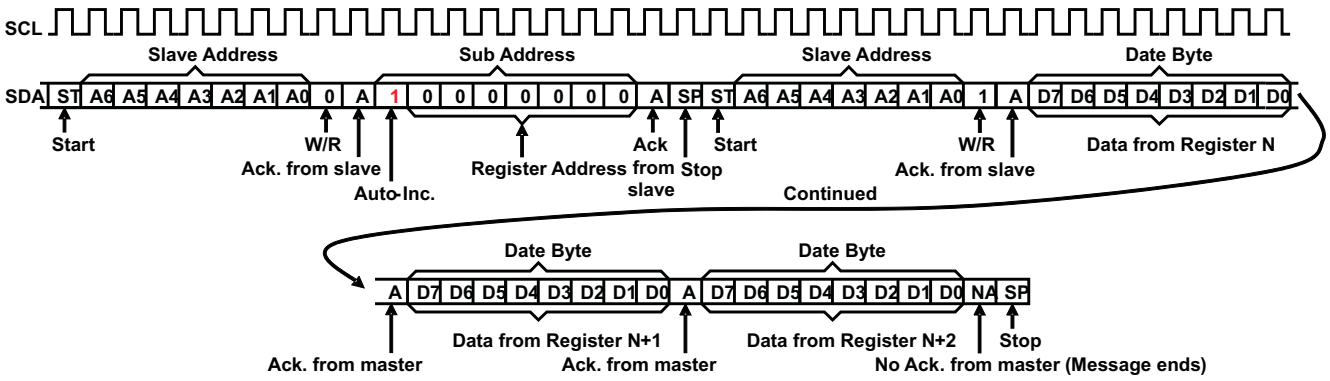

Figure 18. Burst Data Read from Multiple Registers – Split Mode

Notes:

1. SDA is pulled low on Ack. from slave or Ack. from master.
2. Register writes always require sub-address write before first data byte.
3. Repeated data writes to a single register continue indefinitely until Stop or Re-Start.
4. Repeated data reads from a single register continue indefinitely until No Ack. from master.
5. Burst data writes start at the specified register address, then advance to the next register address, even to the read-only registers and continue until Stop or Re-Start. For the read-only registers, data write appears to occur, though no data are changed by the writes.
6. Burst data reads start at the specified register address, then advance to the next register address and continues until No Ack. from master.

REGISTER MAP

Addr (xxh)	Name	Type	Reset Value	b7	b6	b5	b4	b3	b2	b1	b0
0x01	ID	R	NA								
0x02	CTRL1	R/W	0x00					BBM	MODE[2:0]		
0x03	CTRL2	R/W	0x00	S1NR	S1NS	S1PR	S1PS			FET1	FET2
0x04	CTRL3	R/W	0x00				/MIC_ PRESENT MANUAL	DET_TRIG_ DIS	I2C_INT	AUTO_DET_ DIS	DET_ TRIGGER
0x05	DAT1	R	0x00		GND_LOC	SLEEVE_Z[2:0]			RING2_Z[2:0]		
0x06	INT	R	0x00					DET_ ERROR		MIC_PRESENT	STD_TSR
0x07	INT Mask	R/W	0x00				I2C_INT MASK	DET_ ERROR MASK		MIC_PRESENT MASK	STD_TSR MASK

REGISTER DESCRIPTION

1. ID

Address : 0x01 Reset Value : N/A Type : Read

NAME	SIZE(BITS)	DESCRIPTION
Device ID	8	Unique Revision Number

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2. CTRL1

Address : 0x02 Reset Value : 0x00 Type : Read and Write

NAME	SIZE(BITS)	DESCRIPTION	Data [7:0]
RESERVED	4		
BBM	1	0: Disable break-before-make functionality	xxxx0xxx
		1: Enable break-before-make functionality	xxxx1xxx
MODE	3	000: Isolation. All Switch open. This is the default state.	xxxxx000
		001: Reserved	xxxxx001
		010: Normal Single Ended (FET1, S1NR, S1PS closed)	xxxxx010
		011: Reverse Single Ended (FET2, S1NS, S1PR closed)	xxxxx011
		100: Normal Differential (S1NR, S1PS closed)	xxxxx100
		101: Reversed Differential (S1NS, S1PR closed)	xxxxx101
		110: 3Prong (FET1, FET2, S1NS, S1NR closed)	xxxxx110
		111: Manual (I2C mode) with all switches open. Switch position controlled via CTRL2	xxxxx111

3. CTRL2

Address : 0x03 Reset Value : 0x00 Type : Read and Write

NAME	SIZE(BITS)	DESCRIPTION	Data [7:0]
S1NR	1	0: S1NR Switch Disabled when MODE[2:0] = 3'b111 in CTRL1	0xxxxxxx
		1: S1NR Switch Enabled when MODE[2:0] = 3'b111 in CTRL1	1xxxxxxx
S1MS	1	0: S1NS Switch Disabled when MODE[2:0] = 3'b111 in CTRL1	x0xxxxxx
		1: S1NS Switch Enabled when MODE[2:0] = 3'b111 in CTRL1	x1xxxxxx
S1PR	1	0: S1PR Switch Disabled when MODE[2:0] = 3'b111 in CTRL1	xx0xxxxx
		1: S1PR Switch Enabled when MODE[2:0] = 3'b111 in CTRL1	xx1xxxxx
S1PS	1	0: S1PS Switch Disabled when MODE[2:0] = 3'b111 in CTRL1	xxx0xxxx
		1: S1PS Switch Enabled when MODE[2:0] = 3'b111 in CTRL1	xxx1xxxx
Reserved	2		
FET1	1	0: FET1 Disabled when MODE[2:0] = 3'b111 in CTRL1	xxxxxx0x
		1: FET1 Enabled when MODE[2:0] = 3'b111 in CTRL1	xxxxxx1x
FET2	1	0: FET2 Disabled when MODE[2:0] = 3'b111 in CTRL1	xxxxxxx0
		1: FET2 Enabled when MODE[2:0] = 3'b111 in CTRL1	xxxxxxx1

4. CTRL3

Address : 0x041 Reset Value : 0x00 Type : Read and Write

NAME	SIZE(BITS)	DESCRIPTION	Data [7:0]
Reserved	3		
/MIC_PRESENT MANUAL	1	0: Default	xxx0xxxx
		1: Set this bit to 1 manually pull the /MIC_PRESENT output low	Xxx1xxxx
DET_TRIG_DIS	1	0: Enables initiation of a detect sequence through the external DET_TRIGGER pin (default)	xxxx0xxx
		1: Disables initiation of a detect sequence through the external DET_TRIGGER pin	xxxx1xxx
I2C_INT	1	0: /MIC_PRESENT pin used to indicate presence of microphone on output (default)	xxxxx0xx
		1: /MIC_PRESENT pin serves as interrupt for I2C register updates	xxxxx1xx
AUTO_SW_DIS	1	0: Enables auto switching after detection (default)	xxxxxx0x
		1: Disables auto switching after detection	xxxxxx1x
DET_TRIGGER	1	0: default	xxxxxxx0
		1: Initiates a detection through I2C control*	xxxxxxx1

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5. DAT1

Address : 0x05 Reset Value : 0x00 Type : Read and Write

NAME	SIZE(BITS)	DESCRIPTION	Data [7:0]
Reserved	1		
GND_LOC	1	0: GND Segment is located on Ring2 band	x0xxxxxx
		1: GND Segment is located on Sleeve band	x1xxxxxx
SLEEVE_Z	3	000: Impedance between Tip and Sleeve is <400Ω	xx000xxx
		001: 400Ω ≤ Impedance between Tip and Sleeve <800Ω	xx001xxx
		010: 800Ω ≤ Impedance between Tip and Sleeve <1200Ω	xx010xxx
		011: 1200Ω ≤ Impedance between Tip and Sleeve <1600Ω	xx011xxx
		100: 1600Ω ≤ Impedance between Tip and Sleeve <2000Ω	xx100xxx
		101: 2000Ω ≤ Impedance between Tip and Sleeve <2400Ω	xx101xxx
		110: 2400Ω ≤ Impedance between Tip and Sleeve <2800Ω	xx110xxx
		111: Impedance between Tip and Sleeve ≥ 2800 Ω	xx111xxx
RING2_Z	3	000: Impedance between Tip and Ring2 <400Ω	xxxxx000
		001: 400Ω ≤ Impedance between Tip and Ring2 <800Ω	xxxxx001
		010: 800Ω ≤ Impedance between Tip and Ring2 <1200Ω	xxxxx010
		011: 1200Ω ≤ Impedance between Tip and Ring2 <1600Ω	xxxxx011
		100: 1600Ω ≤ Impedance between Tip and Ring2 <000Ω	xxxxx100
		101: 2000Ω ≤ Impedance between Tip and Ring2 <2400Ω	xxxxx101
		110: 2400Ω ≤ Impedance between Tip and Ring2 <2800Ω	xxxxx110
		111: Impedance between Tip and Ring2 ≥ 2800 Ω	xxxxx111

6. INT

Address : 0x06 Reset Value : 0x00 Type : Read

NAME	SIZE(BITS)	DESCRIPTION	Data [7:0]
Reserved	4		
DET_ERROR	1	0: default	xxxx0xxx
		1: Detection sequence completed without successful detection of either a standard plug or a plug with MIC	xxxx1xxx
Reserved	1		
MIC_PRESENT	1	0: default	xxxxxx0x
		1: A microphone detected on either RING2 or SLEEVE	xxxxxx1x
STD_TSR	1	0: default	xxxxxxx0
		1: A standard TSR headset detected, RING2 and SLEEVE shorted	xxxxxxx1

7. INT MASK

Address : 0x07 Reset Value : 0x00 Type : Read and Write

NAME	SIZE(BITS)	DESCRIPTION	Data [7:0]
Reserved	3		
I2C_INT_MASK	1	0: default	xxx0xxxx
		1: Tri-state /MIC_PRESENT pin	xxx1xxxx
DET_ERROR MASK	1	0: default	xxxx0xxx
		1: Mask DET_ERROR from setting an I2C interrupt	xxxx1xxx
Reserved	1		
MIC_PRESENT MASK	1	0: default	xxxxxx0x
		1: Mask MIC_PRESENT from setting an I2C interrupt	xxxxxx1x
STD_TSR MASK	1	0: default	xxxxxxx0
		1: Mask STD_TSR from setting an I2C interrupt	xxxxxxx1

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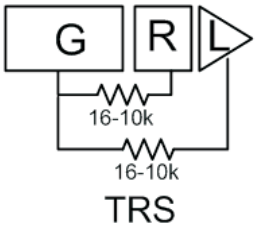
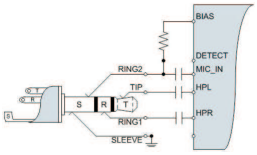
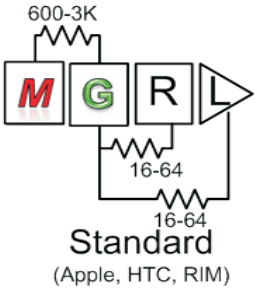
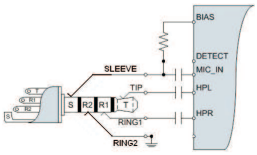
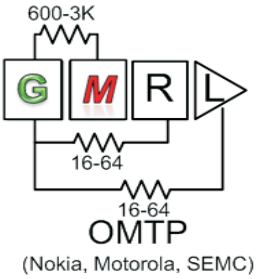
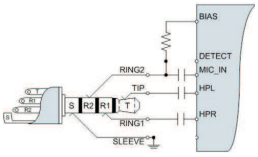
APPLICATION INFORMATION

APPENDIX: TS3A225E APPLICATION GUIDELINE

The TS3A225E is an audio headset switch device. The device detects the presence of an analog microphone and switches a system analog microphone pin between different connectors in an audio stereo jack. There are two different headset connector configurations currently available: TRS and TRRS. The TRS is comprised of a tip, ring, and sleeve connections while the TRRS contains a tip, ring1, ring2, and sleeve connections. The additional ring connection in the TRRS provides a microphone connection to the headset. Currently, there are two configurations for the TRRS: the Standard and OMTP (Open Mobile Terminal Platform) headsets. The difference between these two configurations is that the GND and Microphone bands are switched. Table 1 below depicts the differences between the TRS and the 2 types of TRRS headsets and their range of internal impedance values between the bands.

Table 2. Headset Configuration

Physical Connector	Internal Impedance	Pin Configuration		Connector Structure
		Pin Name	Configuration	
		Tip	Audio Left	
		Ring	Audio Right	
		Sleeve	Ground	
		Tip	Audio Left	
		Ring 1	Audio Right	
		Ring 2	Ground	
		Sleeve	Microphone	
		Tip	Audio Left	
		Ring 2	Audio Right	
		Ring 2	Ground	
		Sleeve	Microphone	

The TS3A225E detects one of the configurations above by going through a series of impedance detection steps. The device automatically connects the microphone line to the appropriate pin after the detection result becomes available. The device also routes the system microphone GND to the proper jack connection to establish appropriate GND return path. Therefore, TS3A225E provides the capability to use one single universal headset jack to accept both types of microphone headsets.

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Reference Schematic

The following figure (Figure 19) is the reference circuit that is recommended to be used to connect the TS3A225E between the audio combo jack and audio CODEC. Table 2 below listed the suggested passive components to be used in the system.

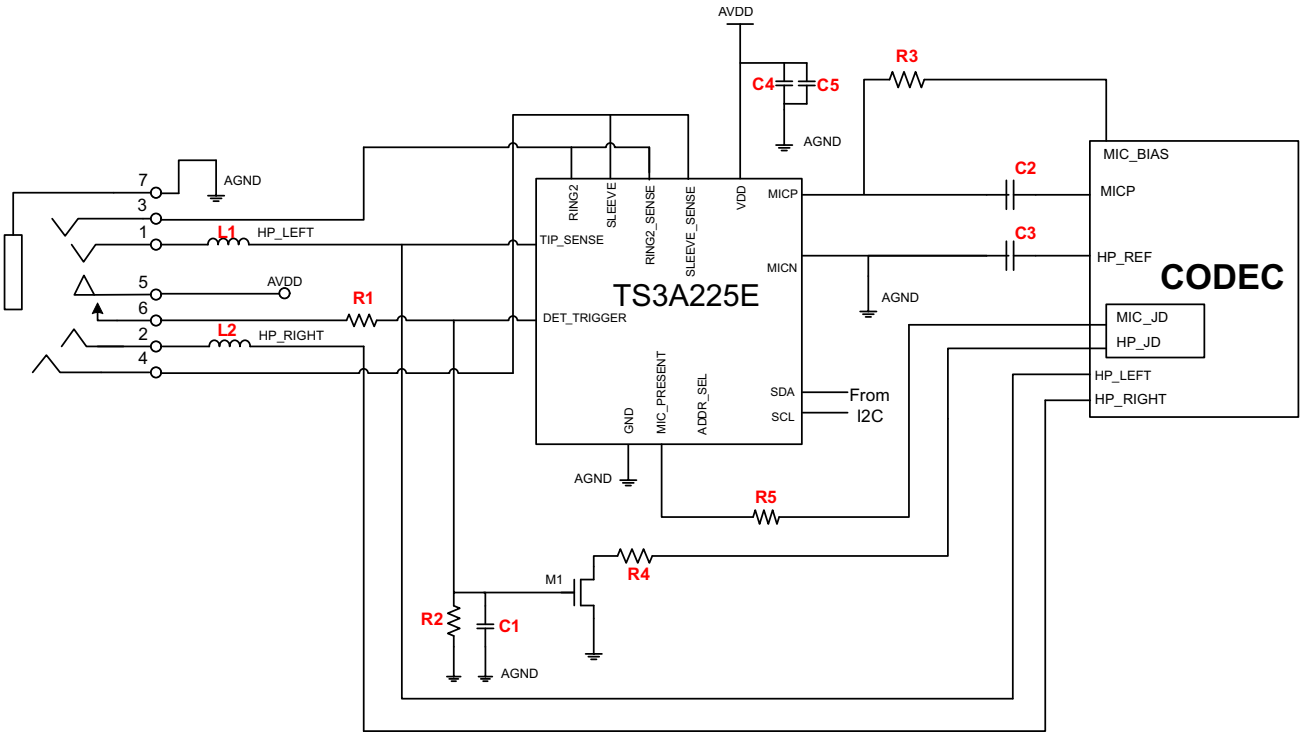

Figure 19. TS3A225E Reference Schematic

Table 3. Components Description

Capacitor	Value	Resistor	Value	Ferrite Bead	Value
C1	1 µF	R1	1 kΩ	L1, L2	N/A
C2	1 µF	R2	100 kΩ		
C3	1 µF	R3	2.2 kΩ		
C4	10 µF	R4	39.2 Ω		
C5	1 µF	R5	20 kΩ		

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Detailed Application Recommendation

The followings are the recommended usages for TS3A225E.

- To properly initiate the detection sequence of TS3A225E, the DET_TRIGGER pin needs to be configured correctly. The detection is triggered with a low to high transition on the DET_TRIGGER pin. To configure this function automatically through hardware, consider using an audio jack similar to the one shown in Figure 1 and connect pin 5 to VDD and pin 6 to GND through a 100k resistor. With this setup, the DET_TRIGGER pin is normally pulled low without a headset plugged-in and goes high when jack is inserted. To smooth out the low-to-high transition and to mitigate “slow plug-in” issue (discussed in the next section), R and C are recommended to be added to the DET_TRIGGER pin (R1 and C1). It’s recommended to have C1 > 1uF. The value of R1 can be adjusted depending on the audio jack used. A good default value to start with is 1kΩ.
- The DET_TRIGGER signal can also be utilized to implement the headphone sense (HP_JD) feature of the audio CODEC. When used together with a MOSFET (M1), this pin can be connected to the HP_JD pin (or any other relevant pin) of the audio CODEC to indicate a headset has been plugged-in. The CODEC can then turns on the left and right channel audios after a specific amount of delay (> detection period of TS3A225E = 360ms). The value of R4 may change depending on CODEC used.
- The MIC_PRESENT pin is an open-drain output and will be pulled low when a microphone is detected by TS3A225E. This pin can be connected directly to the MIC_JD pin on the CODEC to indicate the system a microphone is connected. The value of R5 may change depending on the CODEC used.
- The SLEEVE and RING2 pins should be routed to the actual headset jack connections with low impedance traces (wide, short traces). SLEEVE_SENSE and RING2_SENSE should not use the same traces and they can be much narrower and higher in impedance as they will be fed into high impedance inputs looking into the CODEC. On the CODEC side of the switch, the MICn / HP_REF connection should be fed into the HP_REF input of the CODEC. Utilizing the HP_REF input on CODECs typically improves cross talk by 10-15 dB. Not all CODECs have these inputs, but almost all newly released CODECs have this feature.
- The TIP_SENSE pin goes to the left channel of the audio headphone (HP_LEFT). The right channel does not go through the TS3A225E. Ferrite Beads (L1 and L2) are recommended on these 2 paths to filter out high frequency noises on the audio channels.
- Parallel 10uF and 1uF standard decoupling capacitor are recommended for the supply to decouple noises on the power rail.
- The SDA/SCL pins are connected to the I2C interfaces of the MCU. They maybe pulled up to VDD via resistors if no I2C control is needed. The ADDR_SEL pin is a GPIO-controlled pin for changing TS3A225E’s slave address to avoid system address conflict. If this feature is not needed, ADDR_SEL can be grounded.

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Special Note on Slow Headset Plug-In Issue

In real-world scenario a user might plug in the headset to the audio jack very slowly. This creates a challenging case for TS3A225E's detection mechanism and detection error might occur if care is not taken when designing the components around the TS3A225E. The main concern for slow plug-in is the detection process might have already begun before the headset gets fully inserted into the jack. If the detection is running with headset's plug out of position, the TS3A225E might retrieve false impedance information from the test and give incorrect detection result. To mitigate the slow plug-in issue, the following 3 steps can be implemented:

Jack Selection

Usage of proper audio jack in conjunction with TS3A225E is the most effective technique to alleviate the slow plug-in issue. One type of popular audio combo jack on the market has the pin composition similar to the one shown in Figure 2 below, where the DET_TRIGGER mechanism has to be designed around the RING1 pin. While headset is being inserted, the tip of the headset touches the RING1 pin first, pushing out pin 5 to pin 6 and connect them together, generating a low-to-high transition on the DET_TRIGGER pin and triggers the detection sequence of TS3A225E. However, the headset is not yet fully inserted at this moment (tip has not touched pin 1) and if the insertion is relatively slow the impedance detection of TS3A225E may complete before the tip of the headset touches pin1. This may result in false impedance values read by TS3A225E and affects its proper switching mechanism.

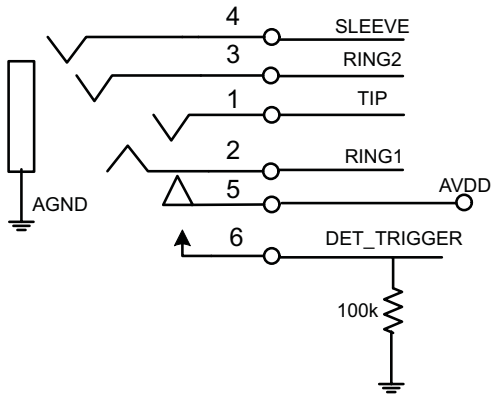

Figure 20. Poor Jack Usage

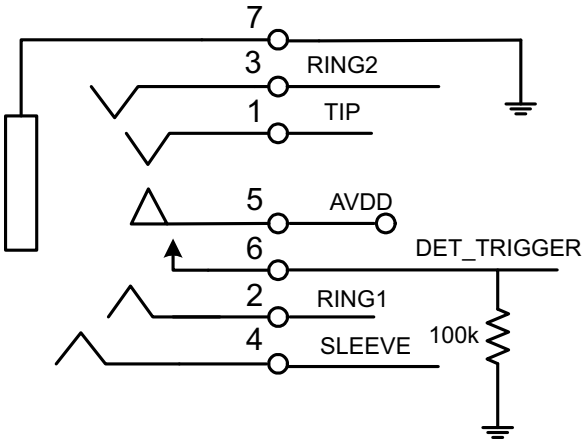

Figure 21. Recommended Audio Jack Selection

A more suitable audio jack to be used with TS3A225E is the one shown in Figure 21 above. This type of jack has the push-out mechanical structure located on the inner-most part of the jack. It thus allows the transition on DET_TRIGGER pin to occur only after the headset has been fully inserted with the tip touching pin 1 and 5, which reduces the risk of early-triggering on TS3A225E's detection sequence.

RC Delay on DET_TRIGGER

Another possible method to alleviate the slow-plug in issue is to introduce RC delay on the DET_TRIGGER pin. As specified in the Reference Schematic (Figure 1) in the previous section, the combination of R1 and C1 produces a low-pass effect on the DET_TRIGGER pin to slow down its transition from low to high. This delay provides more time for the headset to be fully inserted into the jack before the detection sequence of TS3A225E is triggered.

For effective delay implementation, it is recommended to use C1 >1uF. The board layout space can be reserved for R1 and the value of R1 can be adjusted based on the actual measurement data. A good default value to start with is 1kΩ.

Internal Delay

The TS3A225E has built-in 120ms delay to address the slow plug-in issue. After the low-to-high transition on the DET_TRIGGER pin, the TS3A225E does not start impedance detection sequence until 120ms later. This delay period gives some time buffer for the headset to be fully plugged-in.

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Special Note On Power Of Noise Issue

In computing, the Advanced Configuration and Power Interface (ACPI) specification provides an open standard for device configuration and power management by the operating system. The ACPI specification defines a number of different power states for an ACPI-compliant computer-system, ranging from G0 (system working) to G3 (system mechanical off with close to zero power consumption).

When TS3A225E is used in the ACPI-compliant computer-system, and if the user has a speaker (with amplifier) plugged into the audio jack when the system enters low-power state, audible noise interference may be heard during G1, G2, and G3 states. The G1, G2, and G3 states are defined as:

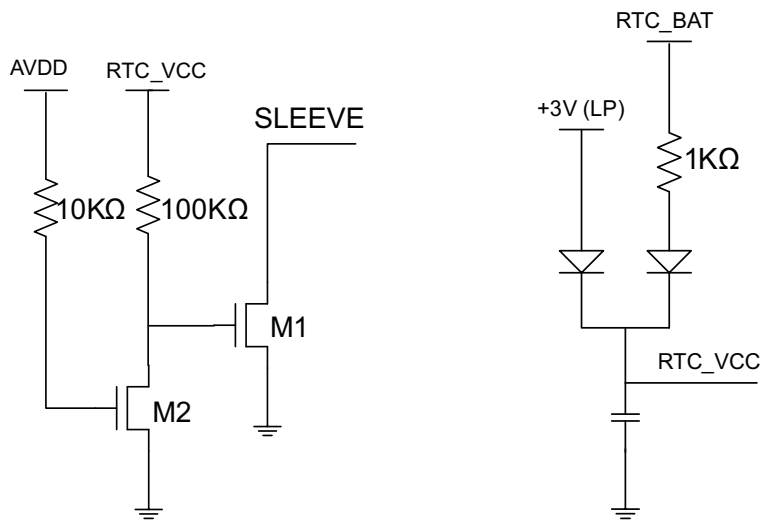
G1: Sleeping mode

G2 (or S5) Soft Off: G2 is almost the same as G3 Mechanical Off, but some components remain powered so the computer can "wake" from input from the keyboard, clock, modem, LAN, or USB device.

G3: Mechanical Off: The computer's power consumption approaches zero, to the point that the power cord can be removed and the system is safe for dis-assembly.

The root cause of this noise interference comes from the fact that the TS3A225E's VDD supply is disconnected during mode G1 to G3. The two2 Ground FET switches (FET1 and FET2) become open by default when no power is supplied to the device, and the ground return path lines become floating under this circumstance. With no established ground return path, the long speaker wire acts as an antenna and picks up random signals from the air and outputs the noise to the amplified speaker, creating undesirable buzzing noises.

To levitate this problem, the following circuitry is recommended:



With the use of this circuitry, the SLEEVE pin will be pulled down to GND by the RTC_VCC power source. The RTC_VCC power source is generated by the Real Time Clock source running off a small on-board battery (RTC_BAT) that is kept running even in G3 mode. With SLEEVE pin pulled down to GND, ground return path is established for the speaker and noises will be eliminated. Diodes are added from RTC_BAT to +3V (LP) to prevent leakage when system is turning on.

During normal system operation, AVDD becomes available to turn on M2 and in turn shut off M1. The SLEEVE to GND path will then be controlled solely by the internal FET switches of TS3A225E.

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REVISION HISTORY

Changes from Original (August 2012) to Revision A **Page**

- Added V_{IO} and $V_{IO(TIP)}$ parameters to the RECOMMENDED OPERATING CONDITIONS. 7
- Deleted DETECTION SEQUENCE AND RESET section. 15

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS3A225ERTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 85	ZTL
TS3A225ERTER.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZTL
TS3A225ERTER.B	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZTL
TS3A225ERTERG4	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZTL
TS3A225ERTERG4.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZTL
TS3A225ERTERG4.B	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZTL
TS3A225EYFFR	Active	Production	DSBGA (YFF) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	YP225E
TS3A225EYFFR.B	Active	Production	DSBGA (YFF) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	YP225E

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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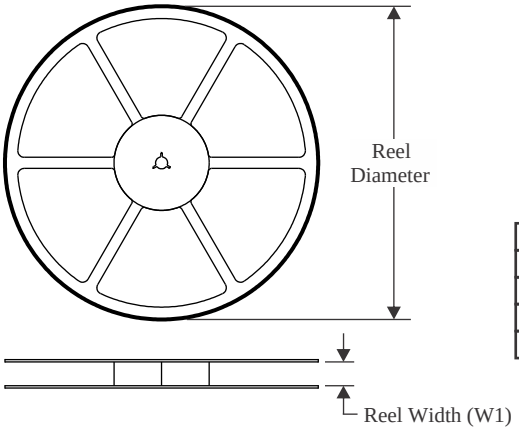
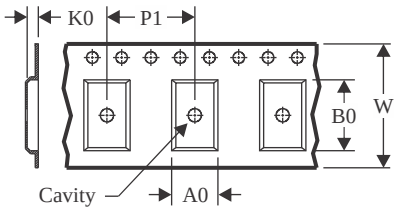
TAPE AND REEL INFORMATION

REEL DIMENSIONS

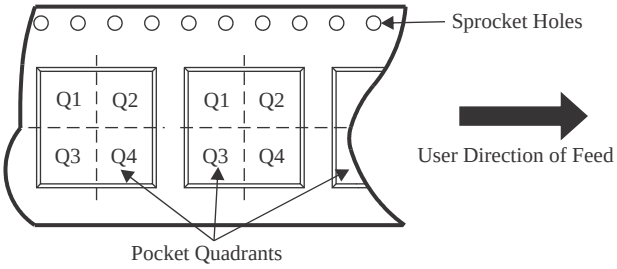


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

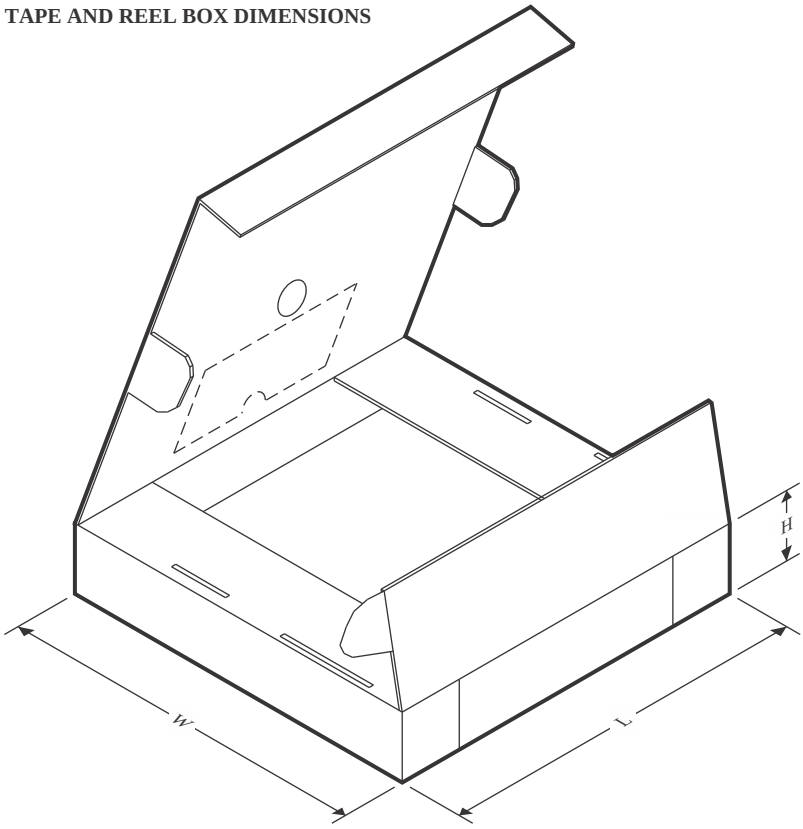
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A225ERTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TS3A225ERTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TS3A225ERTERG4	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TS3A225EYFFR	DSBGA	YFF	16	3000	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A225ERTER	WQFN	RTE	16	3000	360.0	360.0	36.0
TS3A225ERTER	WQFN	RTE	16	3000	346.0	346.0	33.0
TS3A225ERTERG4	WQFN	RTE	16	3000	346.0	346.0	33.0
TS3A225EYFFR	DSBGA	YFF	16	3000	182.0	182.0	20.0

GENERIC PACKAGE VIEW

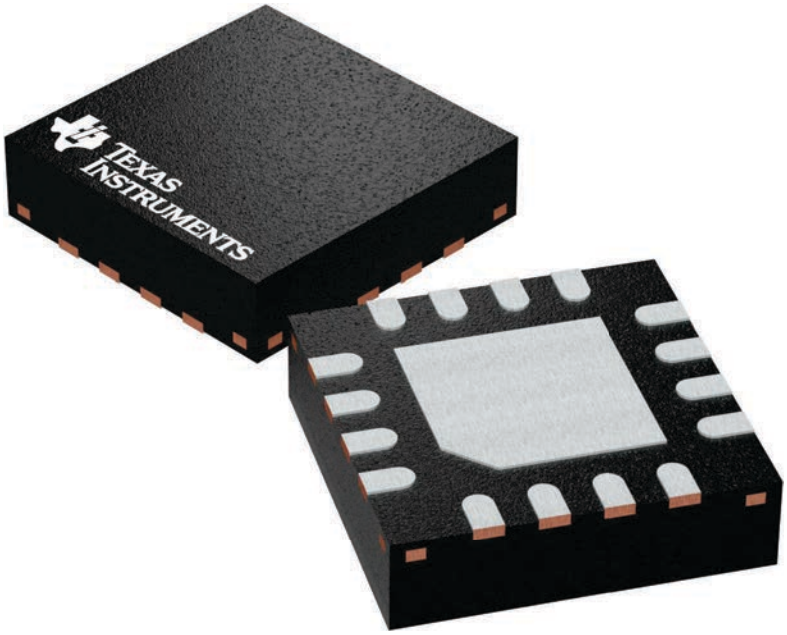
RTE 16

WQFN - 0.8 mm max height

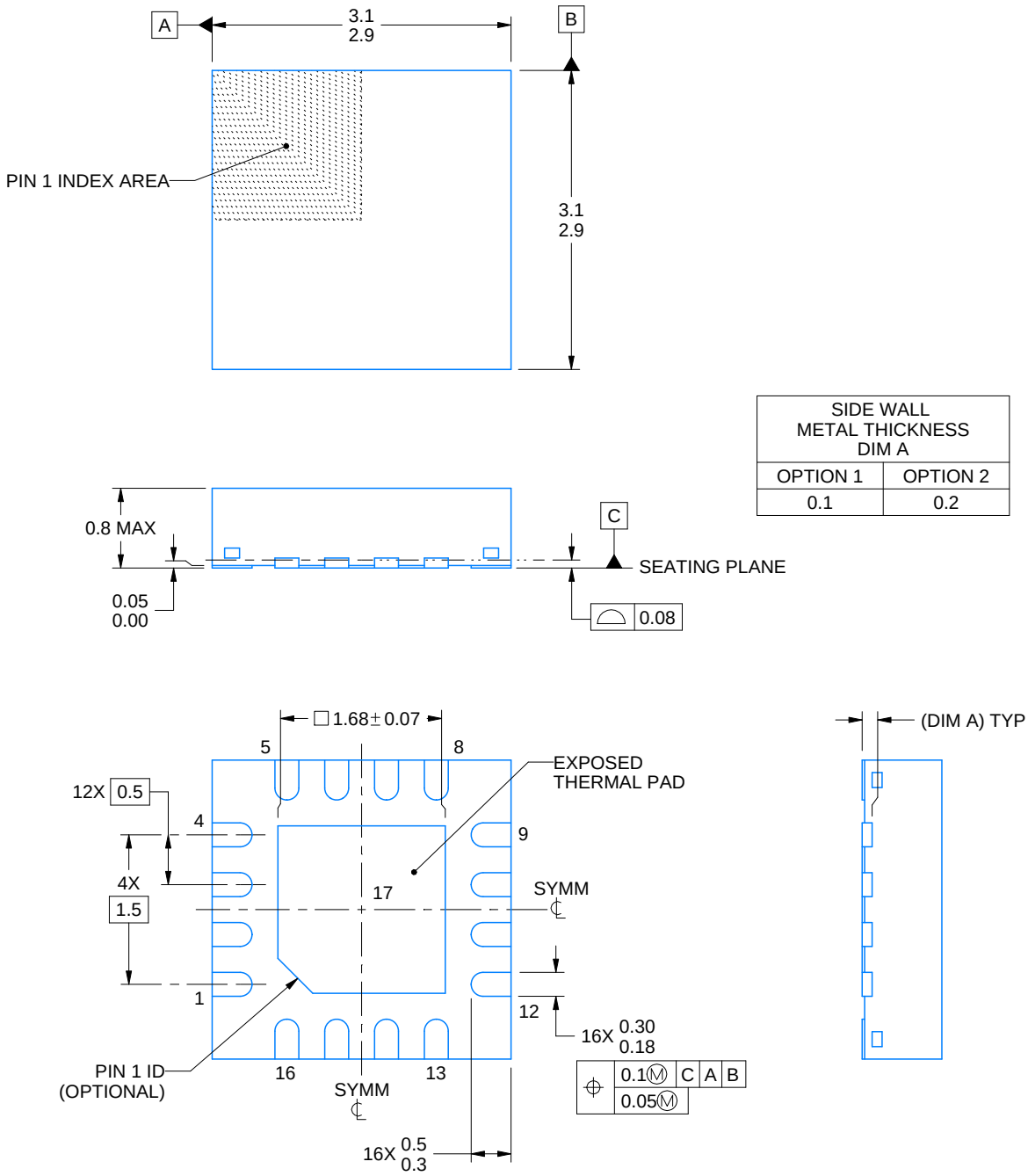
3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



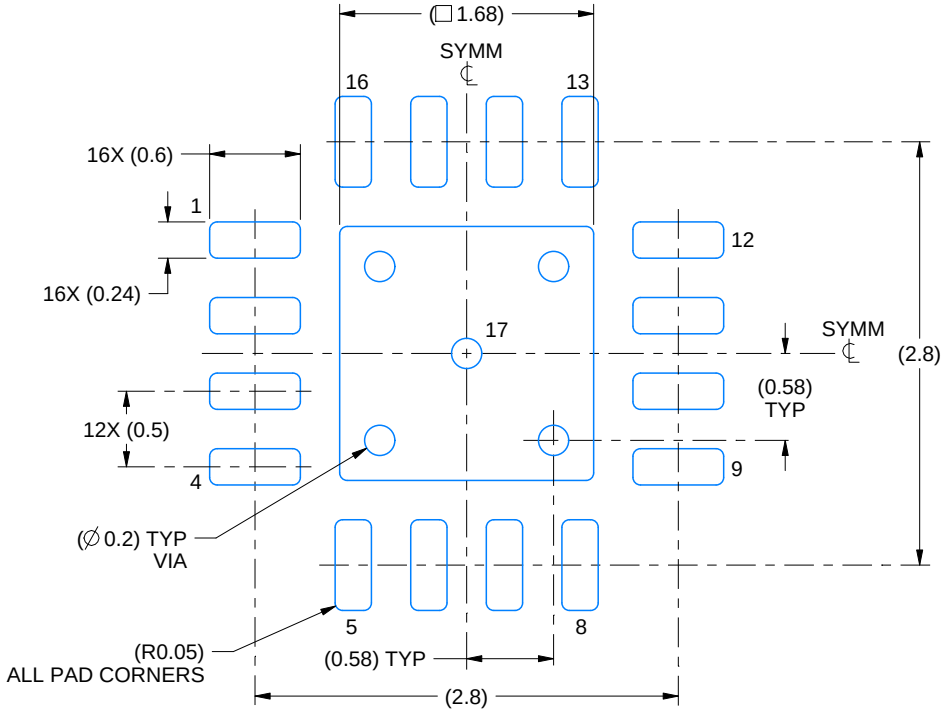
4225944/A



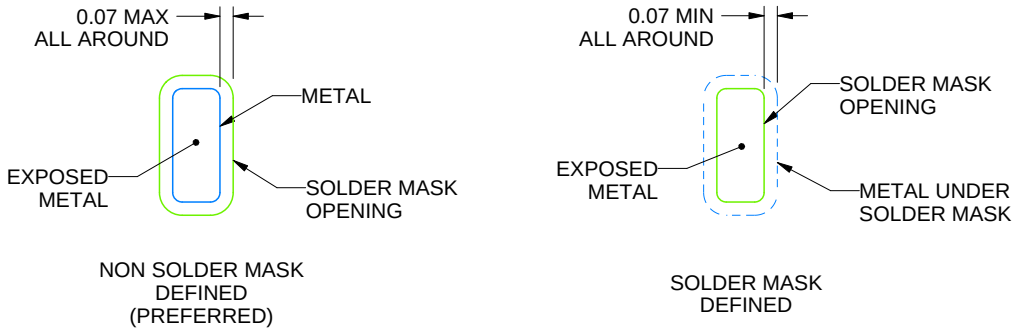
SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

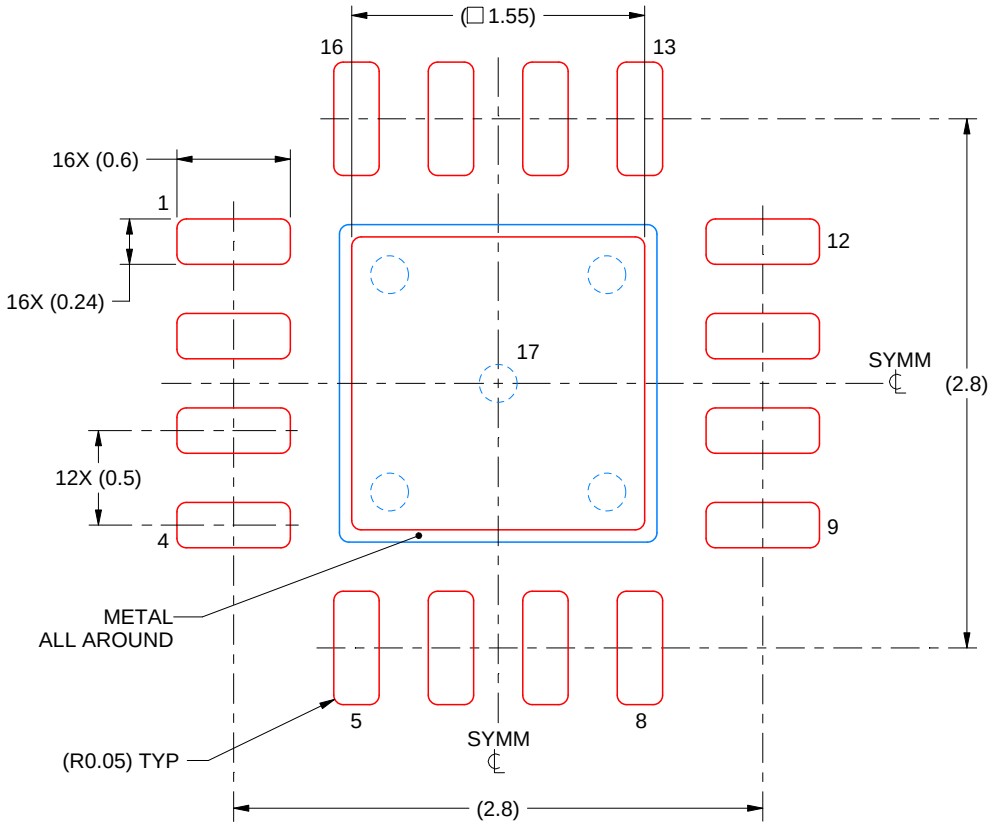


SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



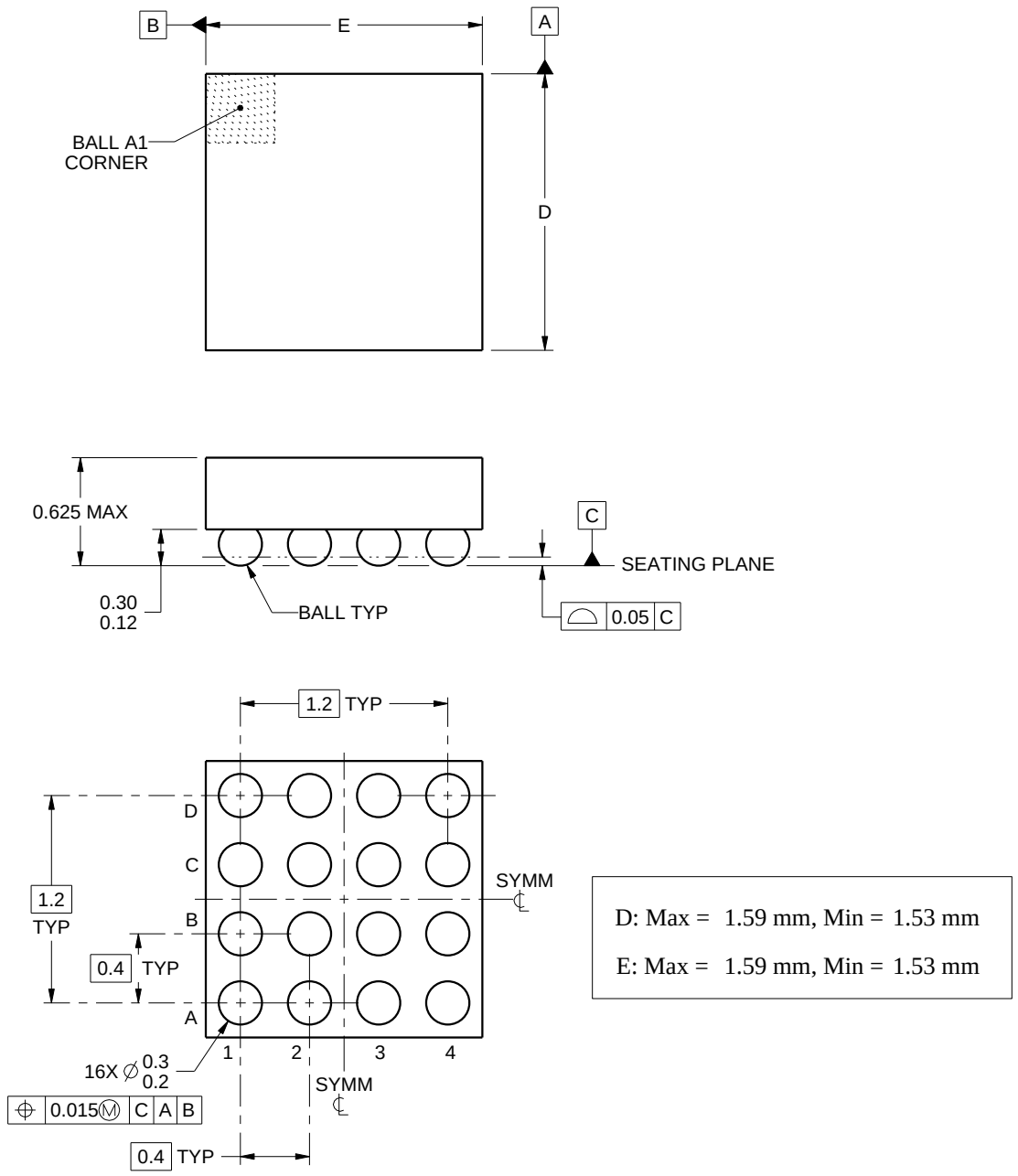
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

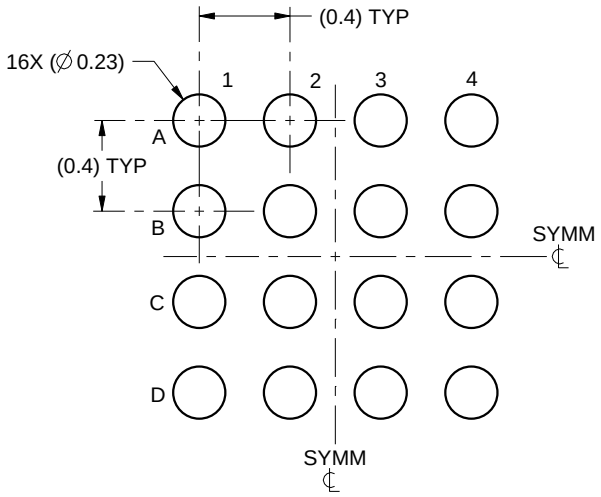
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

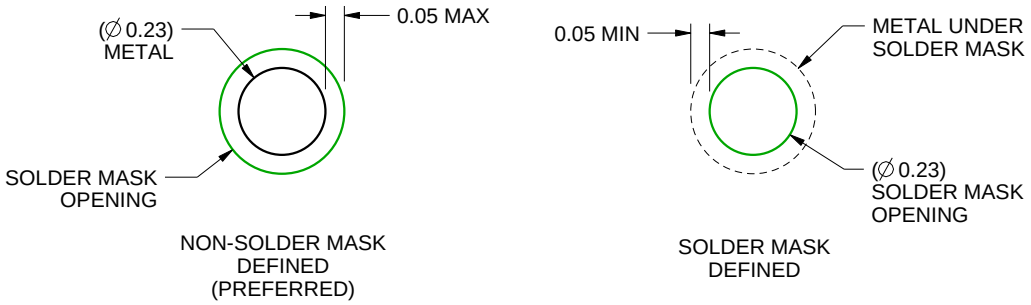


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

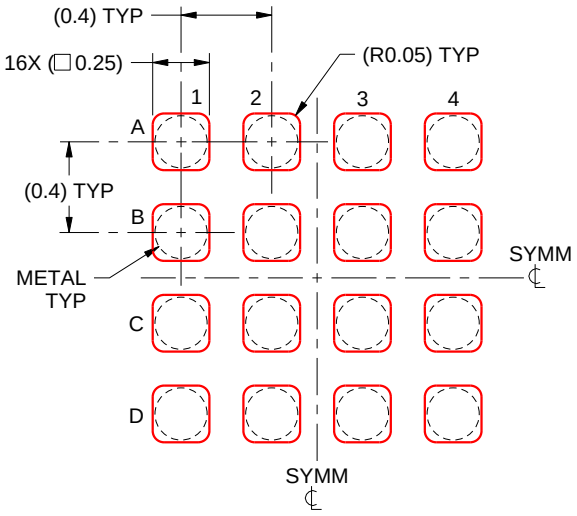


SOLDER MASK DETAILS
NOT TO SCALE

4219386/A 05/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4219386/A 05/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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最后更新日期：2025 年 10 月