TPSM560R6H 采用增强型 HotRod™ QFN 封装的 60V 输入、1V 至 16V 输出、600mA 电源模块

1 特性

- 提供功能安全
  - 可帮助进行功能安全系统设计的文档
- 5.0mm × 5.5mm × 4.0mm 增强型 HotRod™ QFN
  - 出色的热性能：在 85°C 且无散热的情况下高达 9.6W 的输出功率
  - 标准封装尺寸：单个大型散热焊盘和所有引脚均分布在封装外围
- 专为可靠耐用的应用而设计
  - 宽输入电压范围：4.2V 至 60V
  - 高达 66V 的输入电压瞬态保护
  - 工作结温范围：–40°C 至 +125°C
- 固定 1MHz 开关频率
- FPWM 运行模式
- 针对超低 EMI 要求进行了优化
  - 集成屏蔽式电感器和高频旁路电容器
  - 符合 EN55011 EMI 标准
- 26μA 非开关静态电流
- 单调启动至预偏置输出
- 无环路补偿或自举组件
- 具有迟滞功能的精密使能和输入 UVLO
- 具有迟滞功能的热关断保护
- 使用 TPSM560R6H 并借助 WEBENCH® Power Designer 创建定制设计

2 应用

- 现场发送器和传感器、PLC 模块
- 恒温器、视频监控、HVAC 系统
- 交流和伺服驱动器、旋转编码器
- 工业运输、资产跟踪
- 负输出应用

3 说明

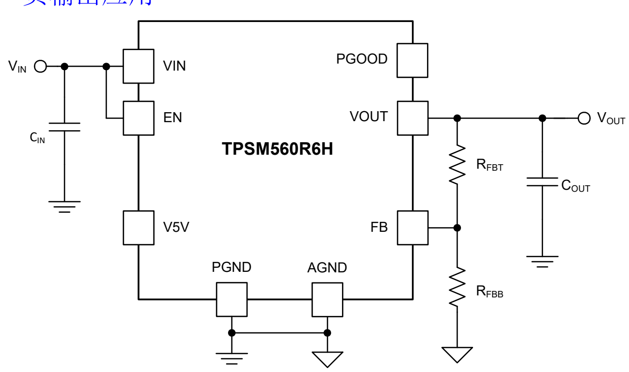
TPSM560R6H 是一款高度集成的 600mA 电源模块，在热增强型 QFN 封装内整合了一个带有功率 MOSFET 的 60V 输入直流/直流降压转换器、一个屏蔽式电感器和多个无源器件。此 5.0mm × 5.5mm × 4.0mm、15 引脚 QFN 封装采用增强型 HotRod QFN 技术来实现增强的热性能、小尺寸和低 EMI。封装引脚外露，具有单个大型散热焊盘，方便布局布线和组装。

TPSM560R6H 是一款紧凑、易用的电源模块，具有 1.0V 至 16V 的可调节宽输出电压范围。该总体解决方案仅需四个外部元件，并且省去了设计流程中的环路补偿和磁性器件选型过程。TPSM560R6H 具有全套功能，包括电源正常状态指示、可编程 UVLO、预偏置启动、过流和温度保护，因此是为各种应用供电的出色器件。空间受限型应用可从 5.0mm × 5.5mm 封装中受益。

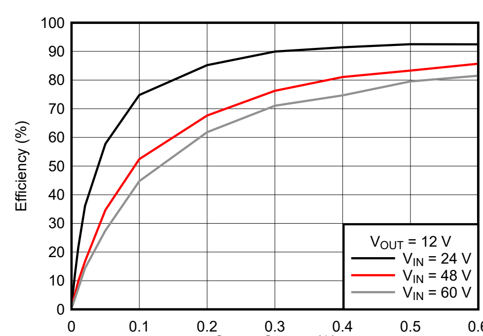
器件信息

器件型号	封装(1)	封装尺寸（标称值）
TPSM560R6H	QFN (15)	5.0mm × 5.5mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型电路原理图



典型效率 (V_{OUT} = 12V)

Table of Contents

4 Revision History

DATE	REVISION	NOTES
September 2021	*	Initial release

5 Pin Configuration and Functions

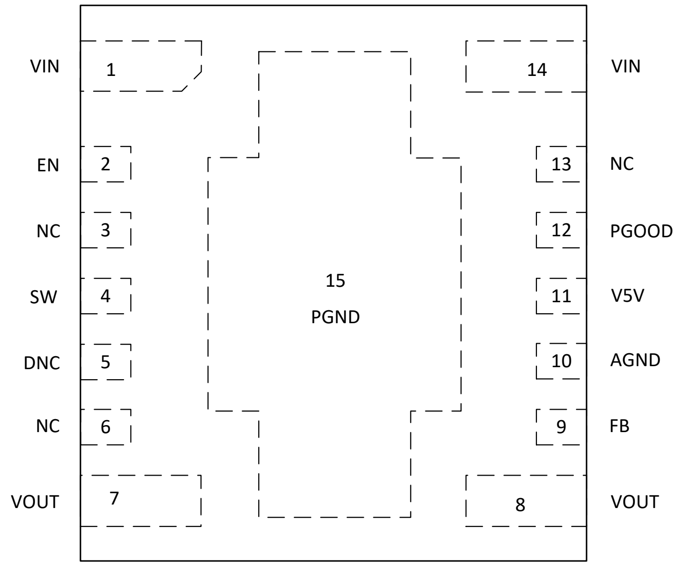


图 5-1. 15-Pin QFN RDA Package (Top View)

表 5-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NO.	NAME		
10	AGND	G	Analog ground. Zero voltage reference for internal references and logic. All electrical parameters are measured with respect to this pin. *This pin must be connected to PGND at a single point.* See 节 10.2 for a recommended layout.
5	DNC	—	Do not connect. Do not connect this pin to ground, to another pin, or to any other voltage. This pin is connected to the internal bootstrap capacitor. This pin must be soldered to an isolated pad.
2	EN	I	Enable pin. This pin turns the converter on when pulled high and turns off the converter when pulled low. This pin can be connected directly to VIN. *Do not float.* This pin can be used to set the input undervoltage lockout with two resistors. See 节 7.3.4.
9	FB	I	Feedback input. Connect the mid-point of the feedback resistor divider to this pin. Connect the upper resistor (R_{FBT}) of the feedback divider to V_{OUT} at the desired point of regulation. Connect the lower resistor (R_{FBB}) of the feedback divider to AGND.
3, 6, 13	NC	—	Not connected. These pins are not connected to any circuitry within the module. Leaving these pins unconnected to any other signal increases spacing near the high voltage pins (VIN, SW, EN, and DNC). However, if the high voltage spacing is not needed in the application, connecting these pins to the PGND plane can help enhance shielding and thermal performance.
15	PGND	G	Power ground. This is the return current path for the power stage of the device. Connect this pad to the input supply return, load return, and capacitors associated with the VIN and VOUT pins. See 节 10.2 for a recommended layout.
12	PGOOD	O	Power-good pin. An open-drain output that asserts low if the feedback voltage is not within the specified window thresholds. A 10-kΩ to 100-kΩ pullup resistor is required and can be tied to the V5V pin or other DC voltage less than 18 V. If not used, this pin can be left open or connected to PGND.
4	SW	O	Switch node. Do not place any external component on this pin or connect this pin to any signal.
1, 14	VIN	I	Input supply voltage. Connect the input supply to these pins. Connect input capacitors between these pins and PGND in close proximity to the device.
7, 8	VOUT	O	Output voltage. These pins are connected to the internal output inductor. Connect these pins to the output load and connect external output capacitors between these pins and PGND.
11	V5V	O	Internal 5-V LDO output. Supplies internal control circuits. Do not connect to external loads. This pin can be used as logic supply for the PGOOD pin.

(1) G = Ground, I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

Over the operating ambient temperature range(1)

PARAMETER		MIN	MAX	UNIT
Input voltage	VIN to PGND	–0.3	66	V
	EN to AGND(2)	–0.3	V_{IN} + 0.3	
	PGOOD to AGND(2)	–0.3	22	
	FB to AGND	–0.3	5.5	
	AGND to PGND	–0.3	0.3	
Output voltage	VOUT to PGND(2)	–0.3	30	
	VCC to AGND	0	5.5	
Operating IC junction temperature, T_J (3)		–40	125	°C
Storage temperature, T_{stg}		–55	150	°C
Peak reflow case temperature			245	
Maximum number or reflows allowed			3	
Mechanical vibration	Mil-STD-883H, Method 2007.3, 1 msec, 1/2 sine, mounted		20	G
Mechanical shock	Mil-STD-883H, Method 2002.5, 20 to 2000Hz		500	G

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V.
(3) The ambient temperature is the air temperature of the surrounding environment. The junction temperature is the temperature of the internal power IC when the device is powered. Operating below the maximum ambient temperature, as shown in the safe operating area (SOA) curves in the t*Typical Applications* sections, ensures that the maximum junction temperature of any component inside the module is never exceeded.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)(1)	±1500	V
		Charged-device model (CDM)(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating ambient temperature range (unless otherwise noted) [(1)]

	MIN	MAX	UNIT
Input voltage, V_{IN}	4.2	60	V
Output voltage, V_{OUT}	1	16 [(3)]	V
Output current, I_{OUT}	0	0.6	A
EN voltage, V_{EN} [(2)]	0	V_{IN}	V
PGOOD pullup voltage, V_{PGOOD} [(2)]	0	18	V
Operating ambient temperature, T_A	–40	105	°C

(1) Recommended operating conditions indicate conditions where the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see the *Electrical Characteristics*.
(2) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V.
(3) The recommended maximum output voltage varies depending input voltage.

6.4 Thermal Information

THERMAL METRIC[(1)]			TPSM560R6H RDA (QFN) 15 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance [(2)]	Nat Conv	20.4	°C/W
		100 LFM	18.9	°C/W
		200 LFM	17.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter [(3)]		3.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter [(4)]		15.3	°C/W
T_{SHDN}	Thermal shutdown temperature		170	°C
	Recovery temperature		158	°C

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction-to-ambient thermal resistance, $R_{\theta JA}$, applies to devices soldered directly to a 6.35-cm × 8.25-cm, four-layer PCB with 2-oz. copper. Additional airflow and PCB copper area reduces $R_{\theta JA}$. See 节 10.2.1 for more information.
(3) The junction-to-top board characterization parameter, ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7). $T_J = \psi_{JT} \times Pdis + T_T$; where Pdis is the power dissipated in the device and T_T is the temperature of the top of the device.
(4) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} \times Pdis + T_B$; where Pdis is the power dissipated in the device and T_B is the temperature of the board 1 mm from the device.

6.5 Electrical Characteristics

Limits apply over T_A = –40°C to +105°C, V_{IN} = 24 V, V_{OUT} = 3.3 V, I_{OUT} = 600 mA, (unless otherwise noted); minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (V_{IN})						
V_{IN}	Input voltage range	Over I_{OUT} range	4.2 (1)		60	V
	V_{IN} turn-on	V_{IN} increasing, I_{OUT} = 0 A, V_{EN} = V_{IN}		3.8		V
	V_{IN} turn-off	V_{IN} decreasing, I_{OUT} = 0 A, V_{EN} = V_{IN}		3.3		V
I_{SHDN}	Shutdown supply current	V_{EN} = 0 V, I_{OUT} = 0 A		5		μA
INTERNAL LDO (V5V)						
V5V	Internal LDO output voltage appearing at the V5V pin	6 V ⩽ V_{IN} ⩽ 60 V	4.75	5	5.25	V
FEEDBACK						
V_{FB}	Load regulation	T_A = +25°C, 0 A ⩽ I_{OUT} ⩽ 0.6 A		0.057		%
V_{FB}	Line regulation	T_A = +25°C, I_{OUT} = 0 A, 6 V ⩽ V_{IN} ⩽ 60 V		0.024		%
I_{FB}	Current into FB pin	FB = 1 V		0.2		nA
CURRENT						
I_{OUT}	Output current	T_A = 25ºC	0		0.6	A
I_{OUT}	Overcurrent threshold	V_{OUT} = 3.3 V, T_A = 25ºC		0.89		A
V_{HC}	FB pin voltage required to trip short-circuit Hiccup mode			0.4		V
t_{HC}	Time between current-limit hiccup burst			94		ms
ENABLE (EN PIN)						
$V_{EN\text{-}VCC\text{-}H}$	EN input level required to turn on the internal LDO	Rising threshold			1.14	V
$V_{EN\text{-}VCC\text{-}L}$	EN input level required to turn off the internal LDO	Falling threshold	0.3			V
$V_{EN\text{-}H}$	EN input level required to start switching	Rising threshold	1.157	1.231	1.30	V
$V_{EN\text{-}HYS}$	Hysteresis below $V_{EN\text{-}H}$	Hysteresis below $V_{EN\text{-}H}$; falling		110		mV
$I_{LKG\text{-}EN}$	Enable input leakage current	V_{EN} = 3.3 V		0.2		nA
POWER GOOD (PGOOD PIN)						
$V_{PG\text{-}LOW\text{-}UP}$	V_{OUT} rising (fault)	% of FB voltage		107%		
$V_{PG\text{-}HIGH\text{-}DN}$	V_{OUT} falling (good)	% of FB voltage		105%		
$V_{PG\text{-}HIGH\text{-}UP}$	V_{OUT} rising (good)	% of FB voltage		95%		
$V_{PG\text{-}LOW\text{-}DN}$	V_{OUT} falling (fault)	% of FB voltage		93%		
R_{PG}	Power-good flag, R_{DSON}	V_{EN} = 0 V		35		Ω
$V_{IN\text{-}PG}$	Minimum input voltage for proper PGOOD function	I_{PG} = 50 μA, EN = 0 V			2	V
PERFORMANCE						
η	Efficiency	V_{OUT} = 3.3 V, I_{OUT} = 0.75 A, T_A = 25ºC		81%		
η	Efficiency	V_{OUT} = 5.0 V, I_{OUT} = 0.75 A, T_A = 25ºC		86%		
SOFT START						
t_{SS}	Internal soft-start time			4.5		ms
SWITCHING FREQUENCY						
f_{SW}	Switching frequency	I_{OUT} = 0.75 A, T_A = 25ºC	0.85	1(2)	1.15	MHz

(1) The recommended minimum V_{IN} is 4.2 V or (V_{OUT} + 600 mV), whichever is greater.
(2) The typical switching frequency of this device changes based on operating conditions. See the Switching Frequency section for more information.

6.6 Typical Characteristics (V_{IN} = 12 V)

T_A = 25°C, unless otherwise noted.

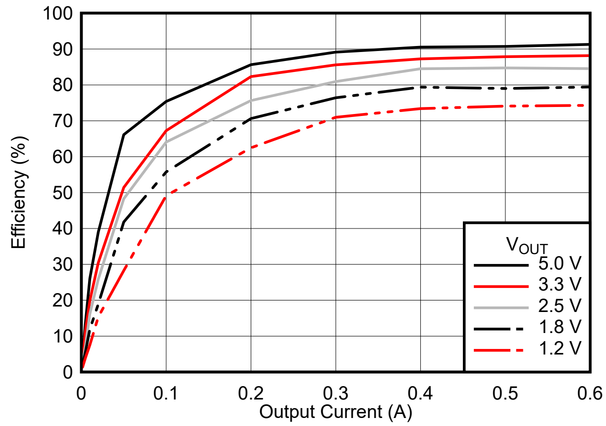


图 6-1. Efficiency

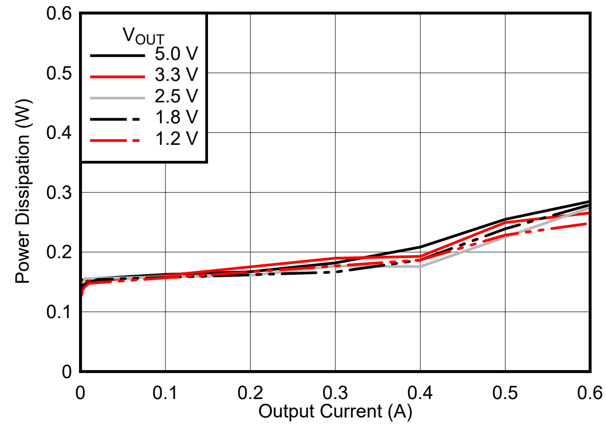
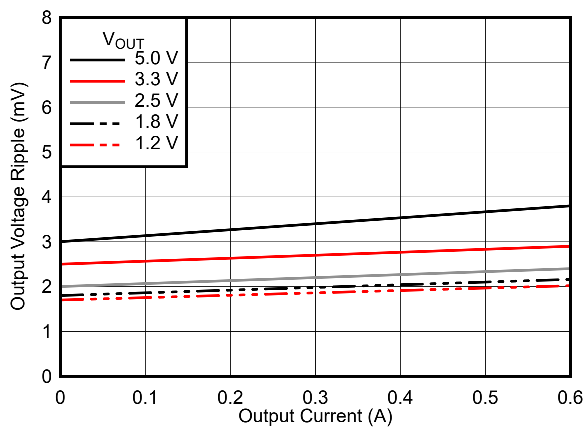
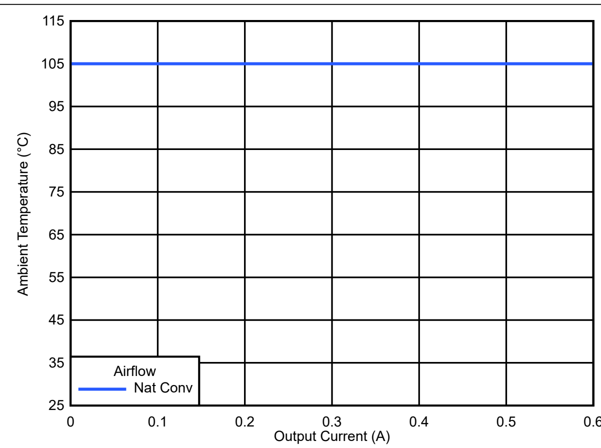


图 6-2. Power Dissipation



C_{OUT} = 4 × 47 µF, 25-V, ceramic

图 6-3. Output Voltage Ripple



Device soldered to a 63.5-mm × 82.5-mm, 4-layer PCB

图 6-4. Safe Operating Area (All V_{OUT})

6.7 Typical Characteristics (V_{IN} = 24 V)

T_A = 25°C, unless otherwise noted.

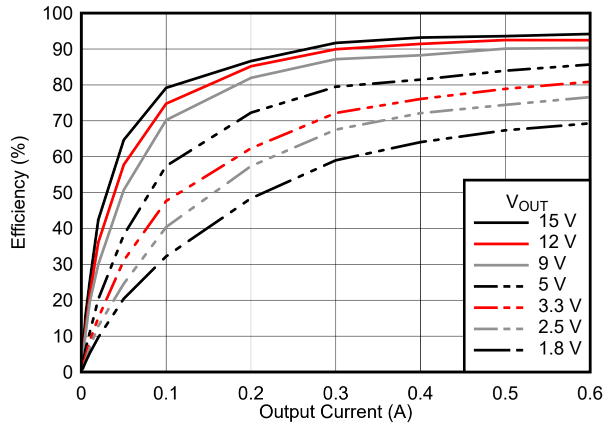


图 6-5. Efficiency

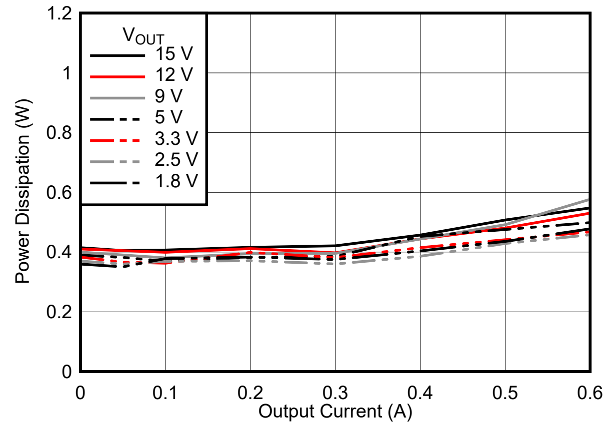
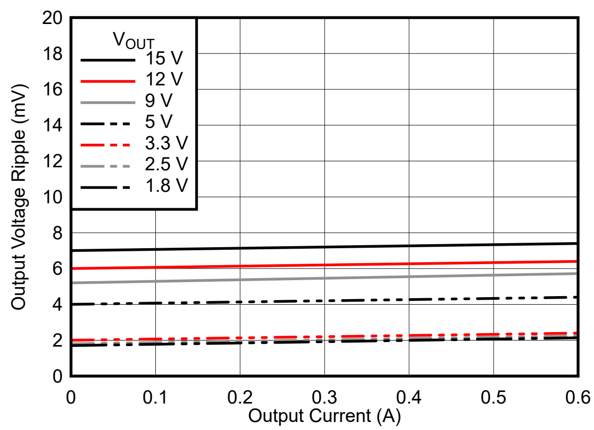
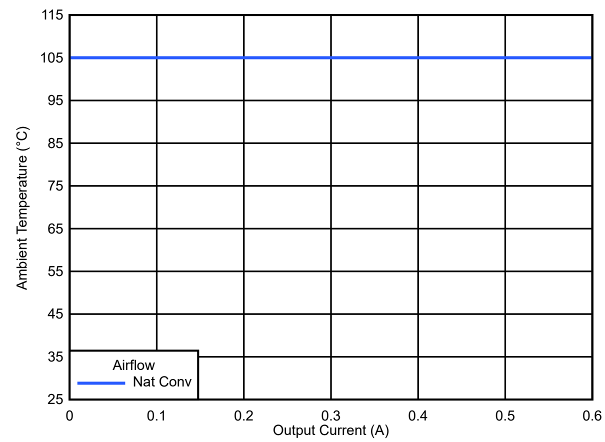


图 6-6. Power Dissipation



C_{OUT} = 4 × 47-μF, 25-V, ceramic

图 6-7. Output Voltage Ripple



Device soldered to a 63.5-mm × 82.5-mm, 4-layer PCB

图 6-8. Safe Operating Area (All V_{OUT})

6.8 Typical Characteristics (V_{IN} = 48 V)

T_A = 25°C, unless otherwise noted.

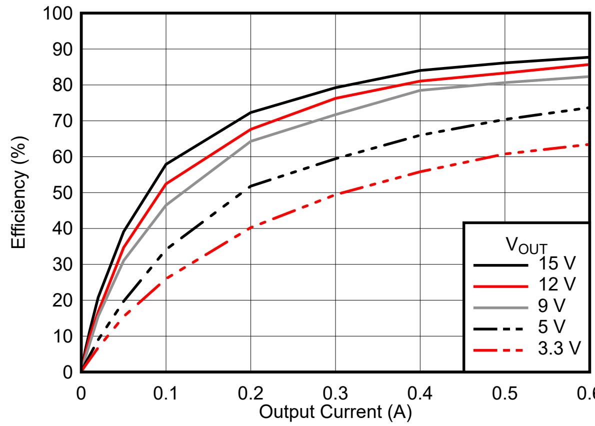


图 6-9. Efficiency

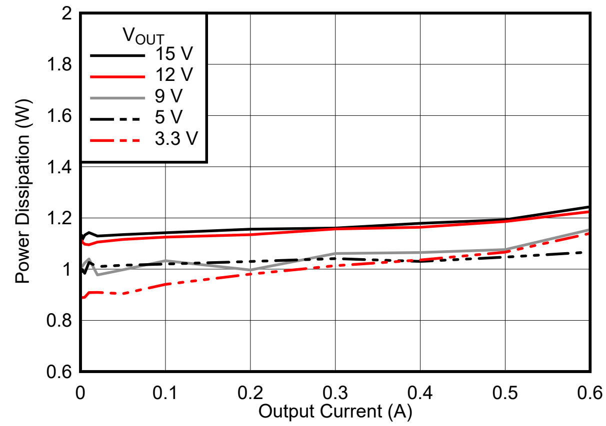
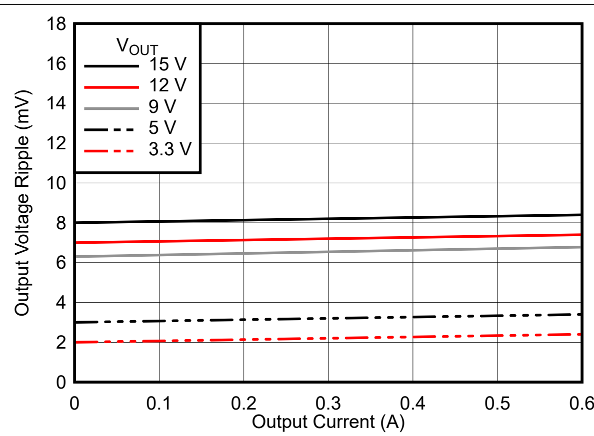
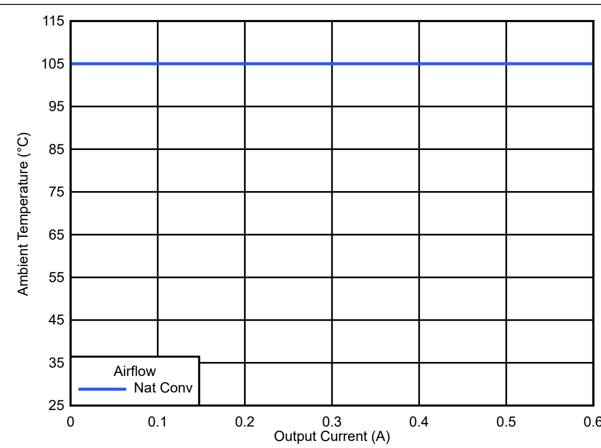


图 6-10. Power Dissipation



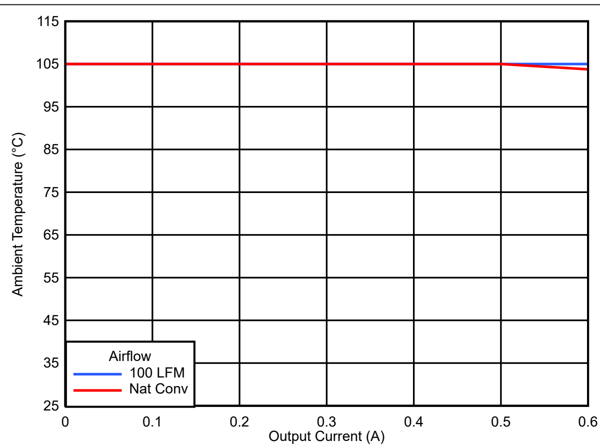
C_{OUT} = 2 × 47-µF, 25-V, ceramic

图 6-11. Output Voltage Ripple



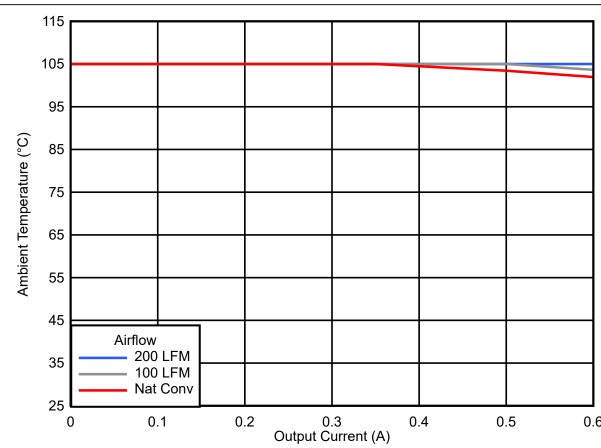
Device soldered to a 63.5-mm × 82.5-mm, 4-layer PCB

图 6-12. Safe Operating Area (V_{OUT} < 10 V)



Device soldered to a 63.5-mm × 82.5-mm, 4-layer PCB

图 6-13. Safe Operating Area (V_{OUT} = 12 V)



Device soldered to a 63.5-mm × 82.5-mm, 4-layer PCB

图 6-14. Safe Operating Area (V_{OUT} = 15 V)

6.9 Typical Characteristics (V_{IN} = 60 V)

T_A = 25°C, unless otherwise noted.

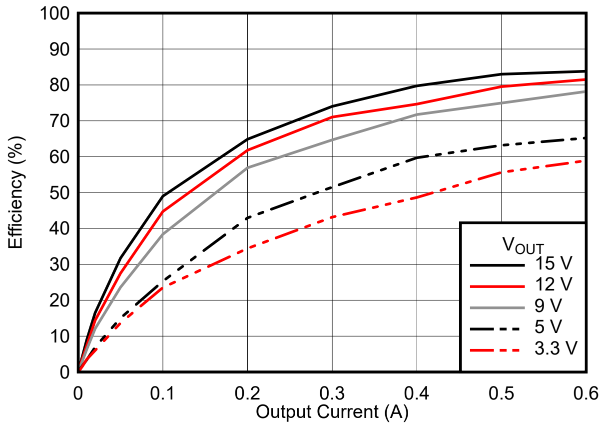


图 6-15. Efficiency

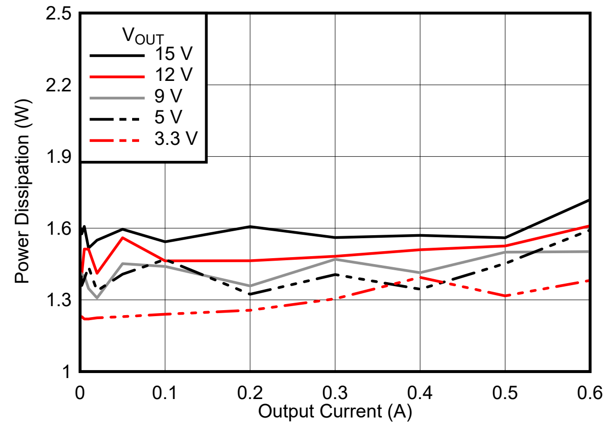
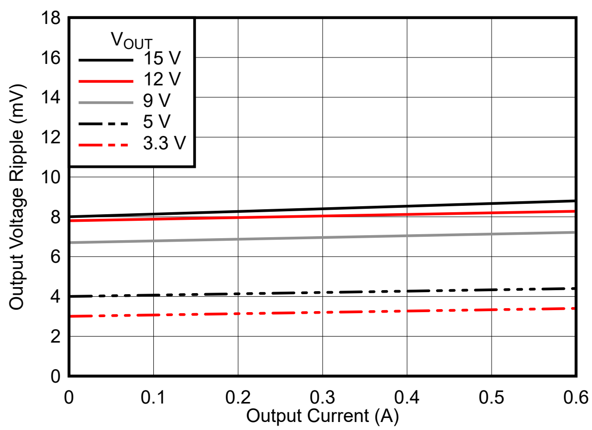
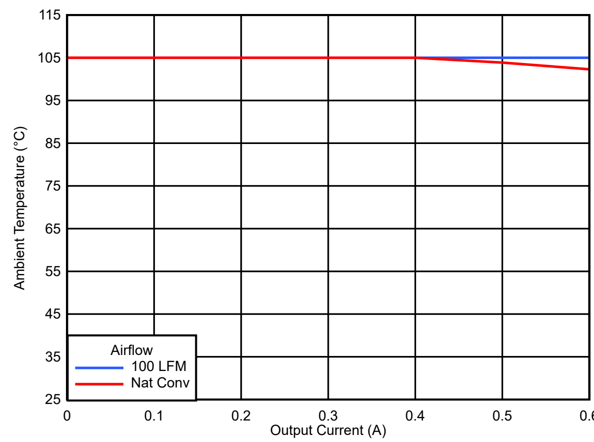


图 6-16. Power Dissipation



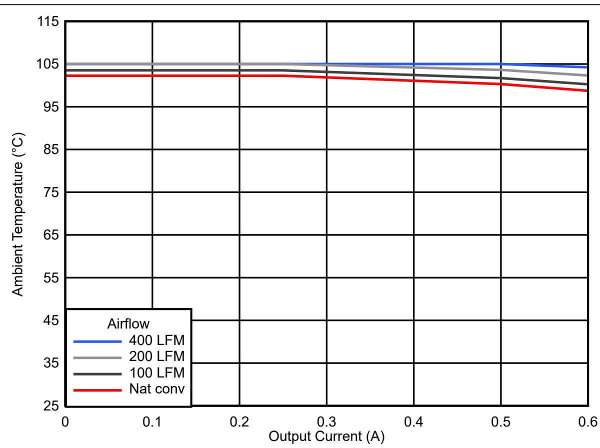
C_{OUT} = 2 × 47-µF, 25-V, ceramic

图 6-17. Output Voltage Ripple



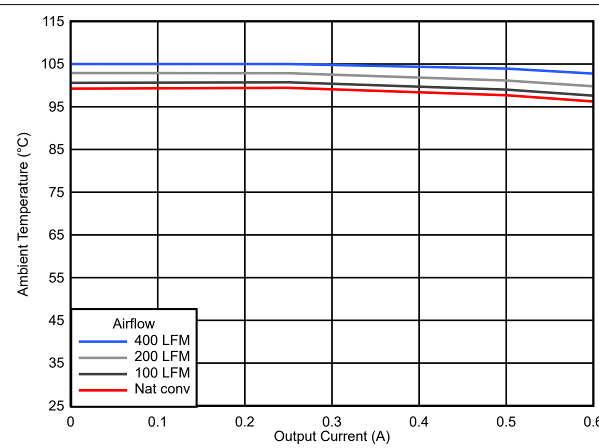
Device soldered to a 63.5-mm × 82.5-mm, 4-layer PCB

图 6-18. Safe Operating Area (V_{OUT} = 5.0 V)



Device soldered to a 63.5-mm × 82.5-mm, 4-layer PCB

图 6-19. Safe Operating Area (V_{OUT} = 12 V)



Device soldered to a 63.5-mm × 82.5-mm, 4-layer PCB

图 6-20. Safe Operating Area (V_{OUT} = 15 V)

7 Detailed Description

7.1 Overview

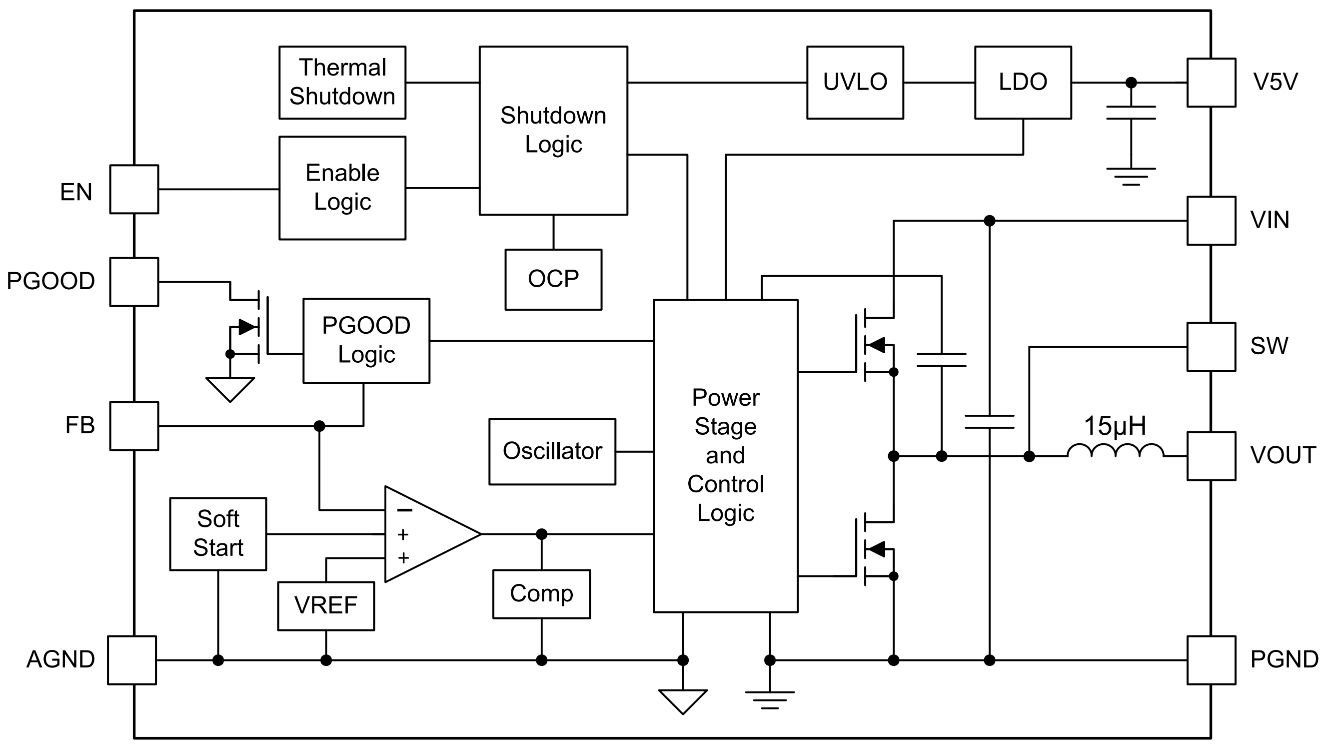
The TPSM560R6H converter is an easy-to-use, synchronous buck, DC-DC power module that operates from a 4.2-V to 60-V supply voltage. The device is intended for step-down conversions from 5-V, 12-V, 24-V, and 48-V unregulated, semi-regulated, or fully-regulated supply rails. With an integrated power controller, inductor, and MOSFETs, the TPSM560R6H delivers up to 600-mA DC load current, with high efficiency and ultra-low input quiescent current, in a very small solution size. Although designed for simple implementation, this device offers flexibility to optimize its usage according to the target application. Control-loop compensation is not required, reducing design time and external component count.

The TPSM560R6H incorporates several features for comprehensive system requirements, including the following:

- Open-drain power-good circuit for power-rail sequencing and fault reporting
- Monotonic start-up into prebiased loads
- Precision enable with customizable hysteresis for programmable line undervoltage lockout (UVLO)
- Overcurrent and thermal shutdown with automatic recovery

These features enable a flexible and easy-to-use platform for a wide range of applications. The pin arrangement is designed for simple PCB layout, requiring as few as four external components.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Adjustable Output Voltage (FB)

The TPSM560R6H has an adjustable output voltage range from 1.0 V to 16 V. Setting the output voltage requires two resistors, R_{FBT} and R_{FBB} (see 图 7-1). Connect R_{FBT} between VOUT at the regulation point and the FB pin. Connect R_{FBB} between the FB pin and AGND (pin 10). The recommended value of R_{FBT} is 10 kΩ. The value for R_{FBB} can be calculated using 方程式 1.

$$R_{FBB} = \frac{1.0}{V_{OUT} - 1.0} \times R_{FBT} \tag{1}$$

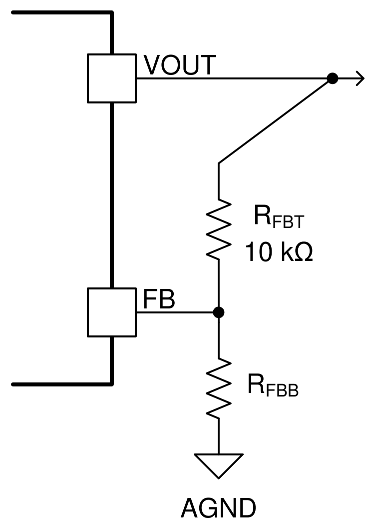


图 7-1. FB Resistor Divider

表 7-1. Standard R_{FBB} Values

VOUT (V)	R_{FBB} (kΩ) (1)		VOUT (V)	R_{FBB} (kΩ) (1)
1.0	open		3.3	4.32
1.2	49.9		5.0	2.49
1.5	20.0		7.5	1.54
1.8	12.4		10	1.10
2.0	10.0		12	0.909
2.5	6.65		15	0.715
3.0	4.99		16	0.665

(1) R_{FBT} = 10 kΩ

Select an R_{FBT} value of 10 kΩ for most applications. A larger R_{FBT} value consumes less DC current, which is mandatory if light-load efficiency is critical. However, R_{FBT} larger than 1 MΩ is not recommended because the feedback path becomes more susceptible to noise. High feedback resistance generally requires more careful layout of the feedback path. It is important to keep the feedback trace as short as possible while keeping the feedback trace away from the noisy area of the PCB. For more layout recommendations, see 节 10.

7.3.2 Minimum Input Capacitance

The TPSM560R6H requires a minimum input capacitance of 9.4 µF (2 × 4.7 µF) of ceramic type. High-quality, ceramic-type X5R or X7R capacitors with sufficient voltage rating are required. Place the input capacitors, as close as possible to both VIN pins of the device between VIN and PGND as shown in 节 10.1. Applications with transient load requirements can benefit from adding additional bulk capacitance to the input as well.

7.3.3 Minimum Output Capacitance

The TPSM560R6H requires a minimum amount of ceramic output capacitance for stability, depending on the output voltage setting. 图 7-2 shows the amount of required output capacitance, which is also the amount of *effective* capacitance. The effects of DC bias and temperature variation must be considered when using ceramic capacitance. For ceramic capacitors, the package size, voltage rating, and dielectric material contribute to the differences between the standard rated value and the actual effective value of the capacitance. Additional output capacitance above the minimum can be added to reduce output voltage ripple and to improve transient response. When adding additional capacitance above the minimum, the capacitance can be ceramic type, low-ESR polymer type, or a combination of the two.

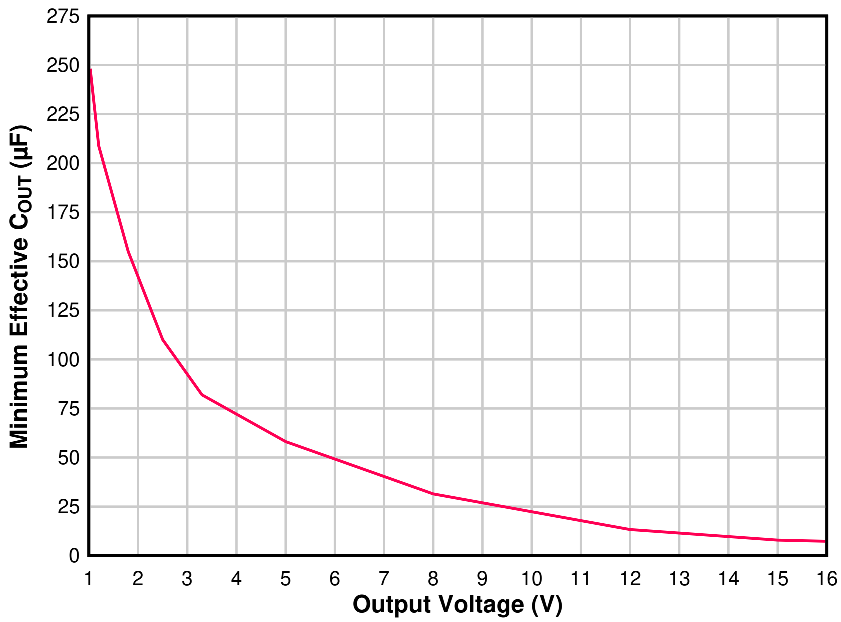


图 7-2. Minimum Required Output Capacitance

7.3.4 Precision Enable (EN), Undervoltage Lockout (UVLO), and Hysteresis (HYS)

The EN pin provides precision ON and OFF control for the TPSM560R6H. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. The simplest way to enable the device is to connect EN directly to VIN. This lets the device start up when V_{IN} is within its valid operating range. An external logic signal can also be used to drive the EN input to toggle the output on and off and for system sequencing or protection. *This input must not be allowed to float.*

The TPSM560R6H implements internal undervoltage lockout (UVLO) circuitry on the VIN pin. The device is disabled when the VIN pin voltage is below the internal VIN UVLO threshold. The internal VIN UVLO rising threshold is 3.8 V (typical) with a typical hysteresis of 500 mV.

If an application requires a higher UVLO threshold, the EN input supports adjustable UVLO by connecting a resistor divider from the VIN to EN pin. Applying a voltage greater than or equal to 1.14 V causes the device to enter Standby mode, powering the internal LDO, but not producing an output voltage. Increasing the EN voltage to 1.231 V (typical) fully enables the device, letting it enter Start-up mode and start the soft-start period. When the EN input is brought below 1.121 V (110-mV hysteresis), the regulator stops running and enters Standby mode. Further decrease in the EN voltage to below 0.3 V completely shuts down the device.

The TPSM560R6H uses a reference-based soft start that prevents output voltage overshoots and large inrush currents as the regulator is starting up. The rise time of the output voltage is approximately 4 ms.

7.3.5 Power Good (PGOOD)

The TPSM560R6H provides a PGOOD signal to indicate when the output voltage is within regulation. Use the PGOOD signal for output monitoring, fault protection, or start-up sequencing of downstream converters. PGOOD is an open-drain output that requires a pullup resistor to a DC supply not greater than 18 V. V5V or VOUT can be used as the pullup voltage source. The typical range of pullup resistance is 10 kΩ to 100 kΩ. If necessary, use a resistor divider to decrease the voltage from a higher voltage pullup rail. If this function is not needed, the PGOOD pin must be grounded.

When the output voltage exceeds 95% (rising) or decreases below 105% (falling) of the setpoint, the internal PGOOD switch turns off and PGOOD can be pulled high by the external pullup. If the FB voltage falls below 93% or rises above 107% of the setpoint, the internal PGOOD switch turns on, and PGOOD is pulled low to indicate that the output voltage is out of regulation.

Note that during initial power up, a delay of approximately 4 ms (typical) is inserted from the time that EN is asserted to the time that the power-good flag goes high. This delay only occurs during start-up and is not encountered during normal operation of the power-good function.

7.3.6 Overcurrent Protection (OCP)

The TPSM560R6H is protected from overcurrent conditions using cycle-by-cycle current limiting for overload conditions and Hiccup mode for short circuits. The current is compared every switching cycle to the current limit threshold. During an overcurrent condition, the output voltage decreases.

7.3.7 Thermal Shutdown

Thermal shutdown is an integrated self-protection used to limit junction temperature and prevent damage related to overheating. Thermal shutdown turns off the device when the junction temperature exceeds 170°C (typical) to prevent further power dissipation and temperature rise. Junction temperature decreases after shutdown and the TPSM560R6H restarts when the junction temperature falls to 158°C (typical).

7.4 Device Functional Modes

7.4.1 Active Mode

The TPSM560R6H is in Active mode when VIN is above the turn-on threshold and the EN pin voltage is above the EN high threshold. Connect the EN pin to VIN to allow the device to start up when a valid input voltage is applied. This allows self start-up of the TPSM560R6H when the input voltage is in the operation range of 4.2 V to 60 V. Connecting a resistor divider between VIN, EN, and AGND adjusts the UVLO to delay the turn on until VIN is closer to its regulated voltage.

7.4.2 Standby Mode

Start-up and shutdown are controlled by the EN input. This input features precision thresholds, allowing the use of an external voltage divider to provide an adjustable input UVLO. Applying a voltage greater than or equal to 1.14 V causes the device to enter Standby mode, powering the internal LDO, but not producing an output voltage. Increasing the EN voltage to 1.231 V (typical) fully enables the device, letting it enter Start-up mode and start the soft-start period. When the EN input is brought below 1.121 V (110-mV hysteresis), the regulator stops running and enters Standby mode. Further decrease in the EN voltage to below 0.3 V completely shuts down the device.

7.4.3 Shutdown Mode

The EN pin provides ON and OFF control for the TPSM560R6H. When V_{EN} is below the EN low threshold, the device is in Shutdown mode. Both the internal LDO and the switching regulator are off. The quiescent current in Shutdown mode drops to 5 µA at V_{IN} = 24 V.

8 Applications and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPSM560R6H only requires a few external components to convert from a wide range of supply voltages to a fixed output voltage. To expedite and streamline the process of designing of a TPSM560R6H, WEBENCH® online software is available to generate complete designs, leveraging iterative design procedures and access to comprehensive component databases. The following section describes the design procedure to configure the TPSM560R6H power module.

As mentioned previously, the TPSM560R6H also integrates several optional features to meet system design requirements, including precision enable, UVLO, and PGOOD indicator. The following application circuit shows TPSM560R6H configuration options suitable for several application use cases. Refer to the *TPSM560R6HEVM User's Guide* for more detail.

8.2 Typical Application

图 8-1 shows the schematic diagram of a 24-V input, 5-V output, 600-mA converter.

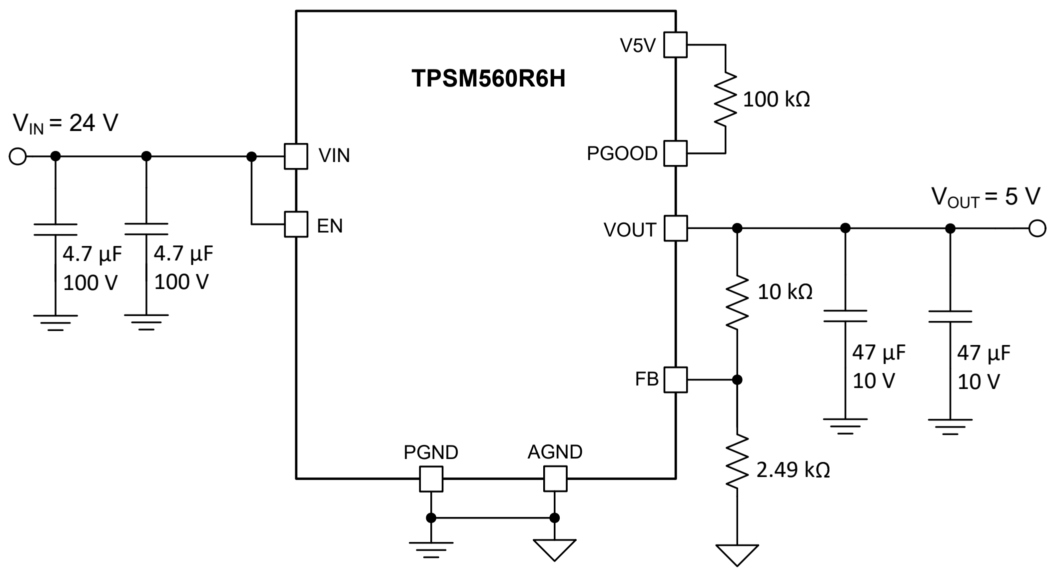


图 8-1. TPSM560R6H Typical Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 as the input parameters and follow the design procedures in 节 8.2.2.

表 8-1. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage V_{IN}	24 V typical
Output voltage V_{OUT}	5 V
Output current rating	600 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM560R6H device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Voltage Setpoint

The output voltage of the TPSM560R6H device is externally adjustable using a resistor divider. The recommended value of R_{FBT} is 10 kΩ. The value for R_{FBB} can be selected from 表 7-1 or calculated using 方程式 2:

$$R_{FBB} = \frac{1.0}{V_{OUT} - 1.0} \times R_{FBT} \tag{2}$$

For the desired output voltage of 5 V, the formula yields a value of 2.5 kΩ. Choose the closest available standard value of 2.49 kΩ for R_{FBB}.

8.2.2.3 Input Capacitor Selection

The TPSM560R6H requires a minimum input capacitance of 2 × 4.7-µF ceramic type. High-quality ceramic type X5R or X7R capacitors with sufficient voltage rating are recommended. The voltage rating of input capacitors must be greater than the maximum input voltage.

For this design, 2 × 4.7-µF, 100-V ceramic capacitors are selected.

8.2.2.4 Output Capacitor Selection

The TPSM560R6H requires a minimum amount of output capacitance for proper operation. The minimum amount of required output varies depending on the output voltage. See 图 7-2 for the required output capacitance. Additional output capacitance can be added to reduce ripple voltage or for applications with transient load requirements.

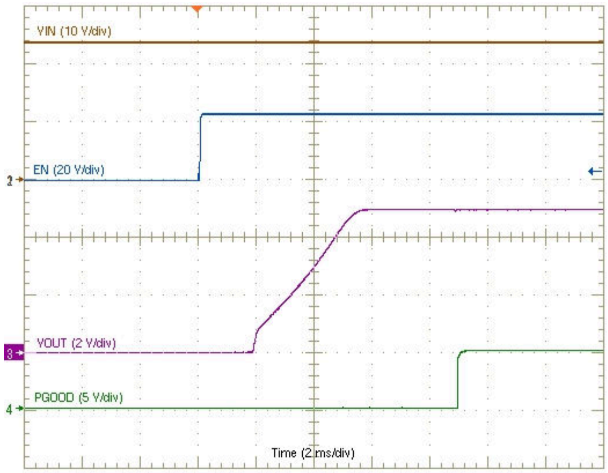
For this design example, 2 × 47-µF, 10-V, ceramic capacitors are used.

8.2.2.5 Power-Good Signal

Use a pullup resistor between the PGOOD pin and a valid voltage source for applications requiring a power-good signal to indicate that the output voltage is present and in regulation.

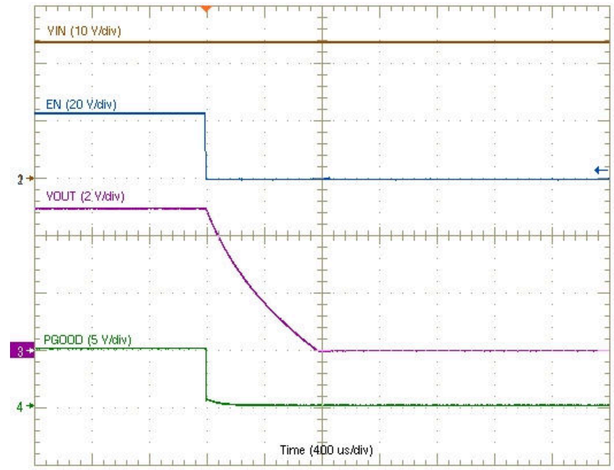
For this design, a 100-kΩ resistor is placed between the PGOOD pin and the V5V pin (the internal 5-V LDO output).

8.2.3 Application Curves



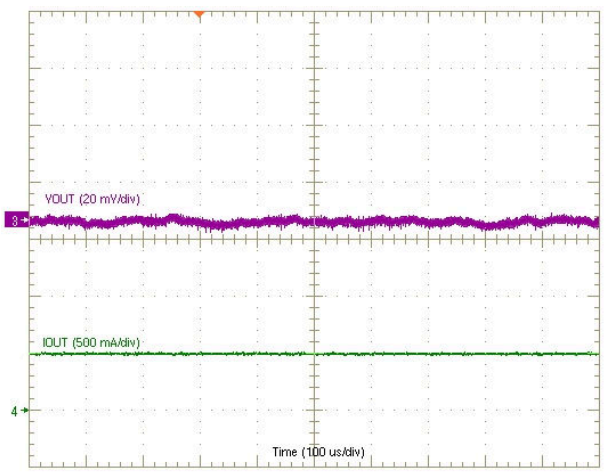
V_{IN} = 24 V V_{OUT} = 5 V I_{OUT} = 600 mA

图 8-2. Start-Up Waveforms



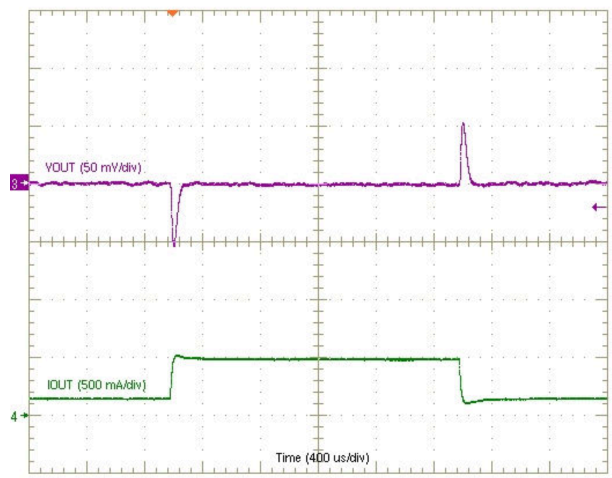
V_{IN} = 24 V V_{OUT} = 5 V I_{OUT} = 600 mA

图 8-3. Enable Shutdown Waveforms



C_{OUT} = 2 × 47 µF I_{OUT} = 600 mA

图 8-4. Output Ripple Waveform



C_{OUT} = 2 × 47 µF   400-mA load step   2.5 A/µs

图 8-5. Transient Response Waveform

9 Power Supply Recommendations

The TPSM560R6H is designed to operate from an input voltage supply range between 4.2 V and 60 V. This input supply must be able to provide the maximum input current and maintain a voltage above the set UVLO voltage. Ensure that the resistance of the input supply rail is low enough that an input current transient does not cause a high enough drop at the TPSM560R6H supply rail to cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the TPSM560R6H, additional bulk capacitance can be required in addition to the ceramic input capacitance. A 47-µF electrolytic capacitor is a typical choice for this function because the capacitor ESR provides a level of damping against input filter resonances. A typical ESR of 0.5 Ω provides enough damping for most input circuit configurations.

10 Layout

The performance of any switching power supply depends as much on the layout of the PCB as the component selection. Use the following guidelines to design a PCB with the best power conversion performance, optimal thermal performance, and minimal generation of unwanted EMI.

10.1 Layout Guidelines

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. 图 10-1 and 图 10-2 show a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- *Connect all PGND pins together using copper plane.*
- Connect the AGND pin to the PGND copper at a single point near the pin.
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Place R_{FBT} and R_{FBB} as close as possible to their respective pins.
- Use multiple vias to connect the power planes to internal layers.

10.2 Layout Example

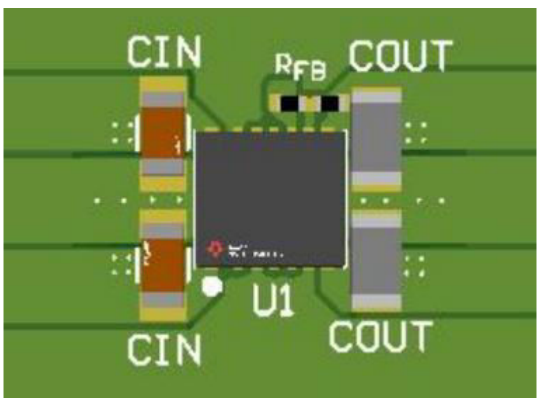


图 10-1. Typical Layout

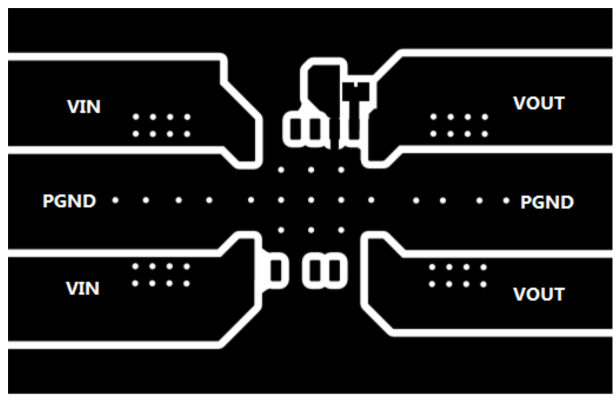


图 10-2. Typical Top-Layer

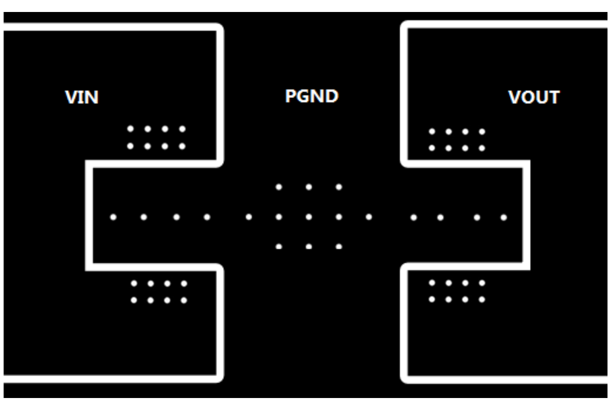


图 10-3. Typical Mid-Layer

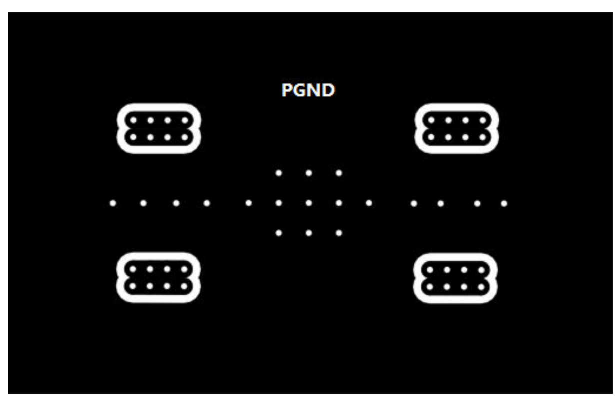


图 10-4. Typical PGND-Layer

10.2.1 Theta JA Versus PCB Area

The amount of PCB copper as well as airflow affects the thermal performance of the device. 图 10-5 shows the effects of copper area and airflow on the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the TPSM560R6H. The junction-to-ambient thermal resistance versus PCB area is plotted for a 4-layer PCB.

To determine the required copper area for an application:

1. Determine the maximum power dissipation of the device in the application by referencing the power dissipation graphs in the *Typical Characteristics*.
2. Calculate the maximum θ_{JA} using 方程式 3 and the maximum ambient temperature of the application.

$$\theta_{JA} = \frac{(125^{\circ}C - T_{A(max)})}{P_{D(max)}} \ (^{\circ}C/W) \tag{3}$$

3. Reference 图 10-5 to determine the minimum required PCB area for the application conditions.

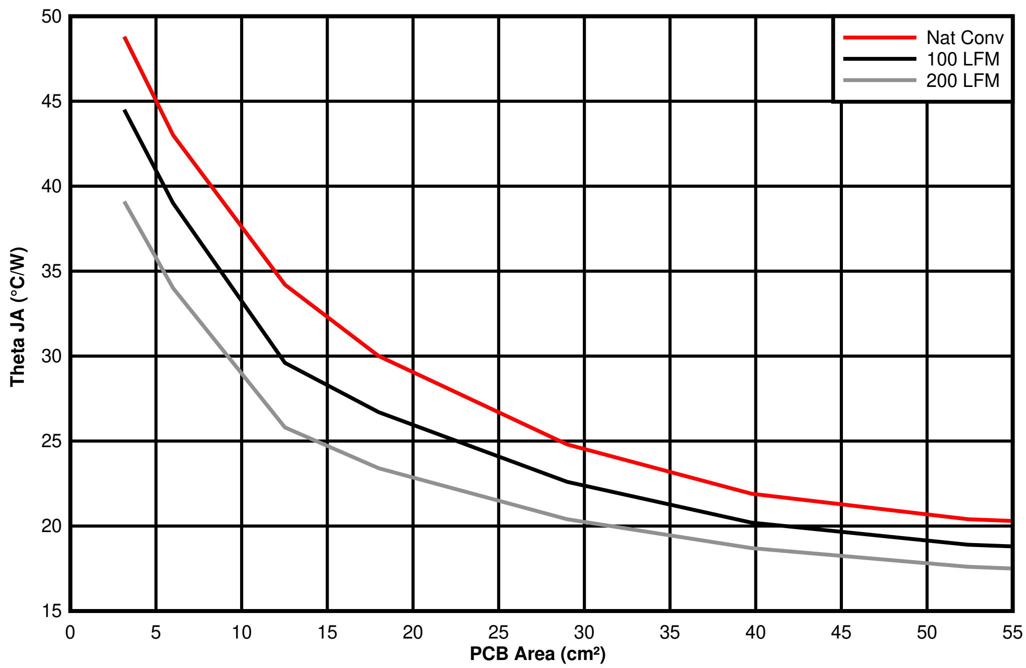


图 10-5. θ_{JA} Versus PCB Area

10.2.2 Package Specifications

表 10-1. Package Specifications Table

TPSM560R6H		VALUE	UNIT
Weight		429	mg
Flammability	Meets UL 94 V-O		
MTBF Calculated Reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign	87.7	MHrs

10.2.3 EMI

The TPSM560R6H is compliant with EN55011 radiated emissions. 图 10-6 through 图 10-9 show typical examples of radiated emission plots for the TPSM5601R5H (1.5-A version). Expect slightly better results for the TPSM560R6H as it is rated for 600 mA. The graphs include the plots of the antenna in the horizontal and vertical positions.

10.2.3.1 EMI Plots

EMI plots were measured using the standard TPSM5601R5HEVM.

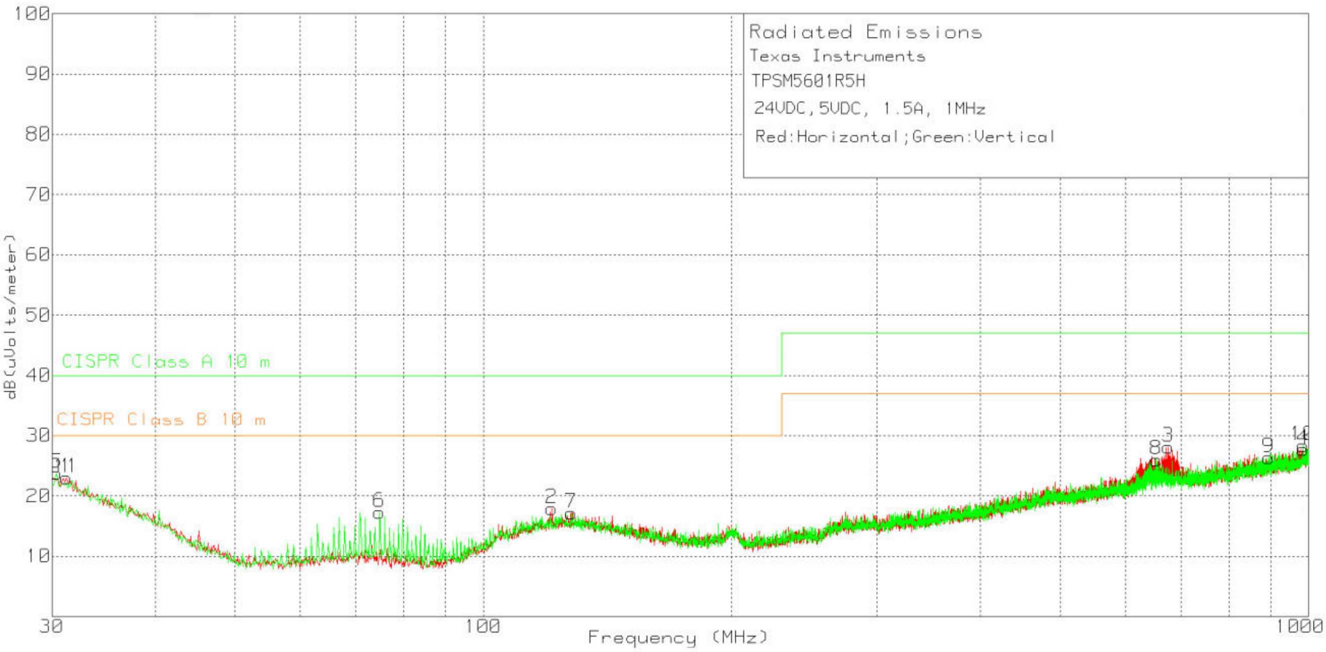


图 10-6. Radiated Emissions 24-V Input, 5-V Output, 1.5-A Load

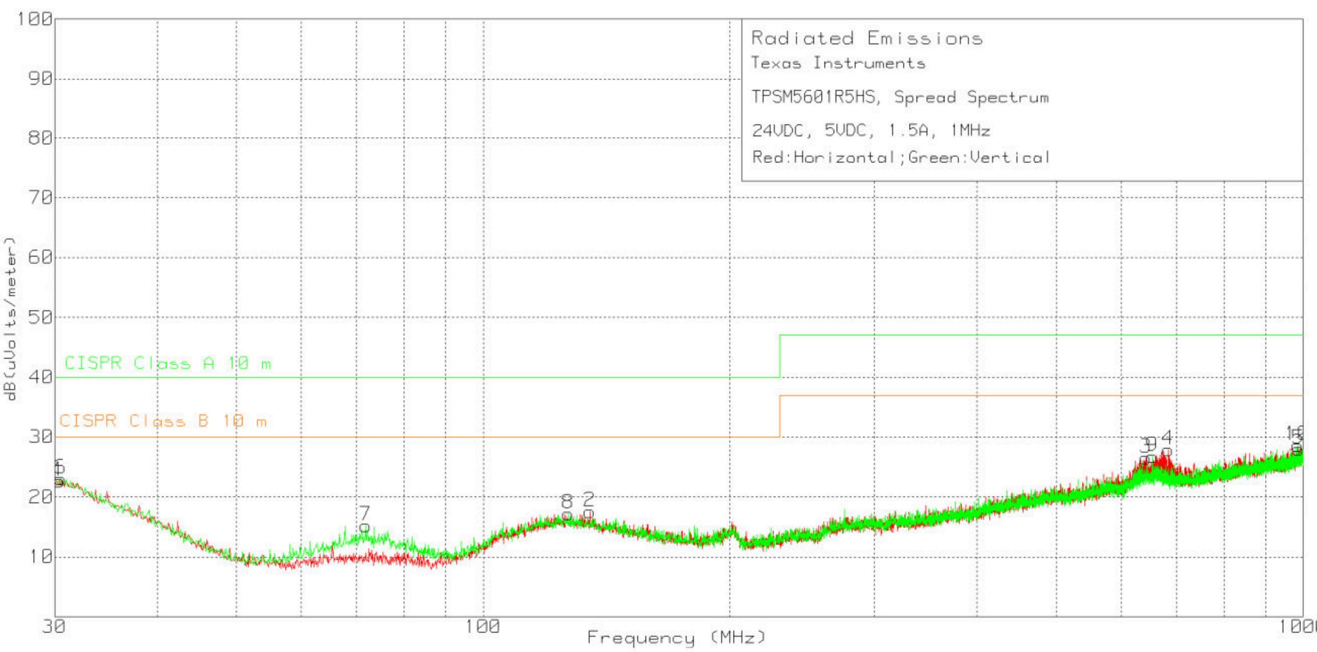


图 10-7. Radiated Emissions 24-V Input, 5-V Output, 1.5-A Load (Spread Spectrum)

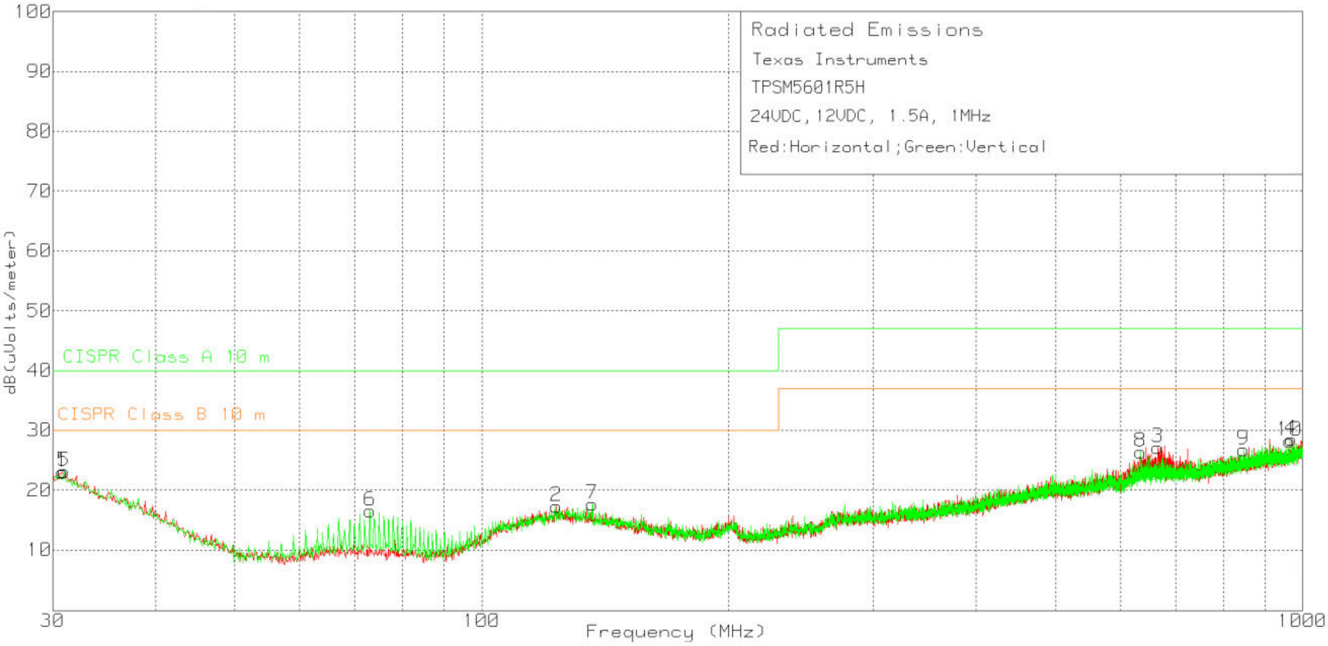


图 10-8. Radiated Emissions 24-V Input, 12-V Output, 1.5-A Load

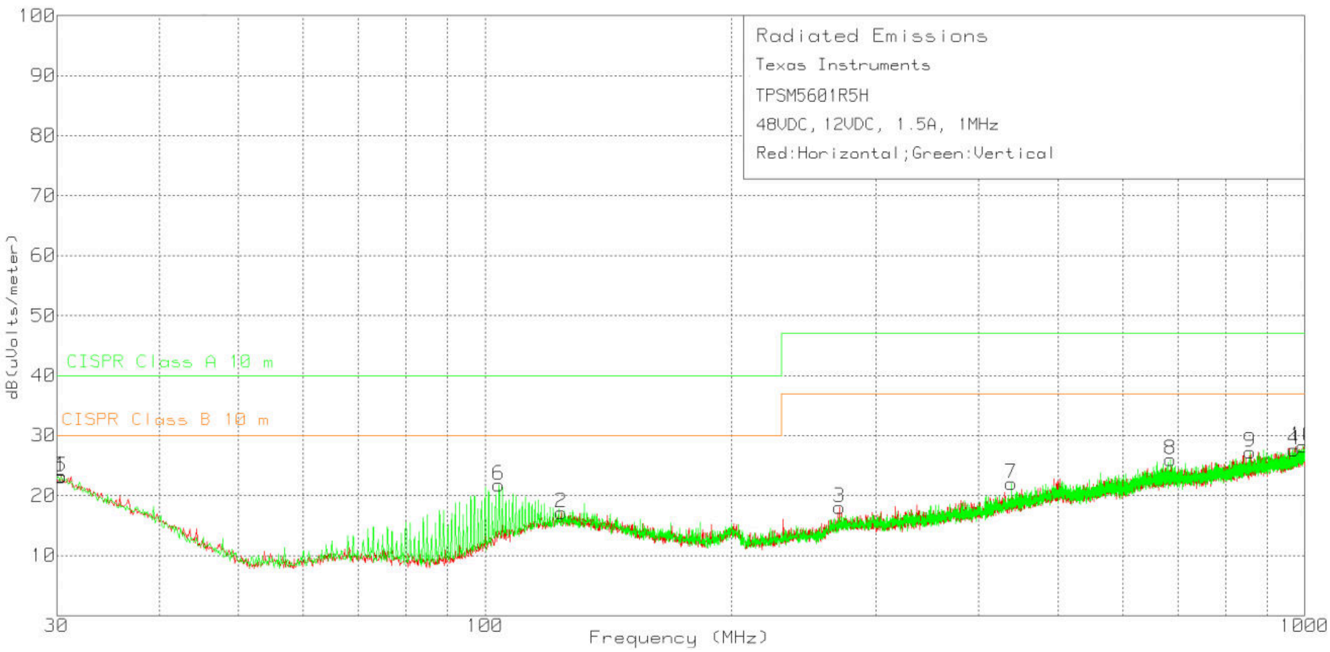


图 10-9. Radiated Emissions 48-V Input, 12-V Output, 1.5-A Load

11 Device and Documentation Support

11.1 Device Support

11.1.1 第三方产品免责声明

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11.1.2 Development Support

For development support, see the following:

- For TI's reference design library, visit TI Designs.
- To view a related device of this product, see the TPSM5601R5Hx.

11.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM560R6H device with WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *TPSM560R6HEVM User's Guide*
- Texas Instruments, *Using the TPSM5601R5Hx in an Inverting Buck-Boost Topology Application Report*
- Texas Instruments, *Using New Thermal Metrics Application Report*
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics Application Report*

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 术语表

TI 术语表　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPSM560R6HRDAR	Active	Production	B3QFN (RDA) | 15	1000 | LARGE T&R	Yes	NIPDAU	Level-3-245C-168 HR	-40 to 125	560R6H
TPSM560R6HRDAR.A	Active	Production	B3QFN (RDA) | 15	1000 | LARGE T&R	Yes	NIPDAU	Level-3-245C-168 HR	-40 to 125	560R6H
TPSM560R6HRDAR.B	Active	Production	B3QFN (RDA) | 15	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

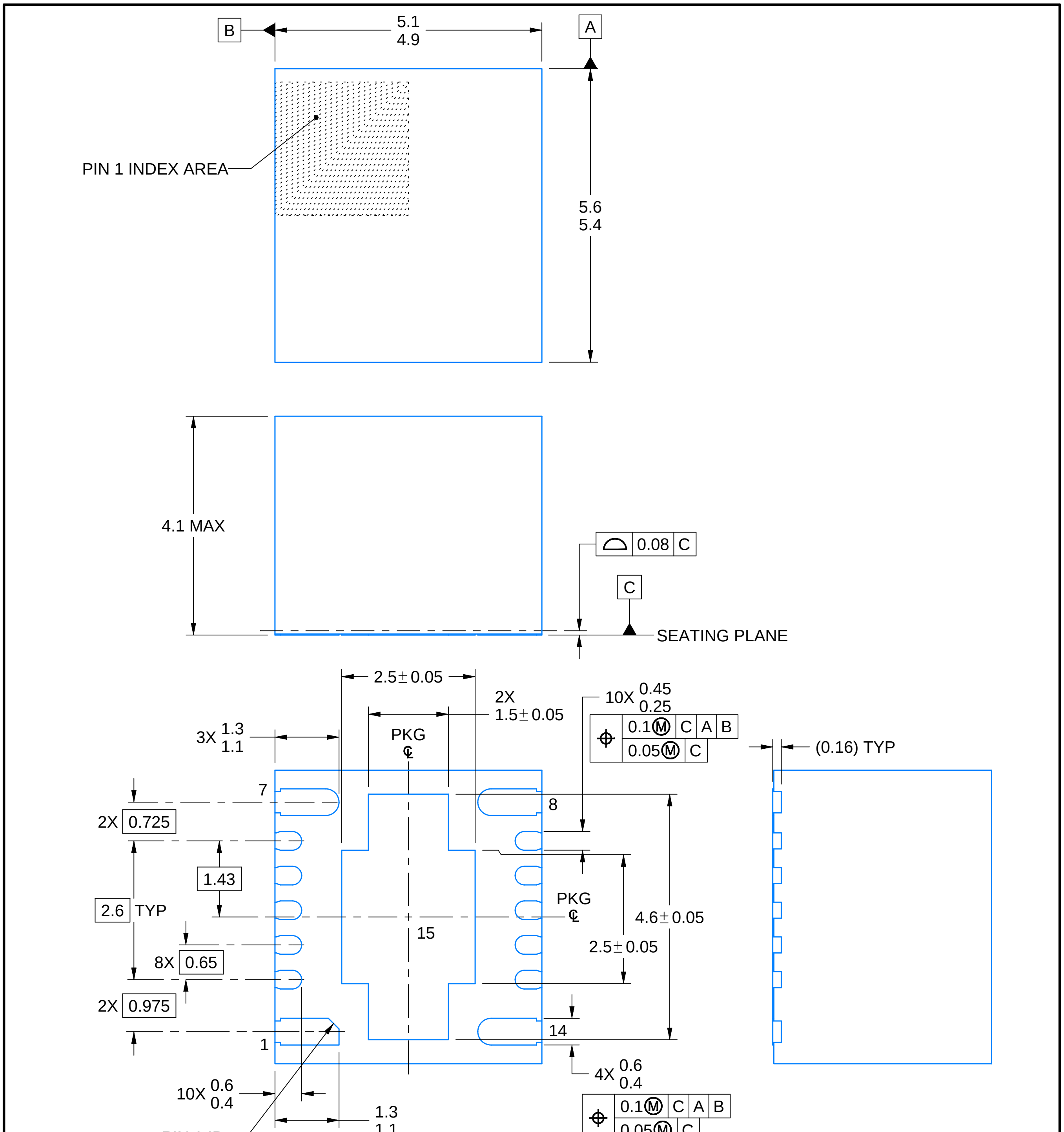
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

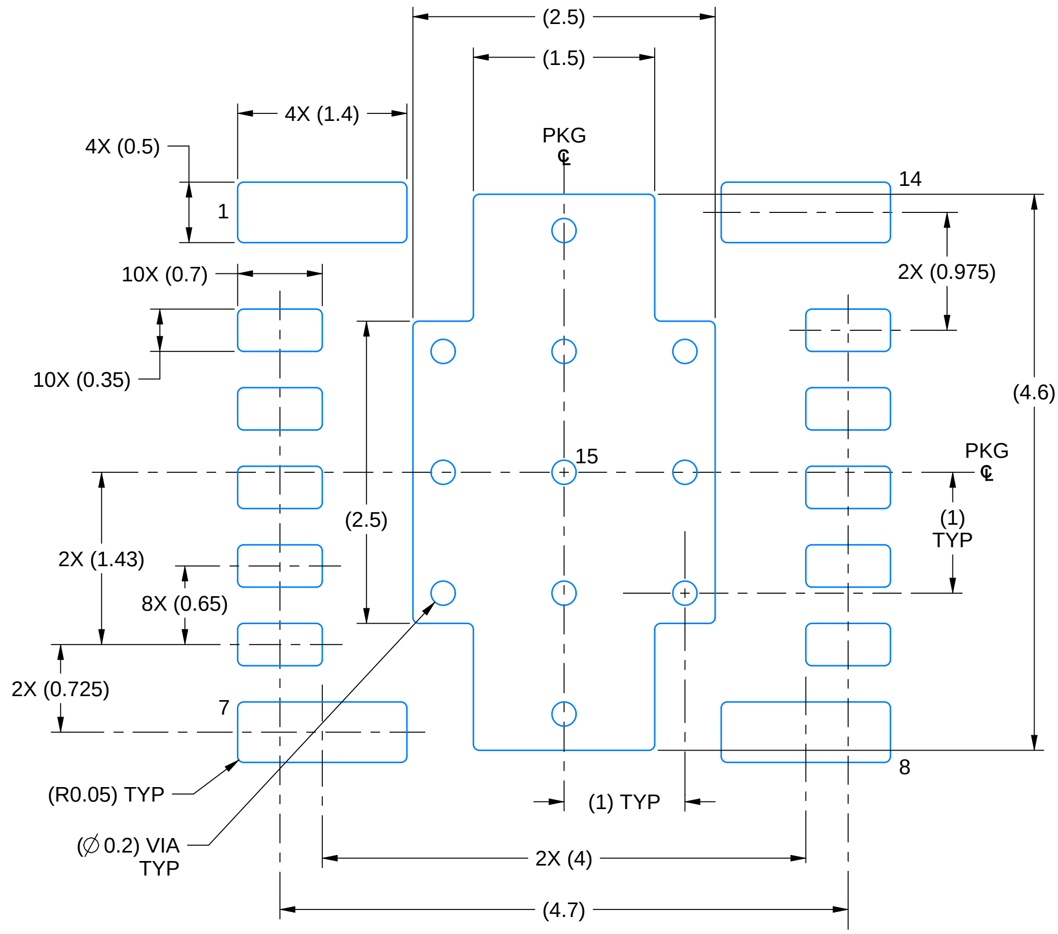
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



4224086/C 03/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



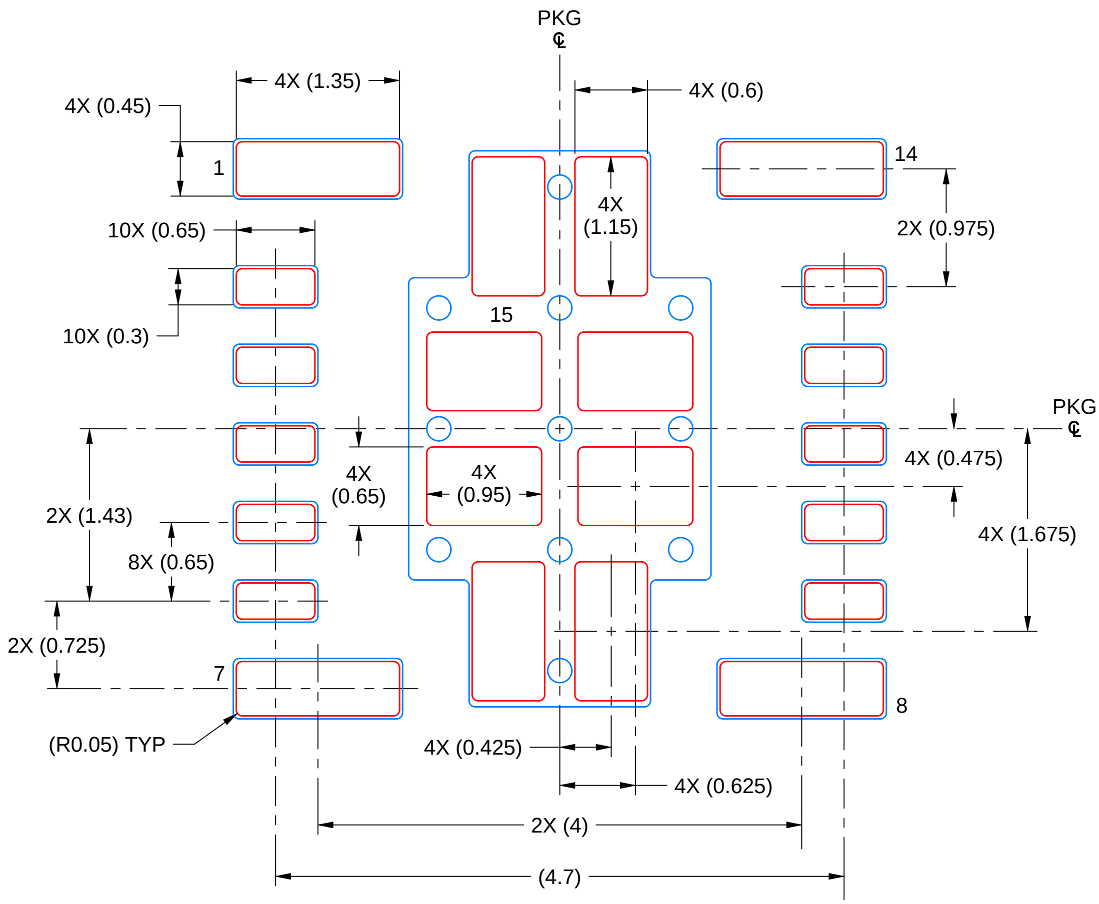
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 16X

SOLDER MASK DETAILS

4224086/C 03/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15:
56% PRINTED SOLDER COVERAGE BY AREA
SCALE: 16X

4224086/C 03/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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