TPSI2140-Q1 具有 2mA 雪崩额定值的 1200V、50mA 汽车类隔离开关

1 特性

- 符合汽车应用要求
  - AEC-Q100 等级 1：–40°C 至 125°C，T_A
- 集成雪崩额定 MOSFET
  - 针对过压条件下的可靠性认证进行设计和认证，包括系统级电介质耐压测试 (Hi-Pot)
    - I_{AVA} = 2mA（5s 脉冲），1mA（60s 脉冲）
  - 1200V 关断电压
  - R_{ON} = 130Ω (T_J = 25°C)
  - T_{ON}，T_{OFF} < 700µs
- 低初级侧电源电流
  - 9mA 导通状态电流
  - 3.5 µA 关断状态电流
- 功能安全型
  - 可帮助进行 ISO 26262 和 IEC 61508 系统设计的文档
- 稳健可靠的隔离栅：
  - 在 1000V_{RMS}/1500V_{DC} 工作电压下预计寿命超过 26 年
  - 隔离额定值 V_{ISO} 高达 3750V_{RMS}/5300V_{DC}
  - 峰值浪涌 V_{IOSM} 高达 5000V
  - ± 100 V/ns CMTI（典型值）
- SOIC 11 引脚 (DWQ) 封装，具有宽引脚，可提高热性能
  - 爬电距离和间隙 ≥ 8mm（初级-次级）
  - 爬电距离和间隙 ≥ 6mm（开关端子之间）
- 安全相关认证
  - （计划）DIN VDE V 0884-11:2017-01
  - （计划）UL 1577 组件认证计划

2 应用

- 固态继电器
- 混合动力、电动和动力传动系统
- 电池管理系统 (BMS)
- 能量存储系统 (ESS)
- 太阳能
- 车载充电器
- 电动汽车充电基础设施
- 另请参阅与这些应用相关的 TI 参考设计。

3 说明

TPSI2140-Q1 是一款隔离式固态继电器，专为高电压汽车和工业应用而设计。TPSI2140-Q1 与 TI 具有高可靠性的电容隔离技术和内部背对背 MOSFET 整合在一起，形成了一款完全集成式解决方案，无需次级侧电源。

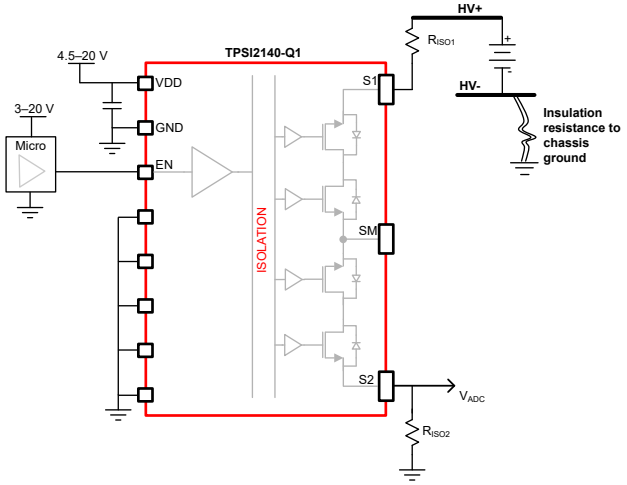
该器件的初级侧仅由 9mA 的输入电流供电，并集成了一个失效防护 EN 引脚，可防止对 VDD 电源反向供电的任何可能性。在大多数应用中，器件的 VDD 引脚应连接到 5V 至 20V 的系统电源，并且器件的 EN 引脚应由逻辑高电平介于 2.1V 至 20V 之间的 GPIO 输出驱动。在其他应用中，VDD 和 EN 引脚可直接由系统电源或 GPIO 输出驱动。TPSI2140-Q1 的所有控制配置都不需要光继电器解决方案通常所需的其他外部元件，例如电阻器和/或低侧开关。

次级侧都包含背对背 MOSFET，从 S1 至 S2 的关断电压为 ±1.2 kV。TPSI2140-Q1 MOSFET 的雪崩稳健性和热敏感封装设计使其能够可靠地支持系统级电介质耐压测试 (HiPot)，并且无需任何外部元件即可承受高达 2mA 的直流快速充电器浪涌电流。

封装信息

器件型号	封装(1)	封装尺寸（标称值）
TPSI2140-Q1	SOIC 11 引脚 (DWQ)	10.3mm × 7.5mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



TPSI2140-Q1 简化版应用原理图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (November 2022) to Revision B (June 2023)	Page
• 将状态从*预告信息*更改为*量产数据*	1
• 更新了“特性”部分中的集成雪崩额定 MOSFET 说明，以添加耐压测试说明	1
• 在“应用”部分中添加了能源存储系统 (ESS) 并更新了链接	1
• Added reference to Layout Guidelines in the Avalanche Robustness section	13
• Updated Layout Guidelines to include further EMI considerations and clarified the high voltage and thermal considerations	22
• Updated EVM images in Layout Example section to show the secondary side metallization for optimized thermals	23
• Added Interlayer Stitch Capacitance Option for EMI and Thermal Optimization in Layout Example section	23

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5 Pin Configuration and Functions

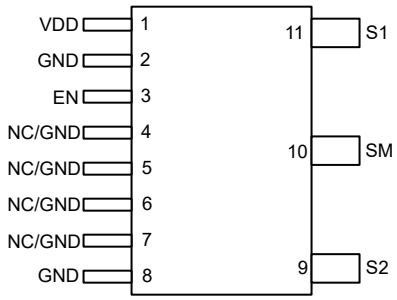

图 5-1. TPSI2140-Q1 DWQ Package, 11-Pin SOIC (Top View)

5.1 Pin Functions

PIN NO.	PIN NAME	TYPE(1)	DESCRIPTION
1	VDD	P	Power supply for primary side
2	GND	GND	Ground supply for primary side
3	EN	I	Active high switch enable signal
4	NC/GND	NC/GND	Internally connected, connect externally to ground or leave floating
5	NC/GND	NC/GND	Internally connected, connect externally to ground or leave floating
6	NC/GND	NC/GND	Internally connected, connect externally to ground or leave floating
7	NC/GND	NC/GND	Internally connected, connect externally to ground or leave floating
8	GND	GND	Internally connected to GND, connect externally to ground or leave floating
9	S2	I/O	Switch input
10	SM	NC	For thermal dissipation only, see Layout Guidelines for more information
11	S1	I/O	Switch input

(1) P = power, I = input, O = output, GND = ground, NC = no connect

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
V_{VDD}	Primary side supply voltage(2)	–0.3	20.7	V
V_{EN}	Enable voltage(2)	–0.3	20.7	V
$I_{S1,S2}$	Switch current, S1/S2	–55	55	mA
$I_{AVA,S1,S2}$	Repetitive avalanche rating, 5s pulse, S1/S2(3)	–2	2	mA
	Repetitive avalanche rating, 60s pulse, S1/S2(4)	–1	1	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Voltage values are with respect to GND.
(3) 5 minutes accumulated over lifetime in increments of no longer than 5 second periods, duty cycle < 33%
(4) 5 minutes accumulated over lifetime in increments of no longer than 60 second periods, duty cycle < 10%

6.2 ESD Ratings

				VALUE	UNIT
HBM_{Prim}	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	Primary Side Pins No. 1-8	±2000	V
HBM_{Sec}		Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 1C	Secondary Side Pins No. 9-11	±1500	V
CDM	Electrostatic discharge	Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4	All pins	±750	V

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{VDD}	Primary side supply voltage(1)	4.5		20	V
V_{EN}	Enable voltage(1)	0		20	V
V_{S2-S1}	Switch input voltage	– 1200		1200	V
$I_{S1,S2}$	Switch current	– 50		50	mA
T_A	Ambient operating temperature	– 40		125	°C
T_J	Junction operating temperature	– 40		150	°C

(1) Voltage values are with respect to GND.

6.4 Thermal Information

THERMAL METRIC (1)		DEVICE DWQ (SOIC) 11 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70	°C/W
$R_{\theta JA, EVM, 60S}$	Junction-to-ambient thermal resistance(2) (3)	52	°C/W
$R_{\theta JA, EVM, 5S}$	Junction-to-ambient thermal resistance(2) (4)	30	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	21	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) EVM PCB dimensions are 74.25mm x 43mm x 1mm. 4 layer PCB with 2oz Cu on layers 1,4 and 1oz Cu on layer 2,3.
(3) Performance of EVM with power applied for 60s.
(4) Performance of EVM with power applied for 5s.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation, total	V_{VDD} = 5 V, V_{EN} = 5 V peak to peak, V_{S1-S2} = 1200V, R_{S1} = 500kΩ f_{EN} = 1Hz square wave			31	mW
P_{D_P}	Maximum power dissipation (primary)				30	mW
P_{D_S}	Maximum power dissipation (secondary)				1	mW

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6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
IEC 60664-1				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	>8	mm
CPG	External Creepage(1)	Shortest terminal-to-terminal distance across the package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>10.5	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	Material Group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ⩽ 300 V_{RMS}	I-IV	
		Rated mains voltage ⩽ 600 V_{RMS}	I-III	
		Rated mains voltage ⩽ 1000 V_{RMS}	I-II	
DIN V VDE 0884-11:2017-01(2), IEC 60747-17:2020				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave)	1000	V_{RMS}
		DC voltage	1500	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60 s (qualification)	5300	V_{PK}
		V_{TEST} = 1.2 × V_{IOTM}, t = 1 s (100% production)	6360	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Tested in oil per IEC 62638-1, 1.2/50 µs waveform, V_{TEST} = 1.3 × V_{IOSM} = 6500 V_{PK} (qualification)	5000	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After I/O safety test subgroup 2/3,V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM} = 1800 V_{PK}, t_m = 10 s	⩽5	pC
		Method a: After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.3 × V_{IORM} = 1950 V_{PK}, t_m = 10 s	⩽5	
		Method b1: At routine test (100% production) and preconditioning (type test), V_{ini} = V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.5 × V_{IORM} = 2250 V_{PK}, t_m = 1 s	⩽5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 × sin (2 π ft), f = 1 MHz	4	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ⩽ T_A ⩽ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
	Climatic category		40/150/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO}, t = 60 s (qualification) V_{TEST} = 1.2 × V_{ISO}, t = 1 s (100% production)	3750	V_{RMS}
Misc.				
V_{ISO}	Withstand isolation voltage		5300	V_{DC}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed-circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.

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6.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Plan to certify according to DIN V VDE V 0884-11:2017-01	Not Planned, contact TI to request.	Plan to certify according to UL 1577 Component Recognition Program	Not Planned, contact TI to request.	Not Planned, contact TI to request.
Maximum transient isolation voltage, 5300 V_{PK}; Maximum repetitive peak isolation voltage, 1500 V_{PK}; Maximum surge isolation voltage, 6000 V_{PK}		Single protection, 3750 V_{RMS}		
Certificate planned		Certificate planned		

6.8 Safety Limiting Values

PARAMETER(1) (2)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety VDD Current	$R_{\theta JA}$ = 70°C/W, V_{VDD} = 20 V, T_J = 150°C, T_A = 25°C			77	mA
	Safety Switch Current (On State)	$R_{\theta JA}$ = 70°C/W, V_{VDD} = 20 V, T_J = 150°C, T_A = 25°C			71	
	Safety Switch Current (Off State, 5 second)	$R_{\theta JA, EVM, 5S}$ (3) = 30°C/W, V_{VDD} = 0 V, T_J = 150°C, T_A = 25°C			2.7	
	Safety Switch Current (Off State, 60 second)	$R_{\theta JA, EVM, 60S}$ (3) = 52°C/W, V_{VDD} = 0 V, T_J = 150°C, T_A = 25°C			1.5	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 70°C/W, T_J = 150°C, T_A = 25°C.			1.78	W
T_S	Maximum safety temperature				150	°C

(1) Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

(2) The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

(3) Assuming PCB layout similar to EVM in Layout Guideline section.

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6.9 Electrical Characteristics

Unless otherwise noted, all minimum/maximum specifications are over recommended operating conditions. All typical values are measured at T_J = 25C, V_{VDD} = 5V, V_{EN} = 5V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PRIMARY SIDE SUPPLY (VDD)						
V_{UVLO_R}	VDD undervoltage threshold rising	VDD rising	4	4.2	4.4	V
V_{UVLO_F}	VDD undervoltage threshold falling	VDD falling	3.9	4.1	4.3	V
V_{UVLO_HYS}	VDD undervoltage threshold hysteresis		40	100	150	mV
I_{VDD_ON}	VDD current, device powered on	T_J = 25°C		9	11	mA
	VDD current, device powered on	–40°C ≤ T_J ≤ 150°C		9	12	mA
I_{VDD_OFF}	VDD current, 5 V, device powered off	V_{VDD} = 5 V, V_{EN} = 0 V, T_J = 25°C		3.5	8	µA
		V_{VDD} = 5 V, V_{EN} = 0 V, T_J = 105°C		4.5	11	µA
		V_{VDD} = 5 V, V_{EN} = 0 V, T_J = 125°C		5.2	16	µA
		V_{VDD} = 5 V, V_{EN} = 0 V, –40°C ≤ T_J ≤ 150°C			30	µA
	VDD current, 20 V, device powered off	V_{VDD} = 20 V, V_{EN} = 0 V, T_J = 25°C		8	10.5	µA
		V_{VDD} = 20 V, V_{EN} = 0 V, T_J = 105°C		10	17	
		V_{VDD} = 20 V, V_{EN} = 0 V, T_J = 125°C		11	25	
		V_{VDD} = 20 V, V_{EN} = 0 V, –40°C ≤ T_J ≤ 150°C			40	
FET CHARACTERISTICS (S1, S2)						
R_{DSON}	On resistance	I_O = 2 mA, T_J = 25°C		130	175	Ω
		I_O = 2 mA, T_J = 85°C		176	235	
		I_O = 2 mA, T_J = 105°C		192	250	
		I_O = 2 mA, T_J = 125°C		210	275	
		I_O = 2 mA, –40°C ≤ T_J ≤ 150°C			300	
I_{OFF}	Off leakage, 1200 V	V = +/– 1200 V, T_J = 25°C		0.02	0.1	µA
		V = +/– 1200 V, T_J = 85°C			0.5	
		V = +/– 1200 V, T_J = 105°C			1.5	
		V = +/– 1200 V, T_J = 125°C			6	
		V = +/– 1200 V, –40°C ≤ T_J ≤ 150°C			50	
	Off leakage, 1000 V	V = +/– 1000 V, T_J = 25°C		0.02	0.1	µA
		V = +/– 1000 V, T_J = 85°C			0.3	
		V = +/– 1000 V, T_J = 105°C			1	
		V = +/– 1000 V, T_J = 125°C			4	
		V = +/– 1000 V, –40°C ≤ T_J ≤ 150°C			35	
V_{AVA}	Avalanche voltage	I_O = 10 µA, T_J = 25°C	1300	1550		V
		I_O = 100 µA, T_J = 150°C	1300	1550		
V_{SM_OFF}	SM voltage	V_{S1} = 1000 V, V_{S2} = 0 V OR V_{S2} = 1000 V, V_{S1} = 0 V	400		600	V
C_{OSS}	S1, S2 capacitance	$V_{S1,S2}$ = 0 V, SM float, F = 1 MHz		75		pF
LOGIC-LEVEL INPUT (EN)						
V_{IL}	Input logic low voltage		0.0		0.8	V
V_{IH}	Input logic high voltage		2.1		20.0	V
V_{HYS}	Input logic hysteresis		100	250	300	mV

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6.9 Electrical Characteristics (continued)

Unless otherwise noted, all minimum/maximum specifications are over recommended operating conditions. All typical values are measured at T_J = 25C, V_{VDD} = 5V, V_{EN} = 5V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL}	Input logic low current	V_{EN} = 0 V	–0.1		0.1	µA
I_{IL}	Input logic low current	V_{EN} = 0.8 V	2	4	6.5	µA
I_{IH}	Input logic high current	V_{EN} = 5 V	10	22	50	µA
I_{IH}	Input logic high current	V_{EN} = 20 V	100	175	350	µA
I_{VDD_FS}	VDD fail-safe current	V_{EN} = 20 V, V_{VDD} = 0 V	–0.1		0.1	µA
R_{PD}	Pulldown resistance	Two point measurement, V_{EN} = 0.5 V and V_{EN} = 0.8 V	100	200	350	kΩ
NOISE IMMUNITY						
CMTI	Common-mode transient immunity	$\|V_{CM}\|$ = 1000 V			100.0	V/ns

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6.10 Switching Characteristics

Unless otherwise noted, all minimum/maximum specifications are over recommended operating conditions. All typical values are measured at T_A = 25C, V_{VDD} = 5V, V_{EN} = 5V.

MODE	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Switching Characteristics							
EN switching	t_{PD_ON}	Input HI to Output voltage falling propagation delay	V_{IN} = 1000 V R_L = 1 MΩ		100	300	µs
	t_F	Output fall time			20	100	
	t_{ON}	Input HI to Output LO delay			160	400	
	t_{PD_OFF}	Input LO to Output voltage rising propagation delay			150	200	
	t_R	Output rise time			50	600	
	t_{OFF}	Input LO to Output HI delay			200	700	
EN and VDD switching	t_{PD_ON}	Input HI to Output voltage falling propagation delay	V_{IN} = 1000 V R_L = 1 MΩ		240	400	µs
	t_F	Output fall time			20	100	
	t_{ON}	Input HI to Output LO delay			260	500	
	t_{PD_OFF}	Input LO to Output voltage rising propagation delay			150	200	
	t_R	Output rise time			50	600	
	t_{OFF}	Input LO to Output HI delay			200	700	

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7 Parameter Measurement Information

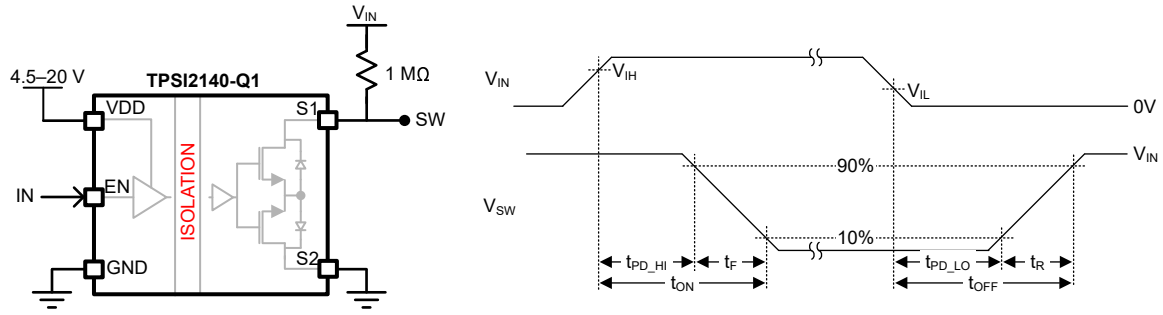

图 7-1. Timing Diagram, EN Switching

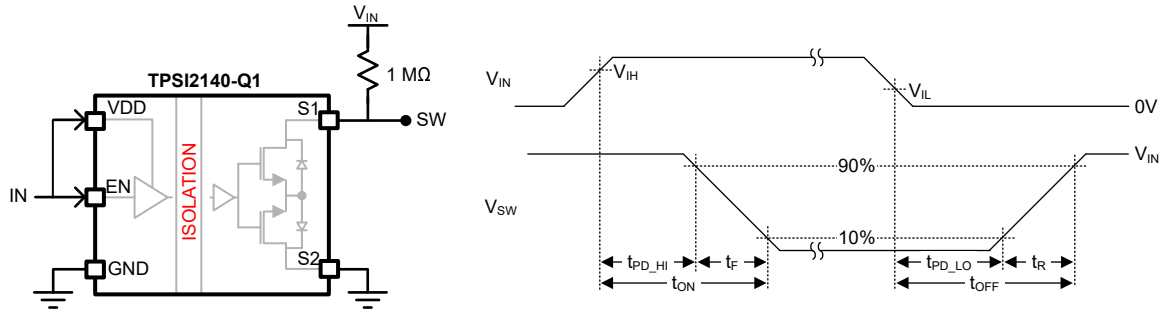

图 7-2. Timing Diagram, EN and VDD Switching

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8 Detailed Description

8.1 Overview

The TPSI2140-Q1 is an isolated solid state relay designed for high voltage automotive and industrial applications. TI's high reliability capacitive isolation technology in combination with back-to-back MOSFETs form a completely integrated solution requiring no secondary side power supply.

As seen in the *Functional Block Diagram*, the primary side consists of a driver which delivers power and enable logic information to each of the internal MOSFETs on the secondary side. The on-board oscillator controls the frequency of the driver's operation and the Spread Spectrum Modulation (SSM) controller varies the driver frequency to improve system EMI performance. When the enable pin is brought HI and the VDD voltage is above the UVLO threshold, the oscillator starts and the driver sends power and a logic HI across the barrier. When the enable pin is brought LO or the VDD voltage falls below the UVLO threshold, the driver is disabled. The lack of activity communicates a logic LO to the secondary side and the MOSFETs are disabled.

Each MOSFET on the secondary side has a dedicated full-bridge rectifier to form its local power supply and a receiver. The receiver determines the logic state delivered from the primary side through the capacitive isolation barrier and uses a slew rate controlled driver to drive the MOSFET's gate. Each receiver performs signal conditioning on the signals received across the barrier in order to filter common mode interference and ensure that the MOSFETs are controlled according to the logic sent by the primary side driver and the system.

The avalanche robust MOSFETs and the thermal benefits of the widened pins on the 11 DWQ package enable the TPSI2140-Q1 to support dielectric withstand testing (HiPot) and DC fast charger surge currents of up to 2 mA without requiring any external protection components.

8.2 Functional Block Diagram

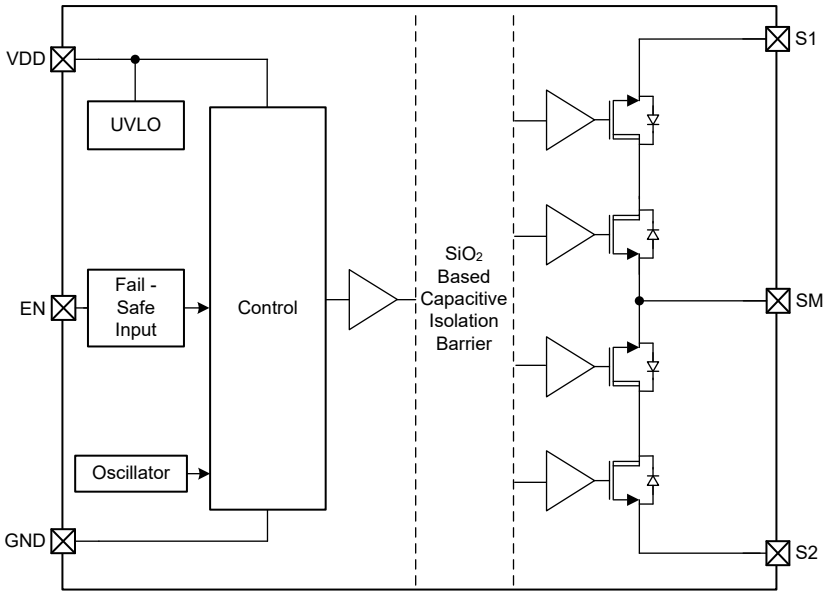

图 8-1. TPSI2140-Q1 Block Diagram

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8.3 Feature Description

8.3.1 Avalanche Robustness

When the voltage between the S1 and S2 pins exceeds +/-1200 V the secondary side MOSFETs could enter an avalanche mode of operation. The MOSFETs and the 11 DWQ package have been designed and qualified to be robust in this mode of operation to support Dielectric Withstand Testing (HiPot). To help ensure the thermal performance of the the system in this mode of operation, refer to the PCB Layout Guidelines.

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8.4 Device Functional Modes

表 8-1. Device Functional Modes

VDD	EN	S1-S2 State	COMMENTS
Powered Up(1)	L	OFF	VDD current is in OFF state range.
	H	ON	VDD current is in ON state range.
Powered Down(2)	L	OFF	VDD current is in OFF state range.
	H	OFF	Primary side analog is powered on, VDD current is between OFF state and ON state ranges.

(1) VDD ⩾ VDD undervoltage rising threshold.
(2) VDD ⩽ VDD undervoltage falling threshold.

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9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The TPSI2140-Q1 is a 1200-V, 50-mA automotive isolated switch optimized for high voltage switching in measurement applications, especially those that require switching across an isolation barrier or galvanically isolated domain. Common end equipments include energy storage systems (ESS), solar panel arrays, EV chargers, and EV battery management systems. The device enables the system designer to reduce cost and improve reliability by replacing mechanical relays and optically isolated devices.

The TPSI2140-Q1's enable input is fail safe and does not need to be driven from the same domain as the VDD pin supply.

The TPSI2140-Q1 supports an input voltage range of 4.5 V to 20 V on the VDD primary supply pin and a logic high of 2.1 V to 20 V on the enable pin. The secondary side supports high voltage switching from –1200 V to 1200 V.

TI Reference Designs

The TI reference designs linked below are a helpful introduction to high voltage applications using the TPSI2140-Q1. To maximize the thermal performance of the TPSI2140-Q1 for dielectric withstand testing (HiPot), please follow the Layout Guidelines contained within this datasheet.

- TIDA-010232: High Voltage Insulation Monitoring
- TIDA-01513: Automotive High Voltage and Isolation Leakage Measurements

9.2 Typical Application

Insulation Resistance Monitoring

In high voltage applications such as electric vehicle systems, the high voltage battery pack is intentionally isolated from the chassis domain of the car to protect the driver and prevent damage to electrical components. These systems actively monitor the integrity of this insulation to ensure the safety of the system throughout its lifetime. This active monitoring is referred to as insulation resistance monitoring (also known as isolation check, insulation check, isolation monitoring, insulation monitoring, and residual current monitoring (RCM)) and is performed by measuring the resistances from each of the battery terminals to the chassis ground, illustrated below as R_{ISOP} and R_{ISON}.

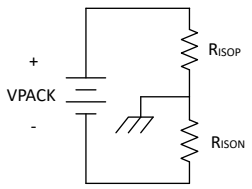

图 9-1. Insulation Resistance Model

There are multiple design architectures using the TPSI2140-Q1 to measure these insulation resistances, R_{ISOP} and R_{ISON}. Some architectures employ a microcontroller that performs measurements from the high voltage domain, which will be referred to in this document as the Battery V- Reference architecture. Others use a

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microcontroller in the low voltage domain, which will be referred to in this document as the Chassis Ground Reference architecture. The primary difference between the two architectures is the node that the MCU uses as its GND reference. An example of a Battery V- MCU is the BQ79631-Q1 UIR sensor.

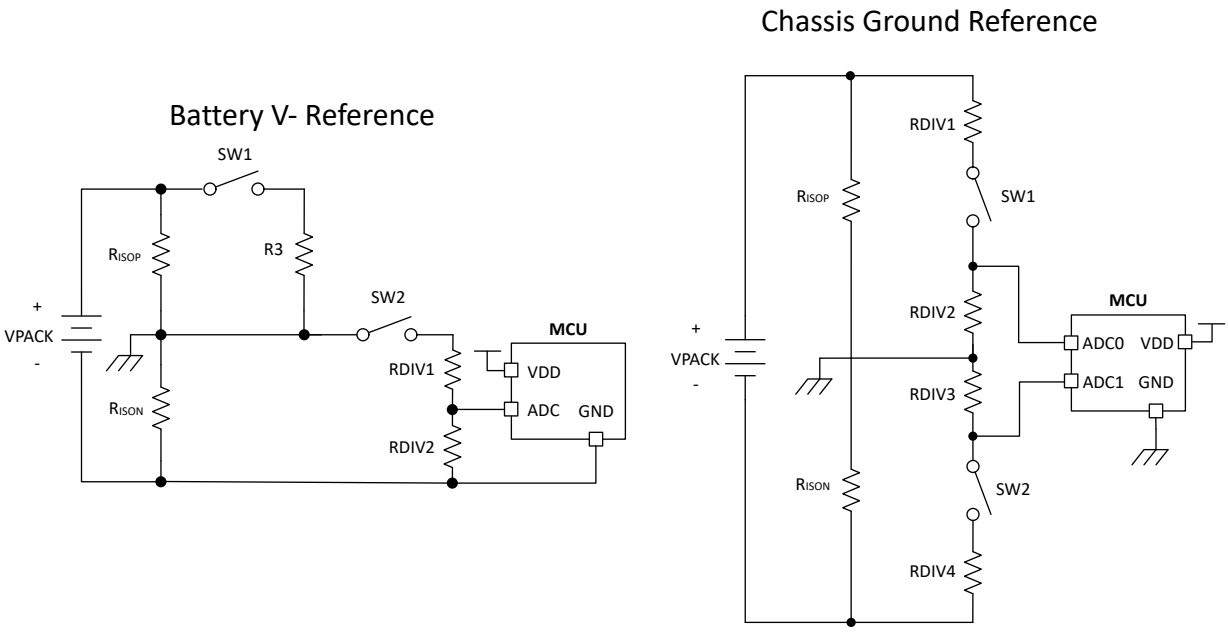

图 9-2. Different MCU ADC Reference Examples

The two following sections demonstrate the measurement algorithms and the systems of equations used to calculate the isolation resistances using each architecture.

Battery V- Reference Example

A Battery V- Reference architecture is shown below with the TPSI2140-Q1 illustrated as a switch (SW1 and SW2). SW2 initiates a connection between the chassis and PACK- and enables the measurement path to the ADC. SW1 initiates a connection between the chassis and the PACK+. RDIV1 and RDIV2 form a divider which scales the measured voltages down to the appropriate ADC range.

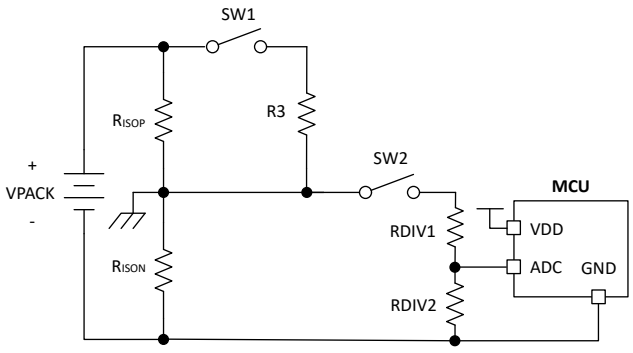

图 9-3. Battery V- Reference Architecture

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Two ADC measurements must be taken in order to obtain enough information to calculate the two unknown isolation resistances. The first measurement is taken with SW1 open and SW2 closed. The second measurement is taken with SW1 closed and SW2 closed. With these two measurements it is possible to solve the system of equations and calculate R_{ISOP} and R_{ISON}.

In the following example the voltage on the chassis ground is arbitrarily referred to as V_{RISONx}.

For the first ADC measurement SW2 is closed as shown below and the following equations relate the ADC voltage to the other parameters in the system in this condition:

- V_{ADC1} measurement 1: SW1 open, SW2 closed

$$V_{RISON1} = V_{PACK} \times \frac{R_{ISON} || (R_{DIV1} + R_{DIV2})}{R_{ISOP} + (R_{ISON} || R_{DIV1} + R_{DIV2})} \quad (1)$$

$$V_{ADC1} = V_{RISON1} \times \frac{R_{DIV2}}{R_{DIV1} + R_{DIV2}} \quad (2)$$

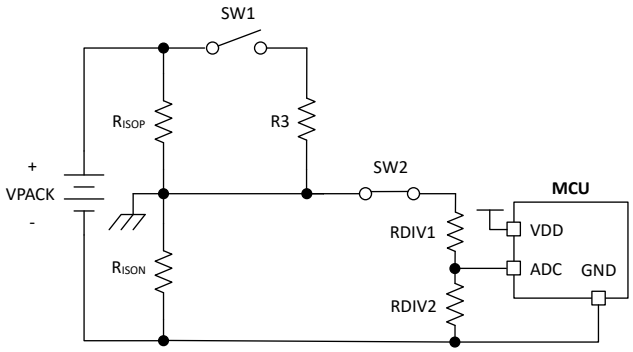

图 9-4. Battery V- Reference Switch Positions for ADC1 Measurement

For the second ADC measurement SW1 and SW2 are closed as shown below and the following equations relate the ADC voltage to the other parameters in the system in this condition:

- V_{ADC2} measurement 2: SW1 closed, SW2 closed

$$V_{RISON2} = V_{PACK} \times \frac{R_{ISON} || (R_{DIV1} + R_{DIV2})}{(R_{ISOP} || R_3) + (R_{ISON} || (R_{DIV1} + R_{DIV2})} \quad (3)$$

$$V_{ADC2} = V_{RISON2} \times \frac{R_{DIV2}}{R_{DIV1} + R_{DIV2}} \quad (4)$$

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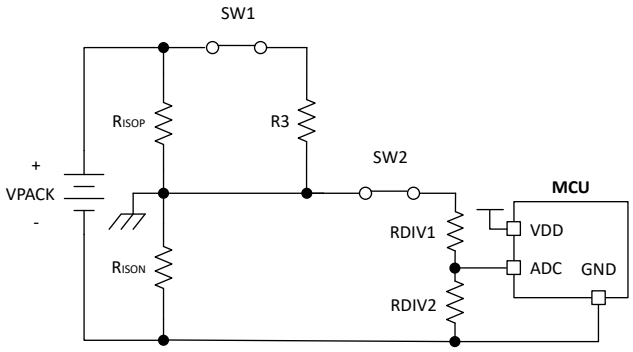

图 9-5. Battery V- Reference Switch Positions for ADC2 Measurement

Chassis Ground Reference Example

A Chassis Ground Reference architecture is shown below. SW1 and SW2 initiate connections to the PACK+ and PACK-, and enable their corresponding measurement paths to their ADCs through their corresponding resistor dividers. RDIV1, RDIV2, RDIV3, and RDIV4 scale the measured voltages down to the appropriate ADC ranges.

This first measurement is taken with SW1 closed and SW2 open and the second measurement is taken with SW1 open and SW2 closed.

- VADC0: SW1 closed, SW2 open

$$V_{ADC1} = V_{RDIV2} = V_{PACK}\frac{(R_{ISOP}||(R_{DIV1}+R_{DIV2}))}{(R_{ISOP}||(R_{DIV1}+R_{DIV2})+R_{ISON})} \times \frac{R_{DIV2}}{R_{DIV1}+R_{DIV2}} \quad (5)$$

- VADC1: SW1 open, SW2 closed

$$V_{ADC2} = V_{RDIV3} = -V_{PACK}\frac{(R_{ISON}||(R_{DIV3}+R_{DIV4}))}{(R_{ISON}||(R_{DIV3}+R_{DIV4}))+R_{ISOP})} \times \frac{R_{DIV3}}{R_{DIV3}+R_{DIV4}} \quad (6)$$

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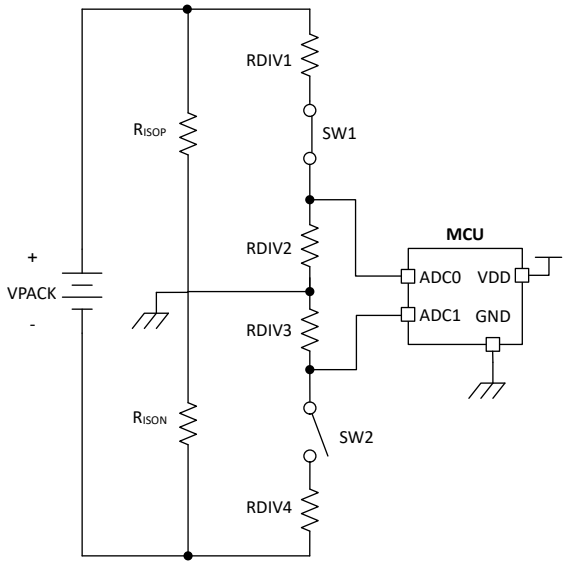

图 9-6. Chassis Ground Reference Switch Positions for ADC1 Measurement

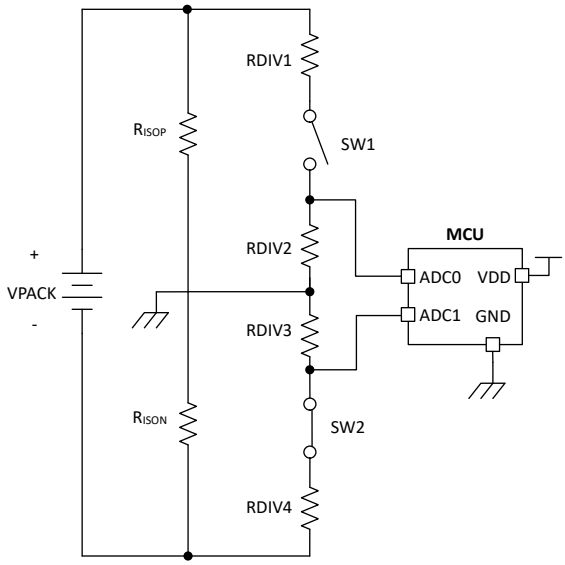

图 9-7. Chassis Ground Reference Switch Positions for ADC2 Measurement

Battery V- Reference and Chassis Ground Reference Architectures with the TPSI2140-Q1

The circuits in 图 9-8 and 图 9-9 demonstrate how to connect the TPSI2140-Q1 as a switch in each of the architectures above.

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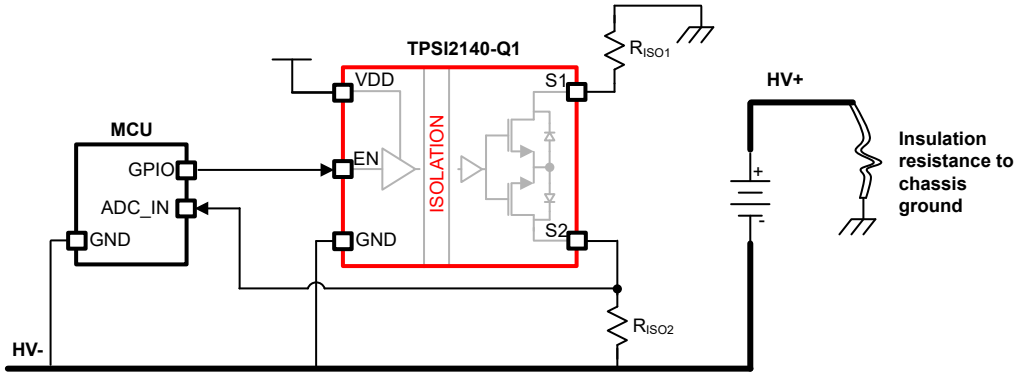

图 9-8. TPSI2140-Q1 Insulation Resistance Monitoring – Battery V- Reference

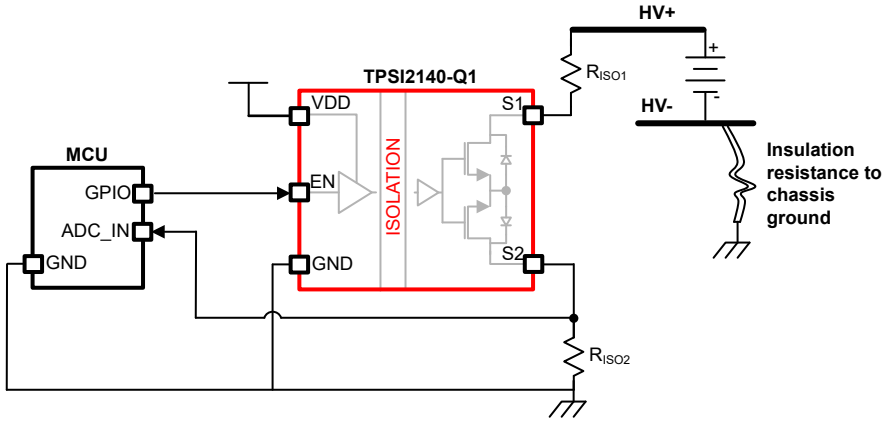

图 9-9. TPSI2140-Q1 Insulation Resistance Monitoring – Chassis Ground Reference

9.2.1 Dielectric Withstand Testing (HiPot)

The TPSI2140-Q1 is specifically designed to support dielectric withstand testing. In a high voltage system, a dielectric withstand test (HiPot) may be administered during the characterization, production or maintenance of the system to validate the reliability of the insulation barriers and galvanically isolated domains it contains. These withstand voltage tests intentionally stress the components spanning these domains and put them in an overvoltage condition. MOSFETs that are placed under these overvoltage conditions will enter avalanche mode and begin conducting current at a high voltage, dissipating high power and heating up. The design and qualification of the TPSI2140-Q1 was completed with this state in mind and supports up to 2 mA I_{AVA} for 5 seconds intervals and 1 mA I_{AVA} for 60 second intervals.

The dielectric withstand test voltage (V_{HiPot}), the TPSI2140-Q1's avalanche voltage (V_{AVA}), and the resistance (R) in series with the TPSI2140-Q1 should limit the avalanche current (I_{AVA}) to the corresponding current limit depending on the test duration. In addition, the PCB design should follow the recommendations in the Layout Guidelines section to ensure adequate thermal performance to keep the junction temperature (T_J) below the absolute maximum rating of the TPSI2140-Q1.

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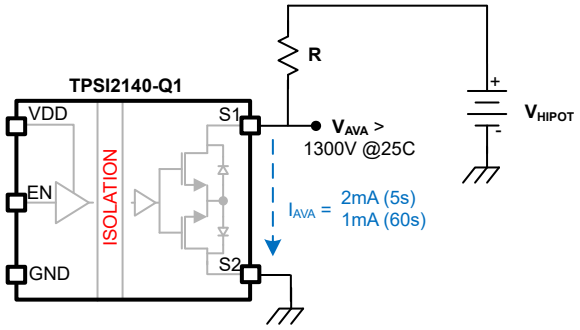

图 9-10. Dielectric Withstand Test (HiPot) - Simplified Schematic

9.2.2 Design Requirements

表 9-1 lists the Design Requirements for a typical insulation resistance monitoring application using the Chassis Ground Reference architecture and the TPSI2140-Q1 for switching.

表 9-1. Typical Design Parameters For Insulation Resistance Monitoring Using the TPSI2140-Q1 – Chassis Ground Reference Architecture

PARAMETER	VALUE
V_{PACK} Voltage (maximum)	1000 V
Primary side supply (V_{VDD})	5 V ±10 %
Dielectric withstand voltage test	3500 V
	5 s
Surge voltage (IEC61000-3-5)	2500 V

9.2.3 Design Procedure - Chassis Ground Reference

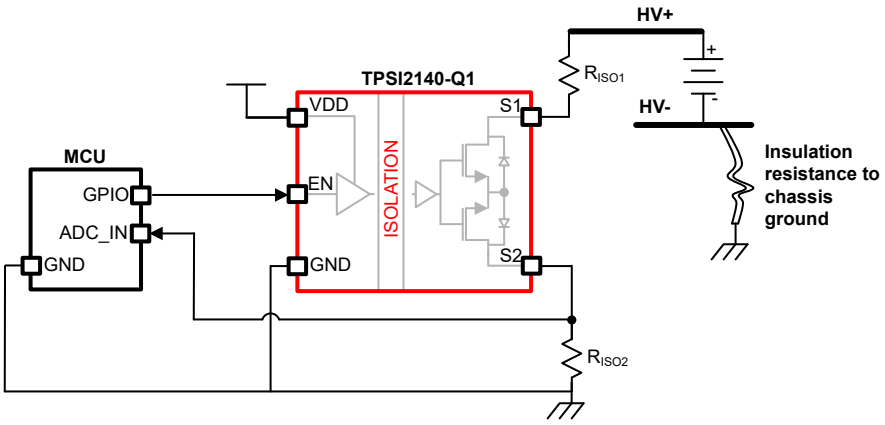

图 9-11. Chassis Ground Reference

R_{ISO1} Selection

In order to protect the TPSI2140-Q1, R_{ISO1} must be sized to limit the current in an overvoltage condition. The amount of resistance required to protect the TPSI2140-Q1 depends on the amount of overvoltage applied. For example, during a dielectric withstand voltage test (HiPot) of 3500 V for 5 seconds, the S1 to S2 voltage will be clamped to 1300 V (V_{AVA} minimum) by the TPSI2140-Q1 and the R_{ISO1} resistance required to keep the current under 2 mA would be 1.1 MΩ.

$$I_{AVA} = \frac{V_{HIPOT} - V_{AVA}}{R_{ISO1}} = \frac{3500V - 1300V}{1.1\ M\Omega} = 2.0mA \quad (7)$$

If the high potential test lasts for 60 seconds, the R_{ISO1} resistance must be doubled to 2.2 MΩ to keep the current below 1 mA.

DC Overvoltage	R_{ISO1} Minimum (5 second intervals)	R_{ISO1} Minimum (60 second intervals)
2000 V	350 kΩ	700 kΩ
2500 V	600 kΩ	1200 kΩ
3500 V	1100 kΩ	2200 kΩ
4300 V	1500 kΩ	3000 MΩ

9.3 Power Supply Recommendations

To ensure a reliable supply voltage, TI recommends that a 100-nF ceramic capacitor be placed between the VDD pin and the GND pin of the TPSI2140-Q1. The capacitor should be placed as close to the device's VDD pin as possible < 10 mm.

9.4 Layout

9.4.1 Layout Guidelines

Component placement:

Decoupling capacitors for the primary side VDD supply must be placed as close as possible to the device pins.

EMI considerations:

The TPSI2140-Q1 employs spread spectrum modulation (SSM) and in some systems, no additional system design considerations are required to meet the EMI performance needs.

However, the system designer may choose to take additional measures to minimize EMI depending on the system requirements and safety preferences of the system designer. The measures listed below reduce emissions by providing a capacitive return path from the secondary side to the primary side or by increasing the common mode loop impedance with an inductive component on the primary side.

- **Capacitive Return Paths:**
  - An interlayer stitching capacitance in the range of 10-20 pF can be implemented on the PCB. This zero-cost implementation is typically preferred as it also serves the purpose of thermal performance improvement if placed directly underneath the TPSI2140-Q1. Please see the Layout Example for more details.
  - Most system designs already employ discrete Y capacitors or contain an amount of parasitic Y capacitance between the high voltage and low voltage domains. If this Y capacitance is located on the same board as the TPSI2140-Q1, they will act as a capacitive return path.
  - Discrete high voltage capacitors could also be placed between the GND pin and the S1 or S2 terminals.
- **Inductive Components:**
  - A pair of ferrite beads or a common mode choke with a high frequency impedance in the range of 10 kΩ may be placed in series with the system VDD pin and GND pin supply on the primary side of the TPSI2140-Q1.

High-voltage considerations:

The creepage from the primary side to the secondary side and from the creepage from the S1 pin to S2 pin of the TPSI2140-Q1 should be maintained according to system requirements. It is most likely that the system designer will avoid any top layer PCB routing underneath the body of the package or between the S1 and S2 pins.

Thermal considerations:

If the system designer plans to use the TPSI2140-Q1 in avalanche mode, it is important for the PCB layout to be designed with thermal performance in mind. Proper PCB layout can help dissipate heat from the device to the PCB and keep the junction temperature (T_J) under the absolute maximum rating. Floating inner layer planes or

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the planes used to implement a stitch capacitor can be drawn beneath the secondary side pins or directly beneath the TPSI2140-Q1 for improved heat dissipation. An example of this can be seen in the Layout Example.

9.4.2 Layout Example

Varying PCB implementations are possible depending on both the system EMI requirements and the system dielectric withstand testing (HiPot) parameters. The following sections detail the TPSI2140-Q1 EVM with Thermal Optimization with secondary side metallization for optimized thermal performance and the Interlayer Stitch Capacitance Option for EMI and Thermal Optimization.

TPSI2140-Q1 EVM with Thermal Optimization

The TPSI2140-Q1 EVM images below demonstrate a secondary side thermal metallization pattern and internal floating metal that provides thermal relief to the TPSI2140-Q1 during system dielectric withstand testing (HiPot). The TPSI2140-Q1 Secondary Side Layout Recommendation for Optimized Thermal Performance: Top Layer 1 shows the top side creepage and clearance considerations.

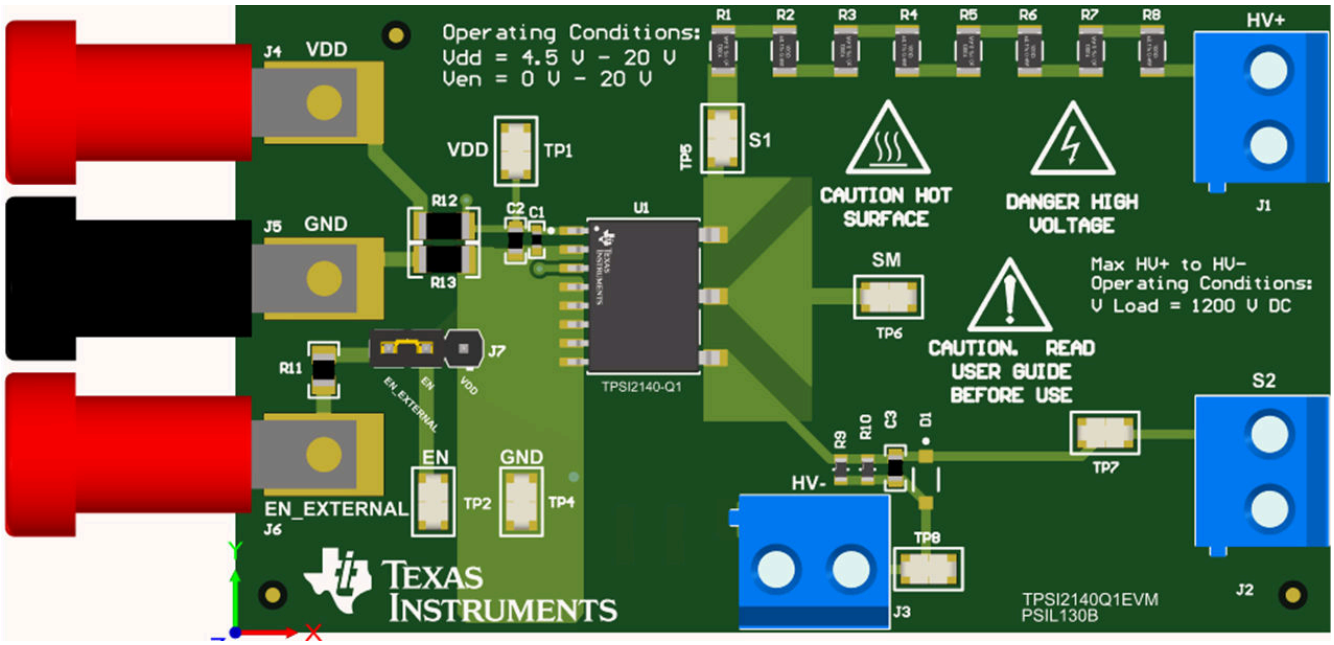

图 9-12. TPSI2140-Q1 EVM - Component View

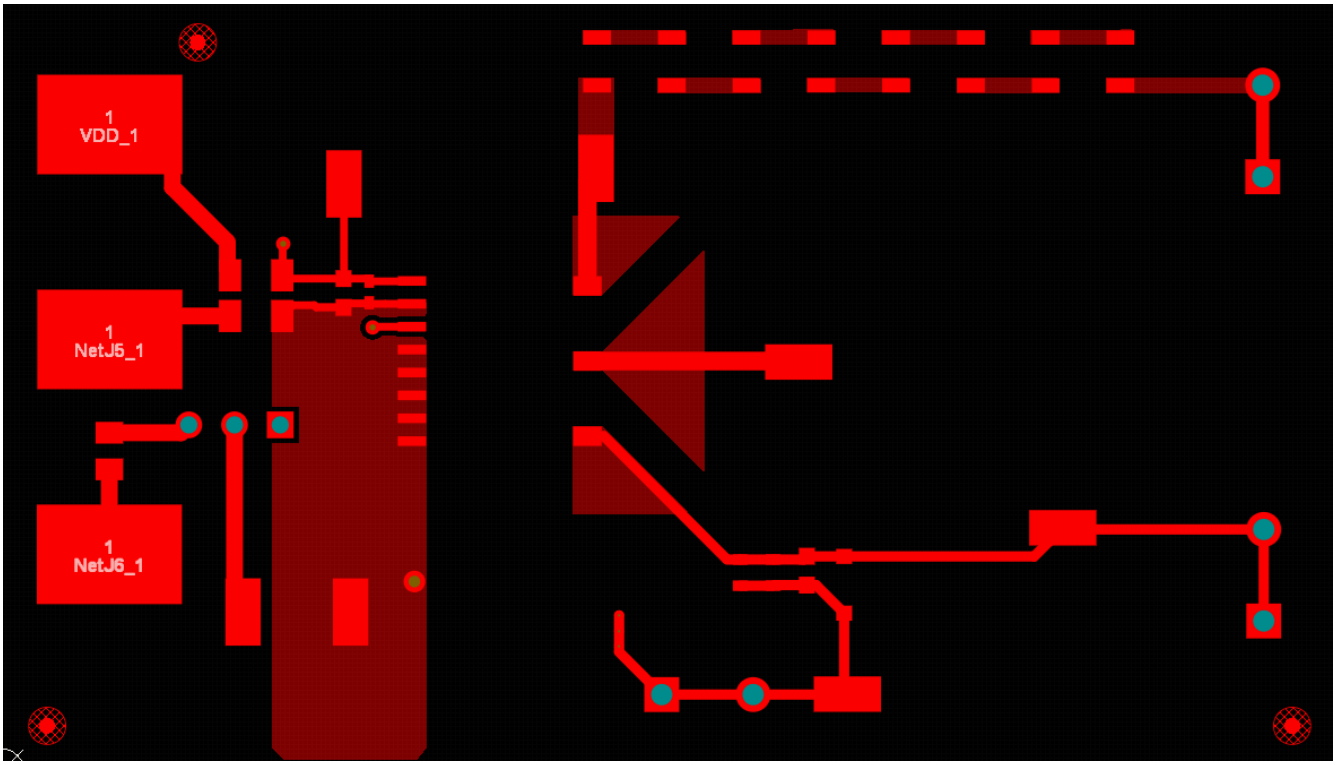

图 9-13. TPSI2140-Q1 EVM - Layer 1

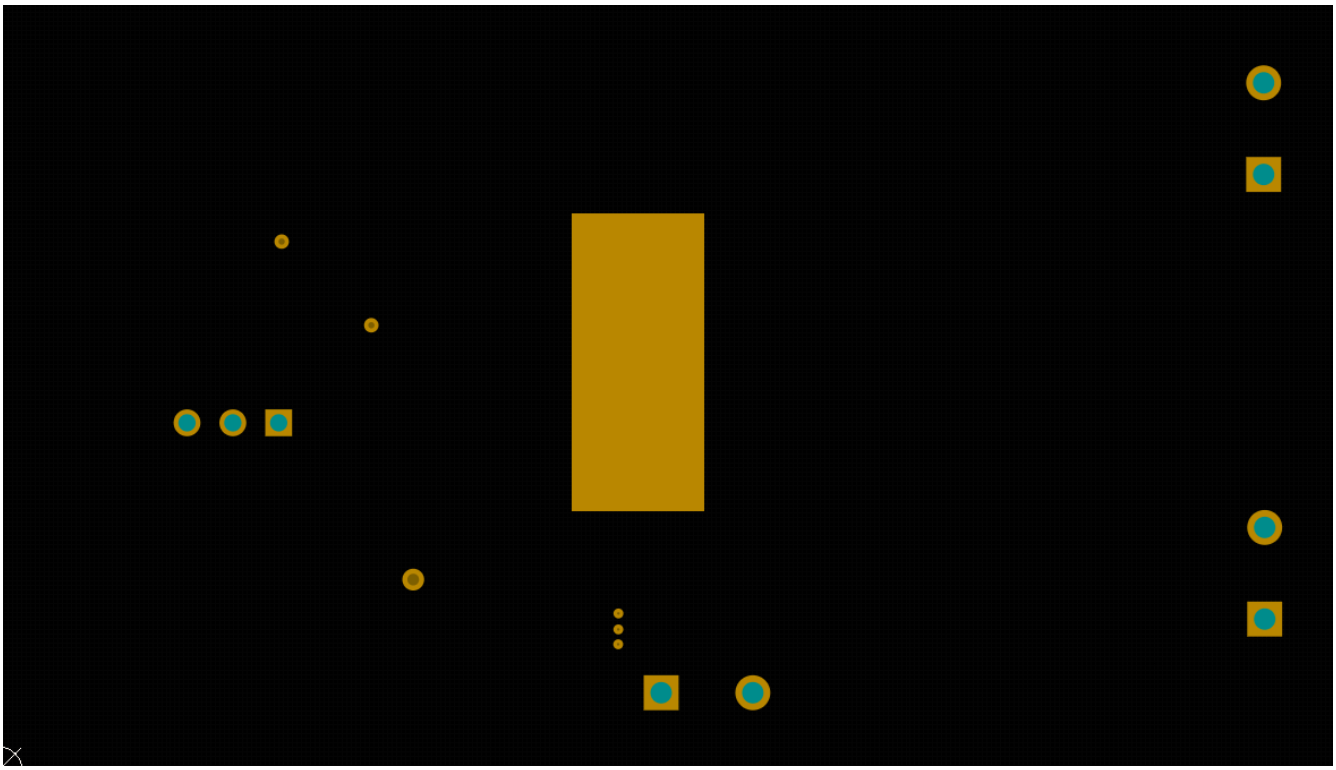

图 9-14. TPSI2140-Q1 EVM - Layer 2

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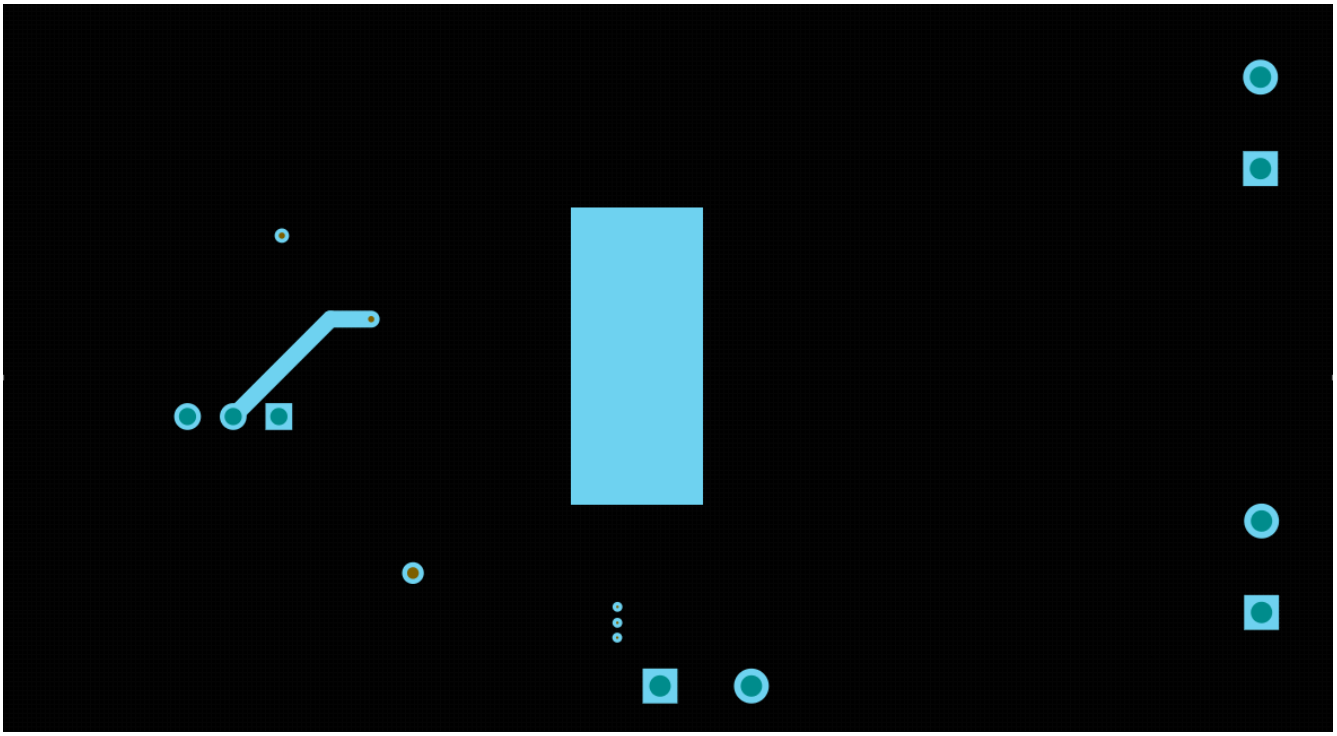

图 9-15. TPSI2140-Q1 EVM - Layer 3

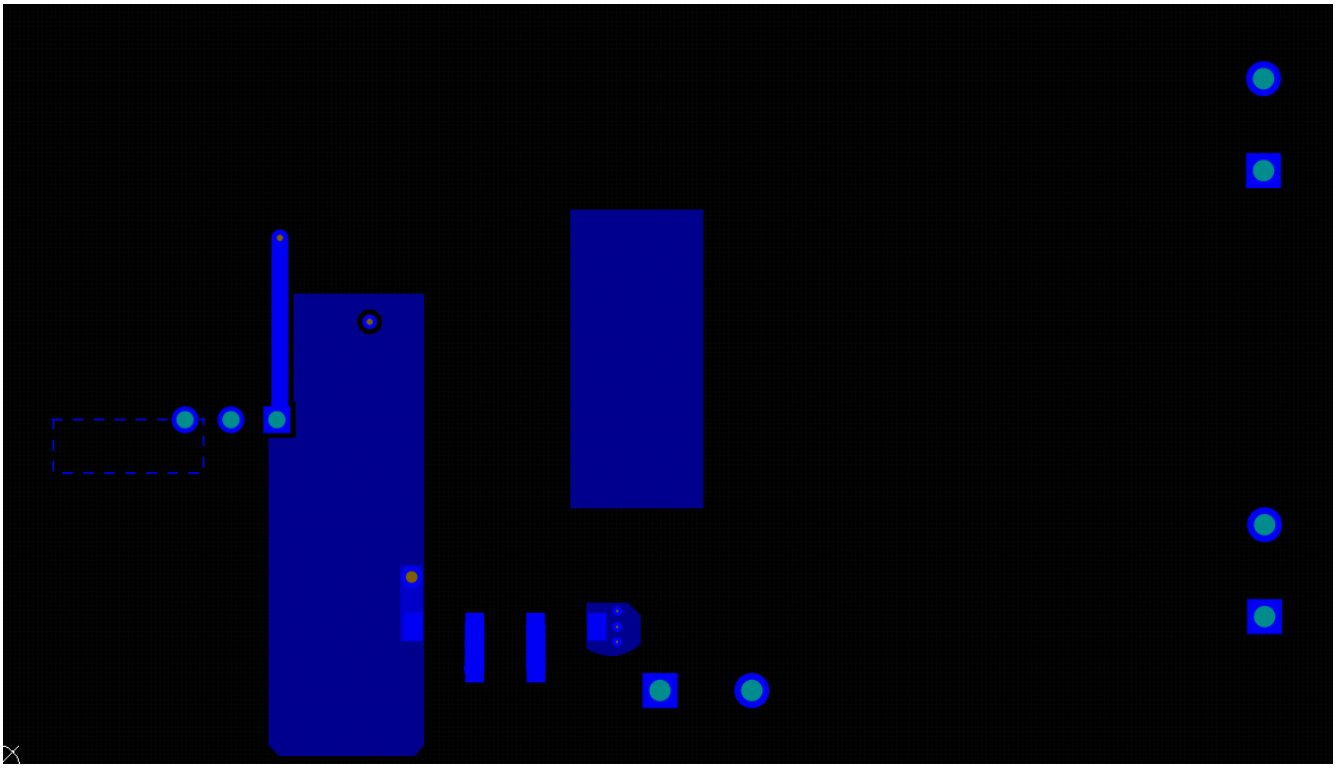

图 9-16. TPSI2140-Q1 EVM - Layer 4

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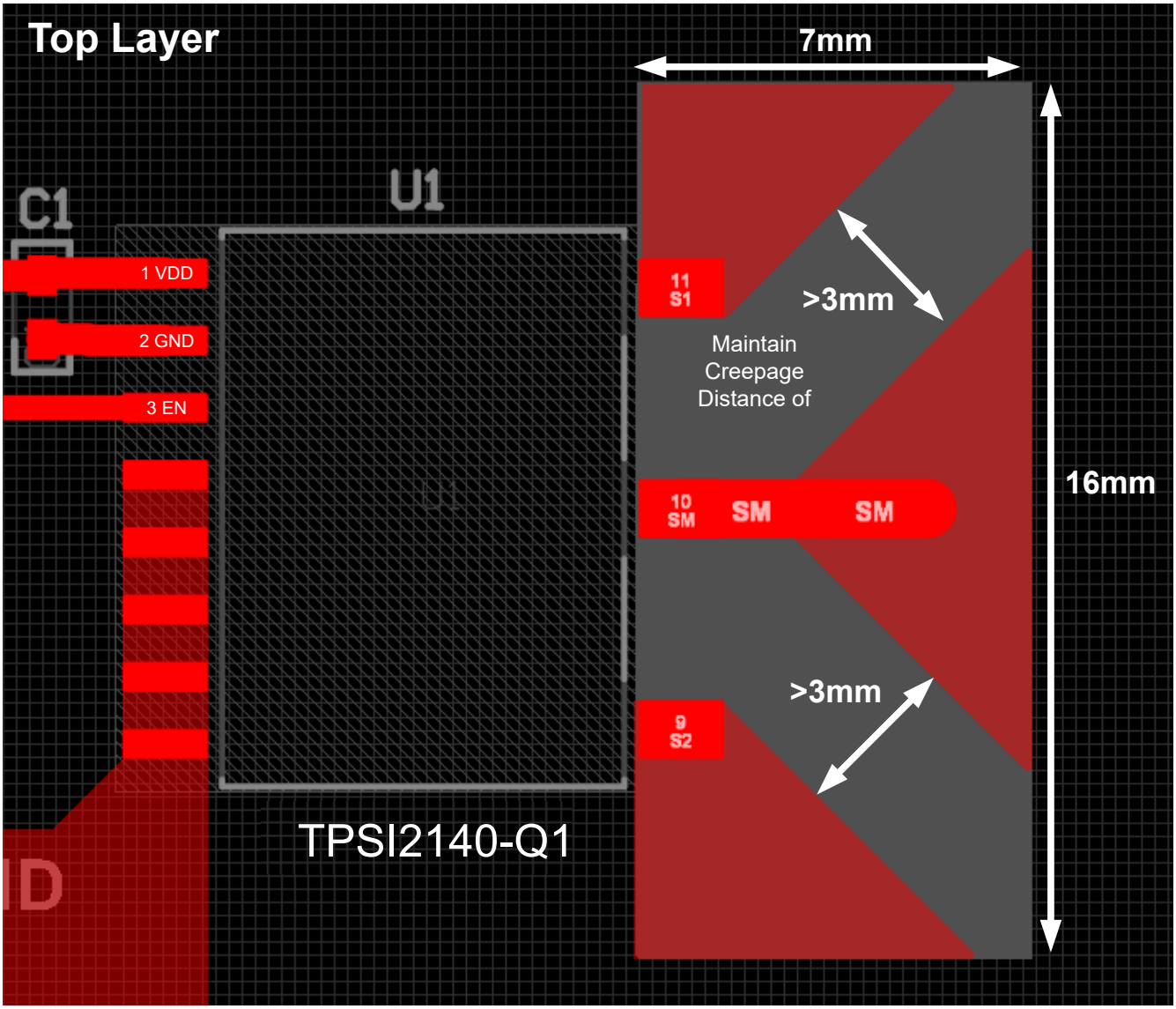

图 9-17. TPSI2140-Q1 Secondary Side Layout Recommendation for Optimized Thermal Performance: Top Layer 1

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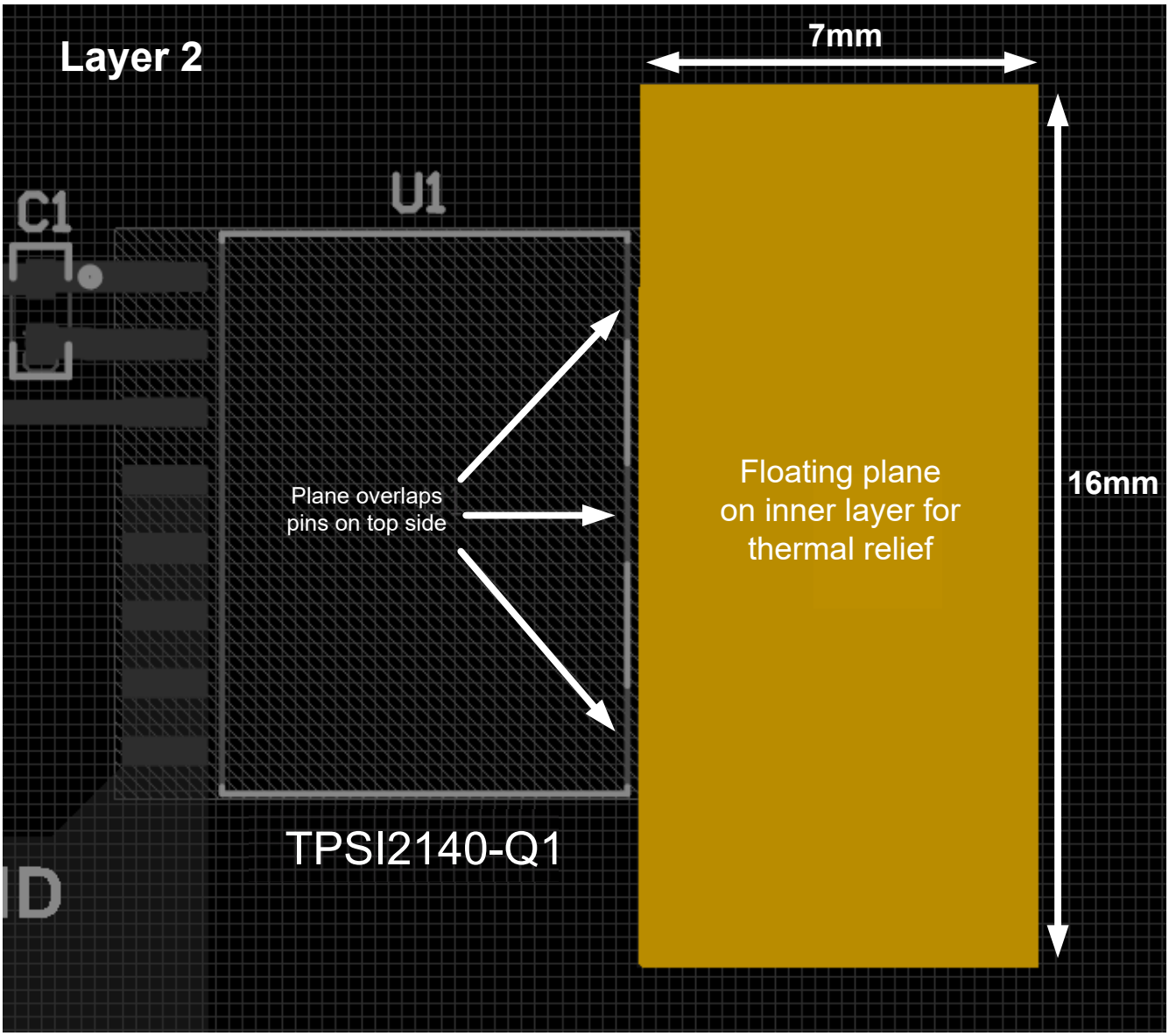

图 9-18. TPSI2140-Q1 Secondary Side Layout Recommendation for Optimized Thermal Performance: Inner Layer 2

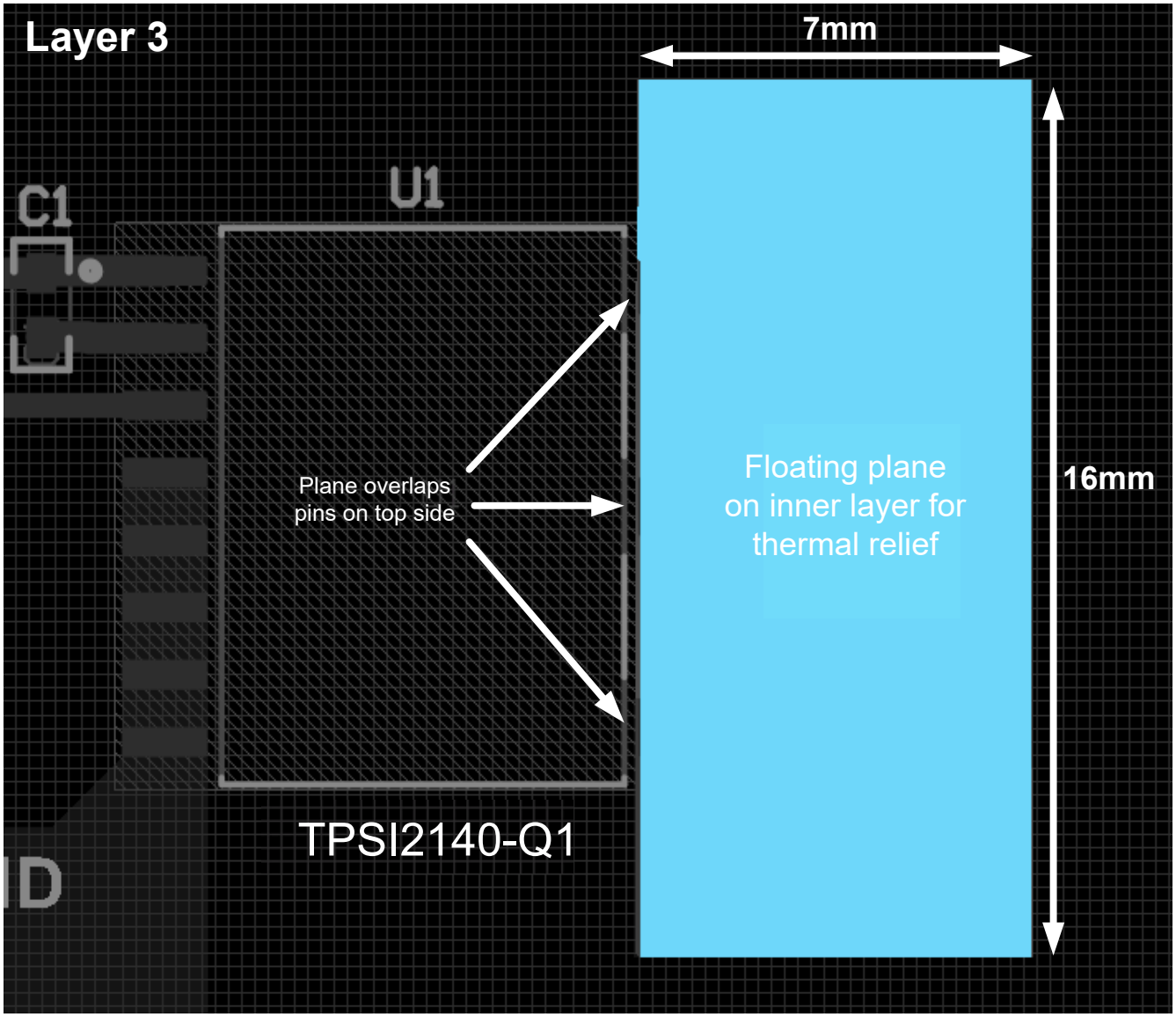

图 9-19. TPSI2140-Q1 Secondary Side Layout Recommendation for Optimized Thermal Performance: Inner Layer 3

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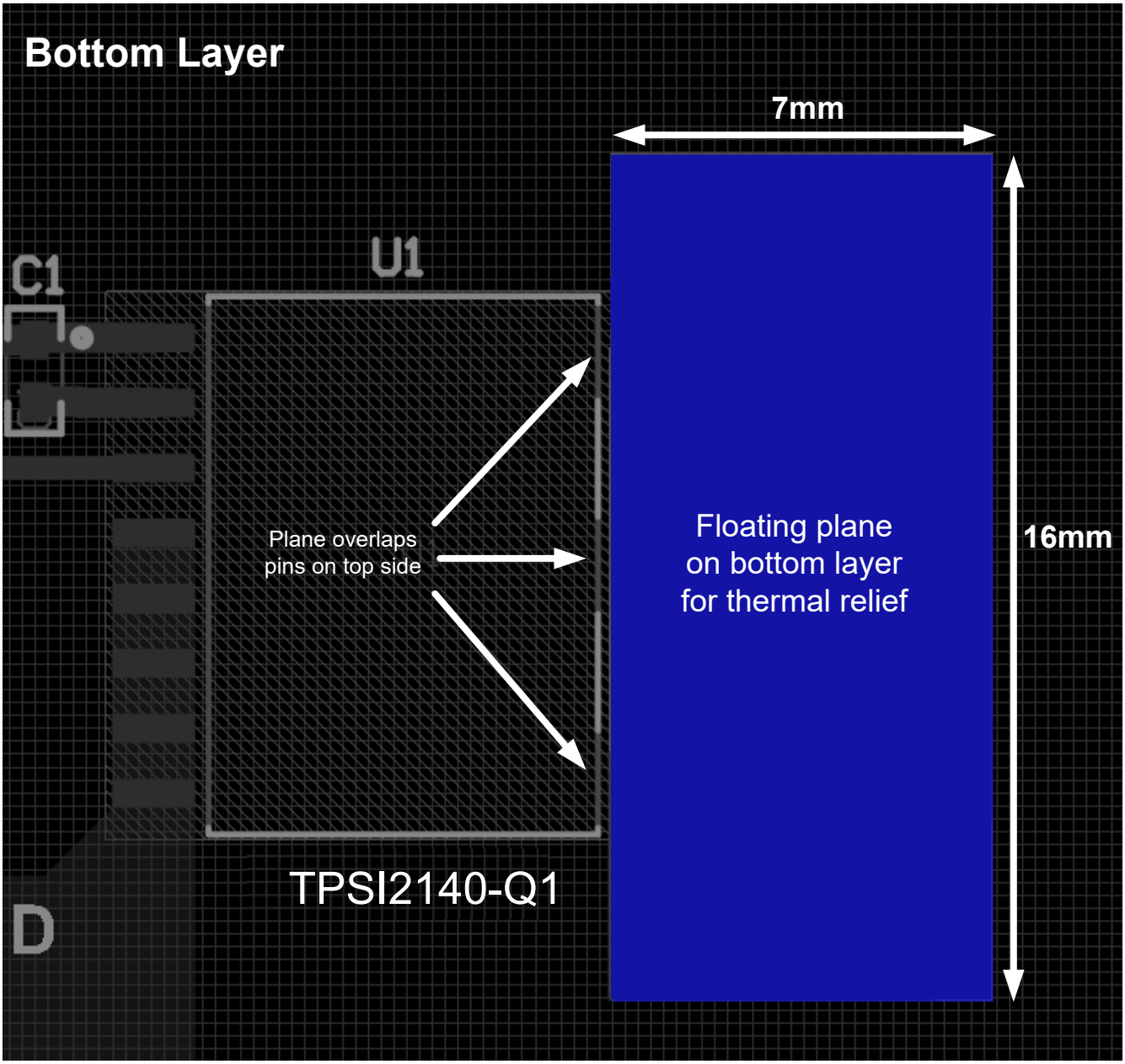

图 9-20. TPSI2140-Q1 Secondary Side Layout Recommendation for Optimized Thermal Performance: Bottom Layer 4

Interlayer Stitch Capacitance Option for EMI and Thermal Optimization

The layout example below demonstrates an EMI optimized and thermally optimized PCB Design for high voltage switching applications. The overlapping metal layers beneath the TPSI2140-Q1 form an interlayer stitching capacitance between the primary side ground and the S2 pin and increase the board copper content, improving the thermal performance for dielectric withstand testing (HiPot). Using S1 or S2 as the secondary side interlayer stitching capacitance terminal is equally effective. Metal islands on the S1 and S2 pin on the top side and inner layers further improve the thermal performance. Care should be taken to maintain both the vertical and horizontal interlayer dielectric (ILD) spacings between high voltage terminals required by the system.

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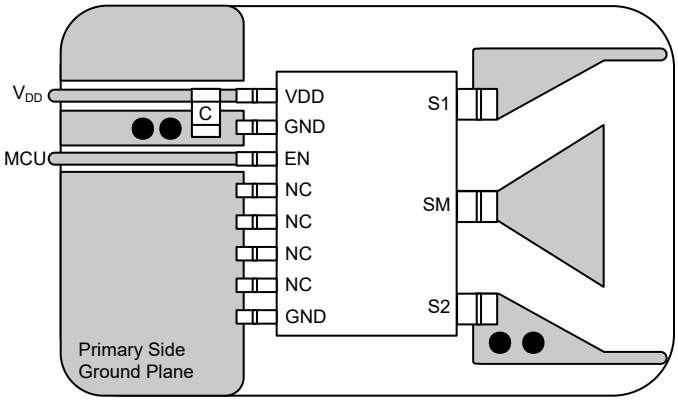

图 9-21. TPSI2140-Q1 Layout with Interlayer Stitch Capacitance: Top Layer (1)

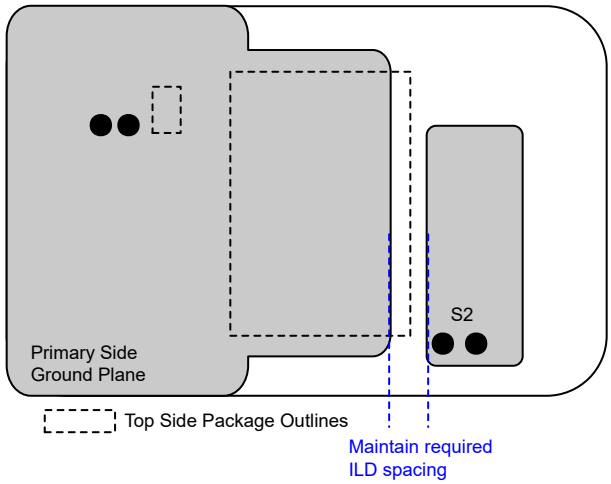

图 9-22. TPSI2140-Q1 Layout with Interlayer Stitch Capacitance: Inner Layer (2,4)

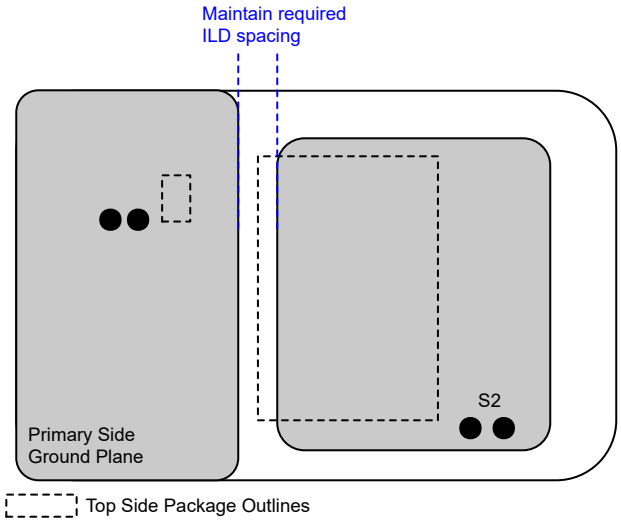

图 9-23. TPSI2140-Q1 Layout with Interlayer Stitch Capacitance: Inner Layer (3)

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10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.3 Trademarks

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10.4 静电放电警告

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPSI2140QDWQRQ1	Active	Production	SOIC (DWQ) | 11	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	2140Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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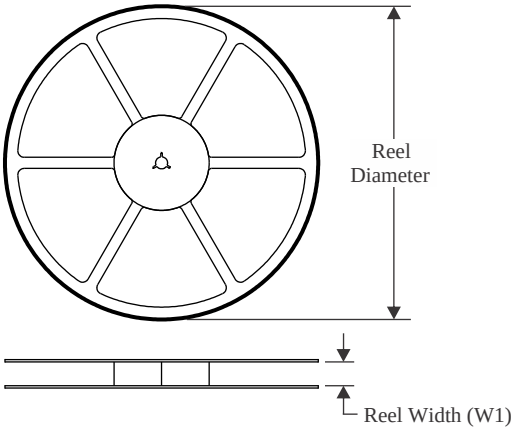
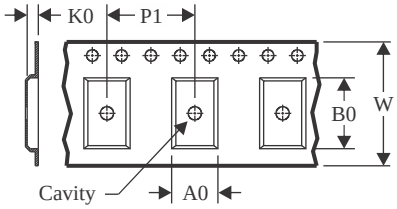
TAPE AND REEL INFORMATION

REEL DIMENSIONS

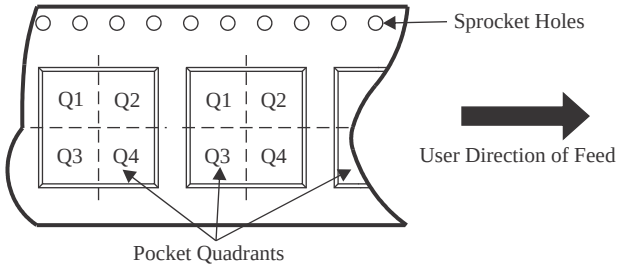


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

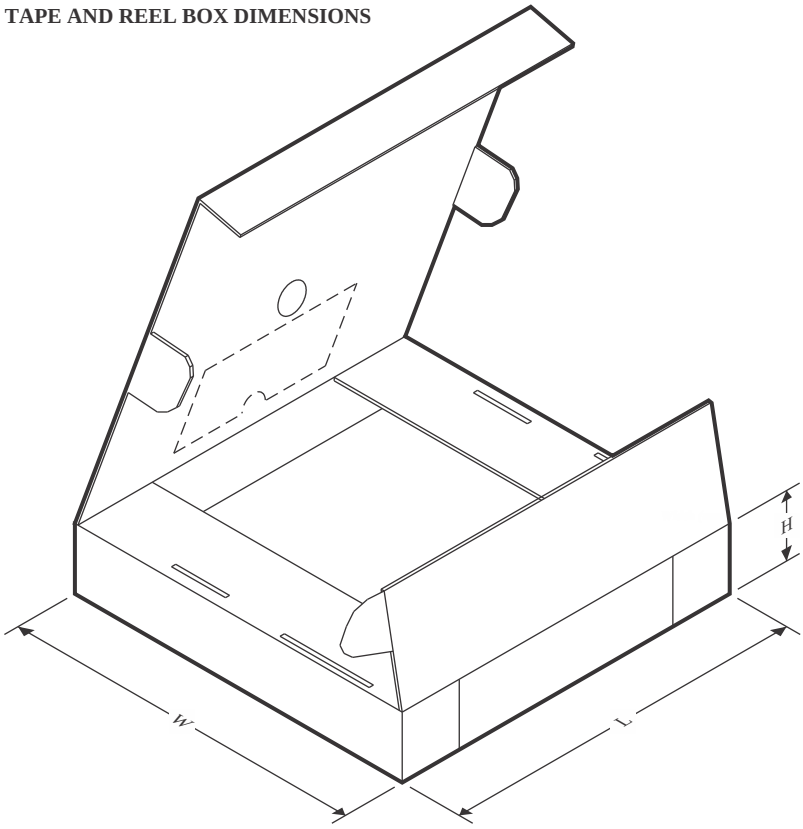
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSI2140QDWQRQ1	SOIC	DWQ	11	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

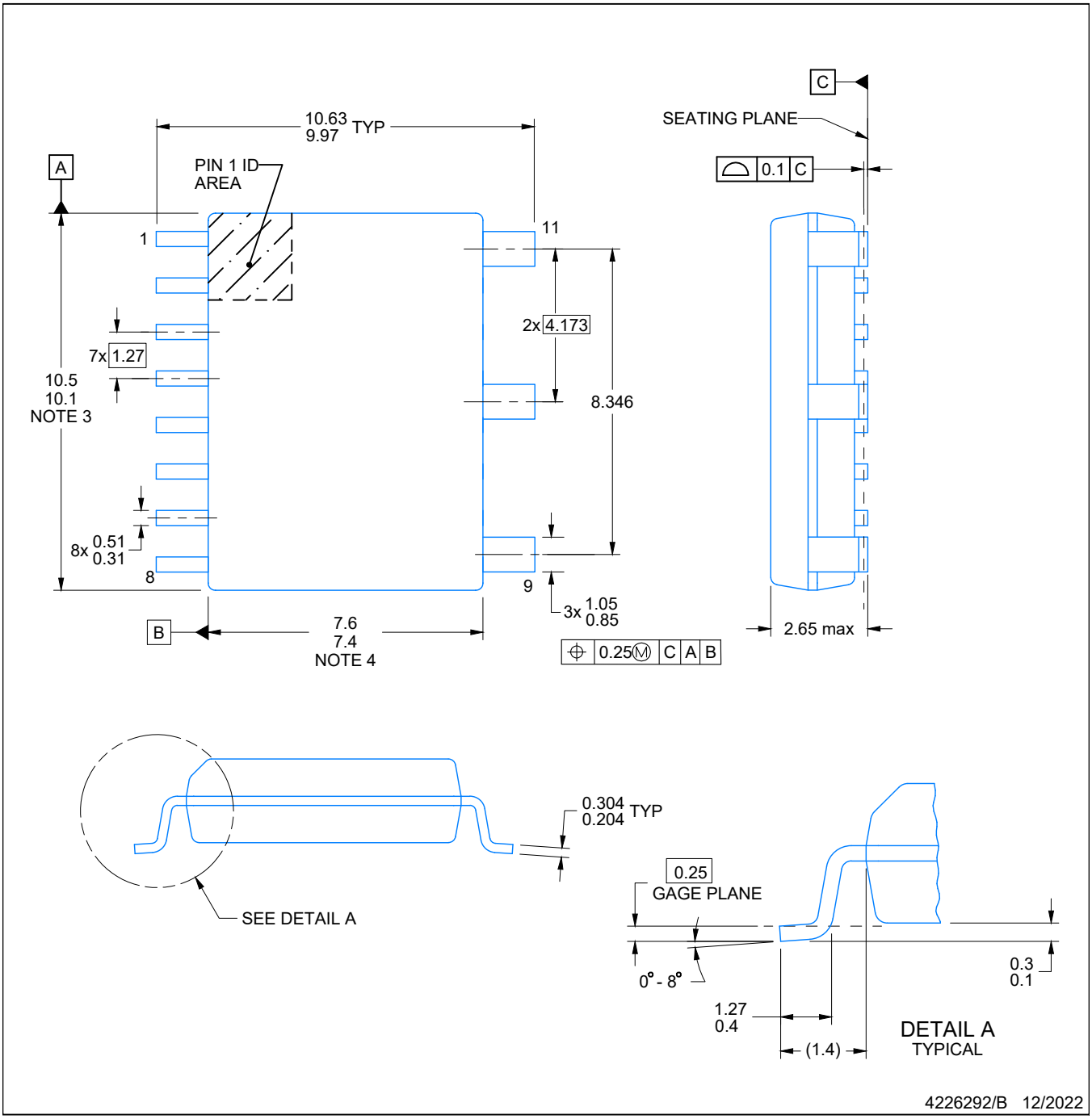
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSI2140QDWQRQ1	SOIC	DWQ	11	2000	350.0	350.0	43.0

PACKAGE OUTLINE

DWQ0011A

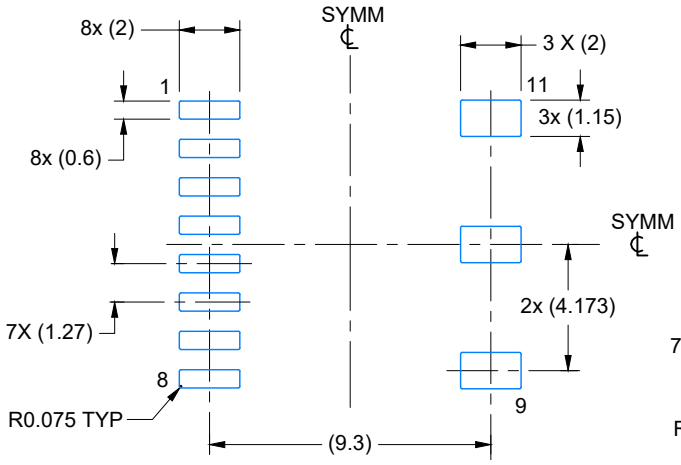
SOIC - 2.65 mm max height

SMALL OUTLINE PACKAGE

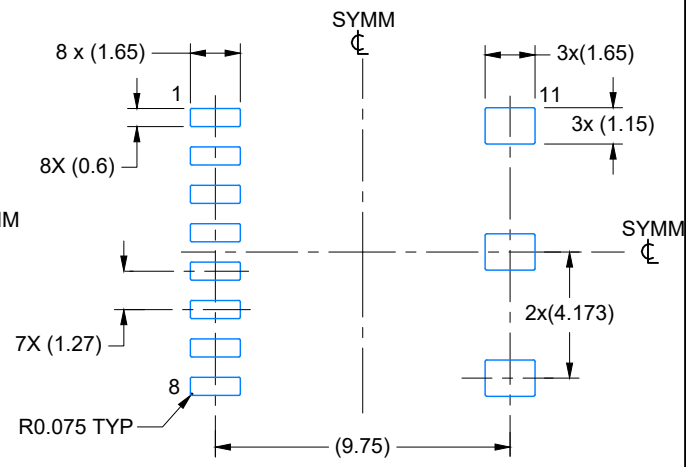


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

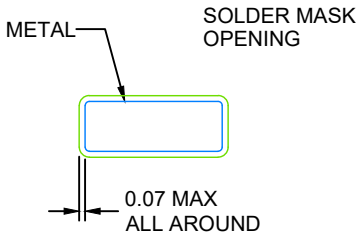


IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

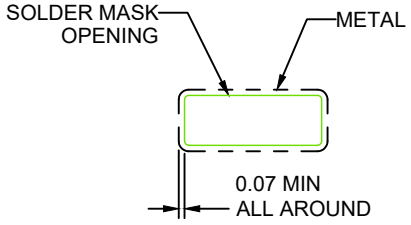


HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK
DEFINED



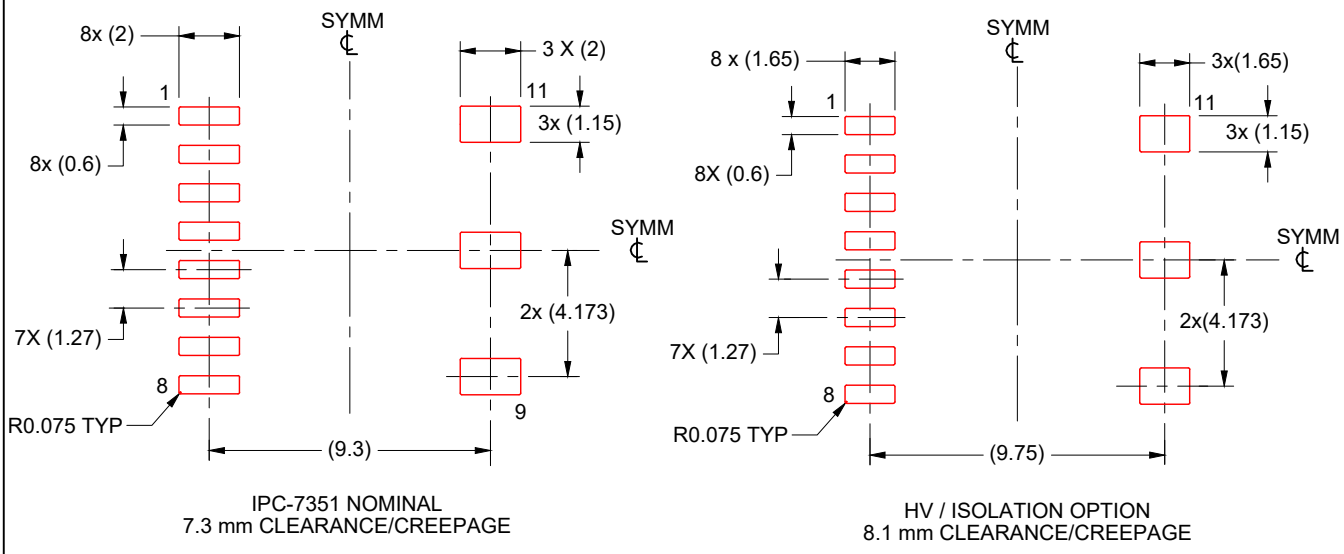
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4226292/B 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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