带有集成型发光二级管 (LED) 温度折返的用于高亮度 LED 的 1.5A 恒流降压转换器

查询样品: TPS92510

特性

- **3.5V** 至 **60V** 输入电压范围
- 集成型 **200mΩ** 高侧金属氧化物半导体场效应晶体管 **(MOSFET)**
- **200mV** 内部电压基准
- **±3% LED** 电流精度
- **100kHz** 至 **2.5MHz** 开关频率范围
- 专用脉宽调制 **(PWM)** 亮度调节输入
- **LED** 温度折返
- 可调节欠压闭锁 **(UVLO)**
- 过流保护
- 过温保护
- 微型小外形尺寸封装 **(MSOP)-10 (DGQ) PowerPAD™** 封装

应用范围

- 街道照明
- 紧急照明
- 通用照明
- 工业用和商用照明
- **MR16 LED** 灯泡

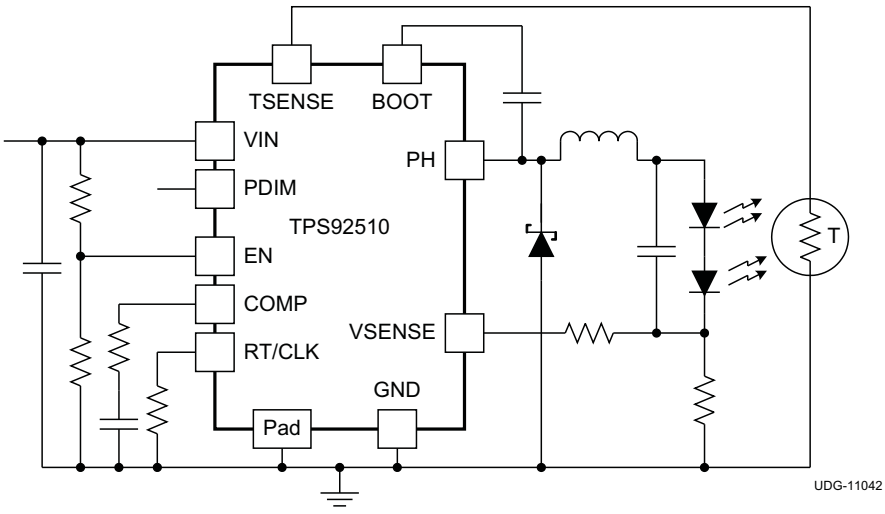
说明

TPS92510 是一款配有集成型高侧 MOSFET 的 60V，1.5A 峰值电流模式降压转换器。 它被专门设计成用一个恒定电流驱动高亮度 LED。 紧密度容限，200mV 内部基准电压减少了电流感测电阻器中的功率耗散。 一个专用的脉宽调制输入引脚可实现对光输出的线性控制。

TPS92510 集成了一个温度折返特性，此特性能够减少平均输出电流来保证感测到的 LED 温度永远不会超过一个特定的值，从而提升了整个系统的可靠性。 一个集成的频率同步特性可减少多串应用中的有害差频并简化对电磁干扰 (EMI) 的滤除。 可调输入电压 UVLO 特性可适应多种电池类型的不同的深度放电水平。

TPS92510 支持逐周期过流保护，和热关断保护。 它采用一个 10 引脚 MSOP PowerPAD™ 封装。

简化的应用



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_J	PACKAGE	PINS	OUTPUT SUPPLY	MINIMUM QUANTITY	ORDERABLE DEVICE NUMBER
–40°C to 150°C	PowerPAD Plastic Small Outline (MSOP)	10	Tube	80	TPS92510DGQ
			Tape and Reel	2500	TPS92510DGQR

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating temperature range (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Input voltage	VIN	–0.3	65	V
	PDIM, EN	–0.3	6	
	BOOT		73	
	VSENSE, TSENSE, COMP	–0.3	3	
	RT/CLK	–0.3	3.6	
Output voltage	BOOT-PH		8	V
	PH	–0.6	65	
	PH, 10-ns Transient	–2	65	
Voltage Difference	PAD to GND		±200	mV
Source current	EN		100	µA
	BOOT		100	mA
	VSENSE		10	µA
	PH		Current Limit	A
	RT/CLK		100	µA
Sink current	VIN		Current Limit	A
	COMP, VSENSE, EN		100	µA
Electrostatic Discharge (HBM) QSS 009-105 (JESD22-A114A)			2	kV
Electrostatic Discharge (CDM) QSS 009-147 (JESD22-C101B.01)			500	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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THERMAL INFORMATION

THERMAL METRIC(1)		TPS92510 MSOP 10 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	66.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	45.8	
θ_{JB}	Junction-to-board thermal resistance(4)	37.5	
ψ_{JT}	Junction-to-top characterization parameter(5)	1.8	
ψ_{JB}	Junction-to-board characterization parameter(6)	37.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	15.4	

(1) 有关传统和全新热度量的更多信息，请参阅 *IC 封装热度量* 应用报告 （文献号：SPRA953）。
(2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的规定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然对流条件下的结至环境热阻抗。
(3) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。 不存在特定的 JEDEC 标准测试，但可在 ANSI SEMI 标准 G30-88 中找到内容接近的说明。
(4) 按照 JESD51-8 中的说明，通过在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结至电路板的热阻。
(5) 结至顶部的特征参数，(ψ_{JT})，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中描述的程序从仿真数据中提取出该参数以便获得 θ_{JA}。
(6) 结至电路板的特征参数，(ψ_{JB})，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第7 章）中描述的程序从仿真数据中提取出该参数以便获得 θ_{JA}。
(7) 通过在外露（电源）焊盘上进行冷板测试仿真来获得结至芯片外壳（底部）热阻。 不存在特定的 JEDEC 标准测试，但可在 ANSI SEMI 标准 G30-88 中找到了内容接近的说明。

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	PWM dimming input frequency	120		1000	Hz
	PWM dimming minimum on-time	10			µs
V_{VIN}	Input voltage	3.5		60	V
$t_{ON(min)}$	High-side MOSFET on-time	350			ns
$I_{L(pk-pk)}$	Peak-to-peak inductor current	150			mA
T_J	Operating junction temperature	–40		125	°C

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ELECTRICAL CHARACTERISTICS

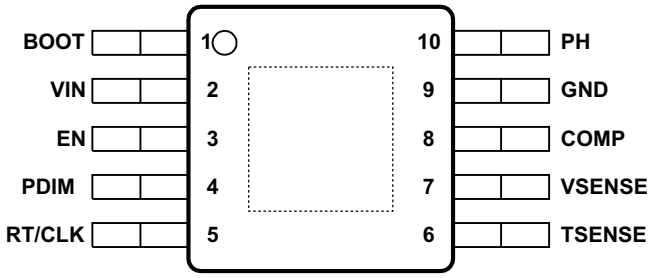
–40°C ≤ T_J ≤ 125°C, V_{VIN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
V_{VIN}	Input voltage		3.5		60	V
V_{UVLO}	Internal undervoltage lockout threshold	No voltage hysteresis, rising and falling		2.5		V
I_{VINSD}	Shutdown supply current	V_{EN} = 0 V, T_A=25°C, 3.5 V ≤ V_{VIN} ≤ 60 V		1.3	4	µA
I_{VIN}	Non-switching supply current	V_{VSENSE} = 210 mV, T_A=25°C		305	400	
ENABLE AND UVLO (EN PIN)						
V_{EN}	Enable threshold voltage	No voltage hysteresis, rising and falling, 25°C	1.135	1.250	1.345	V
	Input current	VREF threshold +50 mV		–3.8		µA
		VREF threshold –50 mV		–0.9		
	Hysteresis current			–2.9		µA
VOLTAGE REFERENCE						
VREF	Voltage reference	3.5 ≤ V_{VIN} ≤ 60 V, T_J = 25°C	194	200	206	mV
		3.5 ≤ V_{VIN} ≤ 60 V, -40°C ≤ T_J ≤ 125°C	190		210	
HIGH-SIDE MOSFET						
$R_{DS(on)}$	On-resistance	V_{VIN} = 3.5 V, (V_{BOOT}– V_{PH}) = 3 V		300		mΩ
		V_{VIN} = 12 V, (V_{BOOT}– V_{PH}) = 6 V		200	410	
ERROR AMPLIFIER						
	Input current			50		nA
$g_{M(ea)}$	Error amplifier transconductance gain	–2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V		310		µA/V
	Error amplifier dc gain	V_{VSENSE} = 0.2 V		10		kV/V
	Error amplifier bandwidth			2.7		MHz
	Error amplifier source/sink	V_{COMP} = 1 V, 100 mV overdrive		±27		µA
	COMP to switch current transconductance			10.5		A/V
CURRENT LIMIT						
	Current limit threshold	T_J = 25°C	2.5	4.0		A
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown			150		°C
	Thermal shutdown hysteresis			20		°C
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)						
f_{SW}	Switching frequency range using RT mode		100		2500	kHz
f_{SW}	Switching frequency	R_{RT} = 200 kΩ	450	581	720	kHz
	Switching frequency range using CLK mode		300		2200	kHz
	Minimum CLK input pulse width			40		ns
	RT/CLK high threshold			1.9	2.2	V
	RT/CLK low threshold		0.5	0.7		V
	RT/CLK falling edge to PH rising edge delay	Measured at 500 kHz with RT resistor in series		60		ns
	Phase loop (PLL) lock-in time	f_{SW} = 500 kHz		100		µs
PWM DIMMING (PDIM)						
V_{IH}	High-level input voltage			1.35	1.55	V
V_{IL}	Low-level input voltage		0.75	0.90		V
THERMAL FOLDBACK PROTECTION (TSENSE)						
	PWM ramp valley voltage		0	100	250	mV
	PWM ramp peak voltage		1.75	1.95	2.15	V
	PWM frequency		3.5	6.0	8.5	kHz
	Current source		70	95	125	µA

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DEVICE INFORMATION

TPS92510
MSOP-10
(Top View)

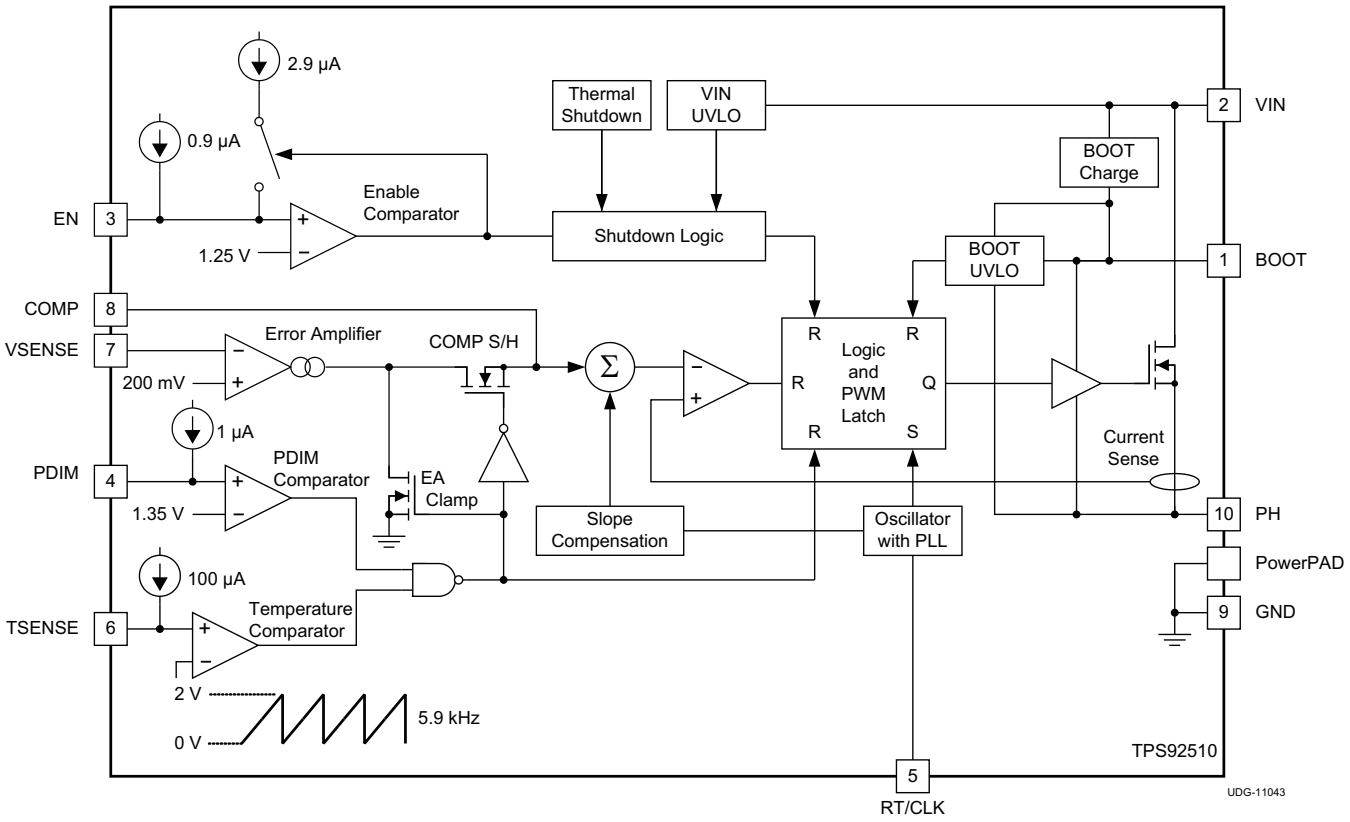


PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	O	A bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor is below the minimum required by the output device, the output is forced to switch off until the capacitor is refreshed.
COMP	8	O	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin.
EN	3	I	Enable pin, internal pull-up current source. Pull below 1.2-V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors.
GND	9	–	Ground
PDIM	4	I	PWM dimming input pin. The duty cycle of the PWM signal linearly controls the average current output of the converter.
PH	10	O	The source of the internal high-side MOSFET.
PowerPAD	Pad	–	GND pin must be electrically connected to the exposed pad on the printed circuit board for proper operation.
RT/CLK	5	I	Resistor timing and external clock. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to program the switching frequency. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin becomes a high impedance clock input to the internal PLL. If the clocking edges stop, the internal amplifier is re-enabled and the mode returns to the resistor-programmed function.
TSENSE	6	I	Temperature fold-back pin. An NTC thermistor connected from this pin to ground provides a thermal feedback to decrease the average LED current as the sensed LED temperature increases. It is recommended to bypass this pin with a capacitor with a value of 0.01 µF (or larger) to GND.
VIN	2	I	Input supply voltage, 3.5 V to 60 V.
VSENSE	7	I	Inverting node of the transconductance (g_M) error amplifier.

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FUNCTIONAL BLOCK DIAGRAM



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TYPICAL CHARACTERISTICS

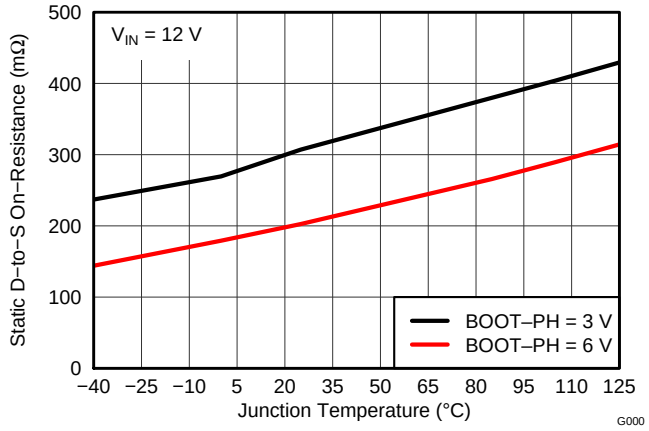


Figure 1. On-Resistance vs. Junction Temperature

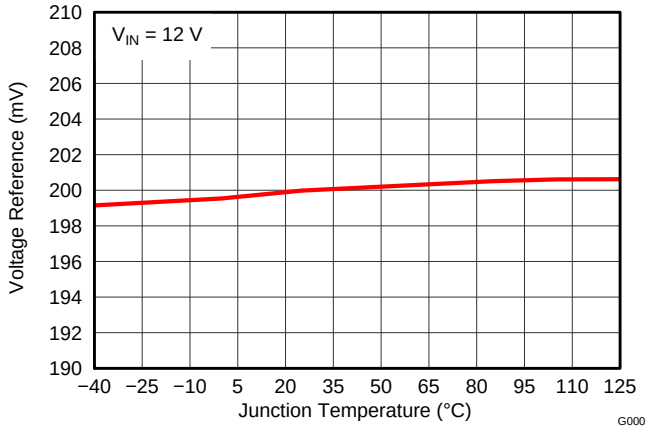


Figure 2. Reference Voltage vs. Junction Temperature

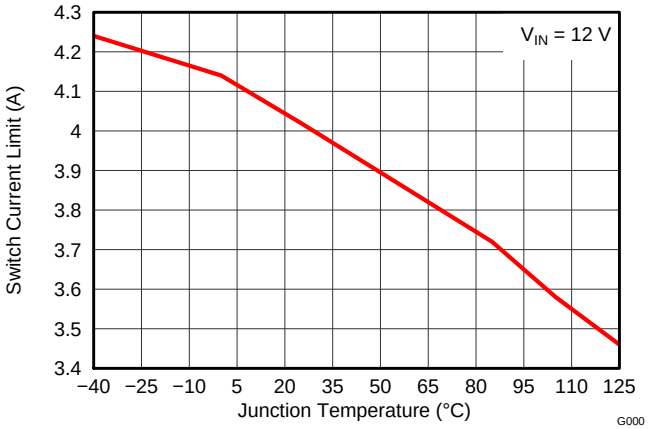


Figure 3. Switch Current vs. Junction Temperature

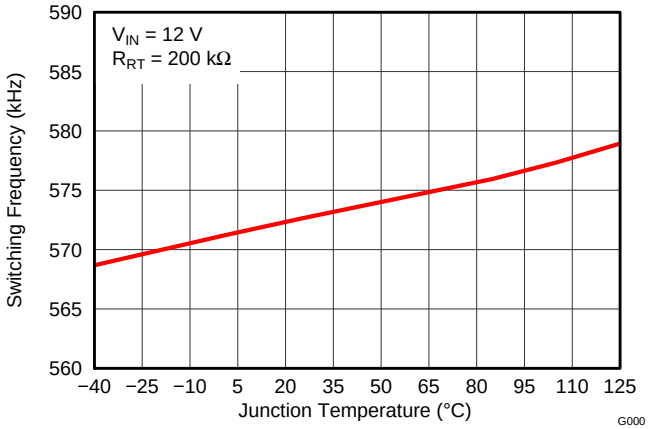


Figure 4. Switching Frequency vs. Junction Temperature

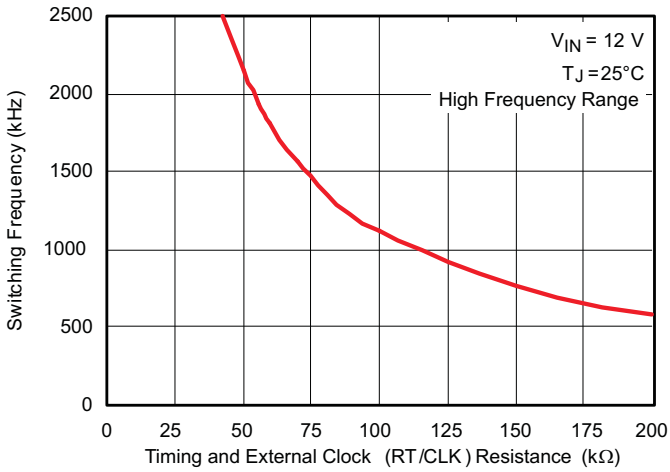


Figure 5. Switching Frequency vs. RT/CLK Resistance

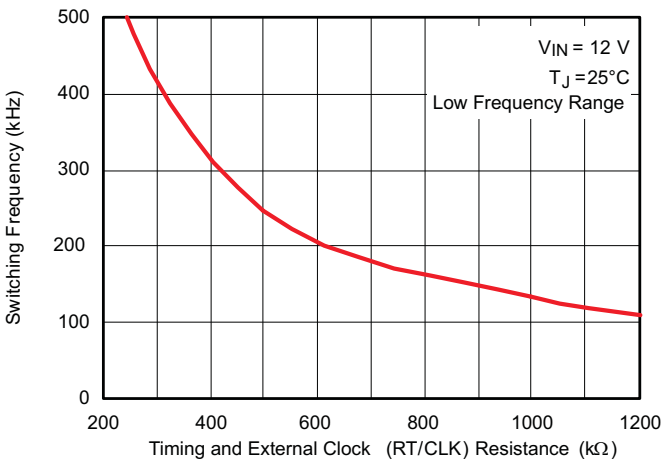


Figure 6. Switching Frequency vs. RT/CLK Resistance

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TYPICAL CHARACTERISTICS (continued)

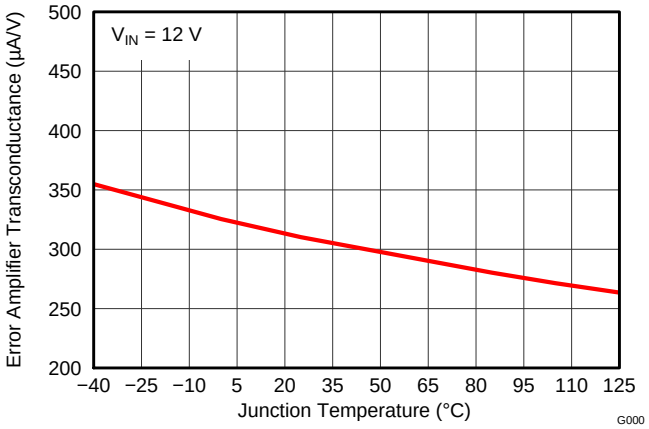


Figure 7. Error Amplifier Transconductance vs. Junction Temperature

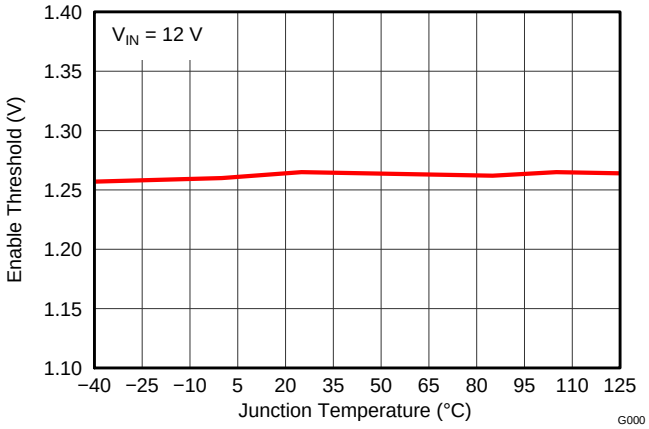


Figure 8. Enable Voltage vs. Junction Temperature

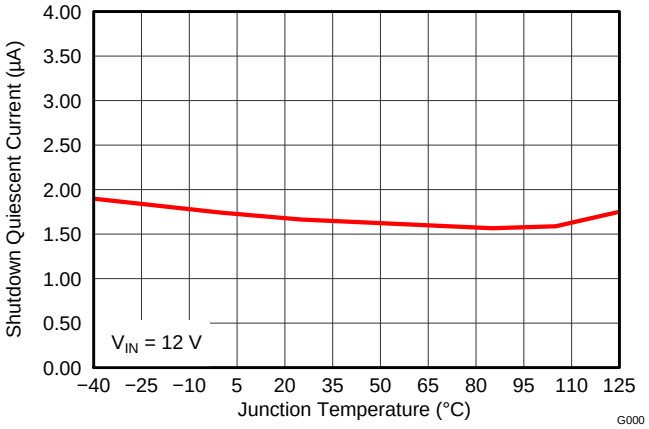


Figure 9. Shutdown Quiescent Current vs. Junction Temperature

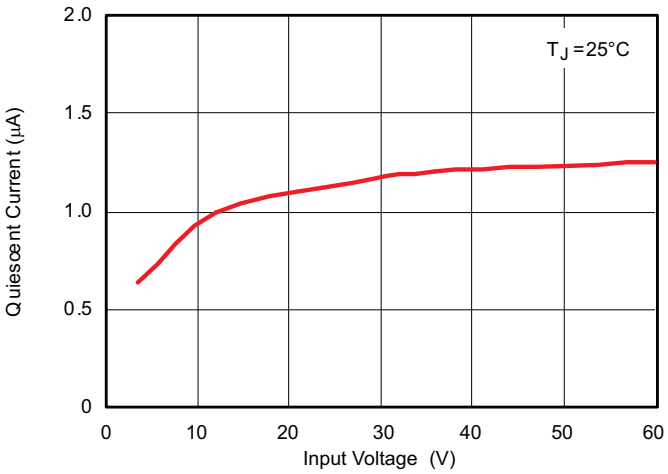


Figure 10. Shutdown Quiescent Current vs. Input Voltage

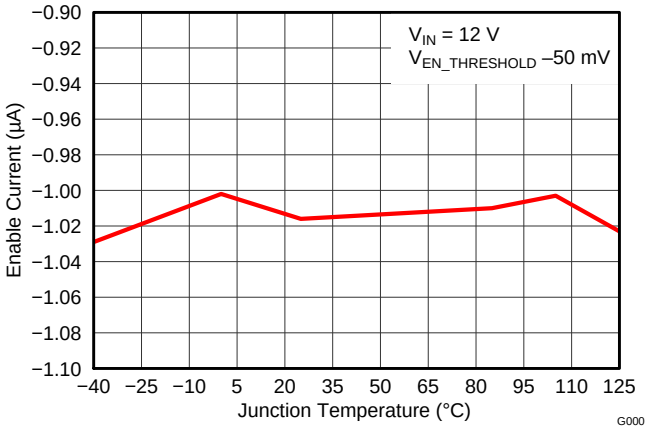


Figure 11. Enable Current vs. Junction Temperature

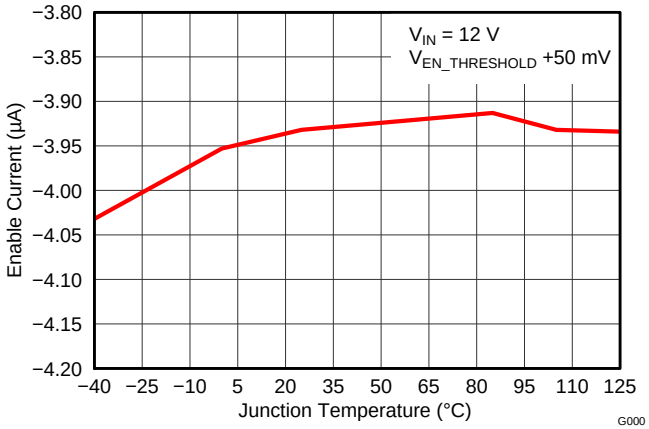


Figure 12. Enable Current vs. Junction Temperature

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TYPICAL CHARACTERISTICS (continued)

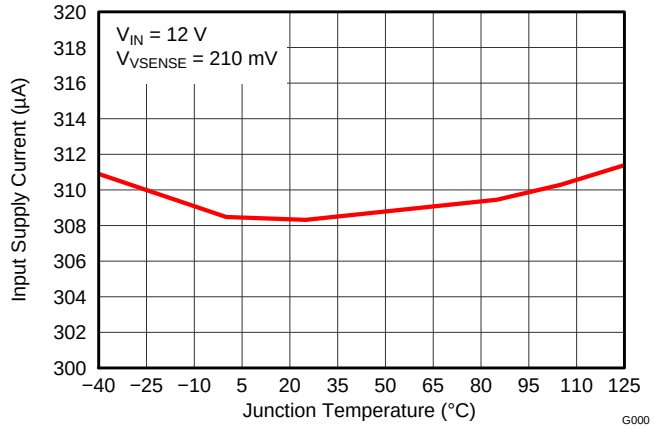


Figure 13. Input Supply Current vs. Junction Temperature

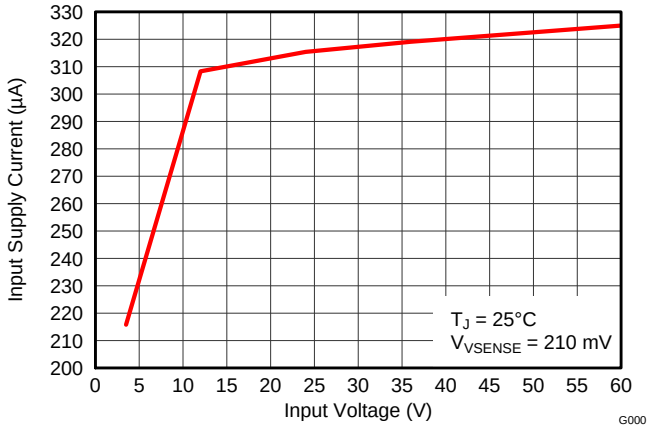


Figure 14. Input Supply Current vs. Input Voltage

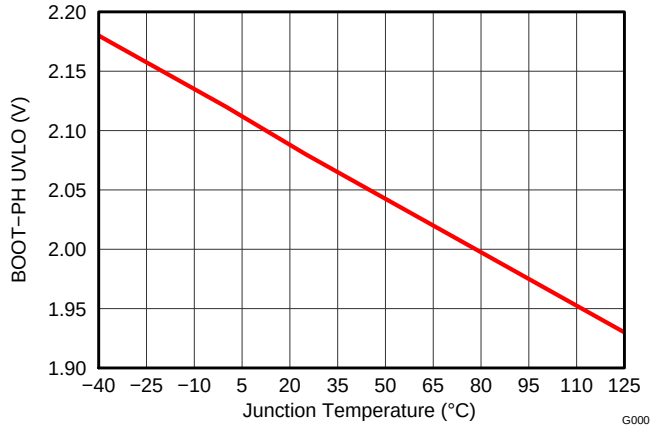


Figure 15. BOOT-PH UVLO vs. Junction Temperature

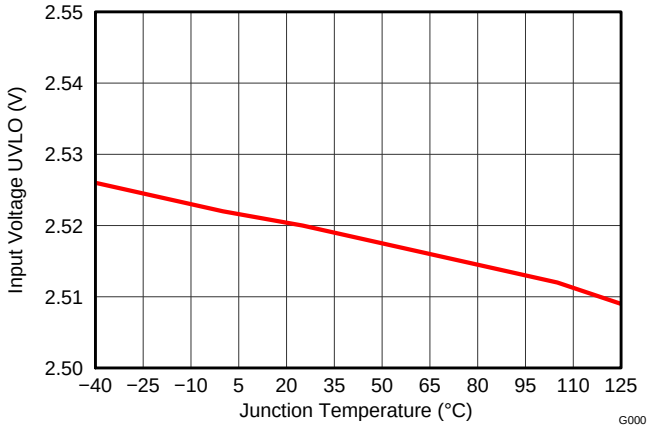


Figure 16. Input Voltage UVLO vs. Junction Temperature

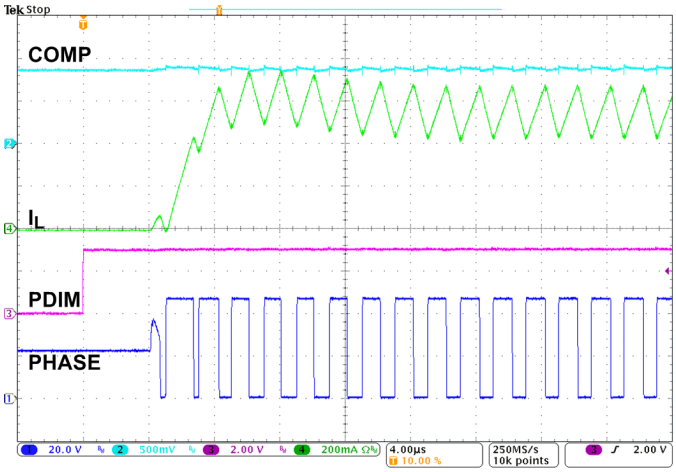


Figure 17. PDIM Rising

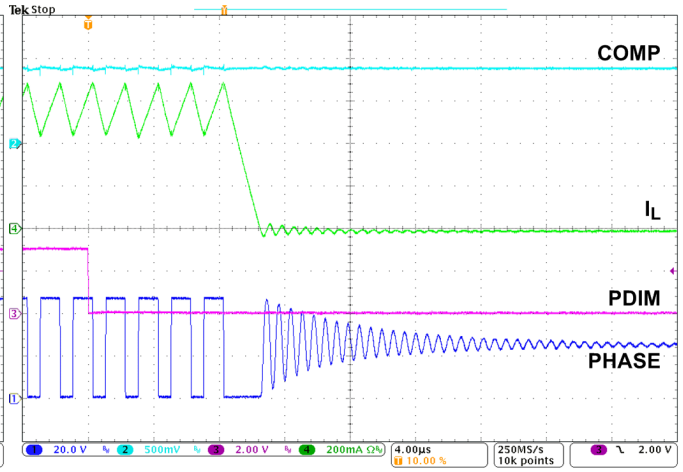
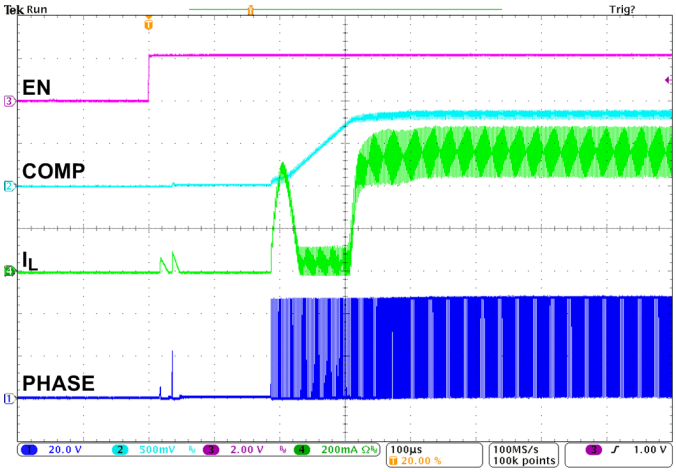


Figure 18. PDIM Falling

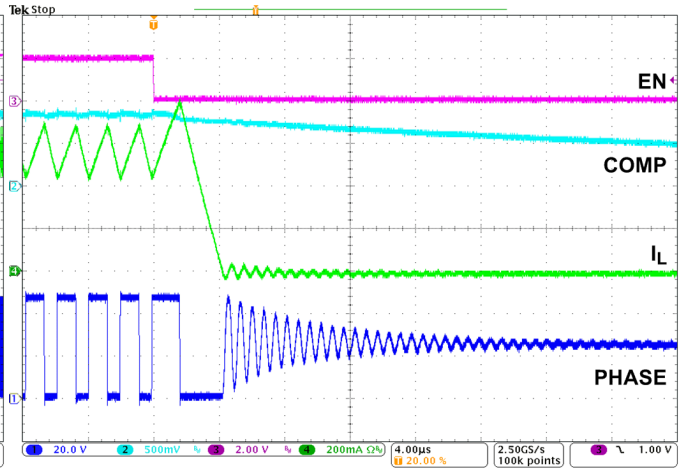
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TYPICAL CHARACTERISTICS (continued)



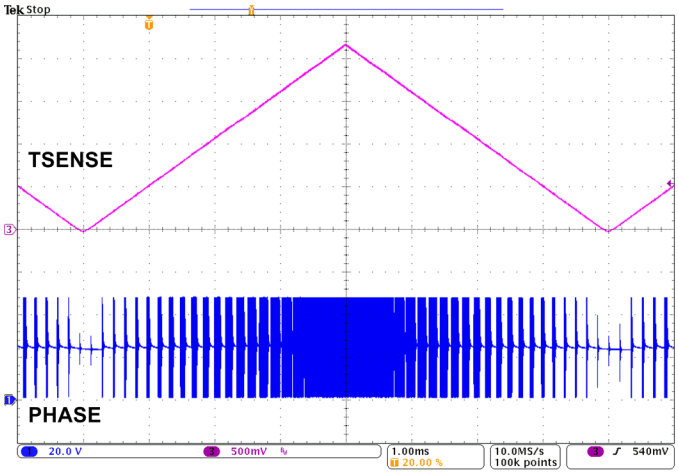
Time

Figure 19. Enable Rising



Time

Figure 20. Enable Falling



Time

Figure 21. TSENSE and High-Side MOSFET

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OVERVIEW

The TPS92510 is a 60-V, 1.5-A, step-down (buck) regulator with an integrated high-side N-channel MOSFET. To improve performance during line and load transients the device implements a constant frequency, peak-current mode control which reduces output capacitance and simplifies external frequency compensation design. The wide switching frequency of 100 kHz to 2500 kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground on the RT/CLK pin. The device has an internal phase lock loop (PLL) on the RT/CLK pin that is used to synchronize the power switch turn on to a falling edge of an external system clock.

The TPS92510 has a default start up voltage of approximately 2.5 V. The EN pin has an internal pull-up current source that can be used to adjust the input voltage under voltage lockout (UVLO) threshold with two external resistors. In addition, the pull up current provides a default condition. When the EN pin is floating the device operates. The operating current is 138 µA when not switching and under no load. When the device is disabled, the supply current is 1.3 µA.

The integrated 200 mΩ high-side MOSFET allows for high efficiency power supply designs capable of delivering 1.5 A of continuous current to a load. The TPS92510 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor on the BOOT to PH pin. The boot capacitor voltage is monitored by an UVLO circuit and turns the high-side MOSFET off when the boot voltage falls below a preset threshold. The TPS92510 can operate at high duty cycles because of the boot UVLO.

DETAILED DESCRIPTION

Start-Up

The VIN and EN UVLO conditions must be satisfied before the TPS92510 is allowed to switch. When the EN pin is held low the device enters a low-power shutdown mode, and some internal circuits are deactivated to conserve power. When EN returns high these circuits are enabled, which results in a delay of approximately 50 µs (typical) before switching starts. During start-up the TPS92510 operates in a *minimum pulse width* mode, which is an open-loop control. At the start of each switching cycle the internal oscillator initiates a SET pulse. The high-side MOSFET turns on with a minimum pulse width of 300 ns (typical), independent of the COMP voltage. The device does not pulse skip. While operating in minimum pulse width mode the LED bypass capacitor is being charged, causing an in-rush current. Also, the COMP voltage begins to rise as the error amplifier output current charges the compensation network. When the COMP voltage reaches approximately 0.7 V, the error amplifier is ensured to be out of saturation and to have sufficient gain to regulate the loop. The TPS92510 then transitions from *minimum pulse width* mode to *regulation* mode. During regulation mode the error amplifier is now in closed-loop control of the system. The gain of the error amplifier quickly increases the duty cycle, which causes the output voltage to increase. Once the output voltage approaches the forward voltage of the LED string the LED current quickly begins to increase until it reaches regulation.

There is a slight delay from the time the VIN and EN UVLO conditions are satisfied until the time the error amplifier has control of the feedback loop. This delay is a result of the time it takes COMP to charge the compensation components to 0.7 V. This delay can be approximated as shown in Equation 1 .

$$t_{DELAY} = C1 \times \frac{\left(0.7\,V - \left(R1 \times 32\,\mu A\right)\right)}{32\,\mu A} \quad (1)$$

where

- C1 is the integrator capacitor from COMP to GND
- R1 is the resistor in series with the integrator capacitor

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DETAILED DESCRIPTION (continued)

The peak in-rush current can be calculated to a first approximation using Equation 2.

$$I_{PEAK} = \frac{V_{IN} \times t_{ON(min)} \times f_{SW}}{\sqrt{\frac{L}{C_{OUT}}} + R_{SENSE}}$$

where

- $t_{ON(min)}$ is the minimum on-time and can be between 200 ns and 300 ns (2)

Minimum Pulse Width Limitations

The TPS92510 is designed to output a minimum pulse width during each switching cycle of 280 ns (typical). The control loop cannot regulate the system to an on-time less than this amount, and it does not skip pulses. When attempting to operate below the minimum on-time the system loses regulation and the LED current increases. This puts a practical limitation on the system operating conditions, as shown in Equation 3.

$$V_{IN} = \frac{V_{OUT}}{f_{SW} \times t_{ON(min)}}$$

where

- V_{OUT} equals the forward voltage of the LED string plus the reference voltage (3)

The system can avoid this operating condition by limiting the maximum input voltage as shown in Equation 3 . If the input voltage cannot be limited due to application, then the switching frequency can be lowered, or the output voltage increased. This region of operation typically occurs with high input voltages, high operating frequencies, and low output voltages (one LED).

Enable and Adjusting Undervoltage Lockout

The TPS92510 is enabled when the VIN pin voltage is above 2.5 V and when the EN pin voltage is above 1.25 V. The VIN pin voltage threshold has no hysteresis. Figure 22 shows how to use the EN pin to adjust the input voltage UVLO to a higher threshold and increase the input voltage hysteresis. The EN pin has an internal pull-up current source, I1, of 0.9 µA that provides a default ON state when the EN pin is floating. Once the EN pin voltage exceeds 1.25 V, an additional 2.9 µA of hysteresis, I_{HYS}, is added. This additional current provides some input voltage hysteresis. Use Equation 4 to set the external hysteresis for the input voltage. Use Equation 5 to set the input start voltage. When the EN pin is held low the internal regulators are shut down and the device enters a low-power mode. In addition, the error amplifier output discharges the COMP voltage through a diode path to GND.

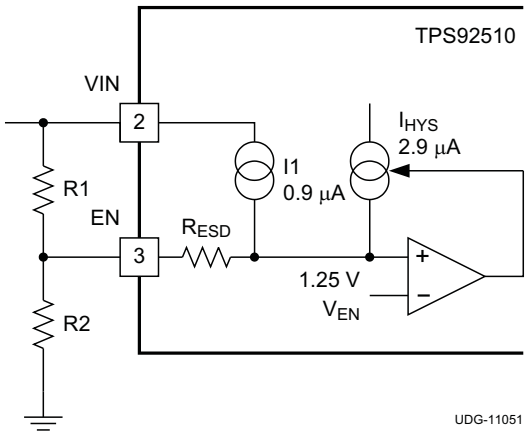


Figure 22. Adjustable Undervoltage Lockout (UVLO)

$$R1 = \frac{V_{HYS} \times \left(V_{EN} - \left(I1 \times R_{ESD}\right)\right) - I_{HYS} \times R_{ESD} \times V_{START}}{I_{HYS} \times V_{EN}} \quad (4)$$

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DETAILED DESCRIPTION (continued)

$$R2 = \frac{R1 \times \left(V_{EN} - \left(R_{ESD} \times \left(I1 + I_{HYS}\right)\right)\right)}{\left(V_{STOP} - V_{EN}\right) + \left(I1 + I_{HYS}\right) \times \left(R1 + R_{ESD}\right)} \quad (5)$$

$$V_{HYS} = V_{START} - V_{STOP} \quad (6)$$

$$R_{ESD} = 10\,k\Omega \quad (7)$$

Fixed Frequency PWM Control

The TPS92510 uses an adjustable, fixed-frequency, peak current mode control. Each switching cycle an internal oscillator initiates the turn-on of the MOSFET. The LED current flows through the sense resistor and develops the feedback voltage on the VSENSE pin. The error amplifier output (COMP pin) is compared to the high-side MOSFET current. When the MOSFET current reaches the level set by the COMP pin voltage the MOSFET is turned off.

Slope Compensation

The TPS92510 adds a compensating ramp to the MOSFET current signal. The slope compensation prevents sub-harmonic oscillations. The available peak inductor current remains constant over the full duty-cycle range.

Constant Switching Frequency and Timing Resistor (RT/CLK Pin)

The switching frequency of the TPS92510 is adjustable over a wide range from approximately 100 kHz to 2500 kHz by placing a resistor on the RT/CLK pin. The RT/CLK pin voltage is typically 0.5V and must have a resistor to ground to set the switching frequency. To determine the timing resistance for a given switching frequency, use Equation 8 or the curves in Figure 5 or Figure 6. To reduce the solution size one typically sets the switching frequency as high as possible, but tradeoffs of the supply efficiency, maximum input voltage and minimum controllable on time should be considered. The minimum controllable on time is typically 135 ns and limits the maximum operating input voltage.

$$R_{RT}\left(k\Omega\right) = \frac{206033}{\left(f_{SW}\right)^{1.0888}\left(kHz\right)} \quad (8)$$

$$f_{SW}\left(kHz\right) = \left(\frac{206033}{R_{RT}\left(k\Omega\right)}\right)^{\left(\frac{1}{1.0888}\right)} \quad (9)$$

Synchronization to an External System Clock (RT/CLK)

The RT/CLK pin can be used to synchronize the regulator to an external system clock by connecting a square wave to the RT/CLK pin through the circuit network as shown in Figure 23. The square wave amplitude must transition lower than 0.5 V and higher than 2.2 V on the RT/CLK pin and have an on-time greater than 40 ns and an off-time greater than 40 ns. The synchronization frequency range is 300 kHz to 2200 kHz. The rising edge of the PH is synchronized to the falling edge of RT/CLK pin signal. The external synchronization circuit default frequency is set by connecting the resistor from the RT/CLK pin to ground should the synchronization signal turn off. It is recommended to use a frequency set resistor connected as shown in Figure 23 through a 50-Ω resistor to ground.

The resistor should set the switching frequency close to the external CLK frequency. It is recommended to ac couple the synchronization signal through a 470-pF ceramic capacitor to RT/CLK pin and a 4-kΩ series resistor. The series resistor reduces PH jitter in heavy load applications when synchronizing to an external clock and in applications which transition from synchronizing to RT mode. The first time the CLK is pulled above the CLK threshold the device switches from the RT resistor frequency to PLL mode. The internal 0.5-V voltage source is removed and the CLK pin becomes high impedance as the PLL starts to lock onto the external signal. Since there is a PLL on the regulator the switching frequency can be higher or lower than the frequency set with the external resistor. The device transitions from the resistor mode to the PLL mode and then increases or decreases the switching frequency until the PLL locks onto the CLK frequency within 100 microseconds.

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When the device transitions from the PLL to resistor mode, the switching frequency slows down from the CLK frequency to 150 kHz, then reapply the 0.5-V voltage and the resistor then sets the switching frequency. It is not recommended that a system transition from PLL mode to resistor mode repeatedly during operation. When the PLL loses the external clock input the default 150-kHz switching frequency creates long on-times, which result in higher inductor ripple currents. This can lead to inductor saturation if the system is not designed to operate at this frequency. Figure 24, shows the device synchronized to an external system clock in continuous conduction mode (CCM).

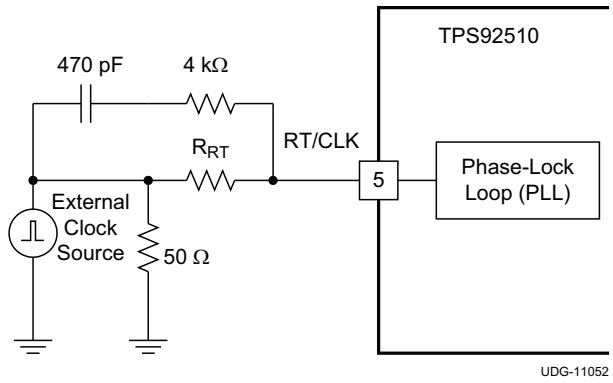


Figure 23. Synchronizing to a System Clock

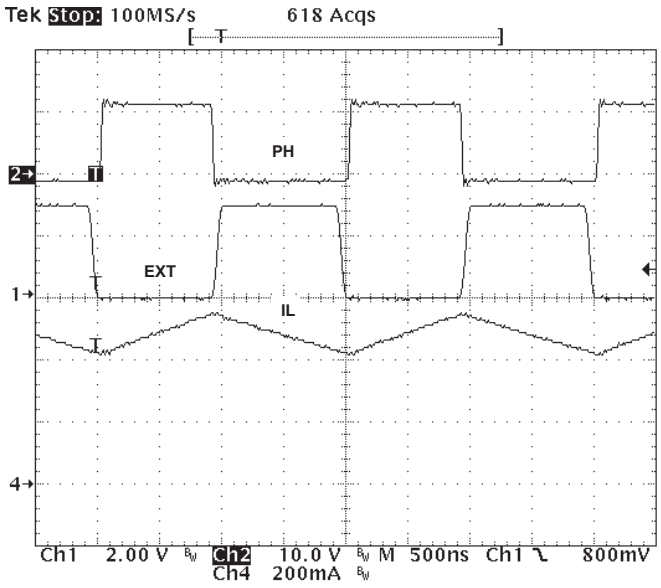


Figure 24. Plot of Synchronizing in CCM

Error Amplifier

The TPS92510 error amplifier is a transconductance amplifier. It compares the VSENSE voltage to the internal 0.2-V voltage reference. The transconductance (gm) of the error amplifier is 310 µA/V. The frequency compensation components are connected from the COMP pin to ground.

Voltage Reference and Output Current

The internal voltage reference is accurate to ± 5% over temperature. The LED current is programmed with a sense resistor from the VSENSE pin to GND. It is recommended to use a 1% tolerance resistor, or better.

PWM Dimming

The TPS92510 incorporates a PWM dimming input pin, which directly controls the enable/disable state of the internal gate driver. When PDIM is low, the gate driver is disabled. The PDIM pin has a 1-µA pull-up current source, which creates a default ON state when the PDIM pin is floating. When PDIM goes low and the gate driver shuts off, and the LED current quickly reduces to zero.

The TPS92510 uses a sample-and-hold switch on the error amplifier output. During the PDIM off-time the COMP voltage remains unchanged. Also, the error amplifier output is internally clamped low. These techniques help the system recover to its regulation duty cycle quickly.

Duty Cycle and Bootstrap Voltage (BOOT)

The TPS92510 requires a small 0.1-µF ceramic capacitor between the BOOT and PH pins to provide the gate drive voltage for the high-side MOSFET. The BOOT capacitor is refreshed when the high-side MOSFET turns off, and the freewheeling diode conducts. A ceramic capacitor with an X7R or X5R dielectric and a minimum voltage rating of 10 V is recommended.

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The TPS92510 is designed to operate up to 100% duty cycle as long as the BOOT to PH voltage is greater than 2.1V. If the BOOT capacitor voltage drops below 2.1 V, then the BOOT UVLO circuit turns off the MOSFET, which allows the BOOT capacitor to be refreshed. The current required from the BOOT capacitor to keep the MOSFET on is quite low. Therefore, many switching cycles occur before the BOOT capacitor is refreshed. In this way, the effective duty cycle of the converter is quite high.

Attention must be taken in maximum duty cycle applications which experience extended time periods with little or no load current. When the voltage across the BOOT capacitor falls below the 2.1 V UVLO threshold, the high-side MOSFET is turned off, but there may not be enough inductor current to pull the PH pin down to recharge the BOOT capacitor. The high-side MOSFET of the regulator stops switching because the voltage across the BOOT capacitor is less than 2.1 V. The output capacitor then decays until the difference between the input voltage and output voltage is greater than 2.1 V, at which point the BOOT UVLO threshold is exceeded, and the device starts switching again until the desired output current is reached. This operating condition persists until the input voltage and/or the load current increases. It is recommended to adjust the VIN stop voltage greater than the BOOT UVLO trigger condition at the minimum load of the application using the adjustable VIN UVLO feature with resistors on the EN pin.

Overcurrent Protection

An overcurrent fault condition is unlikely. It can be the result of a shorted sense resistor, or a direct short from VOUT to GND. In either case, the voltage at the VSENSE pin is zero, and this causes the COMP pin voltage to rise. When V_{COMP} reaches approximately 2.2 V it is internally clamped, and functions as a MOSFET current limit. The TPS92510 limits the MOSFET current to 4 A (typical). If the shorted condition persists the TPS92510 junction temperature increases. If it increases above 150°C, the thermal shutdown protection is activated.

LED Thermal Foldback Protection

The TPS92510 implements a thermal foldback protection to limit the LED temperature in case of a system failure, such as an incorrectly programmed LED current, a poor thermal design or increasing thermal impedance over time. A 100-µA current source generates a voltage across an NTC resistor that is located near the LED load. When the NTC voltage drops below 2 V at the TSENSE pin (due to excessive LED temperature) the device begins to modulate the converter at a frequency of 5.9 kHz. The more the NTC voltage drops, the longer the off-time of the converter. Therefore, the delivered output power is reduced until the NTC cools, the TSENSE voltage (V_{TSENSE}) increases, and the system no longer requires reduced output power. The thermal foldback protection slowly reduces the output power, as a function of the thermal time constant. Thermal foldback protection is intended for protection only. It is not intended to be used as a regulation feature. During thermal foldback the error amplifier output is internally clamped low, and the COMP sample-and-hold switch is open, preserving the COMP pin voltage.

Figure 25 shows the thermal foldback linearity.

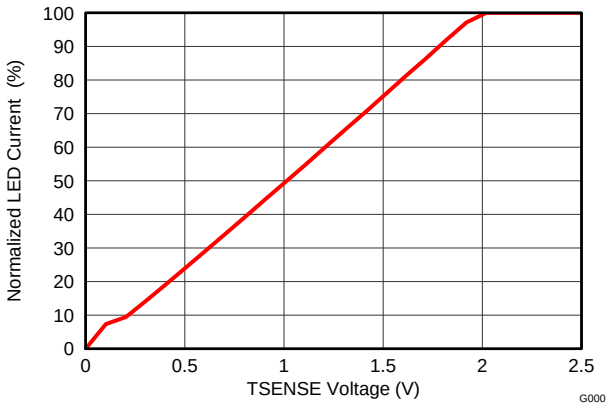


Figure 25. Thermal Foldback Linearity

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Over-Temperature Fault Protection

When the TPS92510 junction temperature reaches 150ºC, the driver immediately disables the high-side MOSFET. The COMP sample-and-hold switch closes, and the COMP pin internally clamps low until the junction temperature drops by approximately 20ºC. At this time, the COMP clamp is removed and the driver attempts to regulate.

APPLICATION INFORMATION

Open LED Fault Protection

An open circuit can be the result of an open LED or an open wire connection. In either case, the voltage at the VSENSE pin becomes zero, and this causes the COMP pin voltage to rise, commanding wide duty cycles. The output voltage eventually rises to the input voltage. This is a safe operating mode, provided that the output capacitors are rated for the input voltage potential.

As shown in Figure 26, a transient voltage suppressor (TVS) device from V_{OUT} to GND, or a diode from V_{OUT} to the VIN pin can be used to clamp the L-C resonant output voltage ringing caused by the inductor and the output capacitor at the moment the LED string opens, particularly at high-input voltage and high-output voltage operating conditions. The TVS should have a voltage rating greater than the maximum output voltage, so that it does not conduct under normal operation. Either of these devices can be used to limit the output voltage to safe levels during an open LED fault.

If the current sense resistor also opens, current attempts to flow into the ESD structure of the VSENSE pin. To prevent damage to the device, a series resistor (R_{ESD}) on the VSENSE pin can be used to limit this current. The VSENSE pin has an internal, 8-V clamp, and the continuous current should be limited to a maximum of 20 mA.

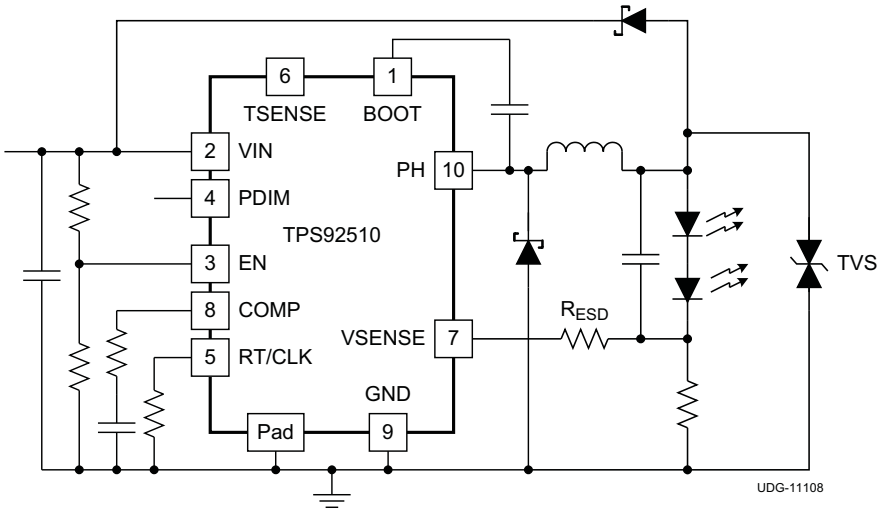


Figure 26. Output Voltage Clamp

An external overvoltage protection circuit consisting of V_Z and R_Z shown in Figure 27, can be applied to the VSENSE pin to regulate the output voltage to less than the input voltage potential.

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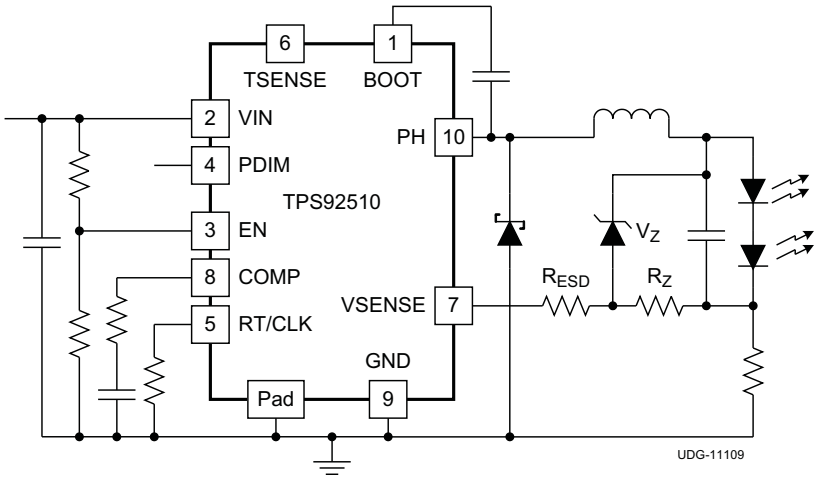


Figure 27. Output Voltage Limiter

Shorted LED(s) Fault Protection

Some LEDs fail to a shorted state. It is unlikely that multiple LEDs fail short simultaneously. If a bypass capacitor is in parallel with the LED string it is charged to the LED string forward voltage. When one or more LEDs instantaneously short, the bypass capacitor senses a voltage transient from the initial LED string voltage to something less, depending on the number of LEDs that are now shorted. The voltage change across the capacitor causes the capacitor to discharge some energy in the form of a transient current through the LED string. This current flows from the bypass capacitor through the LED string, but not through the current sense resistor. Therefore, the TPS92510 does not sense the fault event, and does not respond to it. The peak transient current is a function of the change in forward voltage due to the shorted LED(s), and the dynamic resistance of the LED string at the moment the short occurs. This current can be substantial, and may require a protection circuit as shown in Figure 28, unless the LEDs can survive the transient current. After the LED has shorted the error amplifier continues to regulate the programmed LED current at the new, lower output voltage.

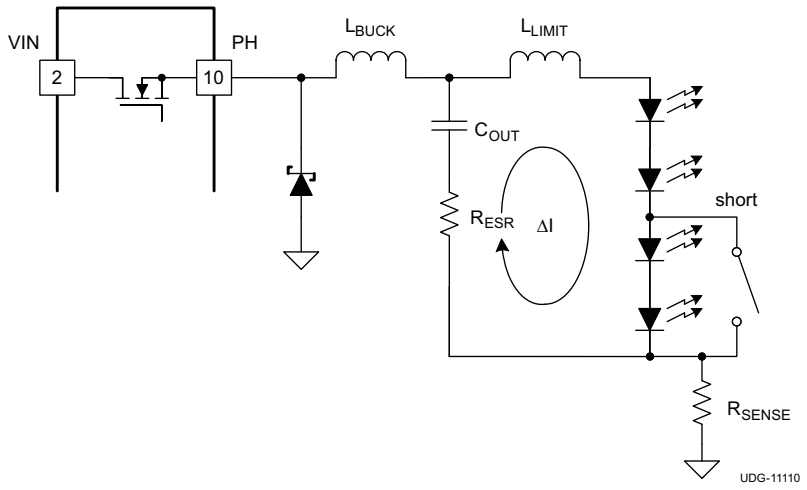


Figure 28. LED Current Limiter Due to a Shorted LED

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Equation 10 shows how to reduce the peak transient current (ΔI) by adding a series inductance (L_{LIMIT}). Typically, the bypass capacitor (C_{OUT}) is used to reduce the high-frequency ripple current through the LED. Adding inductance into this path is counter productive. Alternatively, the buck inductance, or switching frequency can be increased to achieve a lower LED ripple current. In this way, the output capacitor can be reduced in value, which allows L_{LIMIT} to be smaller. The end result of low LED ripple current can still be achieved. Reducing the output capacitor (C_{OUT}) does not reduce the magnitude of the transient current, but it does reduce the settling time.

$$\Delta I = \frac{\Delta V_F}{R_{DYNAMIC} + R_{ESR} + \sqrt{\frac{L_{LIMIT}}{C_{OUT}}}} \tag{10}$$

Open Current Sense Resistor Fault Protection

An open current sense resistor is unlikely, but may be caused by a failing resistor, an open solder joint, or an open PCB trace. As the current sense resistor opens, the output voltage quickly rises due to the energy stored in the inductor, similar to an open LED fault. Therefore, it is necessary to clamp the output voltage, either with a TVS to GND or a diode from VOUT to VIN. It is also necessary to use a current limiting resistor on the VSENSE pin. Otherwise, the output voltage spike causes the VSENSE voltage to break down its internal ESD structure. The ESD device should be limited to 20 mA. In this condition, the converter attempts to regulate the output current through the ESD structure, which results in a very low regulated current. Typically, the output voltage overcharges and holds the VSENSE voltage high within a few switching cycles. The device stops switching, and there is a long off-time between consecutive start-up attempts. The consecutive attempts result in lower peak current through the ESD structure than the initial event.

Shorted Output Fault

A shorted output fault is considered rare, because the system does not require any single component from V_{OUT} to GND. Therefore, a single component failure cannot cause this fault condition. If this failure mode were to occur it would most likely be due to a mechanical short, or a foreign object. In the unlikely event of this failure mode, the TPS92510 responds in the following way.

With the output voltage shorted directly to ground the COMP voltage saturates high, because the feedback voltage is zero. The controller would naturally command wide duty cycle PH pulses. However, as soon as the gate driver turns on, very quickly an overcurrent event is detected and the PH pulse is truncated. This results in minimum on-time pulses at the PH node. Depending upon the impedance of the short, large currents can build up in the inductor, which naturally raises the junction temperature of the TPS92510. The over-temperature protection feature protects the device.

Control-to-Output Transfer Function

The TPS92510 converter uses peak current mode control in order to regulate the average LED current. Slope compensation is utilized internally to eliminate sub-harmonic oscillations over a wide range of operating duty cycles. To properly compensate the closed-loop system the control to output gain characteristics must be calculated. The control to output transfer function is shown in Equation 11.

$$G_{C2O}(s) = \frac{167 \times 10^{-6} \times f_M \times R_{SENSE} \times Gi(s)}{1 + 17 \times 10^{-6} \times f_M \times Gi(s) \times He(s) - f_M \times G_V \times Gi(s) \times Z_{OUT}(s)} \tag{11}$$

where

- R_{SENSE} is the LED current sense resistance

$$f_M = \frac{117 \times 10^3 \times L \times f_{SW}}{V_{IN} - V_{OUT} + 3 \times f_{SW} \times L} \tag{12}$$

where

- L is the output inductance
- f_{SW} is the switching frequency in Hz

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$$Gi(s) = \frac{V_{IN}}{s \times L + R_{DCR} + R_{SENSE} + \frac{\left(R_{ESR} + \frac{1}{s \times C_{OUT}}\right) \times R_{LED}}{\left(R_{ESR} + \frac{1}{s \times C_{OUT}}\right) + R_{LED}}} \quad (13)$$

where

- R_{DCR} is the DC resistance of the output inductor
- C_{OUT} is the output capacitance.
- R_{ESR} is the equivalent series resistance of the output capacitor
- R_{LED} is the dynamic resistance of the entire LED string and is dependent upon the LED current (I_{LED})

$$He(s) = 1 + \frac{s}{-2 \times f_{SW}} + \frac{s^2}{(\pi \times f_{SW})^2} \quad (14)$$

$$G_V = \frac{V_{OUT}}{117.2 \times 10^3 \times L \times V_{IN} \times f_{SW}} \quad (15)$$

$$Z_{OUT} = \frac{R_{LED} \times \left(R_{ESR} + \frac{1}{s \times C_{OUT}}\right)}{R_{LED} + R_{ESR} + \left(\frac{1}{s \times C_{OUT}}\right)} + R_{SENSE} \quad (16)$$

$$V_{OUT} = V_F \times n + 0.2\,V \quad (17)$$

where

- V_F is the forward voltage of an individual LED
- n is the number of LEDs in the string

The control-to-output transfer function can be understood best by plotting it using a computer aided mathematics program such as Mathcad. The resulting plot shows that the control to output DC gain is typically very low, which can also be computed with Equation 18.

$$G_{DC} = \frac{167 \times V_{IN} \times f_M \times R_{SENSE}}{17 \times V_{IN} \times f_M + 1000000 \times \left(R_{DCR} + R_{SENSE} + R_{LED} - f_M \times V_{IN} \times G_V \times \left(R_{SENSE} + R_{LED}\right)\right)} \quad (18)$$

Compensating the Loop

The control-to-output transfer function is compensated by the error amplifier in order to accomplish the following functions.

- more DC gain is required for better current regulation
- more bandwidth is desired for better PWM dimming and transient performance
- adequate phase margin is needed for system stability

The TPS92510 utilizes peak current mode control, which effectively reduces the power stage's second order pole to a first order pole. A single pole power stage can be compensated easily with a single capacitor from COMP to GND, which forms a dominate pole. This compensation topology is referred to as Type I and is shown in Figure 29. In most applications, a Type I compensation network can be used when a low cross-over frequency (typically less than 10 kHz) is desired. Equation 19 calculates the required capacitance from the COMP pin to GND in order to achieve a desired cross-over frequency (f_{CO}), knowing the DC gain of the power stage (G_{DC}).

Type I Compensation

$$C1 = \frac{g_{M(ea)} \times G_{DC}}{2 \times \pi \times f_{CO}} \quad (19)$$

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The compensated loop gain is equal to the control to output transfer function multiplied by the error amplifier transfer function as shown in Equation 20.

$$G_{CL} = G_{C2O} \times G_{EA} \tag{20}$$

$$G_{EA} = \frac{g_{M(ea)}}{s \times C1} \tag{21}$$

The transconductance gain of the error amplifier ($g_{M(ea)}$) is 310 µA/V.

Type II Compensation

When using PWM dimming, it is beneficial to extend the loop bandwidth beyond 10 kHz. In this case, a Type II compensation topology can be used. The gain of the error amplifier changes as shown in Equation 22.

$$G_{EA} = g_{M(ea)} \frac{1 + (s \times R1 \times C1)}{s \times (C1 + C2) + \left(s^2 \times R1 \times C1 \times C2\right)} \tag{22}$$

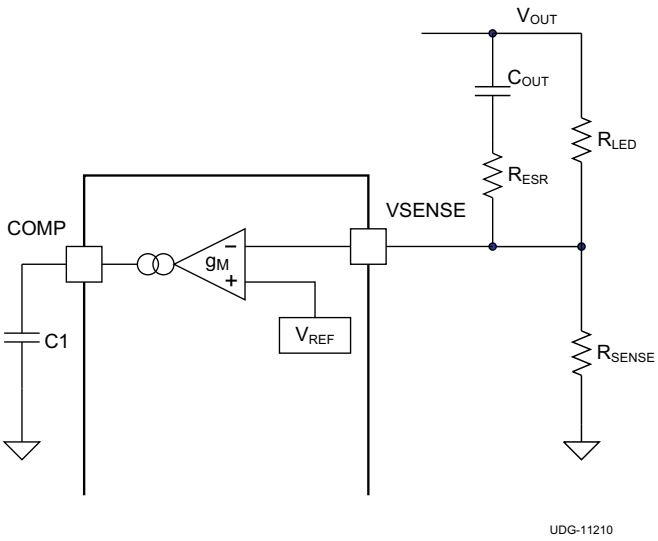


Figure 29. Type I Compensation

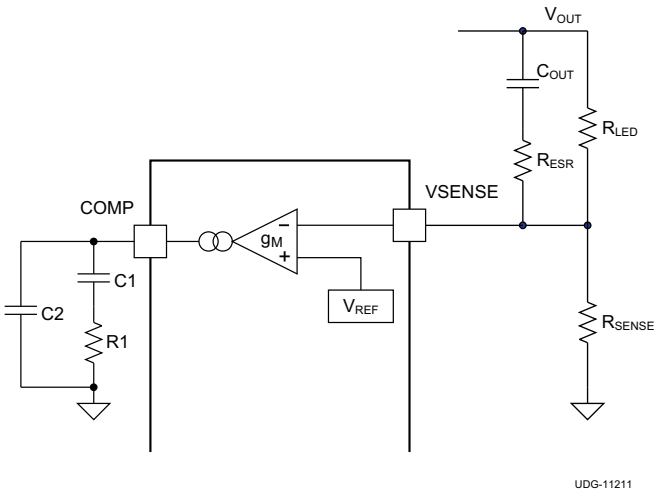


Figure 30. Type II Compensation

Knowing the desired cross-over frequency (f_{CO}) and the power stage DC dain (G_{DC}), the error amplifier can be easily compensated with a Type II network. Equation 23 through Equation 25 show some simple approximations for the compensation values. Capacitor C1 has the biggest influence on the cross-over frequency and low-frequency gain. Resistor R1 creates a zero in the error amplifier transfer function, which improves the phase margin particularly near the cross-over frequency. Capacitor C2 creates a high-frequency pole to reduce gain beyond the cross-over frequency.

$$C1 = \frac{g_{M(ea)} \times G_{DC}}{2 \times \pi \times f_{CO}} \tag{23}$$

$$R1 = \frac{1}{2\pi \times K \times f_{CO} \times C1}$$

where

- K is a multiplier of the desired cross-over frequency (24)

$$C2 = \frac{C1}{10} \tag{25}$$

For reference, the error amplifier zero frequency and high-frequency pole equations are shown in Equation 26 through Equation 27.

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$$f_{EA(zero)} = \frac{1}{2\pi \times R1 \times C1} \quad (26)$$

$$f_{EA(pole)} = \frac{1}{2\pi \times R1 \times \left(\frac{C1 \times C2}{C1 + C2}\right)} \cong \frac{1}{2\pi \times R1 \times C2} \quad (27)$$

The compensation equations above are given as a guideline. It is strongly recommended to verify the closed loop response for adequate gain and phase margin by directly measuring the circuit. The value of C1 is inversely proportional to the closed loop bandwidth of the system: as C1 decreases, the loop bandwidth increases. If the measured loop gain is too high, increase the value of C1 and recalculate R1 and C2. For a Type II compensation network a good cross-over frequency target is between 10 kHz and 50 kHz, but should not exceed one-fifth (1/5) of the switching frequency (f_{SW}).

When calculating the value of R1 the K multiplier must be chosen. Typically, this value is between 1.5 and 4. A good starting value for K is 2 or 3. This places the error amplifier zero frequency two or three times higher than the desired cross-over frequency. When measuring the loop response, if additional phase margin is needed the K value can be reduced, resulting in a larger R1 value. Alternatively, as the K multiplier increases beyond 4 the value of R1 becomes so small that its benefit to phase margin becomes insignificant, and the error amplifier performance begins to approach a Type I network.

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Changes from Original (JANUARY 2012) to Revision A **Page**

- Changed corrected y-axis label on Figure 8 8
- Changed corrected test condition on Figure 14 9

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS92510DGQ	Active	Production	HVSSOP (DGQ) | 10	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	92510
TPS92510DGQ.A	Active	Production	HVSSOP (DGQ) | 10	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	92510
TPS92510DGQG4	Active	Production	HVSSOP (DGQ) | 10	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	92510
TPS92510DGQG4.A	Active	Production	HVSSOP (DGQ) | 10	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	92510
TPS92510DGQR	Active	Production	HVSSOP (DGQ) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	92510
TPS92510DGQR.A	Active	Production	HVSSOP (DGQ) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	92510

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

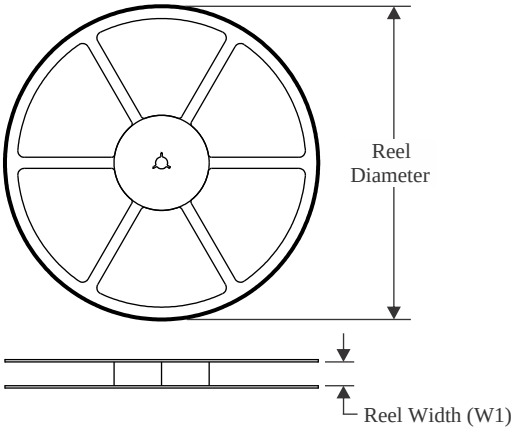
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

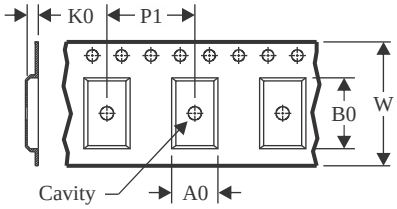
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

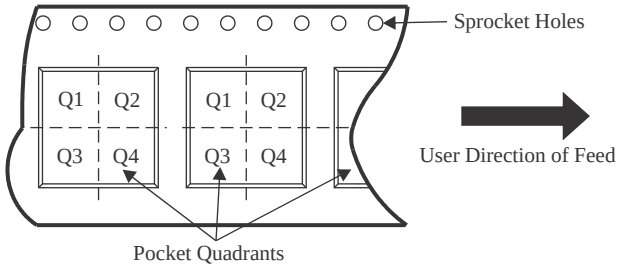


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

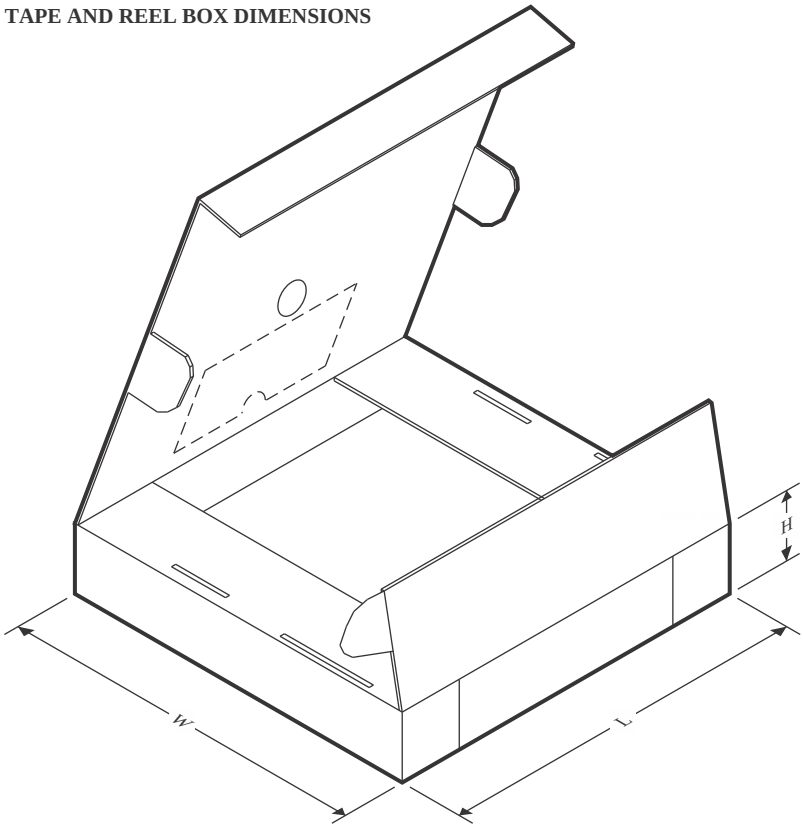
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92510DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

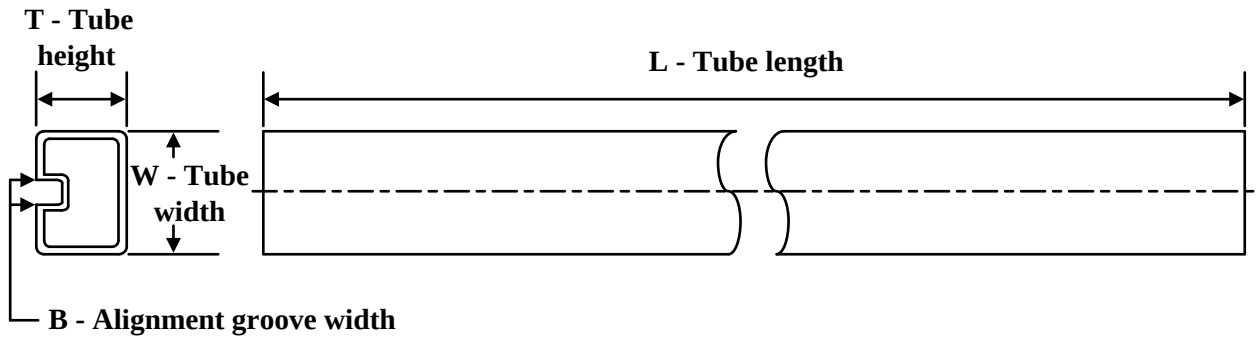
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92510DGQR	HVSSOP	DGQ	10	2500	358.0	335.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS92510DGQ	DGQ	HVSSOP	10	80	274	6.2	2540	2.5
TPS92510DGQ.A	DGQ	HVSSOP	10	80	274	6.2	2540	2.5
TPS92510DGQG4	DGQ	HVSSOP	10	80	274	6.2	2540	2.5
TPS92510DGQG4.A	DGQ	HVSSOP	10	80	274	6.2	2540	2.5

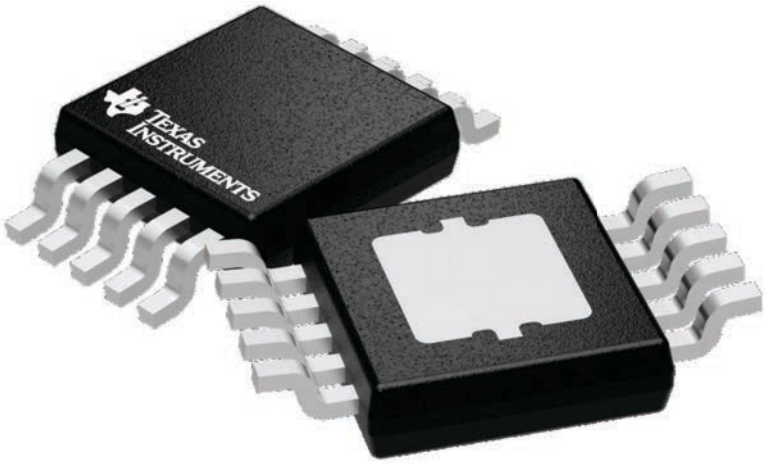
GENERIC PACKAGE VIEW

DGQ 10

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.5 mm pitch

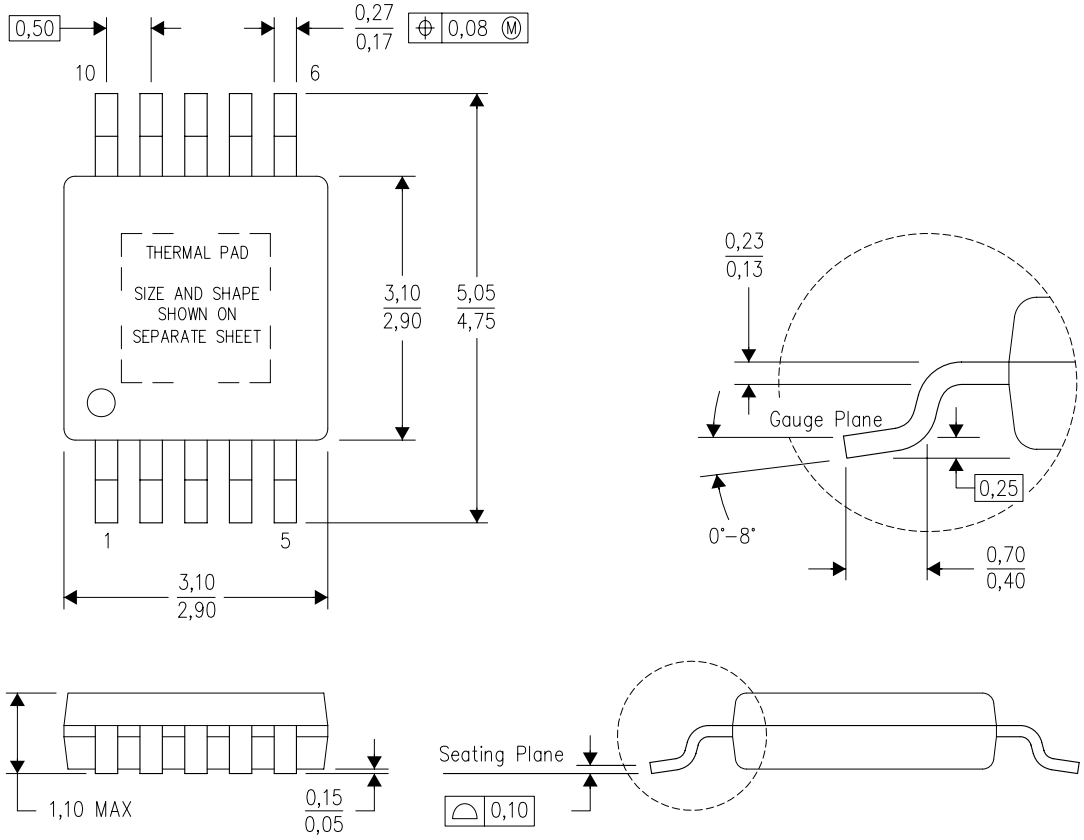
PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224775/A

DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL OUTLINE



4073273/F 11/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation BA–T.

PowerPAD is a trademark of Texas Instruments.

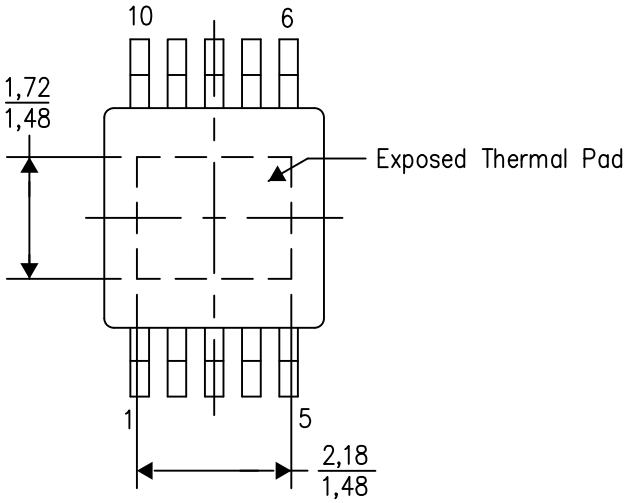
DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206324–4/H 12/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

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