

# TPS7A6650H-Q1 40V、超低 $I_{(q)}$ 、环境温度最高为 150°C 的稳压器

## 1 特性

- 适用于汽车电子应用
- 具有符合 AEC-Q100 标准的下列结果:
  - 器件温度: -40°C 至 150°C 的环境工作温度范围
  - 器件人体模型 (HBM) 静电放电 (ESD) 分类等级 H2
  - 器件组件充电模式 (CDM) ESD 分类等级 C4
- 4V 至 40V 的宽输入电压范围, 瞬态电压高达 45V
- 输出电流: 50mA
- 低静态电流 ( $I_{(q)}$ ):
  - 当 EN = 低电平时 (关断模式) 时为 2μA
  - 轻负载时典型值为 12μA
- 低等效串联电阻 (ESR) 陶瓷输出稳定电容器 (2.2μF-100μF)
- 50mA 时的压降电压为 130mV ( $V_{(Vin)} = 4V$  时的典型值)
- 5V 固定输出电压
- 低输入电压跟踪
- 集成型加电复位
  - 可编程复位脉冲延迟
  - 漏极开路复位输出
- 集成故障保护
  - 热关断
  - 短路保护功能
- 8 引脚 MSOP-DGN 封装

## 2 应用

- 动力传动传感器模块
- 具有睡眠模式的信息娱乐系统
- 车身控制模块
- 常开电池 应用
  - 网关 应用
  - 遥控无钥匙进入系统
  - 发动机防盗锁止系统

## 3 说明

TPS7A6650H-Q1 是一款低压降线性稳压器, 其设计适用于输入电压高达 40V 的操作。该器件在无负载时的静态电流仅为 12μA, 非常适合待机微处理器控制单元系统, 尤其是汽车 应用。

该器件 具有 集成式短路和过流保护。此器件在上电时执行复位延迟以指示输出电压稳定且处于稳压状态。用户可使用一个外部电容器来设定此延迟。低压跟踪特性允许使用更小的输入电容器并且有可能在冷启动条件下无需使用升压转换器。

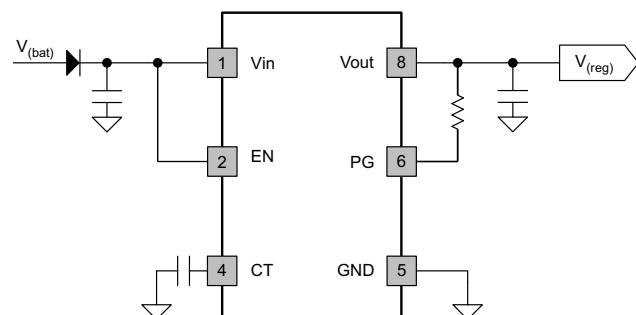
该器件可在 -40°C 至 150°C 的温度范围内工作, 非常适合各类汽车应用中的 电源。

### 器件信息(1)

器件型号	封装	封装尺寸 (标称值)
TPS7A6650H-Q1	HVSSOP (8)	3.00mm x 3.00mm

(1) 如需了解所有可用封装, 请见数据表末尾的可订购产品附录。

### 硬件使能选项



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

English Data Sheet: [SLVSD64](#)

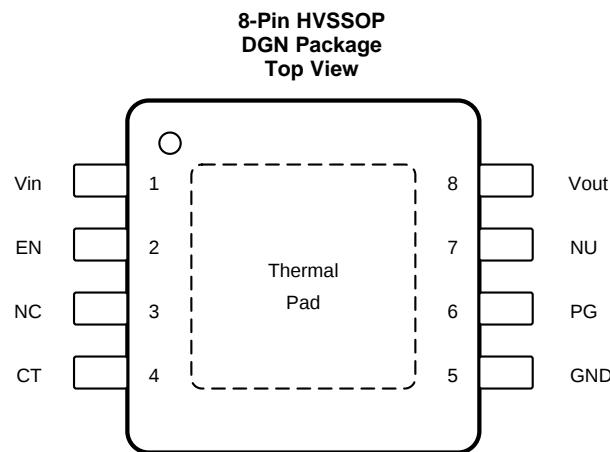
## 目录

1 特性	1	7.2 Functional Block Diagram	9
2 应用	1	7.3 Feature Description	9
3 说明	1	7.4 Device Functional Modes	12
4 修订历史记录	2	8 Application and Implementation	13
5 Pin Configuration and Functions	3	8.1 Application Information	13
6 Specifications	3	8.2 Typical Application	13
6.1 Absolute Maximum Ratings	3	9 Power Supply Recommendations	14
6.2 ESD Ratings	4	10 Layout	15
6.3 Recommended Operating Conditions	4	10.1 Layout Guidelines	15
6.4 Thermal Information	4	10.2 Layout Example	15
6.5 Electrical Characteristics	4	10.3 Power Dissipation and Thermal Considerations	15
6.6 Switching Characteristics	5	11 器件和文档支持	16
6.7 Qualification Summary	5	11.1 商标	16
6.8 Typical Characteristics	6	11.2 静电放电警告	16
7 Detailed Description	9	11.3 Glossary	16
7.1 Overview	9	12 机械、封装和可订购信息	16

## 4 修订历史记录

日期	修订版本	注释
2015年11月	*	最初发布版本

## 5 Pin Configuration and Functions



NC – No internal connection

NU – Make no external connection

### Pin Functions

PIN NAME	PIN NO.	TYPE	DESCRIPTION
CT	4	O	Reset-pulse delay adjustment. Connect this pin via a capacitor to GND
EN	2	I	Enable pin. The device enters the standby state when the enable pin becomes lower than the threshold.
NU	7	I	Not-used pin; make no external connection
GND	5	G	Ground reference
NC	3	—	Not-connected pin
PG	6	O	Output ready. This open-drain pin must connect to Vout via an external resistor. The output voltage going below threshold pulls it down.
Vin	1	P	Input power-supply voltage
Vout	8	O	Output voltage
—	—	—	Thermal pad

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
Vin, EN	Unregulated input <sup>(2)</sup> <sup>(3)</sup>	-0.3	45	V
Vout	Regulated output	-0.3	7	V
CT		-0.3	25	V
PG		-0.3	Vout	V
T <sub>J</sub>	Operating junction temperature range	-40	160	°C
T <sub>stg</sub>	Storage temperature range	-65	160	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to GND

(3) Absolute maximum voltage, withstand 45 V for 200 ms

## 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±4000	V
		Charged device model (CDM), per AEC Q100-011	All pins Corner pins (1, 4, 5, and 8)	
			±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>in</sub>	Unregulated input	4	40	V
EN		0	40	V
CT		0	20	V
V <sub>out</sub>		1.5	5.5	V
PG	Low voltage (I/O)	0	5.5	V
T <sub>A</sub>	Operating ambient temperature	-40	150	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS7A6650H-Q1	UNIT
		DGN (HVSSOP)	
		8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	63.4	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	53	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance <sup>(2)</sup>	37.4	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	3.7	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	37.1	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	13.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report ([SPRA953](#)).

(2) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

## 6.5 Electrical Characteristics

V<sub>(Vin)</sub> = 14 V, 1 mΩ < ESR < 2 Ω, T<sub>J</sub> = -40°C to 160°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY VOLTAGE AND CURRENT (V<sub>in</sub>)</b>					
V <sub>(Vin)</sub>	Input voltage	I <sub>O</sub> = 1 mA	5.5	40	V
I <sub>(q)</sub>	Quiescent current	V <sub>(Vin)</sub> = 5.5 V to 40 V, EN = ON, I <sub>O</sub> = 0.2 mA	12	22	µA
I <sub>(Sleep)</sub>	Input sleep current	No load current and EN = OFF		4	µA
I <sub>(EN)</sub>	EN pin current	V <sub>(EN)</sub> = 40 V		1	µA
V <sub>(VinUVLO)</sub>	Undervoltage detection	Ramp V <sub>(Vin)</sub> down until output turns OFF		2.6	V
V <sub>(UVLOhys)</sub>	Undervoltage hysteresis		1		V
<b>ENABLE INPUT (EN)</b>					
V <sub>IL</sub>	Logic input low level		0	0.4	V
V <sub>IH</sub>	Logic input high level		1.7		V

## Electrical Characteristics (接下页)

$V_{(Vin)} = 14 \text{ V}$ ,  $1 \text{ m}\Omega < \text{ESR} < 2 \Omega$ ,  $T_J = -40^\circ\text{C}$  to  $160^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>REGULATED OUTPUT (V<sub>out</sub>)</b>						
$V_{(Vout)}$	Regulated output	$I_O = 1 \text{ mA}$ , $T_J = 25^\circ\text{C}$	-1%	1%		
		$V_{(Vin)} = 6 \text{ V}$ to $40 \text{ V}$ , $I_O = 1 \text{ mA}$ to $50 \text{ mA}$	-2%	2%		
$V_{(\text{line-reg})}$	Line regulation	$V_{(Vin)} = 5.5 \text{ V}$ to $40 \text{ V}$ , $I_O = 50 \text{ mA}$		5		mV
$V_{(\text{load-reg})}$	Load regulation	$I_O = 1 \text{ mA}$ to $50 \text{ mA}$		20		mV
$V_{(\text{dropout})}$	Dropout voltage	$V_{(\text{dropout})} = V_{(Vin)} - V_{(Vout)}$ , $I_{\text{OUT}} = 50 \text{ mA}$	130	240		mV
$I_O$	Output current	$V_{(Vout)}$ in regulation	0	50		mA
$I_{(\text{reg-CL})}$	Output current limit	$V_{(Vout)}$ short to ground	500	800		mA
PSRR	Power supply ripple rejection <sup>(1)</sup>	$V_{(Vin)} = 12 \text{ V}$ , $I_L = 10 \text{ mA}$ , output capacitance = $2.2 \mu\text{F}$ ,				
		$V_{(Vin)} = 12 \text{ V}$ , $I_L = 10 \text{ mA}$ , output capacitance = $2.2 \mu\text{F}$ , frequency = $100 \text{ Hz}$	60			dB
		$V_{(Vin)} = 12 \text{ V}$ , $I_L = 10 \text{ mA}$ , output capacitance = $2.2 \mu\text{F}$ , frequency = $100 \text{ kHz}$	40			dB
<b>RESET (PG)</b>						
$V_{OL}$	Reset output, low voltage	$I_{OL} = 0.5 \text{ mA}$		0.4		V
$I_{Ikg}$	Leakage current	Reset pulled $V_{out}$ through $10\text{-k}\Omega$ resistor		1		$\mu\text{A}$
$V_{(\text{TH-POR})}$	Power-on-reset threshold	$V_{(Vout)}$ increasing	89.6	91.6	93.6	% of $V_{out}$
$V_{(\text{Thres})}$	Hysteresis			2		% of $V_{out}$
<b>RESET DELAY (CT)</b>						
$I_{(Chg)}$	Delay-capacitor charging current	$V_{(CT)} = 0 \text{ V}$	1.4			$\mu\text{A}$
$V_{(\text{th})}$	Threshold to release PG high		1			V
<b>OPERATING TEMPERATURE RANGE</b>						
$T_J$	Junction temperature		-40	160		$^\circ\text{C}$
$T_{(\text{shutdown})}$	Junction shutdown temperature		175			$^\circ\text{C}$
$T_{(\text{hyst})}$	Hysteresis of thermal shutdown		20			$^\circ\text{C}$

(1) Design information – Not tested

## 6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>TIMING FOR RESET (PG)</b>						
$t_{(\text{POR})}$	Power-on-reset delay	Where $C$ = delay capacitor value; capacitance $C = 100 \text{ nF}$ <sup>(1)</sup>	50	100	180	ms
		No capacitor on pin	100	290	650	$\mu\text{s}$
$t_{(\text{Deglitch})}$	Reset deglitch time		20	250		$\mu\text{s}$

(1) This information only is not tested in production and equation basis is  $(C \times 1) / 1 \times 10^{-6} = t_d$  (delay time).  
Where  $C$  = Delay capacitor value. Capacitance  $C$  range =  $100 \text{ pF}$  to  $100 \text{ nF}$ .

## 6.7 Qualification Summary

The TPS7A6650H-Q1 device has passed all the Grade 0 level qualification items required in AEC-Q100 with one exception: High temperature storage lifetime (HTSL). For the HTSL item, the Grade 0 level requirement is passing  $175^\circ\text{C}$  for 1000 hours of stress. For this device, it passed at  $160^\circ\text{C}$  for 1000 hours stress.

## 6.8 Typical Characteristics

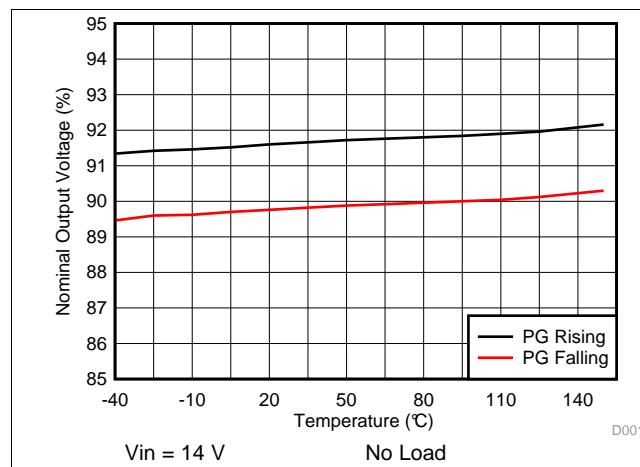


图 1. Power-Good Threshold Voltage vs Temperature

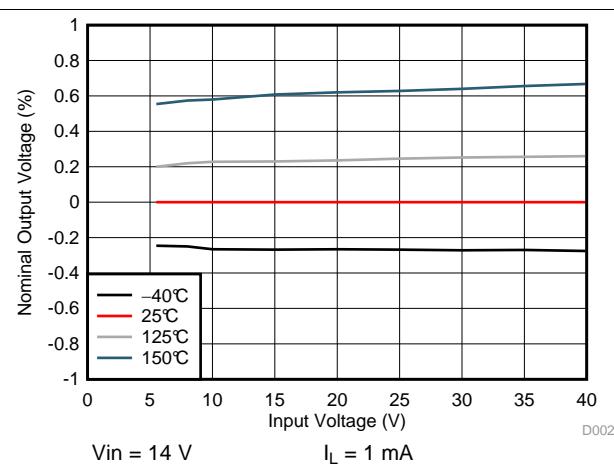


图 2. Line Regulation

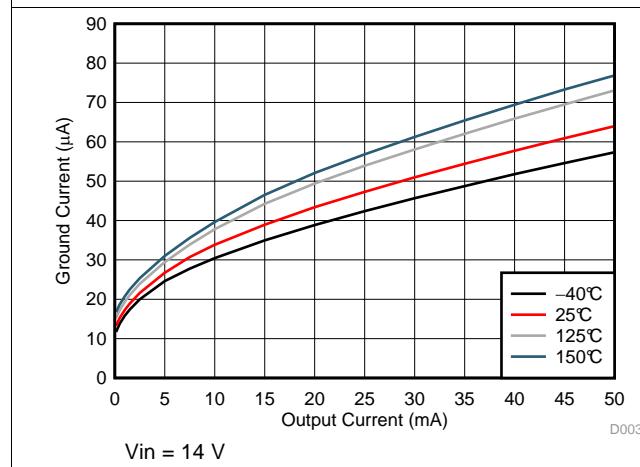


图 3. Ground Current vs Output Current

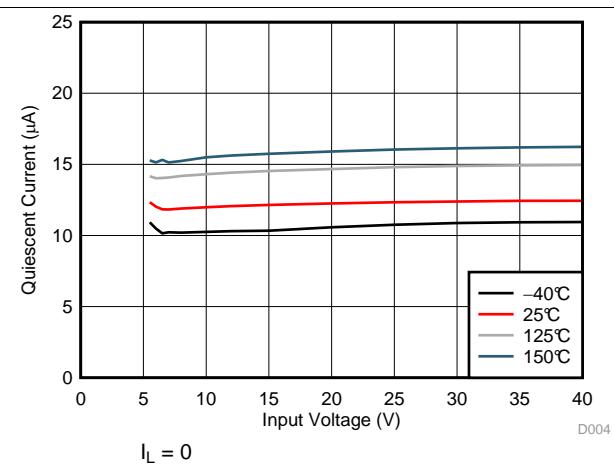


图 4. Quiescent Current vs Input Voltage

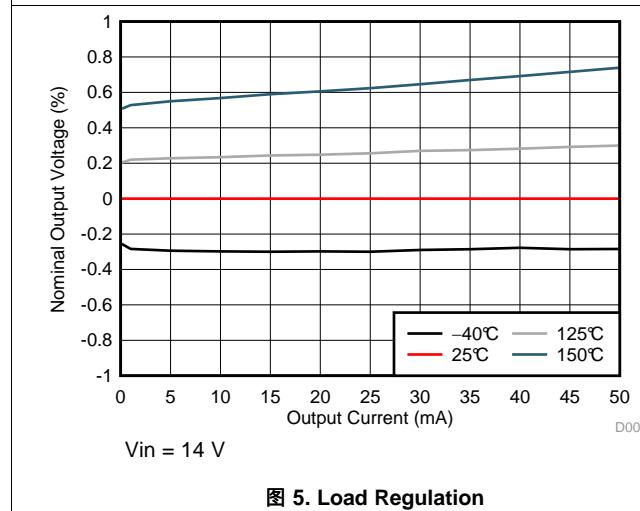


图 5. Load Regulation

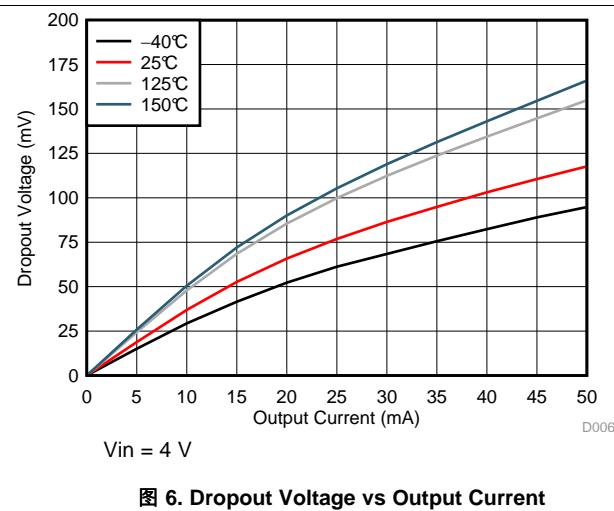
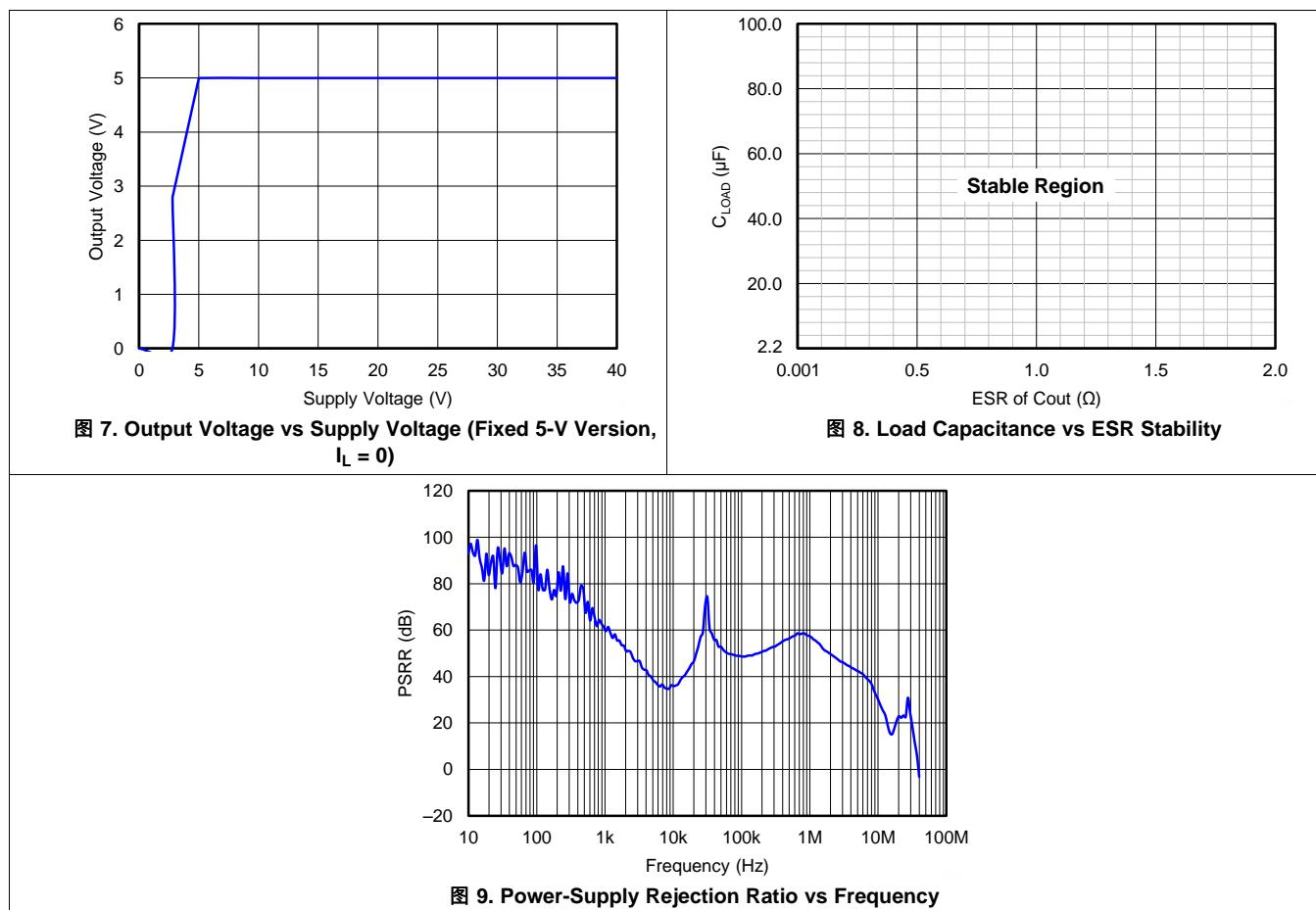
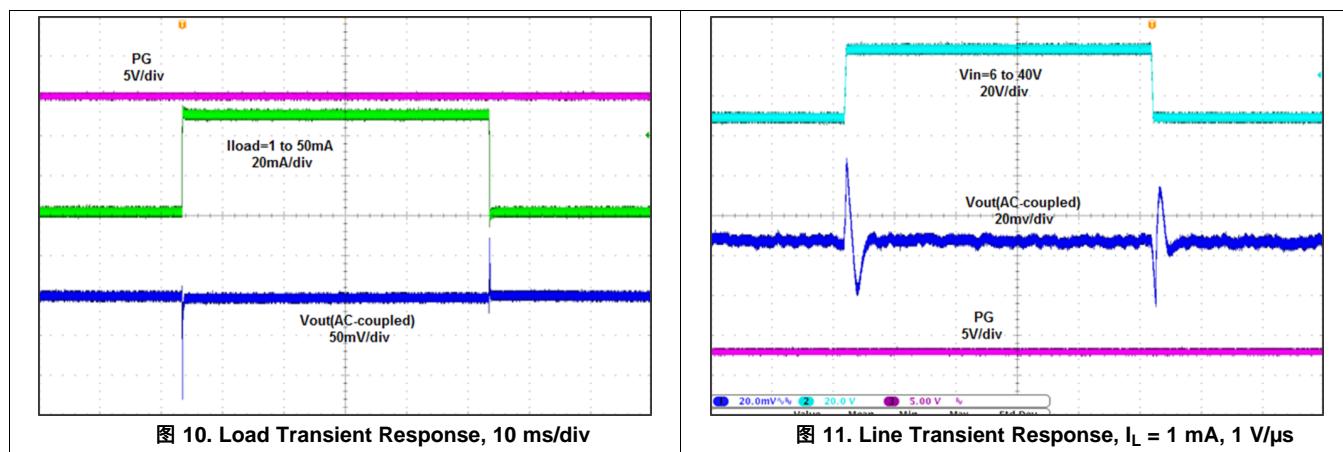


图 6. Dropout Voltage vs Output Current

## Typical Characteristics (接下页)

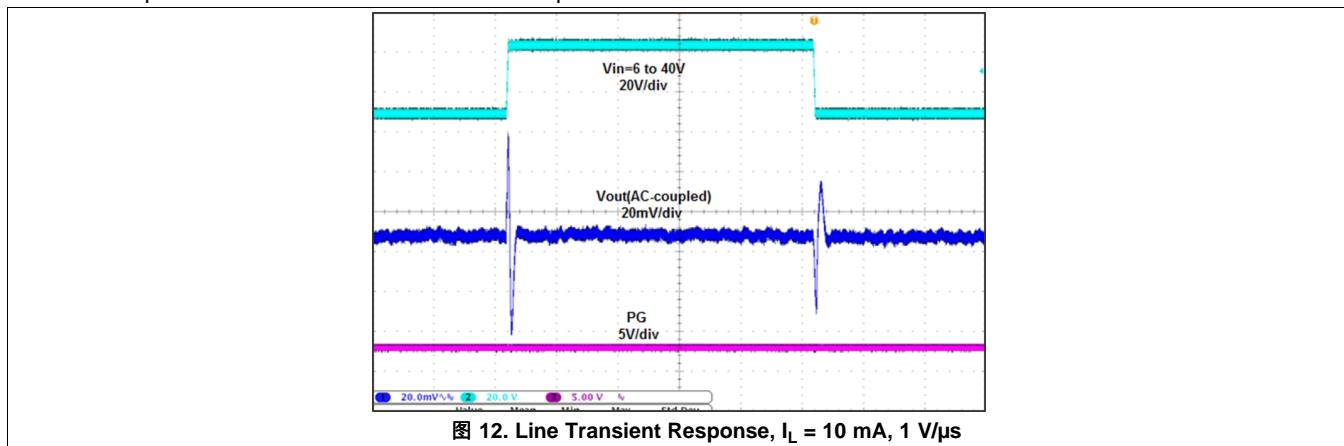


All oscilloscope waveforms were taken at room temperature.



## Typical Characteristics (接下页)

All oscilloscope waveforms were taken at room temperature.



## 7 Detailed Description

### 7.1 Overview

This product is a combination of a low-dropout linear regulator with reset function. The power-on reset initializes once the  $V_{out}$  output exceeds 91.6% of the target value. The power-on-reset delay is a function of the value set by an external capacitor on the CT pin before releasing the PG pin high.

### 7.2 Functional Block Diagram

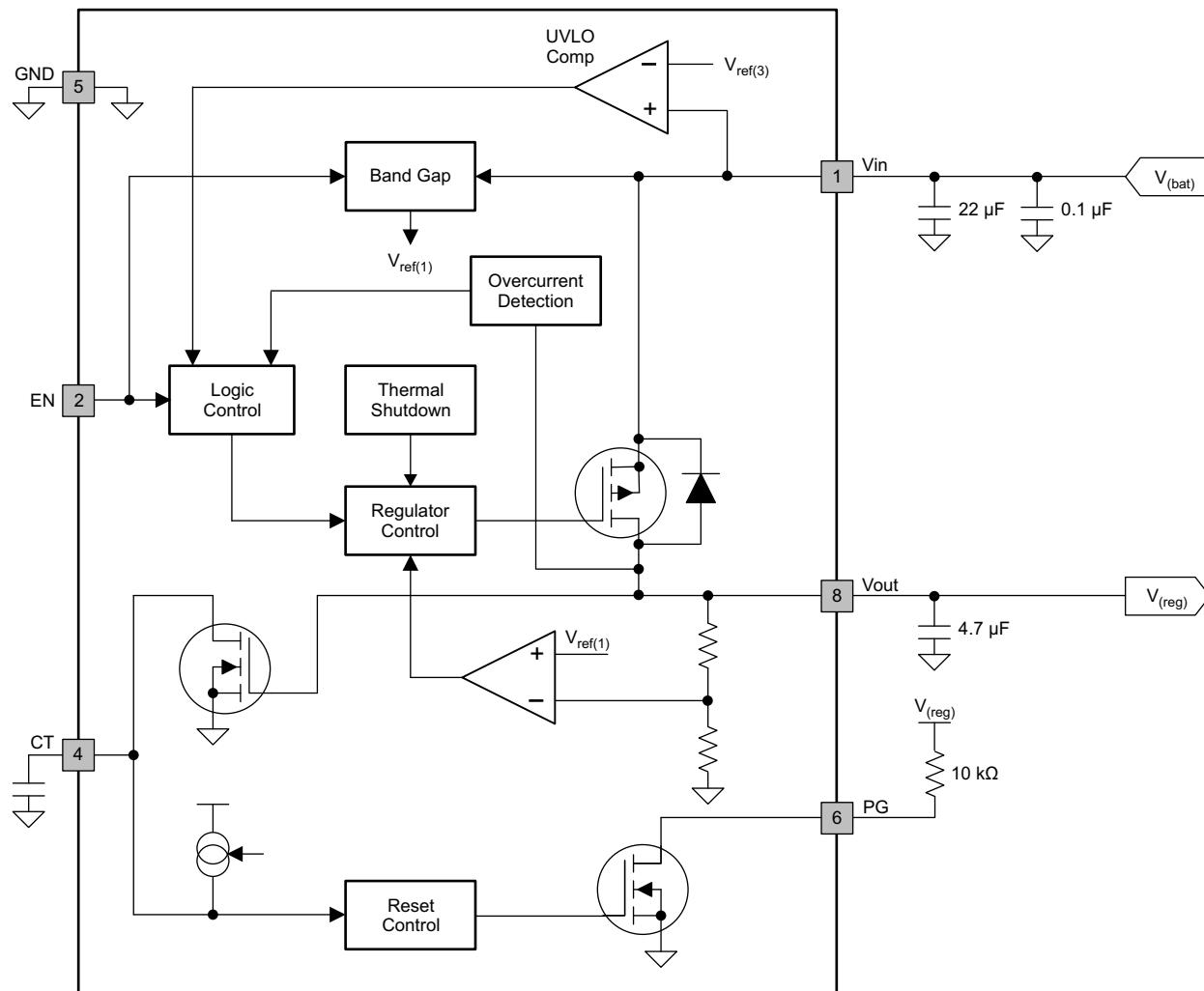


图 13. TPS7A6650H-Q1 Functional Block Diagram

### 7.3 Feature Description

#### 7.3.1 Enable (EN)

This is a high-voltage-tolerant pin; high input activates the device and turns the regulator ON. One can connect this input to the  $V_{in}$  pin for self-bias applications.

#### 7.3.2 Regulated Output ( $V_{out}$ )

This is the regulated output based on the required voltage. The output has current limitation. During initial power up, the regulator has a soft start incorporated to control initial current through the pass element and the output capacitor.

## Feature Description (接下页)

In the event the regulator drops out of regulation, the output tracks the input minus a drop based on the load current. When the input voltage drops below the UVLO threshold, the regulator shuts down until the input voltage recovers above the minimum start-up level.

### 7.3.3 Power-On Reset (PG)

This is an output with an external pullup resistor to the regulated supply. The output remains low until the regulated  $V_{out}$  has exceeded approximately 90% of the set value and the power-on-reset delay has expired. The on-chip oscillator presets the delay. The regulated output falling below the 90% level asserts this output low after a short de-glitch time of approximately 250  $\mu$ s (typical).

### 7.3.4 Reset Delay Timer (CT)

An external capacitor on this pin sets the timer delay before the reset pin is asserted high. The constant output current charges an external capacitor until the voltage exceeds a threshold to trip an internal comparator. If this pin is open, the default delay time is 290  $\mu$ s (typ). After releasing the PG pin high, the capacitor on this pin discharges, thus allowing the capacitor to charge from approximately 0.2 V for the next power-on-reset delay-timer function.

An external capacitor, CT, defines the reset-pulse delay time,  $t_{(POR)}$ , with the charge time of:

$$t_{(POR)} = \frac{C_{(CT)} \times 1\text{ V}}{1\text{ }\mu\text{A}} \quad (1)$$

The power-on reset initializes once the output  $V_{(Vout)}$  exceeds 91.6% of the programmed value. The power-on-reset delay is a function of the value set by an external capacitor on the CT pin before the releasing of the PG pin high.

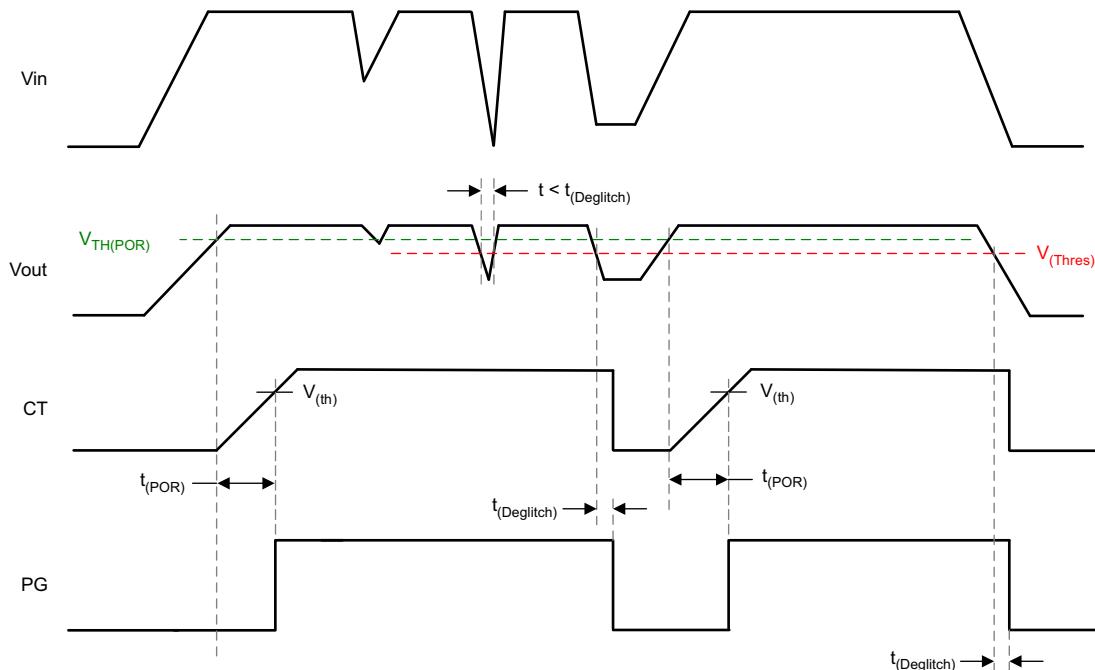


图 14. Conditions for Activation of Reset

## Feature Description (接下页)

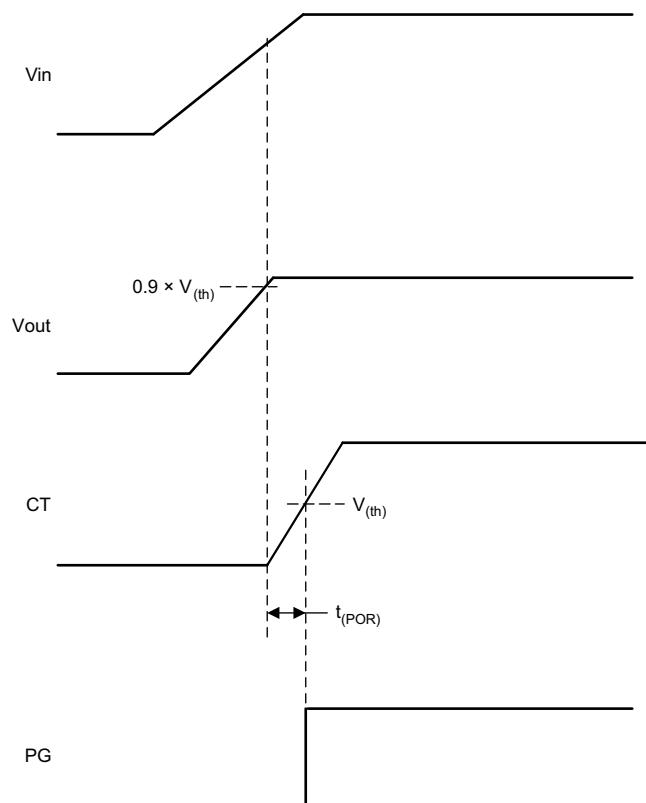


图 15. External Programmable Reset Delay

### 7.3.5 Undervoltage Shutdown

There is an internally fixed undervoltage shutdown threshold. Undervoltage shutdown activates when the input voltage on Vin drops below  $V_{(VinUVLO)}$ . This ensures the regulator is not latched into an unknown state during low input supply voltage. If the input voltage has a negative transient which drops below the UVLO threshold and recovers, the regulator shuts down and powers up with a normal power-up sequence once the input voltage is above the required levels.

### 7.3.6 Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation and the output voltage tracks input minus a voltage based on the load current ( $I_o$ ) and switch resistance ( $R_{sw}$ ). This allows for a smaller input capacitor and can possibly eliminate the need of using a boost convertor during cold-crank conditions.

### 7.3.7 Thermal Shutdown

These devices incorporate a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature falls below the TSD trip point, the output turns on again.

Thermal protection disables the output when the junction temperature rises to approximately 175°C, allowing the device to cool. Cooling of the junction temperature to approximately 155°C enables the output circuitry. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

## Feature Description (接下页)

The purpose of the design of the internal protection circuitry of the TPS7A6650H-Q1 is for protection against overload conditions, not as a replacement for proper heat-sinking. Continuously running the TPS7A6650H-Q1 device into thermal shutdown degrades device reliability.

## 7.4 Device Functional Modes

### 7.4.1 Operation With $V_{(VIN)} < 4$ V

The devices operate with input voltages above 4 V. The maximum UVLO voltage is 2.6 V, and the devices operate at an input voltage above 4 V. The devices can also operate at lower input voltages; no minimum UVLO voltage is specified. At input voltages below the actual UVLO voltage, the devices do not operate.

### 7.4.2 Operation With EN Control

The enable rising edge threshold voltage is 1.7 V (maximum). With the EN pin held above that voltage and the input voltage above 4 V, the device becomes active. The enable falling edge is 0.4 V (minimum). Holding the EN pin below that voltage disables the device, thus reducing the IC quiescent current.

## 8 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TPS7A6650H-Q1 device is a 150-mA low-dropout linear regulator designed for up to 40-V Vin operation with only 12- $\mu$ A quiescent current at no load.

### 8.2 Typical Application

图 16 shows a typical application circuits for the TPS7A6650H-Q1. One may use different values of external components, depending on the end application. An application may require a larger output capacitor during fast load steps in order to prevent reset from occurring. TI recommends a low-ESR ceramic capacitor with dielectric of type X7R or X8R.

#### 8.2.1 TPS7A6650H-Q1 Typical Application

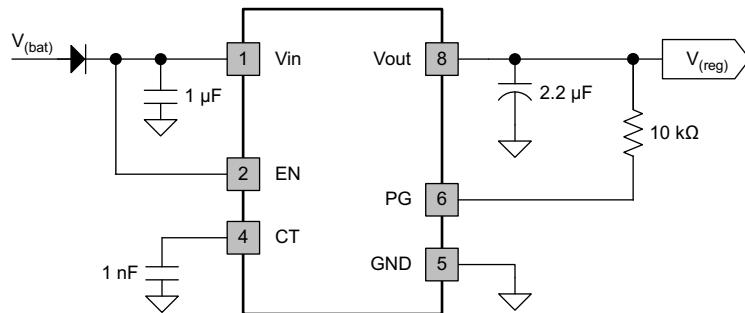


图 16. Typical Application Schematic for TPS7A6650H-Q1

##### 8.2.1.1 Design Requirements

For this design example, use the parameters listed in 表 1 as the design parameters.

表 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	4 V to 40 V
Output voltage	5 V
Output current rating	50 mA
Output capacitor range	2.2 $\mu\text{F}$ to 100 $\mu\text{F}$
Output capacitor ESR range	1 m $\Omega$ to 2 $\Omega$
CT capacitor range	100 pF to 100 nF

### 8.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current rating
- Input capacitor
- Output capacitor
- Power-up-reset delay time

#### 8.2.1.2.1 Input Capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. The typical recommended value for the decoupling capacitor is 10  $\mu$ F. The voltage rating must be greater than the maximum input voltage.

#### 8.2.1.2.2 Output Capacitor

The device requires an output capacitor to stabilize the output voltage. The capacitor value should be between 2.2  $\mu$ F and 100  $\mu$ F. The ESR range should be between 1 m $\Omega$  and 2  $\Omega$ . TI recommends selecting a ceramic capacitor with low ESR to improve the load transient response.

#### 8.2.1.3 Application Performance Plot

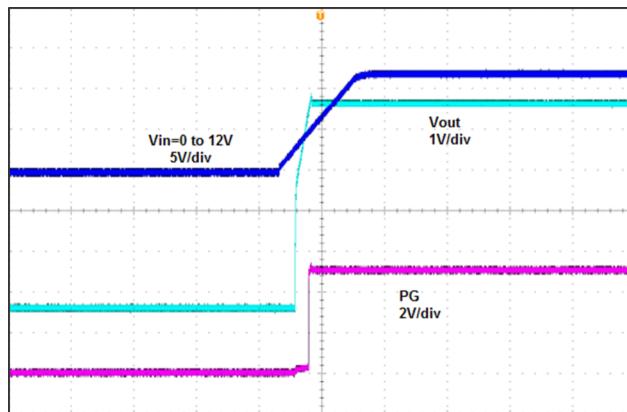


图 17. Power Up (5 V), 20 ms/div,  $I_L = 20$  mA

## 9 Power Supply Recommendations

Design of the device is for operation from an input voltage supply with a range between 4 V and 28 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7A6650H-Q1 device, TI recommends adding an electrolytic capacitor with a value of 22  $\mu$ F and a ceramic bypass capacitor at the input.

## 10 Layout

### 10.1 Layout Guidelines

#### 10.1.1 Package Mounting

Solder pad footprint recommendations for the TPS7A6650H-Q1 are available at the end of this product data sheet and at [www.ti.com](http://www.ti.com).

#### 10.1.2 Board Layout Recommendations to Improve PSRR and Noise Performance

For the layout of TPS7A6650H-Q1, place the input and output capacitors close to the devices as shown in [图 18](#). In order to enhance the thermal performance, TI recommends surrounding the device with some vias.

To improve ac performance such as PSRR, output noise, and transient response, TI recommends a board design with separate ground planes for  $V_{in}$  and  $V_{out}$ , with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Minimize equivalent series inductance (ESL) and ESR in order to maximize performance and ensure stability. Place every capacitor as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. TI strongly discourages the use of vias and long traces because they may impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance specified in this product data sheet, use the same layout pattern used for the TPS7A6650H-Q1 evaluation board, available at [www.ti.com](http://www.ti.com).

### 10.2 Layout Example

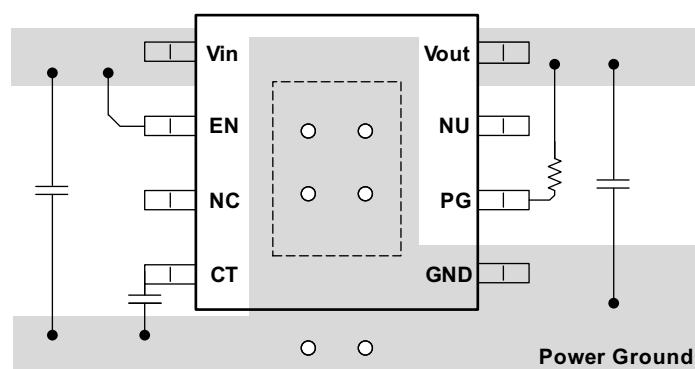


图 18. TPS7A6650H-Q1 Board Layout Diagram

### 10.3 Power Dissipation and Thermal Considerations

Calculate power dissipated in the device using [公式 2](#).

$$P_D = I_O \times (V_{(Vin)} - V_{(Vout)}) + I_{(q)} \times V_{(Vin)} \quad (2)$$

where:

$P_D$  = continuous power dissipation

$I_O$  = output current

$V_{(Vin)}$  = input voltage

$V_{(Vout)}$  = output voltage

As  $I_{(q)} \ll I_O$ , therefore ignore the term  $I_{(q)} \times V_{(Vin)}$  in [公式 2](#).

For a device under operation at a given ambient air temperature ( $T_A$ ), calculate the junction temperature ( $T_J$ ) using [公式 3](#).

## Power Dissipation and Thermal Considerations (接下页)

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (3)$$

where:

$R_{\theta JA}$  = junction-to-ambient air thermal impedance

$$\Delta T = T_J - T_A = (R_{\theta JA} \times P_D) \quad (4)$$

## 11 器件和文档支持

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.1 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 11.2 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时, 应将导线一起截短或将装置放置于导电泡棉中, 以防止 MOS 门极遭受静电损伤。

### 11.3 Glossary

[SLYZ022](#) — *TI Glossary.*

This glossary lists and explains terms, acronyms, and definitions.

## 12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。本数据随时可能发生变更并且不对本文档进行修订, 恕不另行通知。要获得这份数据表的浏览器版本, 请查阅左侧的导航窗格。

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A6650HQDGNRQ1	Active	Production	HVSSOP (DGN)   8	2500   LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	13LV
TPS7A6650HQDGNRQ1.A	Active	Production	HVSSOP (DGN)   8	2500   LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	13LV

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

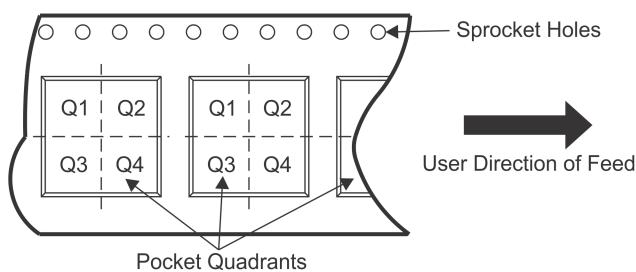
**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A6650HQDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A6650HQDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0

## 重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 [TI 销售条款](#)、[TI 通用质量指南](#) 或 [ti.com](#) 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2025，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月