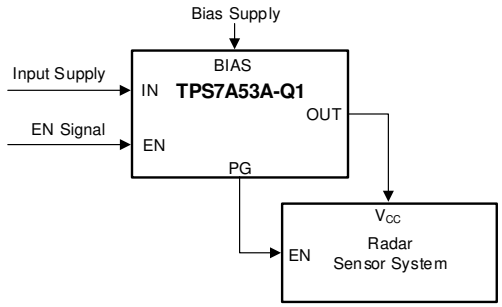
TPS7A53A-Q1 3A 高精度汽车级低噪声 LDO 稳压器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 温度等级 1：–40°C ≤ T_A ≤ +125°C
  - HBM ESD 分类等级 2
  - CDM ESD 分类等级 C4A
- 扩展结温 (T_J) 范围：
  - –40°C 至 +150°C
- 输入电压范围：
  - IN: V_{IN} + V_{DO} 至 6.0V
  - BIAS：V_{OUT} + $V_{DO(BIAS)}$ 至 6.0V
- 低压降：130 mV (3 A)
- 输出电压噪声：5.6μV_{RMS}
- 整个线路、负载和温度范围内的精度：
  - 1.3%（最大值）
- 电源纹波抑制：
  - 500kHz 时为 40dB
- 可调软启动浪涌控制
- 开漏电源正常 (PG) 输出
- 封装：
  - 具有可湿侧面和高 CTE (12ppm/°C) 塑封料的 4mm × 4mm 20 引脚 WQFN

2 应用

- 远程信息处理控制单元
- 信息娱乐系统与仪表组
- 成像雷达



为射频组件供电

3 说明

TPS7A53A-Q1 是一款低噪声 (5.6μV_{RMS})、低压降线性稳压器 (LDO)，可提供 3A 拉电流，压降仅为 130mV。

TPS7A53A-Q1 集低噪声 (5.6μV_{RMS})、高 PSRR 和高输出电流能力等特性于一体，设计用于为雷达电源和信息娱乐等应用中的噪声敏感型组件供电。此器件的优秀性能可抑制电源产生的相位噪声和时钟抖动，适合为射频放大器、雷达传感器和芯片组供电。具体而言，信号链元件将受益于器件的高性能。TPS7A53A-Q1 还提供可湿侧面选项，方便进行光学检查。

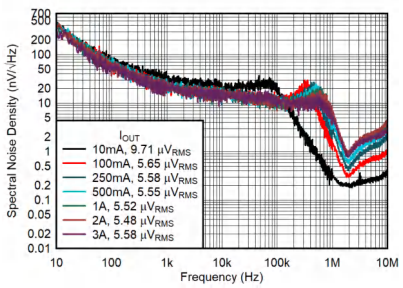
对于需要以低输入和低输出 (LILO) 电压运行的数字负载（例如应用特定集成电路 (ASIC)、现场可编程门阵列 (FPGA) 和数字信号处理器 (DSP)），TPS7A53A-Q1 所具备的出色精度（在负载和温度范围内可达 1.3%）、遥感功能、出色的瞬态性能和软启动功能可实现出色的系统性能。

TPS7A53A-Q1 器件的多功能性使其适用于许多严苛应用。

封装信息(1)

器件型号	封装	封装尺寸（标称值）
TPS7A53A-Q1	具有可湿侧面的 RTJ (WQFN、20)	4.00mm × 4.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。



频谱噪声密度与频率和输出电流

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

Changes from Revision * (November 2022) to Revision A (December 2022)	Page
• 将文档状态从*预告信息*更改为*量产数据*	1

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5 Pin Configuration and Functions

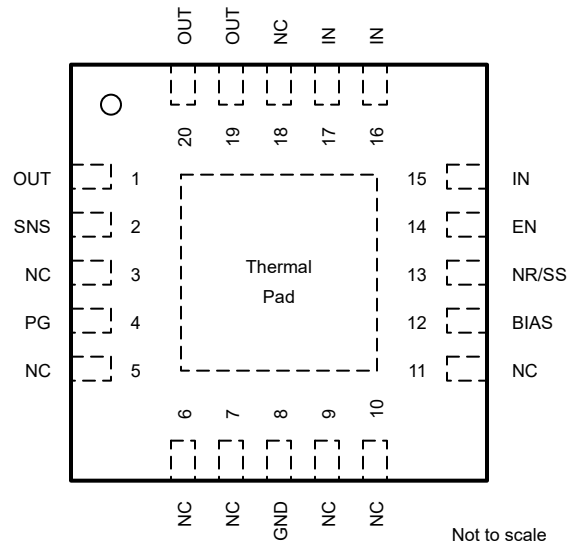


图 5-1. RTJ Package (Fixed), 4-mm × 4-mm, 20-Pin WQFN (Top View)

表 5-1. Pin Functions

PIN			DESCRIPTION
NAME	RTJ (Fixed)	TYPE	
BIAS	12	I	BIAS supply voltage. This pin enables the use of low-input voltage, low-output (LILO) voltage conditions (that is, V_{IN} = 1.3 V, V_{OUT} = 1 V) to reduce power dissipation across the die. Using a BIAS voltage improves dc and ac performance for $V_{IN} \leqslant$ 2.2 V. A 0.1-µF capacitor or larger must be connected between this pin and ground.
EN	14	I	Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device. If enable functionality is not required, this pin must be connected to IN or BIAS.
FB	—	I	Feedback pin connected to the error amplifier. Although not required, a 10-nF, feed-forward capacitor from FB to OUT (as close to the device as possible) maximizes ac performance. Using a feed-forward capacitor can disrupt PG (power-good) functionality.
GND	8	—	Ground pin. This pin must be connected to ground and the thermal pad with a low-impedance connection.
IN	15-17	I	Input supply voltage pin. A 1-µF or larger ceramic capacitor (0.5 µF or greater of capacitance) from IN to ground reduces the impedance of the input supply. Place the input capacitor as close to the input as possible.
NC	3, 5, 6, 7, 9, 10,11, 18	—	No internal connection.
SS	13	—	Noise-reduction and soft-start pin. Connecting an external capacitor between this pin and ground enables the soft-start function.
OUT	1, 19, 20	O	Regulated output pin. A 10-µF or larger ceramic capacitor (5 µF or greater of capacitance) from OUT to ground is required for stability and must be placed as close to the output as possible. Minimize the impedance from the OUT pin to the load.
PG	4	O	Active-high, power-good pin. An open-drain output indicates when the output voltage reaches $V_{IT(PG)}$ of the target. The use of a feed-forward capacitor can disrupt PG (power-good) functionality.
SNS	2	I	Sense pin connected to the error amplifier.
Thermal pad		—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	IN, BIAS, PG, EN	–0.3	6.5	V
	OUT	–0.3	V_{IN} + 0.3	V
	SS, FB	–0.3	6.5	V
Current	OUT	Internally limited		mA
	PG (sink current into device)	0	1.5	
Temperature	Junction, T_J	–40	150	°C
	Storage, T_{stg}	–55	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC specification Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	V_{OUT} + V_{DO} (IN)		6.0	V
V_{EN}	Enable supply voltage			6.0	V
V_{BIAS}	BIAS supply voltage	V_{OUT} + V_{DO} (BIAS)(1)		6.0	V
V_{OUT}	Output voltage	0.8		V_{IN} - V_{DO}	V
I_{OUT}	Output current	0		3	A
C_{OUT}	Output capacitor (3)	10			µF
C_{IN}	Input capacitor (1) (2)	1			µF
C_{BIAS}	Bias capacitor	0.1	1		µF
C_{SS}	Soft-start capacitor	0	10	100	nF
T_J	Operating junction temperature	–40		150	℃

(1) V_{BIAS} has a minimum voltage of 1.7 V or V_{OUT} + V_{DO} (V_{BIAS}), whichever is higher.
(2) If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for the supply is 4.7 µF.
(3) A maximum capacitor derating of 25% is considered for minimum capacitance.

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6.4 Thermal Information

THERMAL METRIC[1]		TPS7A53A-Q1 RTJ (VQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics

at V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{BIAS} = 0.1 µF, C_{IN} = C_{OUT} = 10 µF, C_{NR} = 1 nF, I_{OUT} = 50 mA, V_{BIAS} = 5.0 V [5], and T_J = –40°C to 150°C (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Internal reference	Fixed 1 V only		1.0		V
$V_{NR/SS}$	NR/SS pin voltage	Fixed 1 V only [4]		1		V
$V_{BIAS(UVLO)}$	Rising bias supply UVLO			1.4	1.8	V
$V_{BIAS(UVLO),HYST}$	Bias supply UVLO hysteresis		25	50	75	mV
ΔV_{OUT} / ΔV_{IN}	Accuracy [1] [6]	V_{OUT} + 2.5 V ≤ V_{BIAS} ≤ 5.5 V, 50 mA ≤ I_{OUT} ≤ 3 A, -40°C ≤ T_J ≤ 125°C	–1	±0.5	1	%
		V_{OUT} + 2.5 V ≤ V_{BIAS} ≤ 5.5 V, 50 mA ≤ I_{OUT} ≤ 3 A	–1.3	±0.5	1.3	
ΔV_{OUT} / ΔI_{OUT}	Line regulation	$V_{OUT(nom)}$ + 0.3 V ≤ V_{IN} ≤ 6.0 V		0.025		%/V
V_{OUT}	Load regulation	50 mA ≤ I_{OUT} ≤ 3 A		0.025		%/A
$V_{DO(IN)}$	V_{IN} dropout voltage[2]	I_{OUT} = 3 A, V_{BIAS} – $V_{OUT(nom)}$ ≥ 3.25 V[3], -40°C ≤ T_J ≤ 125°C		130	275	mV
		I_{OUT} = 3 A, V_{BIAS} – $V_{OUT(nom)}$ ≥ 3.25 V[3]		130	285	
$V_{DO(BIAS)}$	V_{BIAS} dropout voltage[2]	I_{OUT} = 3 A, V_{IN} = V_{BIAS}		1.4	1.9	V
I_{CL} (Fixed V_{OUT})	Fixed V_{OUT}, output current limit	V_{OUT} = 80% × $V_{OUT(nom)}$	4.0	4.7	5.5	A
I_{BIAS}	BIAS pin current	I_{OUT} = 50 mA		0.7	1.2	mA
I_{SHDN}	Shutdown supply current (I_{GND})	V_{EN} ≤ 0.4 V, V_{IN} = 1.25 V, V_{BIAS} = 6 V		1	25	µA
$I_{FB/SNS}$	Feedback/sense pin current		–0.3	0.12	0.3	µA
PSRR	Power-supply rejection (V_{IN} to V_{OUT})	1 kHz, I_{OUT} = 2 A, V_{IN} = 1.25 V, V_{OUT} = 1.0 V		70		dB
		3 MHz, I_{OUT} = 2 A, V_{IN} = 1.25 V, V_{OUT} = 1.0 V		27		dB
	Power-supply rejection (V_{BIAS} to V_{OUT})	1 kHz, I_{OUT} = 2 A, V_{IN} = 1.25 V, V_{OUT} = 1.0 V		65		dB
		3 MHz, I_{OUT} = 2 A, V_{IN} = 1.25 V, V_{OUT} = 1.0 V		28		dB
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, I_{OUT} = 2 A, C_{SS} = 1 nF		7		µVrms
t_{STR}	Minimum startup time	C_{SS} = 10 nF, V_{OUT} = 1.0 V		2		ms
I_{SS}	Soft-start charging current	t_{SS} = 4.8 x $V_{OUT(NOM)}$ / 0.8 V, V_{OUT} = 1.0 V		6		µA
$V_{EN(hi)}$	Enable input high level		1.1		5.5	V
$V_{EN(lo)}$	Enable input low level		0		0.4	V
$V_{EN(hys)}$	Enable pin hysteresis			70		mV

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6.5 Electrical Characteristics (continued)

at V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{BIAS} = 0.1 μF, C_{IN} = C_{OUT} = 10 μF, C_{NR} = 1 nF, I_{OUT} = 50 mA, V_{BIAS} = 5.0 V (5), and T_J = –40°C to 150°C (unless otherwise noted); typical values are at T_J = 25°C

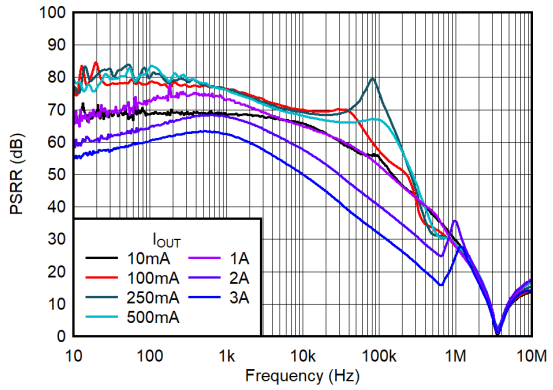
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{EN(dg)}$	Enable pin deglitch time			15		μs
I_{EN}	Enable pin current	V_{EN} = 5 V		0.1	0.25	μA
V_{IT}	PG trip threshold	V_{OUT} decreasing	85	90	94	%V_{OUT}
V_{HYS}	PG trip hysteresis			2.5		%V_{OUT}
$V_{PG(lo)}$	PG output low voltage	I_{PG} = 1 mA (sinking), V_{OUT} < V_{IT}			0.3	V
$I_{PG(lkg)}$	PG leakage current	V_{PG} = 5.25 V, V_{OUT} > V_{IT}		0.001	0.05	μA
$R_{PULLDOWN}$	Output Pulldown resistor	V_{BIAS} = 5 V, V_{EN} = 0 V		0.5		kΩ
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		165		℃
		Reset, temperature decreasing		140		

(1) Adjustable devices tested at 0.8 V; resistor tolerance is not taken into account.
(2) Dropout is defined as the voltage from V_{IN} to V_{OUT} when V_{OUT} is 3% below nominal.
(3) 3.25 V is a test condition of this device and can be adjusted by referring to Figure 6.
(4) For fixed voltage, NR/SS voltage is equal to output voltage.
(5) V_{BIAS} = $V_{DO_MAX(BIAS)}$ + V_{OUT} for V_{OUT} ≥ 3.1V.
(6) The device is not tested under conditions where V_{IN} > V_{OUT} + 0.85 V and I_{OUT} = 3 A, because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply on any application condition that exceeds the power dissipation limit of the package under test.

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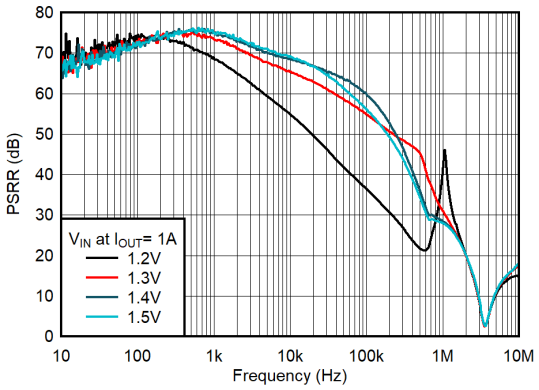
6.6 Typical Characteristics

at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.3 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted)



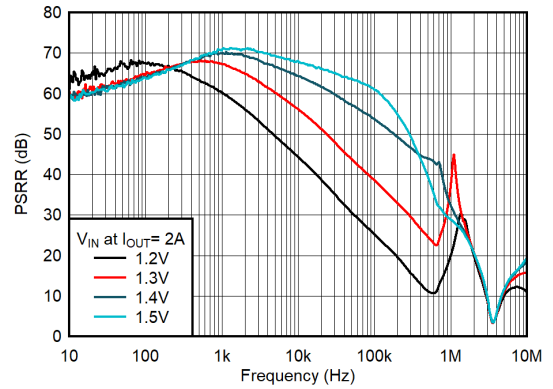
V_{IN} = 1.3 V, V_{BIAS} = 5 V, V_{OUT} = 1.0 V, C_{OUT} = 10 µF, C_{BIAS} = 0.1 µF, C_{SS} = 10 nF

图 6-1. PSRR vs Frequency and I_{OUT}



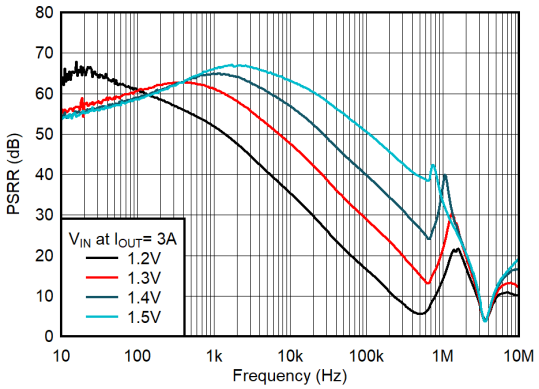
I_{OUT} = 1 A, V_{BIAS} = 5 V, V_{OUT} = 1.0 V, C_{OUT} = 10 µF, C_{BIAS} = 0.1 µF, C_{SS} = 10 nF

图 6-2. PSRR vs Frequency and V_{IN} for I_{OUT} = 1 A



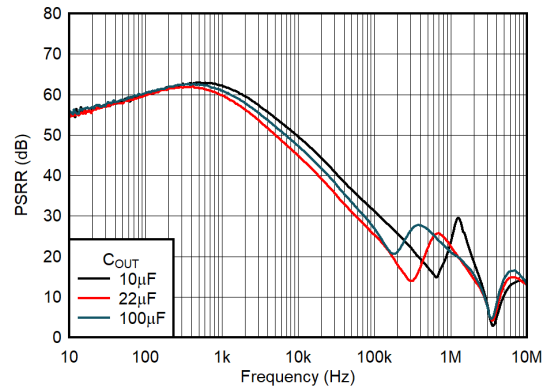
I_{OUT} = 2 A, V_{BIAS} = 5 V, V_{OUT} = 1.0 V, C_{OUT} = 10 µF, C_{BIAS} = 0.1 µF, C_{SS} = 10 nF

图 6-3. PSRR vs Frequency and V_{IN} for I_{OUT} = 2 A



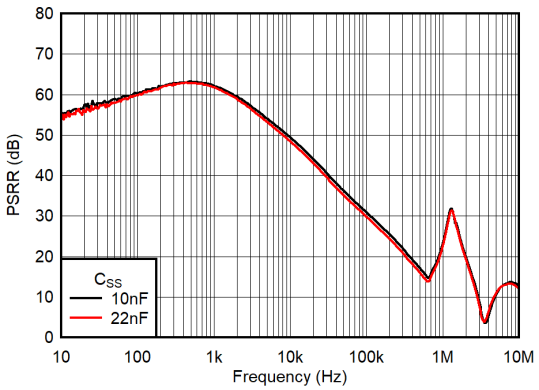
I_{OUT} = 3 A, V_{BIAS} = 5 V, V_{OUT} = 1.0 V, C_{OUT} = 10 µF, C_{BIAS} = 0.1 µF, C_{SS} = 10 nF

图 6-4. PSRR vs Frequency and V_{IN} for I_{OUT} = 3 A



I_{OUT} = 3 A, V_{BIAS} = 5 V, V_{OUT} = 1.0 V, C_{BIAS} = 0.1 µF, C_{SS} = 10 nF

图 6-5. PSRR vs Frequency and C_{OUT}



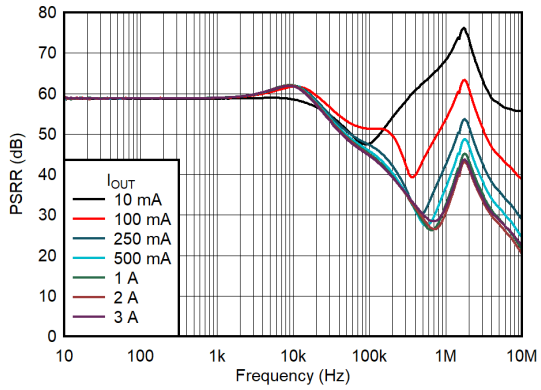
I_{OUT} = 3 A, V_{BIAS} = 5 V, V_{OUT} = 1.0 V, C_{BIAS} = 0.1 µF, C_{OUT} = 10 µF

图 6-6. PSRR vs Frequency and C_{SS}

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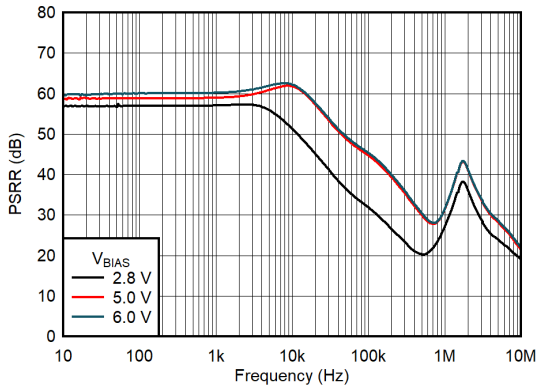
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.3 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted)



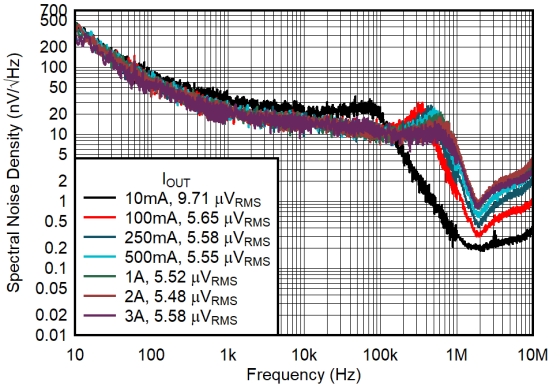
V_{IN} = V_{EN} = 1.3 V, V_{BIAS} = 5 V, V_{OUT} = 1.0 V, C_{IN} = 10 µF, C_{OUT} = 10 µF, C_{SS} = 10 nF

图 6-7. BIAS PSRR vs Frequency and I_{OUT}



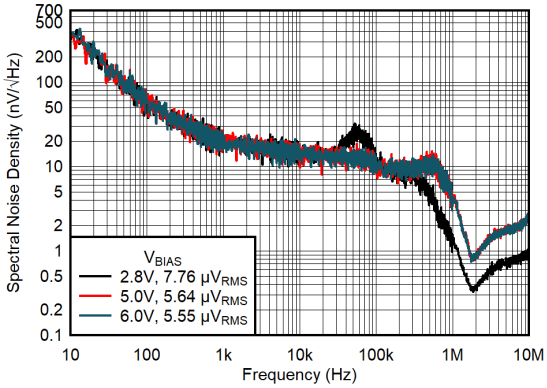
V_{IN} = V_{EN} = 1.3 V, V_{OUT} = 1.0 V, C_{IN} = 10 µF, C_{OUT} = 10 µF, C_{SS} = 10 nF

图 6-8. BIAS PSRR vs Frequency and V_{BIAS}



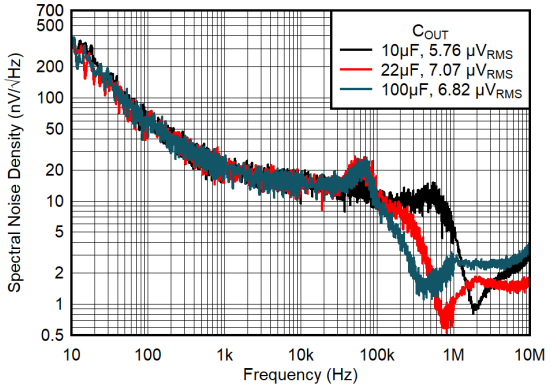
V_{IN} = 1.3 V, V_{OUT} = 1.0 V, V_{BIAS} = 5 V, C_{OUT} = 10 µF, C_{SS} = 10 nF, C_{BIAS} = 0.1 µF, RMS noise BW = 10 Hz to 100 kHz

图 6-9. Spectral Noise Density vs Frequency and I_{OUT}



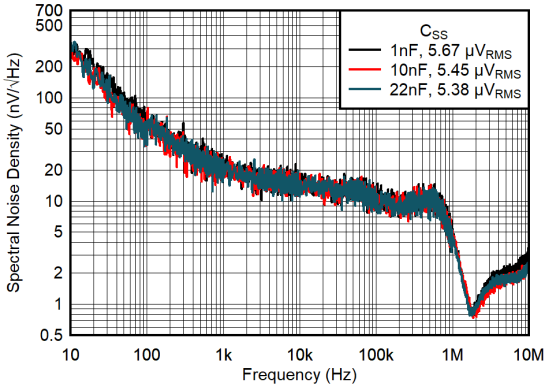
V_{IN} = 1.3 V, V_{OUT} = 1.0 V, C_{OUT} = 10 µF, C_{SS} = 10 nF, C_{BIAS} = 0.1 µF, RMS noise BW = 10 Hz to 100 kHz

图 6-10. Spectral Noise Density vs Frequency and V_{BIAS}



V_{IN} = 1.3 V, V_{OUT} = 1.0 V, V_{BIAS} = 5 V, C_{SS} = 10 nF, C_{BIAS} = 0.1 µF, RMS noise BW = 10 Hz to 100 kHz

图 6-11. Spectral Noise Density vs Frequency and C_{OUT}



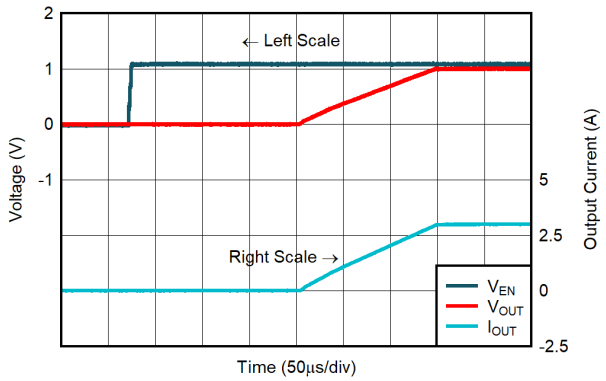
V_{IN} = 1.3 V, V_{OUT} = 1.0 V, V_{BIAS} = 5 V, C_{OUT} = 10 µF, C_{BIAS} = 0.1 µF, RMS noise BW = 10 Hz to 100 kHz

图 6-12. Spectral Noise Density vs Frequency and C_{SS}

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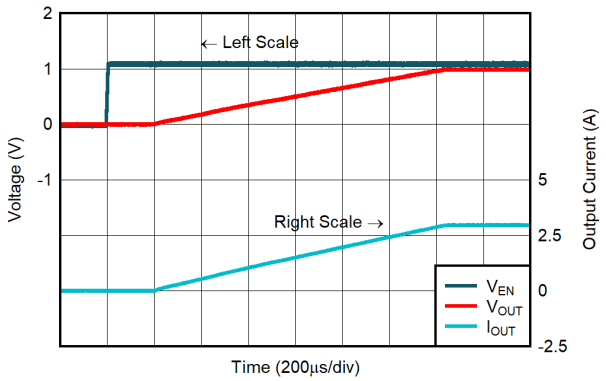
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.3 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted)



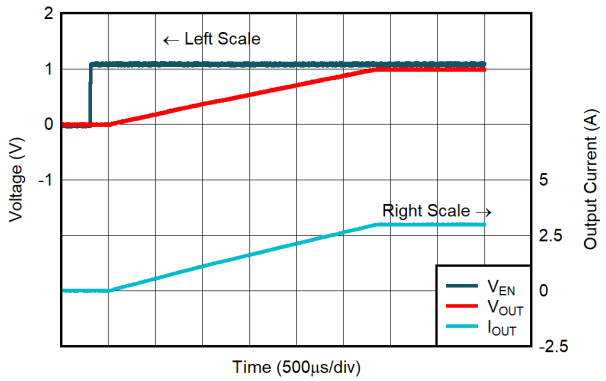
V_{IN} = 1.3 V, V_{OUT} = 1.0 V, V_{BIAS} = 5.0 V, I_{OUT} = 3 A, C_{OUT} = 10 µF, C_{SS} = 1 nF

图 6-13. Start-Up Waveform for C_{SS} = 1 nF



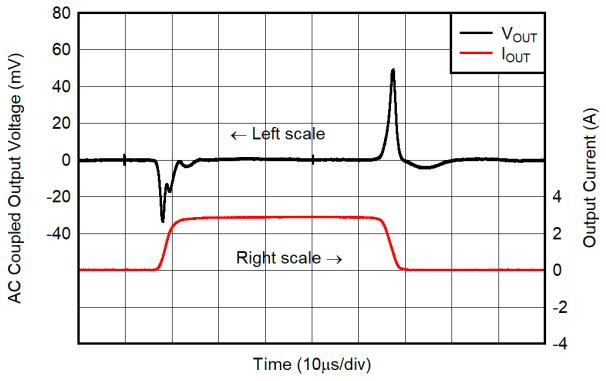
V_{IN} = 1.3 V, V_{OUT} = 1.0 V, V_{BIAS} = 5.0 V, I_{OUT} = 3 A, C_{OUT} = 10 µF, C_{SS} = 10 nF

图 6-14. Start-Up Waveform vs Time for C_{SS} = 10 nF



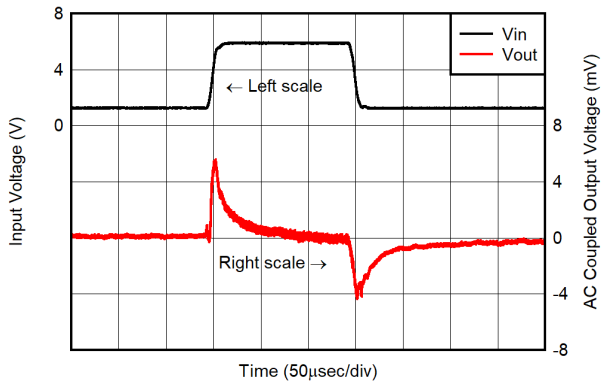
V_{IN} = 1.3 V, V_{OUT} = 1.0 V, V_{BIAS} = 5.0 V, I_{OUT} = 3 A, C_{OUT} = 10 µF, C_{SS} = 22 nF

图 6-15. Start-Up Waveform for C_{SS} = 22 nF



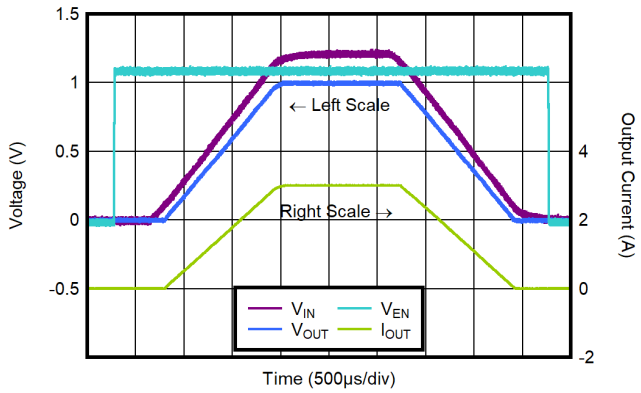
V_{IN} = V_{OUT} + 0.3 V, V_{BIAS} = V_{EN} = 5 V, $I_{OUT, DC}$ = 10 mA, slew rate = 1 A/µs, C_{SS} = 10 nF, C_{OUT} = 10 µF

图 6-16. Load Transient for V_{OUT} With Bias



$I_{OUT, DC}$ = 1.5 A, C_{OUT} = 10 µF, C_{SS} = C_{FF} = 10 nF, slew rate = 1 A/µs

图 6-17. Line Transient for V_{OUT} With Bias



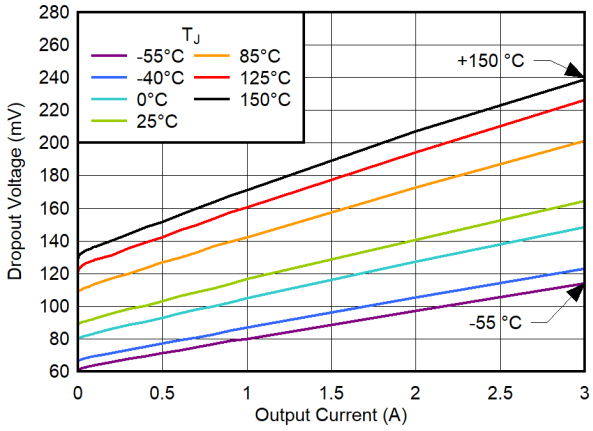
V_{BIAS} = 5 V, I_{OUT} = 3 A, C_{OUT} = 10 µF, C_{SS} = 10 nF

图 6-18. Input Ramp Response

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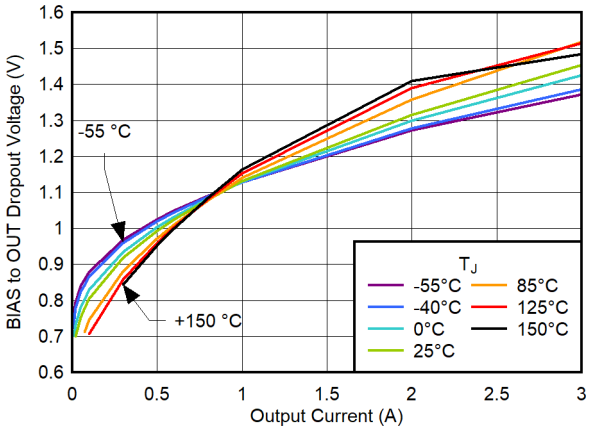
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.3 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted)



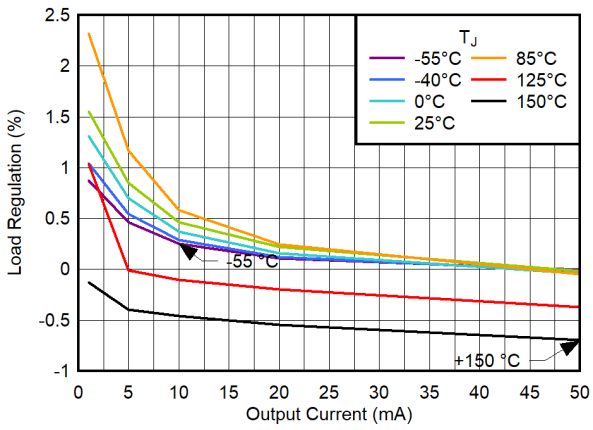
V_{BIAS} = 5 V, V_{OUT} = 1.0 V

图 6-19. IN-to-OUT Dropout Voltage vs Output Current



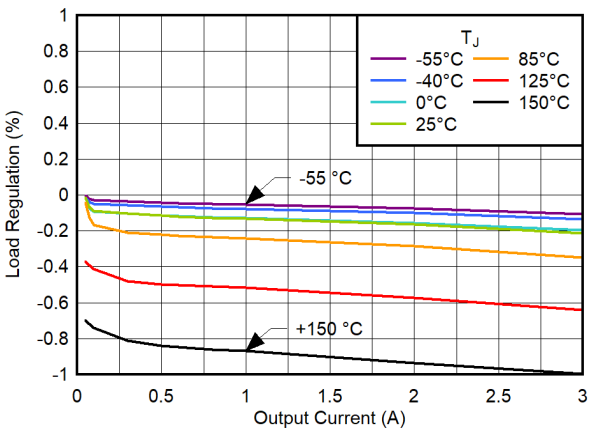
V_{IN} = 1.25 V, V_{OUT} = 1 V

图 6-20. BIAS-to-OUT Dropout Voltage vs Output Current



V_{IN} = 1.25 V, V_{BIAS} = 5 V, V_{OUT} = 1.0 V

图 6-21. Load Regulation vs 0-mA to 50-mA Output Current



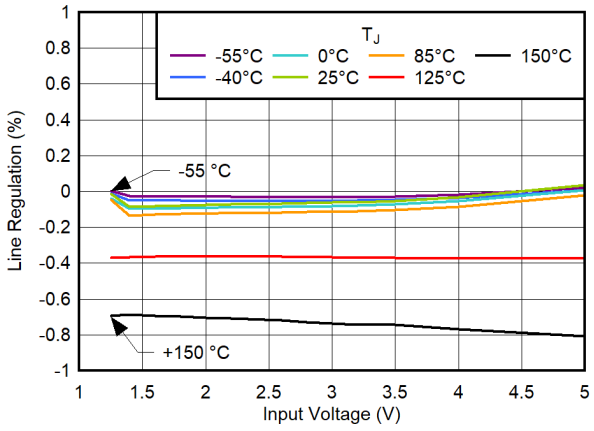
V_{IN} = 1.25 V, V_{OUT} = 1.0 V, V_{BIAS} = 5 V

图 6-22. Load Regulation vs ⩾50-mA Output Current

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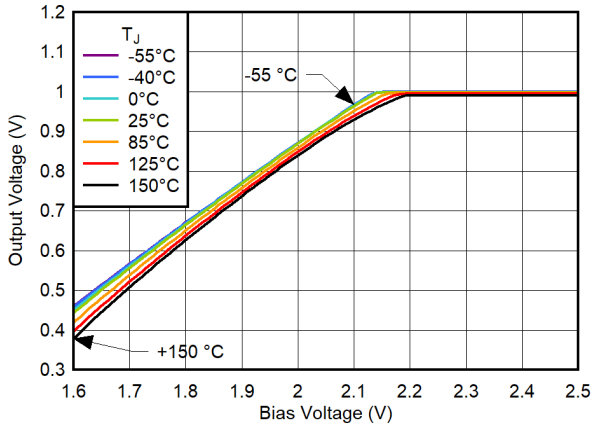
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.3 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted)



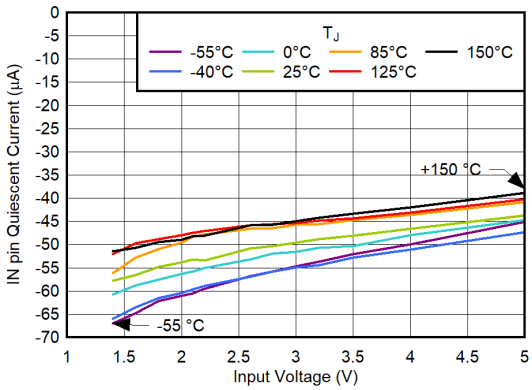
V_{OUT} = 1.0 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA

图 6-23. Line Regulation vs Input Voltage



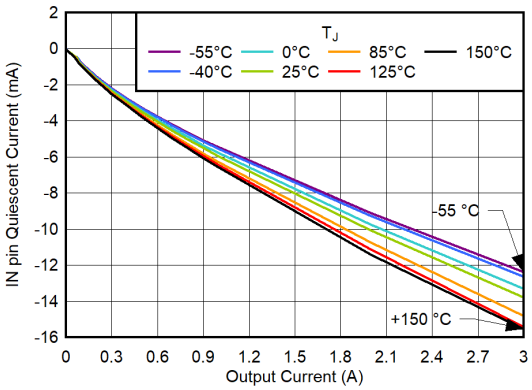
V_{IN} = 5 V, V_{OUT} = 1.0 V, I_{OUT} = 50 mA

图 6-24. Output Voltage vs Bias Voltage



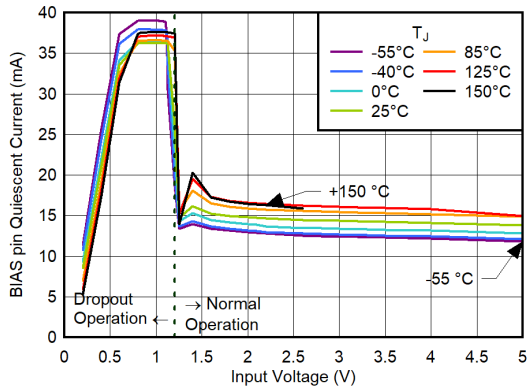
V_{OUT} = 1.0 V, V_{BIAS} = 5.0 V, I_{OUT} = 50 mA

图 6-25. IN Pin Quiescent Current vs Input Voltage



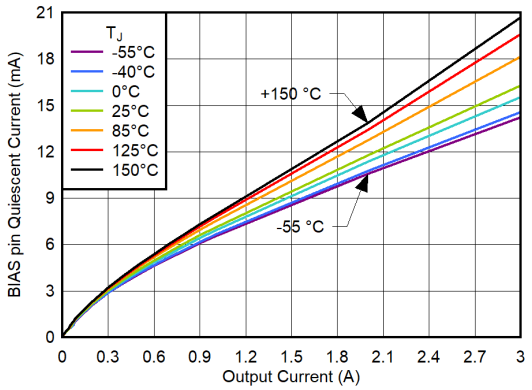
V_{OUT} = 1.0 V, V_{BIAS} = 5.0 V

图 6-26. IN Pin Quiescent Current vs Output Current



V_{OUT} = 1.0 V, V_{BIAS} = 5.0 V, I_{OUT} = 3 A

图 6-27. BIAS Pin Quiescent Current vs Input Voltage



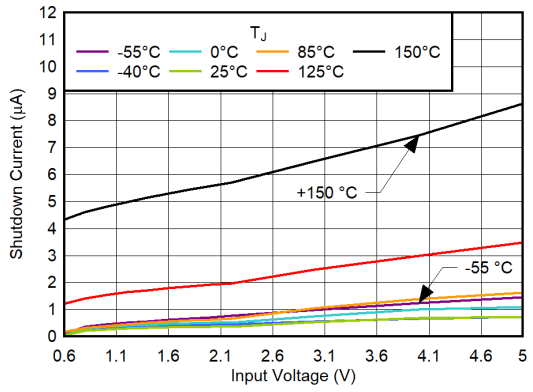
V_{IN} = 1.25 V, V_{BIAS} = 5.0 V, V_{OUT} = 1.0 V

图 6-28. BIAS Pin Quiescent Current vs Output Current

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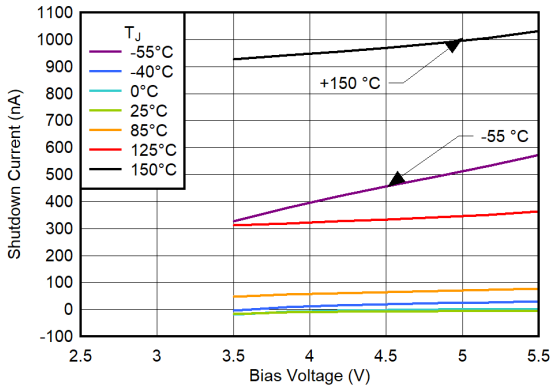
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.3 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted)



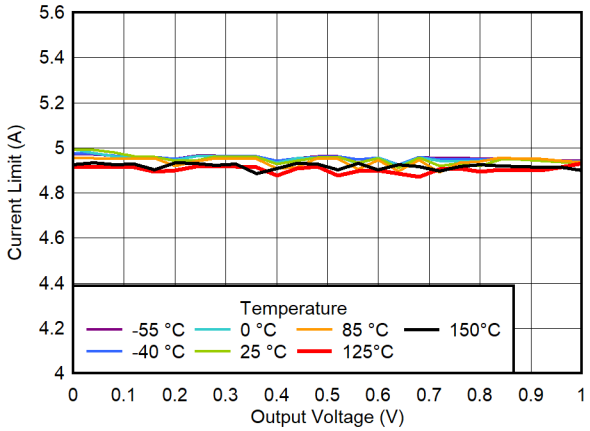
V_{BIAS} = 5 V, V_{EN} = 0 V

图 6-29. Shutdown Current (GND Pin) vs Input Voltage



V_{IN} = 1.25 V, V_{EN} = 0 V

图 6-30. Shutdown Current (GND Pin) vs Bias Voltage



Temperature limited because of power dissipation

图 6-31. Current Limit vs Output Voltage

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7 Detailed Description

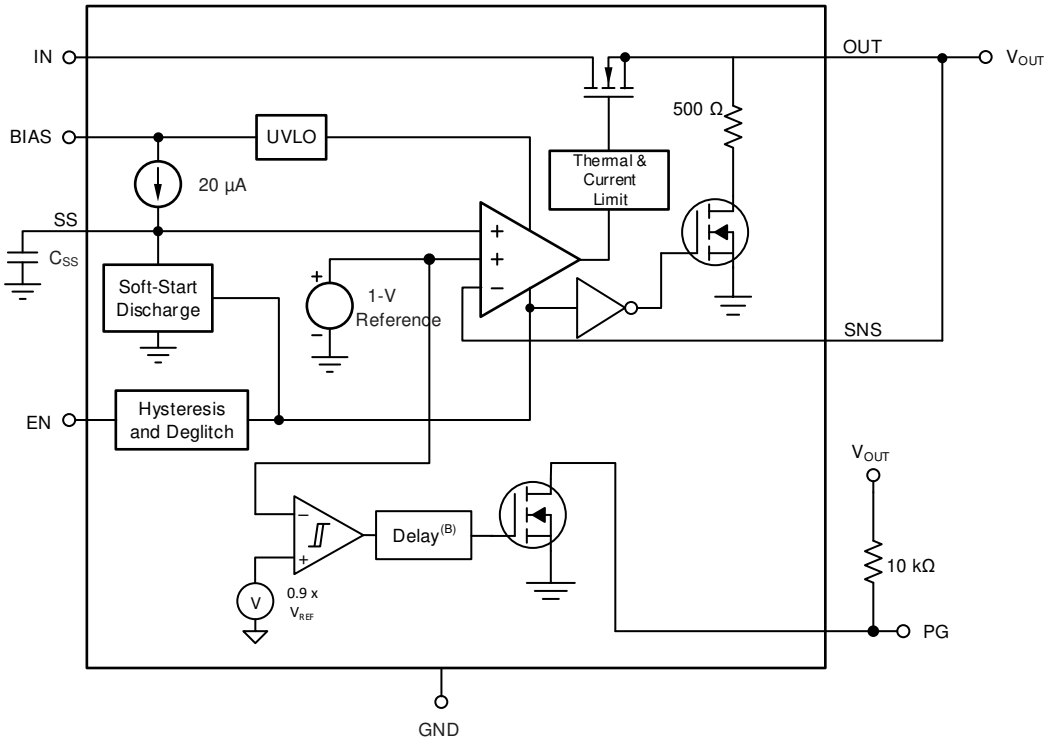
7.1 Overview

The TPS7A53A-Q1 is a low-input, low-output (LILO), low-quiescent-current linear regulator optimized to support excellent transient performance. This regulator uses a low-current bias rail to power all internal control circuitry, allowing the n-type field effect transistor (NMOS) pass transistor to regulate very-low input and output voltages.

Using an NMOS-pass transistor offers several critical advantages for many applications. Unlike a p-channel metal-oxide-semiconductor field effect transistor (PMOS) topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS7A53A-Q1 to be stable with any ceramic capacitor 10 μF or greater. Transient response is also superior to PMOS topologies, particularly for low V_{IN} applications.

The TPS7A53A-Q1 features a programmable, voltage-controlled, soft-start circuit that provides a smooth, monotonic start-up and limits start-up inrush currents that can be caused by large capacitive loads. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low V_{IN} and V_{OUT} capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often required by processor-intensive systems.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable and Shutdown

The enable (EN) pin is active high and compatible with standard digital-signaling levels. Setting V_{EN} below 0.4 V turns the regulator off, and setting V_{EN} above 1.1 V turns the regulator on. Unlike many regulators, the enable circuitry has hysteresis and deglitching for use with relatively slowly ramping analog signals. This configuration allows the device to be enabled by connecting the output of another supply to the EN pin. The enable circuitry typically has 70 mV of hysteresis and a deglitch circuit to help avoid on-off cycling as a result of small glitches in the V_{EN} signal.

The enable threshold is typically 0.75 V and varies with temperature and process variations. Temperature variation is approximately –1.2 mV/°C; process variation accounts for most of the remaining variation to the 0.4-V and 1.1-V limits. If precise turn-on timing is required, a fast rise-time signal must be used.

If not used, EN can be connected to BIAS. Place the connection as close as possible to the bias capacitor.

7.3.2 Active Discharge

The TPS7A53A-Q1 has an internal active pulldown circuits on the OUT pin.

This active discharge function uses an internal metal-oxide-semiconductor field-effect transistor (MOSFET) that connects a resistor ($R_{PULLDOWN}$) to ground when the low-dropout resistor (LDO) is disabled in order to actively discharge the output voltage. The active discharge circuit is activated when the device is disabled by driving EN to logic low, when the voltage at IN or BIAS is below the UVLO threshold, or when the regulator is in thermal shutdown.

The discharge time after disabling the device depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the pulldown resistor.

The active pulldown circuit connects the output to GND through a 500-Ω resistor when the device is disabled.

$$\tau_{OUT} = (500 \times R_L / (500 + R_L) \times C_{OUT} \quad (1)$$

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can flow from the output to the input and can cause damage to the device. Limit reverse current to no more than 5% of the device-rated current.

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7.3.3 Power-Good Output (PG)

The PG signal provides an easy solution to meet demanding sequencing requirements because PG signals when the output nears the nominal value. PG can be used to signal other devices in a system when the output voltage is near, at, or above the set output voltage ($V_{OUT(nom)}$). 图 7-1 shows a simplified schematic.

The PG signal is an open-drain digital output that requires a pullup resistor to a voltage source and is active high. The PG circuit sets the PG pin into a high-impedance state to indicate that the power is good.

Using a large feed-forward capacitor (C_{FF}) delays the output voltage and, because the PG circuit monitors the FB pin, the PG signal can indicate a false positive.

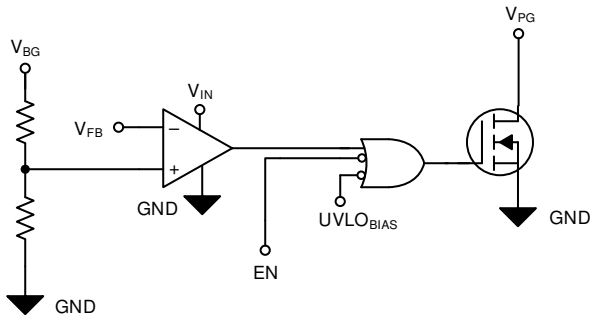


图 7-1. Simplified PG Circuit

7.3.4 Internal Current Limit

The device has an internal current-limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current when the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the *short-circuit current limit* (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK}$ is approximately 60% × $V_{OUT(nom)}$.

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The output voltage is not regulated when the device is in current limit. When a current-limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in a brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{SC}]. If thermal shutdown is triggered, the device turns off. When the device sufficiently cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note. 图 7-2 shows a diagram of the foldback current limit.

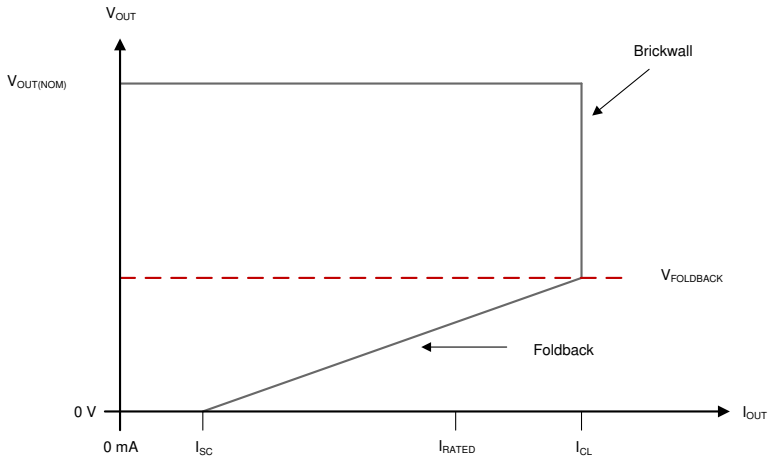


图 7-2. Foldback Current Limit

7.3.5 Thermal Shutdown Protection (T_{SD})

The internal thermal shutdown protection circuit disables the output when the thermal junction temperature (T_J) of the pass transistor rises to the thermal shutdown temperature threshold, $T_{SD(shutdown)\ (typical)}$. The thermal shutdown circuit hysteresis makes sure that the LDO resets (turns on) when the temperature falls to $T_{SD(reset)\ (typical)}$.

The thermal time constant of the semiconductor die is fairly short; thus, the device can cycle on and off when thermal shutdown is reached until the power dissipation is reduced. Power dissipation during start up can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the regulator into thermal shutdown, or above the maximum recommended junction temperature, reduces long-term reliability.

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7.4 Device Functional Modes

表 7-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

表 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER				
	V_{IN}	V_{BIAS}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} \geq V_{OUT\ (nom)} + V_{DO(IN)}$ and $V_{IN} \geq V_{IN(min)}$	$V_{BIAS} \geq V_{OUT} + V_{DO(BIAS)}$	$V_{EN} \geq V_{HI(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT\ (nom)} + V_{DO(IN)}$	$V_{BIAS} < V_{OUT} + V_{DO(BIAS)}$	$V_{EN} > V_{HI(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Disabled mode (any true condition disables the device)	$V_{IN} < V_{UVLO(IN)}$	$V_{BIAS} < V_{BIAS(UVLO)}$	$V_{EN} < V_{LO(EN)}$	—	$T_J \geq T_{SD}$ for shutdown

7.4.1 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO(IN)}$)
- The bias voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO(BIAS)}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD(shutdown)}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. Similarly, if the bias voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode as well. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and functions as a switch. Line or load transients in dropout can result in large output voltage deviations.

When the device is in a steady dropout state, defined as when the device is in dropout ($V_{IN} < V_{OUT} + V_{DO(IN)}$ or $V_{BIAS} < V_{OUT} + V_{DO(BIAS)}$ directly after being in normal regulation state, but not during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO(IN)}$), the output voltage can overshoot for a short time when the device pulls the pass transistor back into the linear region.

7.4.3 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than $V_{IL(EN)}$ (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

The device is disabled under the following conditions:

- The input or bias voltages are below the respective minimum specifications
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold
- The device junction temperature is greater than the thermal shutdown temperature

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8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS7A53A-Q1 is a low-input, low-output (LILO), low-dropout regulator (LDO) that features soft-start capability. This regulator uses a low-current bias input to power all internal control circuitry, allowing the NMOS pass transistor to regulate very low input and output voltages.

Using an NMOS pass transistor offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little effect on loop stability. This architecture allows stability with ceramic capacitors of 10 μF or greater. Transient response is also superior to PMOS topologies, particularly for low V_{IN} applications.

A programmable voltage-controlled, soft-start circuit provides a smooth, monotonic start-up and limits start-up inrush currents that can be caused by large capacitive loads. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low V_{IN} and V_{OUT} capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often required by processor-intensive systems.

8.1.1 Input, Output, and Bias Capacitor Requirements

The device is designed to be stable for ceramic capacitor of values ≥ 10 μF. The device is also stable with multiple capacitors in parallel, which can be of any type or value.

The capacitance required on the IN and BIAS pins strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for V_{IN} is 1 μF and the minimum recommended capacitor for V_{BIAS} is 0.1 μF. If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for V_{BIAS} is 4.7 μF. Use good quality, low equivalent series resistance (ESR) and equivalent series inductance (ESL) capacitors on the input; ceramic X5R and X7R capacitors are preferred. Place these capacitors as close the pins as possible for optimum performance.

Low ESR and ESL capacitors improve high-frequency PSRR.

8.1.2 Dropout Voltage

The TPS7A53A-Q1 offers very low dropout performance, making the device designed for high-current, low V_{IN} and low V_{OUT} applications. The low dropout allows the device to be used in place of a dc/dc converter and still achieve good efficiency. 方程式 2 provides a quick estimate of the efficiency.

$$\text{Efficiency} \approx \frac{V_{OUT} \times I_{OUT}}{\left[V_{IN} \times (I_{IN} + I_Q)\right]} \approx \frac{V_{OUT}}{V_{IN}} \text{ at } I_{OUT} >> I_Q \tag{2}$$

This efficiency provides designers with the power architecture for applications to achieve the smallest, simplest, and lowest cost solutions.

For this architecture, there are two different specifications for dropout voltage. The first specification (see 图 6-19) is referred to as *V_{IN} dropout* and is used when an external bias voltage is applied to achieve low dropout. This specification assumes that V_{BIAS} is at least 2.8 V above V_{OUT}, which is the case for V_{BIAS} when powered by a 5.0-V rail with 5% tolerance and with V_{OUT} = 1.5 V. If V_{BIAS} is higher than V_{OUT} + 2.8 V, the V_{IN} dropout is less than specified.

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备注

2.8 V is a test condition of this device and can be adjusted by referring to the *Electrical Characteristics* table.

The second specification (illustrated in 图 6-20) is referred to as V_{BIAS} *dropout* and applies to applications where IN and BIAS are tied together. This option allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. Dropout is limited by BIAS in these applications because V_{BIAS} provides the gate drive to the pass transistor; therefore, V_{BIAS} must be 1.9 V above V_{OUT}. Because of this usage, having IN and BIAS tied together become a highly inefficient solution that can consume large amounts of power. Pay attention not to exceed the power rating of the device package.

8.1.3 Output Noise

The TPS7A53A-Q1 provides low output noise when a soft-start capacitor is used. When the device reaches the end of the soft-start cycle, the soft-start capacitor serves as a filter for the internal reference. By using a 10-nF, soft-start capacitor, the output noise is reduced by half and is typically 7.1 μV_{RMS} for a 1-V output (10 Hz to 100 kHz). Further increasing C_{SS} has little effect on noise. Because most of the output noise is generated by the internal reference, the noise is a function of the set output voltage. 方程式 3 gives the RMS noise with a 10-nF, soft-start capacitor:

$$V_N(\mu V_{RMS}) = 7.1 \cdot \left(\frac{\mu V_{RMS}}{V}\right) \cdot V_{OUT}(V) \tag{3}$$

The low output noise makes this LDO a good choice for powering transceivers, phase-locked loops (PLLs), or other noise-sensitive circuitry.

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8.1.4 Estimating Junction Temperature

By using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in 方程式 4). For backwards compatibility, an older $\theta_{JC(top)}$ parameter is listed as well.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$
$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{4}$$

where:

- P_D is the power dissipation
- T_T is the temperature at the center-top of the package
- T_B is the PCB temperature measured 1 mm away from the package *on the PCB surface*

备注

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the *Using New Thermal Metrics* application note, available for download at www.ti.com.

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, see the *Using New Thermal Metrics* application note, available for download at www.ti.com. For further information, see the *Semiconductor and IC Package Thermal Metrics* application note, also available on the TI website.

8.1.5 Soft Start, Sequencing, and Inrush Current

Soft-start refers to the ramp-up characteristic of the output voltage during LDO turn-on after EN and UVLO achieve threshold voltage. The soft start current is fixed for fixed output voltage versions.

Although the device does not have any sequencing requirement, following the sequencing order of BIAS, IN, and EN makes sure that the soft start starts from zero.

图 8-1 shows an example of the device behavior when the EN pin is enabled prior to having either power supply up. Under this condition, the output jumps from 0 V to approximately 0.3 V almost instantly when the IN voltage is sufficient to power the circuit.

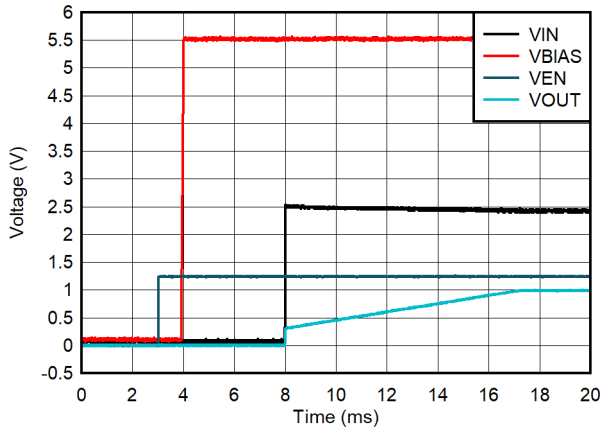


图 8-1. Sequencing and Soft-Start Behavior

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As shown in 图 8-2, connecting EN to IN, in conjunction with a slow input or output voltage ramp, can have undesired behavior in the application. For a smooth IN and OUT ramp, consider using the EN pin separate from the IN voltage.

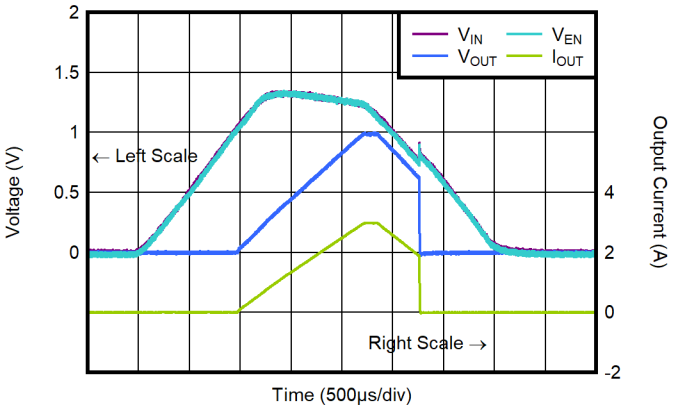


图 8-2. V_{EN} = V_{IN} Behavior

Inrush current is defined as the current into the LDO at the IN pin during start-up. Inrush current then consists primarily of the sum of load current and the current used to charge the output capacitor. This current is difficult to measure because the input capacitor must be removed, which is not recommended. However, 方程式 5 can estimate this soft-start current:

$$I_{OUT(t)} = \left[\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right] + \left[\frac{V_{OUT}(t)}{R_{LOAD}}\right] \quad (5)$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turn-on ramp
- $dV_{OUT}(t) / dt$ is the slope of the V_{OUT} ramp
- R_{LOAD} is the resistive load impedance

8.1.6 Power-Good Operation

For proper operation of the power-good circuit, the pullup resistor value must be between 10 kΩ and 100 kΩ. The lower limit of 10 kΩ results from the maximum pulldown strength of the power-good transistor, and the upper limit of 100 kΩ results from the maximum leakage current at the power-good node. If the pullup resistor is outside of this range, then the power-good signal can possibly not read a valid digital logic level.

The state of PG is only valid when the device operates above the minimum supply voltage. During short UVLO events and at light loads, power-good does not assert because the output voltage is sustained by the output capacitance.

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8.2 Typical Application

This section discusses the implementation of the fixed 1.0-V TPS7A53A-Q1 to regulate a 3-A load requiring good PSRR at high frequency with low noise. 图 8-3 provides a schematic for this typical application circuit.

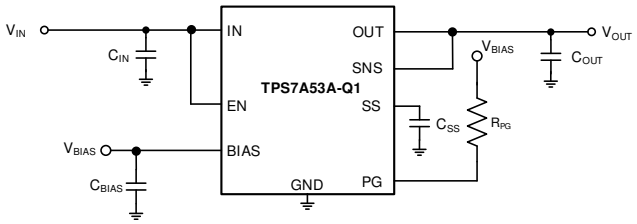


图 8-3. Typical Fixed Voltage Application

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 as the input parameters.

表 8-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	1.3 V, ±3%, provided by the dc/dc converter switching at 500 kHz
Bias voltage	5.0 V
Output voltage	1.0 V, ±1%
Output current	3.0 A (maximum), 10 mA (minimum)
RMS noise, 10 Hz to 100 kHz	< 10 μV_{RMS}
PSRR at 500 kHz	> 40 dB
Start-up time	< 25 ms

8.2.2 Detailed Design Procedure

At 3.0 A and 1.0 V_{OUT}, the dropout of the TPS7A53A-Q1 has a 285-mV maximum dropout over temperature; thus, a 300-mV headroom is sufficient for operation over both input and output voltage accuracy. At full load and high temperature on some devices, the TPS7A53A-Q1 can enter dropout if both the input and output supply are beyond the edges of the respective accuracy specification.

To satisfy the required start-up time and still maintain low noise performance, a 10-nF C_{SS} is selected. 方程式 6 calculates this value.

$$t_{SS} = (V_{SS} \times C_{SS}) / I_{SS} \quad (6)$$

At the 3.0-A maximum load, the internal power dissipation is 0.9 W and corresponds to a 38.3°C junction temperature rise for the RTJ package on a standard JEDEC board. With an 55°C maximum ambient temperature, the junction temperature is at 93.3°C.

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8.2.3 Application Curve

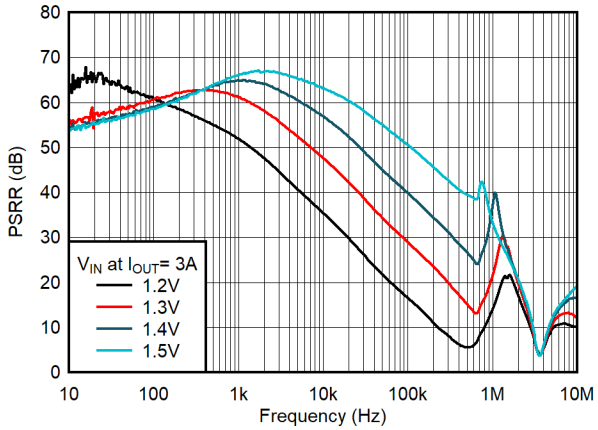


图 8-4. PSRR vs Frequency for V_{OUT} = 1.0 V and I_{OUT} = 3 A

8.3 Power Supply Recommendations

The TPS7A53A-Q1 is designed to operate from an input voltage up to 6.0 V, provided the bias rail is at least 1.3 V higher than the input supply and dropout requirements are met. The bias rail and the input supply must both provide adequate headroom and current for the device to operate normally. Connect a low output impedance power supply directly to the IN pin. This supply must have at least 1 μF of capacitance near the IN pin for optimal performance. A supply with similar requirements must also be connected directly to the BIAS rail with a separate 0.1 μF or larger capacitor. If the IN pin is tied to the BIAS pin, a minimum 4.7-μF capacitor is required for performance. To increase the overall PSRR of the solution at higher frequencies, use a pi-filter or ferrite bead before the input capacitor.

8.4 Layout

8.4.1 Layout Guidelines

8.4.1.1 Board Layout

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. To avoid negative system performance, do not use of vias and long traces to the input and output capacitors. The grounding and layout scheme illustrated in 图 8-5 minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

To improve performance, use a ground reference plane, either embedded in the PCB or placed on the bottom side of the PCB opposite the components. This reference plane serves to provide accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

8.4.1.2 RTJ Package — High CTE Mold Compound

The RTJ package uses a mold compound with a high coefficient of thermal expansion (CTE) of 12 ppm/°C. This mold compound allows for the CTE of the packaged device to more closely match the CTE of a conventional FR4 PCB (approximately 14 ppm/°C to 17 ppm/°C). This CTE match is important when considering the effects that temperature swings can induce on a board with large differences in CTE values. Package and board combinations with widely dissimilar CTEs can experience mechanical cracking or fracturing of the solder joints caused by frequent changes in temperature, and the corresponding differences in expansion. Devices with

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normal mold compounds in similar packages typically have CTE values that are 25% lower than values found with the RTJ package.

8.4.2 Layout Example

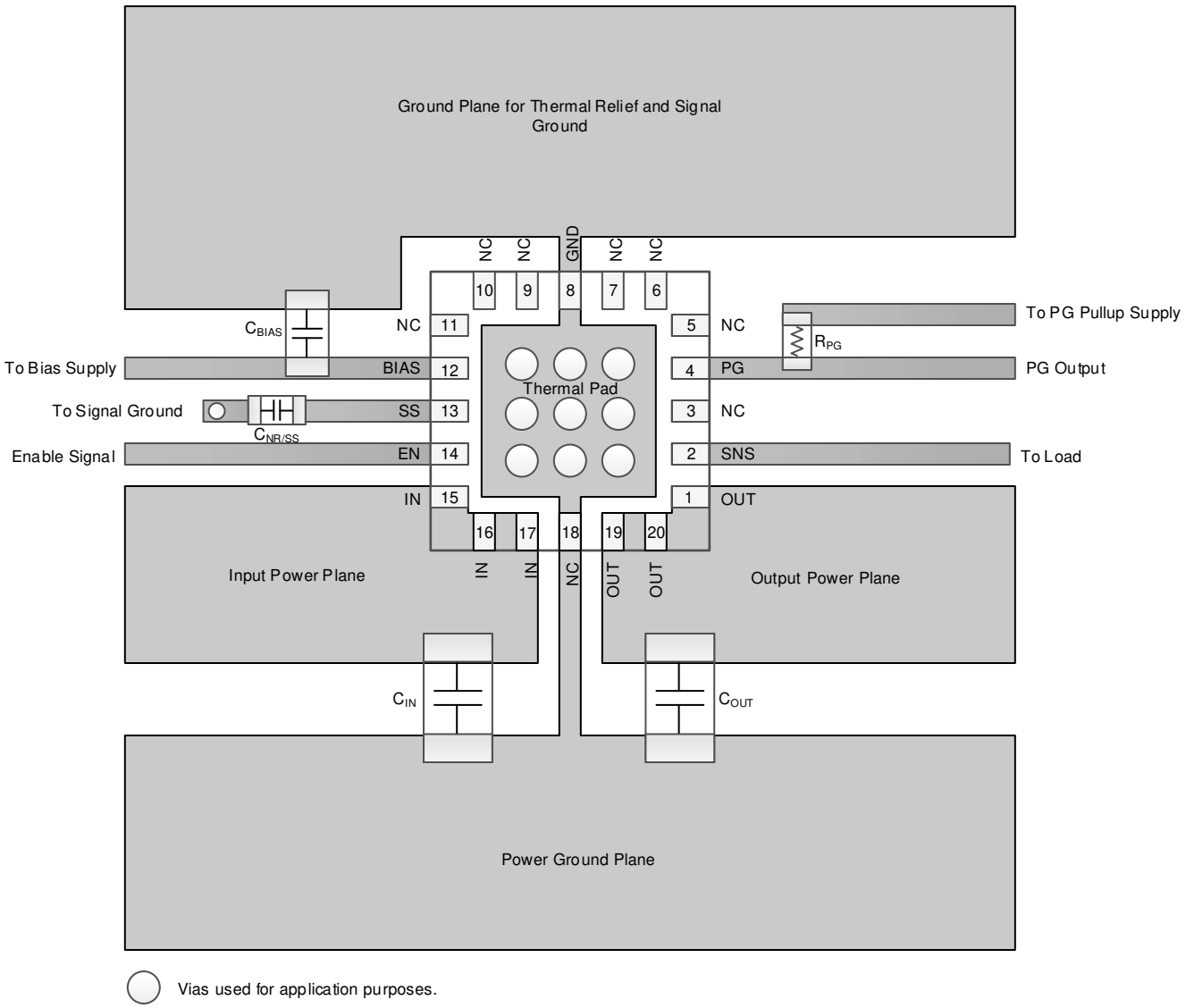


图 8-5. Example Layout

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9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *TPS3702 High-Accuracy, Overvoltage and Undervoltage Monitor* data sheet
- Texas Instruments, *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator* application note
- Texas Instruments, *6 A Current-Sharing Dual LDO* design guide

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

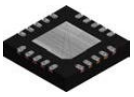
10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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10.1 Mechanical Data

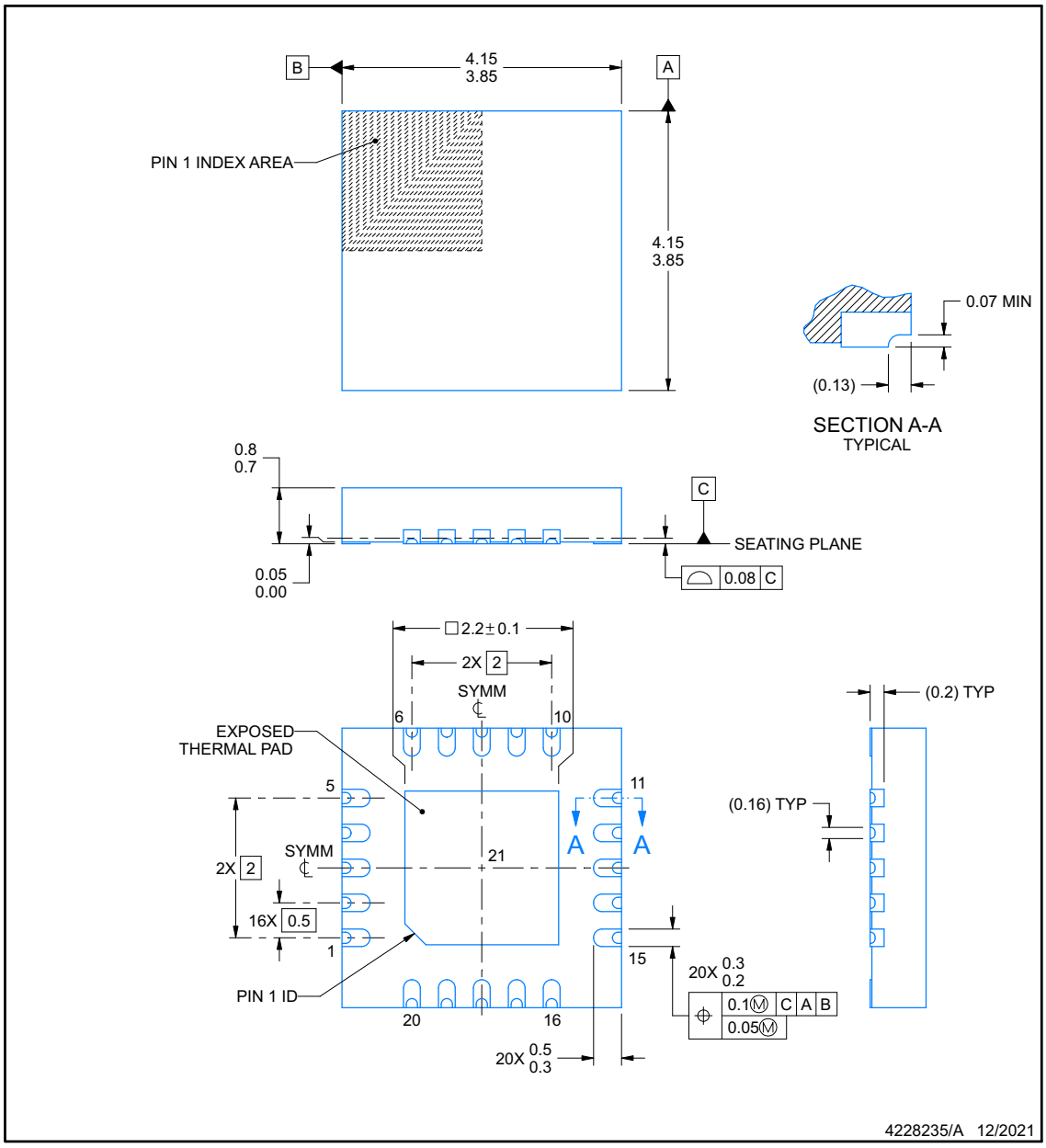
RTJ0020L



PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

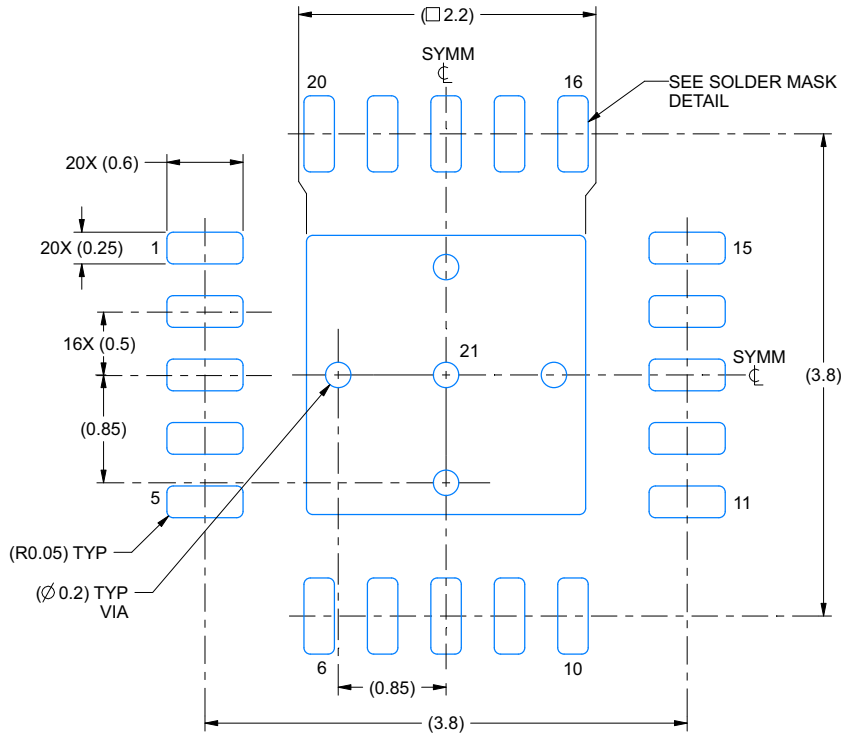
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EXAMPLE BOARD LAYOUT

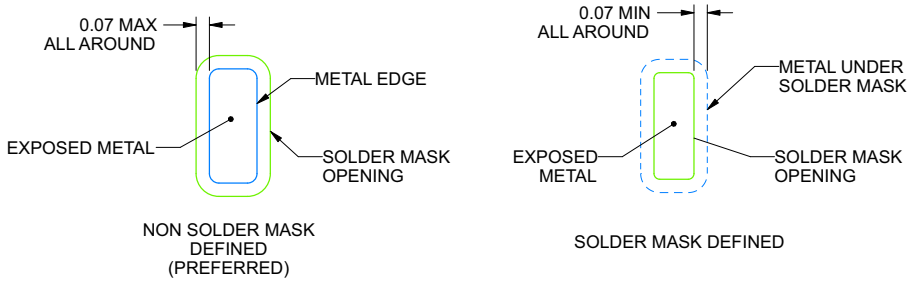
RTJ0020L

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4228235/A 12/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

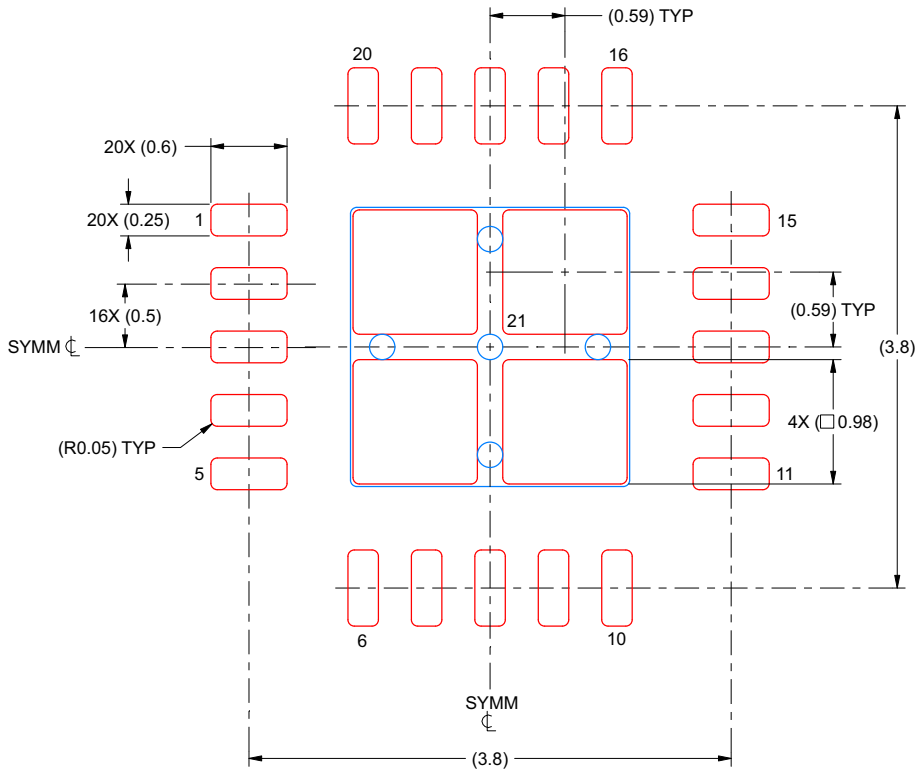
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EXAMPLE STENCIL DESIGN

RTJ0020L

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 21
79% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4228235/A 12/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A5310AQWRTJRQ1	Active	Production	QFN (RTJ) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	7A5310A
TPS7A5310AQWRTJRQ1.A	Active	Production	QFN (RTJ) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	7A5310A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

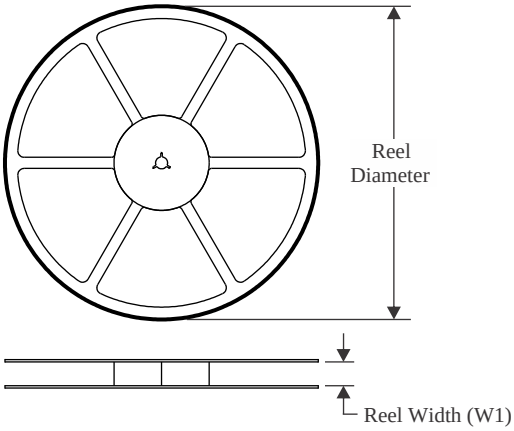
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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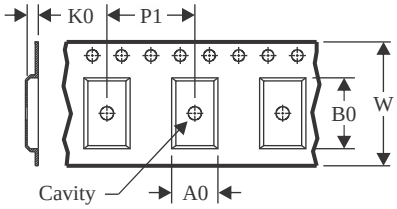
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

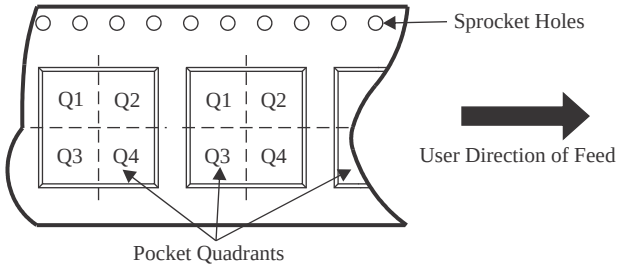


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

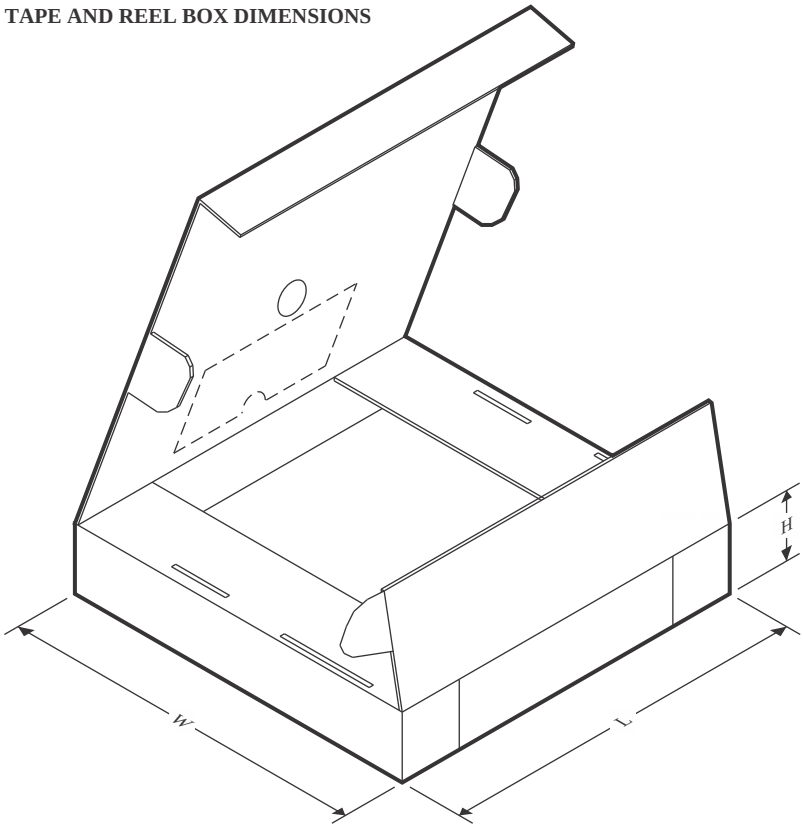
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A5310AQWRTJRQ1	QFN	RTJ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A5310AQWRTJRQ1	QFN	RTJ	20	3000	360.0	360.0	36.0

GENERIC PACKAGE VIEW

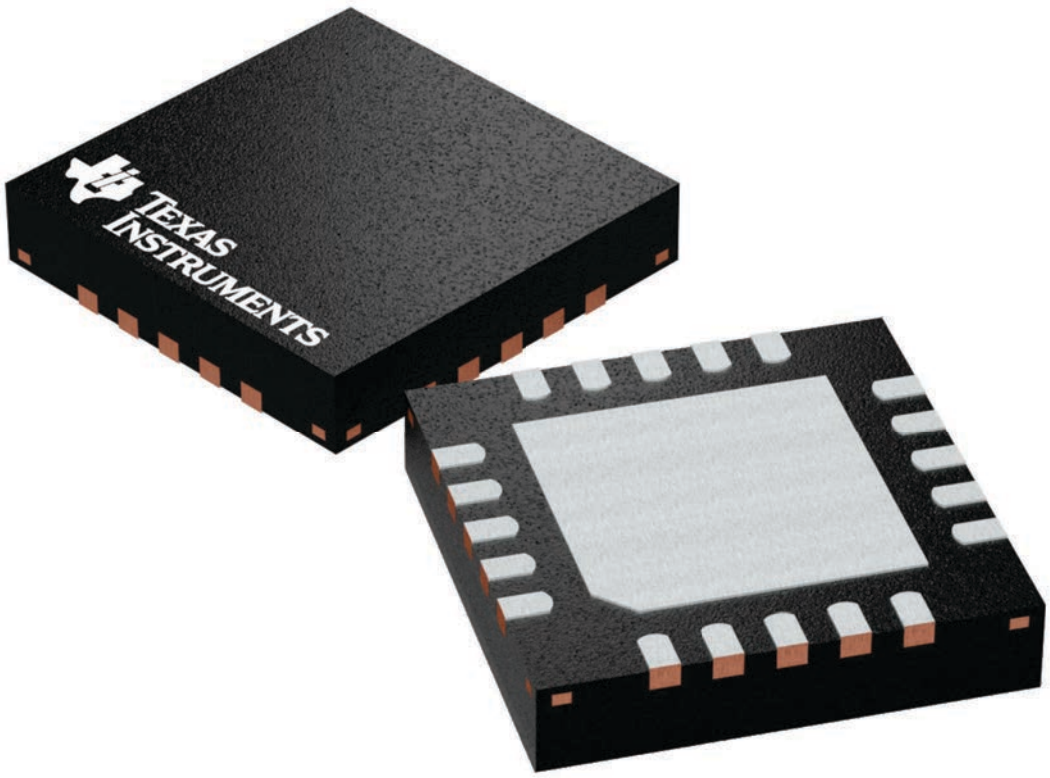
RTJ 20

WQFN - 0.8 mm max height

4 x 4, 0.5 mm pitch

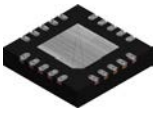
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224842/A

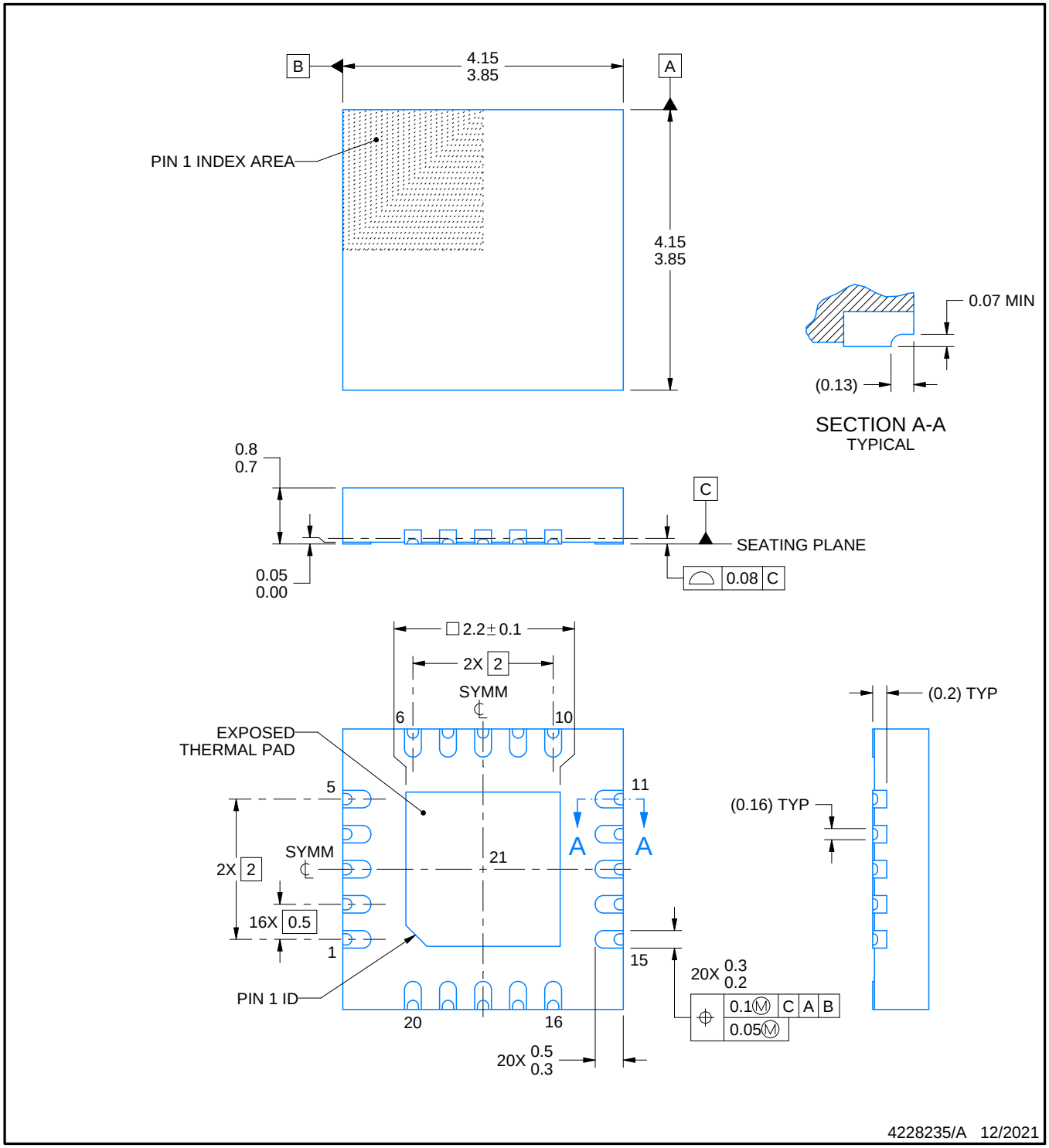
RTJ0020L



PACKAGE OUTLINE

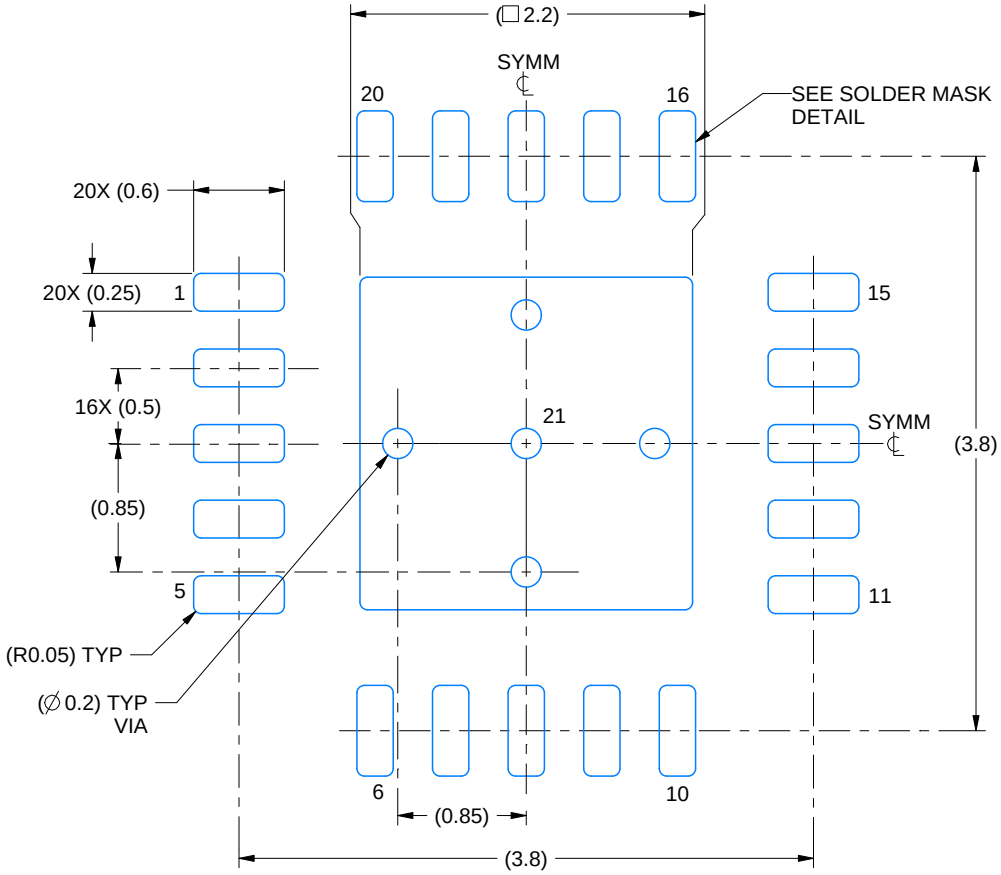
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

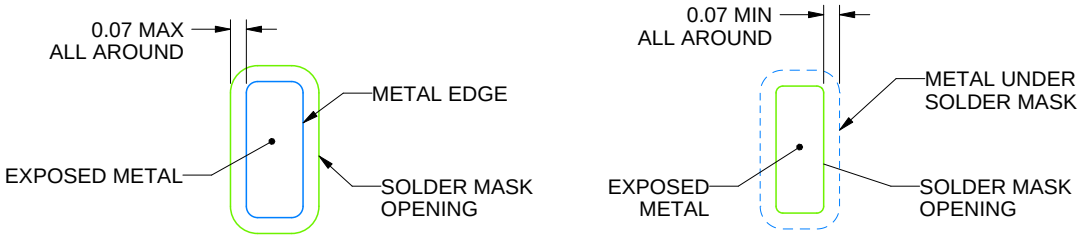


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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NOTES: (continued)

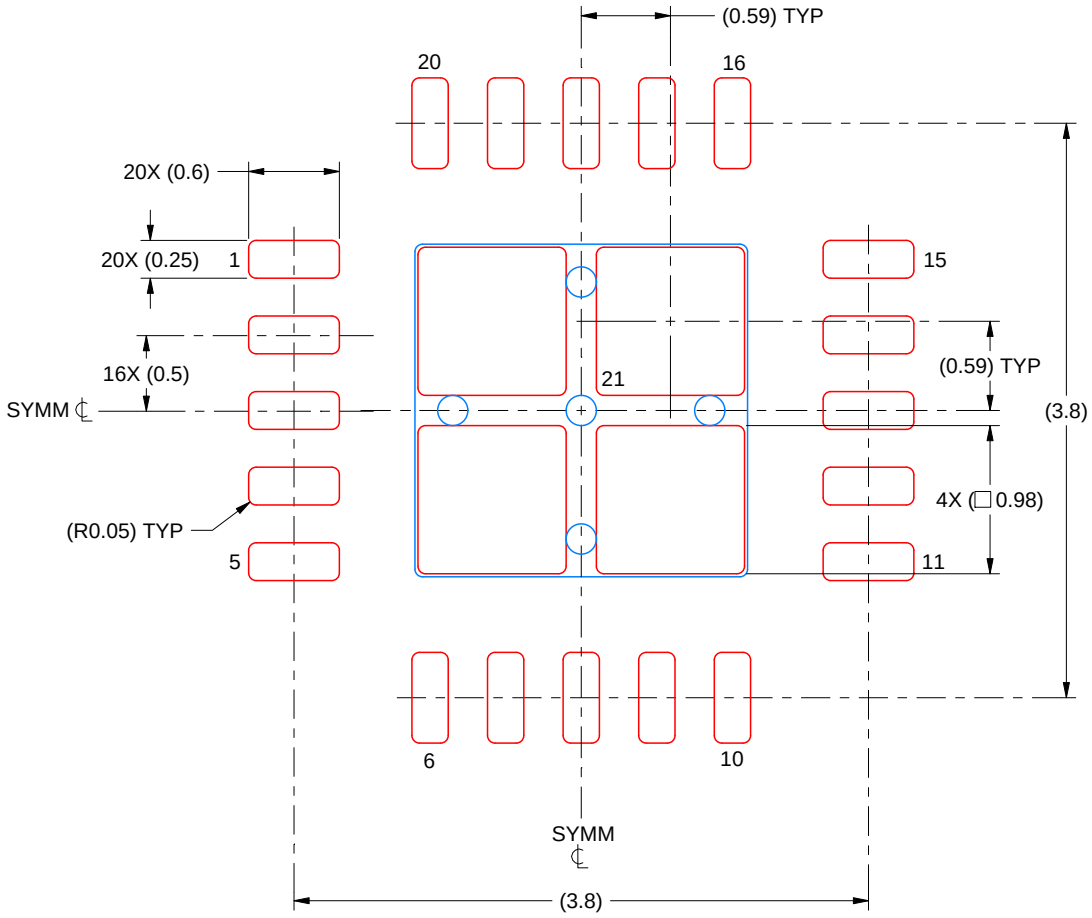
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTJ0020L

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 21
79% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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