TPS7A24 200mA、18V、超低 I_Q 低压降稳压器

1 特性

- 超低 I_Q：2.0 μA
- 输入电压：2.4 V 至 18 V
- 可用输出电压选项：
  - 固定：1.25 V 至 5.5 V
  - 可调节：1.24 V 至 17.75 V
- 在温度范围内的精度为 1.25%
- 低压降：200 mA 时为 250 mV（最大值）
- 主动过冲下拉保护
- 热关断保护和过流保护
- 工作结温：–40°C 至 +125°C
- 与 1μF 输出电容器一起工作时保持稳定
- 封装：5 引脚 SOT-23 封装

2 应用

- 烟雾和热量探测器
- 恒温器
- 运动检测器（PIR、uWave 等）
- 无线电动工具
- 电器电池组
- 电表
- 水表

3 说明

TPS7A24 低压降 (LDO) 线性稳压器支持 2.4V 至 18V 的输入电压范围，并具有超低的静态电流 (I_Q)。这些特性能帮助现代电器满足日益严苛的能源要求，并有助于延长便携式电源解决方案的电池寿命。

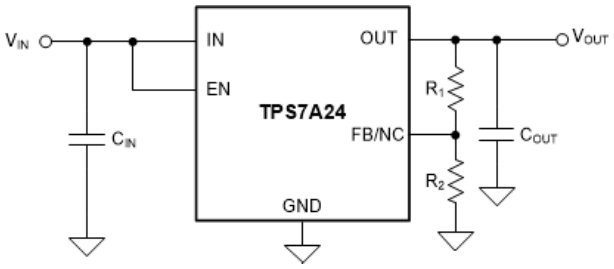
TPS7A24 有固定电压和可调节电压两种版本可供选用。固定电压版本无需外部电阻器，可最大限度减小印刷电路板 (PCB) 尺寸。为获得更大的灵活性或更高的输出电压，可调节电压版本使用反馈电阻器将输出电压设置为 1.24V 到 17.75V 之间。两种版本都具有 1.25% 的输出调节精度，可对微控制器 (MCU) 基准电压进行精密调节。

在电流为 200mA 时，TPS7A24 LDO 的最大压降小于 250mV，因此它比标准线性稳压器的工作效率更高。此最大压降使得在 3.55V 输入电压 (V_{IN}) 至 3.3V 输出电压 (V_{OUT}) 范围内的效率达到了 92.8%。

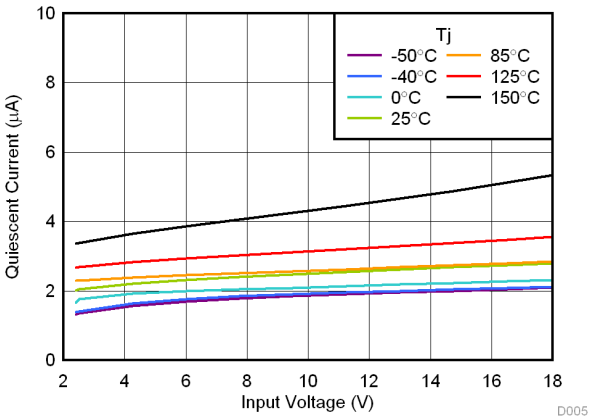
封装信息(1)

器件型号	封装	封装尺寸（标称值）
TPS7A24	DBV（SOT-23，5）	2.90mm × 1.60mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的封装选项附录。



典型应用电路



静态电流与输入电压
(V_{OUT} = 1.24V，I_{OUT} = 0A)

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (May 2022) to Revision E (September 2022)	Page
• Changed *Dropout Voltage vs* V_{IN} and *Dropout Voltage vs* I_{OUT} figures in *Typical Characteristics* section	7

Changes from Revision C (January 2022) to Revision D (May 2022)	Page
• Added Output voltage accuracy at 25 ℃ to *Electrical Characteristics* table	6

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5 Pin Configuration and Functions

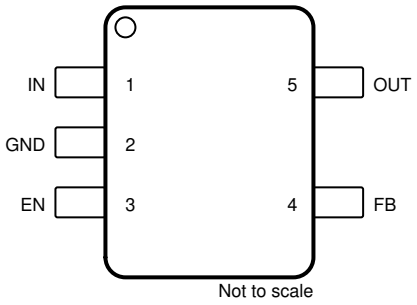


图 5-1. DBV Package (Adjustable), 5-Pin SOT-23 (Top View)

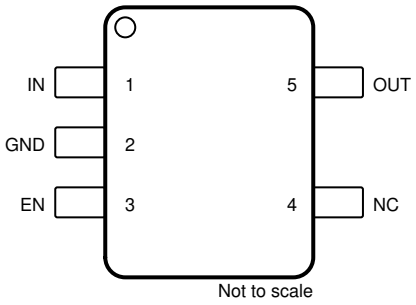


图 5-2. DBV Package (Fixed), 5-Pin SOT-23 (Top View)

表 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	DBV (Adjustable)	DBV (Fixed)		
EN	3	3	Input	Enable pin. Drive EN greater than $V_{EN(HI)}$ to enable the regulator. Drive EN less than $V_{EN(LOW)}$ to put the regulator into low-current shutdown. Do not float this pin. If not used, connect EN to IN.
FB	4	—	Input	Feedback pin. Input to the control-loop error amplifier. This pin is used to set the output voltage of the device with the use of external resistors. For adjustable-voltage version devices only.
GND	2	2	—	Ground pin.
IN	1	1	Input	Input pin. For best transient response and to minimize input impedance, use the recommended value or larger capacitor from IN to ground as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the IN and GND pins of the device as possible.
NC	—	4	—	No internal connection. For fixed-voltage version devices only. This pin can be floated but the device has better thermal performance with this pin tied to GND.
OUT	5	5	Output	Output pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger capacitor from OUT to ground. Follow the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the OUT and GND pins of the device as possible.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	V_{IN}	–0.3	20	V
	V_{OUT}	–0.3	V_{IN} + 0.3(3)	
	V_{FB}	–0.3	5.5	
	V_{EN}	–0.3	20	
Current	Maximum output	Internally limited		A
Temperature	Operating junction, T_J	–50	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages with respect to GND.
(3) V_{IN} + 0.3 V or 20 V (whichever is smaller).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 2-kV HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.4		18	V
V_{OUT}	Output voltage (adjustable version)	1.24		18 - V_{DO}	V
V_{OUT}	Output voltage (fixed version)	1.25		5.5	V
I_{OUT}	Output current	0		200	mA
V_{EN}	Enable voltage	0		18	V
C_{IN} (1)	Input capacitor		1		µF
C_{OUT} (1)	Output capacitor	1	2.2	100	µF
T_J	Operating junction temperature	–40		125	°C

(1) All capacitor values are assumed to derate to 50% of the nominal capacitor value.

6.4 Thermal Information

THERMAL METRIC(1)		TPS7A24 DBV (SOT23-5) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	167.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	86.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics application reports* application report.

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6.5 Electrical Characteristics

specified at T_J = –40°C to + 125°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or V_{IN} = 2.4 V (whichever is greater), FB tied to OUT, I_{OUT} = 1 mA, V_{EN} = 2 V, and C_{IN} = 1 µF, C_{OUT} = 2.2 µF ceramic (unless otherwise noted); typical values are at T_J = 25°C

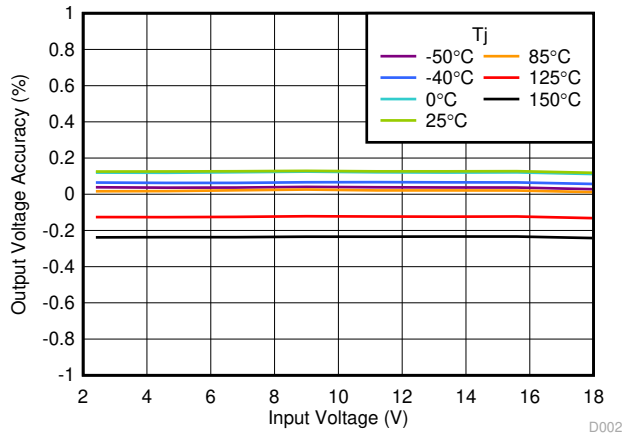
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage accuracy	Adjustable version, V_{OUT} = V_{FB}	1.22	1.24	1.26	V
		Fixed output versions, T_J = -40℃ to 125℃	–1.25		1.25	%
V_{OUT}	Output voltage accuracy	Fixed output versions, T_J = 25 ℃	–0.5		0.5	%
V_{FB}	Feedback voltage	Adjustable version only		1.24		V
$\Delta V_{OUT}(\Delta VIN)$	Line regulation(1)	($V_{OUT(nom)}$ + 0.5 V or 2.4 V) ≤ V_{IN} ≤ 18 V	–0.25		0.25	%
$\Delta V_{OUT}(\Delta IOUT)$	Load regulation	1 mA ≤ I_{OUT} ≤ 200 mA	–0.5		0.5	%
I_{GND}	Ground pin current	I_{OUT} = 0 mA		2	4.5	µA
		I_{OUT} = 1 mA		15		
$I_{SHUTDOWN}$	Shutdown current	V_{EN} ≤ 0.4 V, V_{IN} = 2.4 V, I_{out} = 0 mA		325	650	nA
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(nom)}$	250	410	620	mA
I_{FB}	FB pin current			10		nA
V_{DO}	Dropout voltage(2)	I_{OUT} = 100 mA		110	160	mV
		I_{OUT} = 200 mA		160	250	
PSRR	Power-supply rejection ratio	f = 10 Hz		75		dB
		f = 100 Hz		70		
		f = 1 kHz		62		
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, V_{OUT} = 1.24 V		300		µ V_{RMS}
$V_{UVLO(RISING)}$	UVLO threshold rising	V_{IN} rising	1.95	2.15	2.35	V
$V_{UVLO(HYS)}$	UVLO hysteresis			70		mV
$V_{UVLO(FALLING)}$	UVLO threshold falling	V_{IN} falling	1.85	2.09	2.25	V
$V_{EN(HI)}$	Enable pin high-level input voltage	Device enabled	0.9			V
$V_{EN(LOW)}$	Enable pin low-level input voltage	Device disabled			0.4	V
I_{EN}	EN pin current	V_{EN} = 18 V		10		nA
$T_{SD(shutdown)}$	Thermal shutdown temperature	Shutdown, temperature increasing		165		°C
$T_{SD(reset)}$	Thermal shutdown reset temperature	Reset, temperature decreasing		145		°C

(1) $V_{out(nom)}$ + 0.5 V or 2.4 V (whichever is greater).
(2) V_{DO} is measured with V_{IN} = 0.97 × $V_{OUT(nom)}$ for fixed output voltage versions. V_{DO} is not measured for fixed output voltage versions when V_{OUT} ≤ 2.5 V. For the adjustable output device, V_{DO} is measured with V_{FB} = 0.97 × $V_{FB(nom)}$.

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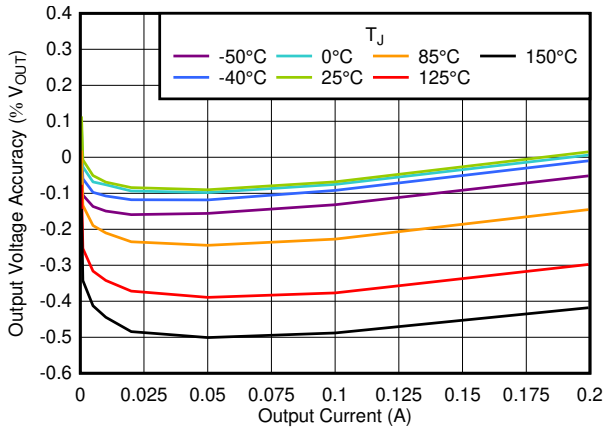
6.6 Typical Characteristics

at operating temperature T_J = 25°C, I_{OUT} = 1 mA, V_{EN} = 0.9 V, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(typ)}$ + 0.8 V or 2.4 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C



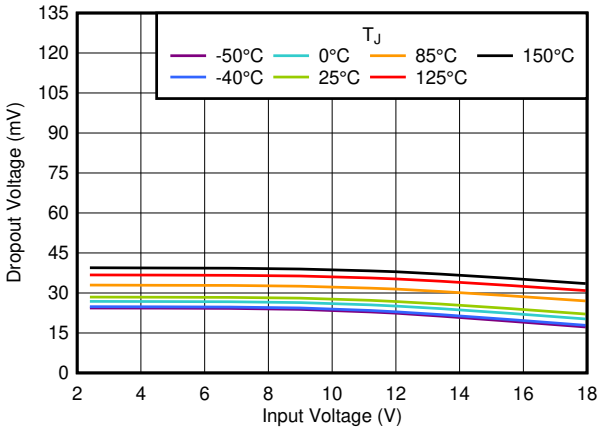
I_{OUT} = 1 mA

图 6-1. Line Regulation vs V_{IN}



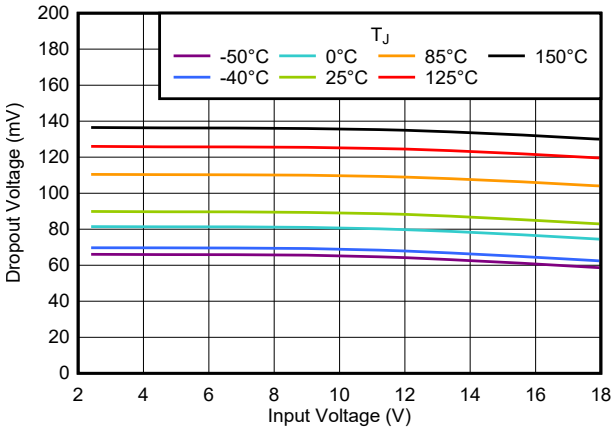
V_{OUT} = 1.24 V

图 6-2. Load Regulation vs I_{OUT}



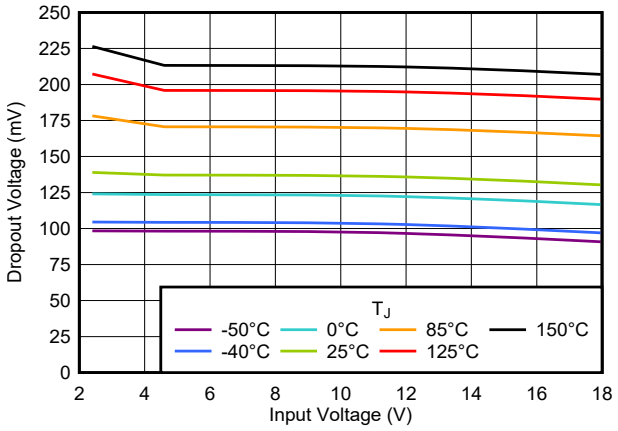
I_{OUT} = 10 mA

图 6-3. Dropout Voltage vs V_{IN}



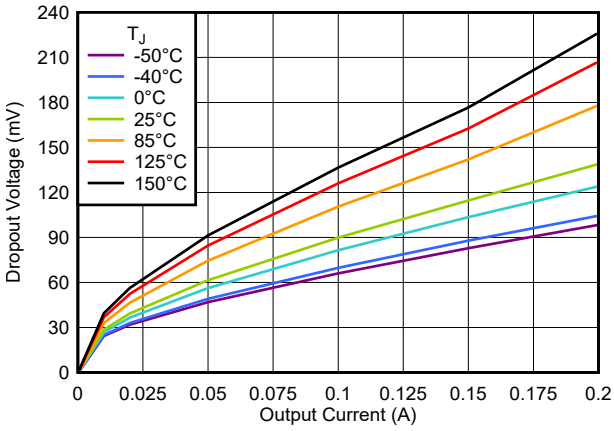
I_{OUT} = 100 mA

图 6-4. Dropout Voltage vs V_{IN}



I_{OUT} = 200 mA

图 6-5. Dropout Voltage vs V_{IN}



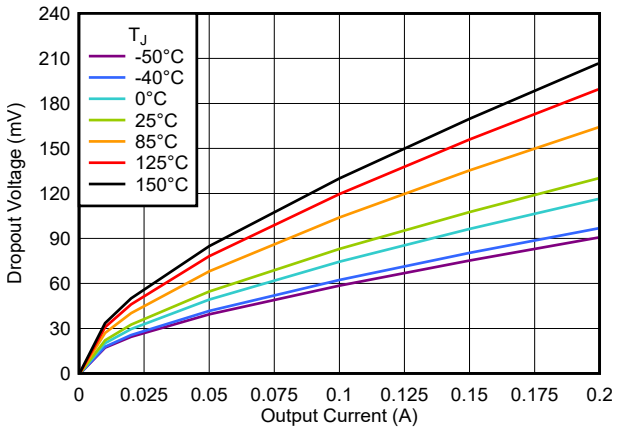
V_{IN} = 2.4 V

图 6-6. Dropout Voltage vs I_{OUT}

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6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1 mA, V_{EN} = 0.9 V, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(typ)}$ + 0.8 V or 2.4 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C



V_{IN} = 18 V

图 6-7. Dropout Voltage vs I_{OUT}

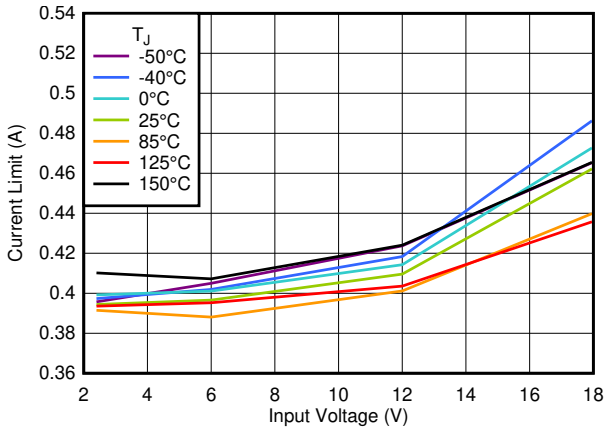
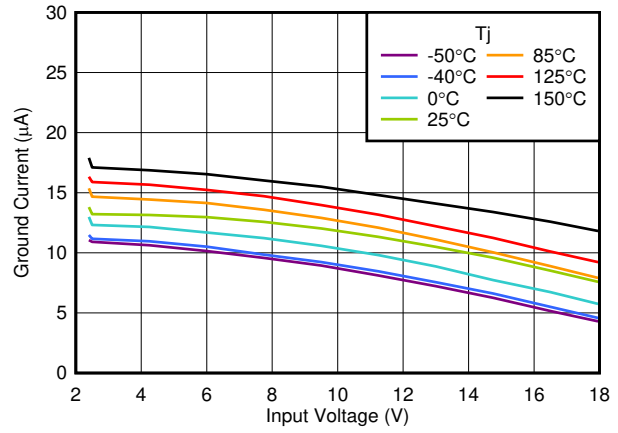
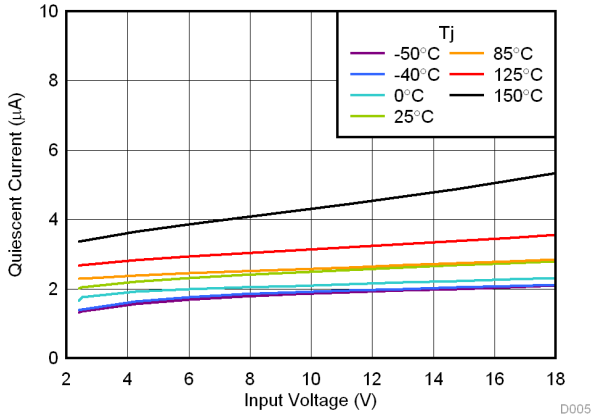


图 6-8. Current Limit vs V_{IN}



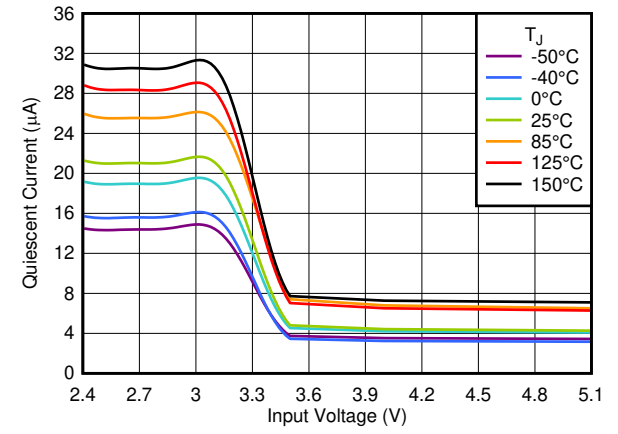
V_{OUT} = 1.24 V, I_{OUT} = 1 mA

图 6-9. I_{GND} vs V_{IN}



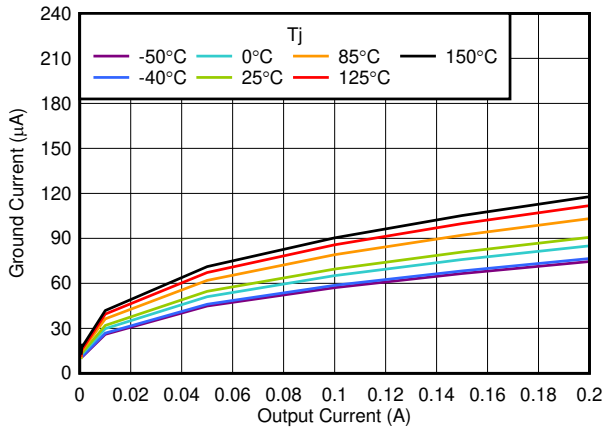
V_{OUT} = 1.24 V, I_{OUT} = 0 A

图 6-10. I_Q vs V_{IN}



V_{OUT} = 3.3 V, I_{OUT} = 0 A

图 6-11. I_Q vs V_{IN}



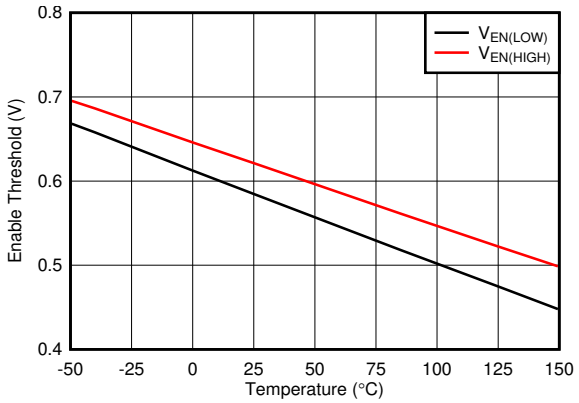
V_{OUT} = 1.24 V

图 6-12. I_{GND} vs I_{OUT}

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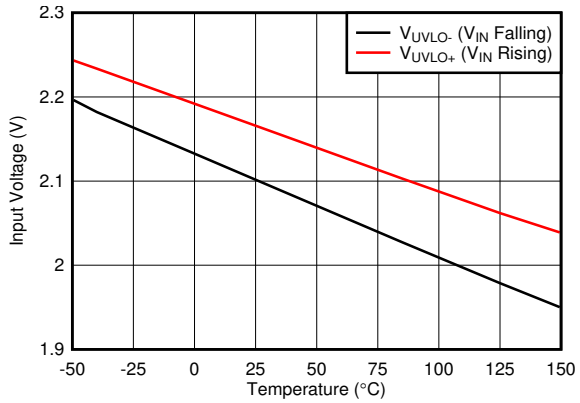
6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1 mA, V_{EN} = 0.9 V, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(typ)}$ + 0.8 V or 2.4 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C



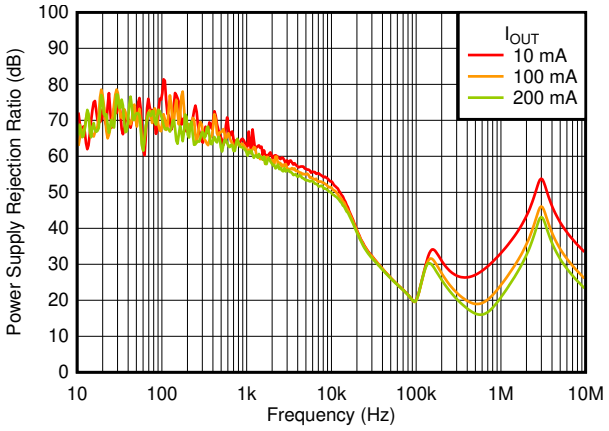
V_{OUT} = 1.24 V, 2.4 V ≤ V_{IN} ≤ 18 V

图 6-13. V_{EN} vs Temperature



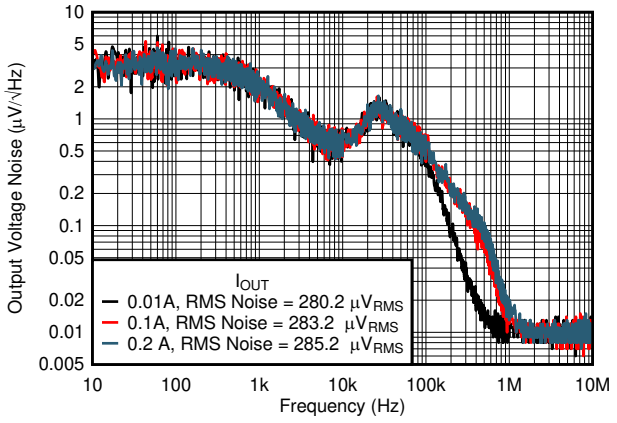
V_{OUT} = 1.24 V, I_{OUT} = 1 mA

图 6-14. UVLO Thresholds vs Temperature



V_{OUT} = 1.24 V, C_{IN} = 0 µF, C_{OUT} = 1 µF

图 6-15. PSRR vs Frequency and I_{OUT}



V_{OUT} = 1.24 V, C_{IN} = 1 µF, C_{OUT} = 1 µF, C_{FF} = 10 nF, V_{RMS} BW = 10 Hz to 100 kHz

图 6-16. Output Noise (V_n) vs Frequency and I_{OUT}

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7 Detailed Description

7.1 Overview

The TPS7A24 is an 18-V, low quiescent current, low-dropout (LDO) linear regulator. The low I_Q performance makes the TPS7A24 an excellent choice for battery-powered or line-power applications that are expected to meet increasingly stringent standby-power standards. The fixed-output versions have the advantage of providing better accuracy with fewer external components, whereas the adjustable version has the flexibility for a far wider output voltage range.

The 1.25% accuracy over temperature makes this device an excellent choice for meeting a wide range of microcontroller power requirements.

For increased reliability, the TPS7A24 also incorporates overcurrent, overshoot pulldown, and thermal shutdown protection. The operating junction temperature is –40°C to +125°C, and adds margin for applications concerned with higher working ambient temperatures.

7.2 Functional Block Diagrams

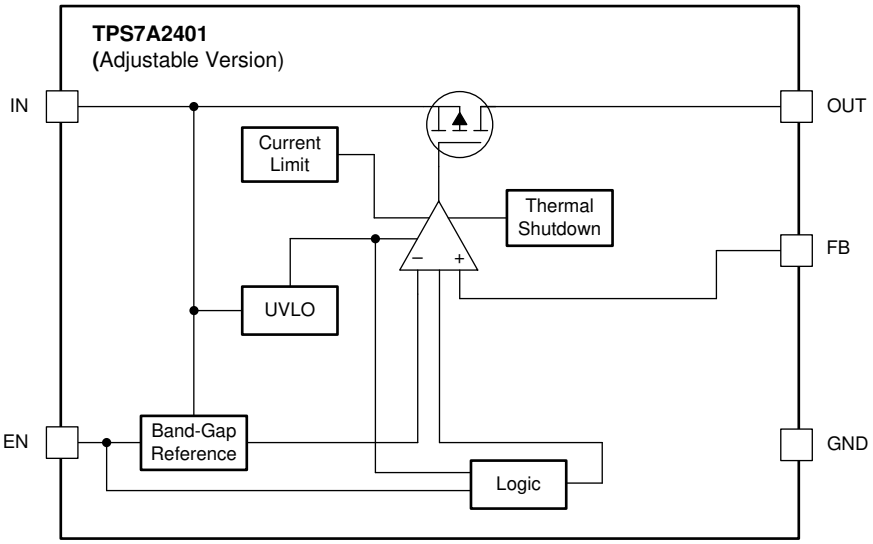


图 7-1. Adjustable Version Block Diagram

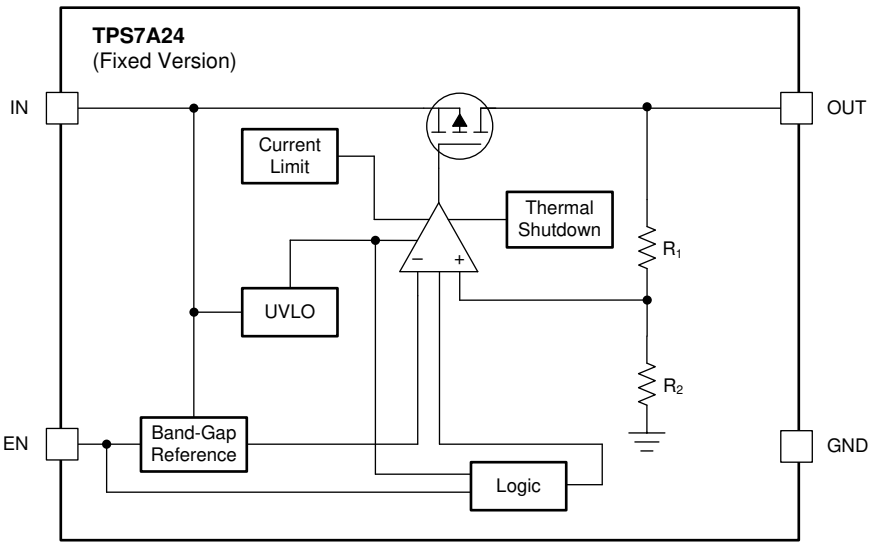


图 7-2. Fixed Version Block Diagram

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7.3 Feature Description

7.3.1 Output Enable

The enable pin for the device is an active-high pin. The output voltage is enabled when the voltage of the enable pin is greater than the high-level input voltage of the EN pin and disabled with the enable pin voltage is less than the low-level input voltage of the EN pin. If independent control of the output voltage is not needed, connect the enable pin to the input of the device.

7.3.2 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} - V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{1}$$

7.3.3 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [($V_{IN} - V_{OUT}$) × I_{CL}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application report.

图 7-3 shows a diagram of the current limit.

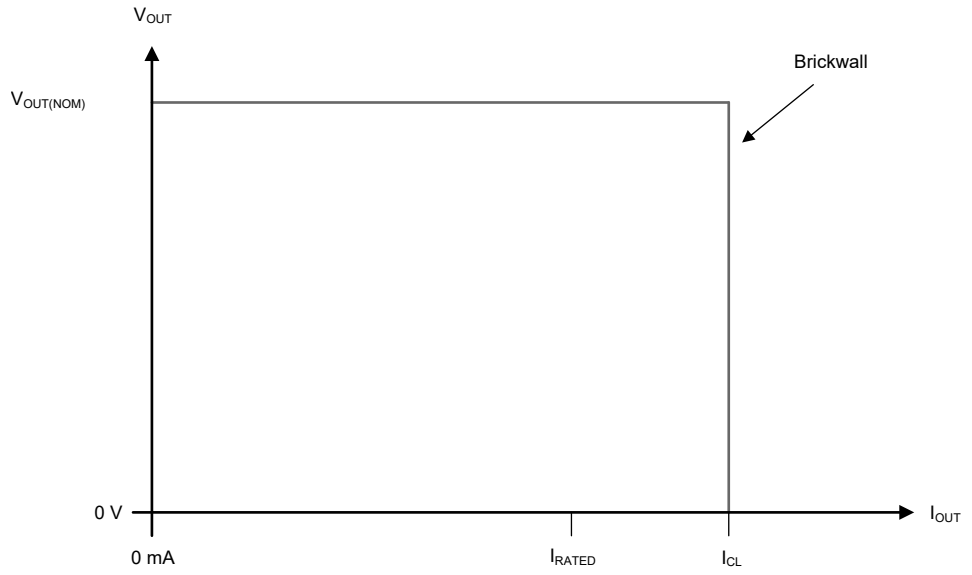


图 7-3. Current Limit

7.3.4 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

7.3.5 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start up can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start up completes.

When the thermal limit is triggered with load currents near the value of the current limit, the output may oscillate prior to the output switching off.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

7.3.6 Active Overshoot Pulldown Circuitry

This device has pulldown circuitry connected to V_{OUT}. This circuitry is a 100-μA current sink, in series with a 5.5-kΩ resistor, controlled by V_{EN}. When V_{EN} is below $V_{EN(LOW)}$, the pulldown circuitry is disabled and the LDO output is in high-impedance mode.

If the output voltage is more than 2% above nominal voltage when $V_{EN} \geqslant V_{EN(LOW)}$, the pulldown circuitry turns on and the output is pulled down until the output voltage is within 2% from the nominal voltage. This feature helps reduce overshoot during the transient response.

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7.4 Device Functional Modes

7.4.1 Device Functional Mode Comparison

表 7-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

表 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

7.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off and internal circuits are shutdown.

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8 Application and Implementation

备注

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8.1 Application Information

8.1.1 Adjustable Device Feedback Resistors

The adjustable-version device requires external feedback divider resistors to set the output voltage. V_{OUT} is set using the feedback divider resistors, R_1 and R_2, according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (2)$$

To ignore the FB pin current error term in the V_{OUT} equation, set the feedback divider current to 100x the FB pin current listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leqslant V_{OUT} / (I_{FB} \times 100) \quad (3)$$

8.1.2 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. As a rule of thumb, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

8.1.3 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. An input capacitor is recommended if the source impedance is more than 0.5 Ω. A higher value capacitor may be necessary if large, fast load transient or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

The effective output capacitance value is recommended to not exceed 50 µF.

8.1.4 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leqslant V_{IN}$ + 0.3 V.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

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If reverse current flow is expected in the application, external protection is recommended to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

图 8-1 shows one approach for protecting the device.

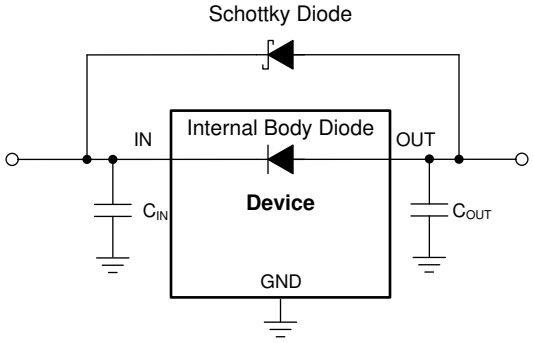


图 8-1. Example Circuit for Reverse Current Protection Using a Schottky Diode

图 8-2 shows another, more commonly used, approach in high input voltage applications.

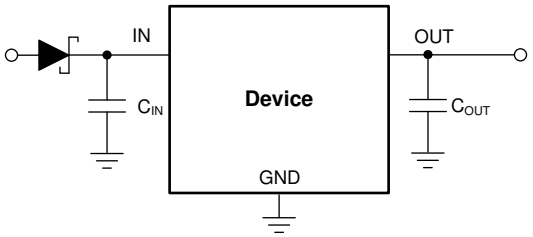


图 8-2. Reverse Current Prevention Using a Diode Before the LDO

8.1.5 Feed-Forward Capacitor (C_{FF})

For the adjustable-voltage version device, a feed-forward capacitor (C_{FF}) can be connected from the OUT pin to the FB pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended C_{FF} values are listed in the *Recommended Operating Conditions* table. A higher capacitance C_{FF} can be used; however, the start-up time increases. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application report.

8.1.6 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. 方程式 4 calculates power dissipation (P_D).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

备注

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

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For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to 方程式 5, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (5)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

8.1.7 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J). As described in 方程式 6, use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. As described in 方程式 7, use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (6)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (7)$$

where

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application report.

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8.1.8 Special Consideration for Line Transients

During a line transient, the response of this LDO to a very large or fast input voltage change can cause a brief shutdown lasting up to a few hundred microseconds from the voltage transition. This shutdown can be avoided by reducing the voltage step size, increasing the transition time, or a combination of both. 图 8-3 provides a boundary to follow to avoid this behavior. If necessary, reduce slew rate and the voltage step size to stay below the curve.

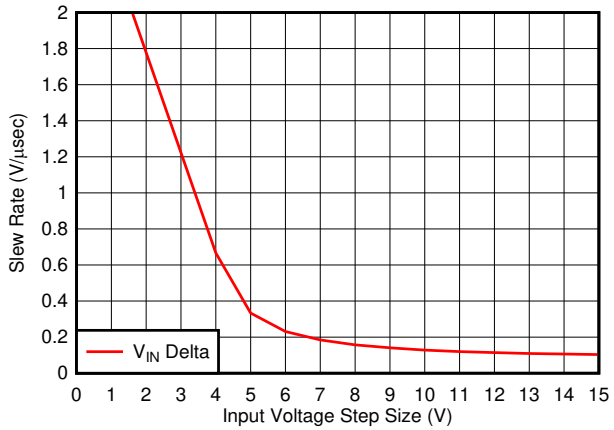


图 8-3. Recommended Input Voltage Step and Slew Rate in a Line Transient

8.2 Typical Application

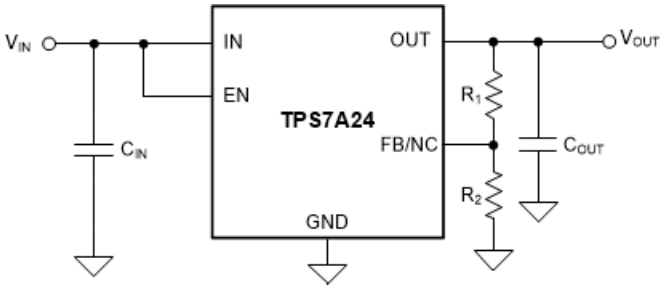


图 8-4. Generating a 3.3-V Rail From a Multicell Power Bank

8.2.1 Design Requirements

表 8-1 summarizes the design requirements for 图 8-4.

表 8-1. Design Parameters

PARAMETER	DESIGN VALUES
V_{IN}	5.3 V
V_{OUT}	3.3 V ±1.25%
$I_{(IN)}$ (no load)	< 5 µA
I_{OUT} (max)	200 mA
T_A	57.88°C (max)

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8.2.2 Detailed Design Procedure

Select a 3.3-V output, fixed or adjustable device to generate the 3.3-V rail. The fixed-version LDO has internal feedback divider resistors, and thus has lower quiescent current. The adjustable-version LDO requires external feedback divider resistors, and is described in the *Selecting Feedback Divider Resistors* section.

8.2.2.1 Transient Response

As with any regulator, increasing the output capacitor value reduces over- and undershoot magnitude, but increases transient response duration.

8.2.2.2 Selecting Feedback Divider Resistors

For this design example, V_{OUT} is set to 5 V. The following equations set the output voltage:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (8)$$

$$R_1 + R_2 \leqslant V_{OUT} / (I_{FB} \times 100) \quad (9)$$

For improved output accuracy, use 方程式 9 and $I_{FB(TYP)}$ = 10 nA as listed in the *Electrical Characteristics* table to calculate the upper limit for series feedback resistance, $R_1 + R_2 \leqslant 5\ M\Omega$.

The control-loop error amplifier drives the FB pin to the same voltage as the internal reference (V_{FB} = 1.24 V as listed in the *Electrical Characteristics* table). Use 方程式 8 to determine the ratio of $R_1 / R_2 = 1.66$. Use this ratio and solve 方程式 9 for R_2. Now calculate the upper limit for $R_2 \leqslant 1.24\ M\Omega$. Select a standard value resistor of $R_2 = 1.18\ M\Omega$.

Reference 方程式 8 and solve for R_1:

$$R_1 = (V_{OUT} / V_{FB} - 1) \times R_2 \quad (10)$$

From 方程式 10, $R_1 = 1.96\ M\Omega$ can be determined. From 方程式 8, select V_{OUT} = 3.299 V.

8.2.2.3 Thermal Dissipation

Junction temperature can be determined using the junction-to-ambient thermal resistance ($R_{\theta JA}$) and the total power dissipation (P_D). Use 方程式 11 to calculate the power dissipation. Multiply P_D by $R_{\theta JA}$ and add the ambient temperature (T_A), as 方程式 12 shows, to calculate the junction temperature (T_J).

$$P_D = (I_{GND} + I_{OUT}) \times (V_{IN} - V_{OUT}) \quad (11)$$

$$T_J = R_{\theta JA} \times P_D + T_A \quad (12)$$

方程式 13 calculates the maximum ambient temperature. 方程式 14 calculates the maximum ambient temperature for typical design applications.

$$T_{A(MAX)} = T_{J(MAX)} - (R_{\theta JA} \times P_D) \quad (13)$$

$$T_{A(MAX)} = 125°C - [167.8°C/W \times (5.3\ V - 3.3\ V) \times 0.2A] = 57.88°C \quad (14)$$

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8.2.3 Application Curve

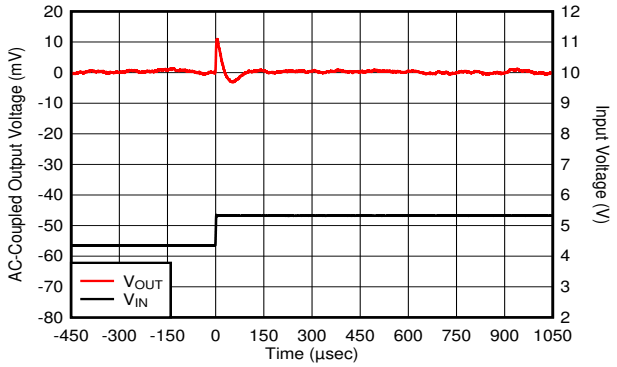


图 8-5. Line Transient (4.3 V to 5.3 V)

8.3 Power Supply Recommendations

The device is designed to operate with an input supply range of 2.4 V to 18 V. If the input supply is noisy, additional input capacitors with low ESR can help improve output noise performance. Connect a low output impedance power supply to the input pin of the TPS7A24. In order to optimize regulation, see the *Feature Description* section for more information on operation modes and performance features.

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8.4 Layout

8.4.1 Layout Guidelines

- Place input and output capacitors as close to the device pins as possible
- Use copper planes for device connections to optimize thermal performance
- Place thermal vias around the device to distribute heat

8.4.2 Layout Examples

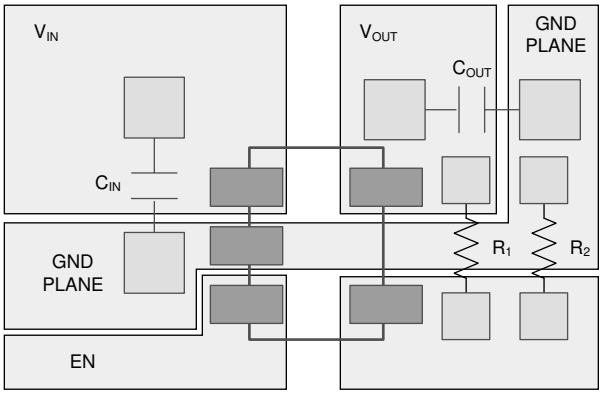


图 8-6. Adjustable Version Layout Example

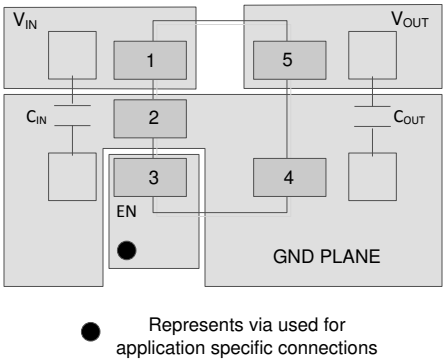


图 8-7. Fixed Version Layout Example

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9 Device and Documentation Support

9.1 Device Support

9.1.1 Device Nomenclature

表 9-1. Device Nomenclature(1)

PRODUCT	V_{OUT}
TPS7A24**xx(x)yyyz**	**xx(x)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; for output voltages with a resolution of 50 mV, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V). 01 indicates adjustable output version. **yyy** is the package designator. **z** is the package quantity. R is for large quantity reel

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

9.2 接收文档更新通知

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A2401DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1XFF
TPS7A2401DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1XFF
TPS7A2401DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1XFF
TPS7A2401DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1XFF
TPS7A24125DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1XTF
TPS7A24125DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1XTF
TPS7A2418DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1XLF
TPS7A2418DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1XLF
TPS7A2418DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1XLF
TPS7A2418DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1XLF
TPS7A2425DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1XKF
TPS7A2425DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1XKF
TPS7A2430DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1XJF
TPS7A2430DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1XJF
TPS7A2433DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1XHF
TPS7A2433DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1XHF
TPS7A2436DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1XIF
TPS7A2436DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1XIF
TPS7A2450DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1XGF
TPS7A2450DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1XGF
TPS7A2450DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1XGF
TPS7A2450DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1XGF

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

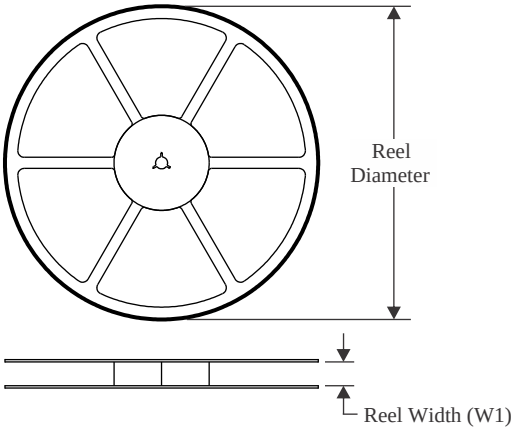
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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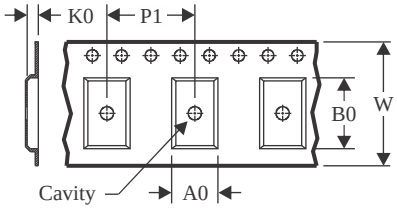
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

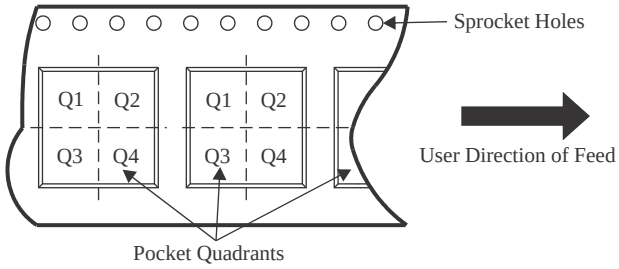


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

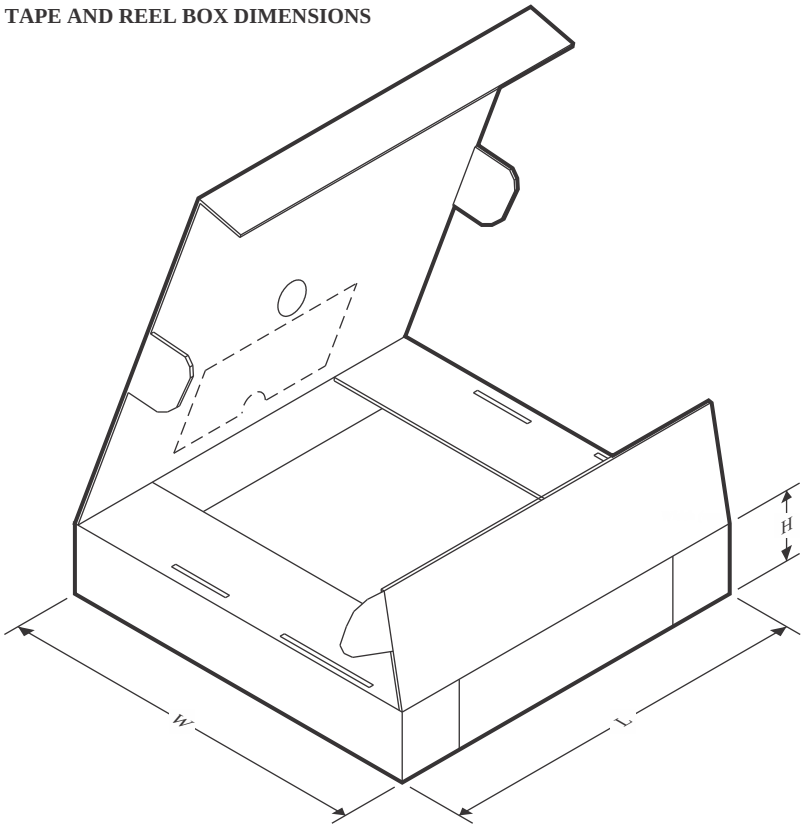


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A2401DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A2401DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2401DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2401DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2401DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2401DBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A24125DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2418DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2418DBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2425DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2430DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2430DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A2433DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2436DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2450DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2450DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A2450DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A2450DBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

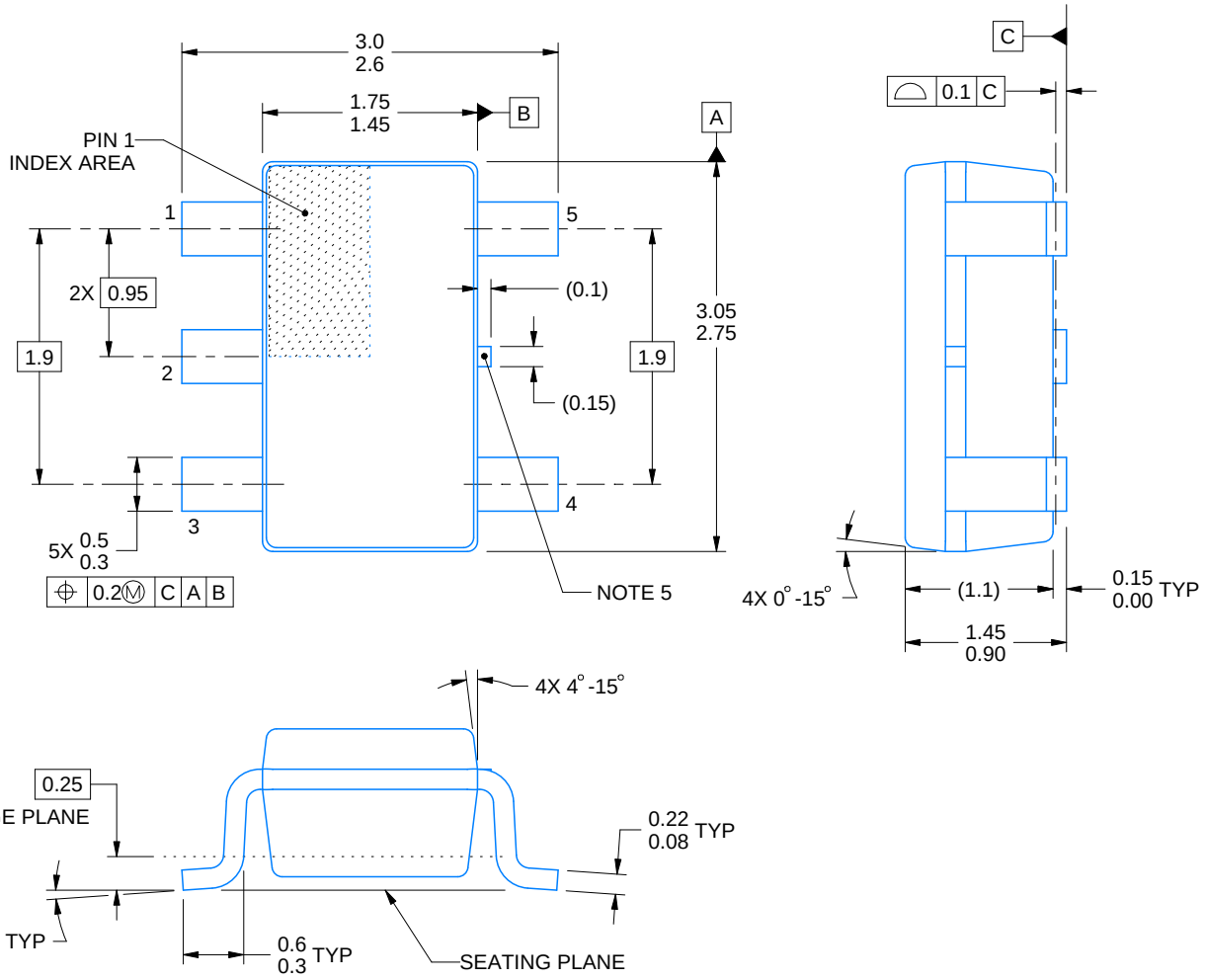
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A2401DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A2401DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2401DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2401DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TPS7A2401DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2401DBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A24125DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2418DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TPS7A2418DBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2425DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2430DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TPS7A2430DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A2433DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TPS7A2436DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TPS7A2450DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2450DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TPS7A2450DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A2450DBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

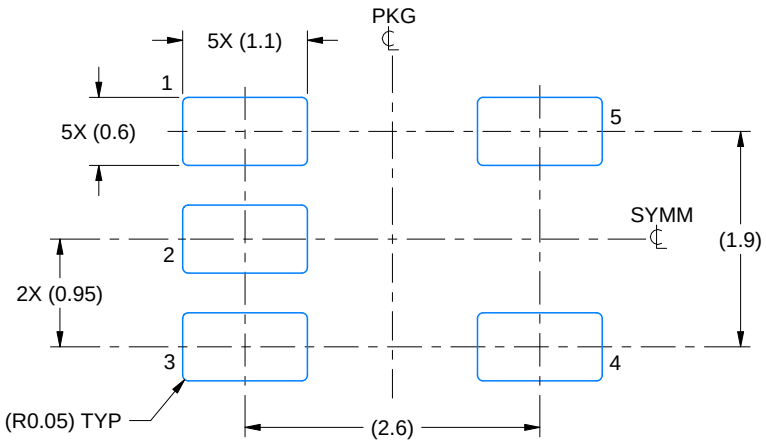
SMALL OUTLINE TRANSISTOR



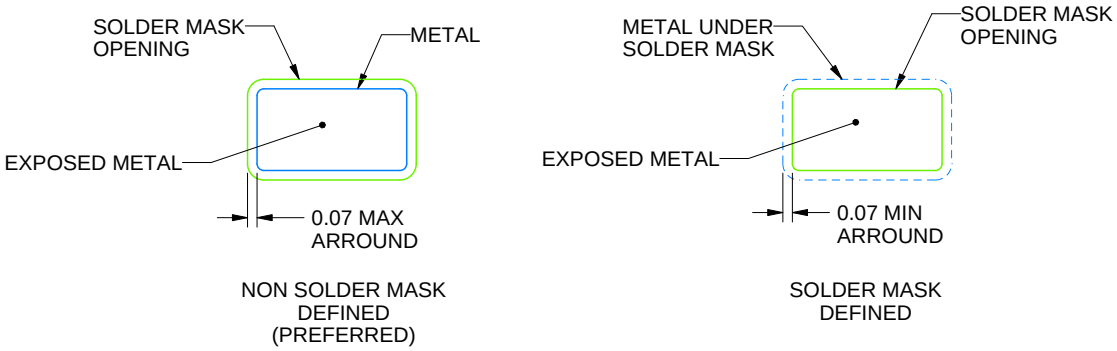
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

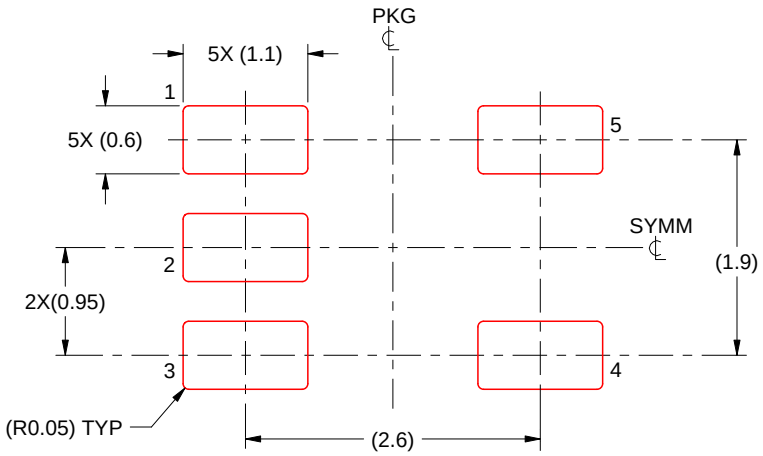


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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