适用于处理器的 TPS659037 电源管理单元 (PMU)

1 器件概述

1.1 特性

- 七个降压开关模式电源 (SMPS) 稳压器：
  - 其中一个输出为 0.7V-1.65V/6A（阶跃为 10mV）
    - 支持数字电压调节 (DVS) 控制的双相配置
  - 其中一个输出为 0.7V-1.65V/4A（阶跃为 10mV）
    - 支持 DVS 控制的双相配置
  - 其中一个输出为 0.7V-3.3V/3A（阶跃为 10mV 或 20mV）
    - 单相配置
    - 该稳压器可搭配 6A 稳压器构成 9A 三相稳压器（通过 DVS 控制）
  - 两个 0.7V-3.3V/2A（步长为 10mV 或 20mV）
    - 单相配置
    - 一个支持 DVS 控制的稳压器，也可配置成 3A 稳压器
  - 两个 0.7V-3.3V/1A（步长为 10mV 或 20mV）
    - 单相配置
    - 一个支持 DVS 控制的稳压器
  - 除 1A SMPS 稳压器外的所有稳压器均支持输出电流测量
  - 双相和三相稳压器均支持差分遥感（输出和接地）
  - 通过硬件和软件控制的 Eco-mode™高达 5mA，静态电流为 15µA
  - 短路保护
  - 电源正常指示（电压和过流指示）
  - 内部软启动可限制浪涌电流
  - 可通过相位同步将 SMPS 与外部时钟或内部备用时钟同步
- 七个步长为 50mV 的通用低压降稳压器 (LDO)：
  - 两个 0.9V-3.3V/300mA LDO，由经过预稳压的电源供电
  - 两个 0.9V-3.3V/200mA LDO，由经过预稳压的电源供电
  - 一个 0.9V-3.3V/50mA LDO，由经过预稳压的电源供电
  - 一个 100mA USB LDO
  - 一个 0.9V-3.3V/高达 100mA 低噪声 LDO（低噪声性能高达 50mA）
  - 两个供 PMU 内部使用的附加 LDO
  - 短路保护
- 时钟管理 16MHz 晶体振荡器和 32kHz RC 振荡器
  - 一个缓冲式 32kHz 输出
- 具有警报唤醒机制的实时时钟 (RTC)
- 具有三个外部输入通道和六个自监控内部通道的 12 位 Σ-Δ 通用模数转换器 (GPADC)
- 过热监控
  - 高温警告
  - 热关断
- 控制
  - 可配置上电和断电序列（一次性可编程 [OTP]）
  - 睡眠和激活状态之间的可配置序列（OTP 可编程）
  - 一个可纳入到启动序列中的专用数字输出信号 (REGEN)
  - 三个与 GPIO 进行多路复用并可纳入到启动序列中的数字输出信号
  - 可选控制接口
    - 一个用于资源配置和 DVS 控制的串行外设接口 (SPI)
    - 两个 I^2C 接口。其中一个专用于 DVS 控制，另一个是用于资源配置和 DVS 控制的通用 I^2C 接口
- 欠压锁定
- 系统电压范围为 3.135V 至 5.25V
- 封装选项
  - 12mm × 12mm、169 引脚 nFBGA 封装，引脚间距为 0.8mm

1.2 应用

- 工厂自动化
- 可编程逻辑控制器
- 模块上系统
- 人机界面

1.3 说明

TPS659037 器件是一款集成式电源管理 IC (PMIC)。该器件提供七个可配置的降压转换器，输出电流高达 6A，可用于存储器、处理器内核、输入/输出 (I/O) 或 LDO 预稳压。其中一个可配置的降压转换器与另一个 3A 稳压器组合后可提供高达 9A 的输出电流。所有这些降压转换器均可与频率介于 1.7MHz 至 2.7MHz 之间的外部时钟源或频率为 2.2MHz 的内部备用时钟同步。

TPS659037 器件提供七个供外部使用的 LDO 稳压器。这些 LDO 稳压器可由系统电源或经过预稳压的电源供电。上电和断电控制器是可配置的，能够支持所有上电和断电序列（基于 OTP）。TPS659037 器件包含一个 32kHz RC 振荡器，可在上电和断电过程中对所有资源进行排序。在需要快速启动的情况下，也可使用 16MHz 晶体振荡器来快速为系统产生一个稳定的 32kHz 频率。所有 LDO 和 SMPS 转换器均可由 SPI 或 I^2C 接口或通过电源请求信号进行控制。此外，电压调节寄存器允许将 SMPS 转换为 SPI、I^2C 或顶部/底部控制所需的不同电压。

每种封装中都有一个专用引脚可配置为上电序列的一部分，用于控制外部资源。该器件具备通用输入输出 (GPIO) 功能，两个 GPIO 均可配置为上电序列的一部分，用于控制外部资源。电源请求信号通过启用电源模式控制功能来实现电源优化。该器件包含一个带有三个外部输入通道的通用 ∑-Δ 模数转换器 (GPADC)。

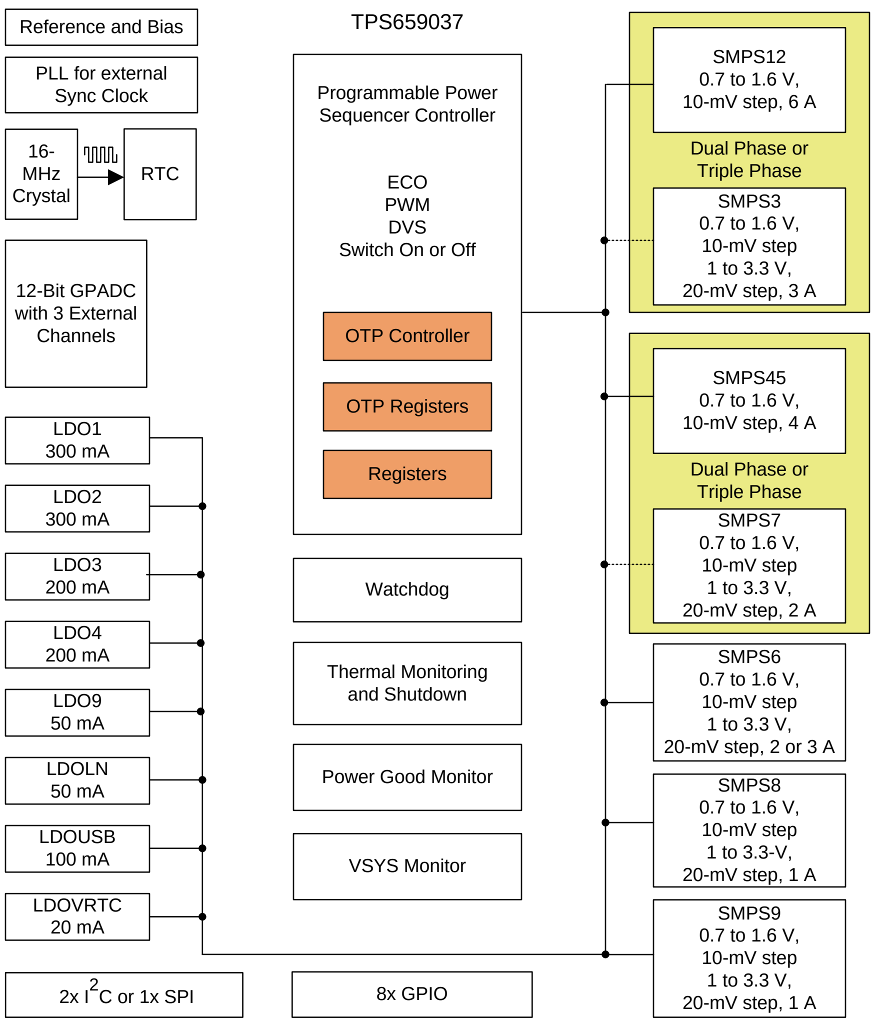
TPS659037 器件采用 13 引脚 × 13 引脚 nFBGA 封装，引脚间距为 0.8mm。

器件信息 (1)

器件型号	封装	封装尺寸（标称值）
TPS659037	ZWS (169)	12.00mm × 12.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

1.4 简化方框图



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内容

2 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision F (January 2018) to Revision G	Page
• Updated the LDOVRTC_OUT pulldown resistor recommendation to only include applicable silicon revisions.	6
• Changed ESD Ratings for charge device model on 6 pins	12
• Clarified that LDO1 and LDO2 input pins are not included in this minimum recommended operating voltage. See *Electrical Characteristics: LDO Regulators* for more information.	13
• Changed minimum recommended operating condition of OSC16MIN from 0V to -0.7V	13
• Added LDO and SMPS output capacitance footnote	14
• Changed VSYS_LO hysteresis from 95mV to 75mV	22
• Updated Caution statement to only include applicable silicon revisions.	31
• Changed discharge resistance to match electrical characteristics table	34
• Added information about shutdown timing during short circuit detection	37
• Updated POWERGOOD description to clarify multi-phase operation.	37
• Updated LDOVRTC note to only include applicable silicon revisions.	42
• Added details on identifying device version.	60
• Added typical debounce time from POWERHOLD to the enable of the first rail in the power sequence.	62
• Added VSYS_LO note for applicable silicon revisions.	73
• Updated POR requirements to only include applicable silicon revisions.	74
• SMPS and LDO output capacitance specification further explained	81
• Added design considerations for VCC1 capacitance to support loss of power	81
• Corrected 9-Vpp with 7V absolute maximum specification in the *Layout Guidelines* section	87

Changes from Revision E (July 2017) to Revision F **Page**

Changes from Revision D (April 2016) to Revision E **Page**

Changes from Revision C (November 2015) to Revision D **Page**

Changes from Revision B (November 2015) to Revision C **Page**

Changes from Revision A (September 2015) to Revision B **Page**

3 Pin Configuration and Functions

	A	B	C	D	E	F	G	H	J	K	L	M	N
13	PBKG	SMPS1_2_FDBK	GPIO_1	SMPS1_IN	SMPS1_SW	SMPS2_SW	SMPS2_IN	SMPS3_IN	SMPS3_SW	SMPS3_FDBK	LDO34_IN	GND_ANA	PBKG
12	GPIO_2	GPIO_0	SMPS1_2_FDBK_GND	SMPS1_IN	SMPS1_SW	SMPS2_SW	SMPS2_IN	SMPS3_IN	SMPS3_SW	LDO4_OUT	LDO34_IN	GND_DIG	VPROG
11	VCC_SENSE2	PBKG	RPWRON	SMPS1_IN	SMPS1_SW	SMPS2_SW	SMPS2_IN	SMPS3_IN	SMPS3_SW	LDO3_OUT	SMPS8_FDBK	CLK32KGO	GPIO_6
10	LDOUSB_IN1	PBKG	GPIO_5	SMPS1_GND	SMPS1_GND	SMPS2_GND	SMPS2_GND	SMPS3_GND	SMPS3_GND	GPIO_4	SMPS8_GND	SMPS8_SW	SMPS8_SW
9	LDOUSB_IN2	LDOUSB_OUT	NC	VIO_IN	SMPS1_GND	SMPS2_GND	GPIO_7	GPIO_3	SMPS3_GND	RESET_IN	SMPS8_GND	SMPS8_IN	SMPS8_IN
8	LDOVRTC_OUT	SYNCDCDC	LDOVANA_OUT	VBUS	PBKG	REGEN1	PWRON	I2C2_SDA_SDO	SMPS9_FDBK	PWRDOWN	SMPS9_GND	SMPS9_IN	SMPS9_IN
7	GND_ANA	VBG	VCC1	PBKG	GND_ANA	PBKG	PBKG	PBKG	POWERGOOD	BOOT1	SMPS9_GND	SMPS9_SW	SMPS9_SW
6	LDO12_IN	LDO2_OUT	LDO1_OUT	PBKG	NRESWARM	PBKG	RESET_OUT	PBKG	PBKG	SMPS6_FDBK	SMPS6_GND	SMPS6_IN	SMPS6_IN
5	LDO9_OUT	LDOLN_OUT	LDOLN_IN	SMPS7_GND	NSLEEP	GND_ANA	SMPS4_GND	SMPS5_GND	ENABLE1	NC	SMPS6_GND	SMPS6_SW	SMPS6_SW
4	REFGND1	GPADC_VREF	LDO9_IN	SMPS7_GND	SMPS7_GND	SMPS4_GND	SMPS4_GND	SMPS5_GND	SMPS5_GND	NC	NC	LDO_SUPPLY	LDO_SUPPLY
3	OSC16MIN	VCC_SENSE	GPADC_IN2	SMPS7_SW	SMPS7_IN	SMPS4_IN	SMPS4_SW	SMPS5_SW	SMPS5_IN	SMPS4_5_FDBK_GND	BOOT0	I2C2_SCL_SCE	LDO_SUPPLY
2	OSC16MOUT	GPADC_IN0	GPADC_IN1	SMPS7_SW	SMPS7_IN	SMPS4_IN	SMPS4_SW	SMPS5_SW	SMPS5_IN	SMPS4_5_FDBK	I2C1_SDA_SDI	PBKG	VIO_GND
1	PBKG	SMPS7_FDBK	OSC16MCAP	SMPS7_SW	SMPS7_IN	SMPS4_IN	SMPS4_SW	SMPS5_SW	SMPS5_IN	INT	I2C1_SCL_SCK	PBKG	PBKG

Figure 3-1. 169-Pin ZWS New Fine Pitch Ball Grid Array (NFBGA) With 0,8-mm Pitch Top View

Pin Functions

PIN		I/O	PU OR PD(1)	CONNECTION IF NOT USED OR NOT AVAILABLE	DESCRIPTION
NO.	NAME				
A1	PBKG	—	—	Ground	Substrate ground
A2	OSC16MOUT	O	—	Floating	16-MHz crystal oscillator output or floating in case of digital clock
A3	OSC16MIN	I	—	Floating or ground in bypass mode	16-MHz crystal oscillator input or digital clock input
A4	REFGND1	—	—	Ground	System reference ground
A5	LDO9_OUT	O	—	Floating	LDO9 output voltage
A6	LDO12_IN	I	—	System supply	Power input voltage for LDO1 and LDO2 regulators
A7	GND_ANA	—	—	Ground	Analog power ground
A8	LDOVRTC_OUT	O	—	—	Internal LDOVRTC output voltage. For silicon revisions 1.3 or earlier, rapid power off and on requires a pulldown resistor on the LDOVRTC_OUT pin. See 节 5.4.11 for more details.
A9	LDOUSB_IN2	I	—	System supply	Power input voltage 2 for LDOUSB regulator
A10	LDOUSB_IN1	I	—	System supply	Power input voltage 1 for LDOUSB regulator
A11	VCC_SENSE2	I	—	System supply	System-supply sense line
A12	GPIO_2	I/O	PPU / PPD	Floating	**Primary function**: General-purpose input(2) or output
		O	—		**Secondary function**: REGEN2 — External regulator enable output 2
A13	PBKG	—	—	Ground	Substrate ground
B1	SMPS7_FDBK	I	—	Floating	Output voltage-sense (feedback) input for step-down converter, SMPS7
B2	GPADC_IN0	I	—	Ground	Sigma-delta GPADC input 0
B3	VCC_SENSE	I	—	System supply	System-supply sense line
B4	GPADC_VREF	O	—	Floating	Sigma-delta GPADC output reference voltage
B5	LDOLN_OUT	O	—	Floating	Output voltage for the low-noise dropout regulator, LDOLN
B6	LDO2_OUT	O	—	Floating	LDO2 output voltage
B7	VBG	O	—	—	Bandgap reference voltage
B8	SYNCDCDC	I	—	Ground	Sync pin to sync DC-DCs with external clock
B9	LDOUSB_OUT	O	—	Floating	LDOUSB output voltage
B10, B11	PBKG	—	—	Ground	Substrate ground
B12	GPIO_0	I/O	PPD	Ground or VSYS (VCC1)	General-purpose input(2) or output
B13	SMPS1_2_FDBK	I	—	Ground	Output voltage-sense (feedback) input for step-down converters, SMPS1 and SMPS2
C1	OSC16MCAP	O	—	Floating	Filtering capacitor for the 16-MHz crystal oscillator
C2	GPADC_IN1	I	—	Ground	Sigma-delta GPADC input 1
C3	GPADC_IN2	I	—	Ground	Sigma-delta GPADC input 2
C4	LDO9_IN	I	—	System supply	Power input voltage for LDO9 regulator
C5	LDOLN_IN	I	—	System supply	Power input voltage for the low-noise dropout regulator, LDOLN
C6	LDO1_OUT	O	—	Floating	LDO1 output voltage
C7	VCC1	I	—	System supply	Analog input voltage supply
C8	LDOVANA_OUT	O	—	—	Internal LDOVANA output voltage
C9	NC	—	—	—	Not connected
C10	GPIO_5	I/O	PPU / PPD(2)	Ground	**Primary function**: General-purpose input(2) or output
		O	—	Floating	**Secondary function**: CLK32KGO1V8 — 32-kHz digital-gated output clock available when VRTC is present
C11	RPWRON	I	PU	Floating	External remote switch-on event
C12	SMPS1_2_FDBK_GND	I	—	Ground	Ground-sense (feedback) input for step-down converters, SMPS1 and SMPS2
C13	GPIO_1	I/O	PPU	Floating	**Primary function**: General-purpose input(2) or output
		O	PPD		**Secondary function**: VBUSDET - VBUS detection

(1) The PU/PD column shows the pullup and pulldown resistors on the digital input lines. The pullup and pulldown resistors are defined as follows:

PU pullup

PD pulldown

PPU software-programmable pullup

PPD software-programmable pulldown

(2) Default option

Pin Functions (continued)

PIN NO.	PIN NAME	I/O	PU OR PD[1]	CONNECTION IF NOT USED OR NOT AVAILABLE	DESCRIPTION
D1 D2 D3	SMPS7_SW	O	—	Floating	Switch node of step-down converter, SMPS7. Connect the output to an inductor.
D4 D5	SMPS7_GND	—	—	Ground	Power ground connection for step-down converter, SMPS7
D6 D7	PBKG	—	—	Ground	Substrate ground
D8	VBUS	I	—	Ground	VBUS Detection Voltage
D9	VIO_IN	I	—	System supply	Digital supply input for GPIOs and I/O supply voltage
D10	SMPS1_GND	—	—	Ground	Power ground connection for step-down converter, SMPS1
D11 D12 D13	SMPS1_IN	I	—	System supply	Power input for step-down converter, SMPS1
E1 E2 E3	SMPS7_IN	I	—	System supply	Power input for step-down converter, SMPS7
E4	SMPS7_GND	—	—	Ground	Power ground connection for step-down converter, SMPS7
E5	NSLEEP	I	PPU[2] PPD	Floating	NSLEEP request signal
E6	NRESWARM	I	PPU[2]	Floating	Warm reset input
E7	GND_ANA	—	—	Ground	Analog power ground
E8	PBKG	—	—	Ground	Substrate ground
E9 E10	SMPS1_GND	—	—	Ground	Power ground connection for step-down converter, SMPS1
E11 E12 E13	SMPS1_SW	O	—	Floating	Switch node of step-down converter, SMPS1. Connect the output to an inductor.
F1 F2 F3	SMPS4_IN	I	—	System supply	Power input for step-down converter, SMPS4
F4	SMPS4_GND	—	—	Ground	Power ground connection for step-down converter, SMPS4
F5	GND_ANA	—	—	Ground	Analog power ground
F6 F7	PBKG	—	—	Ground	Substrate ground
F8	REGEN1	O	—	Floating	External regulator enable output 1
F9 F10	SMPS2_GND	—	—	Ground	Power ground connection for step-down converter, SMPS2
F11 F12 F13	SMPS2_SW	O	—	Floating	Switch node of step-down converter, SMPS2. Connect the output to an inductor.
G1 G2 G3	SMPS4_SW	O	–	Floating	Switch node of step-down converter, SMPS4. Connect the output to an inductor.
G4 G5	SMPS4_GND	—	—	Ground	Power ground connection for step-down converter, SMPS4
G6	RESET_OUT	O	—	Floating	System reset and power on output (Low → Reset, High → Active or Sleep)
G7	PBKG	—	—	Ground	Substrate ground
G8	PWRON	I	PU	Floating	External power-on event (on-button switch-on event)
G9	GPIO_7	I/O	PPD	Ground or VRTC	**Primary function**: General-purpose input[2] or output
		I	PPD[2]		**Secondary function**: POWERHOLD input
G10	SMPS2_GND	—	—	Ground	Power ground connection for step-down converter, SMPS2
G11 G12 G13	SMPS2_IN	I	—	System supply	Power input for step-down converter, SMPS2

Pin Functions (continued)

PIN		I/O	PU OR PD[(1)]	CONNECTION IF NOT USED OR NOT AVAILABLE	DESCRIPTION
NO.	NAME				
H1, H2, H3	SMPS5_SW	O	—	Floating	Switch node of step-down converter, SMPS5. Connect the output to an inductor.
H4, H5	SMPS5_GND	—	—	Ground	Power ground connection for step-down converter, SMPS5
H6, H7	PBKG	—	—	Ground	Substrate ground
H8	I2C2_SDA_SDO	I/O	—	Floating	DVS I^2C serial bidirectional data (external pullup) and SPI data read signal or I^2C serial bidirectional data (external pullup)
H9	GPIO_3	I	PPD	Ground	General-purpose input[(2)] or output
H10	SMPS3_GND	—	—	Ground	Power ground connection for step-down converter, SMPS3
H11, H12, H13	SMPS3_IN	I	—	System supply	Power input for step-down converter, SMPS3
J1, J2, J3	SMPS5_IN	I	—	System supply	Power input for step-down converter, SMPS5
J4	SMPS5_GND	—	—	Ground	Power ground connection for step-down converter, SMPS5
J5	ENABLE1	I	PPU PPD[(2)]	Floating	Peripheral power request input 1
J6	PBKG	—	—	Ground	Substrate ground
J7	POWERGOOD	O	—	Floating	Indication signal for valid regulator output voltages
J8	SMPS9_FDBK	I	—	Ground	Output voltage-sense (feedback) input for step-down converter, SMPS9
J9, J10	SMPS3_GND	—	—	Ground	Power ground connection for step-down converter, SMPS3
J11, J12, J13	SMPS3_SW	O	—	Floating	Switch node of step-down converter, SMPS3. Connect the output to an inductor.
K1	INT	O	—	—	Maskable interrupt output request to the host processor
K2	SMPS4_5_FDBK	I	—	Ground	Output voltage-sense (feedback) input for step-down converters, SMPS4 and SMPS5
K3	SMPS4_5_FDBK_GND	I	—	Ground	Ground-sense (feedback) input for step-down converters, SMPS4 and SMPS5
K4, K5	NC	—	—	—	Not connected
K6	SMPS6_FDBK	I	—	Ground	Output voltage sense (feedback) input for step-down converter, SMPS6
K7	BOOT1	I	—	Ground or VRTC	Boot pin 1 for power-up sequence selection
K8	PWRDOWN	I	PPD	Floating	Power-down signal
K9	RESET_IN	I	PPD	Floating	Reset input
K10	GPIO_4	I/O	PPU PPD[(2)]	Floating	**Primary function**: General-purpose input[(2)] or output
		O			**Secondary function**: SYSEN1 — External system enable
K11	LDO3_OUT	O	—	Floating	LDO3 output voltage
K12	LDO4_OUT	O	—	Floating	LDO4 output voltage
K13	SMPS3_FDBK	I	—	Floating	Output voltage-sense (feedback) input for step-down converter, SMPS3
L1	I2C1_SCL_SCK	I/O	—	Floating	Control I^2C serial clock (external pullup) and SPI clock signal
L2	I2C1_SDA_SDI	I/O	—	Floating	Control I^2C serial bidirectional data (external pullup) and SPI data signal
L3	BOOT0	I	—	Ground or VRTC	Boot pin 0 for power-up sequence selection
L4	NC	—	—	—	Not connected
L5, L6	SMPS6_GND	—	—	Ground	Power ground connection for step-down converter, SMPS6
L7, L8	SMPS9_GND	—	—	Ground	Power ground connection for step-down converter, SMPS9
L9, L10	SMPS8_GND	—	—	Ground	Power ground connection for step-down converter, SMPS8
L11	SMPS8_FDBK	I	—	Ground	Output voltage-sense (feedback) input for step-down converter, SMPS8

Pin Functions (continued)

PIN		I/O	PU OR PD[1]	CONNECTION IF NOT USED OR NOT AVAILABLE	DESCRIPTION
NO.	NAME				
L12 L13	LDO34_IN	I	—	System supply	Power input voltage for LDO3 and LDO4 regulators
M1 M2	PBKG	—	—	Ground	Substrate ground
M3	I2C2_SCL_SCE	I/O	—	Floating	DVS I^2C serial clock (external pullup) and SPI enable signal or I^2C serial clock (external pullup)
M4	LDO_SUPPLY	I	—	System supply	Power input voltage for internal LDO
M5	SMPS6_SW	O	—	Floating	Switch node of step-down converter, SMPS6. Connect the output to an inductor.
M6	SMPS6_IN	I	—	System supply	Power input for step-down converter, SMPS6
M7	SMPS9_SW	O	—	Floating	Switch node of step-down converter, SMPS9 Connect the output to an inductor.
M8	SMPS9_IN	I	—	System supply	Power input for step-down converter, SMPS9
M9	SMPS8_IN	I	—	System supply	Power input for step-down converter, SMPS8
M10	SMPS8_SW	O	—	Floating	Switch node of step-down converter, SMPS8 Connect the output to an inductor.
M11	CLK32KGO	O	—	Floating	32-kHz digital-gated output clock available when VIO_IN input supply is present
M12	GND_DIG	—	—	Ground	Digital power ground
M13	GND_ANA	—	—	Ground	Analog power ground
N1	PBKG	—	—	Ground	Substrate ground
N2	VIO_GND	—	—	Ground	Digital ground connection
N3	LDO_SUPPLY	I	—	System supply	Power input voltage for internal LDO
N4	LDO_SUPPLY	I	—	System supply	Power input voltage for internal LDO
N5	SMPS6_SW	O	—	Floating	Switch node of step-down converter, SMPS6. Connect the output to an inductor.
N6	SMPS6_IN	I	—	System supply	Power input for step-down converter, SMPS6
N7	SMPS9_SW	O	—	Floating	Switch node of step-down converter, SMPS9 Connect the output to an inductor.
N8	SMPS9_IN	I	—	System supply	Power input for step-down converter, SMPS9
N9	SMPS8_IN	I	—	System supply	Power input for step-down converter, SMPS8
N10	SMPS8_SW	O	—	Floating	Switch node of step-down converter, SMPS8 Connect the output to an inductor.
N11	GPIO_6	I/O	PPU PPD[2]	Ground	**Primary function**: General-purpose input[2] or output
		O	—	Floating	**Secondary function**: SYSEN2 — External system enable
N12	VPROG	I	—	Ground or floating	**Primary function**: OTP programming voltage
		O	—	Floating	**Secondary function**: TESTV
N13	PBKG	—	—	Ground	Substrate ground

Table 3-1. Summary of Digital Signals and Some Dedicated Analog Signals

SIGNAL NAME	POWER DOMAIN AND TOLERANCE LEVEL	I/O	INPUT PU/PD (1)	OTP PU/PD SELECTION	OUTPUT TYPE SELECTION	ACTIVE HIGH OR LOW	OTP POLARITY SELECTION
PWRON	VSYS (VCC1)	Input	PU fixed	N/A (fixed)	N/A (input)	Low	No
RPWRON	VSYS (VCC1)	Input	PU fixed	N/A (fixed)	N/A (input)	Low	No
PWRDOWN	VRTC, fail-safe (5.25-V tolerance)	Input	PPD (2) (Optional External PU)	Yes	N/A (input)	Low or high (2)	Yes
POWERGOOD	VRTC	Output	N/A (output)	N/A (output)	Open-drain	Low or high (2)	Yes
BOOT0	VRTC	Input	No	No	N/A (input)	Boot conf.	No
BOOT1	VRTC	Tri-level input	PPU or PPD (2)	No	N/A (input)	Boot conf.	No
GPIO_0	VRTC, fail-safe (5.25-V tolerance)	Input (2) or output	PPD (2)	Yes	Open-drain	Low or high	No
GPIO_1 (primary function)	VSYS	Input (2) or output	PPU/PPD (2)	Yes	Push-pull (2) or open- drain	Low or high	No
GPIO_1 secondary function: VBUSDET		Output	N/A (output)	N/A (output)	Push-pull (2) or open- drain	High	
GPIO_2 (primary function)	VSYS	Input (2) or output	PPU or PPD (2)	Yes	Push-pull (2) or open- drain	Low or high	No
GPIO_2 secondary function: REGEN2		Output	N/A (output)	N/A (output)	Push-pull (2) or open- drain	High	
GPIO_3	VRTC, fail-safe (5.25-V tolerance)	Input (2) or output	PPD (2)	Yes	Open-drain	Low or high (2)	Yes
GPIO_4 (primary function)	VIO (VIO_IN)	Input (2) or output	PPU/PPD (2)	No	Push-pull	Low or high	No
GPIO_4 secondary function: SYSEN1		Output	N/A (output)	N/A (output)		High	
GPIO_5 (primary function)	VRTC	Input (2) or output	PPU/PPD (2)	No	Push-pull (2) or open- drain	Low or high	No
GPIO_5 secondary function: CLK32KGO1V8 or SYNCCLKOUT		Output	N/A (output)	N/A (output)	Push-pull	Toggling	No

(1) The pullup and pulldown resistors are defined as follows:

PU pullup

PD pulldown

PPU software-programmable pullup

PPD software-programmable pulldown

(2) Default option.

Table 3-1. Summary of Digital Signals and Some Dedicated Analog Signals (continued)

SIGNAL NAME	POWER DOMAIN AND TOLERANCE LEVEL	I/O	INPUT PU/PD [1]	OTP PU/PD SELECTION	OUTPUT TYPE SELECTION	ACTIVE HIGH OR LOW	OTP POLARITY SELECTION
GPIO_6 (primary function)	VIO (VIO_IN)	Input[2] or output	PPU/PPD[2]	No	Push-pull	Low or high	No
GPIO_6 secondary function: SYSEN2		Output	N/A (output)	N/A (output)		High	
GPIO_7 (primary function)	VRTC, fail-safe (5.25-V tolerance)	Input[2] or output	PPD[2]	Yes	Open-drain	Low or high	No
GPIO_7 secondary function: POWERHOLD		Input	PD fixed	No	N/A (input)	High	
NSLEEP	VRTC	Input	PPU[2] or PPD	No	N/A (input)	Low[2] or high	No but software possible
ENABLE1	VIO (VIO_IN)	Input	PPU or PPD[2]	No	N/A (input)	Low or high[2]	No but software possible
REGEN1	VSYS (VCC1)	Output	N/A (output)	N/A (output)	Push-pull or open- drain (OTP selection)	High	No
RESET_IN	VRTC, fail-safe (5.25-V tolerance)	Input	PPD[2]	Yes	N/A (input)	Low[2] or high	Yes
RESET_OUT	VIO (VIO_IN)	Output	N/A (output)	N/A (output)	Push-pull	Low	No
NRESWARM	VRTC	Input	PPU[2]	No	N/A (input)	Low	No
INT	VIO (VIO_IN)	Output	N/A (output)	N/A (output)	Push-pull[2] or open- drain	Low[2] or high	No but software possible
CLK32KGO	VIO (VIO_IN)	Output	N/A (output)	N/A (output)	Push-pull	Toggling	No
I2C1_SDA_SDI	VIO (VIO_IN)	Input or output	No	No	Open-drain	High (I^2C)	Yes (I^2C/SPI)
I2C1_SCL_SCK	VIO (VIO_IN)	Input	No	No	N/A (input)	High (I^2C)	Yes (I^2C/SPI)
I2C2_SCL_SCE	VIO (VIO_IN)	Input	No	No	N/A (input)	High (I^2C)	Yes (I^2C/SPI)
I2C2_SDA_SD0	VIO (VIO_IN)	Input or output	No	No	Open-drain (I^2C) or Push-pull (SPI)	High (I^2C)	Yes (I^2C/SPI)
GPADC_IN0	VRTC	Input	No	No	N/A (analog)	Analog	No
GPADC_IN1	VANA	Input	No	No	N/A (analog)	Analog	No
GPADC_IN2	VANA	Input	No	No	N/A (analog)	Analog	No
GPADC_VREF	VANA	Output	No	No	N/A (analog)	Analog	No
OSC16MIN	VRTC	Input	No	No	N/A (analog)	Analog	No
OSC16MOUT	VRTC	Output	No	No	N/A (analog)	Analog	No
VCC_SENSE2	VSYS (VCC1)	Input	No	No	N/A (analog)	Analog	No
VCC_SENSE	VSYS (VCC1)	Input	No	No	N/A (analog)	Analog	No

4 Specifications

4.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[(1)(2)]

			MIN	MAX	UNIT
Voltage	VCC1 pins		–0.3	6	V
	VCC_SENSE, VCC_SENSE2 pins		–0.3	7	V
	All LDOs and SMPS supply voltage input pins (except LDOUSB_IN2)		–0.3	6	V
	SMPSx_SW pins, 10 ns transient		–2	7	V
	All SMPS-related input pins, SMPSx_FDBK		–0.3	3.6	V
	LDOUSB regulator LDOUSB_IN2 input voltage		–0.3	20	V
	I/O digital supply voltage[(3)]		–0.3 V_{IOmax} + 0.3	V_{IOmax} + 0.3	V
	VBUS		–2	20	V
	GPADC pins: GPADC_IN0, GPADC_IN1		–0.3	5.25	V
	GPADC pins: GPADC_IN2		–0.3	2.5	V
	OTP supply voltage VPROG		–0.3	20	V
	VRTC digital input pins	Without fail-safe	–0.3	2.15	V
		With fail-safe	–0.3	5.25	
	VIO digital input pins (VIO_IN pin reference)		–0.3	V_{IOmax} + 0.3	V
	VSYS digital input pins (VCC1 pin reference)		–0.3	6	V
Current	Peak output current on all pins other than power resources		–5	5	mA
	Power pins, nFBGA			1	A
	Buck SMPS, SMPSx_IN, SMPSx_SW, and SMPSx_OUT total per phase			4	A
	LDOs			1	A
Junction temperature range, T_J			–45	150	°C
Storage temperature range, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum conditions for extended periods may affect device reliability.
(2) When operating the TPS659037 device without an external crystal, each SMPS regulating an output voltage greater than 1.8 V must be disabled before VCC is removed. Lowering VCC below the programmed VSYS_LO level while any SMPS is regulating an output voltage above 1.8 V may cause damage to the device.
(3) VIO_IN with respect to VIO_GND.

4.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS–001[(1)]		±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[(2)]	Pins B4, B7, H8, L1, L2, M3	±450	V
			All other pins	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
All system voltage input pins VCC1 (named VSYS in the specification)	3.135	3.8	5.25	V
VCC_SENSE and VCC_SENSE2, HIGH_VCC_SENSE = 0 (1)	3.135		V_{VCC1}	V
VCC_SENSE and VCC_SENSE2, HIGH_VCC_SENSE = 1 (1)	3.135		$V_{VCC1} – 1$	V
All LDO-related input pins _IN (except LDOUSB) (2)	1.75	3.8	5.25	V
LDOUSB_IN1	3.6		5.25	V
LDOUSB_IN2	4.3		5.25	V
All SMPS-related input pin _IN	3.135	3.8	5.25	V
All SMPS-related input pins _FDBK	0		V_{Omax} + 0.3	V
All SMPS-related input pins _FDBK_GND	–0.3		0.3	V
I/O digital supply voltage VIO_IN, for 1.8-V Mode	1.71	1.8	1.89	V
I/O digital supply voltage VIO_IN, for 3.3-V Mode	3.135	3.3	3.465	V
Voltage on the GPADC pins GPADC_IN0, GPADC_IN1 pins	0		1.25	V
Voltage on the GPADC pins GPADC_IN2 pin	0		2.5	V
Voltage on the crystal oscillator OSC16MIN pin	-0.7	$V_{LDOVRTC}$	1.85	V
OTP supply voltage VPROG	0	8	10	V
Voltage on VRTC digital input pins	0	$V_{LDOVRTC}$	1.85	V
Voltage on VIO digital input pins (VIO_IN pin reference)	0	V_{IO}	V_{IOmax}	V
Voltage on VSYS digital input pins (VCC1 pin reference)	0	3.8	5.25	V
Operating free-air temperature range (3)	–40	27	85	°C
Operating Junction temperature	–40	27	125	°C

(1) If measured with GPADC, see 表 5-3.
(2) Does not include LDO1 and LDO2 minimum input voltages.
(3) Additional cooling strategies may be necessary to maintain junction temperature at recommended limits.

4.4 Thermal Information

THERMAL METRIC (1)		TPS659037 ZWS (NFBGA) 169 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	6.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

4.5 Electrical Characteristics: Latch Up Rating

Over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LU}	Latch up current, Class 2	I^2C and SPI pins				90	mA
		LDOVANA_OUT pin		–60			
		All other pins				100	

4.6 Electrical Characteristics: LDO Regulator

Over operating free-air temperature range, typical values are at T_A = 27°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Input filtering capacitance (C29, C30, C31, C32, C33, C34)	Connected from LDOx_IN to GND. Shared input tank capacitance (depending on platform requirements)		0.6	2.2		µF
	Output filtering capacitance (C35, C36, C37, C38, C45, C46, C47)(1)	Connected from LDOx_OUT to GND (Except LDO9)		0.6	2.2	2.7	µF
	LDO9 Output filtering capacitance (C44)(1)	Connected from LDO9_OUT to GND		0.6	2.2	2.7	µF
		Connected from LDO9_OUT to GND. LDO9 configured in BYPASS MODE (LDO9_CTRL.LDO_PYPASS_EN = 1)		0.6	1	1.2	
C_{ESR}	Filtering capacitor ESR	< 100 kHz		20	100	600	mΩ
		1 MHz ≤ f ≤ 10 MHz		1	10	20	mΩ
V_{LDOx}	Input voltage, LDOx	LDO1, LDO2	0.9 V ≤ V_O ≤ 2.15 V	1.2		V_{VCC1}	V
			2.2 V ≤ V_O ≤ 3.3 V	1.2		5.25	
		LDOLN, LDO3, LDO4	0.9 V ≤ V_O ≤ 2.15 V	1.75		V_{VCC1}	
			2.2 V ≤ V_O ≤ 3.3 V	1.75		5.25	
		LDO9	0.9 V ≤ V_O ≤ 1.75 V	1.75		V_{VCC1}	
			1.8 V ≤ V_O ≤ 3.3 V	1.75		5.25	
			Bypass Mode	1.75		3.6	
$V_{LDOUSB1}$	Input voltage, LDOUSB1	LDOUSB – From LDOUSB_IN1	0.9 V ≤ V_O ≤ 2.15 V	3.6		V_{VCC1}	V
			2.2 V ≤ V_O ≤ 3.3 V	3.6		5.25	
$V_{LDOUSB2}$	Input voltage, LDOUSB2	LDOUSB – From LDOUSB_IN2	0.9 V ≤ V_O ≤ 2.15 V	4.3		V_{VCC1}	V
			2.2 V ≤ V_O ≤ 3.3 V	4.3		5.25	
$V_{I(VCC1)}$	Input voltage, VCC1	VCC1 – Used for internal power supply		3.135	3.8	5.25	V
$V_{O(LDOx)}$	LDO output voltage programmable(2) (except LDOVRTC and LDOVANA)	$V_{O(LDOx)} < V_{LDOx} – V_{DROPOUT(LDOx)}$		0.9		3.3	V
		Step size			50		mV
$T_{DCOV(LDOx)}$	Total DC output voltage accuracy, including voltage references, DC load/line regulations, process and temperature	All LDOs except LDO3, LDO4, LDOVANA, and LDOVRTC		0.99 × $V_{O(LDOx)}$ –0.014		1.006 × $V_{O(LDOx)}$ + 0.014	V
		LDO3, LDO4: I_O = 200 mA		0.99 × $V_{O(LDOx)}$ –0.014		1.006 × $V_{O(LDOx)}$ + 0.014	
		LDO3, LDO4: 200 mA < I_O ≤ 300 mA		0.99 × $V_{OUT(LDOx)}$ – 0.018		1.006 × $V_{OUT(LDOx)}$ + 0.018	
		LDOVRTC_OUT		1.726	1.8	1.85	
		LDOVANA_OUT		2.002	2.093	2.119	
$V_{DROPOUT(LDOx)}$	Dropout voltage(3)	LDO1, LDO2: $I_O = I_{Omax}$				150	mV
		LDO3, LDO4: I_O = 200 mA				290	
		LDO3, LDO4: $I_O = I_{Omax}$				550	
		LDO9: $I_O = I_{Omax}$				230	
		LDOLN: $I_O = I_{Omax}$				150	
		LDOLN: I_O = 100 mA (Functional, not low-noise performance)				290	
		LDOUSB – From LDOUSB_IN1: $I_O = I_{Omax}$				200	
		LDOUSB – From LDOUSB_IN2: $I_O = I_{Omax}$				900	
$V_{DROPOUT(LDOx)}$	Dropout voltage, internal LDOs	LDOVRTC, LDOVANA: $I_O = I_{Omax}$				150	mV
$I_{O(LDOx)}$	Output current	LDO1, LDO2				300	mA
		LDO3, LDO4				300	
		LDO9, LDOLN				50	
		LDOUSB				100	
$I_{O(LDOx\_int)}$	Output current, internal LDOs	LDOVANA				10	mA
		LDOVRTC				25	
	LDO inrush current	LDO1, LDO2				500	mA

(1) Additional information about how this parameter is specified is located in 节 6.2.2.
(2) LDO output voltages are programmed separately.
(3) $V_{DROPOUT(LDOx)} = V_I – V_O$, where $V_O = V_O$nom – 2%

Electrical Characteristics: LDO Regulator *(continued)*

Over operating free-air temperature range, typical values are at T_A = 27°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{L(LDOx)}$	LDO current limitation	LDO1, LDO2	380	600	1800	mA
		LDO3, LDO4	400	650	1300	
		LDO9	120	200	400	
		LDOUSB	120	250	600	
		LDOLN	150	325	740	
		LDOVANA	100	250	400	
		LDOVRTC	55	250	400	
$\Delta V_{O(\Delta VI)(DC)}$	DC load regulation, ΔV_O	LDO1, LDO2: I_O = 0 to I_{Omax} at pin		4	16	mV
		LDO3, LDO4: 0 to 200 mA at pin		4	14	
		LDO3, LDO4: I_O = 0 to I_{Omax} at pin		4	18	
		All other LDOs: I_O = 0 to I_{Omax} at pin		4	14	
$\Delta V_{O(DVI)(DC)}$	DC line regulation, except VRTC, ΔV_O / V_O	$V_I = V_{Imin}$ to V_{Imax}, $I_O = I_{Omax}$		0.1%	0.2%	
		$V_{SYS} = V_{SYSmin}$ to V_{SYSmax}, $_{IO} = I_{Omax}$. V_I constant (LDO preregulated), V_O ≤ 2.2 V		0.3%	0.75%	
	DC line regulation on LDOVRTC, $\Delta V_O/V_O$	$V_{SYS} = V_{SYSmin}$ to V_{SYSmax}, $I_O = I_{Omax}$			1%	
	Bypass resistance of LDO9	V_I ≥ 2.7 V, programmed to BYPASS			4.2	Ω
t_{on}	Turnon time	I_O = 0, V_O = 0.1 V up to V_{Omin}		100	500	µs
t_{off}	Turnoff time (except VRTC)	I_O = 0, V_O down to 10% × V_O		250	500	µs
R_{DIS}	Pulldown discharge resistance at LDO output, except LDOVRTC	OFF mode, pull down enabled and LDO disabled. Also applies to bypass mode	30		125	Ω
	Power-supply ripple rejection, LDO1, LDO2	f = 217 Hz, $I_O = I_{Omax}$	55	90		dB
		f = 50 kHz, $I_O = I_{Omax}$	28	45		
		f = 1 MHz, $I_O = I_{Omax}$	25	35		
	Power-supply ripple rejection, LDO3, LDO4,LDO9, LDOUSB	LDO9, LDOUSB: f = 217 Hz, $I_O = I_{Omax}$	55	90		dB
		LDO3, LDO4: f = 217 Hz, $I_O = I_{Omax}$	50	60		
		LDO3, LDO4: f = 217 Hz, I_O = 200 mA	55	90		
		All other LDOs: f = 50 kHz, $I_O = I_{Omax}$	20	45		
		All other LDOs: f = 1 MHz, $I_O = I_{Omax}$	20	35		
	Power-supply ripple rejection, LDOLN	f = 217 Hz, $I_O = I_{Omax}$	55	90		dB
		f = 50 kHz, $I_O = I_{Omax}$	25	45		
		f = 1 MHz, $I_O = I_{Omax}$	25	35		
$I_{Q(off)}$	Quiescent-current off mode	For all LDOs, T = 27°C		0.1		µA
		For all LDOs, T ≥ 85°C		0.2		
$I_{Q(on)}$	Quiescent-current LDO ON mode	I_L = 0 mA (LDO1, LDO2), 0.9 V ≤ V_O ≤ 3.3 V, $V_{O(LDOx)} < V_{LDOx} - V_{DROPOUT(LDOx)}$		39	70	µA
		I_L = 0 mA (LDO3, LDO4, LDO9), $V_{O(LDOx)} < V_{LDOx} - V_{DROPOUT(LDOx)}$		36	47	
		I_L = 0 mA (LDOLN) , V_O ≤ 1.8 V, $V_{O(LDOx)} < V_{LDOx} - V_{DROPOUT(LDOx)}$		140	190	
		I_L = 0 mA (LDOLN) , V_O > 1.8 V, $V_{O(LDOx)} < V_{LDOx} - V_{DROPOUT(LDOx)}$		180	210	
		I_L = 0 mA (LDOUSB) – IN1, $V_{O(LDOx)} < V_{LDOx} - V_{DROPOUT(LDOx)}$		45	65	
		I_L = 0 mA (LDOUSB) – IN2, $V_{O(LDOx)} < V_{LDOx} - D_{V(LDOx)}$		18	25	
αQ	Quiescent current coefficient, LDO ON mode(4)	I_O < 100 µA		4%		
		100 µA ≤ I_O < 1 mA		2%		
		I_O ≥ 1 mA		1%		
$\Delta V_{O(\Delta IO)(T)}$	Transient load regulation ΔV_O	All LDOs except LDO3, LDO4, LDO9, LDOLN: ON mode, I_O = 10 mA to I_{Omax} / 2, $t_r = t_f$ = 1 µs	–25		25	mV
		LDO9, LDOLN: ON mode, I_O = 1 mA to I_{Omax} /2, $t_r = t_f$ = 1 µs	–25		25	
		LDO3, LDO4: ON mode, I_O = 10 mA to 100 mA, $t_r = t_f$ = 1 µs	–25		25	
		LDO3, LDO4: ON mode, I_O = 10 mA to I_{Omax} / 2, $t_r = t_f$ = 1 µs	–40		25	
		ON mode, I_O = 100 µA to I_{Omax} / 2, $t_r = t_f$ = 1 µs	–50		33	
$\Delta V_{O(\Delta VI)(T)}$	Transient line regulation, ΔV_O / V_O	V_I step = 600 mV_{PP}, $t_r = t_f$ = 10 µs		0.25%	0.5%	
		V_{SYS} step = 600 mV_{PP}, $t_r = t_f$ = 10 µs. V_I constant (LDO preregulated), V_O ≤ 2.2 V		0.8%	1.6%	

(4) $I_{QO} = I_{Q(on)} + \alpha Q \times I_O$

Electrical Characteristics: LDO Regulator *(continued)*

Over operating free-air temperature range, typical values are at T_A = 27°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Noise (except LDOLN)	100 Hz < f ≤ 10 kHz		5000	8000	nV/√Hz
		10 kHz < f ≤ 100 kHz		1250	2500	
		100 kHz < f ≤ 1 MHz		150	300	
		f > 1 MHz		250	500	
	Noise (LDOLN)	100 Hz < f ≤ 5 kHz, I_O = 50 mA, V_O ≤ 1.8 V		400	500	nV/√Hz
		5 kHz < f ≤ 400 kHz, I_O = 50 mA, V_O ≤ 1.8 V		62	125	
		400 kHz < f ≤ 10 MHz, I_O = 50 mA, V_O ≤ 1.8 V		25	50	
	Ripple	LDO1, LDO2, ripple (from internal charge pump)			5	mV_{PP}

4.7 Electrical Characteristics: Dual-Phase (SMPS12 and SMPS45) and Triple-Phase (SMPS123 and SMPS457) Regulators

Over operating free-air temperature range, typical values are at T_A = 27°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input capacitance (C9, C10, C11, C12, C13)			4.7		µF
	Output capacitance (C18, C19, C21, C22)(1)	SMPS12 or SMPS45 dual phase operation, per phase	33	47	57	µF
	Output capacitance, (C20, C24)(1)	SMPS3 and SMPS7 (triple phase operation)	33	47	57	µF
C_{ESR}	Filtering capacitor ESR	1 MHz ≤ f ≤ 10 MHz		2	10	mΩ
	Output filter inductance (L1, L2, L3, L4, L5)	SMPSx_SW	0.7	1	1.3	µH
DCR_L	Filter inductor DC resistance			50	100	mΩ
V_{SMPSx}	Input voltage range, SMPSx_IN	Connected to V_{SYS} (VCC1)	3.135		5.25	V
V_OSMPSx	Output voltage, programmable, SMPSx	RANGE = 0 (value for RANGE must not be changed when SMPS is active). In Eco-mode the output voltage values are fixed (defined before Eco-mode is enabled). RANGE = 1 is not supported for Multi-phase regulators.	0.7		1.65	V
		Step size, 0.7 V ≤ V_O ≤ 1.65 V (RANGE = 0)		10		mV
	DC output voltage accuracy, includes voltage references, DC load/line regulation, process and temperature	Eco-mode	–3%		4%	
		Forced PWM mode	–1%		2%	
	Ripple, dual phase	Maximum load, V_I = 3.8 V, V_O = 1.2 V, ESR_{CO} = 2 mΩ, measure with 20-MHz LPF		4		mV_{PP}
	Ripple, triple phase	Maximum load, V_I = 3.8 V, V_O = 1.2 V, ESR_{CO} = 2 mΩ, measure with 20-MHz LPF		1		mV_{PP}
$\Delta V_{O(\Delta VI)}$	DC line regulation			0.1		%/V
$\Delta V_{O(\Delta IO)}$	DC load regulation			0.1		%/A
	Transient load step response, dual phase	I_O = 0.8 to 2 A, t_r = t_f = 400 ns, C_O = 47 µF , L= 1 µH		3%		
	Transient load step response, triple phase	I_O = 0.8 to 2 A, t_r = t_f = 400 ns, C_O = 47 µF , L= 1 µH		3%		
	Transient load step response, dual or triple phase	I_O = 0.5 to 500 mA, t_r = t_f = 100 ns, C_O = 47 µF , L= 1 µH		3%		
I_{Omax}	Rated output current, SMPS12	Advance thermal design is required to avoid thermal shutdown			6	A
	Rated output current, SMPS123	Advance thermal design is required to avoid thermal shutdown			9	
	Rated output current, SMPS45	Advance thermal design is required to avoid thermal shutdown			4	
	Maximum output current, Eco-mode				5	mA
$I_{(LIM\_HS\_FET)}$	High-side MOSFET forward current-limit	SMPS123, each phase	3.7	4		A
		SMPS45, each phase	2.7	3		
$I_{(LIM\_LS\_FET)}$	Low-side MOSFET forward current-limit	SMPS123, each phase		3.7		A
		SMPS45, each phase		2.7		
	Low-side MOSFET negative current-limit	SMPS123, phase 1		0.6		A
		SMPS45, phase 4		0.6		
$r_{DS(on\_HS\_FET)}$	N-channel MOSFET on-resistance, high-side FET	SMPS123, each phase		115		mΩ
		SMPS45, each phase		115		
$r_{DS(on\_LS\_FET)}$	N-channel MOSFET on-resistance, low-side FET	SMPS123, each phase		30		mΩ
		SMPS45, each phase		30		
$t_{(start)}$	Time from enable to start of the ramp			150		µs

(1) Additional information about how this parameter is specified is located in 节 6.2.2.

Electrical Characteristics: Dual-Phase (SMPS12 and SMPS45) and Triple-Phase (SMPS123 and SMPS457) Regulators *(continued)*

Over operating free-air temperature range, typical values are at T_A = 27°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(ramp)}$	Time from enable to 80% of V_O	C_O < 57 µF per phase, no load		400	1000	µs
	Overshoot during turnon				5%	
	Output voltage slew rate	Fixed TSTEP		2.5		mV/µs
$R_{(DIS)}$	Pulldown discharge resistance at SMPS2, SMPS4 output	SMPS turned off		300		Ω
		SMPSx_SW, SMPS turned off. Pulldown is at the master phase output.		9	22	
$R_{(SENSE)}$	Input resistance for remote sense/sense line	Between SMPS1_2_FDBK, SMPS1_2_FDBK_GND	380		1300	kΩ
		Between SMPS4_5_FDBK, SMPS4_5_FDBK_GND	380		1300	
		SMPS3_FDBK input resistance	380		1300	
$I_{Q(off)}$	Quiescent current – OFF mode	I_L = 0 mA		0.1	1	µA
$I_{Q(on)}$	Quiescent current -ON mode, dual or triple phase	Eco-mode, device not switching, V_O < 1.8 V		13.5	19	µA
		Eco-mode, device not switching, V_O ≥ 1.8 V		15	21	
		FORCED_PWM mode, I_L= 0 mA, V_I = 3.8 V, device switching, 1-phase operation		11		mA
V_{SMPSPG}	Powergood threshold	SMPS output voltage rising, referenced to programmed output voltage		–7.5%		
		SMPS output voltage falling, referenced to programmed output voltage		–12.5%		
IL_AVG_COMP	Powergood: GPADC monitoring SMPS	IL_AVG_COMP_rising	I_{Omax} – 20%	I_{Omax}	I_{Omax} + 20%	
		IL_AVG_COMP_falling, 3-A phase		IL_AVG_COMP_rising – 5%		
		IL_AVG_COMP_falling, 2-A phase		IL_AVG_COMP_rising – 8%		

4.8 Electrical Characteristics: Stand-Alone Regulators (SMPS3, SMPS6, SMPS7, SMPS8, and SMPS9)

Over operating free-air temperature range, typical values are at T_A = 27°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input capacitance (C11, C14, C15, C16, C17)			4.7		µF
	Output capacitance (C20, C23, C24, C25, C26)(1)	SMPSx operation	33	47	57	µF
C_{ESR}	Filtering capacitor DC ESR	1 MHz ≤ f ≤ 10 MHz		2	10	mΩ
	Output filter inductance (L3, L6, L7, L8, L9)	SMPSx_SW	0.7	1	1.3	µH
$L_{R(DC)}$	Filter inductor DC resistance			50	100	mΩ
V_{SMPSx}	Input voltage range, SMPSx_IN	Connected to VSYS (VCC1)	3.135		5.25	V
V_OSMPSx	Output voltage, programmable, SMPSx	RANGE = 0 (value for RANGE must not be changed when SMPS is active). In Eco-mode the output voltage value is fixed (defined before Eco-mode is enabled).	0.7		1.65	V
		RANGE = 1 (value for RANGE must not be changed when SMPS is active). In Eco-mode the output voltage value is fixed (defined before Eco-mode is enabled).	1		3.3	
		Step size, 0.7 V ≤ V_O ≤ 1.65 V		10		mV
		Step size, 1 V ≤ V_O ≤ 3.3 V		20		
	DC output voltage accuracy, includes voltage references, DC load/line regulation, process and temperature	Eco-mode	–3%		4%	
		PWM mode	–1%		2%	
	Ripple	Max load, V_I = 3.8 V, V_O = 1.2 V, ESR_{CO} = 2 mΩ, measure with 20-MHz LPF		8		mV_{PP}
DC_{LNR}	DC line regulation	T_A = –40°C to 85°C		0.1		%/V
DC_{LDR}	DC load regulation	T_A = –40°C to 85°C		0.1		%/A
T_{LDSR}	Transient load step response	SMPS3, SMPS6, SMPS7 , I_{OUT} = 0.5 to 500 mA, t_r = t_f = 100 ns, C_O = 47 µF , L = 1 µH		3%		
T_{LDSR}	Transient load step response	SMPS8, SMPS9, I_O = 0.5 to 500 mA, T_R = T_F = 1 µs, C_O = 47 µF , L = 1 µH		3%		
	Rated output current, SMPS3	V_I ≥ 3 V, Advance thermal design is required to avoid thermal shutdown			3	A
		V_I < 3 V, Advance thermal design is required to avoid thermal shutdown			2	

(1) Additional information about how this parameter is specified is located in 节 6.2.2.

Electrical Characteristics: Stand-Alone Regulators (SMPS3, SMPS6, SMPS7, SMPS8, and SMPS9) *(continued)*

Over operating free-air temperature range, typical values are at T_A = 27°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Rated output current, SMPS6	When OTP programmed with BOOST_CURRENT = 0 Advance thermal design is required to avoid thermal shutdown			2	A
		When OTP programmed with BOOST_CURRENT = 1 Advance thermal design is required to avoid thermal shutdown			3	
	Rated output current, SMPS7	Advance thermal design is required to avoid thermal shutdown			2	A
	Rated output current, SMPS8, SMPS9	Advance thermal design is required to avoid thermal shutdown			1	A
	Maximum output current, Eco-mode				5	mA
$I_{LIM\ HS\ FET}$	High-side MOSFET forward current limit	SMPS3, and SMPS6 in 3-A mode	3.7	4		A
		SMPS6 in 2-A mode, SMPS7	2.7	3		
		SMPS8, SMPS9	1.7	2		
$I_{LIM\ LS\ FET}$	Low-side MOSFET forward current limit	SMPS3, and SMPS6 in 3-A mode		3.7		A
		SMPS6 in 2-A mode, SMPS7		2.7		
		SMPS8, SMPS9		1.7		
	Low-side MOSFET negative current limit	SMPS3, and SMPS6 in 3-A mode		0.6		A
		SMPS6 in 2-A mode, SMPS7		0.6		
		SMPS8, SMPS9		0.6		
$r_{DS(on\_HS\_FET)}$	N-channel MOSFET on-resistance (high-side FET)	SMPS3		115		mΩ
		SMPS6, SMPS7		115		
		SMPS8, SMPS9		180		
$r_{DS(on\_LS\_FET)}$	N-channel MOSFET on-resistance (low-side FET)	SMPS3		30		mΩ
		SMPS6, SMPS7		30		
		SMPS8, SMPS9		79		
$t_{(start)}$	Time from enable to start of the ramp			150		µs
$t_{(ramp)}$	Time from enable to 80% of V_O	C_O < 57 µF, no load		400	1000	µs
	Overshoot during turnon				5%	
	Output voltage slew rate	Fixed TSTEP, only available on SMPS6, SMPS8		2.5		mV/µs
$R_{(DIS)}$	Pulldown discharge resistance at SMPSx output	SMPSx_FDBK, SMPS turned off		300		Ω
		SMPSx_SW, SMPS turned off		9	22	
$I_{Q(off)}$	Quiescent current – OFF mode	I_L = 0 mA		0.1	1	µA
$I_{Q(on\_SMPS3,6,7)}$	Quiescent current – ON mode - SMPS3, SMPS6, SMPS7	Eco-mode, device not switching, V_O < 1.8 V		12	15	µA
		Eco-mode, device not switching, V_O ≥ 1.8 V		13.5	23	
		FORCED_PWM mode, I_L = 0 mA, V_I = 3.8 V, device switching		11		mA
$I_{Q(on\_SMPS8,9)}$	Quiescent current – ON mode - SMPS8, SMPS9	Eco-mode, device not switching, V_O < 1.8 V		10.5	15	µA
		Eco-mode, device not switching, V_O ≥ 1.8 V		12	23	
		FORCED_PWM mode, I_L = 0 mA, V_I = 3.8 V, device switching		7		mA
V_{SMPSPG}	Powergood threshold	SMPS output voltage rising, referenced to programmed output voltage		–7.5%		
		SMPS output voltage falling, referenced to programmed output voltage		–12.5%		
	Powergood: GPADC monitoring SMPS	IL_AVG_COMP_rising	I_{Omax} – 20%	I_{Omax}	I_{Omax} + 20%	
		IL_AVG_COMP_falling, 3-A phase		IL_AVG_COMP_rising – 5%		
		IL_AVG_COMP_falling, 2-A phase		IL_AVG_COMP_rising – 8%		

4.9 Electrical Characteristics: Reference Generator (Bandgap)

Over operating free-air temperature range, typical values are at T_A = 27°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Filtering capacitor	Connected from VBG to REFGND	30	100	150	nF
V_I	Input voltage		2.1	3.8	5.25	V
	Output voltage			0.85		V
	Ground current			20	40	µA
	Start-up time			1	3	ms

4.10 Electrical Characteristics: 16-MHz Crystal Oscillator, 32-kHz RC Oscillator, and Output Buffers

Over operating free-air temperature range, typical values are at T_A = 27°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CRYSTAL CHARACTERISTICS					
Crystal frequency	Typical with specified load capacitors		16.384		MHz
Crystal frequency tolerance	Parameter of crystal; T_A 27°C	–30		30	ppm
Crystal motional inductance	Parameter of crystal	23	33	43	mH
Crystal series resistance	At fundamental frequency			90	Ω
Oscillator drive power	The power dissipated in the crystal during oscillator operation		15	120	µW
Load capacitance	Corresponding to crystal frequency, including parasitic capacitances	8	10	12	pF
Crystal shunt capacitance	Parameter of crystal	0.5		4	pF
Oscillator frequency drift	T_J from –40°C to 125°C, VCC1 from 3.15 V to 5.25 V Excluding crystal tolerance	–50		50	ppm
Oscillator startup time	Time from VCC1 > 3.15 V until 32-kHz clock output is available from crystal oscillator			10	ms
32-kHz RC OSCILLATOR					
Output frequency low-level output voltage			32768		Hz
Output frequency accuracy	After trimming, T_A 27°C	–10%	0	10%	
Cycle jitter (RMS)				10%	
Output duty cycle		40%	50%	60%	
Settling time				150	µs
Active current consumption			4	8	µA
Power-down current				30	nA
CLK32KGO OUTPUT BUFFER					
Logic output external load		5	35	50	pF
Rise and fall time	C_L = 35 pF, 10% to 90%	5	50	100	ns
Duty cycle	Logic output signal	40%	50%	60%	
CLK32KGO1 V8 OUTPUT BUFFER					
Settling time			25	50	µs
Active current consumption		5	7	10	µA
Power-down current				30	nA
Duty cycle degradation contribution		–2%		2%	
External output load		5	10	50	pF
Output delay time	Output load = 10 pF		15	30	ns
Output rise and fall time	Output load = 10 pF	7.5		20	ns
SYNCCLKOUT OUTPUT BUFFER					
Logic output external load		5	35	50	pF
Rise and fall time	C_L = 35 pF, 10% to 90%	5	50	100	ns

Electrical Characteristics: 16-MHz Crystal Oscillator, 32-kHz RC Oscillator, and Output Buffers *(continued)*

Over operating free-air temperature range, typical values are at T_A = 27°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Duty cycle	Logic output signal	40%	50%	60%	

4.11 Electrical Characteristics: DC-DC Clock Sync

Over operating free-air temperature range, typical values are at T_A = 27°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYNC CLOCK SPECIFICATION AND DITHER PARAMETERS						
$f_{(SYNC)}$	The allowed range of the external sync clock input		1.7	2.2	2.7	MHz
$A_{(DITHER)}$	Dither amplitude				128	kHz
$M_{(DITHER)}$	Dither slope				1.35	kHz/µs
SYNC DC-DC DIGITAL CLOCK INPUT						
V_{IL}	Low-level input on SYNCDCDC pin		–0.3	0	0.3 × V_{VRTC}	V
V_{IH}	High-level input on SYNCDCDC pin		0.7 × V_{VRTC}	V_{VRTC}	5.25	V
	Duty cycle of SYNCDCDC input signal		20%		80%	
	Hysteresis of input buffer		0.1 × V_{VRTC}			V
SYNC CLOCK AND FREQUENCY FALLBACK						
$f_{(FALLBACK)}$	Fall-back frequency		1.98	2.2	2.42	MHz
$f_{(SAT\_LO)}$	The low saturation frequency output of the PLL				1.65	MHz
$f_{(SAT\_HI)}$	The high saturation frequency output of the PLL		2.8			MHz
$f_{(SETTLE)}$	Time from initial application or removal of sync clock until PLL output has settled to 1% of its final value				100	µs
$f_{(ERROR)}$	The steady-state percent difference between f_{SYNC} and the switching frequency		–1%		1%	
t_d	Time delay between corresponding staggered phases		15	30	45	ns

4.12 Electrical Characteristics: 12-Bit Sigma-Delta ADC

Over operating free-air temperature range, typical values are at T_A = 27°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{Q(on)}$	Current consumption	During conversion		1500	1600	µA
$I_{Q(off)}$	OFF mode current	GPADC is not enabled (no conversion)			1	µA
f	Running frequency			2.5		MHz
	Resolution			12		Bit
	Number of available external inputs			3		
	Number of available internal inputs			5		

Electrical Characteristics: 12-Bit Sigma-Delta ADC *(continued)*

Over operating free-air temperature range, typical values are at T_A = 27°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Turnon time	Active or sleep with VANA ON and RC15MHZ_ON_IN_SLEEP = 1 or sleep with GPADC_FORCE = 1		0		µs
		Sleep or OFF		794		µs
		Sleep with VANA enabled		282		µs
	Gain error (without scaler)		–3.5%		3.5%	
	Gain error of the scaler		–1%		1%	
	Offset before trimming		–50		50	LSB
	Offset drift after trimming	Temperature and supply	–2		2	LSB
	Gain error drift (after trimming, including reference voltage)	Temperature and supply	–0.6%		0.2%	
INL	Integral nonlinearity	Best fitting	–3.5		3.5	LSB
DNL	Differential nonlinearity		–1		3.5	LSB
	Input capacitance	GPADC_IN0–GPADC_IN2		0.5		pF
	Source input impedance	Source resistance without capacitance			20	kΩ
		Source capacitance with > 20-kΩ source resistance	100			nF
	GPADC_VREF voltage reference		1.237	1.25	1.263	V
	Load current for GPADC_VREF				200	µA
	Input range (sigma-delta ADC)	Typical range	0		1.250	V
		Assured range without saturation	0.01		1.215	V
	Conversion time	1 channel, EXTEND_DELAY = 0		113		µs
		1 channel, EXTEND_DELAY = 1		563		µs
		2 channels		223		µs
	GPADC_IN0 current source	CURRENT_SRC_CH0[1:0] = 00 (default)		0		µA
		CURRENT_SRC_CH0[1:0] = 01	4.5	5.13	5.75	µA
		CURRENT_SRC_CH0[1:0] = 10	14.45	15.55	16.65	µA
		CURRENT_SRC_CH0[1:0] = 11	19.2	20.7	22.1	µA
	SMPS current monitoring (GPADC Channel 11)		See 公式 1 and 公式 2			
I_{FS0}	Channel 11 SMPS output current measurement gain factor			3.958		A
I_{OS0}	Channel 11 SMPS output current measurement current offset			0.652		A
TC_R0	Channel 11 SMPS output current measurement temperature coefficient			–1090		ppm/C
	SMPS output current measurement Accuracy, $I_{(ERROR)}$ (%), GPADC trimmed	SMPS3, SMPS6, SMPS7 $I_{L(error)}$ (%) = $I_{L(meas)}$ / I_L × 100 at 1 A, 25°C	–13%		13%	
		SMPS6, SMPS7 $I_{L(error)}$ (%) = $I_{L(meas)}$ / I_L × 100 at 2 A, 25°C	–9%		9%	
		SMPS3 $I_{L(error)}$ (%) = $I_{L(meas)}$ / I_L × 100 at 3 A, 25°C	–8%		8%	
		SMPS45 $I_{L(error)}$ (%) = $I_{L(meas)}$ / I_L × 100 at 4 A, 25°C	–7%		7%	
		SMPS12 $I_{L(error)}$ (%) = $I_{L(meas)}$ / I_L × 100 at 6 A, 25°C,	–7%		7%	
		SMPS123 $I_{L(error)}$ (%) = $I_{L(meas)}$ / I_L × 100 at 9 A, 25°C	–7%		7%	

4.13 Electrical Characteristics: Thermal Monitoring and Shutdown

Over operating free-air temperature range, typical values are at T_A = 27°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Hot-die temperature threshold	Rising threshold, THERM_HD_SEL[1:0] = 00	104	117	129	°C
		Falling threshold, THERM_HD_SEL[1:0] = 00	95	108	119	
		Rising threshold, THERM_HD_SEL[1:0] = 01	109	121	133	
		Falling threshold, THERM_HD_SEL[1:0] = 01	99	112	124	
		Rising threshold, THERM_HD_SEL[1:0] = 10	113	125	136	
		Falling threshold, THERM_HD_SEL[1:0] = 10	104	116	128	
		Rising threshold, THERM_HD_SEL[1:0] = 11	117	130	143	
		Falling threshold, THERM_HD_SEL[1:0] = 11	108	120	132	
	Thermal shutdown threshold	Rising threshold	133	148	163	°C
		Falling threshold	111	123	135	
$I_{Q(off)}$	Off ground current (two sensors on the die, specification for one sensor)	Device in OFF state, V_{VCC1} = 3.8 V, T = 25°C			0.1	µA
		Device in OFF state			0.5	
$I_{Q(on)}$	On ground current (two sensors on the die, specification for one sensor)	Device in ACTIVE state, V_{VCC1} = 3.8 V, T = 25°C		7	15	µA
		Device in ACTIVE state, GPADC measurement		25	40	

4.14 Electrical Characteristics: System Control Threshold

Over operating free-air temperature range, typical values are at T_A = 27°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POR (power-on reset) rising-edge threshold	Measured on VCC1 pin	2	2.15	2.50	V
POR falling-edge threshold	Measured on VCC1 pin	1.90	2	2.10	V
POR hysteresis	Rising edge to falling edge	40		300	mV
VSYS_LO, measured on VCC1 pin	Voltage range, 50-mV steps	2.75		3.10	V
	Voltage accuracy	–50		95	mV
VSYS_LO hysteresis	Falling edge to rising edge	75		460	mV
VSYS_HI, measured on VCC_SENSE pin	Voltage range, 50-mV steps	2.9		3.85	V
	Voltage accuracy	–55		105	mV
VSYS_MON, measured on VCC_SENSE pin	Voltage range, 50-mV steps	2.75		4.6	V
	Voltage accuracy	–70		140	mV
VBUS detection (VBUS wake-up comparator threshold)	Rising threshold	2.9		3.6	V
	Falling threshold	2.8		3.3	V

4.15 Electrical Characteristics: Current Consumption

Over operating free-air temperature range, typical values are at T_A = 27°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFF MODE						
Current consumption in OFF mode	VSYS (VCC1) = 3.8 V			20	45	µA
SLEEP MODE						
Current consumption in SLEEP mode	LDO2 and LDO9 enabled without load, 16-MHz oscillator completely disabled with system clock coming solely on internal 32-KHz RC oscillator	VSYS (VCC1) = 3.8 V		120	180	µA
		VSYS (VCC1) = 5.25 V		150	225	
	LDO2 and LDO9 enabled without load, 16-MHz oscillator enabled	VSYS (VCC1) = 3.8 V		2.64	2.81	mA
		VSYS (VCC1) = 5.25 V		3.3	3.5	

4.16 Electrical Characteristics: Digital Input Signal Parameters

Over operating free-air temperature range, typical values are at T_A = 27°C VIO refers to the VIO_IN pin, VSYS to the VCC1 pin (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWRON, RPWRON						
V_{IL}	Low-level input voltage related to VSYS (VCC1 pin reference)		–0.3	0	0.35 × V_{VSYS}	V
V_{IH}	High-level input voltage related to VSYS (VCC1 pin reference)		0.65 × V_{VSYS}	V_{VSYS}	V_{VSYS} + 0.3 ≤ 5.25	V
	Hysteresis		0.05 × V_{VSYS}			V
ENABLE1, GPIO_4, GPIO_6, I2C1_SCL_SCK, I2C1_SDA_SDI, I2C2_SCL_SCE, I2C2_SDA_SDO						
V_{IL}	Low-level input voltage related to VIO (VIO_IN pin reference)		–0.3	0	0.3 × V_{IO}	V
V_{IH}	High-level input voltage related to VIO (VIO_IN pin reference)		0.7 × V_{IO}	V_{IO}	V_{IO} + 0.3	V
	Hysteresis		0.05 × V_{IO}			V
BOOT0, PWRDOWN, RESET_IN, NSLEEP, NRESWARM, GPIO_0, GPIO_1, GPIO_2, GPIO_3, GPIO_5, GPIO_7 OR POWERHOLD						
V_{IL}	Low-level input voltage related to VRTC		–0.3	0	0.3 × V_{VRTC}	V
V_{IH}	High-level input voltage related to VRTC		0.7 × V_{VRTC}	V_{VRTC}	V_{VRTC} + 0.3	V
	Hysteresis		0.05 × V_{VRTC}			V
	Input voltage maximum for RESET_IN and GPIO_7				5.25	V
BOOT1						
V_{IL}	Low-level input voltage related to VRTC		–0.3	0	0.3 × V_{VRTC}	V
V_{IH}	High-level input voltage related to VRTC		0.95 × V_{VRTC}	V_{VRTC}	V_{VRTC} + 0.3	V

4.17 Electrical Characteristics: Digital Output Signal Parameters

Over operating free-air temperature range, typical values are at T_A = 27°C, VIO refers to the VIO_IN pin, VSYS to the VCC1 pin (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REGEN1, REGEN2						
V_{OL}	Low-level output voltage, push-pull and open-drain	I_{OL} = 2 mA	0		0.45	V
		I_{OL} = 100 µA	0		0.2	V
V_{OH}	High-level output voltage, push-pull	I_{OH} = 2 mA	V_{VSYS} – 0.45		V_{VSYS}	V
		I_{OH} = 100 µA	V_{VSYS} – 0.2		V_{VSYS}	V
	Supply for external pullup resistor, open-drain				V_{VSYS}	V
GPIO_1 or VBUSDET, GPIO_2						
V_{OL}	Low-level output voltage, push-pull and open-drain	I_{OL} = 10 mA	0		0.4	V
V_{OH}	High-level output voltage, push-pull	I_{OH} = 2 mA	V_{VSYS} – 0.45		V_{VSYS}	V
		I_{OH} = 100 µA	V_{VSYS} – 0.2		V_{VSYS}	V
	Supply for external pullup resistor, open-drain				V_{VSYS}	V

Electrical Characteristics: Digital Output Signal Parameters *(continued)*

Over operating free-air temperature range, typical values are at T_A = 27°C, VIO refers to the VIO_IN pin, VSYS to the VCC1 pin (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INT						
V_{OL}	Low-level output voltage, push-pull and open-drain	I_{OL} = 2 mA	0		0.45	V
		I_{OL} = 100 µA	0		0.2	V
V_{OH}	High-level output voltage, push-pull (VIO_IN pin reference)	I_{OH} = 2 mA	V_{IO} – 0.45		V_{IO}	V
		I_{OH} = 100 µA	V_{IO} – 0.2		V_{IO}	V
	Supply for external pullup resistor, open-drain				V_{IO}	V
GPIO_4 or SYSEN1, GPIO_6 or SYSEN2, RESET_OUT						
V_{OL}	Low-level output voltage, push-pull	I_{OL} = 2 mA	0		0.45	V
		I_{OL} = 100 µA	0		0.2	V
V_{OH}	High-level output voltage, push-pull (VIO_IN pin reference)	I_{OH} = 2 mA	V_{IO} – 0.45		V_{IO}	V
		I_{OH} = 100 µA	V_{IO} – 0.2		V_{IO}	V
POWERGOOD						
V_{OL}	Low-level output voltage, open-drain	I_{OL} = 2 mA	0		0.45	V
		I_{OL} = 100 µA	0		0.2	V
	Supply for external pullup resistor, open-drain				V_{VRTC}	V
GPIO5						
V_{OL}	Low-level output voltage, open-drain	I_{OL} = 2 mA	0		0.45	V
		I_{OL} = 100 µA	0		0.2	V
V_{OL}	Low-level output voltage, push-pull	I_{OL} = 2 mA	0		0.45	V
		I_{OL} = 100 µA	0		0.2	V
V_{OH}	High-level output voltage, push-pull	I_{OH} = 2 mA	V_{VRTC} – 0.45		V_{VRTC}	V
		I_{OH} = 100 µA	V_{VRTC} – 0.2		V_{VRTC}	V
	Supply for external pullup resistor, open-drain				V_{VRTC}	V
CLK32KGO1 V8, SYNCCLKOUT						
V_{OL}	Low-level output voltage, push-pull	I_{OL} = 1 mA	0		0.45	V
		I_{OL} = 100 µA	0		0.2	V
V_{OH}	High-level output voltage, push-pull	I_{OH} = 1 mA	V_{VRTC} – 0.45		V_{VRTC}	V
		I_{OH} = 100 µA	V_{VRTC} – 0.2		V_{VRTC}	V
CLK32KGO						
V_{OL}	Low-level output voltage, push-pull	I_{OL} = 1 mA	0		0.45	V
		I_{OL} = 100 µA	0		0.2	V
V_{OH}	High-level output voltage, push-pull (VIO_IN pin reference)	I_{OH} = 1 mA	V_{IO} – 0.45		V_{IO}	V
		I_{OH} = 100 µA	V_{IO} – 0.2		V_{IO}	V
GPIO_0, GPIO_3, GPIO_7						
V_{OL}	Low-level output voltage, open-drain	External pullup to VRTC, I_{OL} = 2 mA	0		0.45	V
		External pullup to VRTCI_{OL} = 100 µA	0		0.2	V
	Maximum supply for external pullup resistor, open-drain				5.25	V
I2C1_SDA_SDI, I2C2_SDA_SDO						

Electrical Characteristics: Digital Output Signal Parameters *(continued)*

Over operating free-air temperature range, typical values are at T_A = 27°C, VIO refers to the VIO_IN pin, VSYS to the VCC1 pin (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Low-level output voltage V_{OL} related to VIO (VIO_IN pin reference)	3-mA sink current	0	0.1 × V_{IO}	0.2 × V_{IO}	V
C_B	Capacitive load for I2C2_SDA_SDO in SPI mode				20	pF

4.18 Electrical Characteristics: I/O Pullup and Pulldown

Over operating free-air temperature range, VIO refers to the VIO_IN pin, VSYS to the VCC1 pin (unless otherwise noted)

PARAMETER	TEST CONDITIONS	PULLUP SUPPLY	MIN	TYP	MAX	UNIT
PWRON, RPWRON pullup resistance, fixed pullup		VSYS	55	120	370	kΩ
PWRDOWN pulldown resistance		—	180	400	900	kΩ
BOOT1 pullup resistance		VRTC			13.5	kΩ
BOOT1 pulldown resistance		—			14	kΩ
GPIO_0 pulldown resistance		—	180	400	900	kΩ
GPIO_1, GPIO_2 pullup resistance		VSYS	170	400	950	kΩ
GPIO_1, GPIO_2 pulldown resistance		—	170	400	950	kΩ
GPIO_3, RESET_IN pulldown resistance		—	180	400	900	kΩ
GPIO_4, GPIO_6 pullup resistance		VIO	170	400	950	kΩ
GPIO_4, GPIO_6 pulldown resistance		—	170	400	950	kΩ
GPIO_5 pullup resistance		VRTC	170	400	950	kΩ
GPIO_5 pulldown resistance		—	170	400	950	kΩ
GPIO_7 or POWERHOLD pulldown resistance		—	180	400	900	kΩ
NSLEEP, ENABLE1 pullup resistance		VRTC	170	400	950	kΩ
NSLEEP, ENABLE1 pulldown resistance		—	170	400	950	kΩ
NRESWARM pullup resistance		VRTC	78	120	225	kΩ

4.19 I²C Interface Timing Requirements

Over operating free-air temperature range(1)(2)(3)(4). For the timing diagram for fast and standard (F/S) modes, see Figure 4-1. For the timing diagram for high-speed (HS) mode, see Figure 4-2.

			MIN	MAX	UNIT
$f_{(SCL)}$	SCL clock frequency	Standard mode		100	kHz
		Fast mode		400	kHz
		High-speed mode (write operation), C_B – 100 pF max		3.4	MHz
		High-speed mode (read operation), C_B – 100 pF max		3.4	MHz
		High-speed mode (write operation), C_B – 400 pF max		1.7	MHz
		High-speed mode (read operation), C_B – 400 pF max		1.7	MHz
$t_{(BUF)}$	Bus free time between a STOP and START condition	Standard mode	4.7		µs
		Fast mode	1.3		µs

(1) Specified by design. Not tested in production.
(2) All values referred to V_{IHmin} and V_{IHmax} levels.
(3) For bus line loads C_B between 100 and 400 pF, the timing parameters must be linearly interpolated.
(4) A device must internally provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time.

I²C Interface Timing Requirements *(continued)*

Over operating free-air temperature range[(1)(2)(3)(4)]. For the timing diagram for fast and standard (F/S) modes, see Figure 4-1. For the timing diagram for high-speed (HS) mode, see Figure 4-2.

			MIN	MAX	UNIT
$t_{h(STA)}$	Hold time (REPEATED) START condition	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode	160		ns
$t_{(LOW)}$	Low period of the SCL clock	Standard mode	4.7		µs
		Fast mode	1.3		µs
		High-speed mode, C_B – 100 pF maximum	160		ns
		High-speed mode, C_B – 400 pF maximum	320		ns
$t_{(HIGH)}$	High period of the SCL clock	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode, C_B – 100 pF maximum	60		ns
		High-speed mode, C_B – 400 pF maximum	120		ns
$t_{su(STA)}$	Setup time for a REPEATED START condition	Standard mode	4.7		µs
		Fast mode	600		ns
		High-speed mode	160		ns
$t_{su(DAT)}$	Data setup time	Standard mode	250		ns
		Fast mode	100		ns
		High-speed mode	10		ns
$t_{h(DAT)}$	Data hold time	Standard mode	0	3.45	µs
		Fast mode	0	0.9	µs
		High-speed mode, C_B – 100 pF maximum	0	70	ns
		High-speed mode, C_B – 400 pF maximum	0	150	ns
$t_{r(CL)}$	Rise time of the SCL signal	Standard mode	20 + 0.1 C_B	1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		High-speed mode, C_B – 100 pF maximum	10	40	ns
		High-speed mode, C_B – 400 pF maximum	20	80	ns
$t_{r(CL1)}$	Rise time of the SCL signal after a REPEATED START condition and after an Acknowledge bit	Standard mode	20 + 0.1 C_B	1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		High-speed mode, C_B – 100 pF maximum	10	80	ns
		High-speed mode, C_B – 400 pF maximum	20	160	ns
$t_{f(CL)}$	Fall time of the SCL signal	Standard mode	20 + 0.1 C_B	300	ns
		Fast mode	20 + 0.1 C_B	300	ns
		High-speed mode, C_B – 100 pF maximum	10	40	ns
		High-speed mode, C_B – 400 pF maximum	20	80	ns
$t_{r(DA)}$	Rise time of the SDA signal	Standard mode	20 + 0.1 C_B	1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		High-speed mode, C_B – 100 pF maximum	10	80	ns
		High-speed mode, C_B – 400 pF maximum	20	160	ns

I²C Interface Timing Requirements *(continued)*

Over operating free-air temperature range(1)(2)(3)(4). For the timing diagram for fast and standard (F/S) modes, see Figure 4-1. For the timing diagram for high-speed (HS) mode, see Figure 4-2.

			MIN	MAX	UNIT
$t_{f(DA)}$	Fall time of the SDA signal	Standard mode	20 + 0.1 C_B	300	ns
		Fast mode	20 + 0.1 C_B	300	ns
		High-speed mode, C_B – 100 pF maximum	10	80	ns
		High-speed mode, C_B – 400 pF maximum	20	160	ns
$t_{su(STOP)}$	Setup time for a STOP condition	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode	160		ns

4.20 SPI Timing Requirements

For the SPI timing diagram, see Figure 4-3

		MIN	MAX	UNIT
$t_{su(ce)}$	Chip-select setup time	30		ns
$t_{h(ce)}$	Chip-select hold time	30		ns
$t_{c(clk)}$	Clock cycle time	67	100	ns
$t_{p(HIGH\_ck)}$	Clock high typical pulse duration	20		ns
$t_{p(LOW\_ck)}$	Clock low typical pulse duration	20		ns
$t_{su(si)}$	Input data set up time, before clock active edge	5		ns
$t_{h(si)}$	Input data hold time, after clock active edge	5		ns
t_{dr}	Data retention time		15	ns
$t_{(CE)}$	Time from CE going low to CE going high	67		ns

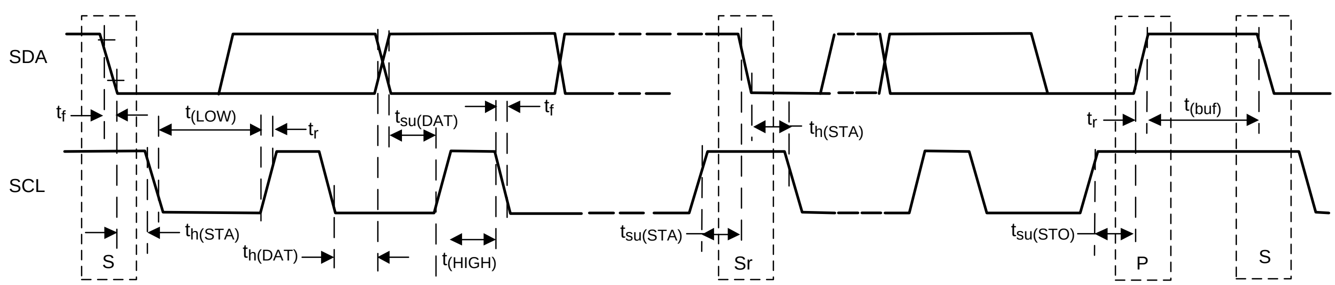
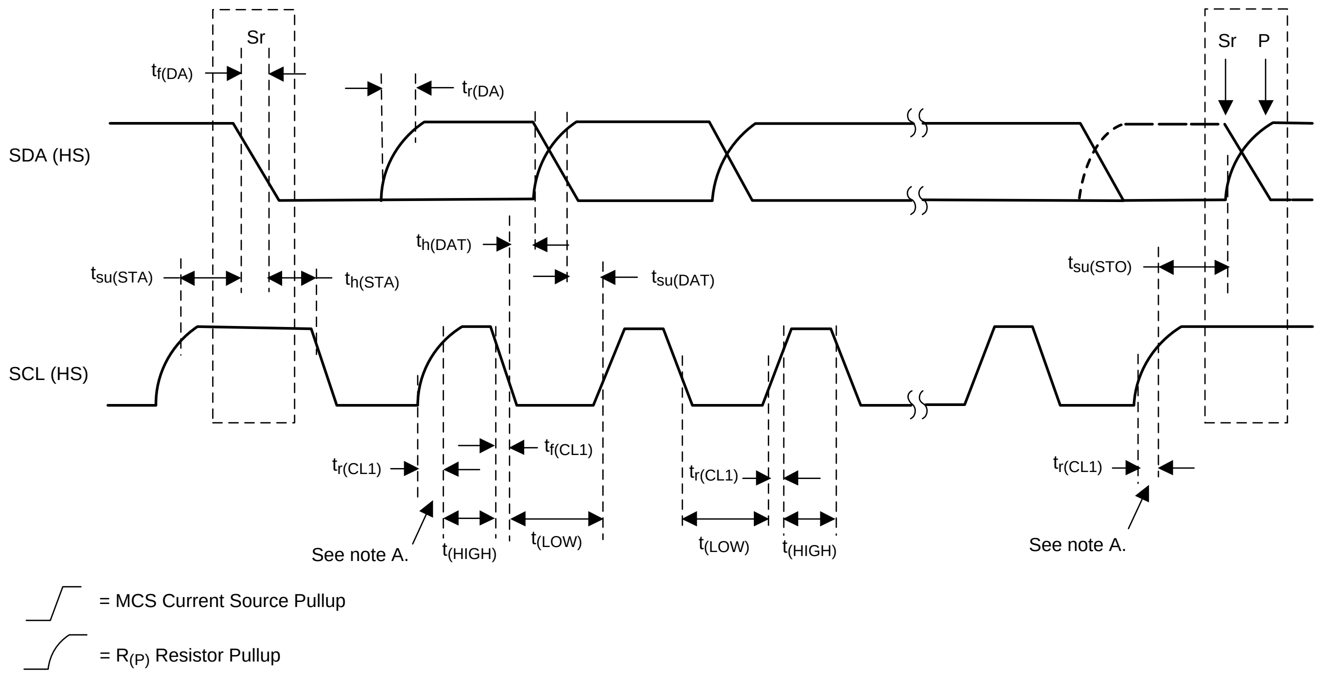


Figure 4-1. Serial Interface Timing Diagram for F/S Mode



A. The first rising edge of the SCL (HS) signal after the repeated START condition (Sr) and after each acknowledge bit.

Figure 4-2. Serial Interface Timing Diagram For HS Mode

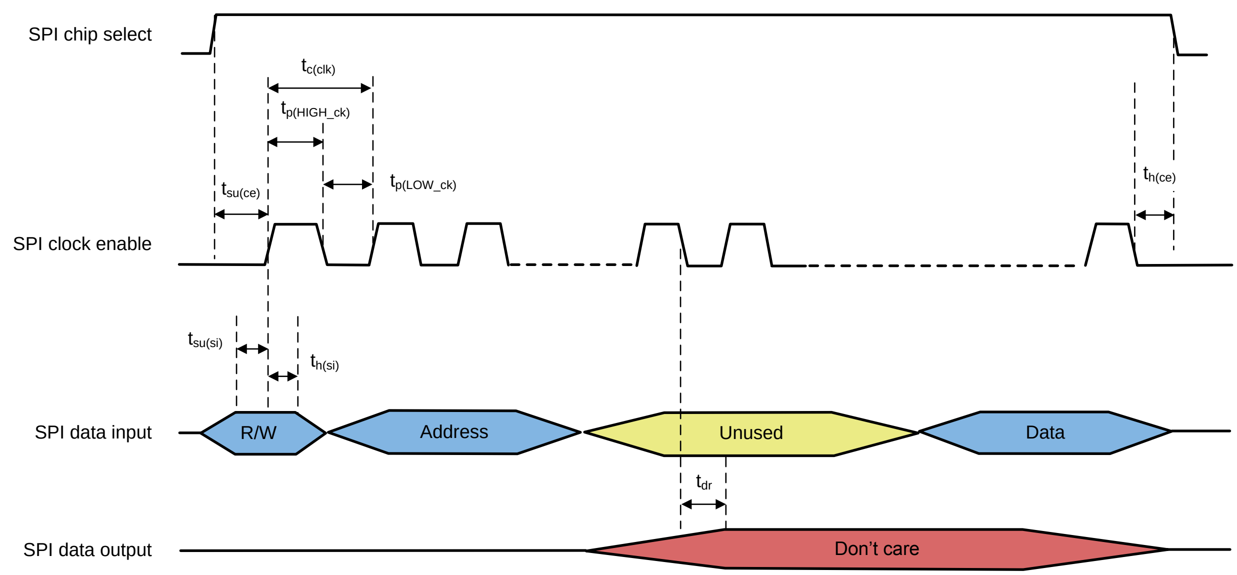
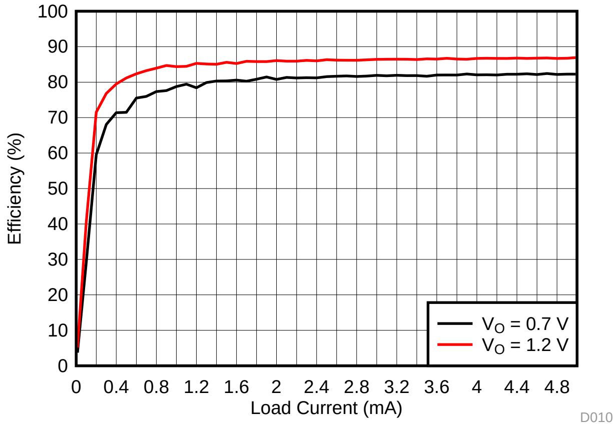


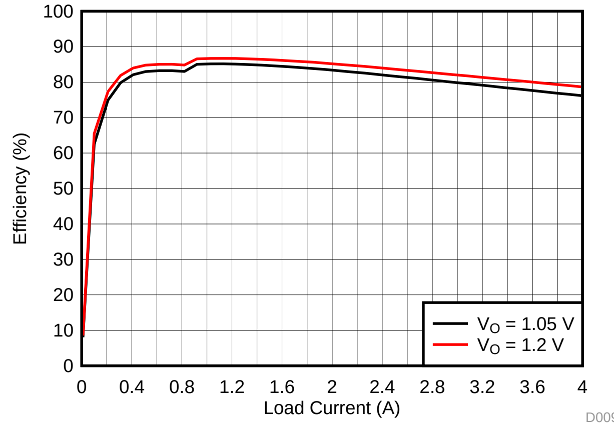
Figure 4-3. SPI Timing Diagram

4.21 Typical Characteristics



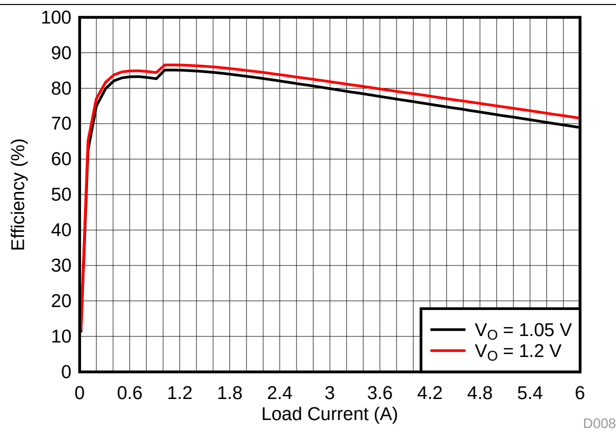
V_I = 3.8 V f_S = 2.2 MHz

图 4-4. SMPS Efficiency for Multi-Phase Eco-mode



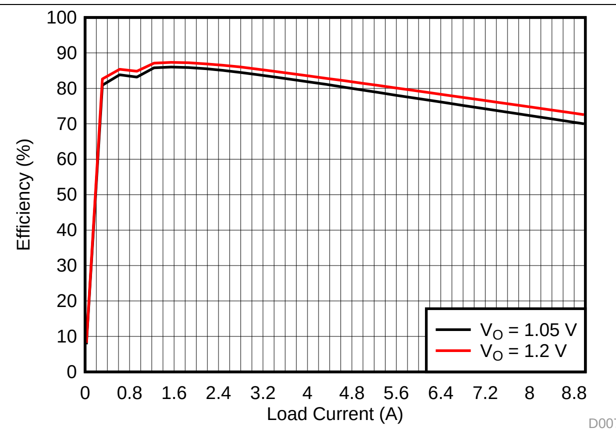
V_I = 3.8 V f_S = 2.2 MHz

图 4-5. SMPS Efficiency for 4-A Multi-Phase PWM Mode



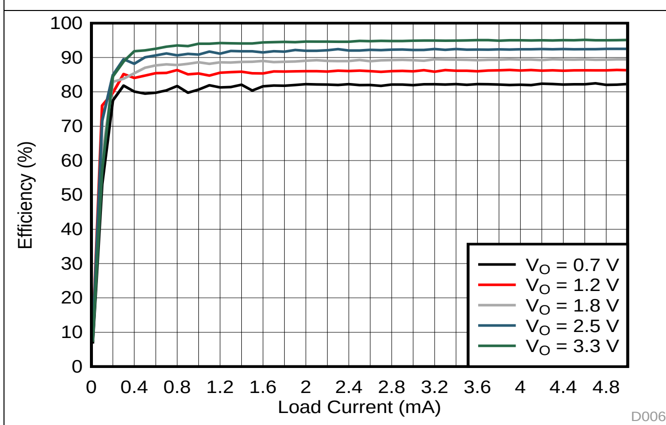
V_I = 3.8 V f_S = 2.2 MHz

图 4-6. SMPS Efficiency for 6-A Multi-Phase PWM Mode



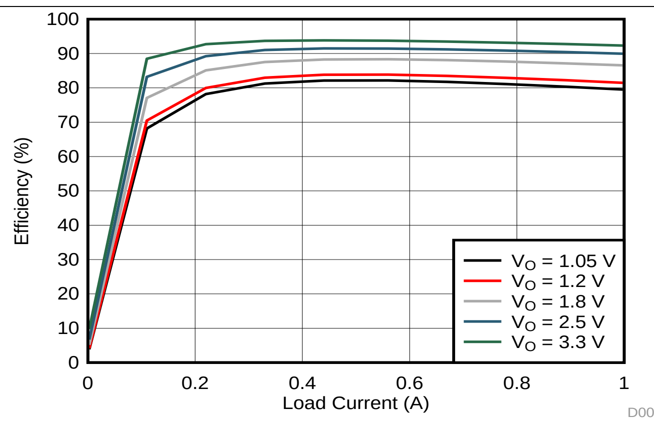
V_I = 3.8 V f_S = 2.2 MHz

图 4-7. SMPS Efficiency for 9-A Multi-Phase PWM Mode



V_I = 3.8 V f_S = 2.2 MHz

图 4-8. SMPS Efficiency for 1-A Single-Phase Eco-mode



V_I = 3.8 V f_S = 2.2 MHz

图 4-9. SMPS Efficiency for 1-A Single-Phase PWM Mode

Typical Characteristics *(continued)*

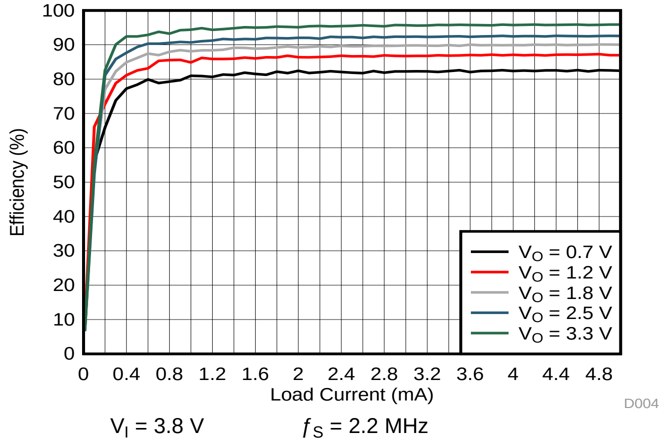


图 4-10. SMPS Efficiency for 2-A Single-Phase Eco-ode

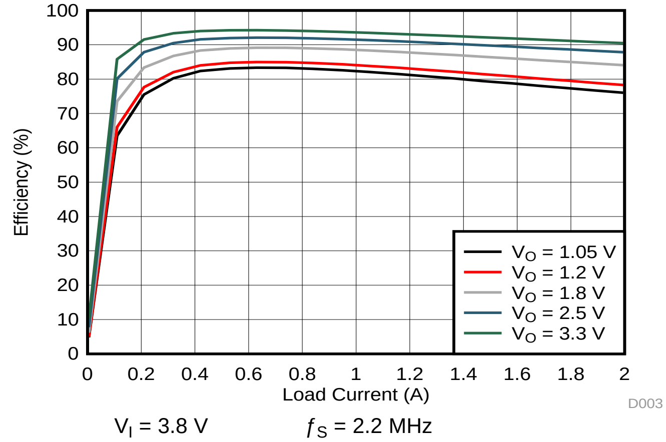


图 4-11. SMPS Efficiency for 2-A Single-Phase PWM Mode

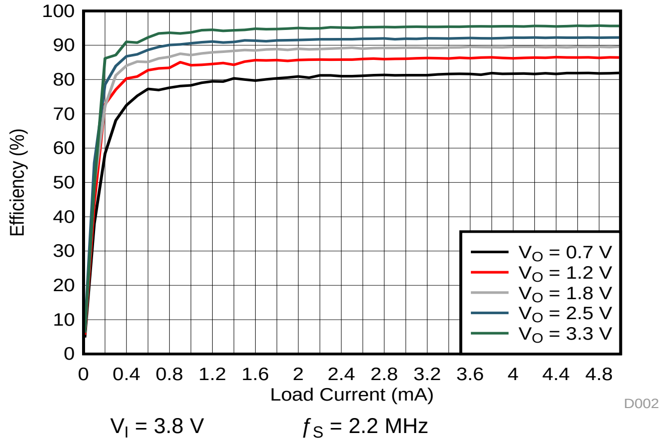


图 4-12. SMPS Efficiency for 3-A Single-Phase Eco-mode

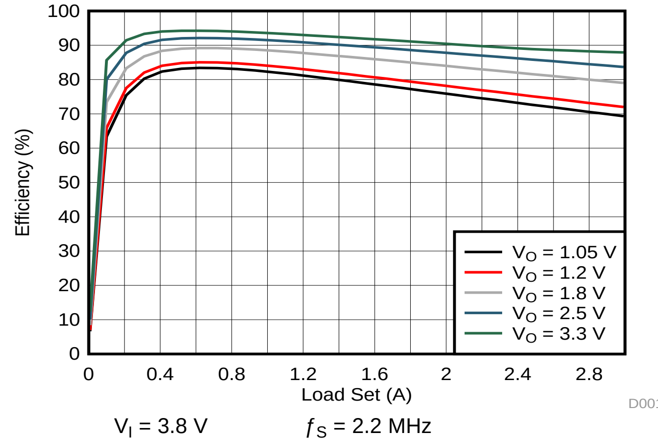


图 4-13. SMPS Efficiency for 3-A Single-Phase PWM Mode

5 Detailed Description

5.1 Overview

The TPS659037 device is a power-management integrated circuit (PMIC), available in a 169-pin, 0.8-mm pitch, 12-mm × 12-mm nFBGA package. The TPS659037 device provides seven configurable step-down converter rails, with the ability to combine power rails and supply up to 9 A of output current in multi-phase mode. The TPS659037 device has seven LDOs. The device also has a 12-bit GPADC with three external channels, eight configurable GPIOs, two I^{2}C interface channels or one SPI channel, real-time clock module with calendar function, PLL for external clock sync and phase delay capability, and programmable power sequencer and control for supporting different processors and applications.

The seven step-down converter rails are consisting of nine high frequency switch mode converters with integrated FETs. The step-down converter rails are capable of synchronizing to an external clock input and supports switching frequency between 1.7 MHz and 2.7 MHz. The SMPS12 and SMPS45 are dual-phase step-down converters that can combine with the SMPS3 or SMPS7 respectively and become triple-phase converters. In addition, the SMPS12, SMPS45, SMPS6, and SMPS8 support dynamic voltage scaling by a dedicated I^{2}C interface for optimum power savings.

All of the LDOs support a 0.9 to 3.3-V output with 50-mV step. The regulators are fully controllable by the I^{2}C interface and can be supplied from either a system supply or a preregulated supply.

All LDOs and step-down converters can be controlled by the SPI or I^{2}C interface, or by power request signals. In addition, voltage scaling registers allow transitioning the SMPS to different voltages by SPI, I^{2}C, or roof-and-floor control.

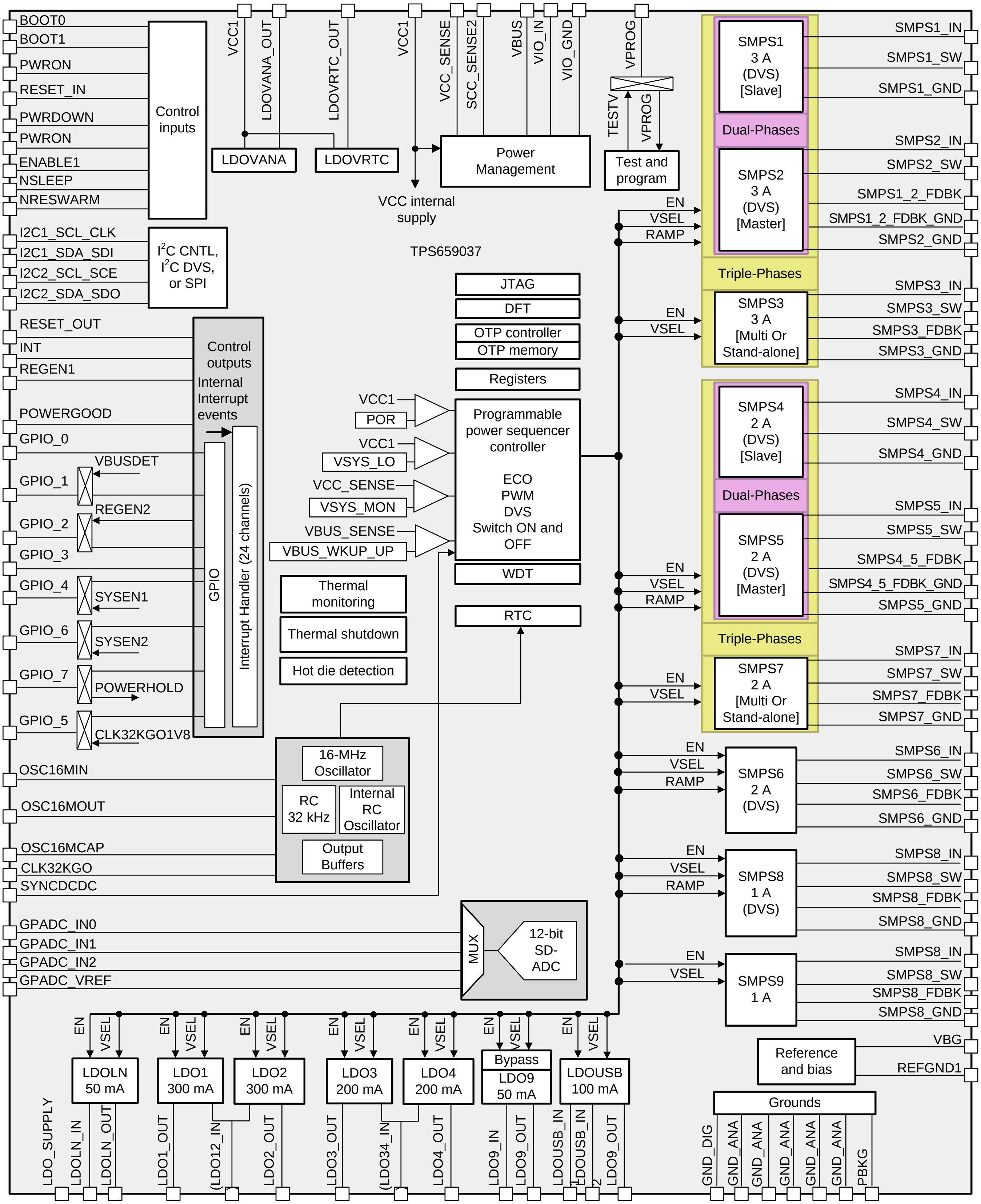
The power-up and power-down controller is configurable and programmable through OTP. The TPS659037 device includes a 32-kHz RC oscillator to sequence all resources during power up and power down. In cases where a fast start-up is required, a 16-MHz crystal oscillator is also included to quickly generate a stable 32-kHz for the system. The TPS659037 device also includes an RTC module which provides date, time, calendar, and alarm capability, which is best used when a 16-MHz crystal or an external and high accuracy 32-kHz clock is present.

The TPS659037 device also has eight configurable GPIOs with a multiplexed feature. Three of the GPIOs, together with the REGEN1 pin can be configured and used as enable signals for external resources, which can be included into the power-up and power-down sequence. The TPS659037 device also includes a general-purpose (GP) sigma-delta analog-to-digital converter (ADC) with three external input channels, which can be used as thermal or voltage and current monitors.

CAUTION

When operating the TPS659037 device using silicon revision 1.3 or earlier, without an external crystal, each SMPS regulating an output voltage greater than 1.8 V must be disabled before VCC is removed. Lowering VCC below the programmed VSYS_LO level while any SMPS is regulating an output voltage above 1.8 V may cause damage to the device. See 节 5.3.10 to identify the silicon version in the device.

5.2 Functional Block Diagram



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5.3 Feature Description

5.3.1 Power Management

The TPS659037 device integrates an embedded power controller (EPC) that fully manages the state of the device during power transitions. According to four defined types of requests (ON, OFF, WAKE, and SLEEP), the EPC executes one of the five predefined power sequences (OFF2ACT, ACT2OFF, SLP2OFF, ACT2SLP, and SLP2ACT) to control the state of the device resources. Any resource can be included in any power sequence. When a resource is not controlled or configured through a power sequence, the resource remains in the default state of the resource (from OTP).

Each resource is configured only through register bits. Therefore, a resource can be controlled statically by the user through the control interfaces (I^2C or SPI) or controlled automatically by the EPC during power transitions (predefined sequences of registers accesses).

The EPC is powered by an internal LDO that is automatically enabled when VSYS is available to the device. Ensuring that the VSYS pin (which is connected to VCC1, VCC_SENSE, SMPSx_In and LDOx_IN as suggested in 节 5.2) is the first supply available to the device is important to ensure proper operation of all the power resources provided by the TPS659037 device. Ensuring that the VSYS pin is stable prior to the VIO supply becoming available is important to ensure proper operation of the control interface and device IOs.

5.3.2 Power Resources (Step-Down and Step-Up SMPS Regulators, LDOs)

The power resources provided by the TPS659037 device includes inductor-based SMPSs and linear low-dropout voltage regulators (LDOs). These supply resources provide the required power to the external processor cores, external components, and to modules embedded in the device. 表 5-1 lists the power sources provided by the TPS659037 device.

表 5-1. Power Sources

RESOURCE	TYPE	VOLTAGE	CURRENT	COMMENTS
SMPS1, SMPS2, and SMPS3	SMPS	0.5 to 1.65 V, 10-mV steps 1 to 3.3 V, 20-mV steps	9 A	Can be used as one triple-phase regulator (9 A) or one dual-phase (6 A) and single-phase (3 A) regulators
SMPS4, SMPS5, and SMPS7	SMPS	0.5 to 1.65 V, 10-mV steps 1 to 3.3 V, 20-mV steps	6 A	Can be used as one triple-phase regulator (6 A) or one dual-phase (4 A) and single-phase (2 A) regulators
SMPS6	SMPS	0.5 to 1.65 V, 10-mV steps 1 to 3.3 V, 20-mV steps	2 A or 3 A	Can be configured as 2-A or 3-A SMPS through OTP programming
SMPS8	SMPS	0.5 to 1.65 V, 10-mV steps 1 to 3.3 V, 20-mV steps	1 A	
SMPS9	SMPS	0.5 to 1.65 V, 10-mV steps 1 to 3.3 V, 20-mV steps	1 A	
LDO1	LDO	0.9 to 3.3 V, 50-mV steps	300 mA	
LDO2	LDO	0.9 to 3.3 V, 50-mV steps	300 mA	
LDO3	LDO	0.9 to 3.3 V, 50-mV steps	200 mA	
LDO4	LDO	0.9 to 3.3 V, 50-mV steps	200 mA	
LDO9	LDO	0.9 to 3.3 V, 50-mV steps	50 mA	
LDOLN	LDO	0.9 to 3.3 V, 50-mV steps	50 mA	
LDOUSB	LDO	0.9 to 3.3 V, 50-mV steps	100 mA	

5.3.2.1 Step-Down Regulators

The synchronous step-down converter used in the power-management core has high efficiency while enabling operation with small and cost-competitive external components. The SMPSx_IN supply pins of all the converters must be individually connected to the VSYS supply (VCC1 pin). Four of these configurable step-down converters are multi-phased to create up to 4-A and 6-A rails, while another converter can be combined to these two rails to create two rails up to 9 A and 6 A of output current. All of the step-down converters can synchronize to an external clock source between 1.7 MHz and 2.7 MHz, or an internal fall back clock at 2.2 MHz.

The step-down converter supports two operating modes, which can be selected independently:

Forced PWM mode: In forced PWM mode, the TPS659037 device avoids pulse skipping and allows easy filtering of the switch noise by external filter components. The drawback is the higher IDDQ at low output current levels.

Eco-mode (lowest quiescent current mode): Each step-down converter can be individually controlled to enter a low quiescent current mode. In Eco-mode, the quiescent current is reduced and the output voltage is supervised by a comparator while most parts of the control are disabled to save power. The regulators should not be enabled under Eco-mode in order to ensure the stability of the output. Eco-mode should be enabled only when a converter has less than 5 mA of load current and V_O can remain constant. In addition, Eco-mode should be disabled before a load transient step to let the converter respond in a timely manner to the excess current draw. To ensure proper operation of the converter while it is in Eco-mode, the output voltage level must be less then 70% of the input supply voltage level. If the V_O of the converter is greater than 2.8 V, the TPS659037 device will monitor the supply voltage of the converter, and automatically shut down the converter if the input voltage falls below 4 V which prevents damage to the converter due to design limitation while the converter is in ECO mode.

In addition to the operating modes, the following parameters can be selected for the regulators:

Power good: The POWERGOOD signal high indicates that all SMPS outputs are within 10% (typical case) of the programmed value. The individual power good signal of a switching regulator is blanked when the regulator is disabled or when the regulator voltage transitions from one set point to another.

Output discharge: Each switching regulator is equipped with an output discharge enable bit. When this bit is set to 1, the output of the regulator is discharged to ground with the equivalent of a 9-Ω resistor when the regulator is disabled. If the regulator enable bit is set, the discharge bit of the regulator is ignored.

Output current monitoring: GPADC can monitor the SMPS output current. One SMPS at a time can be selected for measurement from the following: SMPS12, SMPS3, SMPS123, SMPS45, SMPS457, SMPS6 and SMPS7. Selection is controlled through the GPADC_SMPS_ILMONITOR_EN register.

Step-down converter ENABLE: The step-down converter enable and disable is part of the flexible power-up and power-down state-machine. Each converter can be programmed so that it is powered up automatically to a preselected voltage in one of the time slots after a power-on condition occurs. Alternatively, each SMPS can be controlled by a dedicated pin. Pins NSLEEP and ENABLE1 can be mapped to any resource (LDOs, SMPS converter, 32-kHz clock output or GPIO) to enable or disable it. Each SMPS can also be enabled and disabled through I^2C register access.

5.3.2.1.1 Sync Clock Functionality

The TPS659037 device contains a SYNCDCDC input to sync DC-DCs with the external clock.

In forced PWM mode, SMPSs are synchronized on an external input clock (SYNCDCDC) whereas in Eco-mode or if the SYNCDCDC pin is grounded, the switching frequency is based on an internal RC oscillator. The clock generated from the internal RC oscillator can be output through GPIO5 to provide synchronization clock to external SMPSs. For PWM mode, a PLL is present to buffer the external input clock to create nine clock signals for the nine SMPSs with different phases.

The sync clock dither specification parameters are based on a triangular dither pattern, but other patterns that comply with the minimum and maximum sync frequency range and the maximum dither slope can also be used.

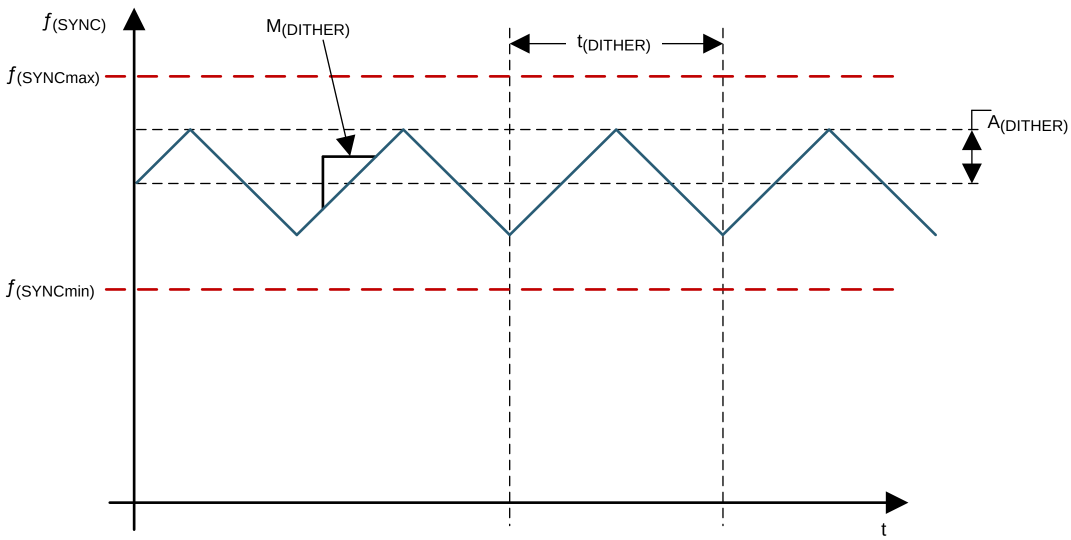


图 5-1. Sync Clock Range and Dither

The ollowing figure shows $f_{(SYNC)}$, the frequency of SYNCDCDC input clock and f_{SW}, the frequency of PLL output signal.

When there is no clock present on SYNCDCDC pin, the PLL generates a clock with a frequency equal to $f_{(FALLBACK)}$.

If a clock is present on SYNCDCDC pin with a frequency between $f_{(SAT\_LO)}$ and $f_{(SAT\_HI)}$, then the PLL is synchronised on SYNCDCDC clock and generates a clock with frequency equal to $f_{(SYNC)}$.

If $f_{(SYNC)}$ is higher than $f_{(SAT\_HI)}$, then the PLL generates a clock with a frequency equal to $f_{(SAT\_HI)}$.

If $f_{(SYNC)}$ is smaller than $f_{(SAT\_LO)}$, then the PLL generates a clock with a frequency equal to $f_{(SAT\_LO)}$.

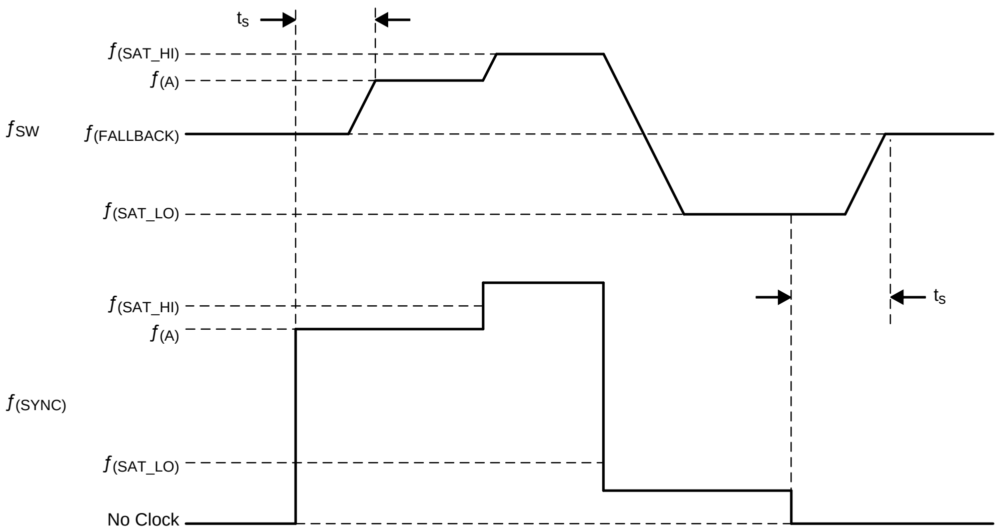


图 5-2. Sync Clock Saturation and Frequency Fallback

5.3.2.1.2 Output Voltage and Mode Selection

The default output voltage and enabling of the regulator during startup sequence is defined by OTP bits.

After start-up the software can change the output voltage with the RANGE and VSEL bits in the SMPSx_VOLTAGE register. The value 0x0 disables the SMPS (OFF).

The operating mode of an SMPSx when the TPS659037 device is in ACTIVE mode can be selected in SMPSx_CTRL register with MODE_ACTIVE[1:0].

The operating mode of an SMPSx when the TPS659037 device is in SLEEP mode is controlled by MODE_SLEEP[1:0] bit depending on SMPS assignment to NSLEEP and ENABLE1, see 表 5-13.

Soft-start slew rate is fixed ($t_{(ramp)}$).

The pulldown discharge resistance for OFF mode is enabled and disabled in the SMPS_PD_CTRL register. By default, discharge is enabled.

SMPS behavior for warm reset (reload default values or keep current values) is defined by the SMPSx_CTRL.WR_S bit.

5.3.2.1.3 Current Monitoring and Short Circuit Detection

The step-down converters include several other features.

The SMPS sink current limitation is controlled with the SMPS_NEGATIVE_CURRENT_LIMIT_EN register. The limitation is enabled by default.

Channel 11 of the GPADC can be used to monitor the output current of SMPS12, SMPS3, SMPS123, SMPS45, SMPS457, SMPS6, or SMPS7. Load current monitoring is enabled for a given SMPS in the SMPS_ILMONITOR_EN register. SMPS output power monitoring is intended to be used during the steady state of the output voltage, and is supported in PWM mode only.

Use 公式 1 as the basic equation for the SMPS output current result.

$$I_L = \frac{I_{FS} \times \text{GPADC code}}{\left(2^{12} - 1\right)} - I_{OS}$$

where

- $I_{FS} = I_{FS0} \times K$ (K is the number of active SMPS phases)
- $I_{OS} = I_{OS0} \times K$ (K is the number of active SMPS phases) (1)

Use 公式 2 to calculate the temperature compensated result.

$$I_L = \frac{I_{FS} \times \text{GPADC code}}{\left(\left[2^{12} - 1\right] \times \left[1 + TC\_R0 \times (\text{Temperature} - 25)\right]\right)} - I_{OS} \quad (2)$$

For values of I_{FS0} and I_{OS0}, see Section 4.12.

The SMPS thermal monitoring is enabled (default) and disabled with the SMPS_THERMAL_EN register. When enabled, the SMPS thermal status is available in the SMPS_THERMAL_STATUS register. SMPS12 and SMPS3 have shared thermal protection, in effect, if SMPS12 triggers the thermal protection, then SMPS3 operating in stand-alone mode is disabled. There is no dedicated thermal protection in SMPS8 or SMPS9.

Each SMPS has a detection for load current above I_{LIM}, indicating overcurrent or shorted SMPS output. A register SMPS_SHORT_STATUS indicates any SMPS short condition. Depending on the interrupt short line mask bit register (INT2_MASK.SHORT), an interrupt is generated upon any shorted SMPS. If a short situation occurs on any enabled SMPSs, the corresponding short status bit is set in the SMPS_SHORT_STATUS register. A switch-off signal is then sent to the corresponding SMPS, and remains off until the corresponding bit in the SMPS_SHORT_STATUS register is cleared. This register is cleared on a read, or by issuing a POR. The SMPS_SHORT_STATUS register is cleared when read, or by issuing a POR. The same behavior applies to LDO shorts using the SDO_SHORT_STATUS registers. This same behavior applies to LDO shorts using the LDO_SHORT_STATUS registers.

A short must occur on any enabled SMPS or LDO for at least 155 us to 185 us for the short detection to shut off the rail. During startup of the device, there is a 2 ms counter that masks any short-circuit shutdown. This counter starts when the device is enabled and the counter is reset when any SMPSx or LDOx rail becomes ACTIVE. When no rail has been enabled for 2 ms, the counter reaches its threshold and the short-circuit shutdown is no longer masked for the enabled SMPSs and LDOs.

5.3.2.1.4 POWERGOOD

The external POWERGOOD pin indicates if the outputs of the SMPS are correct or not (图 5-3). Either voltage and current monitoring or a current monitoring only can be selected for POWERGOOD indication. This selection is common for all SMPSs in the SMPS_POWERGOOD_MASK2.POWERGOOD_TYPE_SELECT bit register. When both voltage and current are monitored, POWERGOOD signal active (polarity is programmable) indicates that all SMPS outputs are within certain percentage, V_{SMPSPG} , of the programmed value and that load current is below I_{LIM}.

All POWERGOOD sources can be masked in the SMPS_POWERGOOD_MASK1 and SMPS_POWERGOOD_MASK2 registers. By default, only the SMPS12 rail (or SMPS123 rail if in triple phase) is monitored. When an SMPS is disabled, it should be masked to prevent it forcing POWERGOOD inactive. When SMPS voltage is transitioning from one target voltage to another due to DVS command, voltage monitoring is internally masked and POWERGOOD is not impacted.

Including POWERGOOD in the GPADC result is possible for SMPS output current monitoring by setting SMPS_COMPMODE = 1. Only one SMPS can be monitored by the GPADC channel at the time.

The POWERGOOD function can also be used for monitoring an external SMPS is at the correct output level and the load is lower than the current limit; indication is through the GPIO_7 pin.

All POWERGOOD sources can be masked in SMPS_POWERGOOD_MASK1 and SMPS_POWERGOOD_MASK2 registers.

CAUTION

The current monitor on multi-phase rails (such as SMPS12, SMPS123, or SMPS45) may cause POWERGOOD to change to a low level (with default polarity) when transitioning from multi-phase operation to single phase operation. TI recommends masking the multi-phase rails as a POWERGOOD source, using SMPS_POWERGOOD_MASK1, or debouncing the POWERGOOD signal if this POWERGOOD toggle is not desired in the application design.

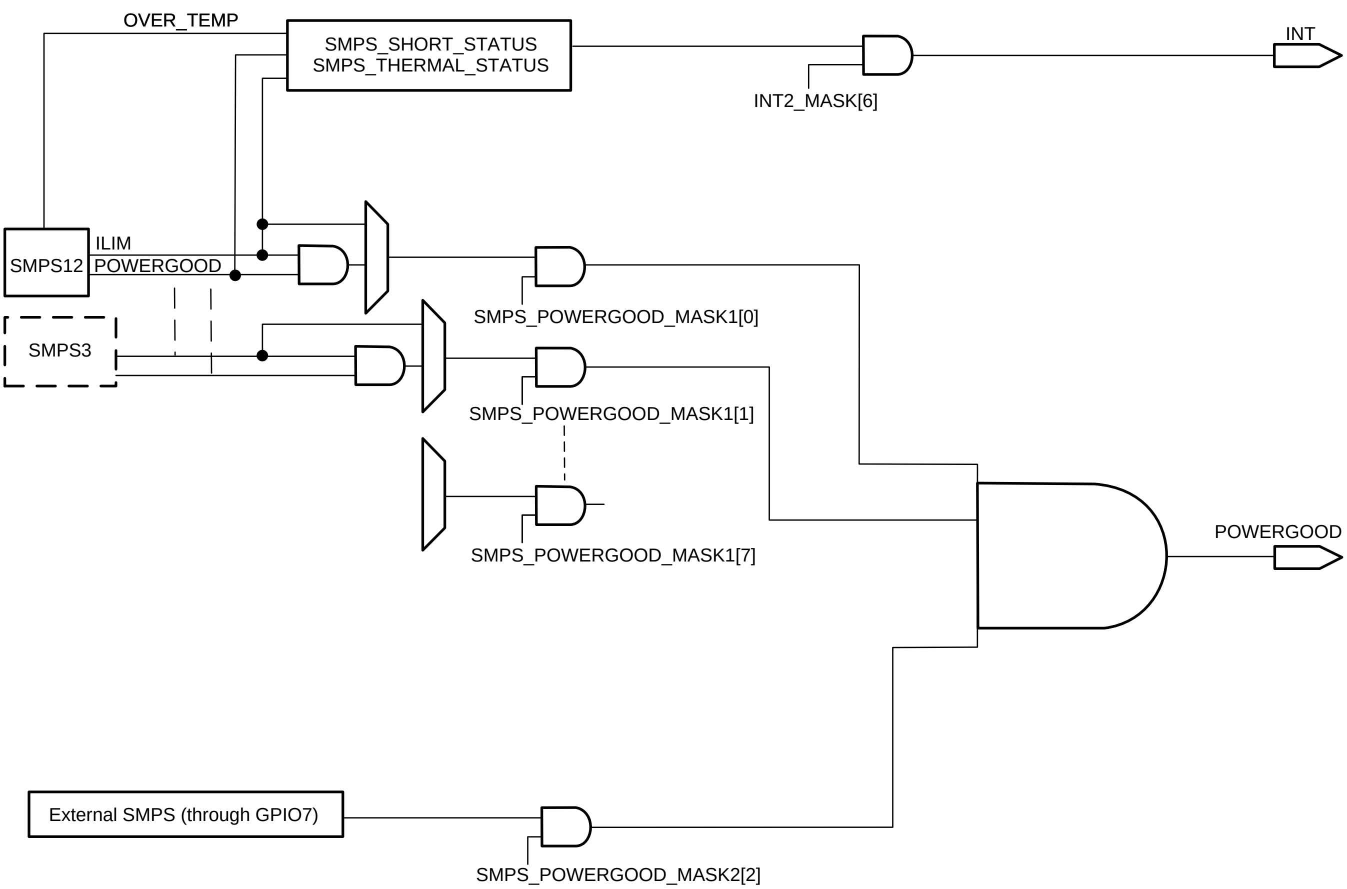


图 5-3. POWERGOOD Block Diagram

5.3.2.1.5 DVS-Capable Regulators

The step-down converters SMPS12 or SMPS123, SMPS45 or SMPS457, SMPS6, and SMPS8 are DVS-capable and have some additional parameters for control. The slew rate of the output voltage during a change in the voltage level is fixed at 2.5 mV/µs. The control for the two different voltage levels (ROOF and FLOOR) with the NSLEEP and ENABLE1 signals is available. The control bits for the output voltage slew rate control the following additional control bits. When the ROOF_FLOOR control is not used, two different voltage levels can be selected with the CMD bit in the SMPSx_FORCE register.

- The output voltage slew rate for achieving new output voltage value is fixed at 2.5 mV/µs.

- The NSLEEP and ENABLE1 pins can be used for roof-floor control of SMPS. For roof-floor operation sets the SMPSx_CTRL.ROOF_FLOOR_EN register, and assign SMPS to NSLEEP and ENABLE1 in the NSLEEP_SMPS_ASSIGN and ENABLE1_SMPS_ASSIGN registers. When the controlling pin is active, the SMPS output value is defined by the SMPSx_VOLTAGE register. When the controlling pin is not active, the SMPS output value is defined by the SMPSx_FORCE register.
- Set the second value for the output voltage with the SMPSx_FORCE.VSEL register. A value of 0x0 disables the SMPS (OFF).
- Select which register, SMPSx_VOLTAGE or SMPSx_FORCE, to use with the SMPSx_FORCE.CMD bit. The default is the voltage setting of SMPSx_VOLTAGE. For the CMD bit to work, ensure that SMPSx_CTRL.ROOF_FLOOR_EN = 0.

图 5-5 and 图 5-4 show the SMPS controls for DVS.

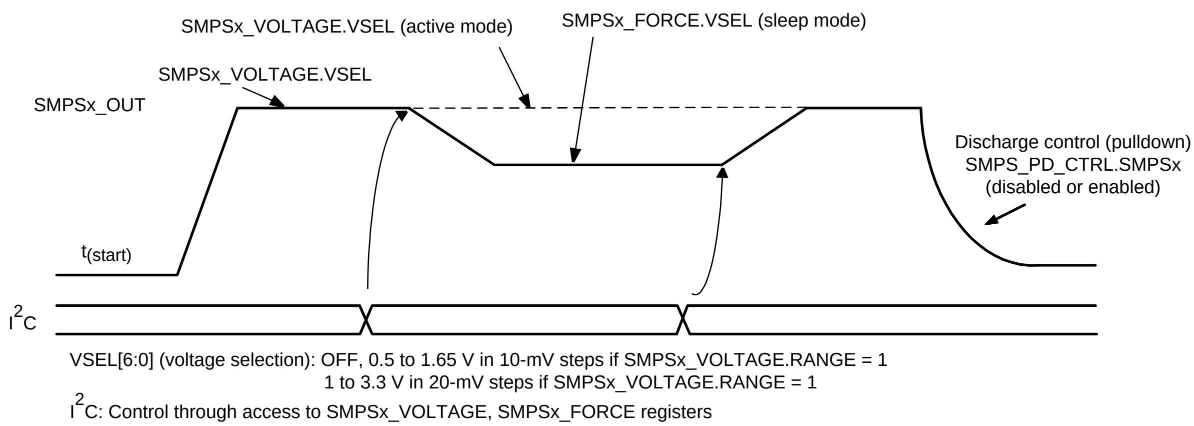
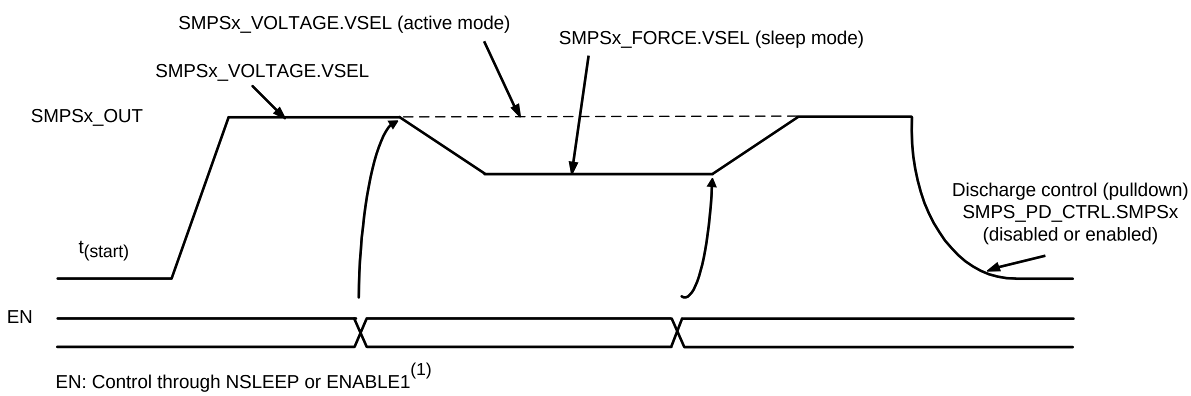


图 5-4. DVS - SMPS Controls
Voltage Control Through I²C (SMPSx_CTRL.ROOF_FLOOR_EN = 0)



(1) See 表 5-13.

图 5-5. DVS - SMPS Controls
Voltage Control Through External Pin (SMPSx_CTRL.ROOF_FLOOR_EN = 1)

5.3.2.1.6 Non DVS-Capable Regulators

SMPS3 and SMPS7, when they are not part of the multi-phase configuration, will work as single phase step down converters. Together with SMPS9, these are non-DVS-Capable regulators. The output voltage slew rate is not controlled internally, and the converter will achieve the new output voltage in JUMP mode. When changes to the output voltage are necessary while SMPS3, SMPS7, or SMPS9 are configured as single phase converters, programming the changes to the output voltages at a rate which is slower than 2.5 mV/μs is recommended to avoid voltage overshoot or undershoot.

5.3.2.1.7 Step-Down Converters SMPS12 and SMPS123

The step-down converters SMPS1, SMPS2, and SMPS3 can be used in two different configurations:

- SMPS12 in dual-phase configuration supporting 6-A load current and SMPS3 in single-phase configuration supporting 3-A load current
- SMPS123 in triple-phase configuration supporting 9-A load current

SMPS1 and SMPS2 cannot be used as separate converters. In dual-phase configuration the two interleaved synchronous buck regulator phases with built-in current sharing operate in opposite phase. In triple-phase configuration the three interleaved synchronous buck regulator phases with built-in current sharing operate 120° out of phase. For light loads, the converter automatically changes to 1-phase operation.

图 5-6 shows the connections for dual-phase and triple-phase configurations.

a. Dual-Phase SMPS and Stand-Alone SMPS **b. Triple Phase SMPS**

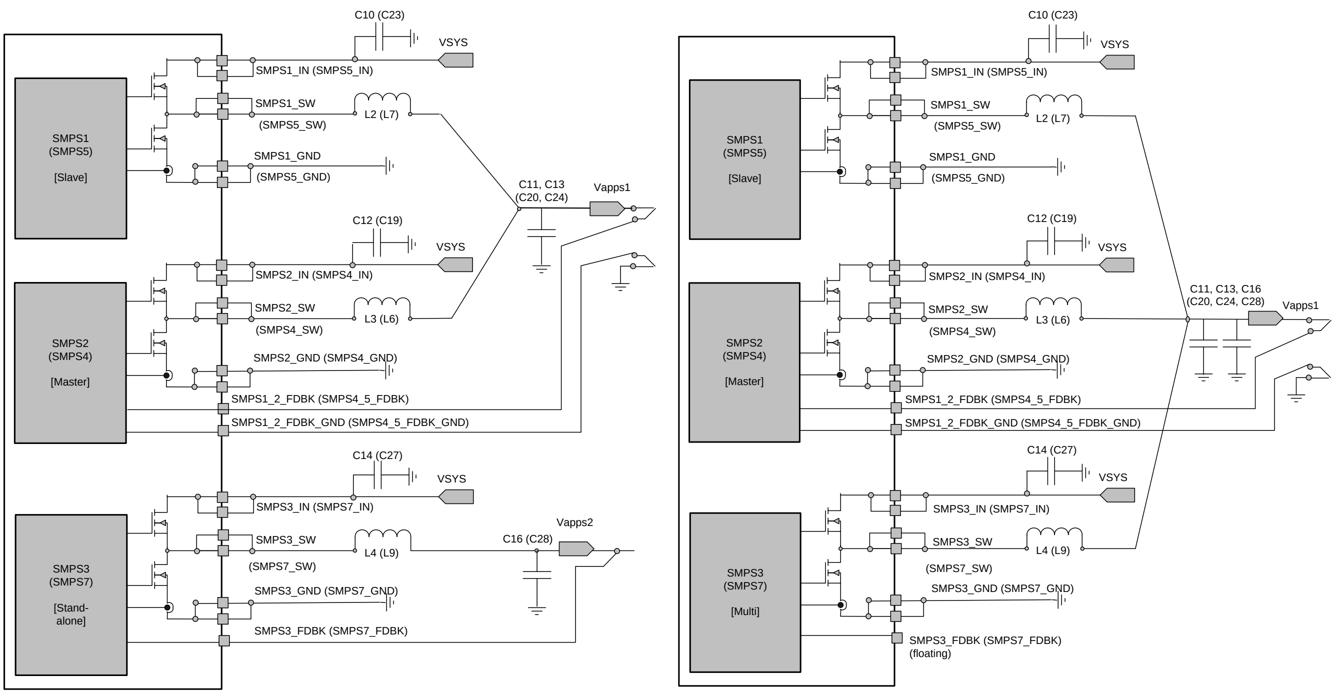


图 5-6. Multi-Phase SMPS Connectivity

To use the SMPS123 or SMPS12 and SMPS3 in the system:

- OTP defines dual-phase (SMPS12) operation, single-phase (SMPS3) operation, or triple-phase (SMPS123) operation. If SMPS123 mode is selected, the SMPS12 registers control SMPS123.
- By default SMPS123 and SMPS12 operate in multiphase mode for higher load currents and switch automatically to single-phase mode for low load currents. Forcing multiphase operation or single-phase operation by setting the SMPS_CTRL.SMPS123_PHASE_CTRL[1:0] bits when the SMPS123 or SMPS12 are loaded is also possible. Under no-load condition, do not force the multiphase operation, as this causes the SMPS to exhibit instability.

5.3.2.1.8 Step-Down Converter SMPS45 and SMPS457

The step-down converters SMPS4, SMPS5 and SMPS7 can be used in two different configurations:

- SMPS45 in dual-phase configuration supporting 4-A load current and SMPS7 in single-phase configuration supporting 2-A load current
- SMPS457 in triple-phase configuration supporting 6-A load current

SMPS4 and SMPS5 cannot be used as separate converters. In dual-phase configuration the two interleaved synchronous buck regulator phases with built-in current sharing operate in opposite phase. In triple-phase configuration the three interleaved synchronous buck regulator phases with built-in current sharing operate 120 degrees out of phase. For light loads, the converter automatically changes to 1-phase operation.

To use SMPS457 or SMPS45 and SMPS7 in the system:

- OTP defines dual-phase (SMPS45) operation, single-phase (SMPS7) operation, or triple-phase (SMPS457) operation. If SMPS457 mode is selected, the SMPS45 registers control SMPS457.
- By default SMPS457 and SMPS45 operate in multiphase mode for higher load currents and switch automatically to single-phase mode for low load currents. Forcing multiphase operation or single-phase operation by setting the SMPS_CTRL.SMPS457_PHASE_CTRL[1:0] bits when the SMPS457 or SMPS45 are loaded is also possible. Under no-load condition, do not force the multiphase operation, as this causes the SMPS to exhibit instability.

5.3.2.1.9 Step-Down Converters SMPS3, SMPS6, SMPS7, SMPS8, and SMPS9

The SMPS3 is a buck converter supporting up to a 3-A load current, SMPS6 and SMPS7 are buck converters supporting up to a 2-A load current. The SMPS6 can support up to 3A if programmed in OTP for boosted current mode. Using extended current mode increases SMPS6 current limits so to protect external coil from damage, coil should be selected according to the higher current rating.

SMPS8 and SMPS9 are buck converters supporting up to a 1-A load current. SMPS6 and SMPS8 are DVS-capable.

5.3.2.2 LDOs – Low Dropout Regulators

All LDOs are integrated so that they can be connected to a system supply, to an external buck boost SMPS, or to another preregulated voltage source. The output voltages of all LDOs can be selected, regardless of the LDO input voltage level V_I. There is no hardware protection to prevent software from selecting an improper output voltage if the V_I minimum level is lower than T_{DCOV} (total DC output voltage) + DV (dropout voltage). In such conditions, the output voltage would be lower and nearly equal to the input supply. The regulator output voltage cannot be modified on the fly from one (0.9–2.1 V) voltage range to the other (2.2–3.3 V) voltage range and vice versa. The regulator must be restarted in these cases. If an LDO is not needed, the external components can be unplaced. The TPS659037 device is not damaged by such configuration, and the other functions do not depend on the unused LDOs and work properly.

5.3.2.2.1 LDOVANA

The VANA voltage regulator is dedicated to supply the analog functions of the TPS659037 device, such as the GPADC and other analog circuits. VANA is automatically enabled and disabled when it is needed. The automatic control optimizes the overall SLEEP state current consumption.

5.3.2.2.2 LDOVRTC

The VRTC regulator supplies always-on functions, such as real-time clock (RTC) and wake-up functions. This power resource is active as soon as a valid energy source is present.

This resource has two modes:

- Normal mode is able to supply all digital parts of the TPS659037 device
- Backup mode is able to supply only always-on parts

VRTC supplies the digital part of the TPS659037 device. In the BACKUP state, the VRTC regulator is in low-power mode and the digital activity is reduced to the RTC parts only and maintained in retention registers of the backup domain. The rest of the digital is under reset and the clocks are gated. In the OFF state, the turn-on events and detection mechanism are also added to the previous RTC current load. In BACKUP and OFF states, the external load on VRTC should not exceed 0.5 mA. In the ACTIVE state, VRTC switches automatically into ACTIVE mode. The reset is released and the clocks are available. In SLEEP state, VRTC is kept active. The reset is released and only the 32-kHz clock is available. To reduce power consumption, low-power mode can be selected by software.

注

For silicon revision 1.3 or earlier, if V_{CC} is discharged rapidly and then resupplied, a POR may not be reliably generated. In this case a pulldown resistor can be added on the LDOVRTC output. See 节 5.4.11 for details. See 节 5.3.10 to identify the silicon version in the device.

5.3.2.2.3 LDO Bypass (LDO9)

LDO9 has a bypass capability to connect the input voltage to the output. It allows switching between 1.8 V and the preregulated supply.

5.3.2.2.4 LDOUSB

This LDOUSB has two inputs, LDOUSB_IN1 and LDOUSB_IN2. The input selection occurs by the LDOUSB_ON_VBUS_VSYS bit in the LDO_CTRL register.

5.3.2.2.5 Other LDOs

All the other LDOs have the same output voltage capability, from 0.9 to 3.3 V in 50-mV steps. All the LDO inputs can be independently connected into system voltage or into preregulated supply. The preregulated supply can be higher or lower than the system supply.

5.3.3 Long-Press Key Detection

The TPS659037 device can detect a long press on the PWRON pin. Upon detection, the device generates a LONG_PRESS_KEY interrupt and then switches the system off. The key-press duration is configured through the LONG_PRESS_KEY.LPK_TIME bits.

The interrupt clear has two behaviors based on the configuration of the LONG_PRESS_KEY .LPK_INT_CLR bit:

- LONG_PRESS_KEY.LPK_INT_CLR = 0: If PWRON remains low and the interrupt is cleared, the switch-off sequence is cancelled. If PWRON remains low and the interrupt is not cleared, the switch-off sequence is executed.
- LONG_PRESS_KEY.LPK_INT_CLR = 1: Switch off cannot be cancelled as long as PWRON remains low (default).

5.3.4 RTC

5.3.4.1 General Description

The RTC is driven by the 32-kHz oscillator and it provides the alarm and time-keeping functions.

The main functions of the RTC block are:

- Time information (seconds, minutes, hours) in binary-coded decimal (BCD) code
- Calendar information (day, month, year, day of the week) in BCD code up to year 2099

- Programmable interrupts generation; the RTC can generate two interrupts:
  - Timer interrupts periodically (1-second, 1-minute, 1-hour, or 1-day periods), which can be masked during the SLEEP state to prevent the host processor from waking up
  - Alarm interrupt at a precise time of the day (alarm function)
- Oscillator frequency calibration and time correction with 1/32768 resolution

图 5-7 shows the RTC block diagram.

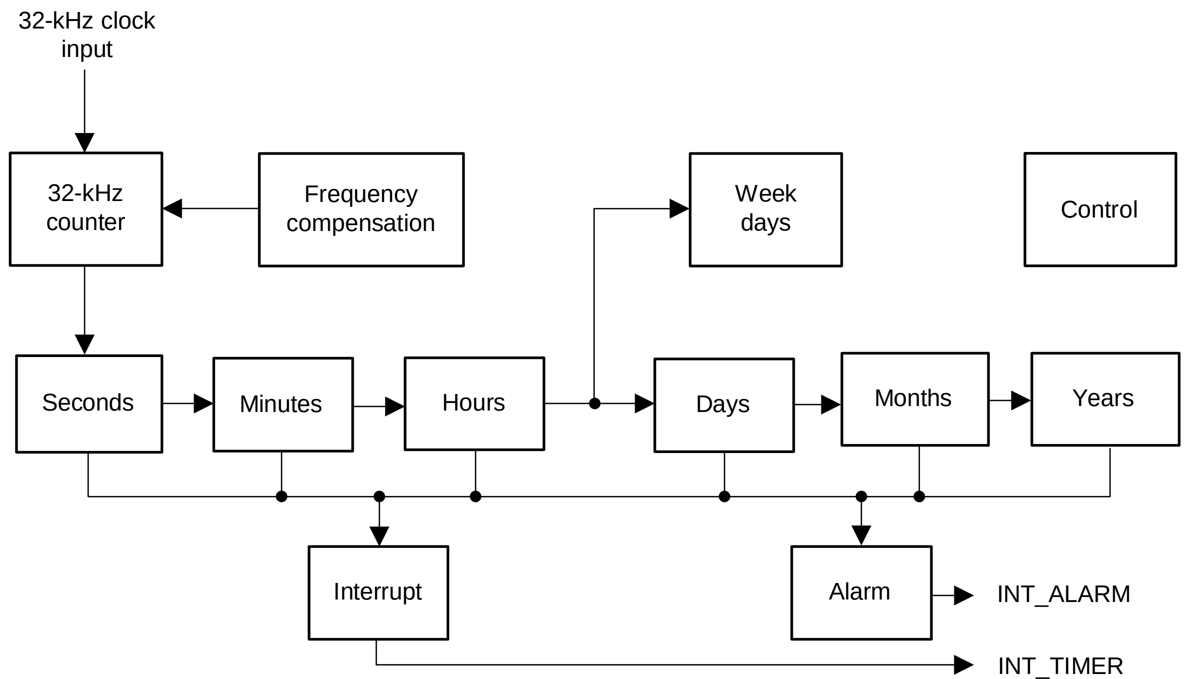


图 5-7. RTC Block Diagram

5.3.4.2 Time Calendar Registers

All the time and calendar information is available in the time calendar (TC) dedicated registers: SECONDS_REG, MINUTES_REG, HOURS_REG, DAYS_REG, WEEKS_REG, MONTHS_REG, and YEARS_REG. The TC register values are written in BCD code.

- Year data ranges from 00 to 99.
  - Leap Year = Year divisible by four (2000, 2004, 2008, 2012, and so on)
  - Common Year = Other years
- Month data ranges from 01 to 12.
- Day value ranges:
  - 1 to 31 when months are 1, 3, 5, 7, 8, 10, 12
  - 1 to 30 when months are 4, 6, 9, 11
  - 1 to 29 when month is 2 and year is a leap year
  - 1 to 28 when month is 2 and year is a common year
- Week value ranges from 0 to 6.
- Hour value ranges from 0 to 23 in 24-hour mode and ranges from 1 to 12 in AM or PM mode.
- Minutes value ranges from 0 to 59.
- Seconds value ranges from 0 to 59.

Example: Time is 10H54M36S PM (PM_AM mode set), 2008 September 5; previous registers values are listed in 表 5-2:

表 5-2. RTC Time Calendar Registers Example

REGISTER	CONTENT
SECONDS_REG	0x36
MINTURES_REG	0x54
HOURS_REG	0x10
DAYS_REG	0x05
MONTHS_REG	0x09
YEARS_REG	0x08

The user can round to the closest minute, by setting the ROUND_30S register bit in the RTC_CTRL_REG register. TC values are set to the closest minute value at the next second. The ROUND_30S bit is automatically cleared when the rounding time is performed.

Example:

- If current time is 10H59M45S, round operation changes time to 11H00M00S
- If current time is 10H59M29S, round operation changes time to 10H59M00S

5.3.4.2.1 TC Registers Read Access

TC registers read accesses can be done in two ways:

- A direct read to the TC registers. In this case, there can be a discrepancy between the final time read and the real time because the RTC keeps running because some of the registers can toggle in between register accesses. Software must manage the register change during the reading.
- Read access to shadowed TC registers. These registers are at the same addresses as the normal TC registers. They are selected by setting the GET_TIME bit in the RTC_CTRL_REG register. When this bit is set, the content of all TC registers is transferred into shadow registers so they represent a coherent timestamp, avoiding any possible discrepancy between them. When processing the read accesses to the TC registers, the value of the shadowed TC registers is returned so it is completely transparent in terms of register access.

5.3.4.2.2 TC Registers Write Access

TC registers write accesses can be done in two ways:

- Direct write into the TC registers. In this case, because the RTC keeps running, there can be a discrepancy between the final time written and the target time to be written because some of the registers can toggle in between register accesses. Software must manage the register change during the writing.
- Write access while RTC is stopped. Software can stop the RTC by the clearing STOP_RTC bit of the control register and checking the RUN bit of the status to be sure that RTC is frozen. It then updates the TC values and restarts the RTC by setting the STOP_RTC bit, which ensures that the final written values are aligned with the targeted values.

5.3.4.3 RTC Alarm

RTC alarm registers (ALARM_SECONDS_REG, ALARM_MINUTES_REG, ALARM_HOURS_REG, ALARM_DAYS_REG, ALARM_MONTHS_REG, and ALARM_YEARS_REG) are used to set the alarm time or date to the corresponding generated IT_ALARM interrupts. This interrupt is enabled through the IT_ALARM bit in the RTC_INTERRUPTS_REG register. These register values are written in BCD code, with the same data range as described for the TC registers (see 节 5.3.4.2).

5.3.4.4 RTC Interrupts

The RTC supports two types of interrupts:

- IT_ALARM interrupt. This interrupt is generated when the configured date or time in the corresponding ALARM registers is reached. This interrupt is enable by the IT_ALARM bit in the RTC_INTERRUPT_REG register.

- IT_TIMER interrupt. This interrupt is generated when the periodic time set in the EVERY bits of the RTC_INTERRUPT_REG register is reached. This interrupt is enabled by the IT_TIMER bit in the RTC_INTERRUPT_REG register. During the SLEEP state, the IT_TIMER interrupt can either be masked (stored and generated as soon as the TPS659037 device exists the SLEEP state) or unmasked using the IT_SLEEP_MASK_EN bit of the RTC_INTERRUPT_REG register.

5.3.4.5 RTC 32-kHz Oscillator Drift Compensation

The RTC_COMP_MSB_REG and RTC_COMP_LSB_REG registers are used to compensate for any inaccuracy of the 32-kHz clock output from the 16.384-MHz crystal oscillator. To compensate for any inaccuracy, software must perform an external calibration of the oscillator frequency, calculate the drift compensation needed versus one time hour period, and load the compensation registers with the drift compensation value.

The compensation mechanism is enabled by the AUTO_COMP_EN bit in the RTC_CTRL_REG register. The process happens after the first second of each hour. The time between second 1 to second 2 (T_ADJ) is adjusted based on the settings of the two RTC_COMP_MSB_REG and RTC_COMP_LSB_REG registers. These two registers form a 16-bit, 2s complement value COMP_REG (from –32767 to 32767) that is subtracted from the 32-kHz counter as shown in 公式 3 to adjust the length of T_ADJ:

$$\left(\frac{32768 - COMP\_REG}{32768}\right) \tag{3}$$

Therefore, adjusting the compensation with a 1/32768-second time unit accuracy per hour and up to 1 s per hour is possible.

Software must ensure that these registers are updated before each compensation process (there is no hardware protection). For example, software can load the compensation value into these registers after each hour event, during second 0 to second 1, just before the compensation period, happening from second 1 to second 2.

Preloading the internal 32-kHz counter with the content of the RTC_COMP_MSB_REG and RTC_COMP_LSB_REG registers possible when setting the SET_32_COUNTER bit in the RTC_CTRL_REG register. This setting must occur when the RTC is stopped.

图 5-8 shows the RTC compensation scheduling.

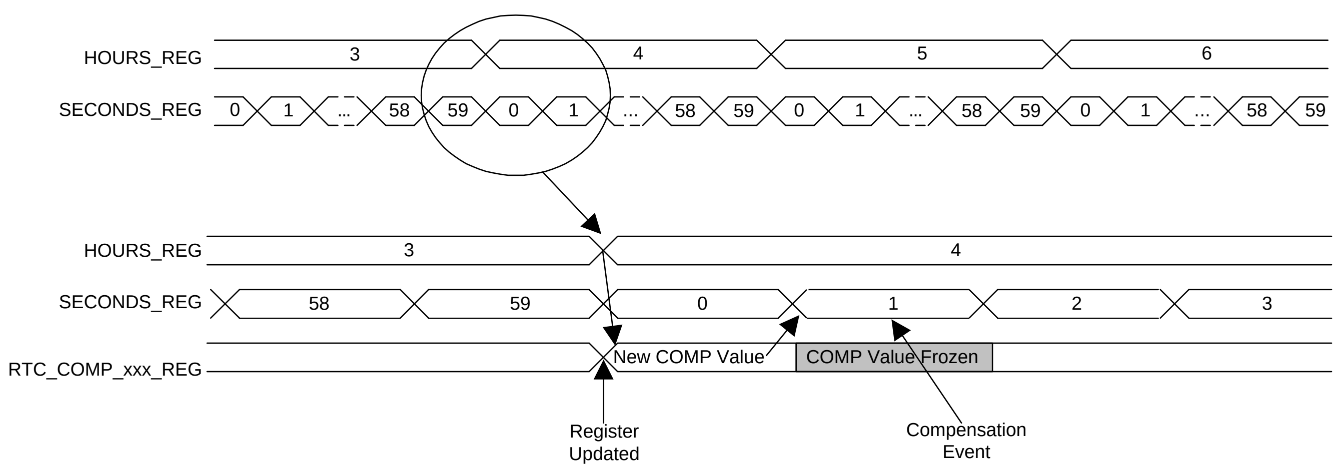


图 5-8. RTC Compensation Scheduling

5.3.5 GPADC – 12-Bit Sigma-Delta ADC

The GPADC consists of a 12-bit sigma-delta ADC combined with an analog input multiplexer. The GPADC allows the host processor to monitor a variety of analog signals using analog-to-digital conversion on the input source. After the conversion completes, an interrupt is generated for the host processor and it can read the result of the conversion through the I^2C interface.

The GPADC on this PMIC supports 16 analog inputs. However only a total of 9 inputs are available for the application use. Three of these inputs are available on external pins, and the remaining six are dedicated to internal resource monitoring. One of the three external inputs is associated with a current source allowing measurements of resistive elements (thermal sensor). To improve the measurement accuracy, the reference voltages GPADC_VREF can be used with an external resistor for the NTC resistor measurement. The reference voltage GPADC_VREF is always present when the GPADC is enabled.

GPADC_IN0 is associated with three selectable current sources. The selectable current levels are 5, 15, and 20 μA.

GPADC_IN1 is intended to measure temperature with an NTC sensor connected to ground. Two resistors, one in parallel with the NTC resistor and the other one between GPADC_IN1 and GPADC_VREF, can be used to modify the exponential function of the NTC resistor.

图 5-9 shows the block diagram of the GPADC.

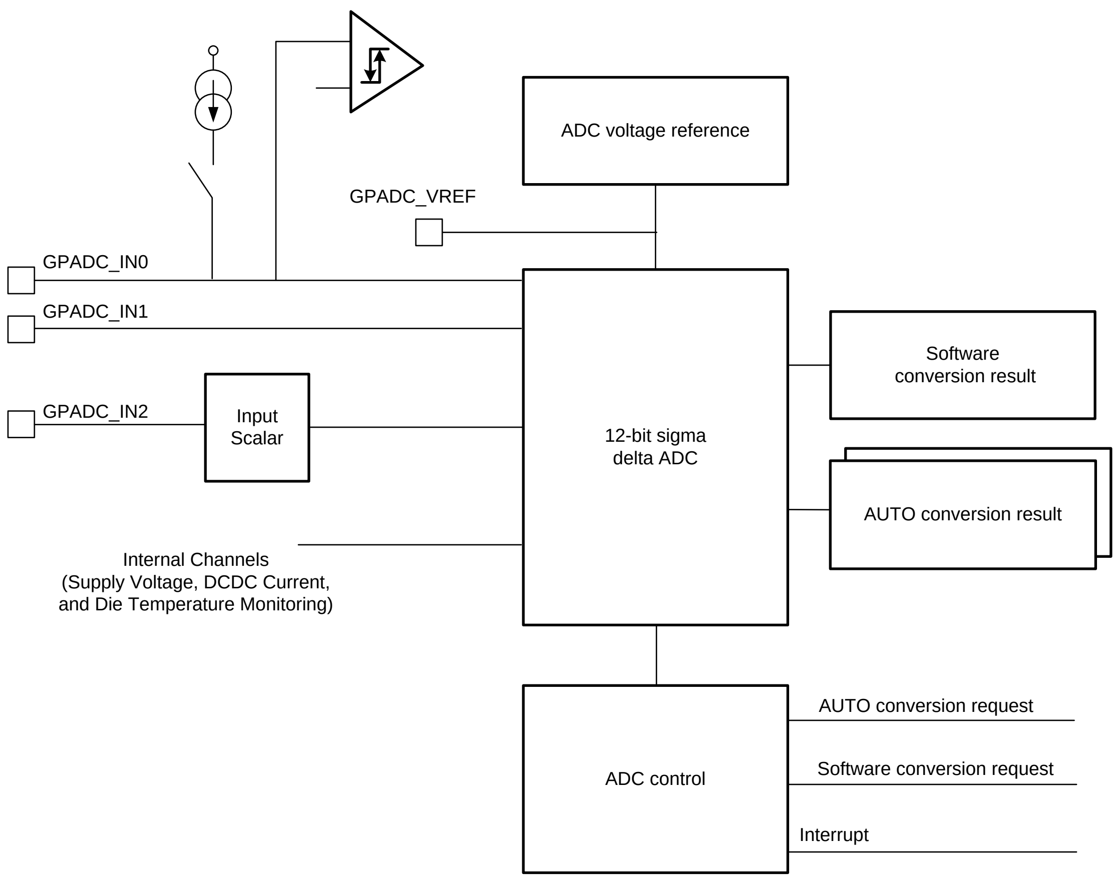


图 5-9. Block Diagram of the GPADC

For all the measurements performed by the monitoring GPADC, voltage dividers, current to voltage converters, and current source are integrated in the TPS659037 device to scale the signal to be measured to the GPADC input range.

The conversion requests are initiated by the host processor either by software through the I^{2}C. This mode is useful when real-time conversion is required.

Two kinds of conversion requests are available with the following priority:

1. Asynchronous conversion request (SW)
2. Periodic conversion (AUTO)

The EXTEND_DELAY bit in the GPADC_RT_CTRL register can extend by 400 µs the delay from the channel selection or triggering to the sampling.

Use 公式 4 to convert from the GPADC code to the internal die temperature using GPADC channels 12 and 13.

$$\text{Die Temperature } (^\circ\text{C}) = \frac{\left(\left[\frac{\text{GPADC Code}}{2^{12}}\right] \times 1.25\right) - 0.753\ \text{V}}{2.64\ \text{mV}} \tag{4}$$

表 5-3. GPADC Channel Assignments

CHANNEL	TYPE	INPUT VOLTAGE FULL RANGE(1)	INPUT VOLTAGE PERFORMANCE RANGE(2)	SCALER	OPERATION
0 (GPADC_IN0)	External(3)	0 to 1.25 V	0.01 to 1.215 V	No	Resistor value or general purpose. Select source current 0, 5, 15, or 20 µA
1 (GPADC_IN1)	External(3)	0 to 1.25 V	0.01 to 1.215 V	No	Platform temperature, NTC resistor value and general purpose
2 (GPADC_IN2)	External(3)	0 to 2.5 V	0.02 to 2.43 V	2	Audio accessory or general purpose
7 (VCC_SENSE)	Internal	2.5 to 5 V when HIGH_VCC_SENSE = 0 2.3 V to (VCC1–1 V) when HIGH_VCC_SENSE = 1	2.5 to 4.86 V when HIGH_VCC_SENSE = 0 2.3 V to (VCC1–1 V) when HIGH_VCC_SENSE = 1	4	System supply voltage (VCC_SENSE)
10 (VBUS)	Internal	0 to 6.875V	0.055 to 5.25 V	5.5	VBUS Voltage
11	Internal	0 to 1.25 V		No	DC-DC current probe
12	Internal	0 to 1.25 V	0 to 1.215 V	No	PMIC internal die temperature
13	Internal	0 to 1.25 V	0 to 1.215 V	No	PMIC internal die temperature
15	Internal	0 to VCC1 V	0.055 to VCC1 V	5	Test network

(1) The minimum and maximum voltage full range corresponds to typical minimum and maximum output codes (0 and 4095).
(2) The performance voltage is a range where gain error drift, offset drift, INL and DNL parameters are specified.
(3) If VANA LDO is OFF, maximum current to draw from GPADC_INx is 1 mA for reliability. For current higher than 1 mA, VANA must be set to SLEEP or ACTIVE mode.

5.3.5.1 Asynchronous Conversion Request (SW)

Software can also request conversion asynchronously. This conversion is not critical in terms of start-of-conversion positioning. Software must select the channel to be converted, and then requests the conversion with the GPADC_SW_SELECT register. An INT interrupt is generated when the conversion result is ready, and the result is stored in the GPADC_SW_CONV0_LSB and GPADC_SW_CONV0_MSB registers.

CAUTION

A defect in the digital controller of TPS659037 device may cause an unreliable result from the first asynchronous conversion request after the device exit from a warm reset. TI recommends that user rely on subsequent requests to obtain accurate result from the asynchronous conversion after a device warm reset.

In addition, a cold reset event which happens during a GPADC conversion will cause the GPADC controller to lock up. A software workaround for these issues are described in detail in the *Guide to Using the GPADC in TPS65903x and TPS6591x Devices*.

5.3.5.2 Periodic Conversion Request (AUTO)

Software can enable periodic conversions to compare one or two channels with a predefined threshold level. Software must select one or two channels with the GPADC_AUTO_SELECT register and thresholds and polarity with the GPADC_THRES_CONV0_LSB, GPADC_THRES_CONV0_MSB, GPADC_THRES_CONV1_LSB, and GPADC_THRES_CONV1_MSB registers. In addition, software must select the conversion interval with the GPADC_AUTO_CTRL register and enable the periodic conversion with the AUTO_CONV0_EN and AUTO_CONV1_EN bits. There is no need to enable the GPADC separately. The control logic enables and disables the GPADC automatically to save power. When AUTO mode is the only conversion enabled, do not use the AUTO_CONV0_EN and AUTO_CONV1_EN bits to disabled the conversion. Instead, force the state machine of the GPADC on by setting the GPADC_CTRL1. GPADC_FORCE bit = 1, then shutdown the GPADC AUTO conversion using GPADC_AUTO_CTRL.SHUTDOWN_CONV[01] = 0. Wait 100 µs before disabling the GPADC state machine by setting GPADC_CTRL1. GPADC_FORCE bit = 0. The latest conversion result is always stored in the GPADC_AUTO_CONV0_LSB, GPADC_AUTO_CONV0_MSB, GPADC_AUTO_CONV1_LSB, and GPADC_AUTO_CONV1_MSB registers. All selected channels are queued and converted from channel 0 to 7. The first (lower) converted channel results is placed in the GPADC_AUTO_CONV0 register and the second one is placed in the GPADC_AUTO_CONV1 register. Therefore, TI recommends putting the lower channel to convert in AUTO_CONV0_SEL and the higher channel to convert in AUTO_CONV1_SEL.

If the conversion result triggers the threshold level, an INT interrupt is generated and the conversion result is stored. If the interrupt is not cleared or the results are not read before another auto-conversion is completed, then the registers store only the latest results, discarding the previous ones. The auto conversion is never stopped by an uncleared interrupt or unread registers.

Programming the triggering of the threshold level can also generate shutdown. This is available for CONV0 and CONV1 channels independently and is enabled with the SHUTDOWN bits in the GPADC_AUTO_CTRL register. During SLEEP and OFF modes, only channels from 0 to 10 can be converted. For channels 12 and 13, conversion is possible in sleep if thermal sensor is not disabled.

5.3.5.3 Calibration

The GPADC channels are calibrated in the production line using a two-point calibration method. The channels are measured with two known values (X1 and X2) and the difference (D1 and D2) to the ideal values (Y1 and Y2) are stored in OTP memory. The principle of the calibration is shown in 图 5-10.

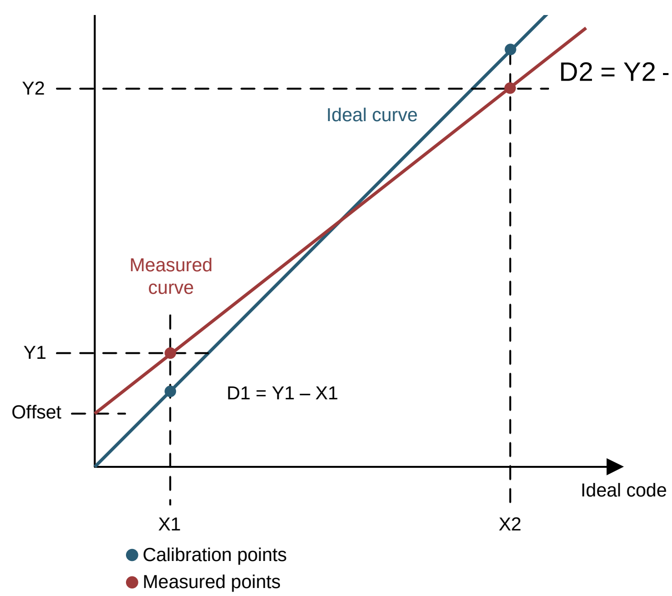


图 5-10. ADC Calibration Scheme

Some of the GPADC channels can use the same calibration data and the corrected result can be calculated using the equations:

Gain: $$k = 1 + \left(\frac{(D2 - D1)}{(X2 - X1)}\right) \quad (5)$$

Offset: $$b = D1 - (k - 1) \times X1 \quad (6)$$

If the measured code is a, the corrected code a' is:

$$a' = \frac{(a - b)}{k} \quad (7)$$

表 5-4 lists the parameters X1 and X2, and the register of D1 and D2 required in the calculation for all the channels.

表 5-4. GPADC Calibration Parameters

CHANNEL	X1	X2	D1	D2	COMMENTS
0,1	2064 (0.63 V)	3112 (0.95 V)	GPADC_TRIM1	GPADC_TRIM2	Channel 1 trimming is used
2	2064 (1.26 V)	3112 (1.9 V)	GPADC_TRIM3	GPADC_TRIM4	
7	2064 (2.52 V)	3112 (3.8 V)	GPADC_TRIM7	GPADC_TRIM8	

5.3.6 General-Purpose I/Os (GPIO Pins)

The TPS659037 device integrates eight configurable general-purpose I/Os that are multiplexed with alternative features as described in 表 5-5.

表 5-5. General Purpose I/Os Multiplexed Functions

PIN	PRIMARY FUNCTION	SECONDARY FUNCTION
GPIO_1	General-purpose I/O	Output: VBUSDET (VBUS detection)
GPIO_2	General-purpose I/O	Output: REGEN2
GPIO_4	General-purpose I/O	Output: SYSEN1 (external system enable)
GPIO_5	General-purpose I/O	Output: CLK32KGO1V8 (32-kHz digital-fated output clock in VRTC domain) or SYNCCLKOUT (Fallback synchronization clock for SMPS, 2.2MHz)
GPIO_6	General-purpose I/O	Output: SYSEN2 (external system enable)
GPIO_7	General-purpose I/O	Input: POWERHOLD

For GPIO characteristics, refer to:

- Pin description (see Section 3)
- Electrical characteristics (see Section 4.16, and Section 4.17)
- Pullup and pulldown characteristics (see Section 4.18)

Each GPIO event can generate an interrupt on either rising and/or falling edge and each line is individually maskable (as described in 节 5.3.8)

All GPIOs can be used as wake-up events.

注

GPIO_4 and GPIO_6 are in the VIO domain and need the I/O supply to be available.

When configured in OTP as SYSEN1 and SYSEN2, GPIO_4 and GPIO_6 can be programmed to be part of power-up sequence.

Selection between primary and secondary functions is controlled through the registers PRIMARY_SECONDARY_PAD1 and PRIMARY_SECONDARY_PAD2.

When configured as primary functions, all GPIOs are controlled through the following set of registers:

- GPIO_DAT_DIR: Configure each GPIO direction individually (Read or Write)
- GPIO_DATA_IN: Data line-in when configured as an input (Read Only)
- GPIO_DATA_OUT: Data line-out when configured as an output (Read or Write)
- GPIO_DEBOUNCE_EN: Enable each GPIO debouncing individually (Read or Write)
- GPIO_CTRL: Global GPIO control to enable or disable all GPIOs (Read or Write)
- GPIO_CLEAR_DATA_OUT: Clear each GPIO data out individually (Write Only)
- GPIO_SET_DATA_OUT: Set each GPIO data out individually (Write Only)
- PU_PD_GPIO_CTRL1, PU_PD_GPIO_CTRL2: Configure each line pull up and pull down (Read or Write)
- OD_OUTPUT_GPIO_CTRL: Enable individual open-drain output (Read or Write)

When configured as secondary functions, none of the GPIO control registers (see 表 5-5) affect GPIO lines. Line configuration (pullup, pulldown, open-drain) for secondary functions is held in a separate register set, as well as specific function settings.

5.3.6.1 REGEN Output

Dedicated REGEN signal REGEN1 can be programmed to be part of power sequences to enable external devices like external SMPS. The REGEN2 signal is MUXed in GPIO_2, and when REGEN2 mode is selected it can also be programmed to be part of power sequences. All REGEN signals are at VSYS level.

5.3.7 Thermal Monitoring

The TPS659037 device includes several thermal monitoring functions:

- Thermal protection module internal to the TPS659037 device, placed close to the SMPS and LDO modules
- Platform temperature monitoring with an external NTC resistor
- Platform temperature monitoring with an external diode

The TPS659037 device integrates two thermal detection modules to monitor the temperature of the die. These modules are placed on opposite sides of the chip and close to the LDO and SMPS modules. Overtemperature at either module generates a warning to the system; if the temperature continues to rise, the TPS659037 device shuts down before damage to the die can occur.

Thus, two protection levels are available:

- A hot-die (HD) function sends an interrupt to software. Software is expected to close any noncritical running tasks to reduce power.
- A thermal shutdown (TS) function immediately begins the TPS659037 device switch-off.

By default, thermal protection is always enabled except in the BACKUP or OFF state. Disabling thermal protection in SLEEP mode for minimum power consumption is possible.

To use thermal monitoring in the system:

- Set the value for the HD temperature threshold with the OSC_THERM_CTRL.THERM_HD_SEL[1:0] register.
- TS can be disabled in SLEEP mode by setting the THERM_OFF_IN_SLEEP bit to 1 in the OSC_THERM_CTRL register.
- During operation, if the die temperature increases above HD_THR_SEL, an interrupt (INT1.HOTDIE) is sent to the host processor. Immediate action to reduce the TPS659037 device power dissipation must be taken by shutting down some function.
- If the die temperature of the TPS659037 device rises further (above 148°C) an immediate shutdown occurs. A TS event indication is written to the status register, INT1_STATUS_HOTDIE. The system cannot restart until the temperature falls below HD_THR_SEL.

5.3.7.1 Hot-Die Function (HD)

The HD detector monitors the temperature of the die and provides a warning to the host processor through the interrupt system when temperature reaches a critical value. The threshold value must be set below the thermal shutdown threshold. Hysteresis is added to the HD detection to avoid the generation of multiple interrupts.

The integrated HD function provides the host PM software with an early warning overtemperature condition. This monitoring system is connected to the interrupt controller and can send an interrupt when the temperature is higher than the programmed threshold. The TPS659037 device allows the programming of four junction-temperature thresholds to increase the flexibility of the system: in nominal conditions, the threshold triggering of the interrupt can be set from 117°C to 130°C. The HD hysteresis is 10°C in typical conditions.

When an interrupt is triggered by the power-management software, immediate action must be taken to reduce the amount of power drawn from the TPS659037 device (for example, noncritical applications must be closed).

5.3.7.2 Thermal Shutdown (TS)

The TS detector monitors the temperature on the die. If the junction reaches a temperature at which damage can occur, a switch-off transition is initiated and a thermal shutdown event is written into a status register.

The system cannot be restarted until the die temperature falls below the HD threshold.

5.3.7.3 Temperature Monitoring With External NTC Resistor or Diode

The GPADC_IN1 channel can be used to measure a temperature with an external NTC resistor. External pullup and pulldown resistors can be connected to the input to linearize the characteristics of the NTC resistor. The temperature limits are set by external resistors.

5.3.8 Interrupts

表 5-6 lists the TPS659037 device interrupts.

These interrupts are split into four register groups (INT1, INT2, INT3, INT4) and each group has three associated control registers:

- INTx_STATUS: Reflects which interrupt source has triggered an interrupt event
- INTx_MASK: Used to mask any source of interrupt, to avoid generating an interrupt on a specified source
- INTx_LINE_STATE: Reflects the real-time state of each line associated to each source of interrupt

The INT4 register group has two additional registers, INT4_EDGE_DETECT1 and INT4_EDGE_DETECT2, to independently configure rising and falling edge detection.

All interrupts are logically combined on a single output line INT (default active low). This line is used as an external interrupt line to warn the host processor of any interrupt event that has occurred within the TPS659037 device. The host processor has to read the interrupt status registers (INTx_STATUS) through the control interface (I^2C or SPI) to identify the interrupt sources. Any interrupt source can be masked by programming the corresponding mask register (INTx_MASK). When an interrupt is masked, its associated event detection mechanism is disabled. Therefore the corresponding STATUS bit is not updated and the INT line is not triggered if the masked event occurs. Any event happening while its corresponding interrupt is masked is lost. If an interrupt is masked after it has been triggered (event has occurred and has not yet been cleared), then the STATUS bit reflects the event until it is cleared and it does not trigger again if a new event occurs (because it is now masked).

Because some interrupts are sources of ON requests (see 表 5-6), source masking can be used to mask a specific device switch-on event. Because an active interrupt line INT is treated as an ON request, any interrupt not masked must be cleared to allow the execution of a SLEEP sequence of the TPS659037 device when requested.

The INT line polarity and interrupts clearing method can be configured using the INT_CTRL register.

An INT line event can be provided to the host in either SLEEP or ACTIVE mode, depending on the setting of the OSC_THERM_CTRL.INT_MASK_IN_SLEEP bit.

When a new interrupt occurs while the interrupt line INT is still active (not all interrupts have been cleared), then:

- If the new interrupt source is the same as the one that has already triggered the INT line, it can be discarded or stored as a pending interrupt depending on the setting of the INT_CTRL.INT_PENDING bit.
  - When the INT_CTRL.INT_PENDING bit is active (default), then any new interrupt event occurring on the same source (while the INT line is still active) is stored as a pending interrupt. Because only one level of pending interrupt can be stored for a given source, when several events (more than two) occur on the same source, only the last one is stored. While an interrupt is pending, two accesses are needed (either read or write) to clear the STATUS bit: one access for the actual interrupt and another for the pending interrupt. Note: two consecutive read or write operations to the same register clear only one interrupt. Another register must be accessed between the two read or write clear operations. Example for clear-on-read: when INT signal is active, read all four INTx_STATUS registers in sequence to collect status of all potential interrupt sources. Read access clears the full register for an active or actual interrupt. If the INT line is still active, repeat read sequence to check and clear pending interrupts.
  - When the INT_CTRL.INT_PENDING bit is inactive, then any new interrupt event occurring on the same source (while the INT line is still active) is discarded. Note: two consecutive read or write operations to the same register clear only one interrupt. Another register must be accessed between the two read or write clear operations.
- If the new interrupt source is different from the one that already triggered the INT line, then it is stored immediately into its corresponding STATUS bit.

To clear the interrupt line, all status registers must be cleared. The clearing of all status registers is achieved by using a clear-on-read or a clear-on-write method. The clearing method is selectable though the INT_CTRL.INT_CLEAR bit. When set, the clearing method applies to all bits for all interrupts.

- Clear-on-read
  - Read access to a single status register clears all the bits for only this specific register (8 bits). Therefore, clearing all interrupts requests to read the four status registers. If the INT line is still active when the four read accesses complete, then another interrupt event has occurred during the read process; therefore the read sequence must be repeated.
- Clear-on-write
  - This method is bit-based; setting a specific bit to 1 clears only the written bit. Therefore, to clear a complete status register, 0xFF must be written. Clearing all interrupts requests to write 0xFF into the four status registers. If the INT line is still active when the four write accesses are complete, then another interrupt event has occurred during the write process; therefore the write sequence must be repeated.

表 5-6. Interrupt Sources

INTERRUPT	ASSOCIATED EVENT	EDGES DETECTION	ON REQUEST	REGISTER GROUP	REGISTER BIT	DESCRIPTION
VSYS_MON	Internal event	Rising and falling	Never	INT1	6	System voltage monitoring interrupt: Triggered when system voltage has crossed the configured threshold in VSYS_MON register.
HOTDIE	Internal event	Rising and falling	Never		5	Hot-die temperature interrupt: The embedded thermal monitoring module has detected a die temperature above the hot-die detection threshold. Interrupt is generated in ACTIVE and SLEEP state, not in OFF state.
PWRDOWN	PWRDOWN (pin)	Rising and falling	Never		4	Power-down interrupt: Triggered when the event is detected on the PWRDOWN pin.
RPWRON	RPWRON (pin)	Falling	Always (INT mask don't care)		3	Remote power-on interrupt: Triggered when a signal change is detected. Interrupt is generated in ACTIVE and SLEEP state, not in OFF state.
LONG_PRESS_KEY	PWRON (pin)	Falling	Never		2	Power-on long key-press interrupt. Triggered when PWRON is low during more than the long-press delay LONG_PRESS_KEY.LPK_TIME.
PWRON	PWRON (pin)	Falling	Always (INT mask don't care)		1	Power-on interrupt: Triggered when PWRON button is pressed (low) while the TPS659037 device is on. Interrupt is generated in ACTIVE and SLEEP state, not in OFF state.
SHORT	Internal event	Rising	Yes (if INT not masked)	INT2	6	Short interrupt: Triggered when at least one of the power resources (SMPS or LDO) has its output shorted.
RESET_IN	RESET_IN (pin)	Rising	Never		4	RESET_IN interrupt: Triggered when event is detected on RESET_IN pin.
WDT	Internal event	Rising	Never		2	Watchdog time-out interrupt: Triggered when watchdog time-out has expired.
RTC_TIMER	Internal event	Rising	Yes (if INT not masked)		1	Real-time clock timer interrupt: Triggered at programmed regular period of time (every second or minute). Running in ACTIVE, OFF, and SLEEP state, default inactive.
RTC_ALARM	Internal event	Rising	Yes (if INT not masked)		0	Real-time clock alarm interrupt: Triggered at programmed determinate date and time.
VBUS	VBUS (pin)	Rising and falling	Yes (if INT not masked)	INT3	7	VBUS wake-up comparator interrupt. Active in OFF state. Triggered when VBUS present.
GPADC_EOC_SW	Internal event	N/A	Yes (if INT not masked)		2	GPADC software end of conversion interrupt: Triggered when conversion result is available.
GPADC_AUTO_1	Internal event	N/A	Yes (if INT not masked)		1	GPADC automatic periodic conversion 1: Triggered when result of conversion is either above or below (depending on configuration) reference threshold GPADC_AUTO_CONV1_LSB and GPADC_AUTO_CONV1_MSB.
GPADC_AUTO_0	Internal event	N/A	Yes (if INT not masked)		0	GPADC automatic periodic conversion 0: Triggered when result of conversion is either above or below (depending on configuration) reference threshold GPADC_AUTO_CONV0_LSB and GPADC_AUTO_CONV0_MSB.
GPIO_7	GPIO_7 (pin)	Rising and/or falling	Yes (if INT not masked)	INT4	7	GPIO_7 rising- or falling-edge detection interrupt
GPIO_6	GPIO_6 (pin)	Rising and/or falling	Yes (if INT not masked)		6	GPIO_6 rising- or falling-edge detection interrupt
GPIO_5	GPIO_5 (pin)	Rising and/or falling	Yes (if INT not masked)		5	GPIO_5 rising- or falling-edge detection interrupt
GPIO_4	GPIO_4 (pin)	Rising and/or falling	Yes (if INT not masked)		4	GPIO_4 rising- or falling-edge detection interrupt
GPIO_3	GPIO_3 (pin)	Rising and/or falling	Yes (if INT not masked)		3	GPIO_3 rising- or falling-edge detection interrupt
GPIO_2	GPIO_2 (pin)	Rising and/or falling	Yes (if INT not masked)		2	GPIO_2 rising- or falling-edge detection interrupt
GPIO_1	GPIO_1 (pin)	Rising and/or falling	Yes (if INT not masked)		1	GPIO_1 rising- or falling-edge detection interrupt
GPIO_0	GPIO_0 (pin)	Rising and/or falling	Yes (if INT not masked)		0	GPIO_0 rising- or falling-edge detection interrupt

5.3.9 Control Interfaces

The TPS659037 device has two exclusive selectable (from factory settings) interfaces; two high-speed I^{2}C interfaces (I2C1_SCL_SCK or I2C1_SDA_SDI and I2C2_SCL_SCE or I2C2_SDA_SDO) or one SPI (I2C1_SCL_SCK, I2C1_SDA_SDI, I2C2_SDA_SDO, or I2C2_SCL_SCE). Both are used to fully control and configure the TPS659037 device and have access to all the registers. When the I^{2}C configuration is selected the I2C1_SCL_SCK or I2C1_SDA_SDI, a general purpose control (GPC) interface is dedicated to configure the TPS659037 device and the I2C2_SCL_SCE or I2C2_SDA_SDO interface dynamic voltage scaling (DVS) is dedicated to dynamically change the output voltage of the SMPS converters. The DVS I^{2}C interface has access only to the voltage scaling registers of the SMPS converters (read and write mode).

5.3.9.1 I^{2}C Interfaces

The GPC I^{2}C interface (I2C1_SCL_SCK and I2C1_SDA_SDI) is dedicated to access the configuration registers of all the resources of the system.

The DVS I^{2}C interface (I2C2_SCL_SCE and I2C_SDA_SDO) is dedicated to access the DVS registers independently from the GPC I^{2}C.

The control interfaces comply with the HS-I^{2}C specification and support the following features:

- Mode: Slave only (receiver and transmitter)
- Speed:
  – Standard mode (100 kbps)
  – Fast mode (400 kbps)
  – High-speed mode (3.4 Mbps)
- Addressing: 7-bit mode addressing device

The following features are not supported:

- 10-bit addressing
- General call
- Master mode (bus arbitration and clock generation)

I^{2}C is a 2-wire serial interface developed by NXP (formerly Philips Semiconductor) (see *I^{2}C-Bus Specification and user manual, Rev 03, June 2007*). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, the SDA and SCL lines are pulled high. All the I^{2}C-compatible devices connect to the I^{2}C bus through open-drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the start and stop of data transfers. A slave device receives and/or transmits data on the bus under control of the master device. The data transfer protocol for standard and fast modes is exactly the same, and they are referred to as F/S mode in this document. The protocol for high-speed mode is different from F/S mode, and it is referred to as HS mode.

5.3.9.1.1 I^{2}C Implementation

The standard I^{2}C 7-bit slave device address is set to 010010xx (binary) where the two least-significant bits are used for page selection.

The TPS659037 device is organized in five internal pages of 256 bytes (registers) as follows:

- Slave device address 0x48: Power registers
- Slave device address 0x49: Interfaces and auxiliaries
- Slave device address 0x4A: Trimming and test
- Slave device address 0x4B: OTP
- Slave device address 0x12: DVS

The device address for the DVS I^{2}C interface is set to 0x12.

If one of the addresses conflicts with another device I²C address, it is possible to remap each address to a fixed alternative one as described in 表 5-7. I²C for DVS is fixed because it is dedicated interface.

表 5-7. I²C Address Configuration

REGISTER	BIT	PAGE	ADDRESSES
I2C_SPI	ID_I2C1[0]	Power registers	ID_I2C1[0] = 0: 0x48
			ID_I2C1[0] = 1: 0x58
	ID_I2C1[1]	Interfaces and auxiliaries	ID_I2C1[1] = 0: 0x49
			ID_I2C1[1] = 1: 0x59
	ID_I2C1[2]	Trimming and test	ID_I2C1[2] = 0: 0x4A
			ID_I2C1[2] = 1: 0x5A
	ID_I2C1[3]	OTP	ID_I2C1[3] = 0: 0x4B
			ID_I2C1[3] = 1: 0x5B
	ID_IDC2	DVS	ID_I2C2 = 0: 0x12

5.3.9.1.2 F/S Mode Protocol

The master initiates data transfer by generating a START condition. The START condition is when a high-to-low transition occurs on the SDA line while SCL is high (see 图 5-11). All I²C-compatible devices should recognize a START condition.

The master then generates the SCL pulses and transmits the 7-bit address and the read or write direction bit (R/W) on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see 图 5-12). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see 图 5-13) by pulling the SDA line low during the entire high period of the ninth SCL cycle. When this acknowledge is detected, the master knows that the communication link with a slave has been established.

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver must acknowledge the data sent by the transmitter. An acknowledge signal can be generated by the master or the slave, depending on which one is the receiver. Nine-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a STOP condition by pulling the SDA line from low to high while the SCL line is high (see 图 5-11). This releases the bus and stops the communication link with the addressed slave. All I²C-compatible devices must recognize the STOP condition. Upon the receipt of a STOP condition, all devices know that the bus is released, and they wait for a START condition followed by a matching address.

Attempting to read data from register addresses not listed in this section results in 0xFF being read out.

5.3.9.1.3 HS Mode Protocol

When the bus is idle, the SDA and SCL lines are pulled high by the pullup devices.

The master generates a START condition followed by a valid serial byte containing HS master code 00001XXX. This transmission is made in F/S mode at no more than 400 kbps. No device is allowed to acknowledge the HS master code, but all devices must recognize it and switch their internal setting to support 3.4-Mbps operation.

The master then generates a REPEATED START condition (a REPEATED START condition has the same timing as the START condition). After the REPEATED START condition, the protocol is the same as F/S mode, except transmission speeds up to 3.4 Mbps are allowed. A STOP condition ends the HS mode and switches all the internal settings of the slave devices to support F/S mode. Instead of using a STOP condition, REPEATED START conditions are used to secure the bus in HS mode.

Attempting to read data from register addresses not listed in this section results in 0xFF being read out.

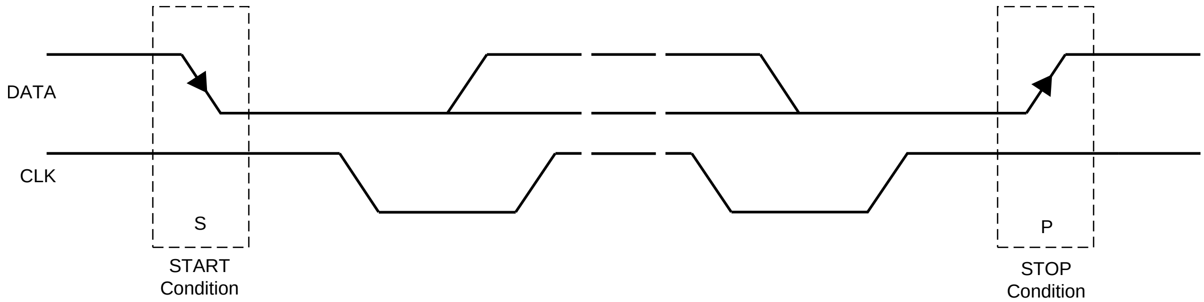


图 5-11. START and STOP Conditions

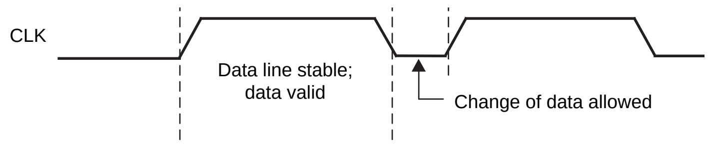


图 5-12. Bit Transfer on the Serial Interface

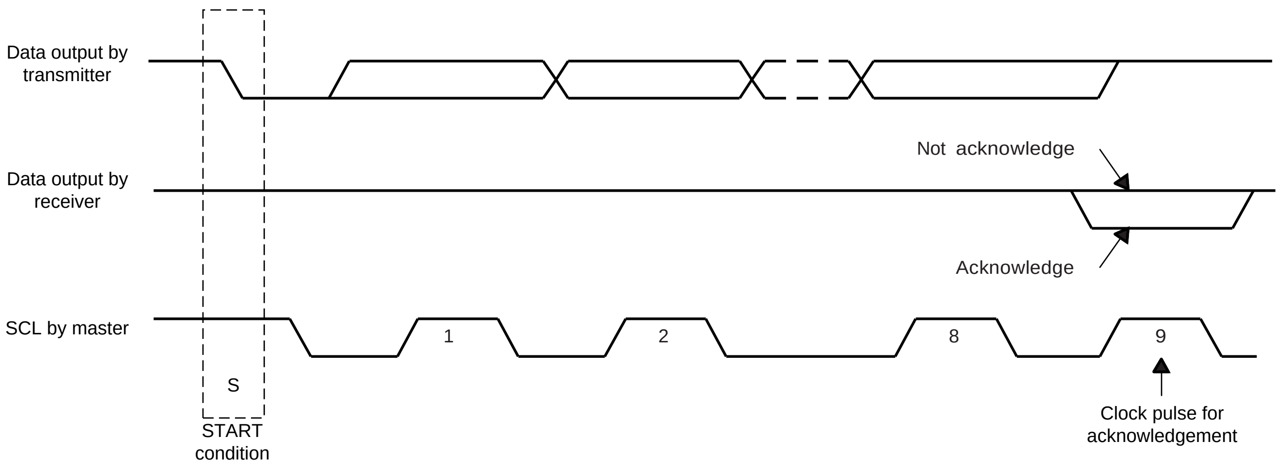


图 5-13. Acknowledge on the I²C Bus

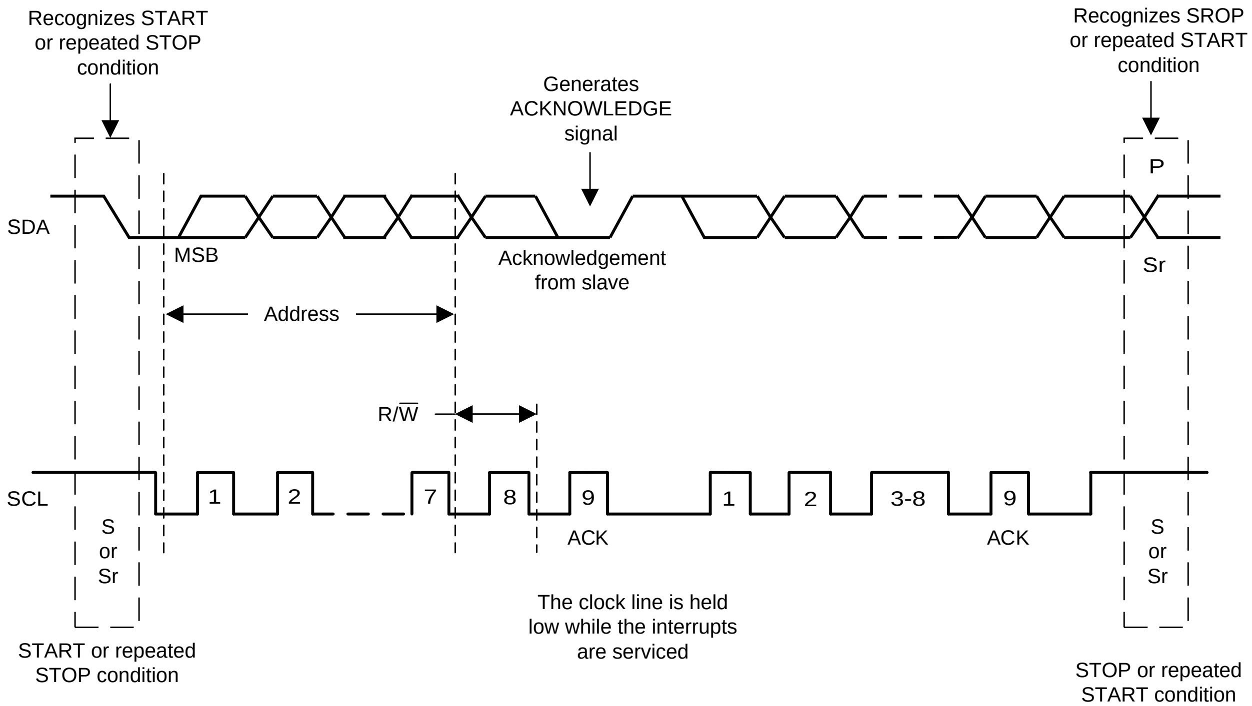


图 5-14. Bus Protocol

5.3.9.2 Serial-Peripheral Interface (SPI)

The SPI is a 4-wire slave interface used to access and configure the TPS659037 device. The SPI allows read-and-write access to the configuration registers of all resources of the system.

The SPI uses the following signals:

- SCE (I2C2_SCL_SCE): Chip enable – Input driven by host master, used to initiate and terminate a transaction
- SCK (I2C1_SCL_SCK): Clock – Input driven by host master, used as master clock for data transaction
- SDI (I2C1_SDA_SDI): Data input – Input driven by host master, used as data line from master to slave
- SDO (I2C2_SDA_SDO): Data output – Output driven by the TPS659037 device, used as data line from slave to master and defaults to high impedance

5.3.9.2.1 SPI Modes

The SPI does not have access to the OTP and DVS registers (slave device address 0x4B & 0x12) of the device. The SPI_PAGE_CTRL.SPI_PAGE_ACCESS regsiter can be configured to access all other registers (slave device address 0x48, 0x49, & 0x4A) by:

- SPI_PAGE_CTRL.SPI_PAGE_ACCESS = 0: Page1 = 0x48, Page2 = 0x49
- SPI_PAGE_CTRL.SPI_PAGE_ACCESS = 1: Page1 = 0x48, Page3 = 0x4A

This SPI supports two access modes (Note: all shifts are done MSB first (Data, Address, Page):

- Single access (read or write)
  - This consists of fetching and storing one single data location. The protocol is depicted in 图 5-15.
  - The R/W bit is always provided first, followed by page address and register address fields. When R/W = 0, a read access is performed. When R/W = 1, a write access is performed.
  - 1 burst bit indicates if following transfer is a single access (BURST = 0) or a burst access (BURST = 1).
  - 4 unused bits follow the burst bit and finally the 8-bit data is either shifted in (write) or out (read).
  - For a write access, the data output line SDO is invalid (useless) during the whole transaction.
  - For a read access, the data output line SDO is invalid during the unused bits (time slot used for data fetch) and then becomes active or valid after the unused bits.
- Burst access (read or write)
  - This consists of fetching and storing several data at contiguous locations. The protocol is depicted in 图 5-16.
  - The R/W bit is always provided first, followed by page address and register address fields. When R/W = 0, a read access is performed. When R/W = 1, a write access is performed.
  - 1 burst bit indicates if following transfer is a single access (BURST = 0) or a burst access (BURST = 1).
  - 4 unused bits follow the burst bit and finally packets of 8-bit data are either shifted in (write) or out (read).
  - The transaction remains active as long as the SCE signal is maintained high by the host.
  - The address is automatically incremented internally for each new 8-bit packet received.
  - The host must pull the SCE signal low after a complete 8-bit data is transferred, otherwise the last transaction is discarded.
  - For a write access, the data output line SDO is invalid (useless) during the whole transaction.
  - For a read access, the data output line SDO is invalid during the unused bits (time slot used for data fetch) and then becomes active or valid after the unused bits.

5.3.9.2.2 SPI Protocol

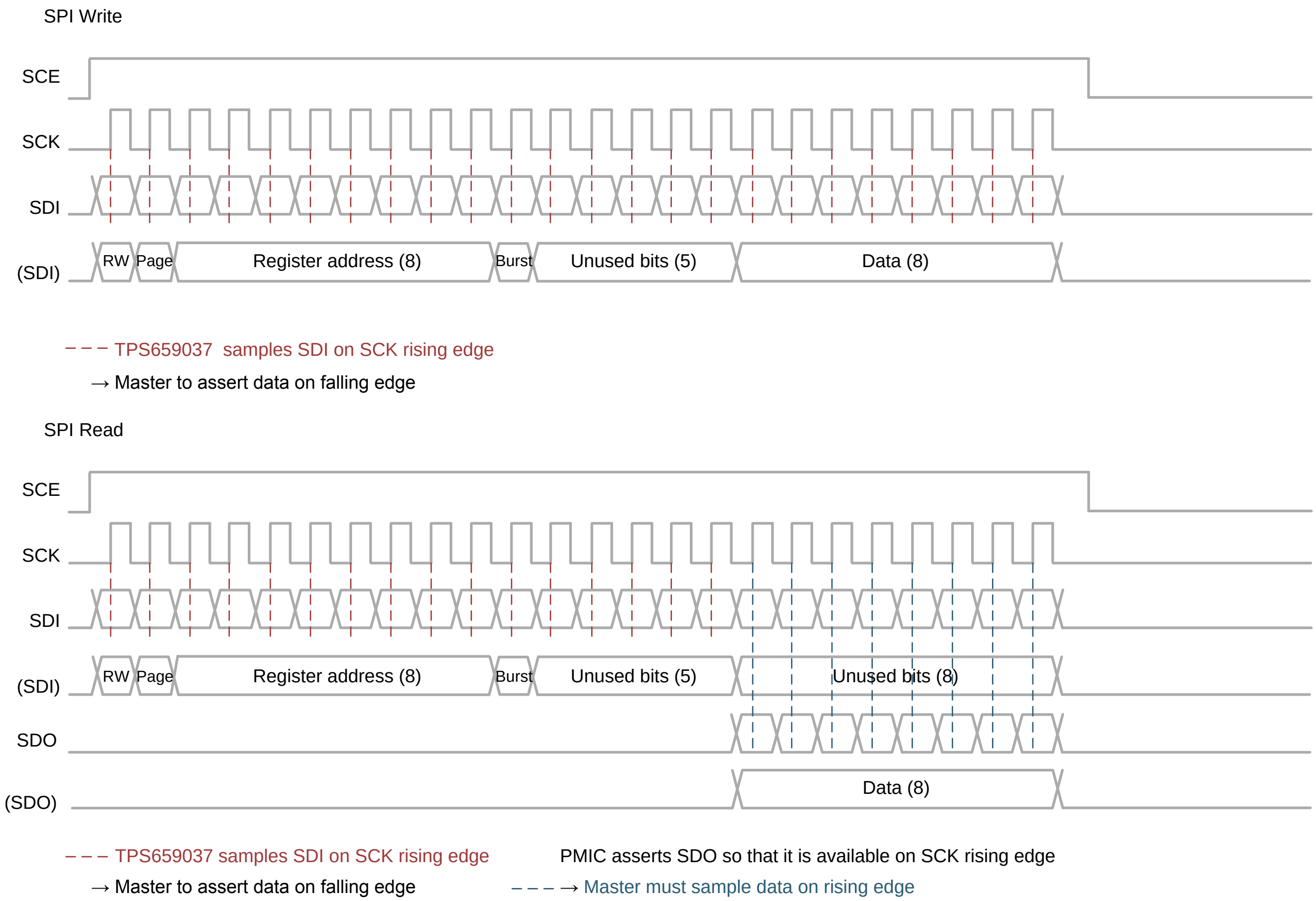


图 5-15. SPI Single Read and Write Access

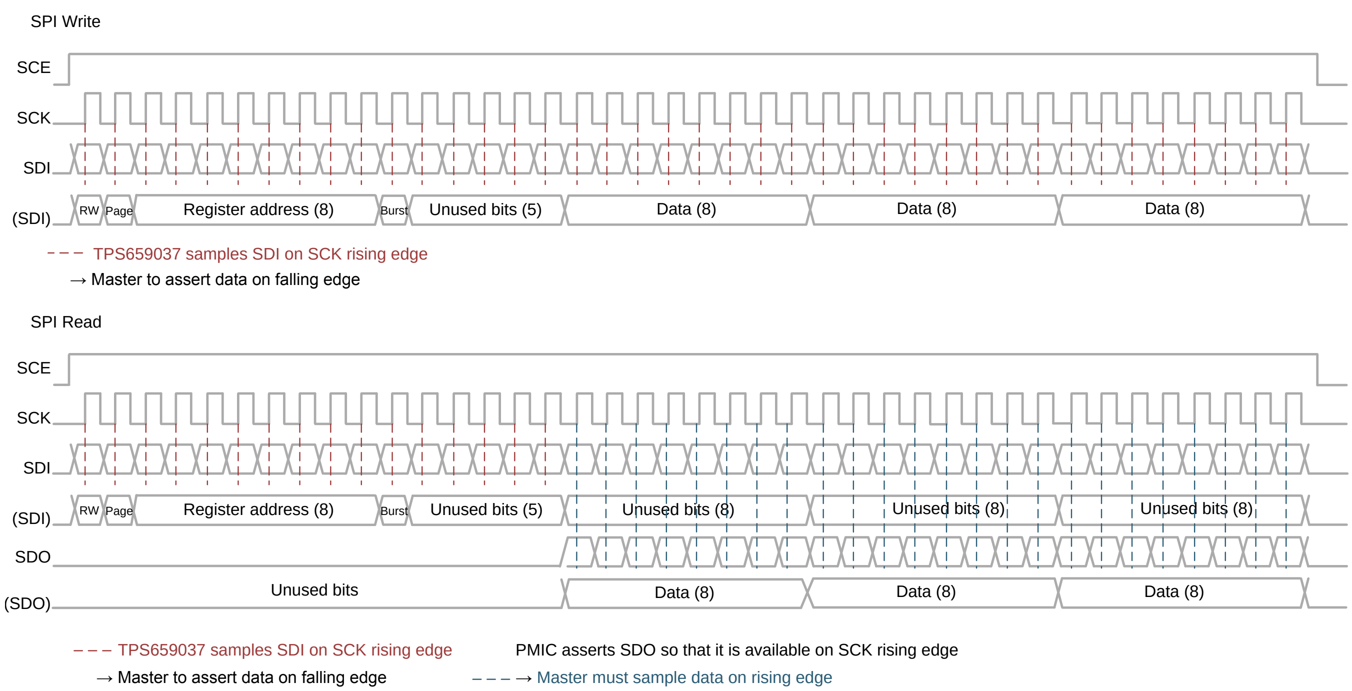


图 5-16. SPI Burst Read and Write Access

5.3.10 Device Identification

The following registers can differentiate the TPS659037 device being used.

表 5-8. TPS65903x-Q1 Device ID

REGISTER NAME	REGISTER DESCRIPTION		VALUE
PRODUCT_ID_MSB	For all TPS659037 devices, this register will have the same value.		0x90
PRODUCT_ID_LSB	For all TPS659037 devices, this register will have the same value.		0x39
DESIGNREV	This register distinguishes which silicon version is used.	Revision 1.0	0x0
		Revision 1.1	0x1
		Revision 1.2	0x2
		Revision 1.3	0x3
		Revision 1.4	0x4
SW_REVISION	This register will be representative of the OTP version programmed on the device.		OTP dependent

5.4 Device Functional Modes

5.4.1 Embedded Power Controller

The EPC is composed of three main modules:

- An event arbitration module used to prioritize ON, OFF, WAKE, and SLEEP requests.
- A power state-machine used to determine which power sequence to execute, based on the system state (supplies, temperature, and so forth) and requested transition (from the event arbitration module).
- A power sequencer that fetches the selected power sequence from OTP and executes it. The power sequencer sets up and controls all resources accordingly, based on the definition of each sequence.

图 5-17 shows the EPC block diagram.

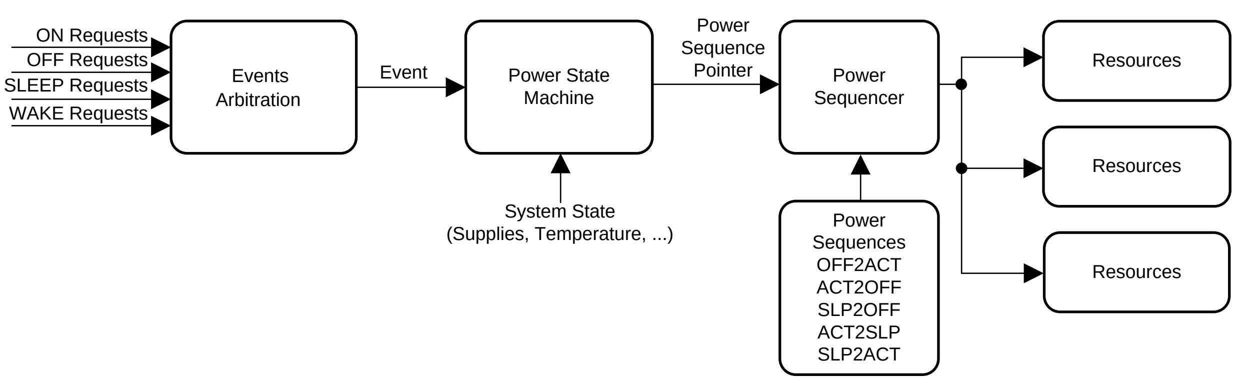


图 5-17. EPC Block Diagram

The power state-machine is defined through the following states:

NO SUPPLY The TPS659037 device is not powered by any energy source on the system power rail (VCC1 < POR).

BACKUP The TPS659037 device is not powered by a valid supply on the system power rail (VCC1 < VSYS_LO) (VCC > POR).

OFF The TPS659037 device is powered by a valid supply on the system power rail (VCC1 > VSYS_LO) and it is waiting for a start-up event or condition. All device resources are in the OFF state. The approximate time for the TPS659037 device to arrive the OFF state from the NO SUPPLY state, without considering the rise time of VSYS and the settling time of the VSYS_LO comparator, is approximately 5.5 ms.

ACTIVE The TPS659037 device is powered by a valid supply on the system power rail (VCC1 > VSYS_LO) and has received a start-up event. It has switched to the ACTIVE state, having full capacity to supply the processor and other platform modules.

SLEEP The TPS659037 device is powered by a valid supply on the system power rail (VCC1 > VSYS_LO) and is in low-power mode. All configured resources are set to their low-power mode, which can be ON, SLEEP, or OFF depending on the specific resource setting. If a given resource is maintained active (ON) during low-power mode, then all its linked subsystems are automatically maintained active.

图 5-18 shows the state diagram for the power control state-machine.

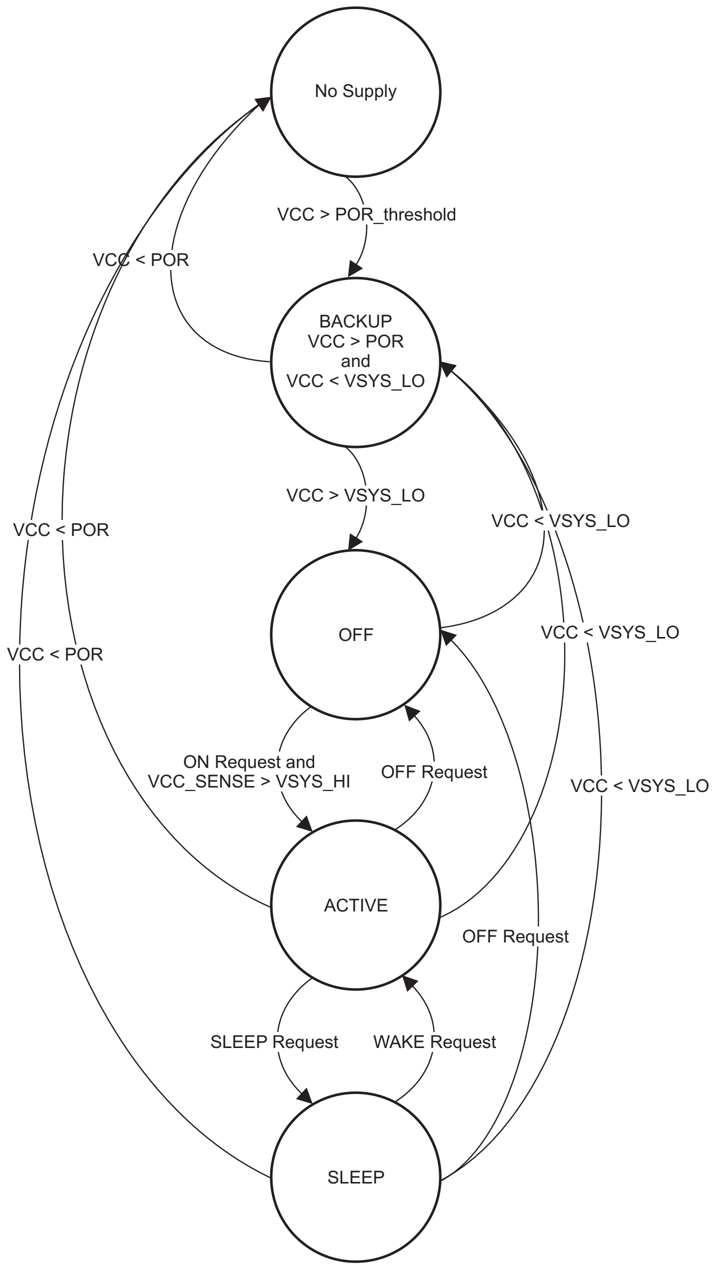


图 5-18. State Diagram for the Power Control State-Machine

Power sequences define how a resource state switches between the OFF, ACTIVE, and SLEEP states, but they have no effect during the NO SUPPLY or BACKUP states. The EPC supervises the system according to these power sequences when the TPS659037 device is brought into the OFF state from a NO SUPPLY or BACKUP state. This supervision is achieved automatically by internal hardware controlling the device before handing it over to the EPC.

The allowed power transitions are:

- OFF to ACTIVE (OFF2ACT)
- ACTIVE to OFF (ACT2OFF)
- ACTIVE to SLEEP (ACT2SLP)
- SLEEP to ACTIVE (SLP2ACT)
- SLEEP to OFF (SLP2OFF)

Each power transition consists of a sequence of one or several register accesses that controls the resources according to the EPC supervision. Because these sequences are stored in nonvolatile memory (OTP), they cannot be altered.

5.4.2 State Transition Requests

5.4.2.1 ON Requests

ON requests are used to switch on the TPS659037 device, which transitions the device from the OFF to the ACTIVE state. 表 5-9 lists the ON requests.

表 5-9. ON Requests

EVENT	MASKABLE	POLARITY	COMMENT	DEBOUNCE
RPWRON (pin)	No	Low	Level sensitive	16 ms ± 1 ms
PWRON (pin)	No	Low	Level sensitive	N/A
Part of interrupts (event)	Yes (INTx_MASK register. Default: Masked)	Event	Edge sensitive	N/A
POWERHOLD (pin)	No	High	Level sensitive	3 - 5 ms typical

If one of the events listed in 表 5-9 occurs, it powers on the device, unless one of the gating conditions listed in 表 5-10 is present. For interrupt sources that can be configured as ON requests, see 表 5-6.

表 5-10. ON Requests Gating Conditions

EVENT	MASKABLE	POLARITY	COMMENT
VSYS_HI (event)	No	Low	VCC_SENSE < VSYS_HI
HOTDIE (event)	No	High	Device temperature exceeds HOTDIE level
PWRDOWN (pin)	No	OTP configurable	
RESET_IN (pin)	No	OTP configurable	

5.4.2.2 OFF Requests

OFF requests are used to switch off the TPS659037 device, and transition the device from the SLEEP or the ACTIVE to the OFF state. 表 5-11 lists the OFF requests. OFF requests have the highest priority, and no gating conditions exist. Any OFF request is executed even though a valid SLEEP or ON request is present and force the device to go to the OFF state. When the OFF request is cleared it reacts to an ON request, if any is present.

表 5-11. OFF Requests

EVENT	MASKABLE	POLARITY	DEBOUNCE	SWITCH OFF DELAY	RESET LEVEL	RESET SEQUENCE
PWRON (pin) (long press key)	No	Low	N/A	SWOFF_DLY	HWRST	SD
PWRDOWN (pin)	No	OTP configurable		SWOFF_DLY	OTP Configurable	OTP Configurable

表 5-11. OFF Requests (continued)

EVENT	MASKABLE	POLARITY	DEBOUNCE	SWITCH OFF DELAY	RESET LEVEL	RESET SEQUENCE
WATCHDOG TIMEOUT (internal event)	N/A. WDT is disabled by default but software can enable it.	NA	N/A	SWOFF_DLY	OTP Configurable	OTP Configurable
THERMAL SHUTDOWN (internal event)	No	NA	N/A	0	OTP Configurable	OTP Configurable
RESET_IN (pin)	No	OTP configurable	N/A	SWOFF_DLY	OTP Configurable	OTP Configurable
SW_RST (register bit)	No	NA	N/A	0	OTP Configurable	OTP Configurable
DEV_ON (register bit)	No	NA	N/A	0	SWORST	SD
VSYS_LO (internal event)	No	NA		0	OTP Configurable	OTP Configurable
POWERHOLD (pin)	No	Low		0	SWORST	SD
GPADC_SHUTDOWN	Yes	NA	N/A	SWOFF_DLY	OTP Configurable	OTP Configurable

Notes:

- SWOFF_DLY is the same for all requests. When configured to a specific value (0, 1, 2, or 4 s) it is applied to all OFF requests.
- RESET_LEVEL is selectable as HWRST (wide set of registers is reset to default values) or SWORTS (more limited set of registers is reset).
- OFF requests are configured to force the EPC to either execute a shutdown (SD) or a cold restart (CR).
  - When configured to generate an SD, the EPC executes a transition to the OFF state (SLP2OFF or ACT2OFF power sequence) and remains in the OFF state.
  - When configured to generate a CR, the EPC executes a transition to the OFF state (SLP2OFF or ACT2OFF power sequence) and restarts, transitioning to the ACTIVE state (OFF2ACT power sequence) if none of the ON request gating conditions are present.
- Watchdog is disabled by default. SW can enable watchdog and lock (write protect) watchdog register (WATCHDOG).
- The DEV_ON event has a lower priority over other ON events; it forces the TPS659037 device to go to the OFF state only if no other ON conditions are keeping the device active (POWERHOLD).
- The POWERHOLD event has a lower priority over other ON events; it forces the TPS659037 device to go to the OFF state only if no other ON conditions are keeping the device active (DEV_ON).

5.4.2.3 SLEEP and WAKE Requests

SLEEP requests are used to put the TPS659037 device in the SLEEP state, meaning a transition from the ACTIVE to SLEEP state. This sets internal resources into low-power mode, as well as user-defined resources into their user predefined low-power mode. The states of the resources during active and sleep modes are defined in the LDO*_CTRL registers and SMPSx_CTRL registers.

表 5-12 lists the SLEEP requests. Any of these events trigger the ACT2SLP sequence unless pending interrupts (unmasked) occur. Only an interrupt or NSLEEP inactive (high) generates a WAKE request to wake up the TPS659037 device (exit from the SLEEP state). A WAKE request (only during the SLEEP state) wakes up the device and triggers a SLEEP2ACT or a SLEEP2OFF power sequence.

表 5-12. SLEEP Requests

EVENT	MASKABLE	POLARITY	COMMENT
NSLEEP (pin)	Yes (Default: Masked)	Low	Level sensitive

For each resource, a transition from the ACTIVE to SLEEP state or SLEEP to ACTIVE state can be controlled in two different ways:

- Through EPC sequencing (ACT2SLP or SLP2ACT power sequence), when the resource is associated to the NSLEEP signal.
- Through direct control of the resource power mode (active or sleep).
  – The user can bypass SLEEP and WAKE sequencing by having resources assigned to one external control signal (ENABLE1). This signal has direct control on the power modes (active or sleep) of any resources associated to it and it triggers an immediate switch from one mode to the other, regardless of the EPC sequencing.

All resources can therefore be associated to two external pins (NSLEEP and ENABLE1) and they switch between the SLEEP and ACTIVE states based on 表 5-13.

表 5-13. Resources SLEEP and ACTIVE Assignments

ENABLE1 ASSIGNMENT	NSLEEP ASSIGNMENT	ENABLE1 PIN STATE	NSLEEP PIN STATE	STATE	TRANSITION
0	0	Don't care	Don't care	ACTIVE	None
0	1	Don't care	0 ↔ 1	SLEEP ↔ ACTIVE	Sequenced
1	0	0 ↔ 1	Don't care	SLEEP ↔ ACTIVE	Immediate
1	1	0	0 ↔ 1	SLEEP ↔ ACTIVE	Sequenced
		1	0 ↔ 1	ACTIVE	None
		0 ↔ 1	0	SLEEP ↔ ACTIVE	Immediate
		0 ↔ 1	1	ACTIVE	None

注

- The polarity of the NSLEEP and ENABLE1 signals is configurable through the POLARITY_CTRL register. By default:
  – ENABLE1 is active high; a transition from 0 to 1 requests a transition from SLEEP to ACTIVE.
  – NSLEEP is active low; a transition from 1 to 0 requests a transition from ACTIVE to SLEEP.
- Resource assignments to the NSLEEP and ENABLE1 signals are configured in the ENABLEx_YYY_ASSIGN and NSLEEP_YYY_ASSIGN registers (where x = 1 or 2 and YYY = RES or SMPS or LDO)
- Several resources can be assigned to the same ENABLE1 signal and therefore, when triggered, they all switch their power mode at the same time.
- When resources are assigned only to the NSLEEP signal, their respective switching order is controlled and defined in the power sequence.
- When a resource is not assigned to any signal (NSLEEP and ENABLE1), it never switches from the ACTIVE to SLEEP state. The resource always remains in active mode.

CAUTION

A defect in the digital controller of the TPS659037 device was discovered, which may cause the PLL to shut down unexpectedly under the following sequence of events:

- PLL is programmed to be OFF under SLEEP mode through the PLLEN_CTRL register
- NSLEEP is assigned to control the entering of SLEEP mode for the PLL through the NSLEEP_RES_ASSIGN register
- The TPS659037 device goes through a SLP2OFF state transition followed by an OFF2ACT state transition
- PLL is again assigned to be OFF in SLEEP mode through the programming of the PLLEN_CTRL and the NSLEEP_RES_ASSIGN registers while the TPS659037 device remains in ACTIVE mode

Two possible actions are recommended to help prevent the PLL from shutting down unexpectedly:

- [Hardware Implementation] Toggle the NSLEEP pin twice to force the ACT2SLP and SLP2ACT state transitions as soon as the TPS659037 device wakes up from back to back SLP2OFF and OFF2ACT state transitions
- [Software Implementation] Toggle the NSLEEP_POLARITY bit (0 → 1 → 0) of the POLARITY_CTRL register to force the ACT2SLP and SLP2ACT device state transitions as soon as the TPS659037 device wakes up from back to back SLP2OFF and OFF2ACT state transitions

5.4.3 Power Sequences

A power sequence is an automatic pre-programmed sequence handled by the TPS659037 device to configure the device resources: SMPSs, LDOs, 32-kHz clock, part of GPIOs, , REGEN signals) into on, off, or sleep modes. See 节 5.3.6 for GPIO details.

图 5-19 shows an example of an OFF2ACT transition followed by an ACT2OFF transition. The sequence is triggered through PWRON pin and the resources controlled (for this example) are: SMPS8, LDO1, SMPS12, SMPS45, REGEN1, LDOLN, LDOUSB, and LDO2. The time between each resource enable and disable ($t_{(instX)}$) is also part of the preprogrammed sequence definition.

When a resource is not assigned to any power sequence, it remains in off mode. The user (through software) can enable and configure this resource independently after the power sequence completes.

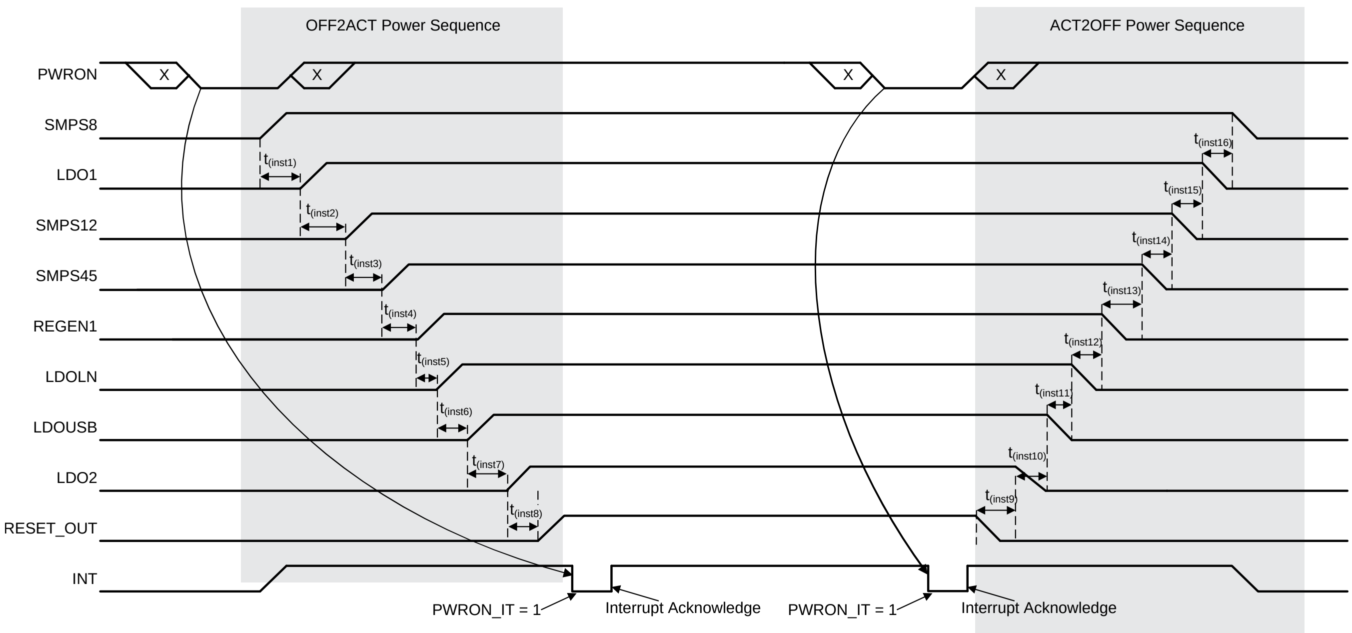


图 5-19. Power Sequence Example

The power sequence of the TPS659037 device is defined according to the processor requirements. For more information, refer to *TPS659037 User's Guide to Power AM572x and AM571x*.

5.4.4 Startup Timing and RESET_OUT Generation

The total start-up time of the TPS659037 device from the first supply insertion until the release of reset to the processor is defined by the boot time of internal resources as well as the OTP defined boot sequence.

Following figure shows the power up sequence timing and the generation of the RESET_OUT signal.

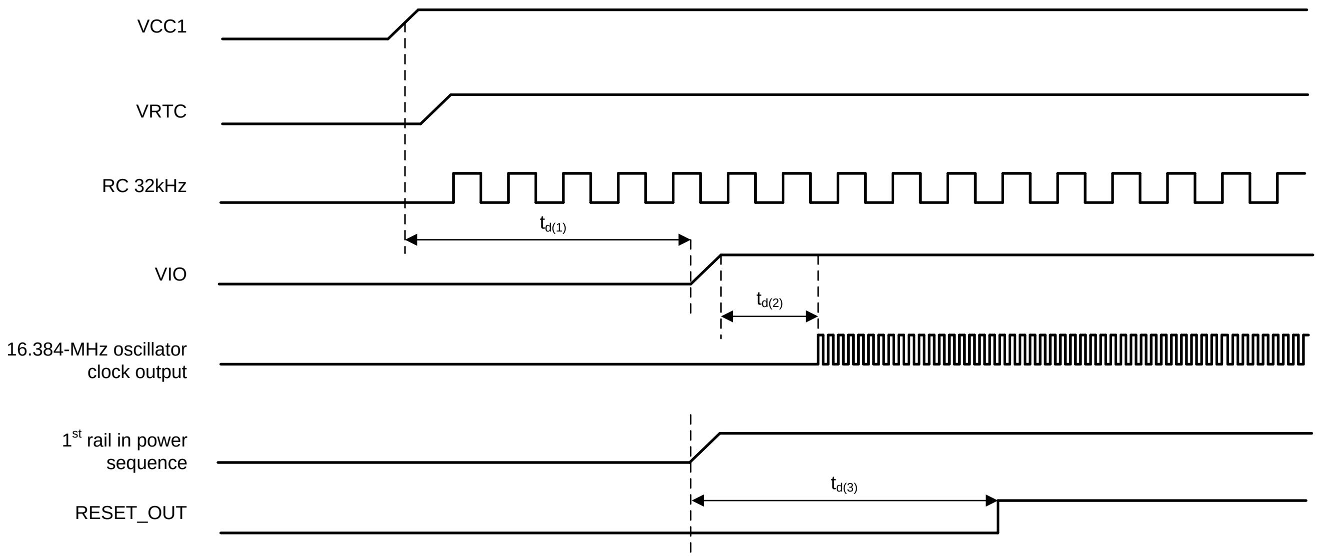


图 5-20. Startup Timing Diagram

The $t_{d(1)}$ time is the delay between VCC1 crossing the POR threshold and VIO (first rail in the power sequence) rising up. The $t_{d(1)}$ time must be at least 6 ms. If the time from VCC to VIO is less than 6 ms, the VIO buffers are supplied while the OTP is still being initialized, which could cause glitches on any VIO output buffer. Supplying VIO at least 6 ms after supplying VCC makes sure that the OTP is initialized and the output buffers are held low when VIO is supplied. The VIO_IN pin may be supplied before or after the first rail in the power sequence is enabled, as long as it is at least 6 ms after VCC.

The $t_{d(2)}$ time is the internal 16.384-MHz crystal oscillator start-up time, or the external 32-kHz clock input availability delay time.

The $t_{d(3)}$ time is the delay between the power up sequence start and RESET_OUT release. RESET_OUT is released when the power up sequence is complete and one of the following:

- The 16.384-MHz clock is stabilized if the 16.384-MHz crystal is present and the oscillator is enable.
- The external 32-kHz clock is stabilized and the 16.384-MHz oscillator is bypassed.
- The GATE_RESET_OUT_OTP bit is used to allow the TPS659037 device to power up without the presence of the 16.384-MHz crystal nor the external 32-kHz clock input.

The duration of the power-up sequence depends on OTP programming; average value is about 10 ms.

5.4.5 Power On Acknowledge

The TPS659037 device is designed to support the following power on acknowledge modes: POWERHOLD mode and AUTODEVON mode.

5.4.5.1 POWERHOLD Mode

In POWERHOLD mode, the acknowledge of the power on is achieved through a dedicated pin, POWERHOLD. Upon receipt of an ON request, the TPS659037 device initiates the power-up sequence and asserts the RESET_OUT pin high when it is in the ACTIVE state (reset released). While in the ACTIVE state, the device remains active for 8 s and then automatically shuts down. During this time-frame, to keep the device active, the host processor must assert and keep the POWERHOLD pin high. If the POWERHOLD pin is then set back to low, it is interpreted as an OFF request by the TPS659037 device.

图 5-21 shows the POWERHOLD mode timing diagrams.

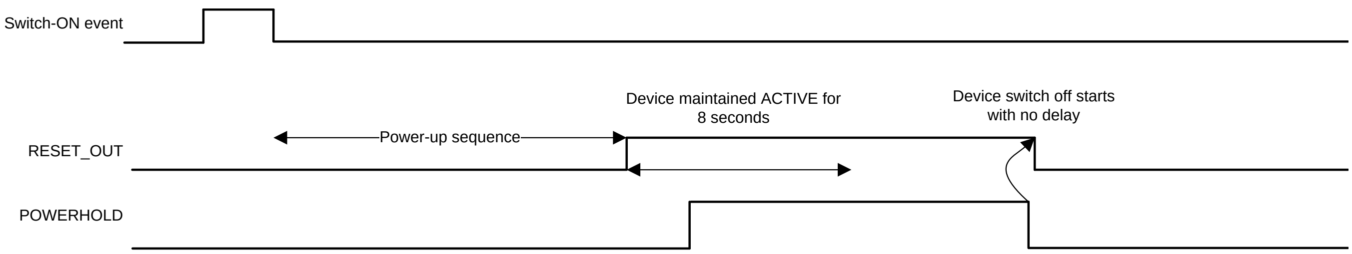


图 5-21. POWERHOLD Mode Timing Diagrams

5.4.5.2 AUTODEVON Mode

In this mode, at the end of the power-up sequence, the register bit DEV_CTRL.DEV_ON is automatically set to 1 and the TPS659037 device remains in its ACTIVE state until this bit is cleared by the host processor.

图 5-22 and 图 5-23 show the AUTODEVON mode timing diagrams.

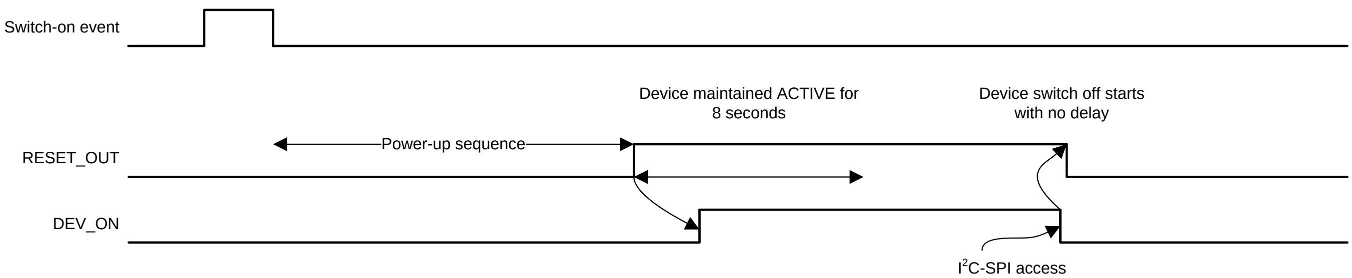


图 5-22. AUTODEVON Mode Timing Diagrams

The DEV_ON bit can also be configured so that it is not auto-updated (set to 1) at the end of the power-up sequence. In this case, the TPS659037 device behaves similarly to the POWERWHOLD mode, except the host has control over it using the DEV_CTRL.DEV_ON register bit instead of the POWERHOLD pin. Therefore, to keep the TPS659037 device active, the host must set and keep this bit at 1.

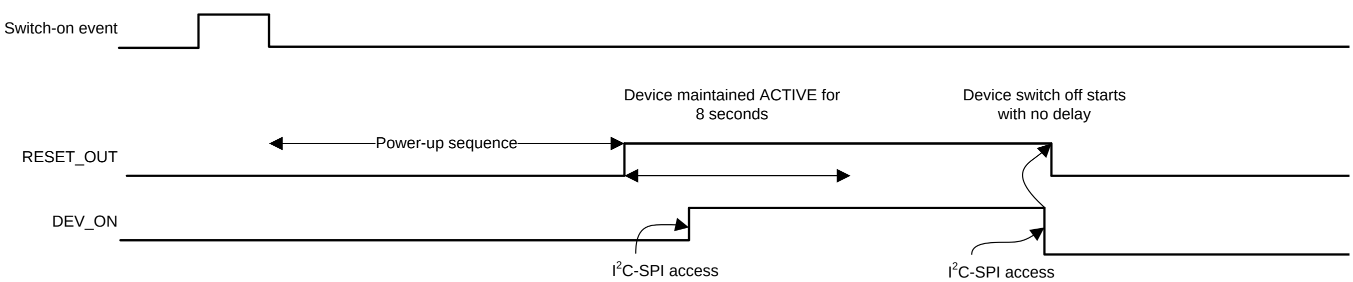


图 5-23. DEV_ON Mode Timing Diagrams

5.4.6 BOOT Configuration

All of the device resource settings are stored under the form of registers. Therefore, any platform-related settings are linked to an action altering these registers. This action can be a static update (register initialization value) or a dynamic update of the register (either from the user or from a power sequence).

Resources and platform settings are stored in nonvolatile memory (OTP):

- Static platform settings:
  – These settings define, for example, SMPS or LDO default voltages, GPIO functionality, and the device switch-on events. Part of the static platform settings can have two different values, and these values are selected with the BOOT0 pin. Static platform settings can be overwritten by a power sequence or by the user.
- Sequence platform settings:
  – These settings define the TPS659037 device power sequences between state transitions, for example, the OFF2ACT sequence when transitioning from OFF mode to ACTIVE mode. Each power sequence is composed of several register accesses that define which resources (and their corresponding registers) must be updated during the respective state transition. Three different sequences can be defined with the BOOT0 and BOOT1 pins. These settings can be overwritten by the user when the power sequence completes execution.

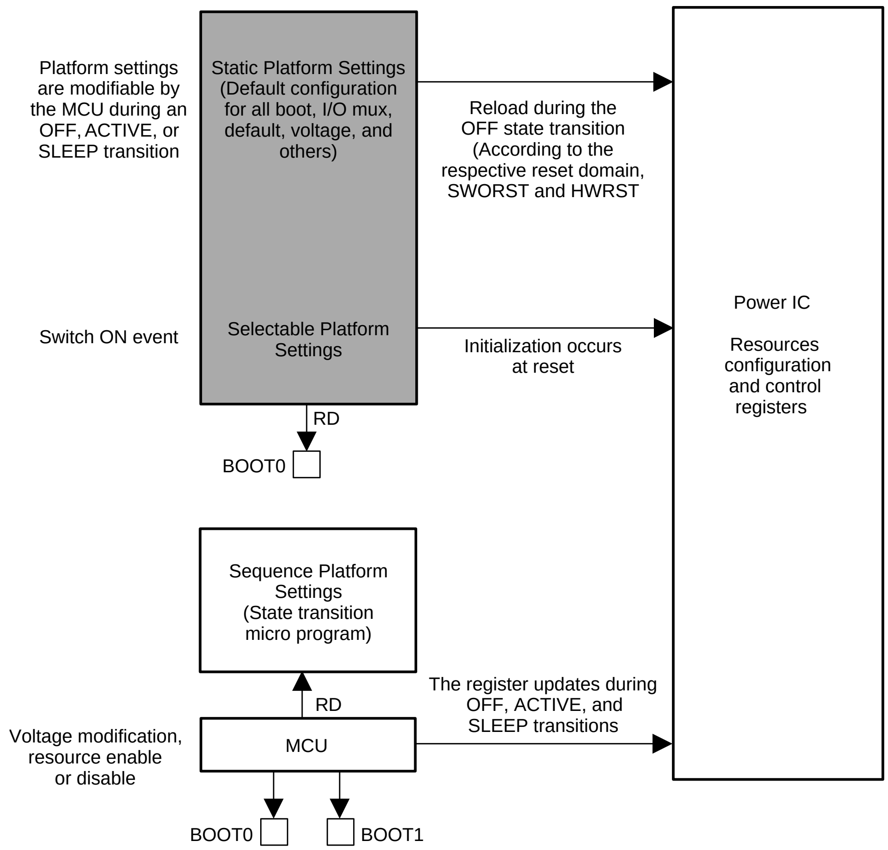


图 5-24. Boot Pin Control

5.4.6.1 Boot Pin Selection

表 5-14 lists the boot pins associated configurations.

注

Generally two of the three power sequence definitions are small modifications from the main sequence to the respective OTP memory size.

表 5-14. Boot Pin Associated Configurations

BOOT0	BOOT1	OTP CONFIGURATION	POWER SEQUENCE SELECTOR
0	0	Set_0	Sel_0
0	1	Set_0	Sel_1
1	0	Set_1	Sel_2
1	1	Set_1	Sel_2

The BOOT0 and BOOT1 pins must be grounded or pulled up, but the pins must not be unconnected (high impedance).

The BOOT0 pin is used to select between two different OTP sets (Set_0 and Set_1) of device configuration (referred to as selectable platform settings in 图 5-24). For list of OTP programmable parameters with programmed values refer to the Application Note of the relevant part number.

注

The respective VSEL[6:0] bit field in the SMPSn_VOLTAGE and SMPSn_FORCE registers is mapped on a same OTP memory location, meaning that they are loaded at reset with the same value and that the BOOT0 pin changes the setting for both of them.

The BOOT0 pin can also be used with the BOOT1 pin as static selectors during execution of the power sequence. This is intended to provide a possibility from within a static power sequence, to branch to different instructions. This allows choosing power sequences (or subpart of power sequences) based on BOOT pins without altering power sequences themselves in OTP.

5.4.7 Reset Levels

The TPS659037 device resource control registers are defined by three categories:

- POR registers
- HW (HARDWARE) registers
- SWO (SWITCHOFF) registers

These registers are associated to three levels of reset as described below:

- Power-on reset (POR)
  – Power-on reset happens when the TPS659037 device gets its supplies and transition from the NOSUPPLY state to the BACKUP state. This is the global device reset.
  – Additionally, SMPS_THERMAL_STATUS, SMPS_SHORT_STATUS, SMPS_POWERGOOD_MASK, LDO_SHORT_STATUS and SWOFF_STATUS registers are in POR domain. This list is indicative only.
- HWRST – Hardware reset
  – Hardware reset happens when any OFF request is configured to generate a hardware reset. This reset triggers a transition to the OFF state from either the ACTIVE or SLEEP state (execute either the ACT2OFF or SLP2OFF sequence).

- SWORST – Switch-off reset
  - Switch-off reset happens when any OFF request is configured to not generate a hardware reset. This reset acts as the HWRST, except only the SWO registers are reset. The device goes in the OFF state, from either ACTIVE or SLEEP, and therefore executes the ACT2OFF or SLP2OFF sequence.
  - Power resource control registers for SMPS and LDO voltage levels and operating mode control are in SWORST domain. Additionally some registers control the 32-kHz, REGENx and SYSENx, watchdog, external charger control, and VSYS_MON comparator. This list is indicative only.

表 5-15 lists the reset levels, and 图 5-25 shows the reset levels versus registers.

表 5-15. Reset Levels

LEVEL	RESET TAG	REGISTERS AFFECTED	COMMENT
0	POR	POR, HW, SWO	This reset level is the lowest level, for which all registers are reset.
1	HWRST	HW, SWO	During hardware reset (HWRST), all registers are reset except the POR registers.
2	SWORST	SWO	Only the SWO registers are reset.

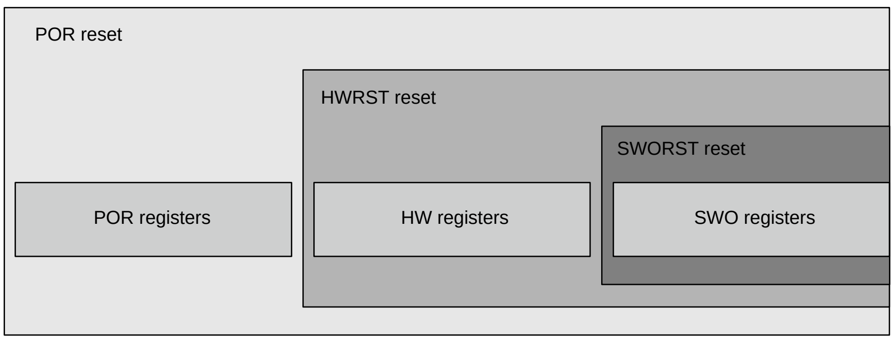


图 5-25. Reset Levels versus Registers

5.4.8 Warm Reset

The TPS659037 device can execute a warm reset. The main purpose of this reset is to recover the TPS659037 device from a locked or unknown state by reloading the default configuration. The warm reset is triggered by the NRESWARM pin. During a warm reset, the OFF2ACT sequence is executed regardless of the actual state (ACTIVE, SLEEP) and the TPS659037 device returns to or remains in the ACTIVE state. Resources that are not part of the OFF2ACT sequence are not impacted by warm reset and maintain the previous state. Resources that are part of power-up sequence go to ACTIVE mode and the output voltage level is reloaded from OTP or kept in the previous value depending on the WR_S bit in the SMPSx_CTRL register or the LDOx_STRL register.

5.4.9 RESET_IN

RESET_IN is a gating signal for on request and causes a switch-off event (Cold Reset or Shutdown). 表 5-11 shows that the RESET_IN behavior is programmable.

5.4.10 Watchdog Timer (WDT)

The watchdog timer has two modes of operation, periodic mode and interrupt mode.

In periodic mode, an interrupt is generated with a regular period *N* that is defined by the WATCHDOG.TIMER setting. This interrupt is generated at the beginning of the period (when the watchdog internal counter equals 1). The IC initiates a shutdown at the end of the period (when the internal counter has reached *N*) only if the interrupt has not been cleared within the defined time frame (0 to *N*). In this mode, when the interrupt is cleared, the internal counter is not reset. The counter continues to count until it reaches the maximum value (defined by the TIMER setting) and automatically rolls over to 0 in order to start a new counting period. Regardless of when the interrupt is cleared within a given period (*N*), the next interrupt is generated only when the ongoing period completes (reaches *N*). The internal watchdog counter is initialized and kept at 0 as long as the RESET_OUT pin is low. The counter begins counting as soon as the RESET_OUT pin is released.

In interrupt mode, any interrupt source resets the watchdog counter and begins the counting. If the sources of the interrupts are not cleared (INT line released) before the end of the predefined period *N* (set by WATCHDOG.TIMER setting) then the device initiates a shutdown. If the sources of the interrupts are cleared within the predefined period, then the watchdog counter is discarded (DC) and no shutdown sequence is initiated.

By default, the watchdog is disabled.

图 5-27 and 图 5-26 show the watchdog timings.

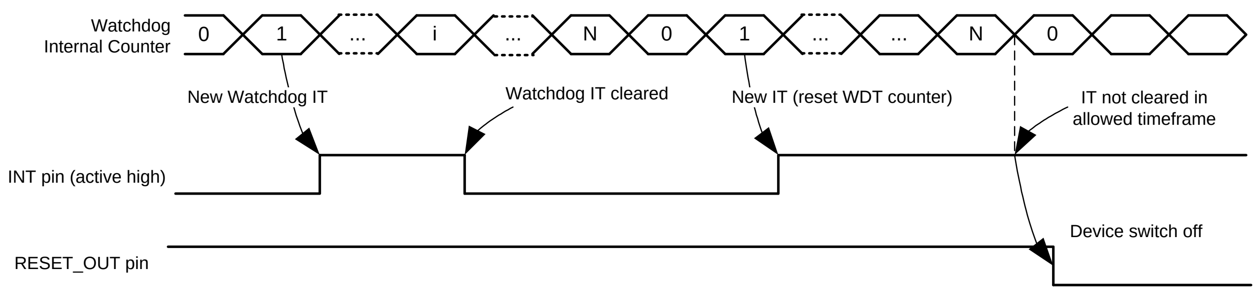


图 5-26. Watchdog Timing Diagrams—Periodic Mode

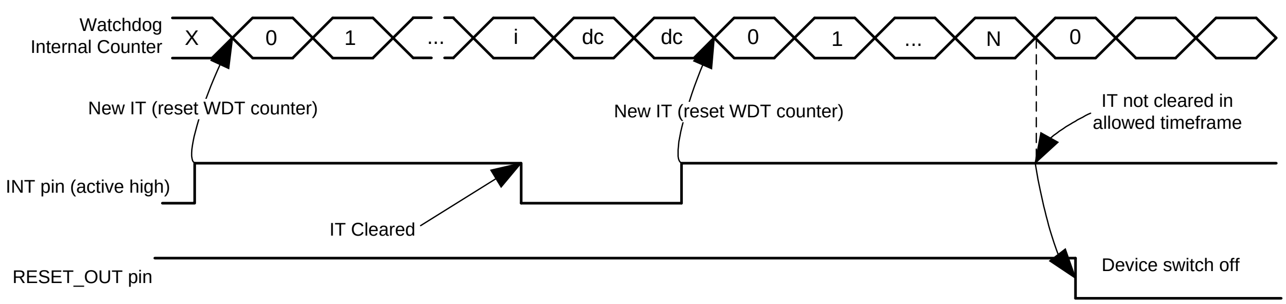


图 5-27. Watchdog Timing Diagrams—Interrupt Mode

5.4.11 System Voltage Monitoring

The power state-machine of the TPS659037 device is controlled by comparators monitoring the voltage on the VCC_SENSE and VCC1 pins. For electrical parameters see Section 4.14.

POR: When the supply at the VCC1 pin is below the POR threshold, the TPS659037 device is in the NO SUPPLY state. All functionality, including RTC, is off. When the voltage in VCC1 rises above the POR threshold, the device enters from the NO SUPPLY to the BACKUP state.

VSYS_LO: When the voltage on VCC1 pin rises above VSYS_LO, the TPS659037 device enters from the BACKUP state to the OFF state. When the device is in the ACTIVE, SLEEP, or OFF state and the voltage on VCC1 decreases below VSYS_LO, the device enters BACKUP mode. When the device transitions from the ACTIVE state to the BACKUP state, all active SMPS and LDO regulators, except LDOVRTC, are disabled simultaneously. When operating with a 16.384-MHz crystal, the regulators are immediately disabled after VCC1 becomes less than VSYS_LO. When operating without a crystal, a 180-µs deglitch time occurs after VCC1 becomes less than VSYS_LO and before the regulators are disabled. The VSYS_LO level is OTP programmable.

注

For silicon revision 1.3 or earlier, when operating without a crystal, transitioning from the ACTIVE state to the BACKUP state using VSYS_LO while the outputs are active must always be followed by a POR event to make sure the device is reset properly. See 节 5.3.10 to identify the silicon version in the device.

VSYS_MON: During power up, the VSYS_HI OTP value is used as a threshold for the VSYS_MON comparator which is gating the PMIC start-up (as a threshold for transition from OFF to ACTIVE state). The VSYS_MON comparator monitors the VCC_SENSE pin. After power up, software can configure the comparator threshold in the VSYS_MON register.

图 5-28 shows a block diagram of the system comparators.

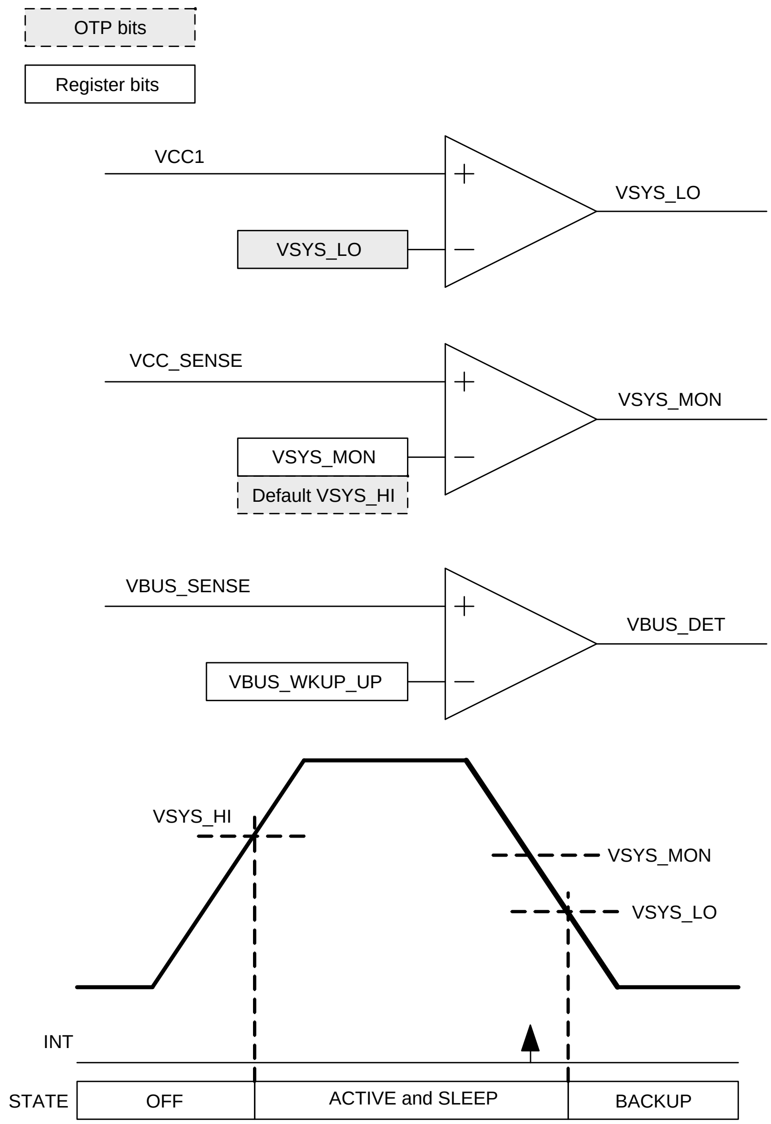


图 5-28. System Comparators

To use comparators in the system:

- The VSYS_LO and VSYS_HI thresholds are defined in the OTP. Software cannot change these levels.

- After start-up, the VSYS_MON comparator is automatically disabled. Software can select a new threshold level using the VSYS_MON register and enable the comparator.
- In order for the same coding on the rising and falling edge, the VSYS_MON comparator does not include hysteresis and therefore can generate multiple interrupts when the voltage level is at the threshold level. New interrupt generation has a 125-µs debounce time which allows the software to mask the interrupt and update the threshold level or disable the comparator before receiving a new interrupt.

图 5-29 shows additional details on the VSYS_MON comparator. When the VSYS_MON comparator is enabled, and the internal buffer is bypassed, input impedance at the VCC_SENSE pin is 500 kΩ (typical). When the comparators are disabled, the VCC_SENSE pin is at high impedance mode. If GPADC is enabled to measure channel 6 or channel 7, 40 kΩ is added in parallel to the corresponding comparator. See 表 5-3 for the GPADC input range.

To enable system voltage sensing above 5.25 V, an external resistive divider can be used. Internal buffers are enabled by setting OTP bit HIGH_VCC_SENSE = 1 to provide high impedance for the external resistive dividers. The maximum input level for the internal buffer is VCC1 – 1 V.

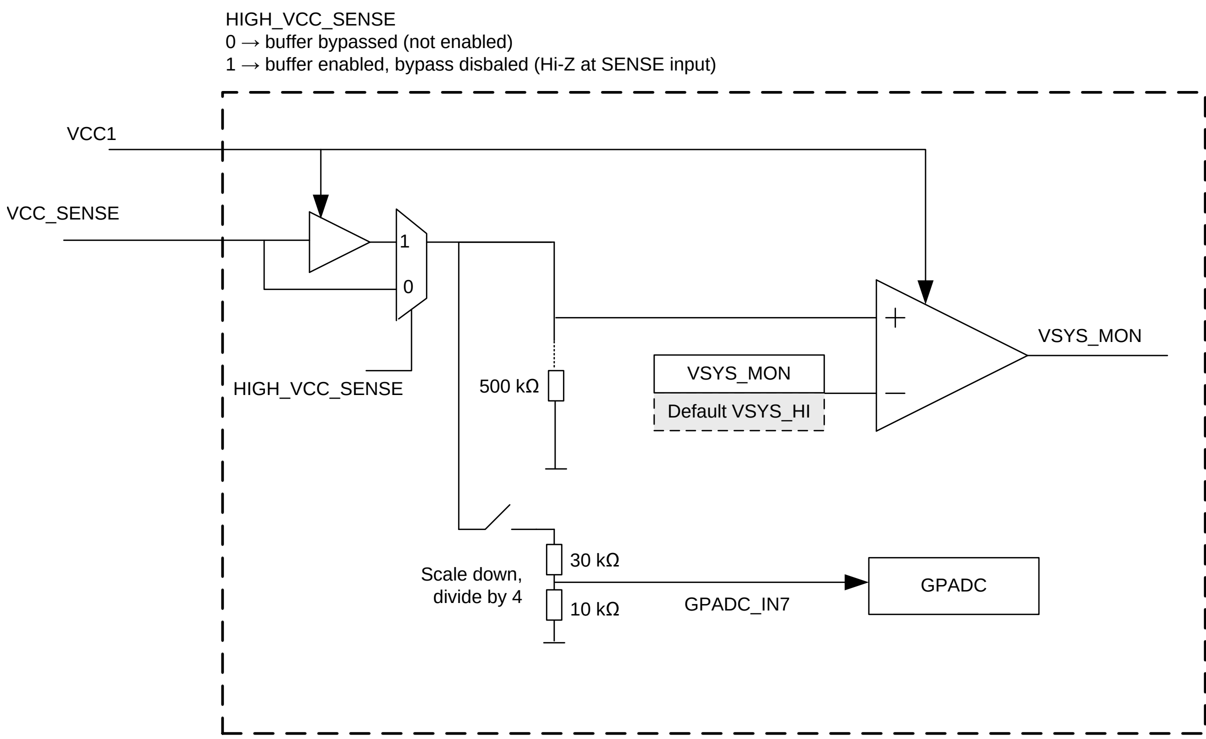


图 5-29. VSYS_MON Comparator Details

5.4.11.1 Generating a POR

注

This section applies to silicon revisions 1.3 or earlier. Newer silicon revisions do not have this requirement because the V_{CC} is continuously sampled. See 节 5.3.10 to identify the silicon version in the device.

To generate a POR from a falling V_{CC}, V_{CC} is sampled every 1 ms and compared to the POR threshold.In case V_{CC} is discharged and resupplied quickly, a POR may not be reliably generated if V_{CC} crosses the POR threshold between samples. Another way to generate POR is to discharge the LDOVRTC regulator to 0 V after V_{CC} is removed. With no external load, this could take 3 s for the LDOVRTC output to discharge to 0 V. The PMIC should not be restarted after V_{CC} is removed but before LDOVRTC is discharged to 0 V. If necessary, TI recommends to add a pulldown resistor from the LDOVRTC output to GND with a minimum of 3.9 kΩ to speed up the LDOVRTC discharge time. For more details, refer to the *POR Generation in TPS65903x and TPS6591x Devices* application report.

The value of the pulldown resistor should be chosen based on the desired discharge time and acceptable current draw in the OFF state, but no greater than 0.5 mA. Use 公式 8 to calculate the pulldown resistor based on the desired discharge time.

$$R_{PD}\ (k\Omega) = t_{discharge}\ (ms) / [C_O\ (\mu F) \times 3]$$

where

- $t_{discharge}$ = discharge time of the VRTC output
- R_{PD} = pulldown resistance from the VRTC output to GND
- C_O = output capacitance on the VRTC line (typically 2.2 µF) (8)

Because LDOVRTC is always on when V_{CC} is supplied, additional current is drawn through the pulldown resistor. The output current of LDOVRTC while the PMIC is in OFF state should not exceed 0.5 mA. Use 公式 9 to calculate the pulldown current.

$$I_{PD} = 1.8\ V / R_{PD}$$

where

- I_{PD} = current through the pulldown resistor
- R_{PD} = pulldown resistance from the VRTC regulator (9)

6 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

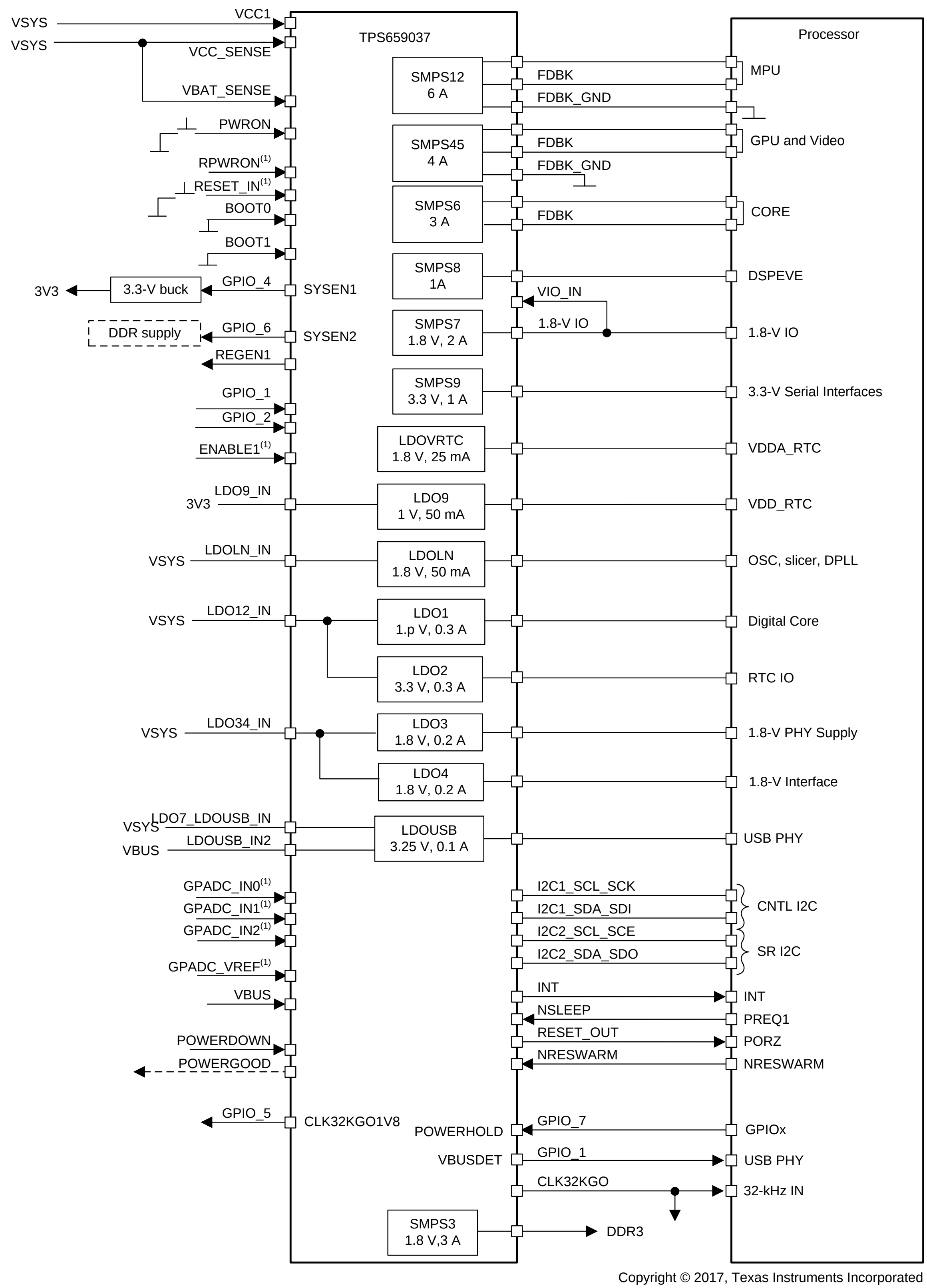
The TPS659037 device is integrated power management integrated circuits (PMIC), both available in a 169-pin, 0.8-mm pitch, 12-mm × 12-mm nFBGA package. It has seven configurable step-down converter rails, with the ability to combine power rails and supply up to 9 A of output current in multi-phase mode. The TPS659037 device also has seven LDOs. The device has a 12-bit GPADC with three external channels, eight configurable GPIOs, two I^2C interface channels or one SPI channel, a real-time clock module with calendar function, a PLL for external clock sync and phase delay capability, and a programmable power sequencer and control for supporting different processors and applications.

As the TPS659037 device is highly integrated PMIC device, users must take necessary actions to ensure the PMIC is operating under the recommended operating conditions to ensure desired performance from the device. Additional cooling strategies may be necessary to maintain the junction temperature below maximum limit allowed for the device. To minimize the interferences when turning on a power rail while the device is in operation, optimal PCB layout and grounding strategy are essential and are recommended in 节 8. In addition, users can take steps such as turning on additional rails only when the systems is operating in light load condition.

The following sections provides the typical application use case with the recommended external components and layout guidelines. For application design guidance and cross checks, refer to the *TPS659037 Design Guide* and the *TPS659037 Design Checklist*.

6.2 Typical Application

Following the typical application schematic and the list of recommended external components will allow the TPS659037 device to achieve accurate and stable regulation with its SMPS and LDO outputs. These power sources are internally compensated and have been designed to operate most effectively with the component values listed in 表 6-2. Deviating from these values is possible but is highly discouraged.



(1) Input can be left floating if not used.

(2) Processor connections are OTP dependent. For OTP-specific connections, refer to the *TPS659037 User's Guide to Power AM572x and AM571x*.

图 6-1. Application Schematic

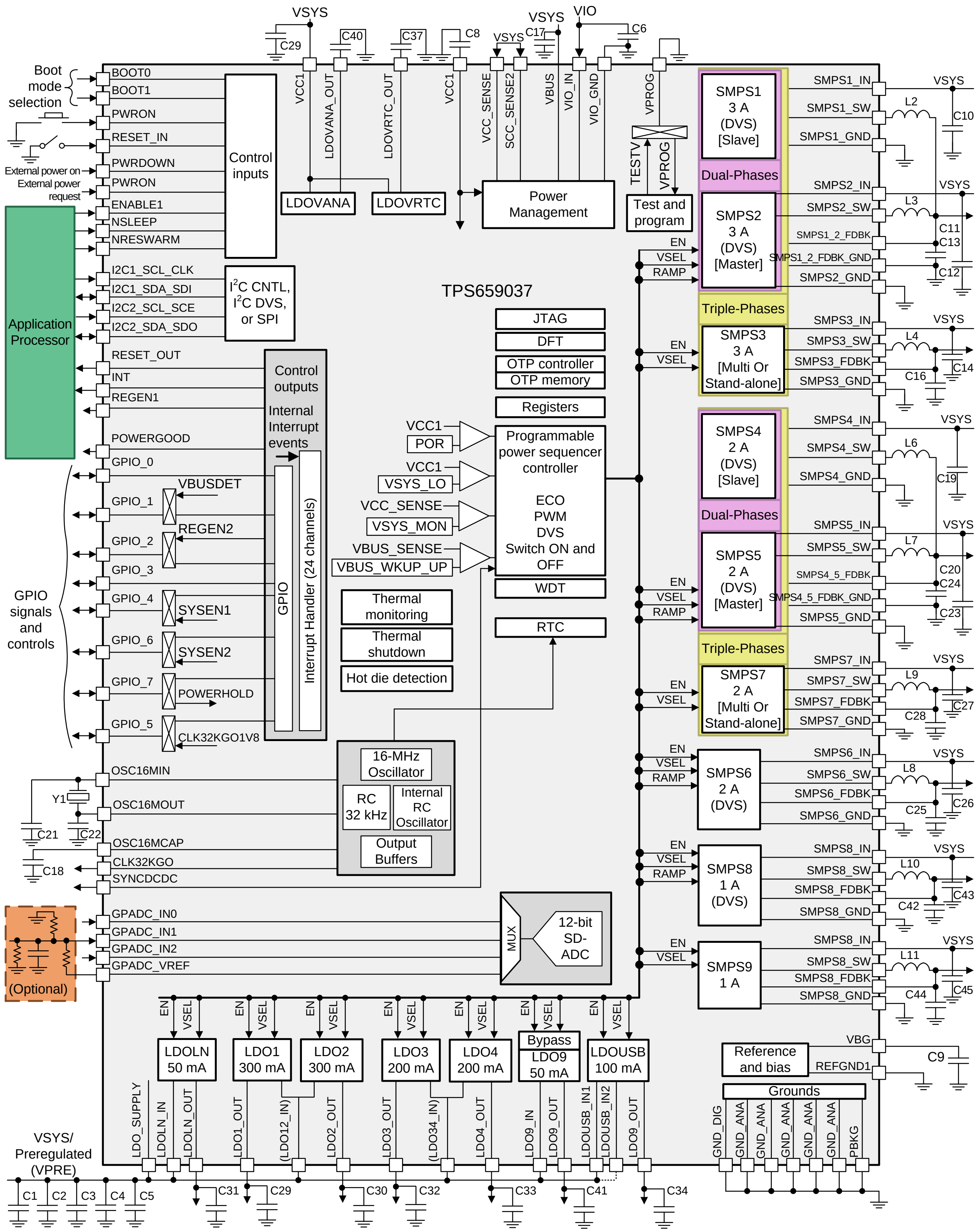


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图 6-2. Typical Application Schematic

6.2.1 Design Requirements

For this design example, use the parameters listed in 表 6-1.

表 6-1. Design Parameters

DESIGN PARAMETER	TPS6590378ZWSR	TPS6590379ZWSR
Supply voltage	3.3 V to 5 V	3.8 V to 5 V
Switching frequency	2.2 MHz	2.2 MHz
SMPS12 voltage	1.15 V	1.15 V
SMPS12 current	6 A	6 A
SMPS3 voltage	1.35 V or 1.5 V	1.35 V or 1.5 V
SMPS3 current	3 A	3 A
SMPS45 voltage	1.06 V	1.06 V
SMPS45 current	4 A	4 A
SMPS6 voltage	1.15 V	1.06 V
SMPS6 current	3 A	3 A
SMPS7 voltage	0.7 V to 3.3 V	1.15 V
SMPS7 current	2 A	2 A
SMPS8 voltage	1.06 V	1.06 V
SMPS8 current	1 A	1 A
SMPS9 voltage	0.7 V to 3.3 V	3.3 V
SMPS9 current	1 A	1 A
LDO1 voltage	3.3 V	3.3 V
LDO1 current	300 mA	300 mA
LDO2 voltage	3.3 V	1.8 V
LDO2 current	300 mA	300 mA
LDO3 voltage	1.8 V	1.8 V
LDO3 current	200 mA	200 mA
LDO4 voltage	1.8 V	1.8 V
LDO4 current	200 mA	200 mA
LDO9 voltage	1.05 V	1.05 V
LDO9 current	50 mA	50 mA
LDOLN voltage	1.8 V	1.8 V
LDOLN current	50 mA	50 mA
LDOUSB voltage	3.3 V	3.3 V
LDOUSB current	100 mA	100 mA

6.2.2 Detailed Design Procedure

6.2.2.1 Recommended External Components

表 6-2. Recommended External Components for Commercial Usage

REFERENCE COMPONENTS	COMPONENT(1)	MANUFACTURER	PART NUMBER	VALUE	EIA SIZE CODE	SIZE (mm)
INPUT POWER SUPPLIES EXTERNAL COMPONENTS						
C7, C8	VSYS (VCC1) tank capacitor(2)	Murata	GRM188R60J106ME84	10 µF, 6V3	0603	1.6 × 0.8 × 0.8
C6	Decoupling capacitor	Murata	GRM155R61C104KA88	100 nF, 6V3	0402	1 × 0.5 × 0.5
CRYSTAL OSCILLATOR EXTERNAL COMPONENTS						
Y1	Crystal	Epson	FA-238	16.384 MHz	-	3.2 × 2.5 × 0.6
		TXC	7V-16.384MAAE-T	16.384 MHz	-	3.2 × 2.5 × 0.8
C21, C22	Crystal decoupling	Murata	GRM1555C1H100JA01	10 pF, 50V	0402	1 × 0.5 × 0.5
C18	Crystal supply decoupling	Murata	GRM155R60J225ME15	2.2 µF, 6V3	0402	1 × 0.5 × 0.5
		TDK	C1005X5R0J225M	2.2 µF, 6V3	0402	1 × 0.5 × 0.5
BANDGAP EXTERNAL COMPONENTS						
C9	Capacitor	Murata	GRM155R61C104KA88	100 nF, 6V3	0402	1 × 0.5 × 0.5
SMPS EXTERNAL COMPONENTS						
C10, C12, C14, C19, C23, C26, C27, C43, C45	Input capacitor	Murata	GRM155R60J475ME47	4.7 µF, 6V3	0402	1 × 0.5 × 0.5
C11, C13, C16, C20, C24, C25, C28, C42, C44	Output Capacitance for all SMPS	Murata	GRM21BR60J476ME15	47 µF, 6V3	0805	2 × 1.25 × 1.25
L2, L3, L4, L6, L7, L8, L9, L10, L11	Inductor (BUCK)	TOKO	DFE252010C-1RON	1 µH	2520	2.5 × 2 × 1
		Vishay	IHLP1616ABER1R0M11	1 µH		4 × 4.4 × 1.2
LDO EXTERNAL COMPONENTS						
C1, C2, C3, C4, C5	Input capacitor	Murata	GRM155R60J225ME15	2.2 µF, 6V3	0402	1 × 0.5 × 0.5
		TDK	C1005X5R0J225M	2.2 µF, 6V3	0402	1 × 0.5 × 0.5
C29, C30, C31, C32, C33, C34, C37, C40, C41	Output capacitor	Murata	GRM155R60J225ME15	2.2 µF, 6V3	0402	1 × 0.5 × 0.5
		TDK	C1005X5R0J225M	2.2 µF, 6V3	0402	1 × 0.5 × 0.5
VBUS EXTERNAL COMPONENTS						
C17	VBUS decoupling capacitor	Murata	GRM188R71C104KA01	100 nF 16 V	0603	1.6 × 0.8 × 0.8
		Murata	GRM155R61C104KA88	100 nF 16 V	0402	1 × 0.5 × 0.5

(1) Component minimum and maximum tolerance values are specified in the electrical parameters section of each IP.
(2) The tank capacitors filter the VSYS/VCC1 input voltage of the LDO and SMPS core architectures.

6.2.2.2 SMPS Input Capacitors

All SMPS inputs require an input decoupling capacitor to minimize input ripple voltage. TI recommends using a 10-V, 4.7-µF capacitor for each SMPS. Depending on the input voltage of the SMPS, a 6.3-V or 10-V capacitor can be used. See 表 6-2 for the specific part number of the input capacitor that is recommended.

For optimal performance, the input capacitors should be placed as close to the SMPS input pins as possible. See 节 8.1 for more information about component placement.

6.2.2.3 SMPS Output Capacitors

All SMPS outputs require an output capacitor to hold up the output voltage during a load step or changes to the input voltage. To ensure stability across the entire switching frequency range, the TPS659037 device requires an output capacitance value between 33 µF and 57 µF. To meet this requirement across temperature and DC bias voltage, TI recommends using a 47-µF capacitor for each SMPS. It is important to remember that each SMPS requires an output capacitor, not just each output rail. For example, SMPS12 is a dual phase regulator and an output capacitor is required for the SMPS1 output and the SMPS2 output. Note, this requirement excludes any capacitance seen at the load and only refers to the capacitance seen close to the device. Additional capacitance placed near the load can be supported, but the end application or system should be evaluated for stability. See 表 6-2 for the specific part number of the recommended output capacitor.

6.2.2.4 SMPS Inductors

Again, to ensure stability across the entire switching frequency range, TI recommends using a 1-µH inductor on each SMPS. It is important to remember that each SMPS requires an inductor, not just each output rail. For example, SMPS12 is a dual phase regulator and an inductor is required for the SMPS1_SW pins and the SMPS2_SW pins. See 表 6-2 for the specific part number of the recommended inductor.

6.2.2.5 LDO Input Capacitors

All LDO inputs require an input decoupling capacitor to minimize input ripple voltage. TI recommends using a 2.2-µF capacitor for each LDO. Depending on the input voltage of the LDO, a 6.3-V or 10-V capacitor can be used. See 表 6-2 for the specific part number of the input capacitor that is recommended.

For optimal performance, the input capacitors should be placed as close to the LDO input pins as possible. See 节 8.1 for more information about component placement.

6.2.2.6 LDO Output Capacitors

All LDO outputs need an output capacitor to hold up the output voltage during a load step or changes to the input voltage. Using a 2.2-µF capacitor for each LDO output is recommended. Note, this requirement excludes any capacitance seen at the load and only refers to the capacitance seen close to the device. Additional capacitance placed near the load can be supported, but the end application or system should be evaluated for stability. See 表 6-2 for the specific part number of the recommended output capacitor.

6.2.2.7 VCC1

VCC1 is the supply for the analog input voltage of the device. This pin requires a 10-µF decoupling capacitor.

Texas Instruments recommends to always power down the TPS659037 before removing power from VCC1. If the input voltage to the device is removed while the device is ACTIVE, the device will shut off when VCC1 reaches the VSYS_LO threshold. As mentioned in the 节 5.4.11 section, once VCC1 reaches VSYS_LO, there is about 180 us delay before all the output rails are disabled simultaneously.

There are two scenarios to consider in the system-level design in the event of unexpected loss of power.

6.2.2.7.1 Meeting the Power Down Sequence

To prevent a sequencing violation, it is important to block reverse current and implement a disable signal to the PMIC. A Schottky diode can block reverse current when the input is removed. Additionally, capacitors can help maintain the input voltage level while the power-down sequence occurs. Depending on the system design, there are a couple ways to implement a disable signal.

For a system where the TPS659037 is powered by the system input voltage, a supervisor can be used to create a logic signal, indicating if the power is at a good level. An example of this solution is shown in 图 6-3.

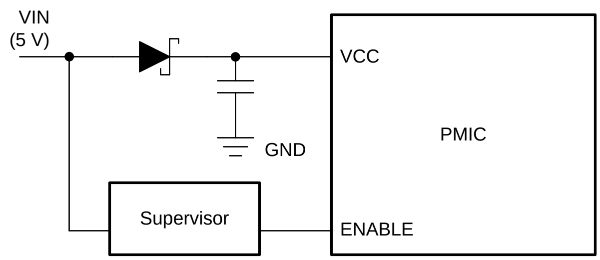


图 6-3. Supporting Uncontrolled Power Down When the PMIC is Supplied by the System Input Voltage

An alternative solution is possible when a pre-regulator is present. In the case of the pre-regulator, the pre-regulator output capacitance can also act as the energy storage to maintain VCC1 for the necessary time. The total supply capacitance should be calculated to support the worst-case leakage current during power down so that the voltage is maintained until the power-down sequence completes. 图 6-4 shows an example of this configuration.

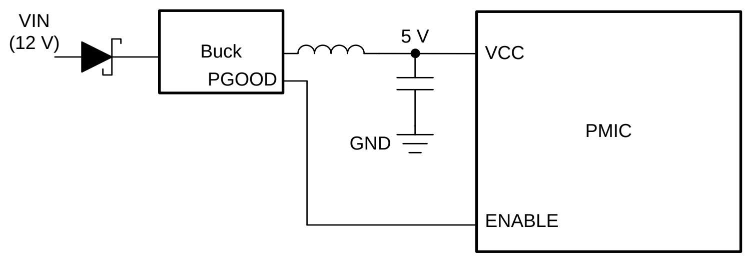


图 6-4. Supporting Uncontrolled Power Down when the PMIC is Supplied by a Preregulator

To determine the capacitance needed at the output of the pre-regulator, use 公式 10. This equation is used to ensure that the power down sequence is complete before the device is disabled.

$$C = I \times \Delta T / (VCC1 - VSYS\_LO) \tag{10}$$

where

- C is total capacitance on VCC1, including pre-regulator output capacitance and PMIC input capacitance
- I is the total current on the PMIC input supply
- ΔT is the time it takes the power-down sequence to complete
- VCC1 is the voltage at the VCC1 pin
- VSYS_LO is the threshold where the device is disabled

6.2.2.7.2 Maintaining Sufficient Input Voltage

In the event of high loading during loss of input voltage, there is a risk to go below the voltage level necessary for the internal logic of the device to work properly before the device is disabled. This means that when the VCC1 voltage supply level becomes lower than the VSYS_LO threshold, the input voltage may continue dropping to very low voltages during the 180 us ±10% delay before the device is disabled.

If a large input voltage drop occurs before the device is disabled, the internal logic can no longer properly drive the FETs of the SMPS, and it is possible that the high-side FET and low-side FET of the SMPS are on at the same time. In the event that the high-side and low-side FETs for an SMPS are on at the same time, there is a direct path from SMPSx_IN to SMPSx_GND, allowing cross-conduction and possible damage of the device.

In order to prevent damage or irregular switching behavior, it is important that the voltage at the SMPSx_IN pin stays above 1.8 V, including negative transients, before the device is disabled. The minimum voltage seen at the SMPSx_IN pin is dependent on VCC1 and the PCB inductance between the SMPSx_IN pin and the input capacitor. Use 公式 11 to determine the minimum capacitance needed on VCC1 to ensure that the device continues switching properly before it is disabled.

$$C = I \times \Delta T / (VSYS\_LO - VCC1_{MIN})$$

where

- C is total capacitance on VCC1, including pre-regulator output capacitance and PMIC input capacitance
- I is the total current on the PMIC input supply
- ΔT is the maximum debounce time after VCC1 = VSYS_LO before the device switches off (198us)
- VSYS_LO is the threshold where the device is disabled
- $VCC1_{MIN}$ is the minimum VCC1 voltage to keep the SMPSx_IN transients above 1.8 V (11)

When measuring the SMPSx_IN and VCC1 during power down, use active differential probes and a high resolution oscilloscope (4GS/sec or more). VCC1 can be measured over the 10uF input capacitor. However, SMPSx_IN must be measured at the pin in order to measure the transients on this rail accurately. To measure SMPSx_IN, place the negative lead of the differential probe at a nearby GND, such as the GND of the SMPSx_IN input capacitor. Place the positive lead of the differential probe as close as possible to the SMPSx_IN pin. With this set up, verify that SMPSx_IN, including the ripple on this signal, does not drop below 1.8V before the SMPS stops switching. See 图 6-5 for an example of how to take this measurement. For ways to decrease the amplitude of the transient spikes, see 表 8-1 for recommended parasitic inductance requirements.

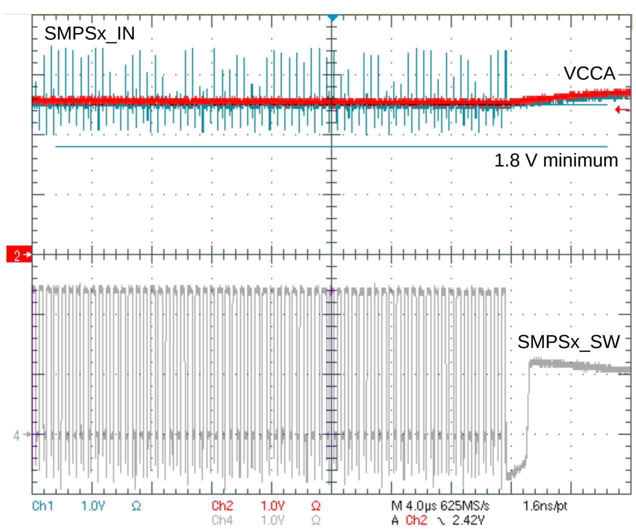


图 6-5. Waveform of SMPSx_IN Transients

6.2.2.8 VIO_IN

VIO_IN is the supply for the digital circuits inside the TPS659037 device. This pin requires a 0.1-µF decoupling capacitor.

6.2.2.9 16-MHz Crystal

The TPS659037 device has the ability to accept a 16-MHz crystal input. Providing the 16-MHz crystal input to the device allows the output of a stable and accurate 32-kHz clock to be used by the applications processor. The crystal input is divided down by 500 internally to produce the 32-kHz output clock. The crystal should be connected to the TPS659037 device as shown in 图 6-6.

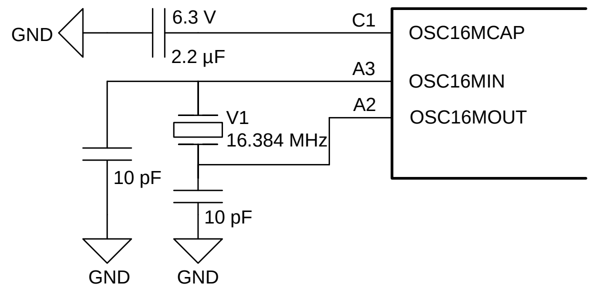


图 6-6. Crystal Input Configuration

As shown in 图 6-6, the OSC16MCAP pin requires a 2.2-µF 6.3-V filtering capacitor near the pin. Also, the crystal requires between 9 pF and 11 pF of load capacitance on both pins. To meet this requirement, using two 10-pF capacitors is recommended. See 表 6-2 for the specific load capacitors that are recommended.

The 16-MHz crystal is not required for operation of the TPS659037 device. The OSC16M_CFG OTP bit can be set to disable the 16MHz crystal completely, and enable one of the following two alternative options for system clock generation:

- A 32-kHz square wave can be supplied to the OSC16MIN pin. This option is typically used in applications where the processor requires an accurate system clock and there is one already available in the system. In that case, the available 32-kHz clock can be provided to the PMIC and added to the boot sequence as an output. In this configuration, the OSC16MOUT and OSC16MCAP pins can be left floating, and the internal 16-MHz oscillator is bypassed. Bypassing the 16-MHz oscillator results in a lower quiescent current.
- If the application does not require an accurate system clock for the processor, then providing one to the PMIC is not required. This option produces a lower quiescent current as seen in Section 4. In this configuration, the OSC16MIN pin should be grounded, while the OSC16MOUT and OSCMCAP pins can be left floating. Lastly, the GATE_RESET_OUT OTP bit should be used to allow the TPS659037 device to power up without the presence of the 16.384-MHz crystal nor the 32-kHz clock input.

Please note that if the OSC16M_CFG OTP bit is set to 0, a 16-MHz crystal must be present for the proper operation of the device.

6.2.2.10 GPADC

Instructions on how to perform a software conversion with the GPADC:

1. Enable software conversion mode – GPADC_SW_SELECT.SW_CONV_EN
2. Select the channel to convert – GPADC_SW_SELECT.SW_CONV0_SEL
   – For channel 0, set up the current source in the GPADC_CTRL1 register if needed.
3. For minimum latency, the GPADC can be set to always on (instead of default enabled from conversion request) by GPADC_CTRL1.GPADC_FORCE.
4. Unmask software conversion interrupt – INT3_MASK.GPADC_EOC_SW
5. Start conversion – GPADC_SW_SELECT.SW_START_CONV0.
6. An interrupt is generated at the end of the conversion INT3_STATUS.GPADC_EOC_SW.
7. Read conversion result – GPADC_SW_CONV0_MSB and GPADC_SW_CONV0_LSB
8. Expected result = dec(GPADC_SW_CONV0_MSB[3:0].GPADC_SW_CONV0_LSB[7:0])/ 4096 × 1.25

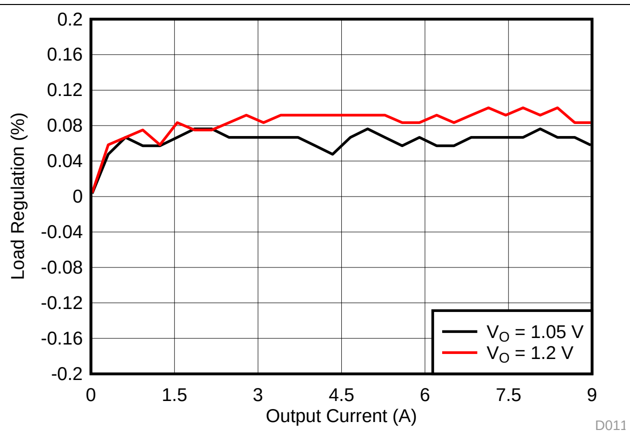
× scalar

Instructions on how to perform an auto conversion with the GPADC:

1. Select the channel to convert – GPADC_AUTO_SELECT.AUTO_CONV0_SEL
2. Configure auto conversion frequency – GPADC_AUTO_CTRL.COUNTER_CONV
3. Set the threshold level for comparison – GPADC_THRESH_CONV0_MSB.THRESH_CONV0_MSB, GPADC_THRESH_CONV0_LSB.THRESH_CONV0_LSB
   – Level = expected voltage threshold / (1.25 × scalar) × 4096 (in hexadecimal)
4. Set if the interrupt is triggered when conversion is above or below threshold – GPADC_THRESH_CONV0_MSB.THRESH_CONV0_POL
5. Triggering the threshold level can also be programmed to generate shutdown – GPADC_AUTO_CTRL.SHUTDOWN_CONV0
6. Unmask AUTO_CONV_0 interrupt – INT3_MASK.GPADC_AUTO_0
7. Enable AUTO CONV0 – GPADC_AUTO_CTRL.AUTO_CONV0_EN
8. When selected channel crosses programmed threshold, interrupt is generated – INT3_STATUS.GPADC_AUTO_0
9. Conversion results are available – GPADC_AUTO_CONV0_MSB, GPADC_AUTO_CONV0_LSB
10. If shutdown was enabled, chip switches off after SWOFF_DLY, unless interrupt is cleared

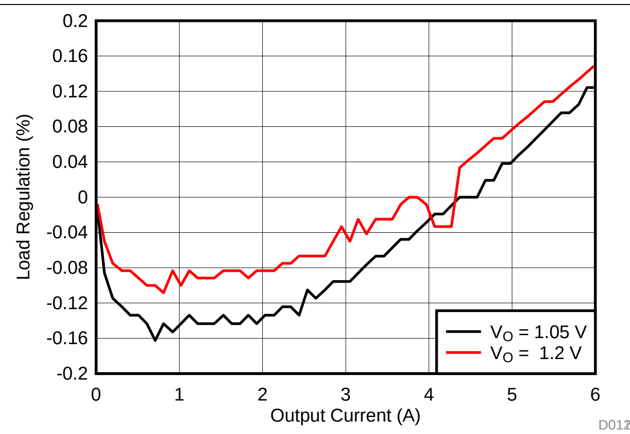
The example above is for CONV0; a similar procedure applies to CONV1.

6.2.3 Application Curves



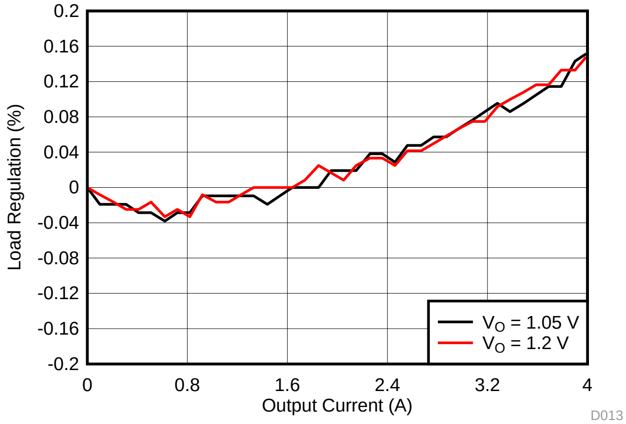
V_I = 3.8 V f_{SW} = 2.2 MHz

图 6-7. SMPS Load Regulation for 9-A Triple Phase



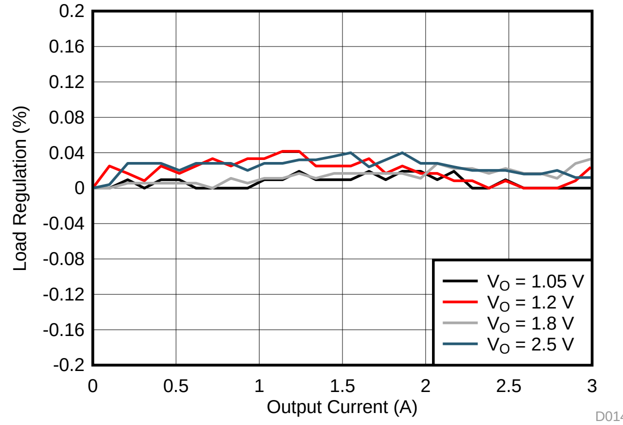
V_I = 3.8 V f_{SW} = 2.2 MHz

图 6-8. SMPS Load Regulation for 6-A Dual Phase



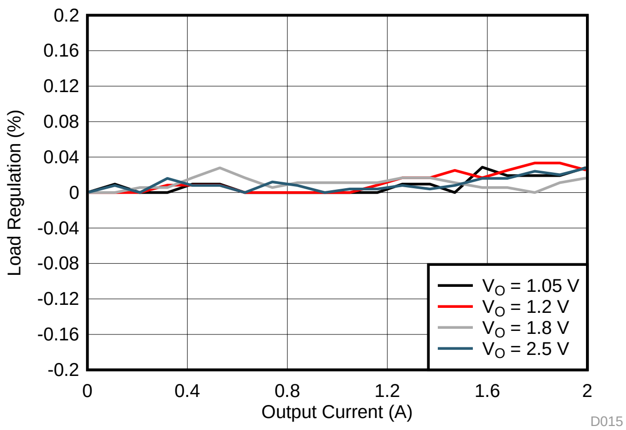
V_I = 3.8 V f_{SW} = 2.2 MHz

图 6-9. SMPS Load Regulation for 4-A Dual Phase



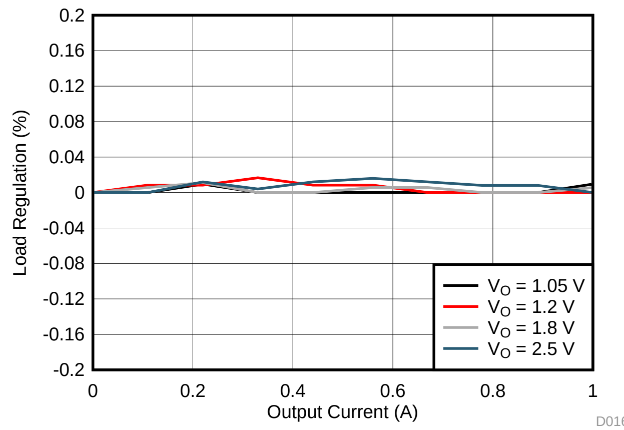
V_I = 3.8 V f_{SW} = 2.2 MHz

图 6-10. SMPS Load Regulation for 3-A Single Phase



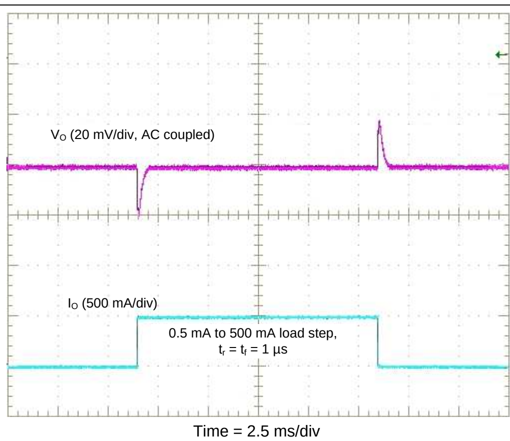
V_I = 3.8 V f_{SW} = 2.2 MHz

图 6-11. SMPS Regulation for 2-A Single Phase



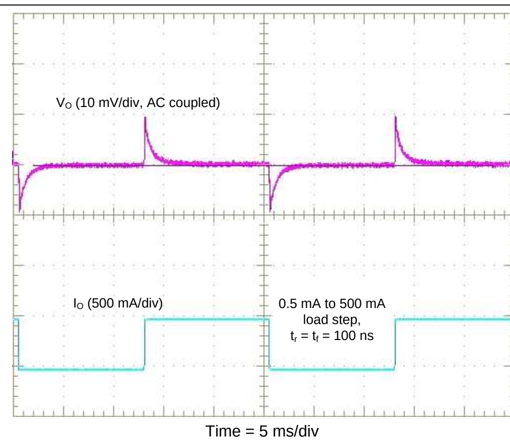
V_I = 3.8 V f_{SW} = 2.2 MHz

图 6-12. SMPS Load Regulation for 1-A Single Phase



V_I = 3.5 V V_O = 1.05 V f_{SW} = 2.2 Hz

图 6-13. Typical SMPS Load Transient Response for SMPS8 and SMPS9



V_I = 3.5 V V_O = 1.05 V f_{SW} = 2.2 Hz

图 6-14. Typical SMPS Load Transient Response for SMPS12, SMPS3, SMPS45, SMPS6, and SMPS7

7 Power Supply Recommendations

The TPS659037 device is designed to work with an analog supply voltage range of 3.135 V to 5.25 V. The input supply should be well regulated and connected to the VCC1 pin, as well as SMPS and LDO input pins with appropriate bypass capacitors as recommended in 图 6-1. If the input supply is located more than a few inches from the TPS659037 device, additional capacitance may be required in addition to the recommended input capacitors at the VCC1 pin and the SMPS and LDO input pins.

8 Layout

8.1 Layout Guidelines

As in every switch-mode-supply design, the following general layout rules apply:

- Use a solid ground-plane for power-ground (PGND)
- Use an independent ground for Logic, LDOs and Analog (AGND)
- Connect those Grounds at a star-point ideally underneath the device.
- Place input capacitors as close as possible to the input-pins of the device. This is paramount and more important than the output-loop!
- Place the inductor and output capacitor as close as possible to the phase node (or switch-node) of the device.
- Keep the loop-area formed by Phase-node, Inductor, output-capacitor and PGND as small as possible.
- For traces and vias on power-lines, keep inductance and resistance as small as possible by using wide traces, avoid switching layers but if needed, use plenty of vias.

The goal of the previously listed guidelines is a layout that minimizes emissions, maximizes EMI-immunity, and maintains a safe operating area for the device.

To minimize the spiking at the phase-node for both, high-side (VIN – SWx) as well as low-side (SWx – PGND), the decoupling of VIN is paramount. Appropriate decoupling and thorough layout should ensure that the spikes never exceed 7V across the high-side and low-side FETs.

TI recommends the guidelines shown in 图 8-1 regarding parasitic inductance and resistance.

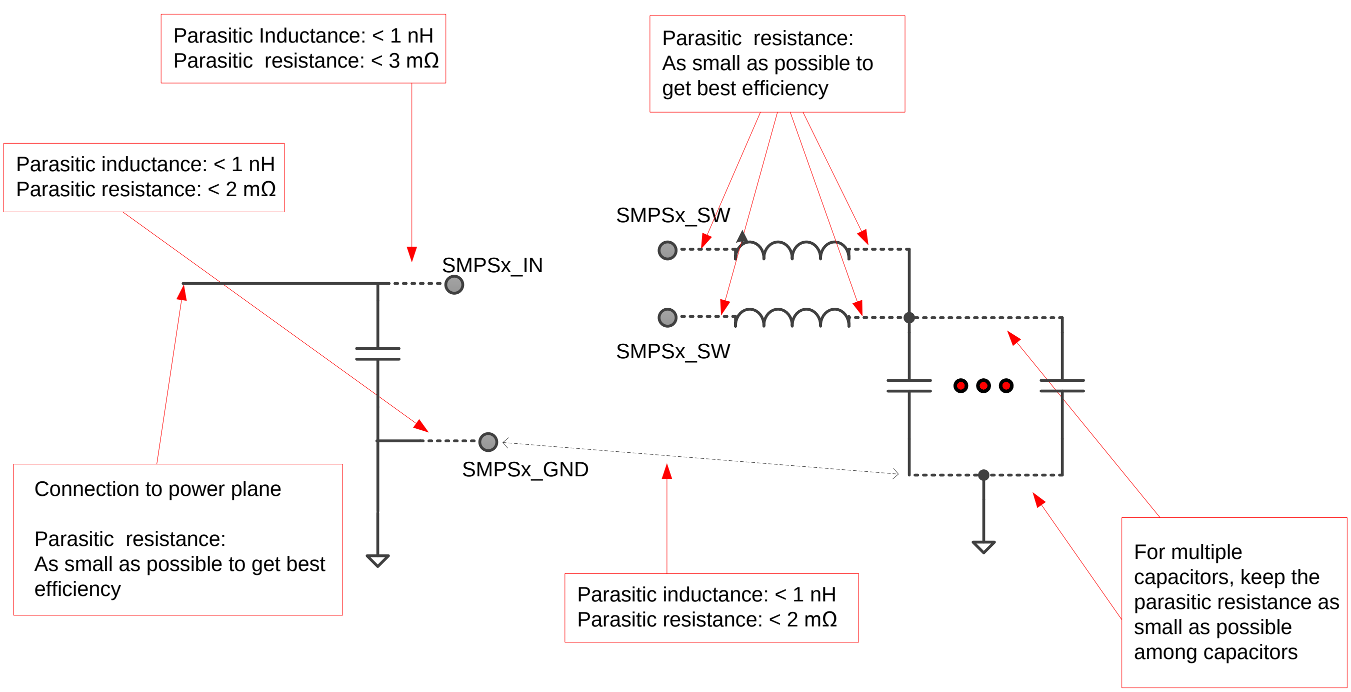


图 8-1. Parasitic Inductance and Resistance

表 8-1 lists the maximum allowable parasitic (inductance measured at 100 MHz) and the achievable values in an optimized layout.

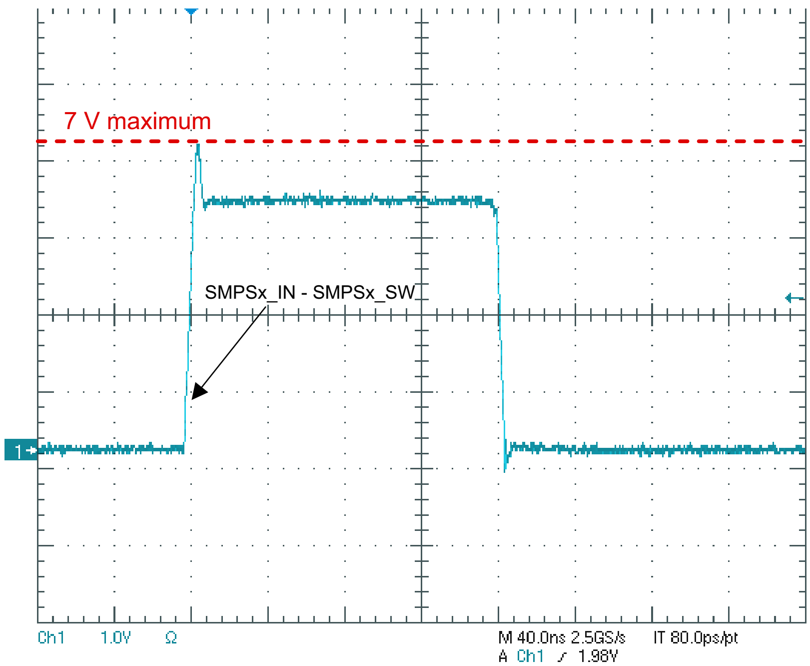
表 8-1. Maximum Allowable Parasitic

CONNECTION	MAXIMUM ALLOWABLE INDUCTANCE	MAXIMUM ALLOWABLE RESISTANCE	OPTIMIZED LAYOUT (EVM) INDUCTANCE		OPTIMIZED LAYOUT (EVM) RESISTANCE	
PowerPlane – C_{IN}	N/A	N/A for SOA, keep small for efficiency	N/A		N/A for SOA, keep small for efficiency	
C_{IN} – SMPSx_IN	1 nH	3 mΩ	SMPS1	0.533 nH	SMPS1	1.77 mΩ
			SMPS2	0.465 nH	SMPS2	1.22 mΩ
			SMPS3	0.494 nH	SMPS3	1.37 mΩ
			SMPS4	0.472 nH	SMPS4	1.23 mΩ
			SMPS5	0.517 nH	SMPS5	1.27 mΩ
			SMPS6	0.518 nH	SMPS6	1.69 mΩ
			SMPS7	0.501 nH	SMPS7	1.27 mΩ
			SMPS8	0.509 nH	SMPS8	1.42 mΩ
			SMPS9	0.491 nH	SMPS9	1.4 mΩ
C_{IN} – SMPSx_GND	1 nH	2 mΩ	SMPS1	0.552 nH	SMPS1	1.21 mΩ
			SMPS2	0.583 nH	SMPS2	0.8 mΩ
			SMPS3	0.668 nH	SMPS3	0.93 mΩ
			SMPS4	0.57 nH	SMPS4	0.81 mΩ
			SMPS5	0.577 nH	SMPS5	0.76 mΩ
			SMPS6	0.608 nH	SMPS6	1.13 mΩ
			SMPS7	0.646 nH	SMPS7	0.83 mΩ
			SMPS8	0.67 nH	SMPS8	0.73 mΩ
			SMPS9	0.622 nH	SMPS9	0.82 mΩ
SMPSx_SW – Inductor	N/A	N/A for SOA, keep small for efficiency	N/A		SMPS1	1.9 mΩ
					SMPS2	0.89 mΩ
					SMPS3	1.99 mΩ
					SMPS4	0.93 mΩ
					SMPS5	1.37 mΩ
					SMPS6	1.11 mΩ
					SMPS7	1.17 mΩ
					SMPS8	1.35 mΩ
					SMPS9	0.88 mΩ
Inductor – C_{OUT}	N/A	N/A for SOA, keep small for efficiency	N/A		N/A for SOA, keep small for efficiency	
C_{OUT} – GND	Use dedicated GND plane to keep inductance low	mΩ	SMPS1	0.552 nH	SMPS1	1.21 mΩ
			SMPS2	0.583 nH	SMPS2	0.8 mΩ
			SMPS3	0.668 nH	SMPS3	0.93 mΩ
			SMPS4	0.57 nH	SMPS4	0.81 mΩ
			SMPS5	0.577 nH	SMPS5	0.76 mΩ
			SMPS6	0.608 nH	SMPS6	1.13 mΩ
			SMPS7	0.646 nH	SMPS7	0.83 mΩ
			SMPS8	0.67 nH	SMPS8	0.73 mΩ
			SMPS9	0.622 nH	SMPS9	0.82 mΩ
GND(C_{IN}) – GND(C_{OUT})	Use dedicated GND plane to keep inductance low	mΩ	Use dedicated GND plane to keep inductance low		mΩ	

TI recommends to measure the voltages across the high-side FET (voltage at SMPSx_IN vs. SMPSx_SW) and the low-side FET (SMPSx_SW vs. SMPSx_GND) with a high-bandwidth high-sampling rate scope with a low-capacitance probe (ideally a differential probe). Measure the voltages as close as possible to the device-pins and verify the amplitude of the spikes. A small-loop-GND-connection to the closest accessible SMPSx_GND (of the particular rail) is essential. Ideally, this measurement should be performed during start-up of the respective SMPS-rail (to take in account the inrush-current) and at high temperature.

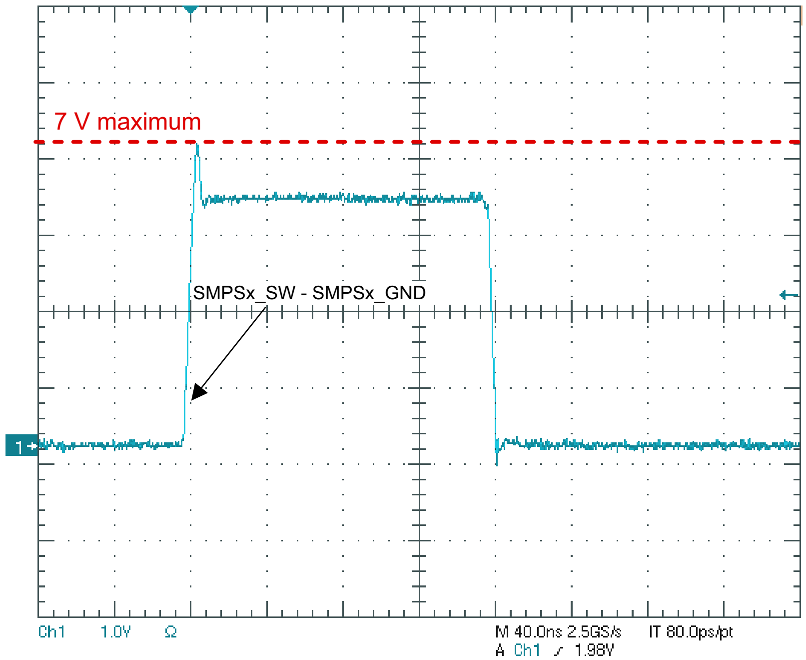
When measuring the voltage difference between the SMPSx_IN and SMPSx_SW pins, there should be a maximum of 7V when measuring at the pins. Similarly, when measuring the voltage difference between the SMPSx_SW and SMPSx_GND pins, there should be a maximum of 7V when measuring at the pins.

For more information on cursor-positioning, see 图 8-2 and 图 8-3.



Measure across the high-side FET (SMPSx_IN – SMPSx_SW) as close to the IC as possible. The preferred measurement is with a differential probe. The negative side of the probe should be at SMPSx_SW and the positive side of the probe should measure SMPSx_IN. As shown in this image, the voltage across the high-side FET should not exceed 7V. Repeat the measurement for all SMPSs in use.

图 8-2. Measuring the High-side FET (Differentially)



Measure across the low-side FET (SMPSx_SW – SMPSx_GND) as close to the IC as possible. The preferred measurement is with a differential probe. The negative side of the probe should be at SMPSx_GND and the positive side of the probe should measure SMPSx_SW. As shown in this image, the voltage across the low-side FET should not exceed 7V.Repeat the measurement for all SMPSs in use.

图 8-3. Measuring the Low-side FET (Differentially)

8.2 Layout Example

图 8-4, 图 8-5, 图 8-6, and 图 8-7 show the actual placement and routing on the EVM.

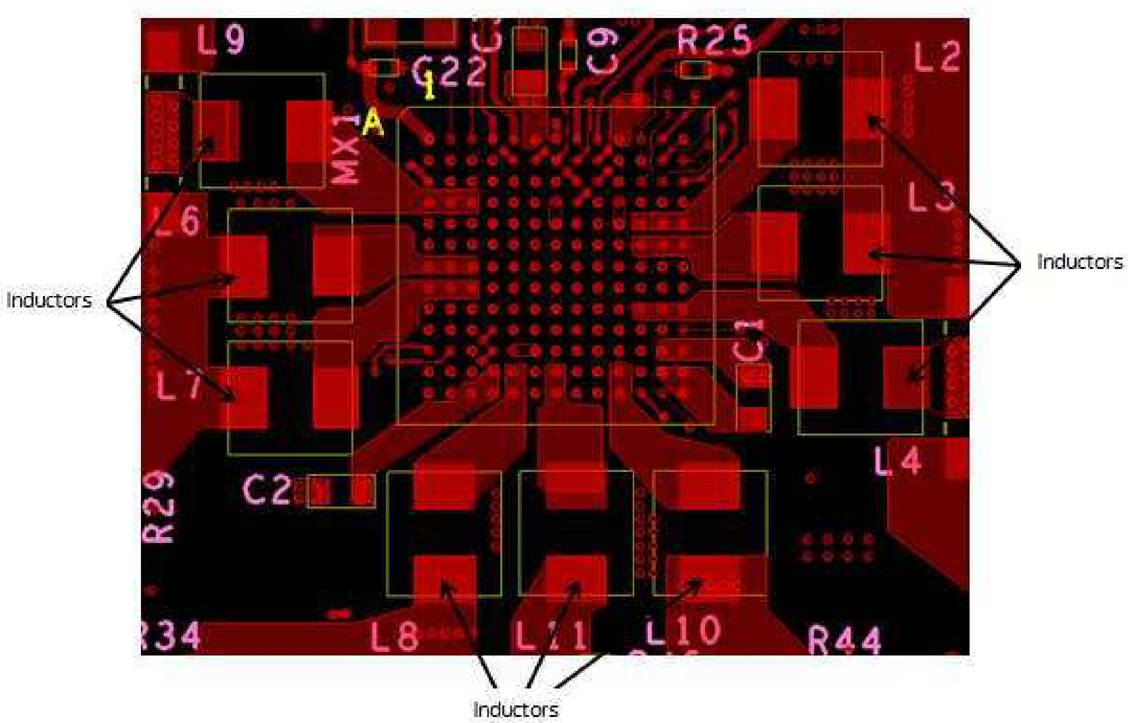


图 8-4. Top-Layer Overview of Inductor Placement

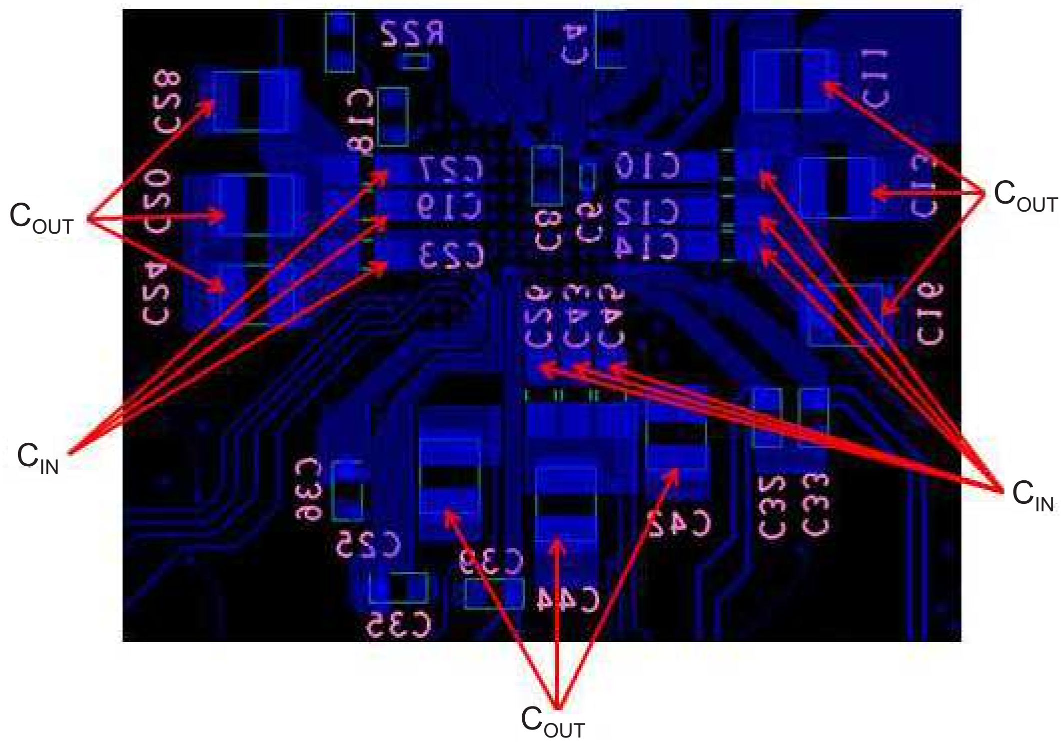


图 8-5. Bottom-Layer Overview of Input and Output Capacitor Placement

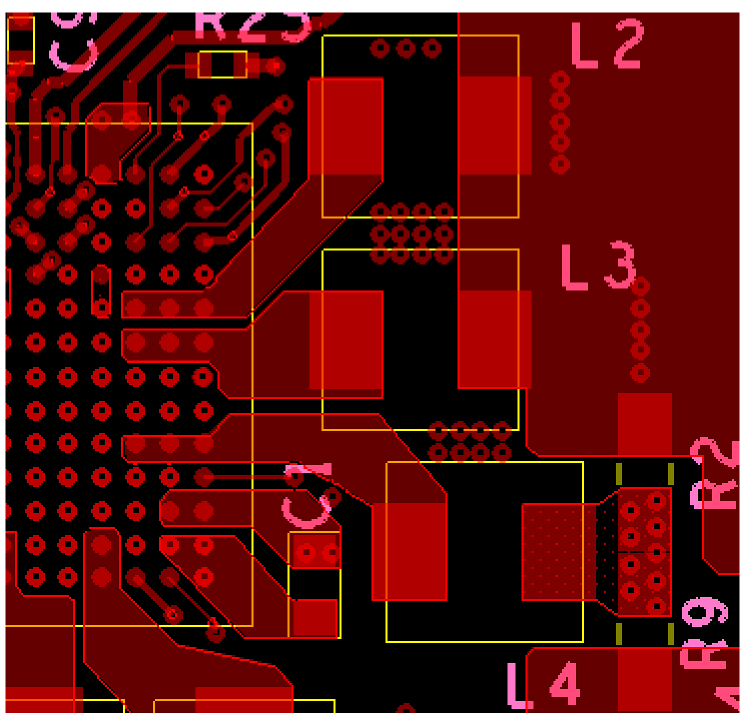


图 8-6. Top-Layer Zoomed-In View of SMPS123 SW Connections to Inductors

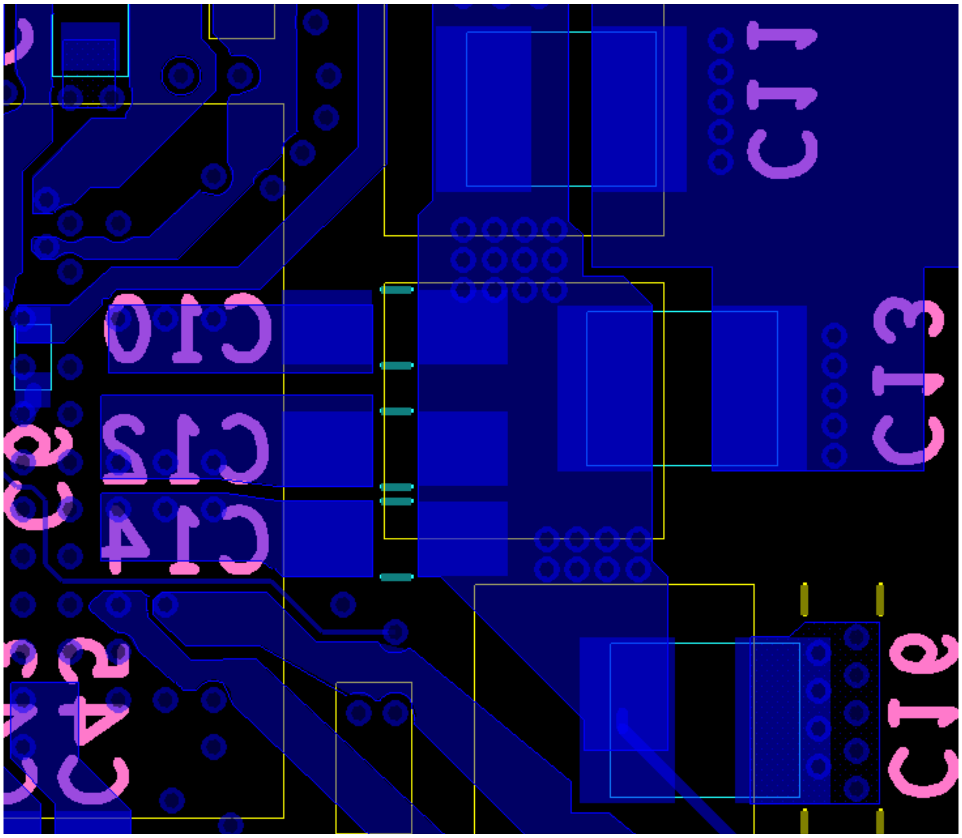


图 8-7. Bottom-Layer Zoomed-In View of SMPS123 Input and Output Capacitor Layout

9 器件和文档支持

9.1 器件支持

9.1.1 第三方产品免责声明

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9.2 文档支持

9.2.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《TPS65903x 和 TPS6591x 器件中的 GPADC 使用指南》*
- 德州仪器 (TI)，*《使用 TI AM57x 处理器的电源设计和热设计注意事项》设计指南*
- 德州仪器 (TI)，*《TPS65903x 和 TPS6591x 器件中的 POR 生成》*
- 德州仪器 (TI)，*《TPS659037 设计检查清单》*
- 德州仪器 (TI)，*《TPS659037 设计指南》*
- 德州仪器 (TI)，*《TPS659037 寄存器映射》*
- 德州仪器 (TI)，*《为 AM572x 和 AM571x 供电的 TPS659037 用户指南》*
- 德州仪器 (TI)，*《TPS659037EVM 用户指南》*

9.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

设计支持 ***TI** 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

9.5 商标

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS6590376ZWSR	NRND	Production	NFBGA (ZWS) | 169	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS659037 OTP 8A 1.3
TPS6590376ZWSR.A	NRND	Production	NFBGA (ZWS) | 169	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS659037 OTP 8A 1.3
TPS6590376ZWSR.B	NRND	Production	NFBGA (ZWS) | 169	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS659037 OTP 8A 1.3
TPS6590376ZWST	NRND	Production	NFBGA (ZWS) | 169	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS659037 OTP 8A 1.3
TPS6590376ZWST.A	NRND	Production	NFBGA (ZWS) | 169	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS659037 OTP 8A 1.3
TPS6590376ZWST.B	NRND	Production	NFBGA (ZWS) | 169	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS659037 OTP 8A 1.3
TPS6590377ZWSR	NRND	Production	NFBGA (ZWS) | 169	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS659037 OTP 8B 1.3
TPS6590377ZWSR.A	NRND	Production	NFBGA (ZWS) | 169	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS659037 OTP 8B 1.3
TPS6590377ZWSR.B	NRND	Production	NFBGA (ZWS) | 169	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS659037 OTP 8B 1.3
TPS6590377ZWST	NRND	Production	NFBGA (ZWS) | 169	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS659037 OTP 8B 1.3
TPS6590377ZWST.A	NRND	Production	NFBGA (ZWS) | 169	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS659037 OTP 8B 1.3
TPS6590377ZWST.B	NRND	Production	NFBGA (ZWS) | 169	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS659037 OTP 8B 1.3
TPS6590378ZWSR	Active	Production	NFBGA (ZWS) | 169	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS659037 OTP 96 1.3
TPS6590378ZWSR.A	Active	Production	NFBGA (ZWS) | 169	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS659037 OTP 96 1.3
TPS6590378ZWSR.B	Active	Production	NFBGA (ZWS) | 169	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS659037 OTP 96 1.3
TPS6590378ZWST	Active	Production	NFBGA (ZWS) | 169	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS659037 OTP 96 1.3

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS6590378ZWST.A	Active	Production	NFBGA (ZWS) | 169	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS659037 OTP 96 1.3
TPS6590378ZWST.B	Active	Production	NFBGA (ZWS) | 169	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS659037 OTP 96 1.3
TPS6590379ZWSR	Active	Production	NFBGA (ZWS) | 169	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS659037 OTP 97 1.3
TPS6590379ZWSR.A	Active	Production	NFBGA (ZWS) | 169	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS659037 OTP 97 1.3
TPS6590379ZWSR.B	Active	Production	NFBGA (ZWS) | 169	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS659037 OTP 97 1.3
TPS6590379ZWST	Active	Production	NFBGA (ZWS) | 169	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS659037 OTP 97 1.3
TPS6590379ZWST.A	Active	Production	NFBGA (ZWS) | 169	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS659037 OTP 97 1.3
TPS6590379ZWST.B	Active	Production	NFBGA (ZWS) | 169	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS659037 OTP 97 1.3

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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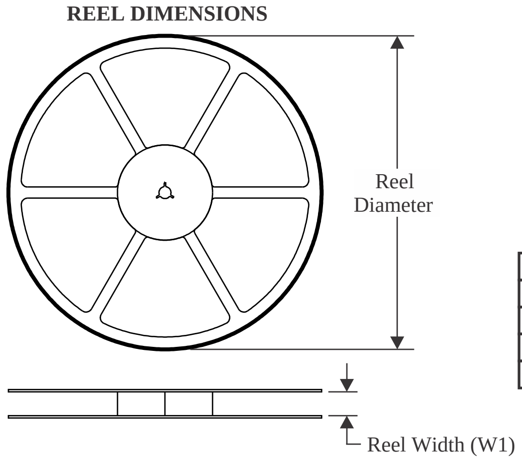
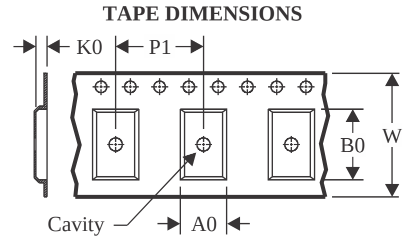
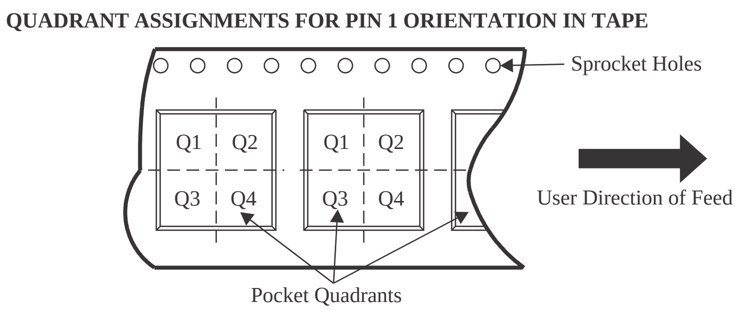
TAPE AND REEL INFORMATION





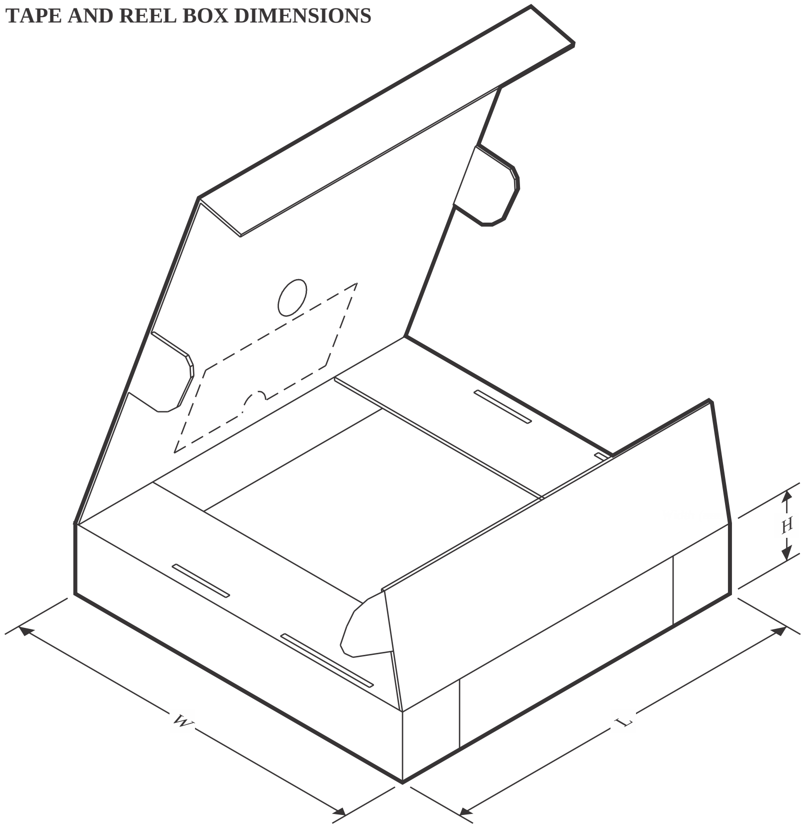
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

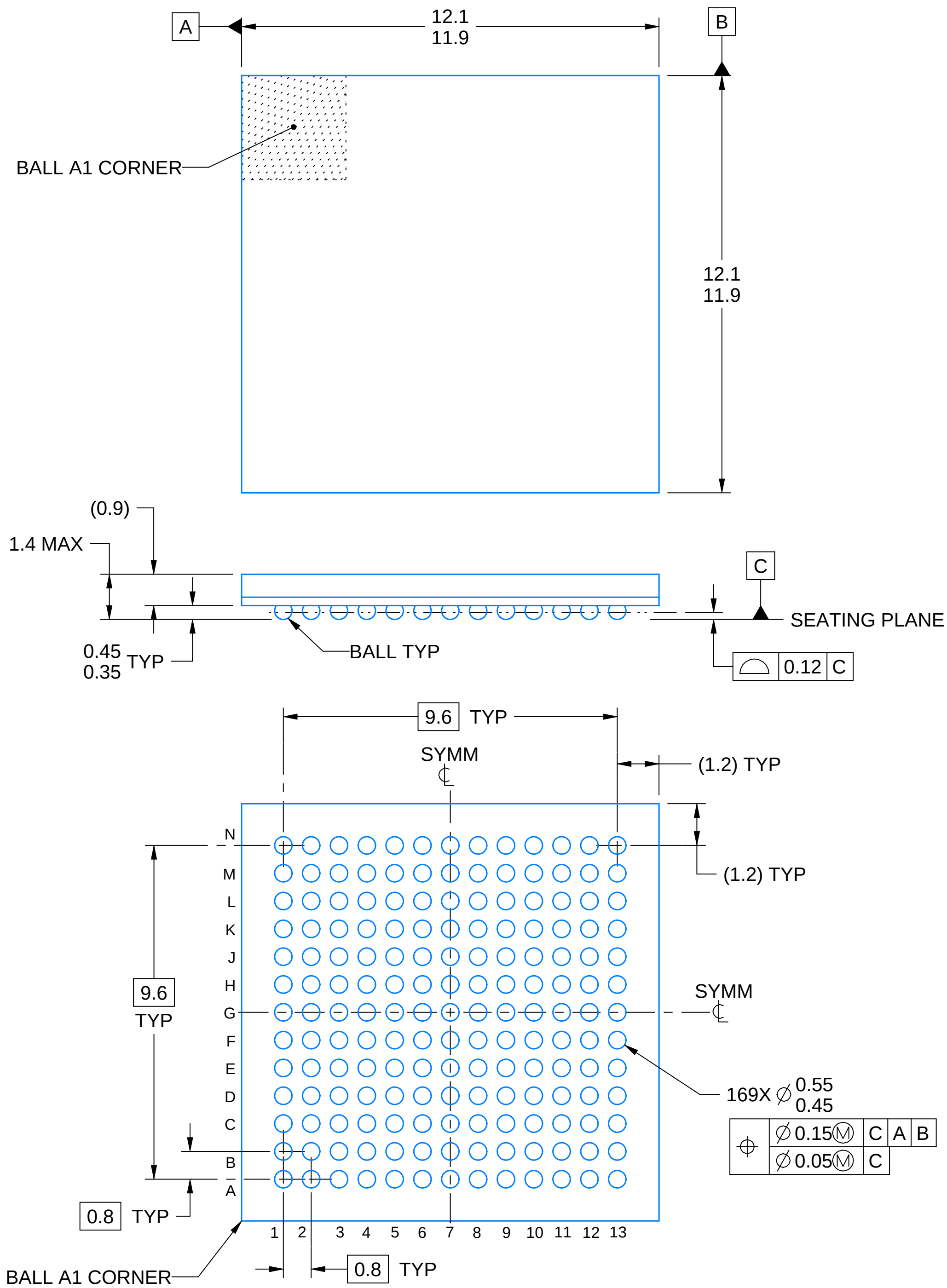
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS6590376ZWSR	NFBGA	ZWS	169	1000	330.0	24.4	12.35	12.35	2.3	16.0	24.0	Q1
TPS6590376ZWST	NFBGA	ZWS	169	250	330.0	24.4	12.35	12.35	2.3	16.0	24.0	Q1
TPS6590377ZWSR	NFBGA	ZWS	169	1000	330.0	24.4	12.35	12.35	2.3	16.0	24.0	Q1
TPS6590377ZWST	NFBGA	ZWS	169	250	330.0	24.4	12.35	12.35	2.3	16.0	24.0	Q1
TPS6590378ZWSR	NFBGA	ZWS	169	1000	330.0	24.4	12.35	12.35	2.3	16.0	24.0	Q1
TPS6590378ZWST	NFBGA	ZWS	169	250	330.0	24.4	12.35	12.35	2.3	16.0	24.0	Q1
TPS6590379ZWSR	NFBGA	ZWS	169	1000	330.0	24.4	12.35	12.35	2.3	16.0	24.0	Q1
TPS6590379ZWST	NFBGA	ZWS	169	250	330.0	24.4	12.35	12.35	2.3	16.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS6590376ZWSR	NFBGA	ZWS	169	1000	336.6	336.6	41.3
TPS6590376ZWST	NFBGA	ZWS	169	250	336.6	336.6	41.3
TPS6590377ZWSR	NFBGA	ZWS	169	1000	336.6	336.6	41.3
TPS6590377ZWST	NFBGA	ZWS	169	250	336.6	336.6	41.3
TPS6590378ZWSR	NFBGA	ZWS	169	1000	336.6	336.6	41.3
TPS6590378ZWST	NFBGA	ZWS	169	250	336.6	336.6	41.3
TPS6590379ZWSR	NFBGA	ZWS	169	1000	336.6	336.6	41.3
TPS6590379ZWST	NFBGA	ZWS	169	250	336.6	336.6	41.3



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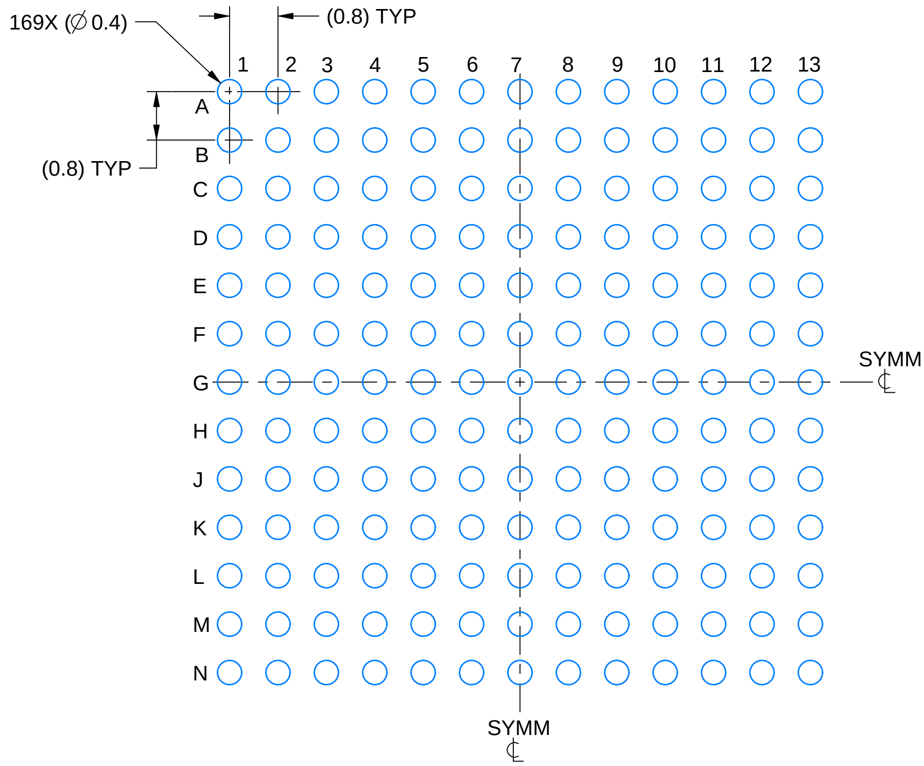
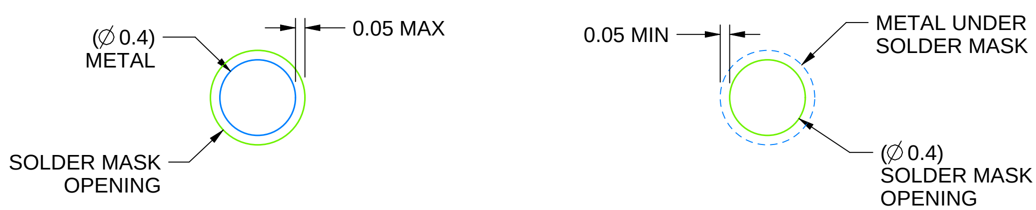
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS
NOT TO SCALE

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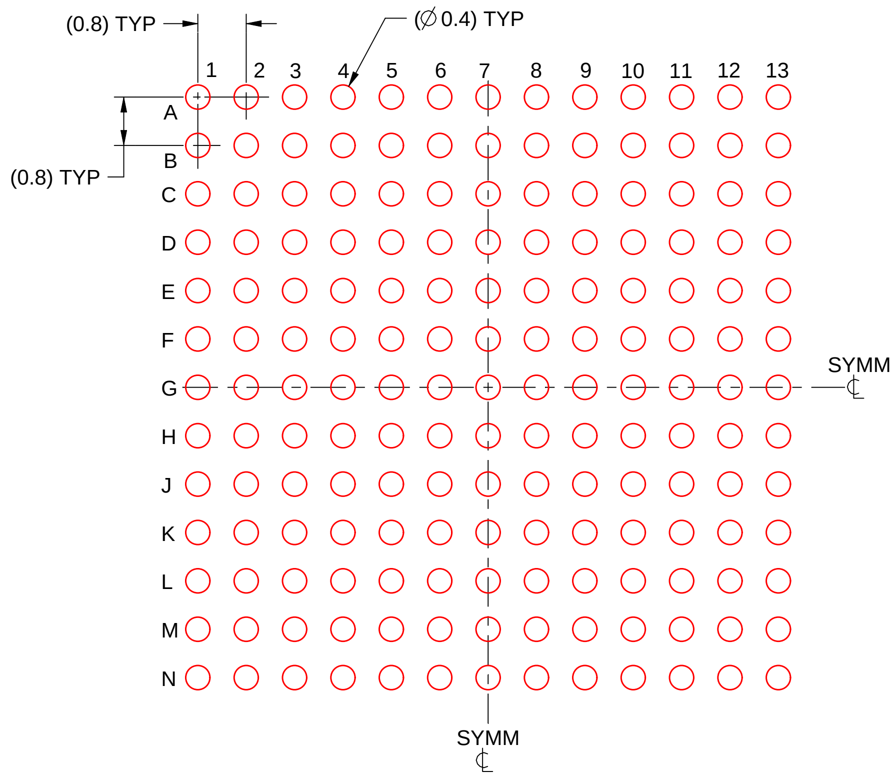
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SSZA002 (www.ti.com/lit/ssza002).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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