# 4.5V 至 18V 输入电压 1.5A，2.5A，1.5A 三路同步降压转换器

查询样品: TPS65581

## 特性

- 高级 **D-CAP2™** 控制模式
  - 快速瞬态响应
  - 环路补偿无需外部部件
  - 与陶瓷输出电容器兼容
- 宽输入电压范围：**4.5V** 至 **18V**
- 输出电压范围：**0.76V** 至 **7V**
- 针对低占空比应用对高效集成场效应晶体管 **(FET)** 进行了优化
  - 对于 **2.5A** 电流为 **160mΩ**（高侧）和 **130mΩ**（低侧）
  - 对于 **1.5A** 电流为 **250mΩ**（高侧）和 **230mΩ**（低侧）
- 高初始基准精度
- 低侧 $R_{DS(on)}$ 低损耗电流感测
- 固定 **1.2ms** 软启动
- 非吸入预偏置软启动
- **700kHz** 开关频率
- 逐周期过流限制控制
- 过流限制 **(OCL)**，过压 **(OVP)**，欠压 **(UVP)**，欠压闭锁 **(UVLO)**，热关断 **(TSD)** 保护
- 针对过载保护的断续定时器
- 电源正常 **(PowerGood)**
- 带有集成式升压 **P** 通道金属氧化物半导体 **(PMOS)** 开关的自适应栅极驱动器
- 由于热补偿 $R_{DS(on)}$ 的值为 **4000ppm/**℃ ，过流保护 **(OCP)** 恒定
- **20** 引脚散热薄型小外形尺寸封装 **(HTSSOP)**
- 自动跳跃 **Eco-mode ™** 为了在轻负载下实现高效率

## 应用范围

- 针对广泛应用的低功耗系统中的负载点调节
  - 数字电视电源
  - 网络互联家庭终端设备
  - 数字机顶盒 **(STB)**
  - **DVD** 播放器，刻录机
  - 游戏控制台和其它设备

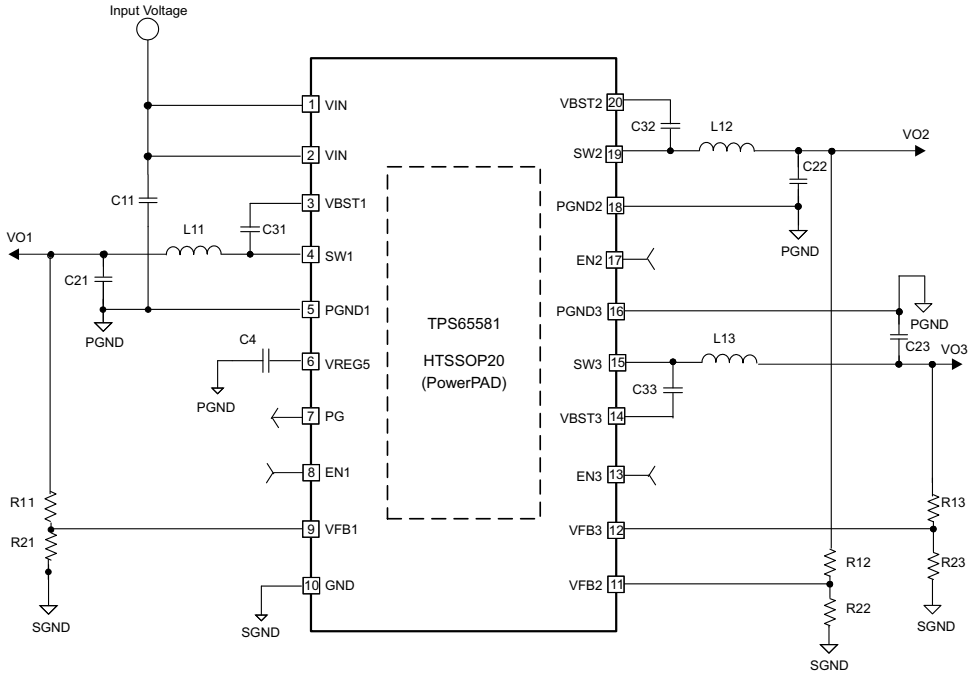
## 说明

TPS65581 是一款三路、高级 D-CAP2™ 模式同步降压转换器。 TPS65581 可帮助系统设计人员通过成本有效性、低组件数量和低待机电流解决方案来完成多种终端设备的电源总线调节器集。 TPS65581 的主控制环路采用高级 D-CAP2™ 模式控制，无需外部补偿组件即可提供快速的瞬态响应。 高级 D-CAP2™ 模式控制支持较高负载条件下脉宽调制 (PWM) 模式与 Eco-mode™ 之间的无缝转换，从而使得 TPS65581 能够在轻负载期间保持高效率。 此器件能够适应诸如高分子有机半导体固体电容器 (POSCAP) 或者高分子聚合物电容器 (SP-CAP) 等低等效串联电阻 (ESR) 输出电容器，以及超低 ESR，陶瓷电容器。 此器件在输入电压为 4.5V 至 18V 之间时提供便捷且有效的运行。

TPS65581 采用 4.4mm x 6.5mm 20 引脚 TSSOP (PWP) 封装，额定环境温度范围为 -40°C 至 85°C。

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## HTSSOP APPLICATION DIAGRAM




## ORDERING INFORMATION

| $T_A$ | PACKAGE(1) | ORDERING PART NUMBER | PINS | OUTPUT SUPPLY |
|---|---|---|---|---|
| –40℃ to 85℃ | PWP | TPS65581PWPR | 20 | Tape-and-Reel |
| | | TPS65581PWP | | Tube |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)(2)

| | | VALUE | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| Input voltage range | VIN, EN1, EN2, EN3 | –0.3 | 20 | V |
| | VBST1, VBST2, VBST3 | –0.3 | 26 | |
| | VBST1, VBST2, VBST3 (10ns transient) | –0.3 | 28 | |
| | VBST1–SW1, VBST2–SW2, VBST3–SW3 | –0.3 | 6.5 | |
| | VFB1, VFB2, VFB3 | –0.3 | 6.5 | |
| | SW1, SW2, SW3 | –2 | 20 | |
| | SW1, SW2, SW3 (10ns transient) | –3 | 22 | |
| Output voltage range | VREG5, PG | –0.3 | 6.5 | V |
| | PGND1, PGND2, PGND3 | –0.3 | 0.3 | |
| Electrostatic discharge | Human Body Model (HBM) | | 2 | kV |
| | Charged Device Model (CDM) | | 500 | V |
| Operating ambient temperature range, $T_A$ | | –40 | 85 | °C |
| Storage temperature range, $T_{STG}$ | | –55 | 150 | °C |
| Junction temperature range, $T_J$ | | –40 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to IC GND terminal.

## THERMAL INFORMATION

| THERMAL METRIC(1) | | TPS65581 | UNITS |
|---|---|---|---|
| | | PWP (20) PINS | |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 40.0 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 24.8 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 21.3 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.8 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 21.1 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | 1.7 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics application report*, SPRA953.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | | VALUES | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| | Supply input voltage range | VIN | 4.5 | 18 | V |
| | Input voltage range | VBST1, VBST2, VBST3 | –0.1 | 24 | V |
| | | VBST1, VBST2, VBST3 (10ns transient) | –0.1 | 27 | |
| | | VBST1–SW1, VBST2–SW2, VBST3–SW3 | –0.1 | 5.7 | |
| | | VFB1, VFB2, VFB3 | –0.1 | 5.7 | |
| | | EN1, EN2, EN3 | –0.1 | 18 | |
| | | SW1, SW2, SW3 | –1.0 | 18 | |
| | | SW1, SW2, SW3 (10ns transient) | –3 | 21 | |
| | Output voltage range | VREG5, PG | –0.1 | 5.7 | V |
| | | PGND1, PGND2, PGND3 | –0.1 | 0.1 | |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |
| $T_J$ | Operating Junction Temperature | | –40 | 150 | °C |

## ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range, VIN = 12 V (unless otherwise noted)

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | |
| $I_{IN}$ | VIN supply current | $T_A$ = 25°C, EN1 = EN2 = EN3 = 5 V, VFB1 = VFB2 = VFB3 = 1 V, non-switching | | 2.9 | 3.6 | mA |
| $I_{VINSDN}$ | VIN shutdown current | $T_A$ = 25°C, EN1 = EN2 = EN3 = 0 V | | 1.8 | 3 | µA |
| **VFB VOLTAGE** | | | | | | |
| $V_{VFBTHL}$ | VFBx threshold voltage (1) | $T_A$ = 25°C, CH1 = 3.3 V, CH2 = 1.2 V, CH3 = 1.5 V | 752 | 764 | 776 | mV |
| $TC_{VFBx}$ | Temperature coefficient | On the basis of 25°C (2) | –180 | | 180 | ppm/°C |
| **VREG5 OUTPUT** | | | | | | |
| $V_{UVREG5}$ | VREG5 UVLO Threshold | VREG5 Rising | | 4 | | V |
| | | Hysteresis | | 0.3 | | |
| $V_{VREG5}$ | VREG5 output voltage | $T_A$ = 25°C, $V_{IN}$ = 12 V, $I_{VREG}$ = 5 mA | | 5.5 | | V |
| $I_{VREG5}$ | Output current | VIN = 6 V, $T_A$ = 25°C | 20 | | | mA |
| **MOSFETs** | | | | | | |
| $r_{DS(on)H2}$ | High side switch resistance for 2.5A | $T_A$ = 25℃, VBST2-SW2 = 5.5 V (2) , CH2 | | 160 | | mΩ |
| $r_{DS(on)H2}$ | Low side switch resistance for 2.5A | $T_A$ = 25℃ (2), CH2 | | 130 | | mΩ |
| $r_{DS(on)Hx}$ | High side switch resistance for 1.5A | $T_A$ = 25℃, VBSTx-SWx = 5.5 V (2) , CH1, CH3 | | 250 | | mΩ |
| $r_{DS(on)Lx}$ | Low side switch resistance for 1.5A | $T_A$ = 25℃ (2), CH1, CH3 | | 230 | | mΩ |
| **MIN ON/OFF TIME and SW frequency** | | | | | | |
| $t_{ONminx}$ | Min On Time | $T_A$ = 25℃, VOUTx = 0.8V (2) | 80 | | | ns |
| $t_{OFFminx}$ | Minoff time | $T_A$ = 25℃, VFBx = 0.7 V | | 220 | | ns |
| Fsw | SW-frequency | $T_A$ = 25℃ | | 700 | | kHz |
| **SOFT START** | | | | | | |
| $T_{SS}$ | Soft-start time | Internal soft-start time | | 1.2 | | ms |

(1) x means either 1 or 2 or 3, that is, VFBx means VFB1, VFB2 or VFB3.
(2) Specified by design. Not production tested.

## ELECTRICAL CHARACTERISTICS (continued)

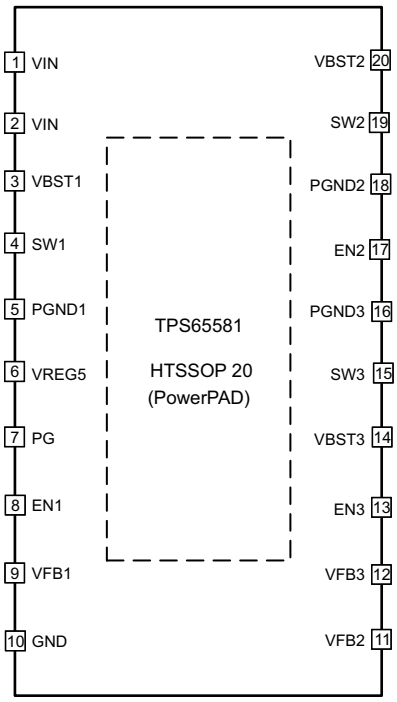
over recommended free-air temperature range, VIN = 12 V (unless otherwise noted)

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER GOOD** | | | | | | |
| $V_{PGTH}$ | PG threshold | PG from lower VOx (going high) | | 84% | | |
| | | PG from higher VOx (going low) | | 116% | | |
| $R_{PG}$ | PG pull-down resistance | $V_{PG}$ = 0.5 V | 50 | 85 | 130 | Ω |
| $T_{PGDLY}$ | PG delay time | Delay for PG going high | | 1.5 | | ms |
| | | Delay for PG going low | | 2 | | µs |
| $T_{PGCOMPSS}$ | PGOOD comparator start-up delay | PG comparator wake-up delay | | 2.8 | | ms |
| **LOGIC THRESHOLD** | | | | | | |
| $V_{ENH}$ | ENx H-level threshold voltage | | 2 | | | V |
| $V_{ENL}$ | ENx L-level threshold voltage | | | | 0.4 | V |
| $R_{ENx\_IN}$ | ENx input resistance | ENx = 12 V | 225 | 400 | 900 | kΩ |
| **CURRENT LIMIT** | | | | | | |
| $I_{OCL1}$ | Current limit | $L_{OUT}$ = 3.3 µH(3), VOUT1 = 3.3 V | 1.7 | 2.0 | 3.4 | A |
| $I_{OCL2}$ | | $L_{OUT}$ = 2.2 µH(3) VOUT2 = 1.2 V | 2.9 | 3.5 | 4.9 | A |
| $I_{OCL3}$ | | $L_{OUT}$ = 2.2 µH(3) VOUT3 = 1.5 V | 1.8 | 2.2 | 3.6 | A |
| **UNDER VOLTAGE PROTECTION** | | | | | | |
| $V_{UVP}$ | Output UVP trip threshold | measured on VFBx | 63% | 68% | 73% | |
| $T_{UVPDEL}$ | Output UVP delay time | | | 0.5 | | ms |
| $T_{UVPEN}$ | Output UVP enable delay | UVP Enable Delay | | 2.8 | | ms |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{SD}$ | Thermal shutdown threshold | Shutdown temperature(3) | | 155 | | °C |
| | | Hysteresis(3) | | 30 | | |

(3) Specified by design. Not production tested.

## DEVICE INFORMATION

**HTSSOP PACKAGE**
**(TOP VIEW)**

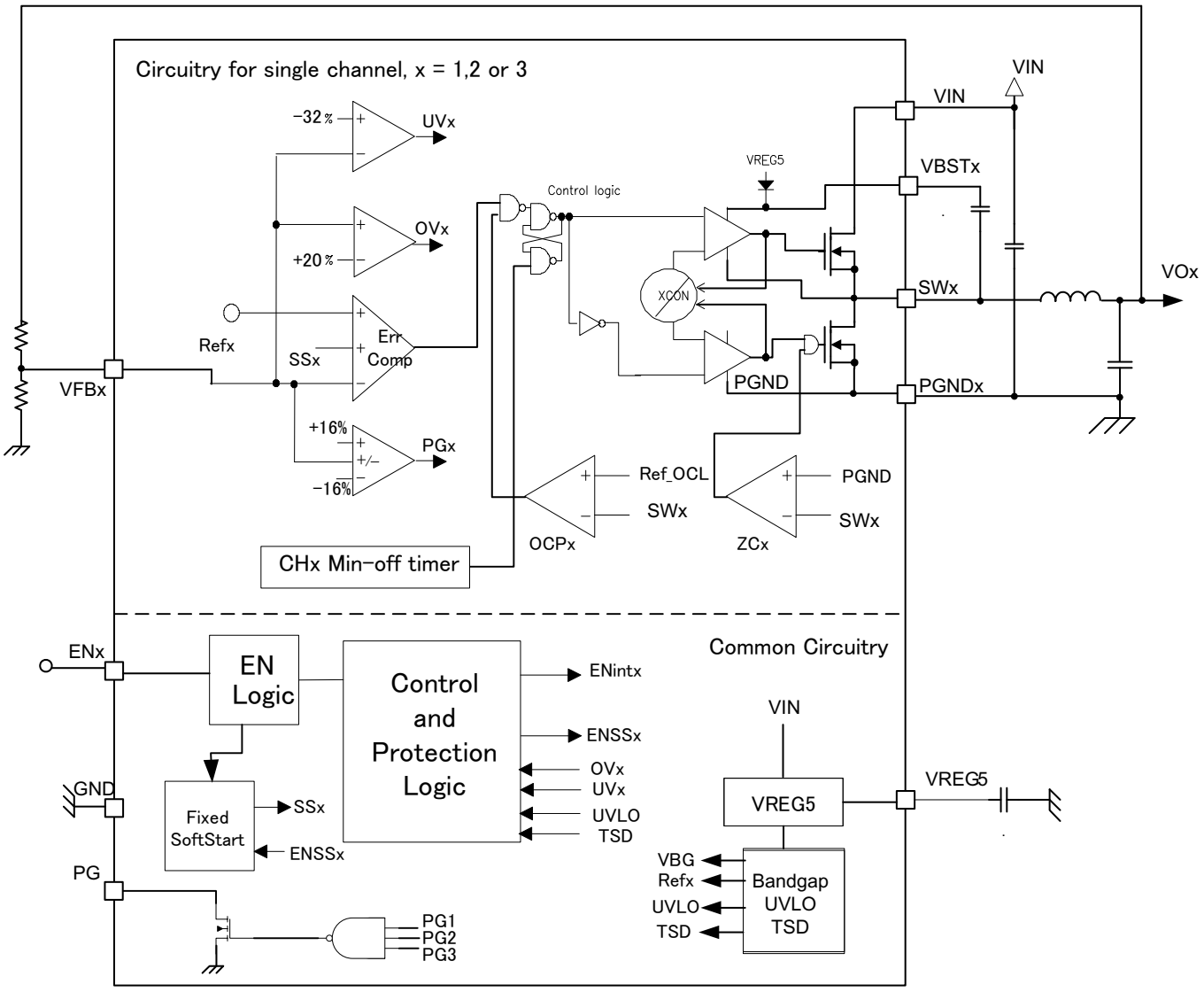



### PIN FUNCTIONS(1)

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | HTSSOP20 | | |
| VIN | 1,2 | I | Power input and connects to both high side NFET drains. Supply Input for 5.5V linear regulator. |
| VBST1, VBST2, VBST3 | 3, 14, 20 | I | Supply input for high-side NFET gate drive circuit. Connect 0.1µF ceramic capacitor between VBSTx and SWx pins. An internal diode is connected between VREG5 and VBSTx |
| SW1, SW2, SW3 | 4,15,19 | I/O | Switch node connections for both the high-side NFETs and low–side NFETs. Input of current comparator. |
| PGND1, PGND2, PGND3 | 5,16,18 | I/O | Ground returns for low-side MOSFETs. Input of current comparator. |
| VREG5 | 6 | O | Output of 5.5V linear regulator. Bypass to GND with a high-quality ceramic capacitor of at least 1.0µF. VREG5 is active when ENx is high level. |
| PG | 7 | O | Open drain power good output. Low means the output voltage is out of regulation. |
| EN1, EN2, EN3 | 8,13,17 | I | Enable. Pull High to according converter. |
| VFB1, VFB2, VFB3 | 9,11,12 | I | Advanced D-CAP2 feedback inputs. Connect to output voltage with resistor divider. |
| GND | 10 | I/O | Signal GND. Connect sensitive VFBx returns to GND at a single point. |
| Exposed Thermal Pad | Back side | I/O | Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Must be connected to GND. |

(1) x means either 1, 2 or 3, VFBx means VFB1, VFB2 or VFB3.

## FUNCTIONAL BLOCK DIAGRAM



## OVERVIEW

The TPS65581 is a 1.5A, 2.5A, 1.5A triple synchronous step-down (buck) converter with two integrated N-channel MOSFETs for each channel. It operates using Advanced D-CAP2™ control mode. The fast transient response of Advanced D-CAP2™ control reduces the required output capacitance to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

## DETAILED DESCRIPTION

### PWM Operation

The main control loop of the TPS65581 is a fixed switching frequency pulse width modulation (PWM) controller that supports a proprietary advanced D-CAP2™ mode control. Advanced D-CAP2™ mode control combines constant switching frequency with an internal compensation circuit and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

### Auto-Skip Eco-mode™ Control

The TPS65581 is designed with Auto-Skip Eco-mode™ to increase light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when its zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

### PWM Frequency and Adaptive On-Time Control

TPS65581 uses a advanced D-CAP2 mode control scheme and have a dedicated on board oscillator. The device runs with fixed frequency of 700 kHz.

### Soft Start and Pre-Biased Soft Start

The TPS65581 has an internal, 1.2 ms, soft-start for each channel. When the ENx pin becomes high, an internal DAC begins ramping up the reference voltage to the PWM comparator. Smooth control of the output voltage is maintained during start up.

The device contains a unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than internal feedback voltage $V_{FB}$), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-biased output, and ensures that the output voltage (VOx) starts and ramps up smoothly into regulation from pre-biased startup to normal mode operation.

### Current Protection

The output overcurrent protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit and using HICCUP mode overcurrent protection. The switch current is monitored by measuring the low-side FET switch voltage between the SWx pin and PGNDx. This voltage is proportional to the switch current and the on-resistance of the FET. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by $V_{IN}$, $V_{OUT}$, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current $I_{OX}$. If the sensed voltage on the low side FET is above the voltage proportional to the current limit, the converter keeps the low-side switch on until the measured voltage falls below the voltage corresponding to the current limit and a new switching cycle begins. In subsequent switching cycles, the on-time is set to the value determined for CCM and the current is monitored in the same manner.

Following are some important considerations for this type of overcurrent protection. The load current one half of the peak-to-peak inductor current higher than the overcurrent threshold. Also when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. When the over current condition is removed, the output voltage returns to the regulated value. This protection is non-latching.

Lower than 1.5 A load current for CH1 and CH3 is required at the $V_{OUT}$ setting in high on-duty because the overcurrent limit function causes the degradation of load transient response.

### Hiccup Mode

Hiccup mode of operation protects the power supply from being damaged during an ove-current fault condition. The operation of hiccup is as follows. If the OCL comparator circuit detects an over-current event the output voltage falls. When the feedback voltage falls below 68% of the reference voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After counting UVP delay time, the TPS65581 shuts off the power supply for a given time (7x UVP Enable Delay Time) and then tries to re-start the power supply. If the over-load condition has been removed, the power supply starts and operates normally; otherwise, the TPS65581 detects another overcurrent event and shuts off the power supply again, repeating the previous cycle. Excess heat due to overload lasts for only a short duration in the hiccup cycle, therefore the junction temperature of the power devices is much lower.

### POWERGOOD

The TPS65581 has power-good output that are measured on VFBx. The power-good function is activated after the soft-start has finished. If the all output voltages of 3 channels are within 16% of the target voltage, the internal comparator detects the power good state and the power good signal becomes high after 1.5ms delay. During start-up, this internal delay starts after 1.5ms of the UVP Enable delay time to avoid a glitch of power-good signal. Even if at least one of the feedback voltages of 3 channels goes outside of ±16% of target value, the power-good signal becomes low after 2 µs.

<Start up>

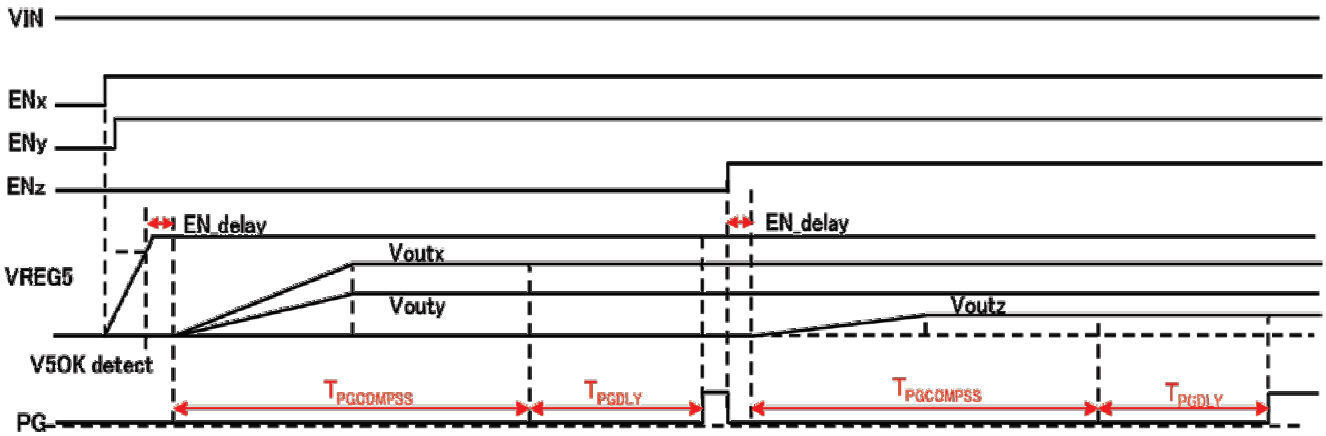



**Figure 1. Start up**

<Vout Transient>

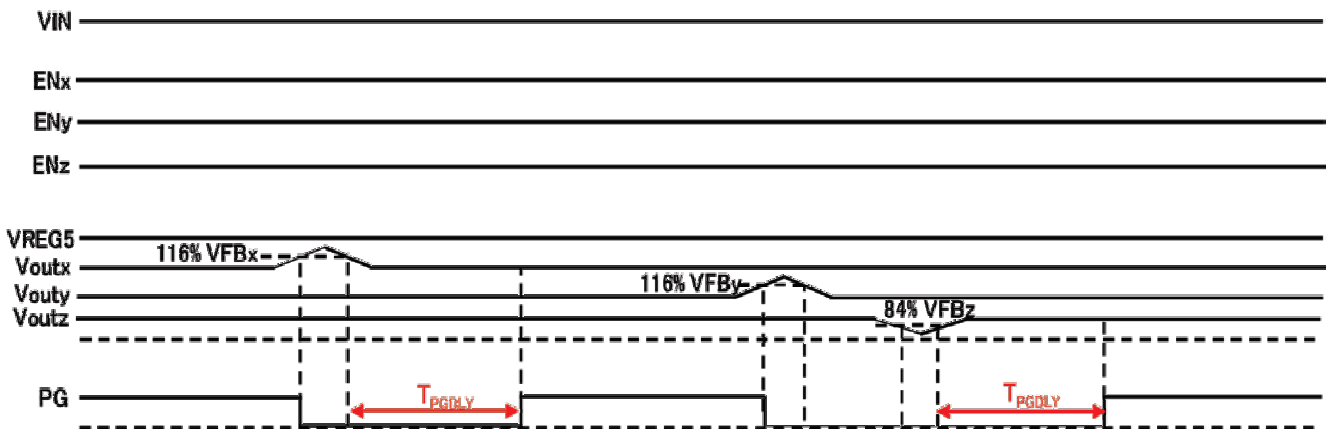



**Figure 2. $V_{OUT}$ Transient**

<Power Down>

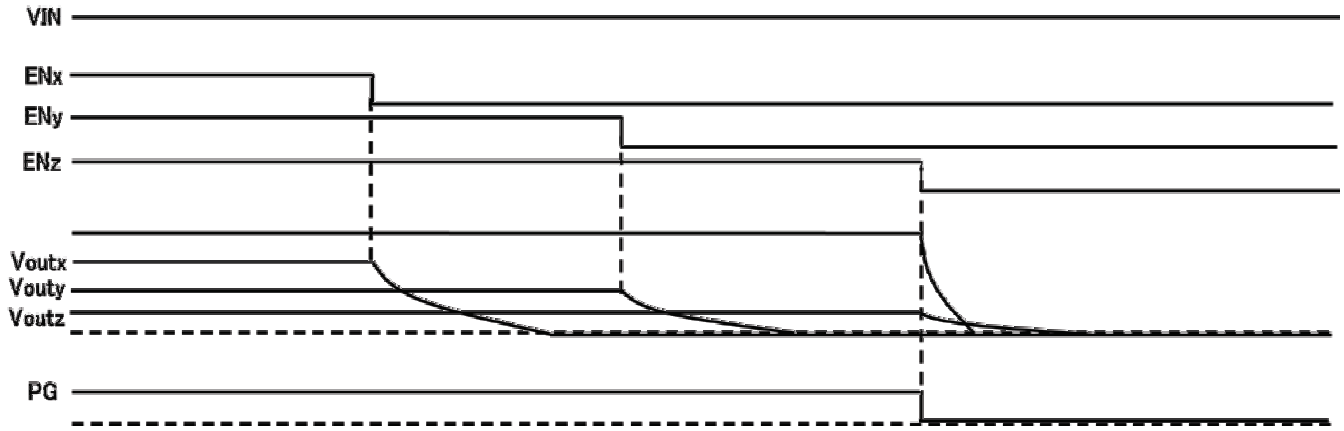



**Figure 3. Power Down**

### UVLO Protection

Under voltage lock out protection (UVLO) monitors the voltage of the VREG5 pin. When the VREG5 voltage is lower than UVLO threshold voltage, the TPS65581 is shut down. As soon as the voltage increases above the UVLO threshold, the converter starts again.

### Thermal Shutdown

TPS65581 monitors its temperature of itself. If the temperature exceeds the threshold value (typically 155°C), the device is shut down. When the temperature falls below the threshold, the IC starts again.

When VIN starts up and VREG5 output voltage is below its nominal value, the thermal shutdown threshold is lower than 155℃. As long as VIN and VREG5 rise, $T_J$ must be kept below 110℃.

## TYPICAL CHARACTERISTICS

VIN = 12 V, $T_A$ = 25°C (unless otherwise noted)

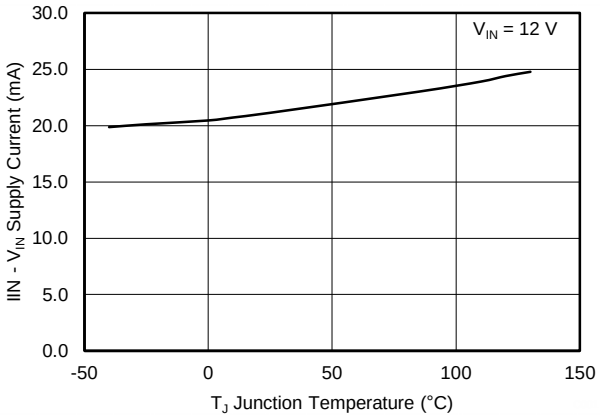



**Figure 4. VIN Current vs Junction Temperature (VIN Current at All CHs Switching with $I_O$ = 0 A)**

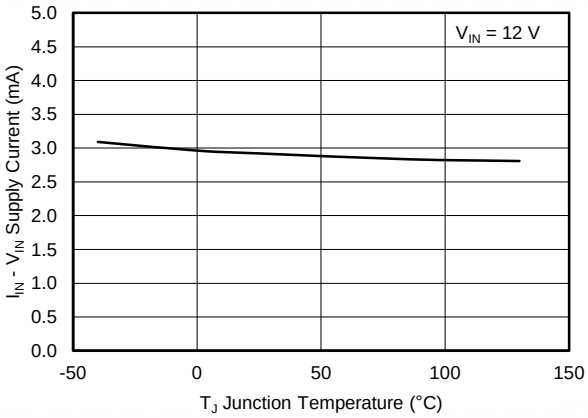



**Figure 5. VIN Current vs Junction Temperature (VIN Current at All CHs Non-switching, EN = H)**

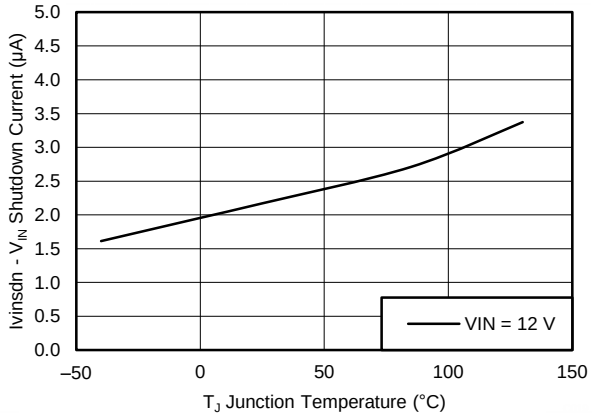



**Figure 6. VIN Shutdown Current vs Junction Temperature**

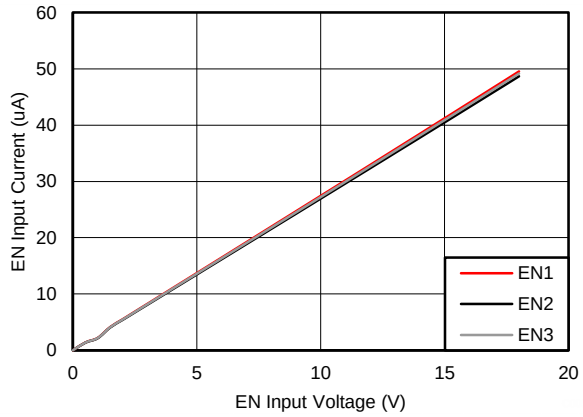



**Figure 7. EN Current vs EN Voltage**

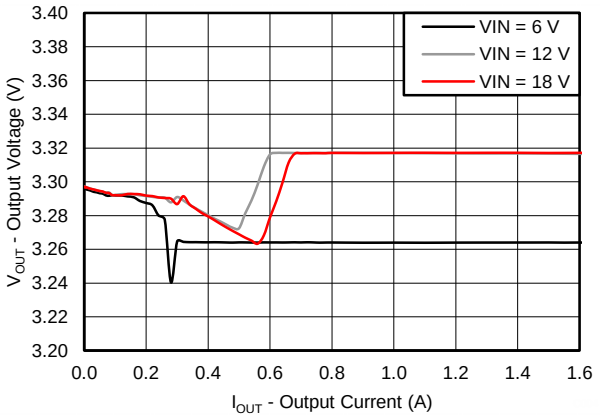



**Figure 8. VOUT1 = 3.3 V Output Voltage vs Output Current**

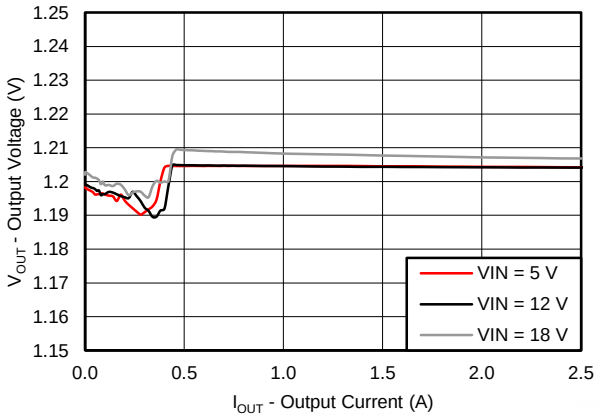



**Figure 9. VOUT2 = 1.2 V Output Voltage vs Output Current**

## TYPICAL CHARACTERISTICS (continued)

VIN = 12 V, $T_A$ = 25°C (unless otherwise noted)

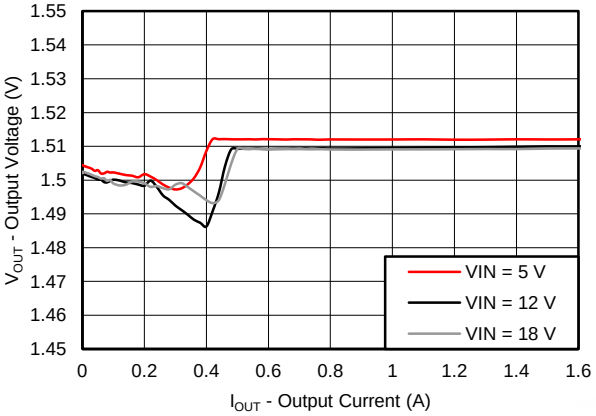



**Figure 10. VOUT3 = 1.5 V Output Voltage vs Output Voltage**

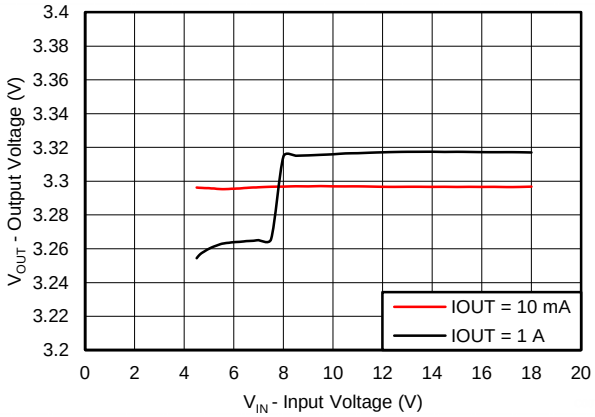



**Figure 11. VOUT1 = 3.3 V Output Voltage vs Input Voltage**

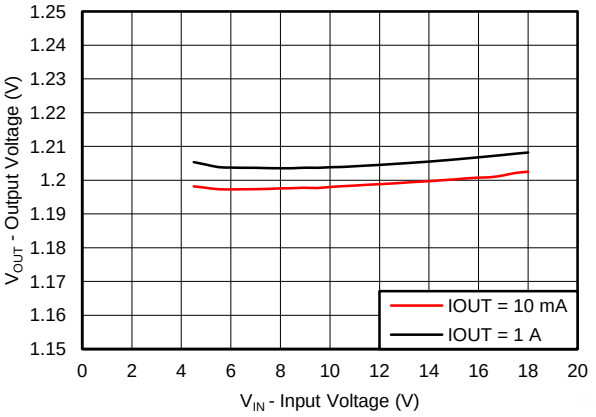



**Figure 12. VOUT2 = 1.2 V Output Voltage vs Input Voltage**

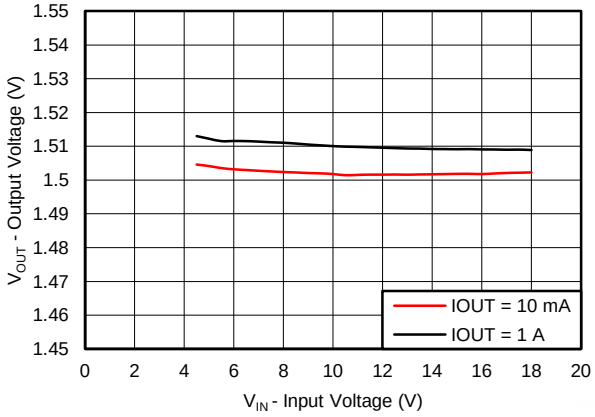



**Figure 13. VOUT3 = 1.5 V Output Voltage vs Input Voltage**

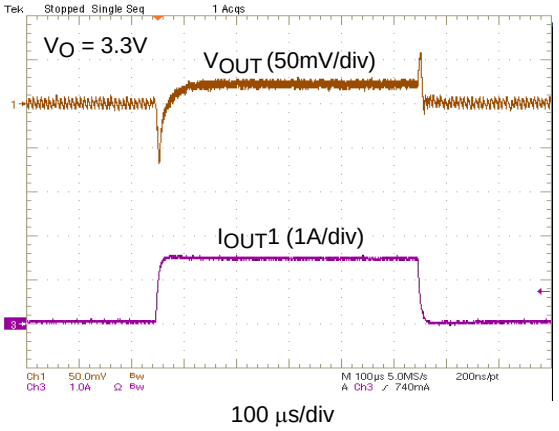



**Figure 14. VOUT1 = 3.3V, 0A to 1.5A Load Transient Response**

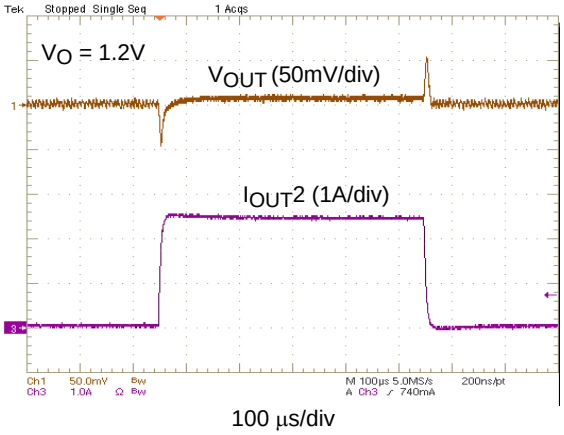



**Figure 15. VOUT2 = 1 .2V, 0A to 2.5A Load Transient Response**

## TYPICAL CHARACTERISTICS (continued)

VIN = 12 V, $T_A$ = 25°C (unless otherwise noted)

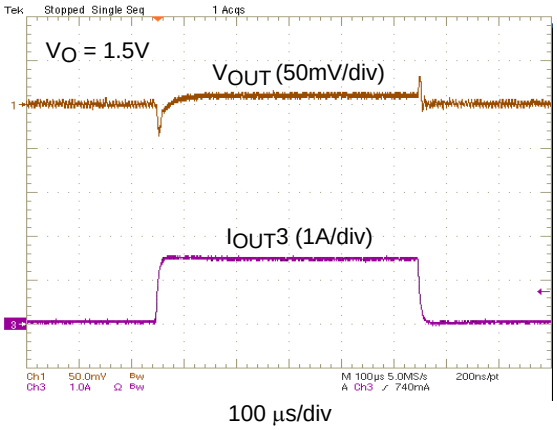



**Figure 16. VOUT3 = 1.5V, 0A to 1.5A Load Transient Response**

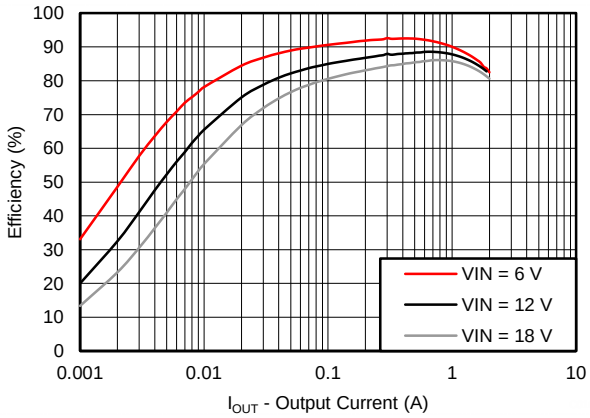



**Figure 17. VOUT1 = 3.3V Light Load Efficiency vs Output Current**

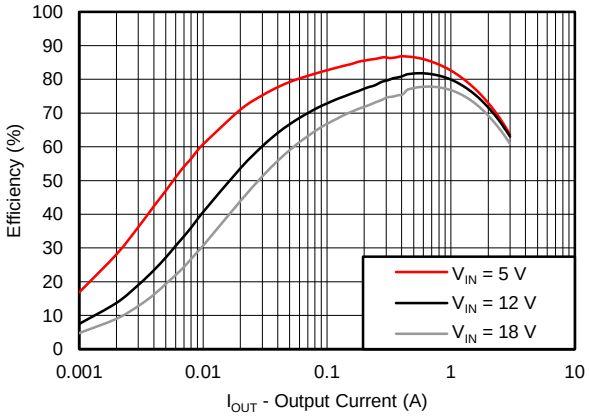



**Figure 18. VOUT2 = 1.2V Light Load Efficiency vs Output Current**

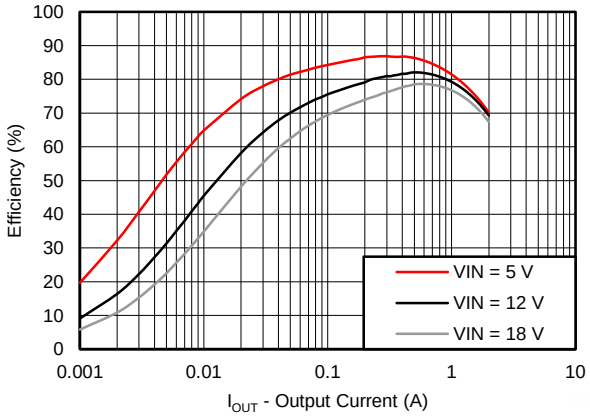



**Figure 19. VOUT3=1.5V, Light Load Efficiency vs Output Current**

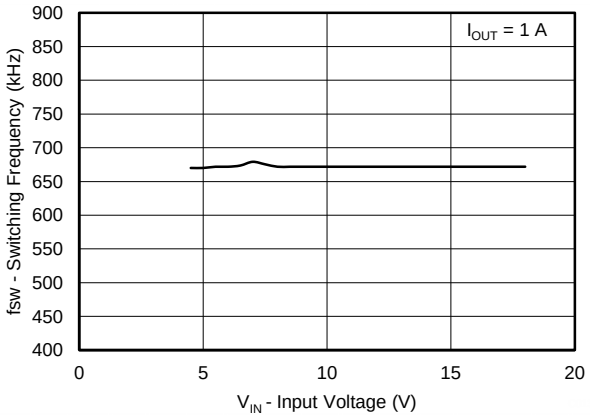



**Figure 20. VOUT1 = 3.3V Switching Frequency vs Input Voltage**

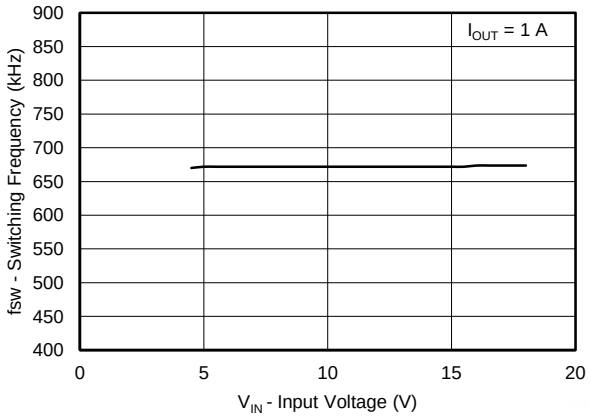



**Figure 21. VOUT2 = 1.2V Switching Frequency vs Input Voltage**

## TYPICAL CHARACTERISTICS (continued)

VIN = 12 V, $T_A$ = 25°C (unless otherwise noted)

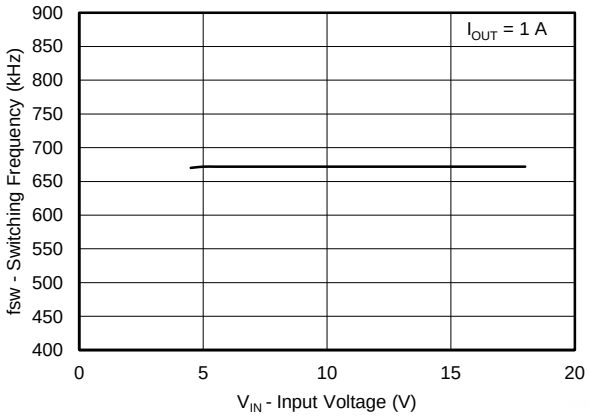



**Figure 22. VOUT3 = 1.5V Switching Frequency vs Input Voltage**

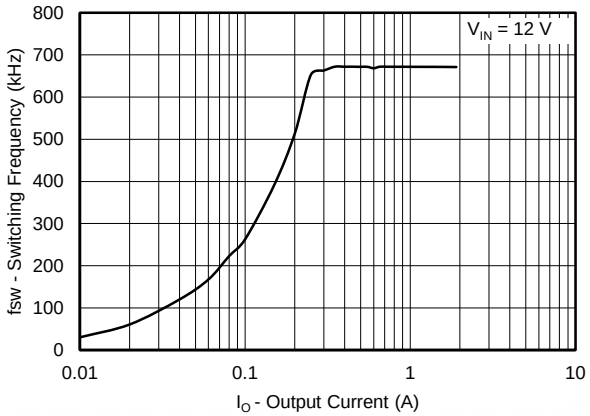



**Figure 23. VOUT1 = 3.3V Switching Frequency vs Output Current**

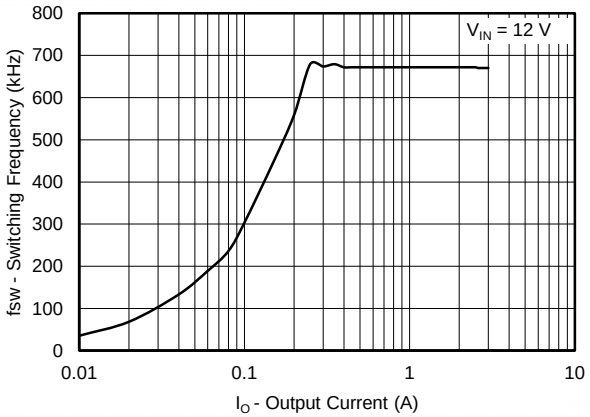



**Figure 24. VOUT2 = 1.2V, Switching Frequency vs Output Current**

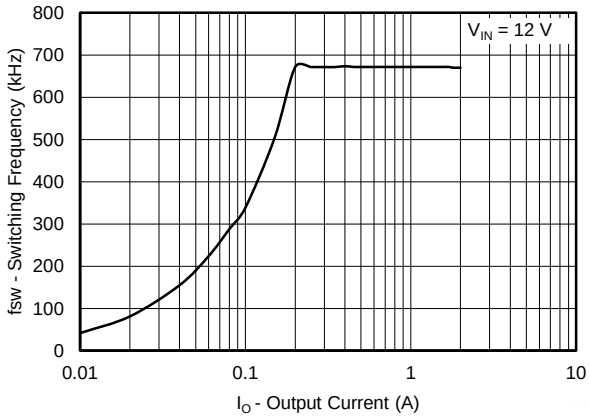



**Figure 25. VOUT3 = 1.5V, Switching Frequency vs Output Current**

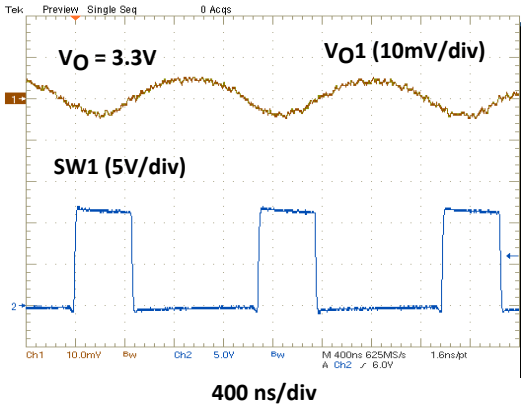



**Figure 26. VOUT1 = 3.3V, Ripple Voltage at IOUT1 = 1.5A**

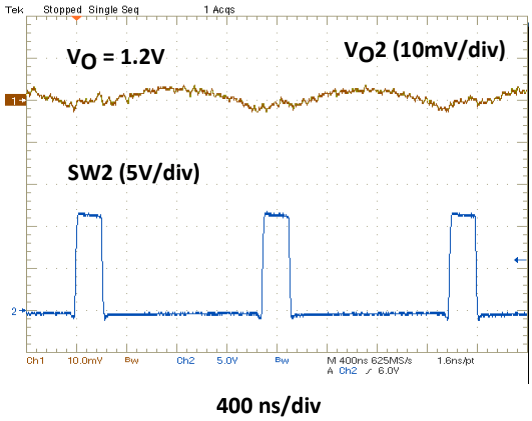



**Figure 27. VOUT2 = 1.2V, Ripple Voltage at IOUT1 = 2.5A**

## TYPICAL CHARACTERISTICS (continued)

VIN = 12 V, $T_A$ = 25°C (unless otherwise noted)

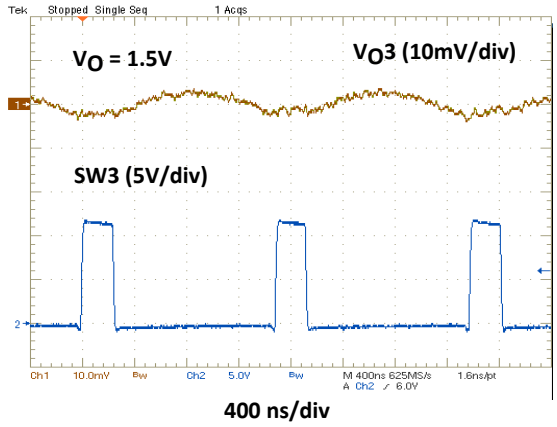



**Figure 28. VOUT3 = 1.2V, Ripple Voltage at IOUT1 = 1.5A**

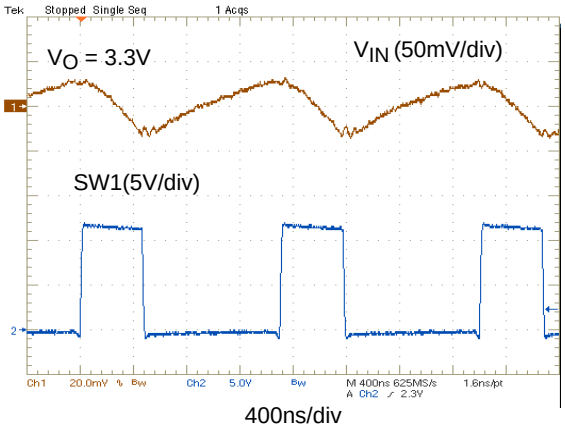



**Figure 29. VOUT1 = 3.3V, VIN Ripple Voltage at IOUT1 = 1.5A**

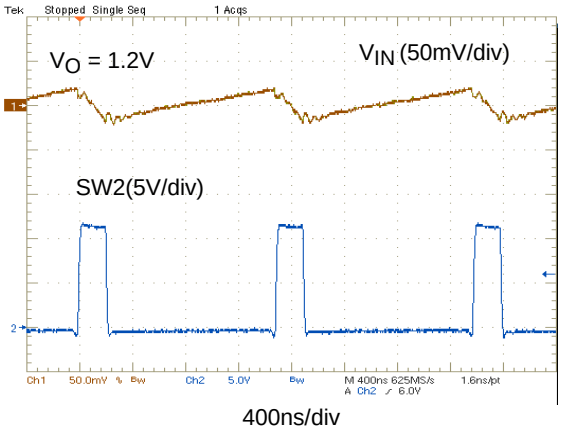



**Figure 30. VOUT2 = 1.2V VIN Ripple at IOUT2 = 2.5A**

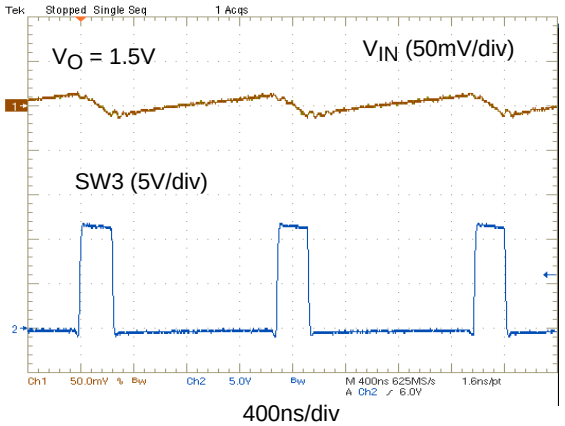



**Figure 31. VOUT3 = 1.5V VIN Ripple at IOUT3 = 1.5A**

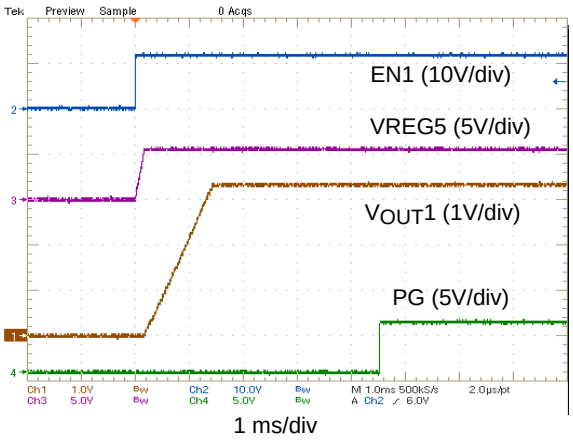



**Figure 32. VOUT1 = 3.3V Soft-Start IOUT1 = 1.5A**

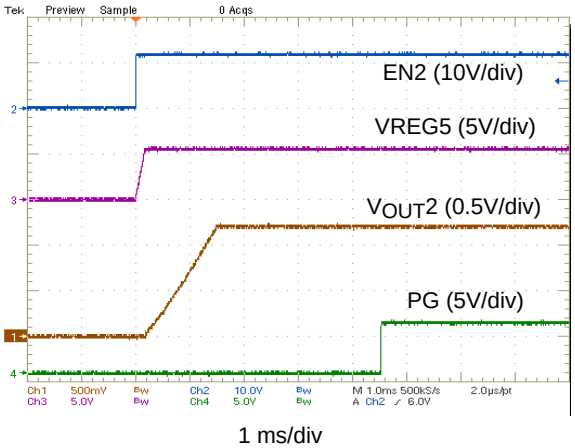



**Figure 33. VOUT2 = 1.2V Soft-Start IOUT2 = 2.5A**

## TYPICAL CHARACTERISTICS (continued)

VIN = 12 V, $T_A$ = 25°C (unless otherwise noted)

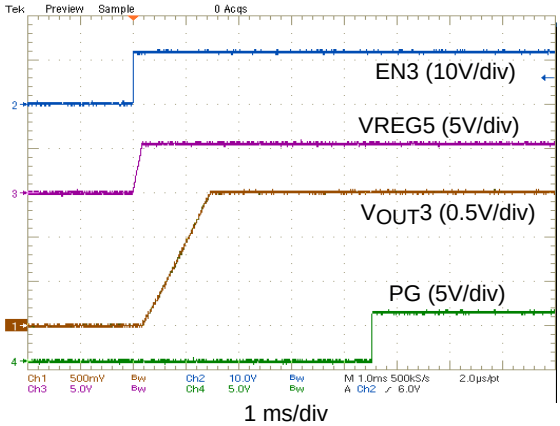



**Figure 34. VOUT3 = 1.5V Soft-Start IOUT3 = 1.5A**

## DESIGN GUIDE

### Step By Step Design Procedure

To begin the design process, you must know a few application parameters:

- Input voltage range
- Output voltage
- Output current

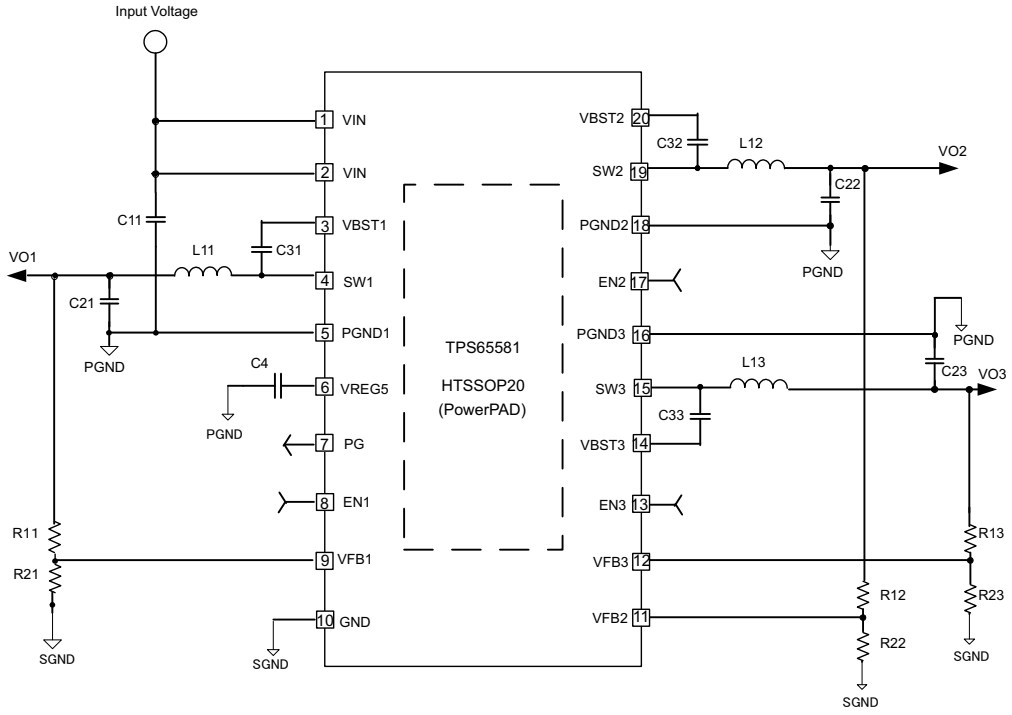



**Figure 35. Schematic Diagram for the Design Example at $V_{IN}$ = 12V**

### Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFBx pin. It is recommended to use 1% tolerance or better divider resistors. Start by using Equation 2 to calculate $V_{Ox}$.

To improve the efficiency at very light loads consider using larger value resistors, but too high resistance values will be more susceptible to noise and voltage errors due to the VFBx input current will be more noticeable.

$$V_{OX} = 0.764 \times \left(1 + \frac{R1x}{R2x}\right) \quad (2)$$

### Output Filter Selection

The output filter used with the TPS65581 is an LC circuit. This LC filter has double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L_{1X} \times C_{2X}}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS65581. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. Advanced D-CAP2™ introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of Equation 3 is located below the high frequency zero but close enough that the phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement, use the values recommended in Table 1.

**Table 1. Recommended Component Values**

| OUTPUT VOLTAGE (V) | R1x (kΩ) | R2x (kΩ) | L1x (µH) | C2x (µF) |
|---|---|---|---|---|
| 1 | 0.68 | 2.2 | 1.5 to 3.3 | 22 - 68 |
| 1.05 | 0.82 | 2.2 | 1.5 to 3.3 | 22 - 68 |
| 1.2 | 1.27 | 2.2 | 1.5 to 3.3 | 22 - 68 |
| 1.5 | 2.15 | 2.2 | 1.5 to 3.3 | 22 - 68 |
| 1.8 | 3.00 | 2.2 | 1.5 to 3.3 | 22 - 68 |
| 2.5 | 4.98 | 2.2 | 2.2 to 4.7 | 22 - 68 |
| 3.3 | 7.36 | 2.2 | 2.2 to 4.7 | 22 - 68 |
| 5 | 12.4 | 2.2 | 2.2 to 4.7 | 22 - 68 |
| 6.5 | 16.5 | 2.2 | 2.2 to 4.7 | 22 - 68 |

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 4, Equation 5 and Equation 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

For the calculations, use 700 kHz as the switching frequency, $f_{SW}$. Make sure the chosen inductor is rated for the peak current of Equation 5 and the RMS current of Equation 6.

$$\Delta I_{L1X} = \frac{V_{OX}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OX}}{L1x \times f_{SW}} \quad (4)$$

$$I_{L1XPEAK} = I_{OX} + \frac{\Delta I_{L1X}}{2} \quad (5)$$

$$I_{L1X(RMS)} = \sqrt{I_{OX}^2 + \frac{1}{12}\Delta I_{L1X}^2} \quad (6)$$

For the above design example, the calculated peak current is 2.46 A and the calculated RMS current is 2.02 A. for Vo1. The inductor used is a TDK CLF7045-1R5N with a rated current of 7.3 A based on the inductance change and of 4.9A based on the temperature rise.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS65581 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 22µF to 68µF. Use Equation 7 to determine the required RMS current rating for the output capacitor(s).

$$I_{C2X(RMS)} = \frac{V_{OX} \times (V_{IN} - V_{OX})}{\sqrt{12} \times V_{IN} \times L_{IX} \times f_{SW}} \quad (7)$$

For this design two TDK C3216X5R0J226M 22 µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.19A and each output capacitor is rated for 4 A.

## Input Capacitor Selection

The TPS65581 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10µF x 2 is recommended for the decoupling capacitor. Accordingly, 0.1 µF ceramic capacitors from pin 1 to ground is recommended to improve the stability and reduce the SWx node overshoots. The capacitor voltage rating needs to be greater than the maximum input voltage.

## Bootstrap Capacitor Selection

A 0.1 µF ceramic capacitors must be connected between the VBSTx and SWx pins for proper operation. It is recommended to use ceramic capacitors with a dielectric of X5R or better.

## VREG5 Capacitor Selection

A 1 µF ceramic capacitor must be connected between the VREG5 and GND pins for proper operation. It is recommended to use a ceramic capacitor with a dielectric of X5R or better.

## Thermal Information

This 20-pin PWP package incorporates an exposed thermal pad that is designed to be directly to an external heartsick. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heartsick. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heartsick structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the exposed thermal pad and how to use the advantage of its heat dissipating abilities, refer to the Technical Brief, *PowerPAD™ Thermally Enhanced Package*, Texas Instruments Literature No. SLMA002 and Application Brief, *PowerPAD™ Made Easy*, Texas Instruments Literature No. SLMA004.

The exposed thermal pad dimensions for this package are shown in the following illustration.

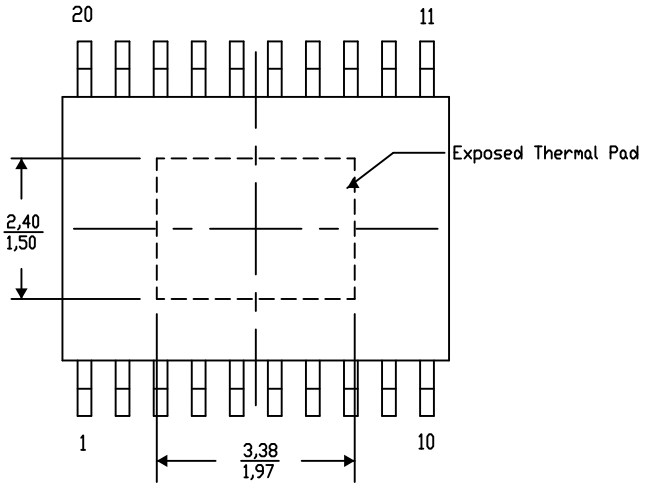



**Figure 36. Thermal Pad Dimensions**

## Layout Considerations

1. Keep the input current loop as small as possible. And avoid the input switching current through the thermal pad.
2. Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin of the device.
3. Keep analog and non-switching components away from switching components.
4. Make a single point connection from the signal ground to power ground.
5. Do not allow switching currents to flow under the device.
6. Keep the pattern lines for VIN and PGND broad.
7. Exposed pad of device must be connected to PGND with solder.
8. VREG5 capacitor should be placed near the device, and connected to PGND.
9. Output capacitors should be connected with a broad pattern to the PGND.
10. Voltage feedback loops should be as short as possible, and preferably with ground shield.
11. Kelvin connections should be brought from the output to the feedback pin of the device.
12. Providing sufficient vias is preferable for VIN, SW and PGND connection.
13. PCB pattern for VIN, SW, and PGND should be as broad as possible.
14. VIN Capacitor should be placed as near as possible to the device.

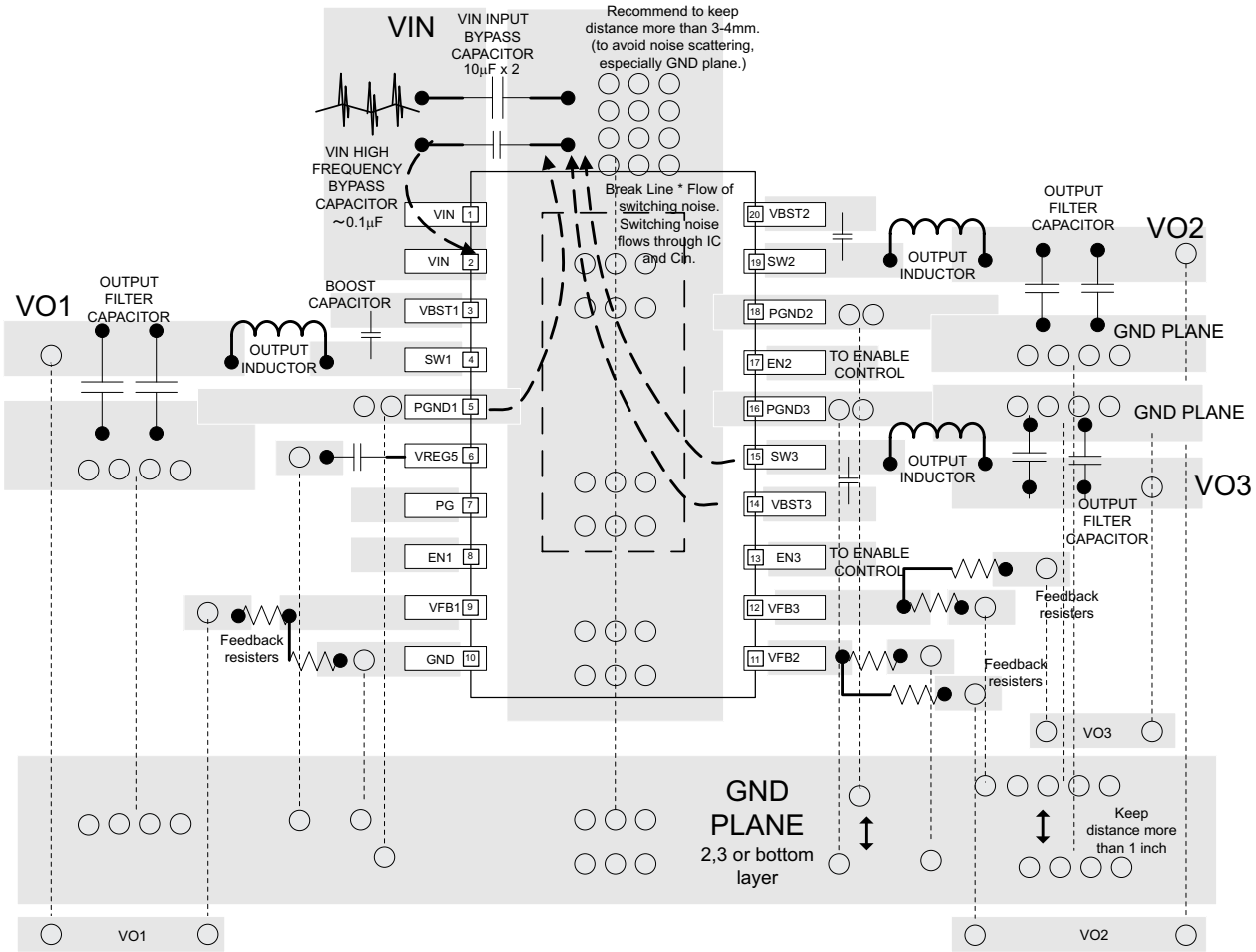



**Figure 37. TPS65581 Layout**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS65581PWP | Active | Production | HTSSOP (PWP) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TPS65581 |
| TPS65581PWP.A | Active | Production | HTSSOP (PWP) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TPS65581 |
| TPS65581PWPR | Active | Production | HTSSOP (PWP) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TPS65581 |
| TPS65581PWPR.A | Active | Production | HTSSOP (PWP) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TPS65581 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

# GENERIC PACKAGE VIEW

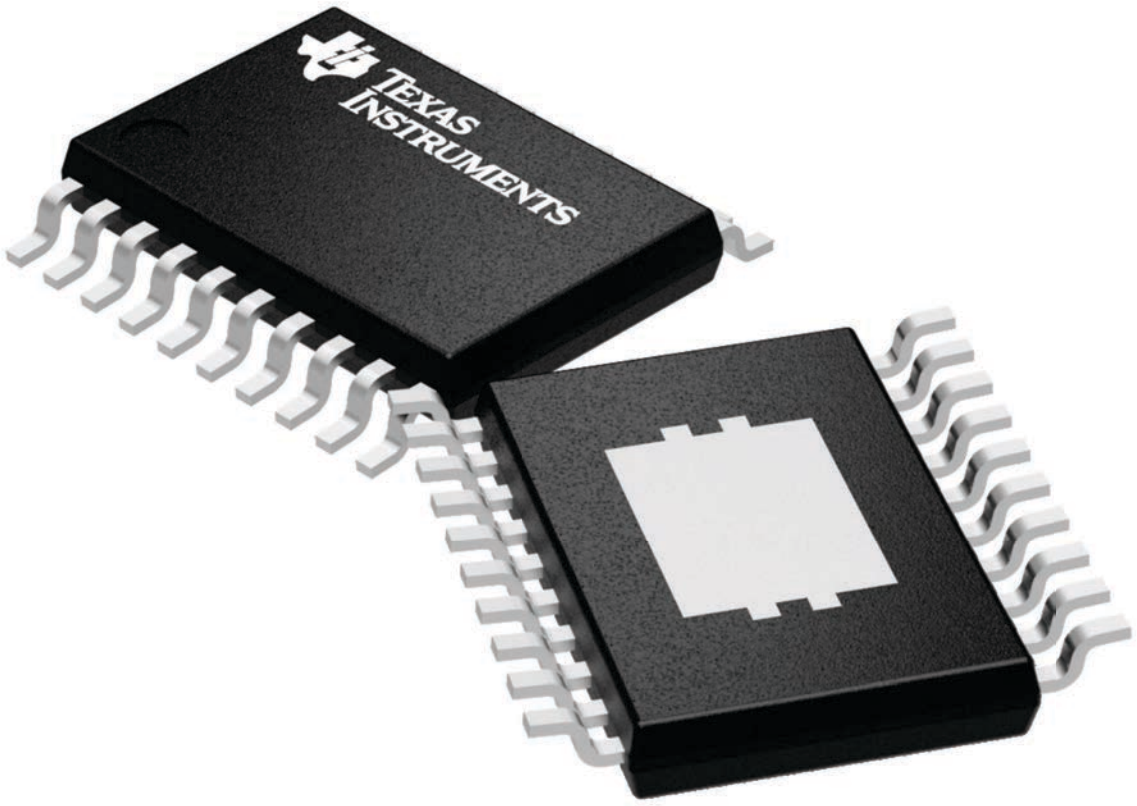
## PWP 20

## HTSSOP - 1.2 mm max height

**6.5 x 4.4, 0.65 mm pitch**

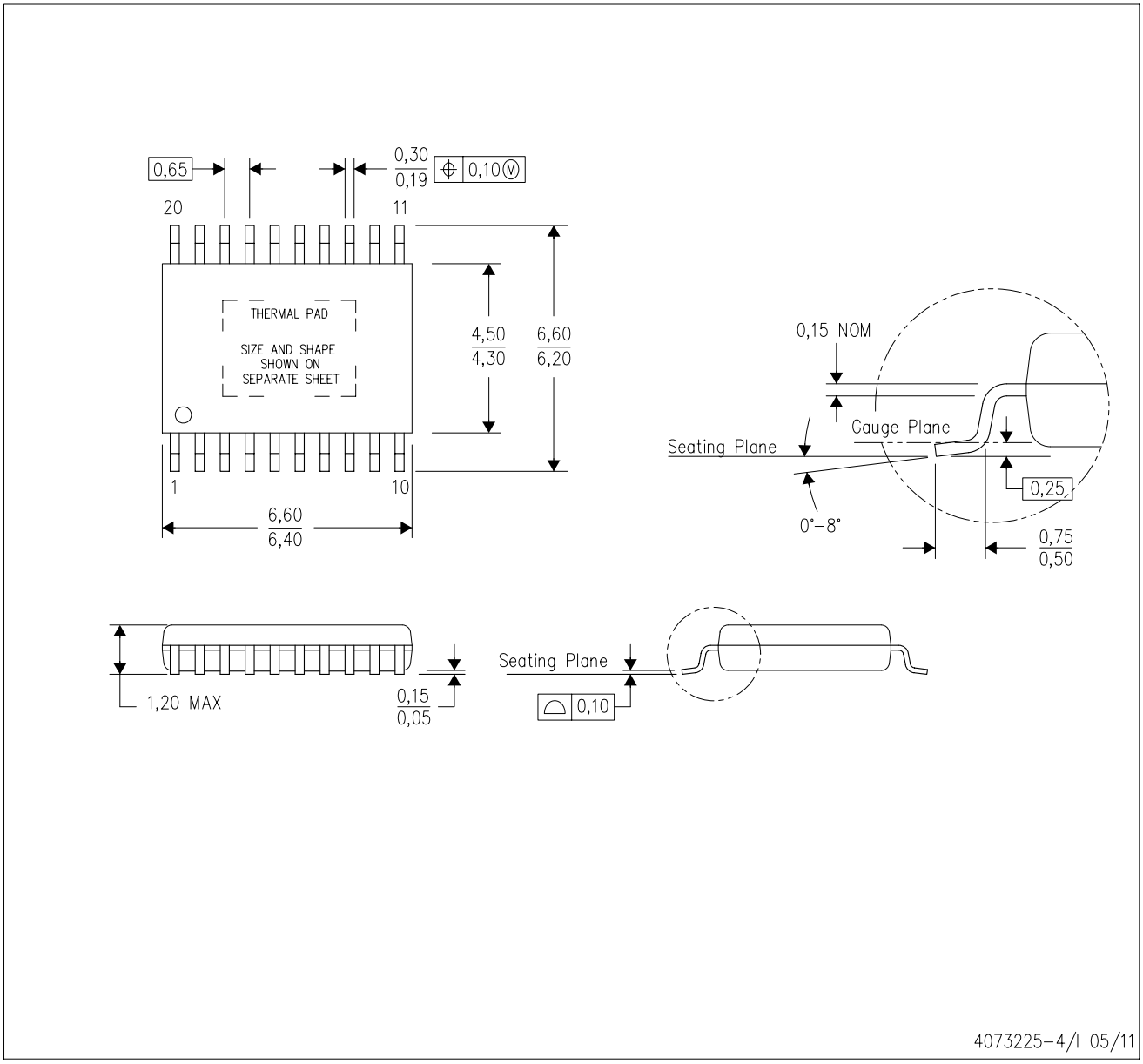
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4224669/A

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

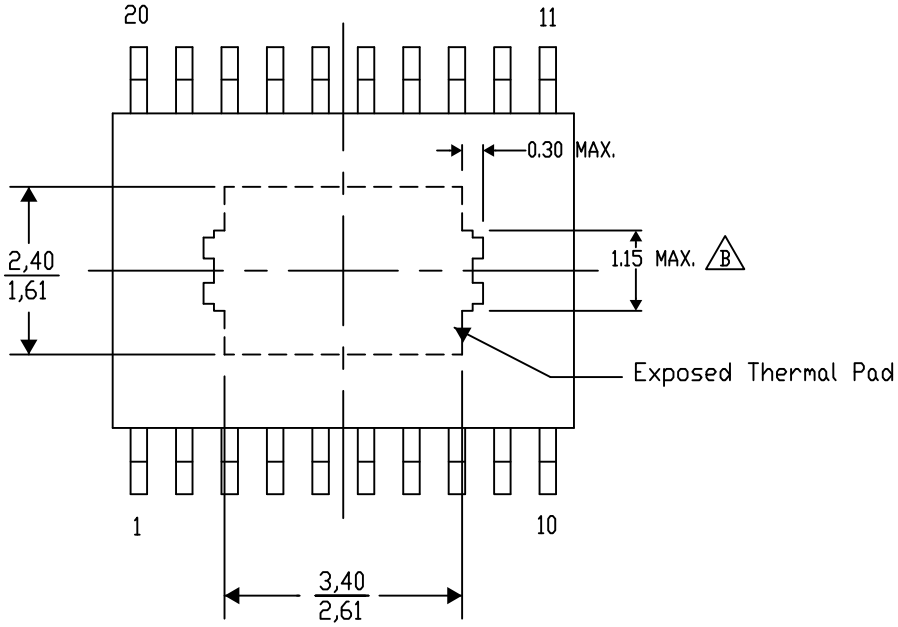
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

Exposed Thermal Pad Dimensions

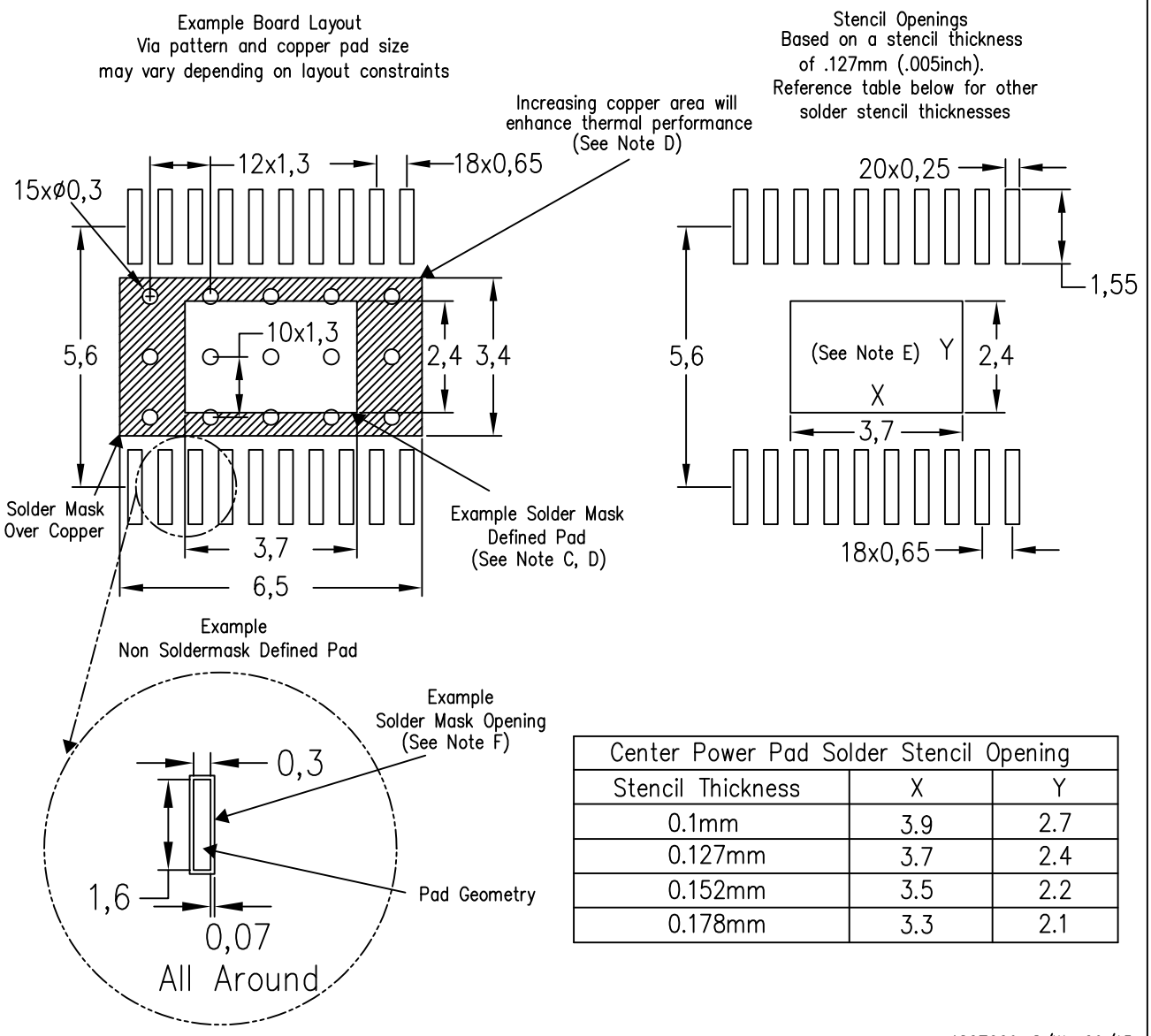
4206332–15/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

## PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 3.9 | 2.7 |
| 0.127mm | 3.7 | 2.4 |
| 0.152mm | 3.5 | 2.2 |
| 0.178mm | 3.3 | 2.1 |

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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