具有 I²C 受控 VID 的 4.5V 至 18V 输入电压，6A/3.5A 双路同步降压转换器

查询样片: TPS65276V

特性

- **4.5V** 至 **18V** 的宽输入电压范围
- 对于每个降压转换器，**I²C** 受控 **7** 位 **VID** 可编程输出电压的范围为 **0.68V** 至 **1.95V**，步长为 **10mV**；输出电压也可由电阻分压器设定
- 针对输出电压转换的可编程转换率控制
- 降压转换器 **1** 中高达 **6A** 的最大持续输出电流和降压转换器 **2** 中 **3.5A** 的最大持续输出电流
- 支持标准模式 **(100kHz)** 和快速模式 **(400kHz)** 的 **I²C** 兼容接口
- **I²C** 回读电源正常状态和裸片温度报警
- 脉冲跳跃模式以在轻负载时实现高效率
- 可调开关频率
  由外部电阻器设定的 **200kHz - 1.6MHz**
- 针对每个降压转换器的专用启用和软启动
- 具有简单补偿电路的峰值电流模式控制
- 逐周期过流保护
- **180°** 相移运行可减少输入电容量和电源引入感应噪声
- 过热保护
- 可提供 **32** 引脚耐热增强型散热薄型小外形尺寸封装 **(HTSSOP)(DAP)** 以及 **36** 引脚四方扁平无引线 **(QFN) 6mm x 6mm (RHH)** 封装

应用范围

- 数字电视 **(DTV)**
- 时序控制器 **(TCON)**
- 蓝光播放器 **(BDVD)**
- 机顶盒
- 平板电脑

说明/订购信息

TPS65276V 是一款具有 4.5V 至 18V 宽泛工作输入电压范围的单片双路同步降压转换器，这个电压范围曾包括大多数中间总线关闭电压为 5V，9V，12V 或 15V 的电源总线或电池。 这个具有恒定频率峰值电流模式控制的转换器被设计用来简化它的应用，与此同时，能够使设计人员根据目标应用来优化他们的使用方法。

TPS65276V 中的每个降压转换器具有可被用来设定初始启动电压的外部反馈电阻器。 针对此启动选项的反馈电压基准为 0.6V。一旦通过 I²C 更新 VID 数模转换器 (DAC)，此降压转换器将反馈电阻器从外部切换为内部。 可使用 I²C 受控 7 位 VID 在 0.68V 至 1.95V 的范围内设定每个降压转换器的输出电压（步长 10mV）。

TPS65276V 中的每个降压转换器可由 I²C 控制启用/禁用输出电压、设置脉冲跳跃模式以及读取电源正常状态和裸片温度报警。

可使用一个外部电阻器将此转换器的开关频率设定在 200kHz 至 1.6MHz 之间。 2 个转换器具有 180° 相移时钟信号。

当 I²C 接口不可用时，TPS65276V 特有专用使能引脚。 独立软启动引脚提供加电可编程性中的灵活性。 恒定频率峰值电流模式控制简化了补偿并提供快速瞬态响应。 逐周期过流保护和断续模式操作在短路或者过载故障条件下限制 MOSFET 功率耗散。 低侧反向过流保护还能够防止过多吸收电流损坏转换器。

TPS65273V 还特有一个轻负载脉冲跳跃模式 (PSM)，此模式可由 I²C 或 MODE 引脚配置进行控制。 PSM 模式可减少系统输入电源上的功率损耗以便在轻负载时实现高效率。

TPS65273V 采用一个 32 引脚耐热增强型 HTSSOP (DAP) 封装和 36 引脚 QFN 6mm x 6mm (RHH) 封装。

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	32-pin HTSSOP (DAP)	TPS65276VDAPR	TPS65276V
	36-pin QFN (RHH)	TPS65276VRHHR	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

TYPICAL APPLICATION

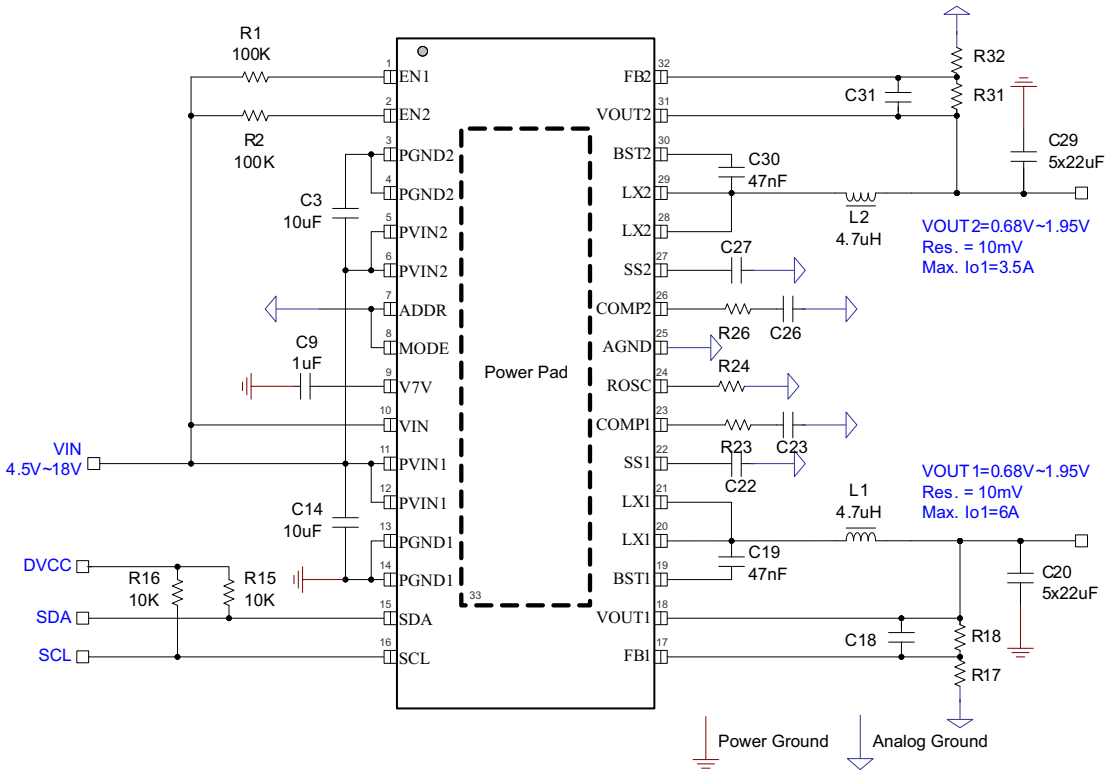
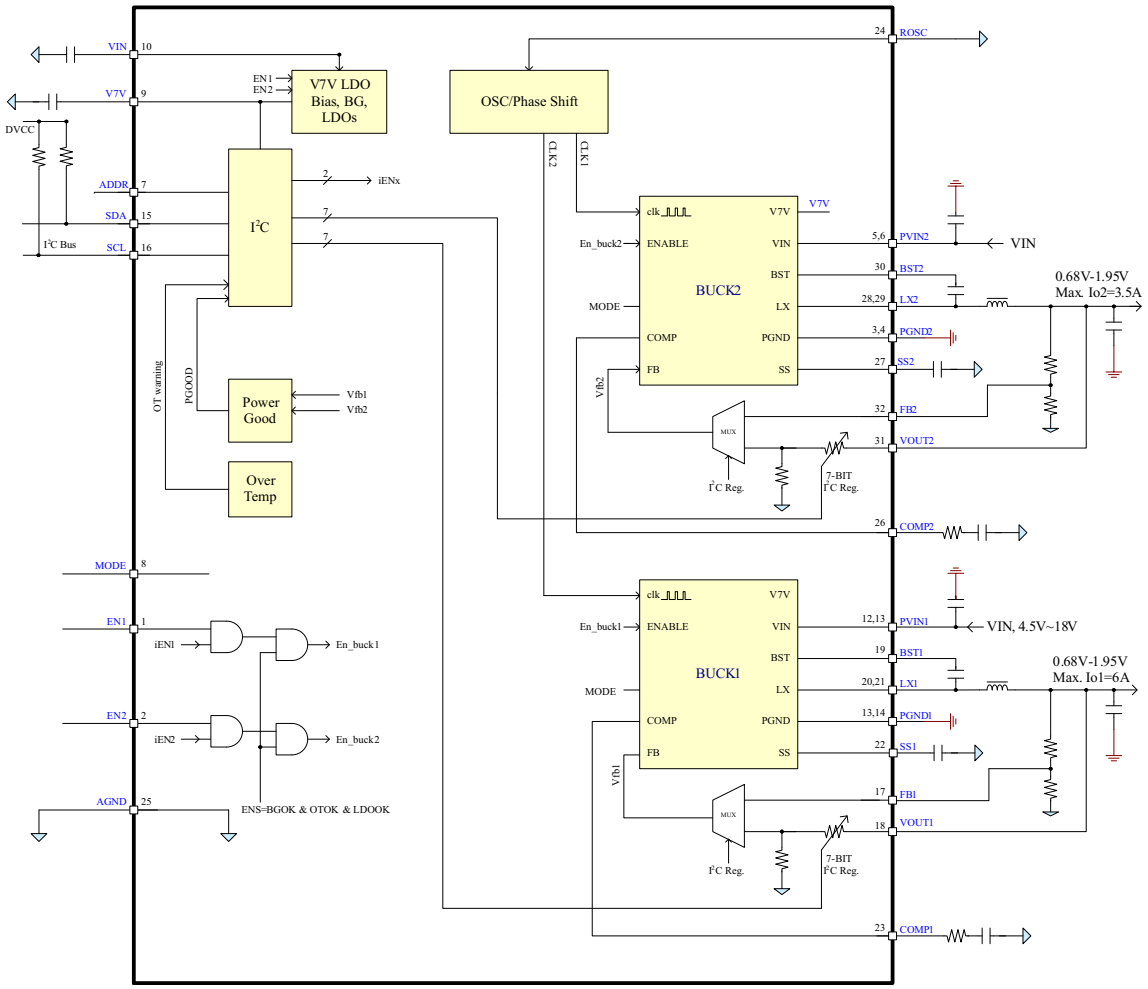


Figure 1. Dual Mode Operation to Deliver 6 A at Buck 1 and 3.5 A at Buck 2

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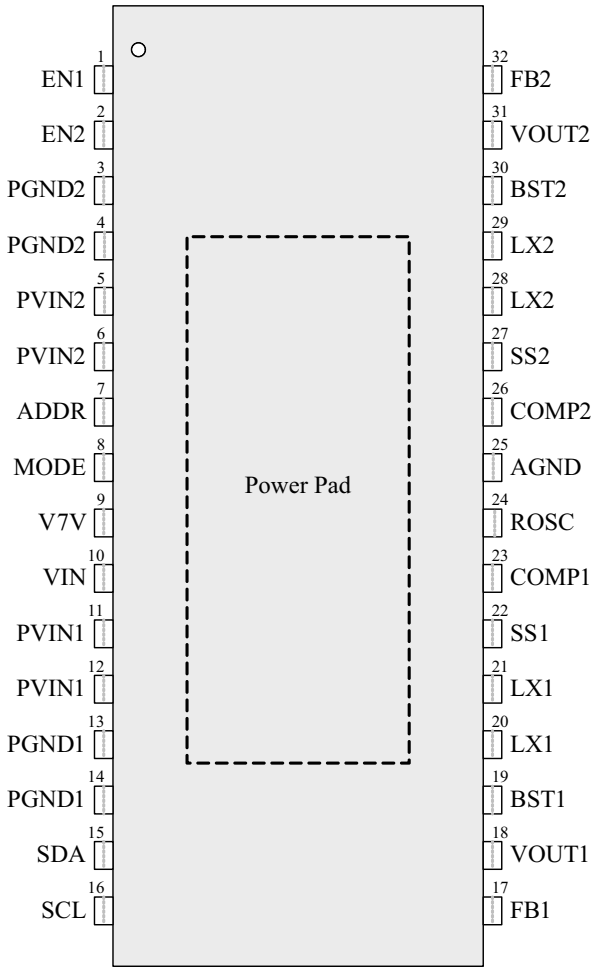
FUNCTIONAL BLOCK DIAGRAM



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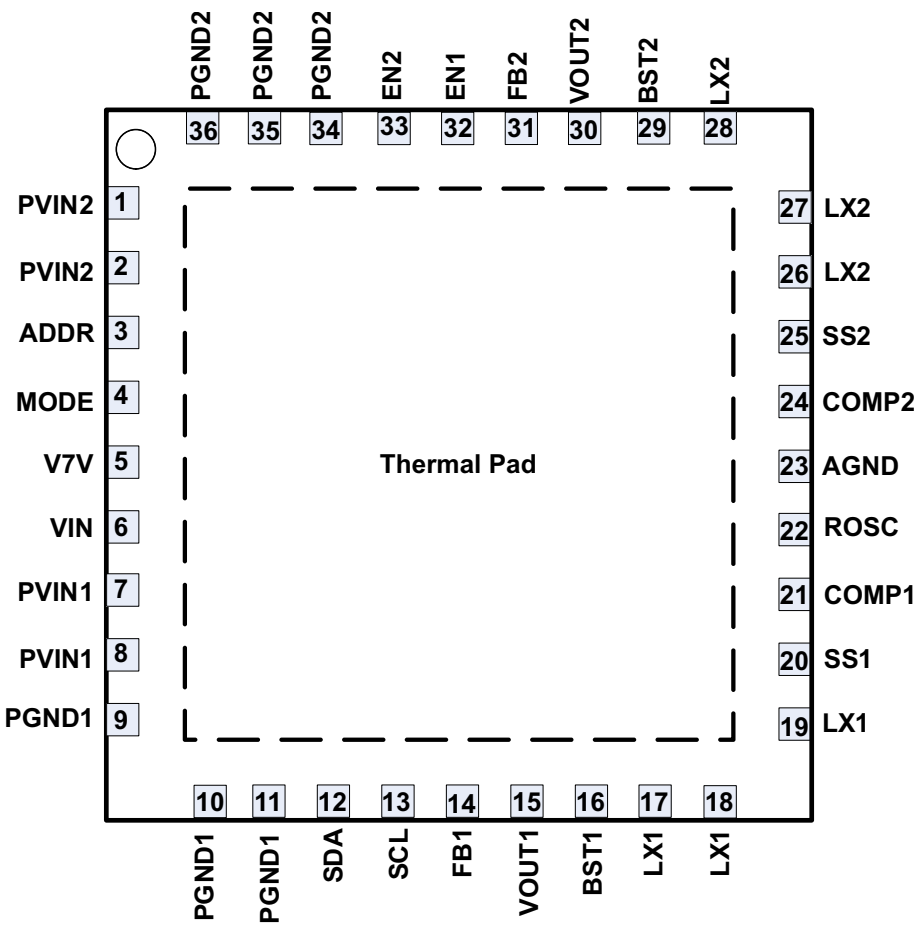
PIN OUT

DAP PACKAGE
(TOP VIEW)



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RHH PACKAGE
(TOP VIEW)



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TERMINAL FUNCTIONS

NAME	NO. (HTSSOP)	NO. (QFN)	DESCRIPTION
EN1, EN2	1, 2	32, 33	Enable pin. Adjust the input under-voltage lockout with two resistors.
PGND2	3, 4	34, 35, 36	Power ground of Buck 2, place the input capacitor's ground pin as close as possible to this pin.
PVIN2	5, 6	1, 2	Power input. Input power supply to the power switches of the power converter 2.
ADDR	7	3	I^2C address configuration pin. Connect this pin to low, high or leave it open to select different I^2C slave address.
MODE	8	4	Operation mode control pin. Connect this pin to ground to choose forced PWM mode without current sharing; leave the pin open for pulse skipping mode (PSM) operation at light load condition; connect this pin to V7V to choose forced PWM mode and current sharing with paralleling two bucks.
V7V	9	5	Internal low-drop linear regulator (LDO) output to power internal driver and control circuits. Decouple this pin to power ground with a minimum 1-µF ceramic capacitor. Output regulates to typical 6.3 V for optimal conduction on-resistances of internal power MOSFETs. In PCB design, the power ground and analog ground should have one-point common connection at the (-) terminal of V7V bypass capacitor. If VIN is lower than 6.3 V, V7V will be slightly lower than VIN.
VIN	10	6	Power supply of the internal LDO and controllers
PVIN1	11, 12	7, 8	Power input. Input power supply to the power switches of the power converter 1.
PGND1	13, 14	9, 10, 11	Power ground of Buck 1, place the input capacitor's ground pin as close as possible to this pin.
SDA	15	12	I^2C interface data pin
SCL	16	13	I^2C interface clock pin
FB1	17	14	Feedback sensing pin for the external feedback resistors in Buck 1. Before I^2C controlled VID selection is enabled, an external resistor divider connects to this pin to pre-set the output voltage.
VOUT1	18	15	Buck 1 output voltage sensing pin; When I^2C controlled VID selection is enabled, output voltage can be programmed from 0.68 V to 1.95 V with 10-mV steps. In current sharing application, this pin is the output voltage sensing pin.
BST1	19	16	Add a bootstrap capacitor between BST1 and LX1. The voltage on this capacitor carries the gate drive voltage for the high-side MOSFET.
LX1	20, 21	17, 18, 19	Switching node of Buck 1
SS1	22, 27	20, 25	Soft-start and voltage tracking in Buck 1. An external capacitor connected to this pin sets the internal voltage reference rise time. Since the voltage on this pin overrides the internal reference, it can be used for tracking and sequencing. In current sharing application, this pin serves as the soft-start pin.
COMP1	23	21	Error amplifier output and loop compensation pin for Buck 1. Connect frequency compensation to this pin; In current sharing application, this pin serves as the compensation pin.
ROSC	24	22	Oscillator frequency programmable pin. Connect an external resistor to set the switching frequency. When connected to an external clock, the internal oscillator synchronizes to the external clock.
AGND	25	23	Analog ground of the controllers
COMP2	26	24	Error amplifier output and loop compensation pin for Buck 2. Connect frequency compensation to this pin. In current sharing application, connect this pin to ground.
SS2	27	25	Soft-start and voltage tracking in Buck 2. An external capacitor connected to this pin sets the internal voltage reference rise time. Since the voltage on this pin overrides the internal reference, it can be used for tracking and power sequencing. In current sharing application, connect this pin to ground.
LX2	28, 29	26, 27, 28	Switching nodes

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TERMINAL FUNCTIONS (continued)

NAME	NO. (HTSSOP)	NO. (QFN)	DESCRIPTION
BST2	30	29	Add a bootstrap capacitor between BST2 and LX2. The voltage on this capacitor carries the gate drive voltage for the high-side MOSFET of Buck 2.
VOUT2	31	30	Buck 2 output voltage sensing pin; When I^2C controlled VID selection is enabled, output voltage can be programmed from 0.68 V to 1.95 V with 10-mV steps. In current sharing application, connect this pin to the ground.
FB2	32	31	Feedback sensing pin for the external feedback resistors in Buck 2. Before I^2C controlled VID selection is enabled, an external resistor divider connects to this pin to pre-set the output voltage.
Exposed Thermal Pad	33	37	Exposed thermal pad of the package. Connect to the power ground. Always solder thermal pad to the board, and have as many vias as possible on the PCB to enhance power dissipation. There is no electric signal down bonded to the thermal pad inside the IC package.

ABSOLUTE MAXIMUM RATINGS (1)

over operating free-air temperature range (unless otherwise noted)

	Voltage range at VIN, PVIN1,PVIN2	–0.3 to 20	V
	Voltage range at LX1, LX2 (maximum withstand voltage transient < 20 ns)	–4.5 to 20	V
	Voltage at BST1, BST2, referenced to LX1, LX2 pin	–0.3 to 7	V
	Voltage at V7V, EN1, EN2, VOUT1, VOUT2, MODE	–0.3 to 7	V
	Voltage at SS1, SS2, FB1, FB2, COMP1, COMP2	–0.3 to 3	V
	Voltage at SDA, SCL, ADDR, EN1, EN2, ROSC	–0.3 to 7	
	Voltage at AGND, PGND1, PGND2	–0.3 to 0.3	V
T_J	Operating virtual junction temperature range	–40 to 150	°C
T_{STG}	Storage temperature range	–55 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC		TPS65276V		UNITS
		DAP	RHH	
		32 PINS	36 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(1)	35	30.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(2)	17.7	18.8	
θ_{JB}	Junction-to-board thermal resistance(3)	19	6	
ψ_{JT}	Junction-to-top characterization parameter(4)	0.5	0.2	
ψ_{JB}	Junction-to-board characterization parameter(5)	18.9	6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(6)	1.3	0.7	

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Input operating voltage	4.5		18	V
T_A	Ambient temperature	–40		85	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MIN	MAX	UNIT
Human body model (HBM)	1000		V
Charge device model (CDM)	250		V

ELECTRICAL CHARACTERISTICS

T_J = 25°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Input Voltage range	VIN1 and VIN2	4.5		18	V
IDD_{SDN}	Shutdown supply current	EN1 = EN2 = low		10		µA
IDD_{Q_NSW}	Switching quiescent current with no load at DCDC output	EN1 = EN2 = 3.3 V Without bucks switching		1.2		mA
IDD_{Q_SW}	Switching quiescent current with no load at DCDC output, Buck switching	EN1 = EN2 = 3.3 V With bucks switching		10		mA
UVLO	V_{IN} under voltage lockout	Rising V_{IN}		4.25	4.50	V
		Falling V_{IN}	3.5	3.75		
		Hysteresis		0.5		
V_{7V}	6.3 V LDO	V_{7V} load current = 0 A, V_{IN} = 12 V	6.10	6.3	6.5	V
I_{OCP_V7V}	Current limit of V7V LDO			200		mA
ENABLE						
V_{ENR}	Enable threshold			1.21	1.26	V
V_{ENF}	Enable threshold		1.10	1.17		V
I_{ENR}	Enable Input current	EN = 1 V		3		µA
I_{ENF}	Enable hysteresis current	EN = 1.5 V		3		µA
OSCILLATOR						
F_{SW}	Switching frequency		200		1600	kHz
		R_{OSC} = 100 kΩ (1%)	340	400	460	
T_{SYNC_w}	Clock sync minimum pulse width			20		ns
V_{SYNC_HI}	Clock sync high threshold				2	V
V_{SYNC_LO}	Clock sync low threshold		0.8			V
V_{SYNC_D}	Clock falling edge to LX rising edge delay			66		ns
F_{SYNC}	Clock sync frequency range		200		1600	kHz

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ELECTRICAL CHARACTERISTICS (continued)

T_J = 25°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BUCK 1, BUCK 2 CONVERTERS						
$V_{ref(min)}$	Voltage reference	0 A < I_{OUT1} < 6 A, 0 A < I_{OUT2} < 3.5 A	0.594	0.6	0.606	V
$V_{OUT1,2}$	Output voltage step size (VID 0x00 – 0x7F)		8	10	12	mV
$V_{LINEREG3}$	Line regulation-DC	I_{OUT} = 2 A		0.5		%/V
$V_{LOADREG3}$	Load regulation-DC	I_{OUT} = (10-90%) x I_{OUT_max}		0.5		%/A
G_{m_EA3}	Error amplifier trans-conductance	-2 µA < I_{COMP} < 2 µA		1350		µs
G_{m_SRC3}	COMP voltage to inductor current Gm	I_{LX} = 0.5 A		10		A/V
I_{SSx}	Soft-start pin charging current	SS1, SS2		6		µA
I_{LIMIT1}	Buck 1 peak inductor current limit			8		A
I_{LIMIT2}	Buck 2 peak inductor current limit			5		A
$I_{LIMITLSx}$	Low side sinking current limit			-2.6		A
R_{dsonx_HS}	On resistance of high side FET	V7V = 6.3 V		31		mΩ
R_{dsonx_LS}	On resistance of low side FET	V_{IN} = 12 V		23		mΩ
T_{minon}	Minimum on time			94		ns
V_{bootUV}	Boot-LX UVLO			2.1	3	V
$T_{hiccupwait}$	Hiccup wait time			512		cycles
T_{hiccup_re}	Hiccup time before re-start			16384		cycles
I²C READ BACK FAULT STATUS						
V_{PGOOD}	PGOOD trip levels	Feedback lower voltage rising (with respect to 0.6 V)		94		%
		Feedback lower voltage falling (with respect to 0.6 V)		92.5		
		Feedback upper voltage rising (with respect to 0.6 V)		107.5		
		Feedback upper voltage falling (with respect to 0.6 V)		105.5		
T_{warn}	Temperature warning threshold			125		°C
THERMAL SHUTDOWN						
T_{TRIP}	Thermal protection trip point	Rising temperature		160		°C
T_{HYST}	Thermal protection hysteresis			20		°C
I²C INTERFACE						
	Address	0x60H if ADDR = 0; 0x61H if ADDR = high; 0x62H if ADDR = open				
V_{IH} SDA, SCL	Input high voltage				1.3	V
V_{IL} SDA, SCL	Input low voltage		0.4			V
I_I	Input current	SDA, SCL, V_I = 0.4 V to 4.5 V	-10		10	µA
V_{OL} SDA	SDA output low voltage	SDA open drain, I_{OL} = 4 mA			0.4	V
$f_{(SCL)}$	Maximum SCL clock frequency		400			kHz
t_{BUF}	Bus free time between a STOP and START condition		1.3			µs
t_{HD_STA}	Hold time (Repeated) START condition		0.6			µs
t_{SU_STO}	Setup time for STOP condition		0.6			µs
t_{LOW}	LOW period of the SCL clock		1.3			µs
t_{HIGH}	HIGH period of the SCL clock		0.6			µs
t_{SU_STA}	Setup time for a repeated START condition		0.6			µs

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ELECTRICAL CHARACTERISTICS (continued)

T_J = 25°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SU_DAT}	Data setup time		0.1			µs
t_{HD_DAT}	Data hold time		0		0.9	µs
t_{RCL}	Rise time of SCL signal	Capacitance of one bus line (pF)	$20 + 0.1C_B$		300	ns
t_{RCL1}	Rise time of SCL signal after a repeated START condition and after an acknowledge BIT	Capacitance of one bus line (pF)	$20 + 0.1C_B$		300	ns
t_{FCL}	Fall time of SCL sgnal	Capacitance of one bus line (pF)	$20 + 0.1C_B$		300	ns
t_{RDA}	Rise time of SDA signal	Capacitance of one bus line (pF)	$20 + 0.1C_B$		300	ns
t_{FDA}	Fall time of SDA signal	Capacitance of one bus line(pF)	$20 + 0.1C_B$		300	ns
C_B	Capacitance of one bus line (SCL and SDA)				400	pF

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TYPICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 625 kHz (unless otherwise noted)

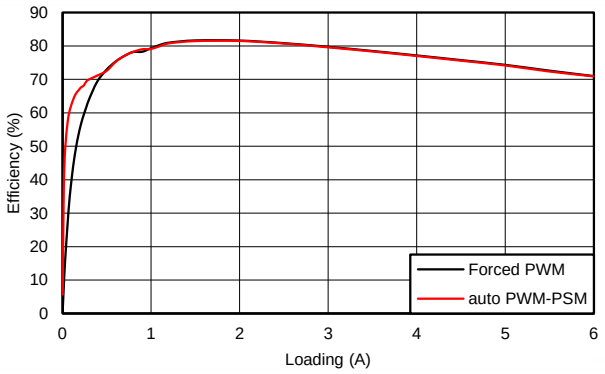


Figure 2. 0.8-V Efficiency
V_{IN} = 12 V, V_{OUT} = 0.8 V

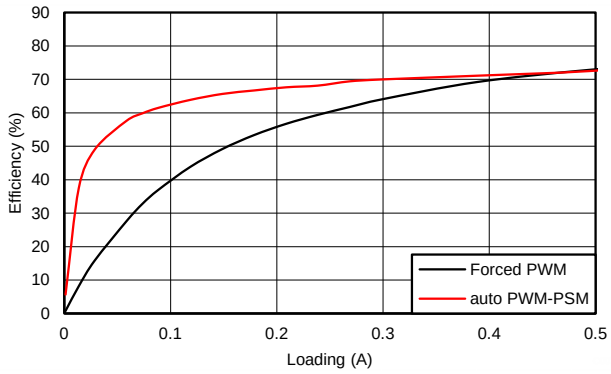


Figure 3. 0.8-V Efficiency, Light Load
V_{IN} = 12 V, V_{OUT} = 0.8 V

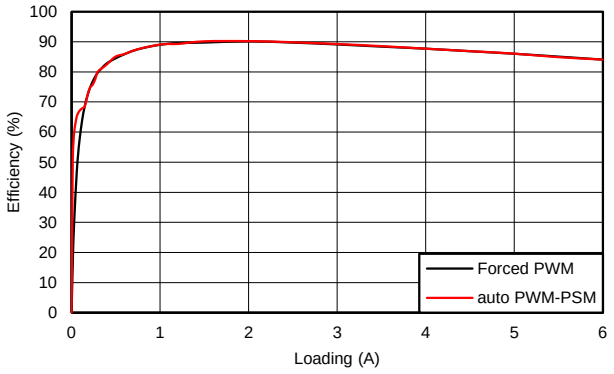


Figure 4. 1.8-V Efficiency
V_{IN} = 12 V, V_{OUT} = 1.8 V

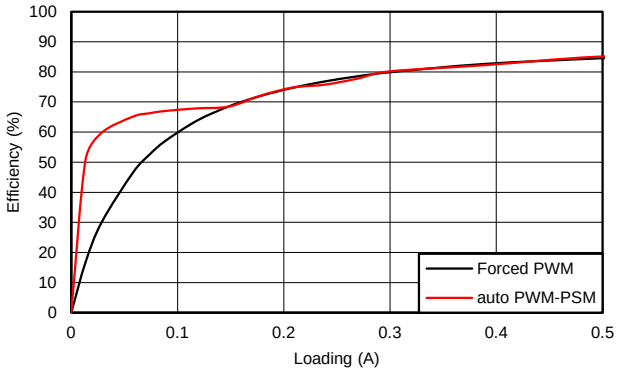


Figure 5. 1.8-V Efficiency, Light Load
V_{IN} = 12 V, V_{OUT} = 1.8 V

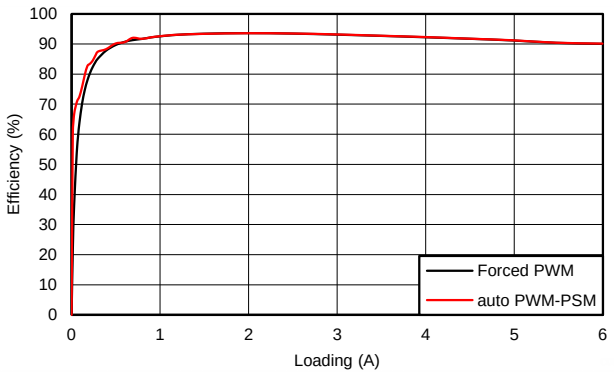


Figure 6. 3.3-V Efficiency
V_{IN} = 12 V, V_{OUT} = 3.3 V

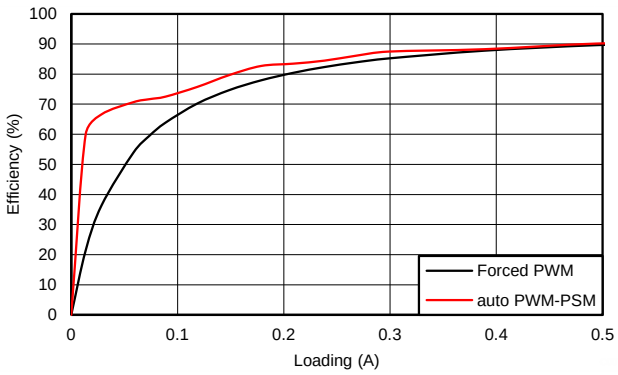


Figure 7. 3.3-V Efficiency, Light Load
V_{IN} = 12 V, V_{OUT} = 3.3 V

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TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 625 kHz (unless otherwise noted)

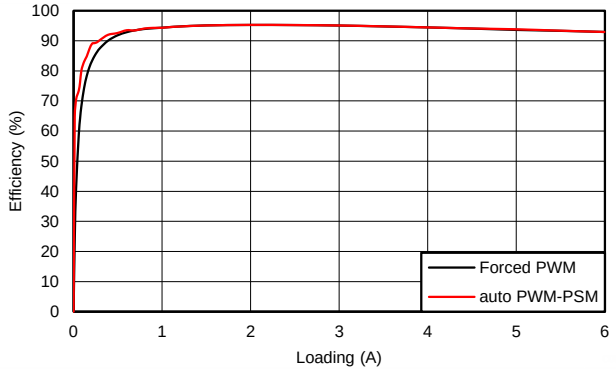


Figure 8. 5-V Efficiency
V_{IN} = 12 V, V_{OUT} = 5 V

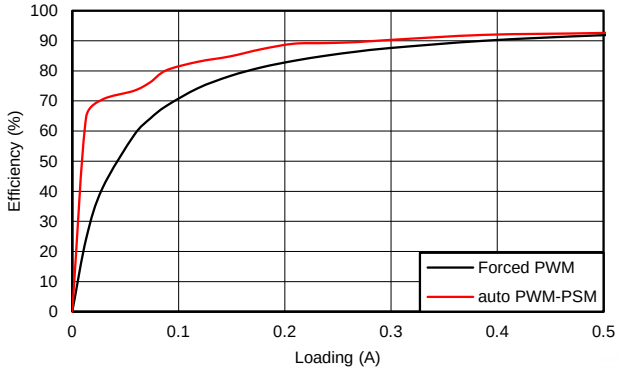


Figure 9. 5-V Efficiency, Light Load
V_{IN} = 12 V, V_{OUT} = 5 V

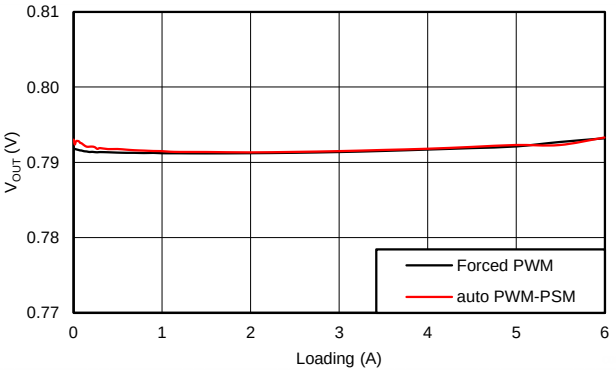


Figure 10. 0.8-V Load Regulation
V_{IN} = 12 V, V_{OUT} = 0.8 V

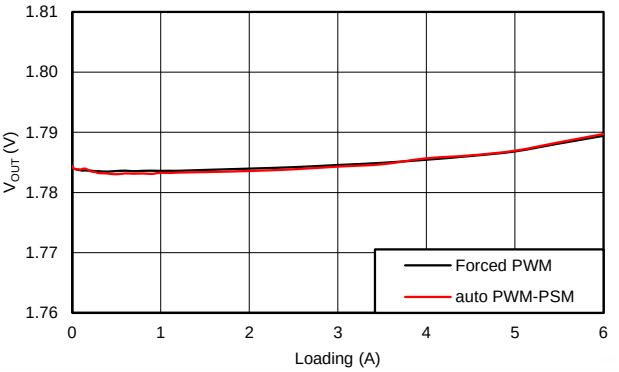


Figure 11. 1.8-V Load Regulation
V_{IN} = 12 V, V_{OUT} = 1.8 V

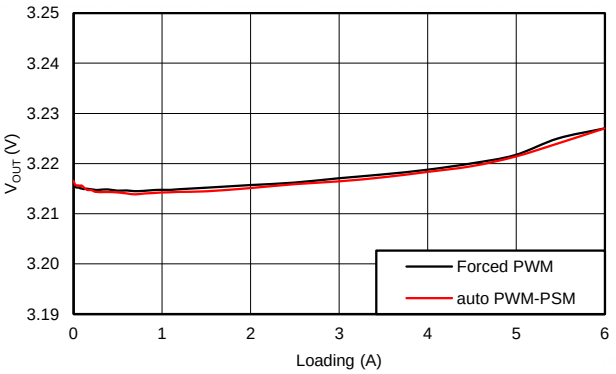


Figure 12. 3.3-V Load Regulation
V_{IN} = 12 V, V_{OUT} = 3.3 V

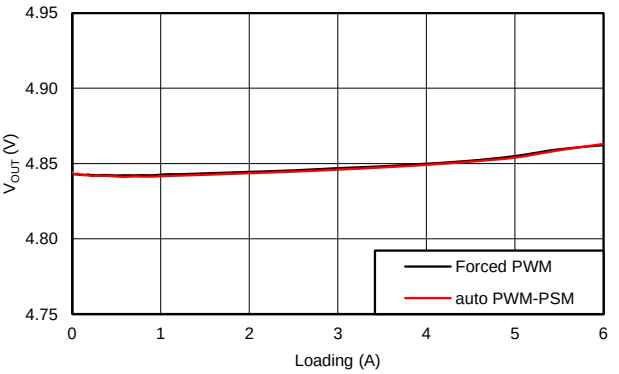


Figure 13. 5-V Load Regulation
V_{IN} = 12 V, V_{OUT} = 5 V

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TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 625 kHz (unless otherwise noted)

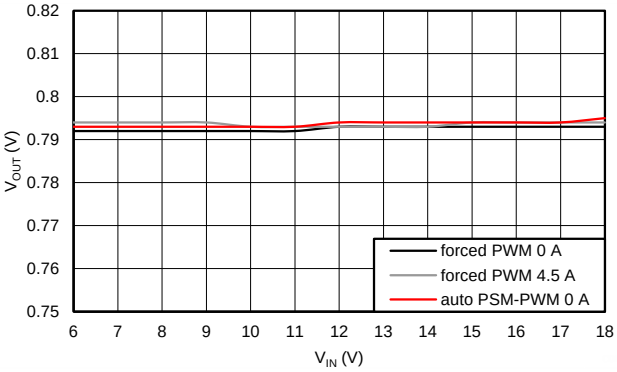


Figure 14. 0.8-V Line Regulation
V_{OUT} = 0.8 V

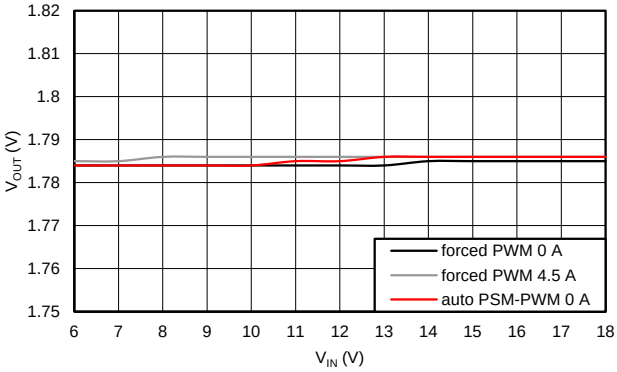


Figure 15. 1.8-V Line Regulation
V_{OUT} = 1.8 V

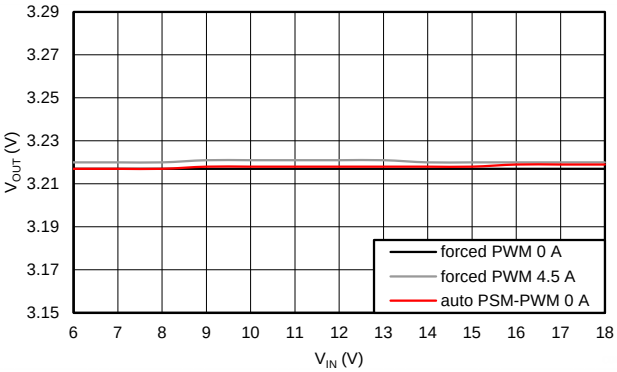


Figure 16. 3.3-V Line Regulation
V_{OUT} = 3.3 V

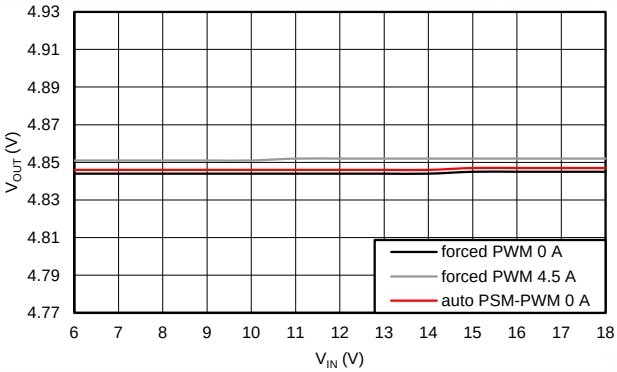


Figure 17. 5-V Line Regulation
V_{OUT} = 5 V

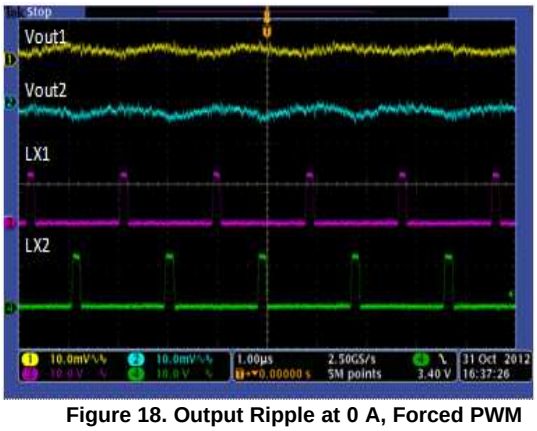


Figure 18. Output Ripple at 0 A, Forced PWM

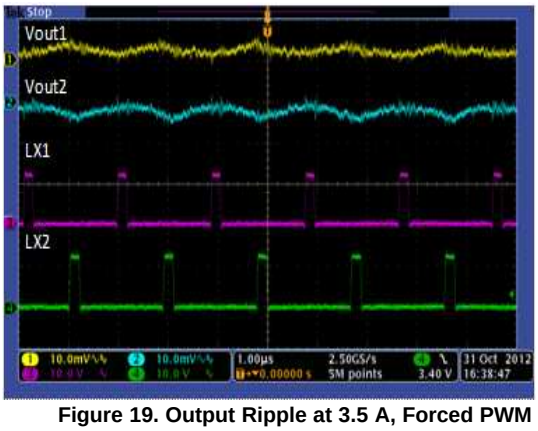


Figure 19. Output Ripple at 3.5 A, Forced PWM

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TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 625 kHz (unless otherwise noted)

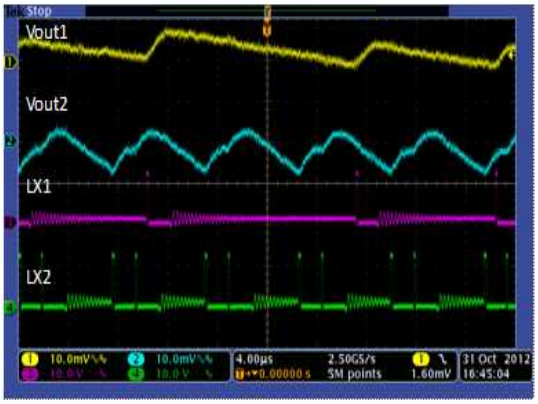


Figure 20. Output Ripple, Buck1 at 0.05 A, Buck 2 at 0.2 A Auto PSM-PWM Mode

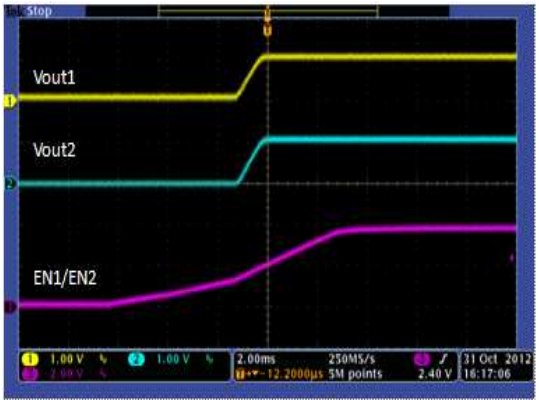


Figure 21. Startup With Enable

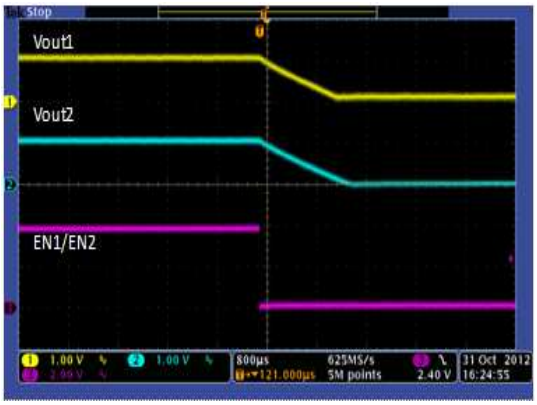


Figure 22. Shutdown With Enable

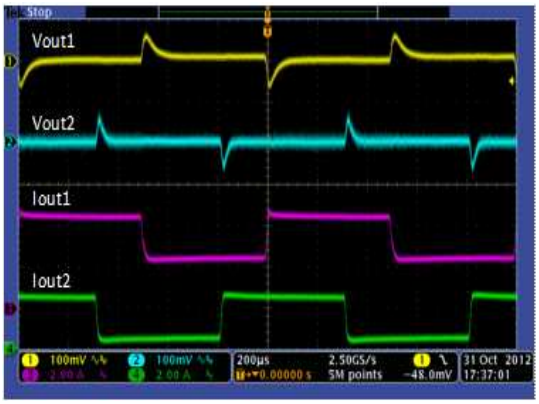


Figure 23. Load Transient, Buck 1 2.5 A - 4.5 A, Buck2 0.5 A - 2.5 A



Figure 24. Load Transient, Buck 1 (0.5 A - 2.5 A)

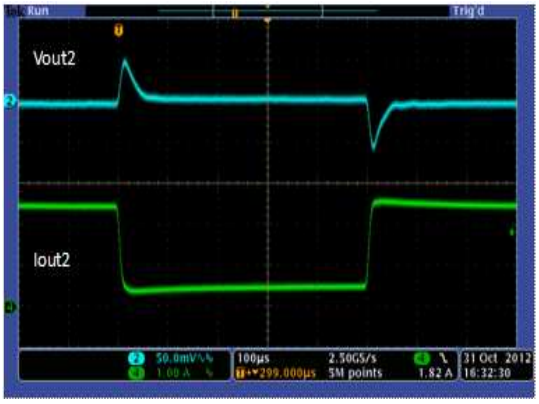


Figure 25. Load Transient, Buck 2 (0.5 A - 2.5 A)

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TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 625 kHz (unless otherwise noted)

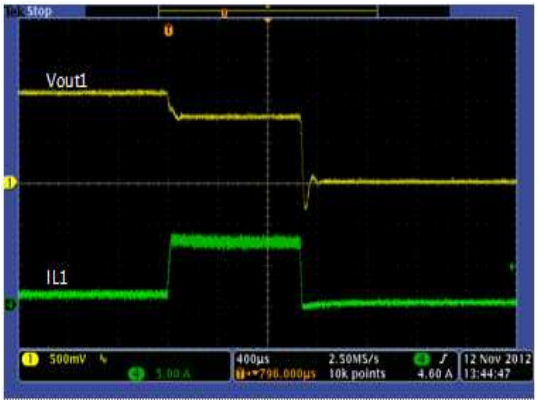


Figure 26. Over Current Protection Buck 1



Figure 27. Hiccup Recover, Buck 1

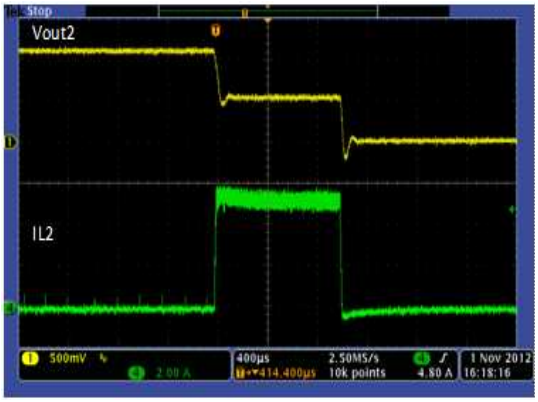


Figure 28. Over Current Protection, Buck 2



Figure 29. Hiccup Recover, Buck 2

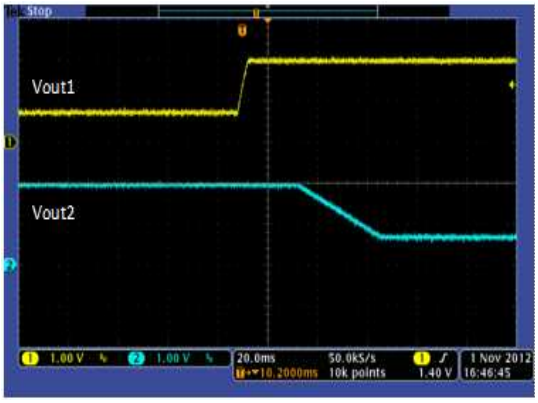


Figure 30. Voltage Change With I²C Control Buck 1, 0.68 V - 1.95 V, SR = 10 mV/16 Tsw, Buck 2, 1.95 V - 0.68 V, SR = 10 mV/128 Tsw



Figure 31. Synchronization at 500 kHz

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OVERVIEW

TPS65276V is a dual 6.3-A/3.5-A output current, synchronous step-down (buck) converter with integrated n-channel MOSFETs. A wide 4.5-V to 18-V input supply range to buck encompasses most intermediate bus voltages operating off 9-V, 12-V or 15-V power bus.

TPS65276V is equipped with I^2C compatible bus for sophisticated control and communication with SoC. With I^2C interface, SoC can enable or disable the power converters, set output voltage and read status registers. The buck regulator has external feedback resistors that can be used for setting the initial start up voltage. The feedback voltage reference for this start-up option is 0.6V. Once the voltage identification VID DAC is updated via the I^2C, output voltage of each channel can be independently programmed with 7 bits VID from 0.68 V to 1.95 V in 10-mV steps. Output voltage transitions begin once the I^2C interface receives the command for GO bit in command registers. In light loading condition, low pulse skipping mode can be I^2C controlled or selected with MODE pin configuration.

TPS65276V implements a constant frequency, peak current mode control which simplifies external frequency compensation. The wide switching frequency of 200 kHz to 1600 kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency can be adjusted with an external resistor to ground on the ROSC pin. The TPS65276V also has an internal phase lock loop (PLL) controlled by the ROSC pin that can be used to synchronize the switching cycle to the falling edge of an external system clock. 180° out-of-phase operation between two channels reduces input filter and power supply induced noise.

TPS65276V has been designed for safe monotonic startup into pre-biased loads. The default start up is when VIN is typically 4.5 V. The EN pin has an internal pull-up current source that can be used to adjust the input voltage under voltage lockout (UVLO) with two external resistors. In addition, the EN pin can be floating for automatically starting up the TPS65276V with the internal pull up current.

The integrated MOSFETs of each channel allow for high efficiency power supply designs with continuous output currents up to 6 A and 3.5 A respectively. The MOSFETs have been sized to optimize efficiency for lower duty cycle applications.

The TPS65276V reduces the external component count by integrating the boot recharge circuit. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BOOT and LX pins. The boot capacitor voltage is monitored by a BOOT to LX UVLO (BOOT-LX UVLO) circuit allowing LX pin to be pulled low to recharge the boot capacitor. The TPS65276V can operate at 100% duty cycle as long as the boot capacitor voltage is higher than the preset BOOT-LX UVLO threshold which is typically 2.1 V.

The TPS65276V has a power good comparator (PWRGD) with hysteresis which monitors the output voltage through internal feedback voltage. I^2C can read the power good status with commanding register.

The SS (soft start/tracking) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor or resistor divider should be coupled to the pin for soft start or critical power supply sequencing requirements.

The TPS65276V is protected from output overvoltage, overload and thermal fault conditions. The TPS65276V minimizes excessive output overvoltage transients by taking advantage of the power good comparator. When the overvoltage comparator is activated, the high-side MOSFET is turned off and prevented from turning on until the internal feedback voltage is lower than 108% of the 0.6-V reference voltage. The TPS65276V implements both high-side MOSFET overload protection and bidirectional low-side MOSFET overload protections which help control the inductor current and avoid current runaway. If the over current condition has lasted for more than the hiccup wait time, the TPS65276V will shut down and re-start after the hiccup time. The TPS65276V also shuts down if the junction temperature is higher than thermal shutdown trip point. When the junction temperature drops 20°C typically below the thermal shutdown trip point, the built-in thermal shutdown hiccup timer is triggered. The TPS65276V will be restarted under control of the soft start circuit automatically after the thermal shutdown hiccup time is over.

Furthermore, if the over-current condition has lasted for more than the hiccup wait time which is programmed for 512 switching cycles, the TPS65276V will shut down itself and re-start after the hiccup time which is set for 16384 cycles. The hiccup mode helps to reduce the device power dissipation under severe over-current conditions.

The TPS65276V operates at any load conditions unless the COMP pin voltage drops below the COMP pin start switching threshold which is typically 0.25 V.

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When PSM mode operation is enabled, the TPS65276V monitors the peak switch current of the high-side MOSFET. Once the peak switch current is lower than typically 1 A, the device stops switching to boost the efficiency until the peak switch current is higher than typically 1 A again.

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DETAILED DESCRIPTION

Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node (VOUT) to the FB pin. It is recommended to use 1% tolerance or better divider resistors.

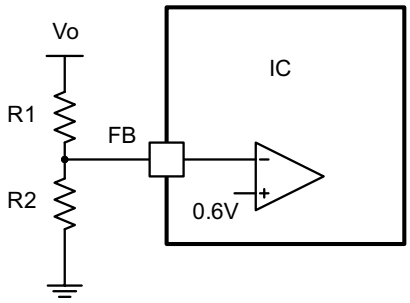


Figure 32. Voltage Divider Circuit

$$R2 = R1 \cdot \left(\frac{0.6V}{V_{OUT} - 0.6V} \right) \quad (1)$$

Start with a 40.2-kΩ for R1 and use Equation 1 to calculate R2. To improve efficiency at light loads consider using larger value resistors. If the values are too high, the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable.

Output voltage can also be changed by I^2C controlled VID in a 7-bit register.

The minimum output voltage and maximum output voltage can be limited by the minimum on time of the high-side MOSFET and bootstrap voltage (BOOT-PH voltage) respectively. More discussions are located in Minimum Output Voltage and Bootstrap Voltage (BOOT) and Low Dropout Operation.

Enable and Adjusting Under-Voltage Lockout

The EN pin provides electrical on/off control of the device. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low Iq state.

The EN pin has an internal pull-up current source, allowing the user to float the EN pin for enabling the device. If an application requires controlling the EN pin, use open drain or open collector output logic to interface with the pin.

The device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 500mV.

If an application requires either a higher UVLO threshold on the VIN pin or a secondary UVLO on the PVIN, in split rail applications, then the EN pin can be configured as shown in Figure 33.

When using the external UVLO function it is recommended to set the hysteresis to be greater than 500 mV.

The EN pin has a small pull-up current I_P which sets the default state of the pin to enable when no external components are connected. The pull-up current is also used to control the voltage hysteresis for the UVLO function since it increases by Ih once the EN pin crosses the enable threshold. The UVLO thresholds can be calculated using Equation 2 and Equation 3.

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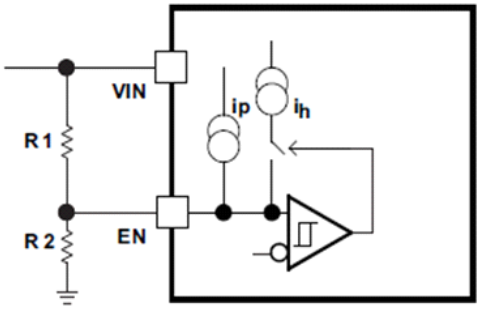


Figure 33. Adjustable VIN Under-Voltage Lockout

$$R_1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_P\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \quad (2)$$

$$R_2 = \frac{R_1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R_1(I_h + I_p)} \quad (3)$$

Where I_h = 3 µA, I_P = 3 µA, $V_{ENRISING}$ = 1.21 V, $V_{ENFALLING}$ = 1.17 V.

Adjustable Switching Frequency and Synchronization

The ROSC pin can be used to set the switching frequency of the device in two mode. The resistor mode is to connect a resistor between ROSC pin and GND. The switching frequency of the device is adjustable from 200 kHz to 1600 kHz. The other mode called synchronization mode is to connect an external clock signal directly to the ROSC pin. The device is synchronized to the external clock frequency with PLL.

Synchronization mode overrides the resistor mode. The device is able to detect the proper mode automatically and switch from synchronization mode to resistor mode.

Adjustable Switching Frequency (Resistor Mode)

To determine the ROSC resistance for a given switching frequency, use Equation 4 or the curve in Figure 34. To reduce the solution size one would set the switching frequency as high as possible, but tradeoffs of the supply efficiency and minimum controllable on time should be considered.

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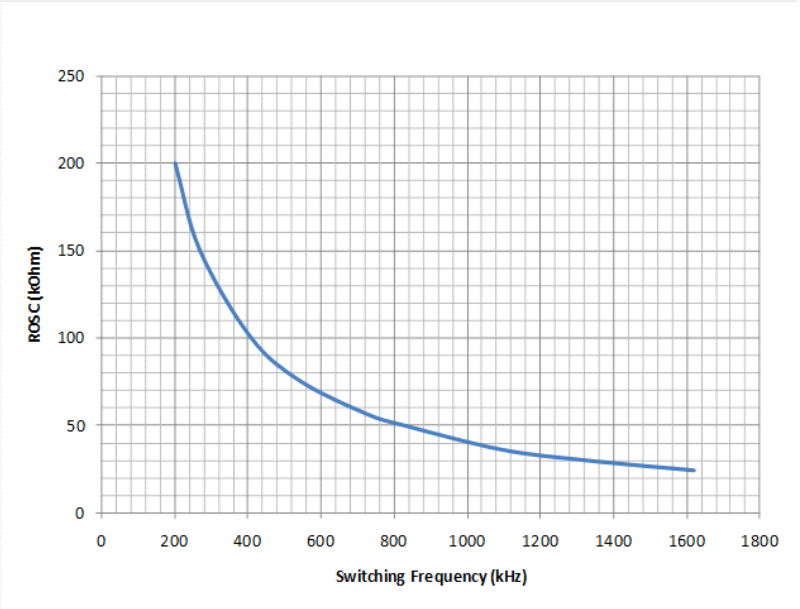


Figure 34. ROSC vs Switching Frequency

$$R_{osc}(k\Omega) = 45580 \cdot f_{sw}^{-1.019}(kHz) \quad (4)$$

Synchronization

An internal phase locked loop (PLL) has been implemented to allow synchronization between 200 kHz and 1600 kHz, and to easily switch from Resistor mode to Synchronization mode.

To implement the synchronization feature, connect a square wave clock signal to the ROSC pin with a duty cycle between 20% to 80%. The clock signal amplitude must transition lower than 0.8 V and higher than 2 V. The start of the switching cycle is synchronized to the falling edge of ROSC pin.

In applications where both Resistor mode and Synchronization mode are needed, the device can be configured as shown in Figure 35. Before the external clock is present, the device works in Resistor mode and the switching frequency is set by ROSC resistor. When the external clock is present, the Synchronization mode overrides the Resistor mode. The first time the ROSC pin is pulled above the ROSC high threshold (2 V), the device switches from the Resistor mode to the Synchronization mode and the ROSC pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock. It is not recommended to switch from the Synchronization mode back to the Resistor mode because the internal switching frequency drops to 100 kHz first before returning to the switching frequency set by ROSC resistor.

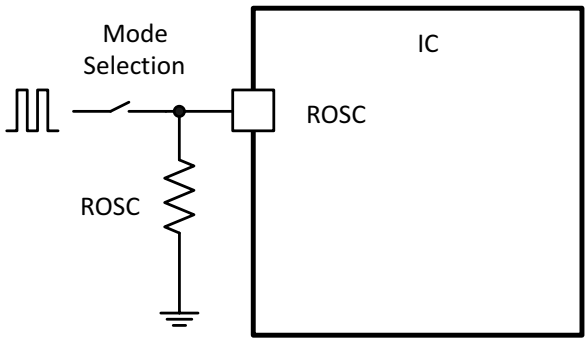


Figure 35. Resistor Mode and Synchronization Mode

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Soft Start Time

The start-up of buck output is controlled by the voltage on the respective SS pin. When the voltage on the SS pin is less than the internal 0.6-V reference, the TPS65276V regulates the internal feedback voltage to the voltage on the SS pin instead of 0.6 V. The SS pin can be used to program an external soft-start function or to allow output of buck to track another supply during start-up. The device has an internal pull-up current source of 6 µA that charges an external soft-start capacitor to provide a linear ramping voltage at SS pin. The TPS65276V regulates the internal feedback voltage according to the voltage on the SS pin, allowing VOUT to rise smoothly from 0 V to its final regulated voltage. The total soft-start time will be calculated approximately:

$$Tss(ms) = Css(nF) \cdot \left(\frac{0.6 \cdot V}{6 \cdot \mu A} \right) \quad (5)$$

VID Control

When I^2C is not in function, the output voltage of TPS65276V is solely set by an external resistor divider. If system wants to control the output voltage, VID (voltage identification) DAC can be controlled via I^2C interface to the Output Voltage Selection register of 0x00H (Buck 1) and 0x1H (Buck 2). Output voltage is required to be preset by the external resistor divider. When VID DAC is selected via I^2C interface and the “GO” bit in command register is set, the output voltage is set with the internal voltage divider over the external voltage divider.

Out-of-Phase Operation

In order to reduce input ripple current, Buck 1 and Buck 2 operate 180° out-of-phase. This enables the system having less input ripple, then to lower component cost, save board space and reduce EMI.

Output Overvoltage Protection (OVP)

The device incorporates an output overvoltage protection (OVP) circuit to minimize output voltage overshoot. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the FB pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. Once the condition is removed, the regulator output rises and the error amplifier output transitions to the steady state voltage. In some applications with small output capacitance, the power supply output voltage can respond faster than the error amplifier. This leads to the possibility of an output overshoot. The OVP feature minimizes the overshoot by comparing the FB pin voltage to the OVP threshold. If the FB pin voltage is greater than the OVP threshold the high-side MOSFET is turned off preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVP threshold, the high-side MOSFET is allowed to turn on at the next clock cycle.

Bootsrap Voltage (BOOT) and Low Dropout Operation

The device has an integrated boot regulator, and requires a small ceramic capacitor between the BOOT and LX pins to provide the gate drive voltage for the high-side MOSFET. The boot capacitor is charged when the BOOT pin voltage is less than VIN and BOOT-LX voltage is below regulation. The value of this ceramic capacitor should be 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and voltage.

To improve drop out, the device is designed to operate at 100% duty cycle as long as the BOOT to LX pin voltage is greater than the BOOT-LX UVLO threshold which is typically 2.1 V. When the voltage between BOOT and LX drops below the BOOT-LX UVLO threshold the high-side MOSFET is turned off and the low-side MOSFET is turned on allowing the boot capacitor to be recharged. In applications with split input voltage rails.

100% duty cycle operation can be achieved as long as (VIN – PVIN) > 4 V.

Over Current Protection

The device is protected from over current conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

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High-Side MOSFET Over Current Protection

The device implements current mode control which uses the COMP pin voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle by cycle basis. Each cycle the switch current and the current reference generated by the COMP pin voltage are compared, when the peak switch current intersects the current reference the high-side switch is turned off.

Low-Side MOSFET Over Current Protection

While the low-side MOSFET is turned on its conduction current is monitored by the internal circuitry. During normal operation the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current limit. If the low-side sourcing current is exceeded, the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET is turned on again when the low-side current is below the low-side sourcing current limit at the start of a cycle.

The low-side MOSFET may also sink current from the load. If the low-side sinking current limit is exceeded the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario both MOSFETs are off until the start of the next cycle.

Furthermore, if an output overload condition (as measured by the COMP pin voltage) has lasted for more than the hiccup wait time which is programmed for 512 switching cycles, the device will shut down itself and restart after the hiccup time of 16384 cycles. The hiccup mode helps to reduce the device power dissipation under severe overcurrent conditions.

Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160°C typically. Once the junction temperature drops below 140°C typically, the internal thermal hiccup timer will start to count. The device reinitiates the power up sequence after the built-in thermal shutdown hiccup time (16384 cycles) is over.

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APPLICATION INFORMATION

Output Inductor Selection

To calculate the value of the output inductor, use Equation 18. LIR is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impact the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, LIR is normally from 0.1 to 0.3 for the majority of applications.

$$L = \frac{V_{inmax} - V_{out}}{I_o \cdot LIR} \cdot \frac{V_{out}}{V_{inmax} \cdot f_{sw}} \quad (6)$$

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 8 and Equation 9.

$$I_{ripple} = \frac{V_{inmax} - V_{out}}{L} \cdot \frac{V_{out}}{V_{inmax} \cdot f_{sw}} \quad (7)$$

$$I_{Lrms} = \sqrt{I_O^2 + \frac{\left(\frac{V_{out} \cdot (V_{inmax} - V_{out})}{V_{inmax} \cdot L \cdot fsw}\right)^2}{12}} \quad (8)$$

$$I_{Lpeak} = I_{out} + \frac{I_{ripple}}{2} \quad (9)$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

Output Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator cannot. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as a transition from no load to full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 10 shows the minimum output capacitance necessary to accomplish this.

$$C_o = \frac{2 \cdot \Delta I_{out}}{f_{sw} \cdot \Delta V_{out}} \quad (10)$$

Where ΔI_{OUT} is the change in output current, f_{SW} is the regulators switching frequency and ΔV_{OUT} is the allowable change in the output voltage. For this example, the transient load response is specified as a 5% change in V_{OUT} for a load step of 3 A. For this example, ΔI_{OUT} = 3 A and ΔV_{OUT} = 0.05 x 3.3 = 0.165 V. Using these numbers gives a minimum capacitance of 75.8 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

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Equation 11 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where f_{SW} is the switching frequency, $V_{oripple}$ is the maximum allowable output voltage ripple, and $I_{oripple}$ is the inductor ripple current.

$$C_o > \frac{1}{8 \cdot f_{sw}} \cdot \frac{1}{\frac{V_{oripple}}{I_{oripple}}} \tag{11}$$

Equation 12 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification.

$$R_{esr} < \frac{V_{oripple}}{I_{oripple}} \tag{12}$$

Additional capacitance de-ratings for aging, temperature and DC bias should be factored in which increases this minimum value.

Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the root mean square (RMS) value of the maximum ripple current. Equation 13 can be used to calculate the RMS ripple current the output capacitor needs to support.

$$I_{corms} = \frac{V_{out} \cdot (V_{inmax} - V_{out})}{\sqrt{12} \cdot V_{inmax} \cdot L \cdot f_{sw}} \tag{13}$$

Input Capacitor Selection

The TPS65276V requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 10-µF of effective capacitance on the PVIN input voltage pins. In some applications additional bulk capacitance may also be required for the PVIN input. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS65276V. The input ripple current can be calculated using Equation 14.

$$I_{inrms} = I_{out} \cdot \sqrt{\frac{V_{out}}{V_{inmin}} \cdot \frac{(V_{inmin} - V_{out})}{V_{inmin}}} \tag{14}$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases. For this example design, a ceramic capacitor with at least a 25-V voltage rating is required to support the maximum input voltage. TPS65276V may operate from a single supply. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 15.

$$\Delta V_{in} = \frac{I_{outmax} \cdot 0.25}{C_{in} \cdot f_{sw}} \tag{15}$$

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Loop Compensation

Integrated buck DC/DC converter in TPS65276V incorporates a peak current mode control scheme. The error amplifier is a transconductance amplifier with a gain of 1350 µA/V. A typical type II compensation circuit adequately delivers a phase margin between 60° and 90°. C_b adds a high frequency pole to attenuate high frequency noise when needed. To calculate the external compensation components, follow the following steps.

1. Select switching frequency f_{sw} that is appropriate for application depending on L and C sizes, output ripple, EMI, and etc. Switching frequency between 500 kHz to 1 MHz gives best trade off between performance and cost. To optimize efficiency, lower switching frequency is desired.
2. Set up cross over frequency, f_c, which is typically between 1/5 and 1/20 of f_{sw}.
3. R_C can be determined by:

$$R_C = \frac{2\pi \cdot fc \cdot Vo \cdot Co}{g_M \cdot Vref \cdot gm_{ps}}$$

   Where is the error amplifier gain (1350 µA/V) is the power stage voltage to current conversion gain (10 A/V).

4. Calculate C_C by placing a compensation zero at or before the dominant pole:

$$(fp = \frac{1}{C_O \cdot R_L \cdot 2\pi}) \cdot s \quad (16)$$

$$C_C = \frac{R_L \cdot Co}{R_C} \quad (17)$$

5. Optional C_b can be used to cancel the zero from the ESR associated with C_O.

$$C_b = \frac{R_{ESR} \cdot Co}{R_C} \quad (18)$$

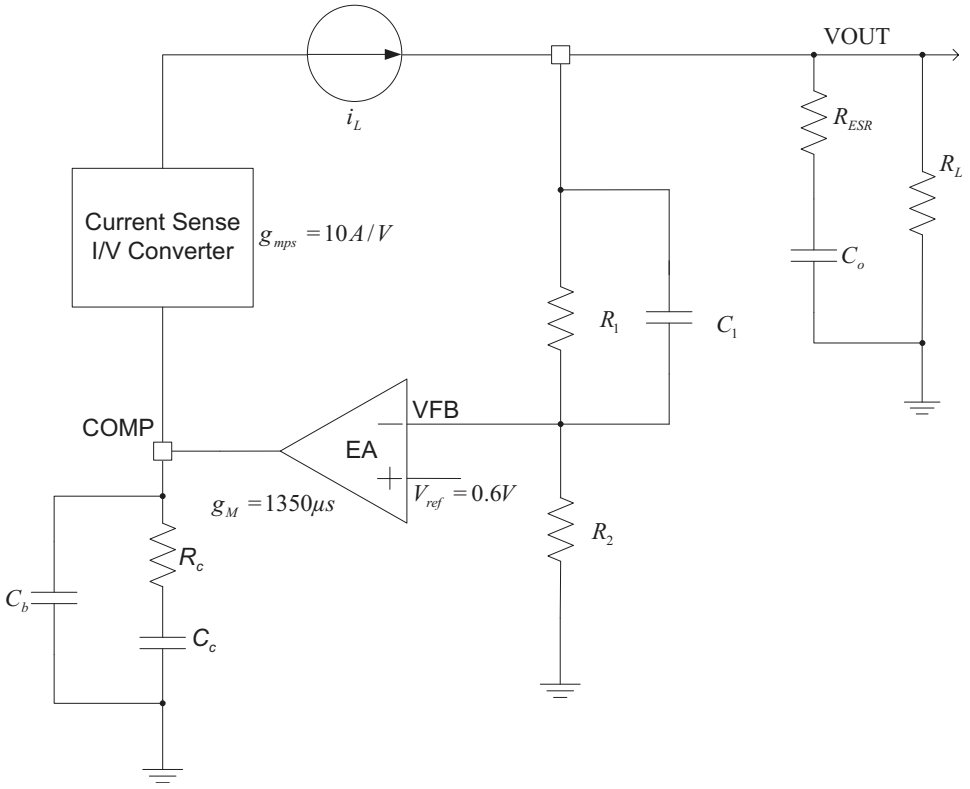


Figure 36. DC/DC Loop Compensation

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Serial Interface Description

I^2C is a 2-wire serial interface developed by Philips Semiconductor (see I^2C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^2C compatible devices connect to the I^2C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The TPS65276V device works as a slave and supports the following data transfer modes, as defined in the I^2C-Bus Specification: standard mode (100 kbps), and fast mode (400 kbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as supply voltage remains above 4.5 V (typical).

The data transfer protocol for standard and fast modes is exactly the same, therefore, they are referred to as F/S-mode in this document. The TPS65276V device supports 7-bit addressing; 10-bit addressing and general call address are not supported.

The TPS65276V device has a 7-bit address with the 2 LSB bits set by ADDR pin. Connecting ADDR to ground set the address 0x60H, connecting to high set the address 0x61H, leaving this pin open set the address 0x62H.

Table 1. I^2C Address Selection

ADDR PIN	I^2C ADDRESS
Connect to Ground	0x60H
Open	0x61H
Connect to High	0x62H

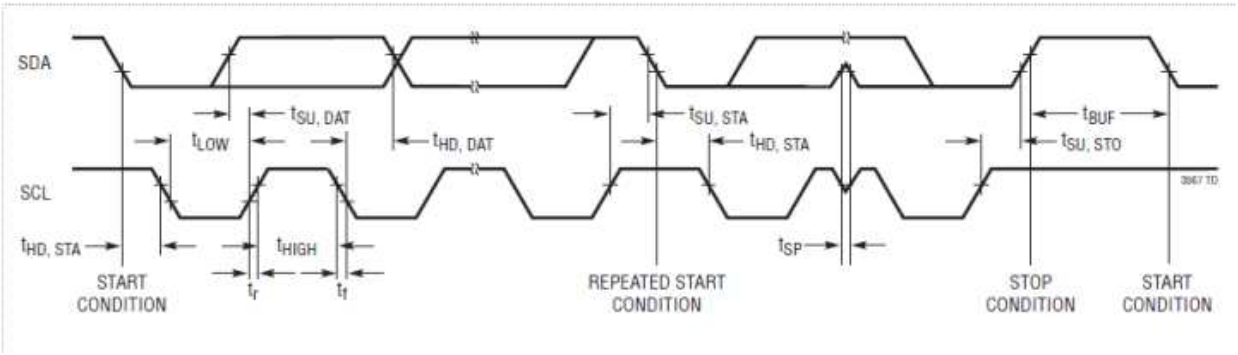


Figure 37. I^2C Interface Timing Diagram

TPS65276V I²C Update Sequence

The TPS65276V requires a start condition, a valid I²C address, a register address byte, and a data byte for a single update. After the receipt of each byte, TPS65276V device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the TPS65276V. TPS65276V performs an update on the falling edge of the LSB byte.

When the TPS65276V is in hardware shutdown (EN1 and EN2 pin tied to ground) the device can not be updated via the I²C interface. Conversely, the I²C interface is fully functional during software shutdown (EN1 and EN2 bit = 0).



Figure 38. I²C Write Data Format

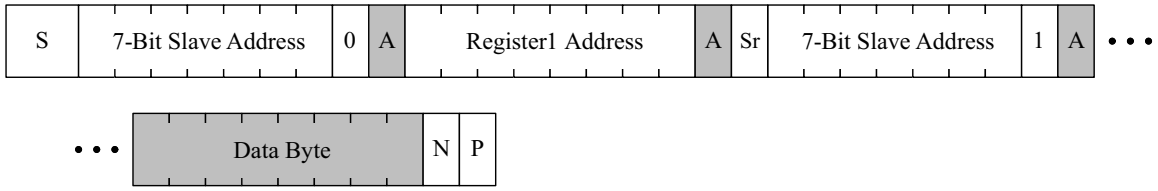


Figure 39. I²C Read Data Format

A: Acknowledge
N: Not Acknowledge
S: Start
P: Stop
Sr: Repeated Start

System Host
Chip

Register Description

Register descriptions are shown in the below tables.

Table 2. Register Addresses

NAME	BITS	ADDRESS
Vout1_SEL	8	0x00H
Vout2_SEL	8	0x01H
Vout1_COM	8	0x02H
Vout2_COM	8	0x03H
Sys_STATUS	8	0x04H

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Table 3. Vout1 Voltage Selection Register

	NUMBER OF BITS	ACCESS	NAME	DEFAULT VALUE	DESCRIPTION
Vout1_SEL	7				10-mV step, from 0.68 V to 1.95 V
address: 0x00H	Bit 7	R/W	Vout1_Bit7	0	Go bit, must set "1" to enable I^2C voltage control
	Bit 6	R/W	Vout1_Bit6	0	0x00H: 0.68V; 0x7FH: 1.95V
	Bit 5	R/W	Vout1_Bit5	0	
	Bit 4	R/W	Vout1_Bit4	0	
	Bit 3	R/W	Vout1_Bit3	0	
	Bit 2	R/W	Vout1_Bit2	0	
	Bit 1	R/W	Vout1_Bit1	0	
	Bit 0	R/W	Vout1_Bit0	0	

Table 4. Vout2 Voltage Selection Register

	NUMBER OF BITS	ACCESS	NAME	DEFAULT VALUE	DESCRIPTION
Vout2_SEL	7				10-mV step, from 0.68 V to 1.95 V
address: 0x01H	Bit 7	R/W	Vout2_Bit7	0	Go bit, must set "1" to enable I^2C voltage control
	Bit 6	R/W	Vout2_Bit6	0	0x00H: 0.68V; 0x7FH: 1.95V
	Bit 5	R/W	Vout2_Bit5	0	
	Bit 4	R/W	Vout2_Bit4	0	
	Bit 3	R/W	Vout2_Bit3	0	
	Bit 2	R/W	Vout2_Bit2	0	
	Bit 1	R/W	Vout2_Bit1	0	
	Bit 0	R/W	Vout2_Bit0	0	

Table 5. Vout1 Command Register

	NUMBER OF BITS	ACCESS	NAME	DEFAULT VALUE	DESCRIPTION
Vout1_COM	8				
address: 0x02H	Bit 7				Reserved
	Bit 6	R/W	Slew Rate 3	0	Vout slew rate control. 000: 10 mV/cycle; 001: 10 mV/2 cycles; 010: 10 mV/4 cycles; 011: 10 mV/8 cycles; 100: 10 mV/16cycles; 101: 10 mV/32cycles; 110: 10 mV/64cycles; 111: 10 mV/128 cycles
	Bit 5	R/W	Slew Rate 2	0	
	Bit 4	R/W	Slew Rate 1	0	
	Bit 3				Reserved
	Bit 2	R/W	PSM Mode	0	00: select by MODE pin; 01: forced PWM mode; 10: auto PSM-PWM mode; 11: reserved
	Bit 1	R/W	PSM Mode	0	
	Bit 0	R/W	Disable1	0	0: output enabled; 1: output disabled

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Table 6. Vout2 Command Register

	NUMBER OF BITS	ACCESS	NAME	DEFAULT VALUE	DESCRIPTION
Vout2_COM	8				
address: 0x03H	Bit 7				Reserved
	Bit 6	R/W	Slew Rate 3	0	Vout slew rate control. 000: 10 mV/cycle; 001: 10 mV/2 cycles; 010: 10 mV/4 cycles; 011: 10 mV/8 cycles; 100: 10 mV/16cycles; 101: 10 mV/32cycles; 110: 10 mV/64cycles; 111: 10 mV/128 cycles
	Bit 5	R/W	Slew Rate 2	0	
	Bit 4	R/W	Slew Rate 1	0	
	Bit 3				Reserved
	Bit 2	R/W	PSM Mode	0	00: select by MODE pin; 01: forced PWM mode; 10: auto PSM-PWM mode; 11: reserved
	Bit 1	R/W	PSM Mode	0	
	Bit 0	R/W	Disable2	0	0: output enabled; 1: output disabled

Table 7. System Status Register

	NUMBER OF BITS	ACCESS	NAME	DEFAULT VALUE	DESCRIPTION
SYS_STATUS	8				
address: 0x04H	Bit 7				Reserved
	Bit 6				Reserved
	Bit 5				Reserved
	Bit 4				Reserved
	Bit 3				Reserved
	Bit 2	R	Temperature Warning (> 125°C)	0	1: Die temperature over 125°C; 0: Die temperature below 125°C
	Bit 1	R	PGOOD2	0	1: Vout2 in power good regulation range; 0: Vout2 not in power good regulation range
	Bit 0	R	PGOOD 1	0	1: Vout1 in power good regulation range; 0: Vout1 not in power good regulation range

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Table 8. Vout1 and Vout2 Output Voltage Setting

VOUT_SEL <7:0>	OUTPUT VOLTAGE (V)	VOUT_SEL <7:0>	OUTPUT VOLTAGE (V)	VOUT_SEL <7:0>	OUTPUT VOLTAGE (V)	VOUT_SEL <7:0>	OUTPUT VOLTAGE (V)
0	0.68	20	1	40	1.32	60	1.64
1	0.69	21	1.01	41	1.33	61	1.65
2	0.7	22	1.02	42	1.34	62	1.66
3	0.71	23	1.03	43	1.35	63	1.67
4	0.72	24	1.04	44	1.36	64	1.68
5	0.73	25	1.05	45	1.37	65	1.69
6	0.74	26	1.06	46	1.38	66	1.7
7	0.75	27	1.07	47	1.39	67	1.71
8	0.76	28	1.08	48	1.4	68	1.72
9	0.77	29	1.09	49	1.41	69	1.73
A	0.78	2A	1.1	4A	1.42	6A	1.74
B	0.79	2B	1.11	4B	1.43	6B	1.75
C	0.8	2C	1.12	4C	1.44	6C	1.76
D	0.81	2D	1.13	4D	1.45	6D	1.77
E	0.82	2E	1.14	4E	1.46	6E	1.78
F	0.83	2F	1.15	4F	1.47	6F	1.79
10	0.84	30	1.16	50	1.48	70	1.8
11	0.85	31	1.17	51	1.49	71	1.81
12	0.86	32	1.18	52	1.5	72	1.82
13	0.87	33	1.19	53	1.51	73	1.83
14	0.88	34	1.2	54	1.52	74	1.84
15	0.89	35	1.21	55	1.53	75	1.85
16	0.9	36	1.22	56	1.54	76	1.86
17	0.91	37	1.23	57	1.55	77	1.87
18	0.92	38	1.24	58	1.56	78	1.88
19	0.93	39	1.25	59	1.57	79	1.89
1A	0.94	3A	1.26	5A	1.58	7A	1.9
1B	0.95	3B	1.27	5B	1.59	7B	1.91
1C	0.96	3C	1.28	5C	1.6	7C	1.92
1D	0.97	3D	1.29	5D	1.61	7D	1.93
1E	0.98	3E	1.3	5E	1.62	7E	1.94
1F	0.99	3F	1.31	5F	1.63	7F	1.95

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PCB Layout Guideline

TPS65276V can be layout on 2-layer PCB illustrated below.

Layout is a critical portion of good power supply design. See Figure 40 for a PCB layout example. The top layer contains the main power traces for VIN, VOUT, and VLX. Also on the top layer are connections for the remaining pins of the TPS65276V and a large top side area filled with ground. The top layer ground area should be connected to the internal ground layer(s) using vias at the input bypass capacitor, the output filter capacitor and directly under the TPS65276V device to provide a thermal path from the exposed thermal pad land to ground. The bottom layer acts as ground plane connecting analog ground and power ground.

The GND pin should be tied directly to the power pad under the IC and the power pad. For operation at full rated load, the top side ground area together with the internal ground plane, must provide adequate heat dissipating area. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the PVIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the PVIN pins, and the ground connections.

The VIN pin must also be bypassed to ground using a low ESR ceramic capacitor with X5R or X7R dielectric.

Since the LX connection is the switching node, the output inductor should be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The output filter capacitor ground should use the same power ground trace as the PVIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width. The additional external components can be placed approximately as shown.

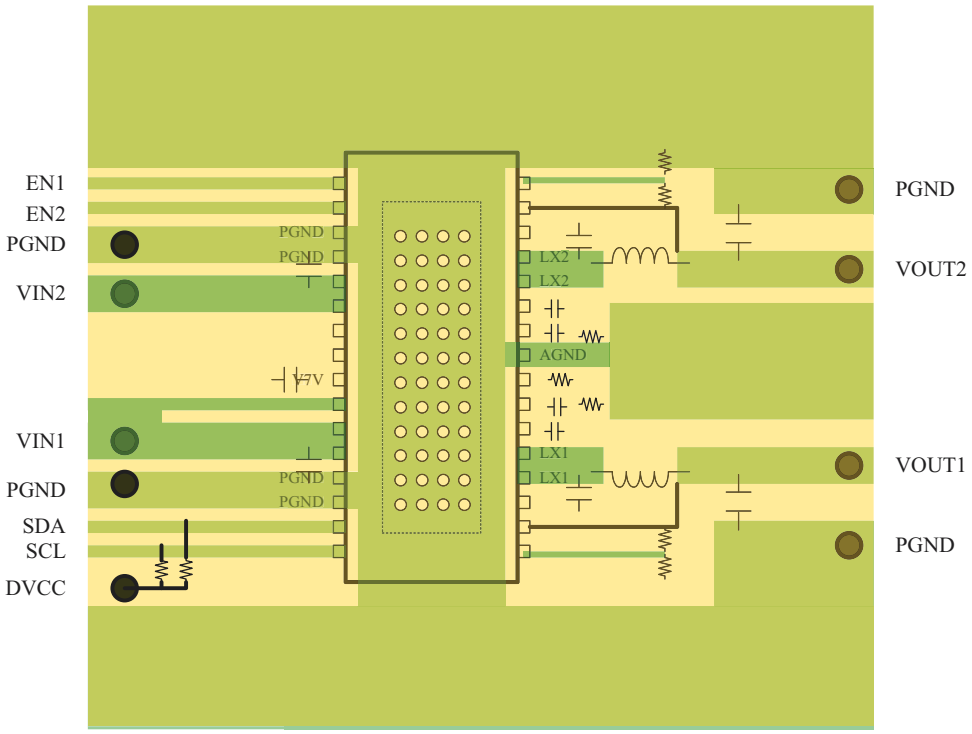


Figure 40. TPS65276V Layout on 2-layer PCB

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修订历史记录

Changes from Revision A (June 2013) to Revision B **Page**

- Changed FUNCTIONAL BLOCK DIAGRAM 4
- Changed ABSOLUTE MAXIMUM RATINGS table 8

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS65276VDAPR	Active	Production	HTSSOP (DAP) | 32	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS65276V
TPS65276VDAPR.A	Active	Production	HTSSOP (DAP) | 32	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS65276V
TPS65276VRHHR	Active	Production	VQFN (RHH) | 36	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 65276V
TPS65276VRHHR.A	Active	Production	VQFN (RHH) | 36	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 65276V
TPS65276VRHHT	Active	Production	VQFN (RHH) | 36	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 65276V
TPS65276VRHHT.A	Active	Production	VQFN (RHH) | 36	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 65276V
TPS65276VRHHTG4	Active	Production	VQFN (RHH) | 36	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 65276V
TPS65276VRHHTG4.A	Active	Production	VQFN (RHH) | 36	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 65276V

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

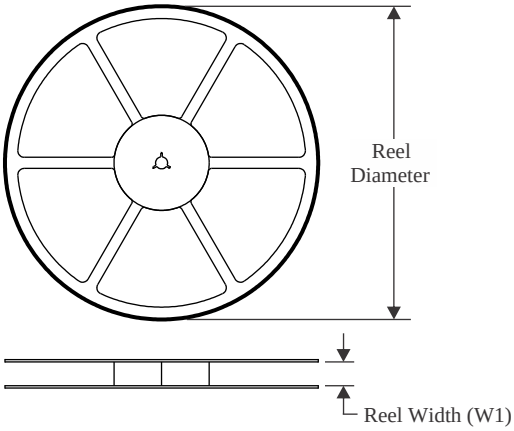
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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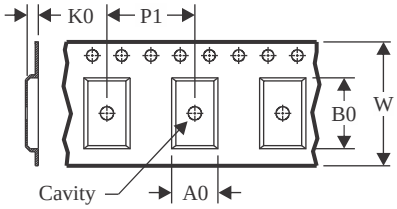
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

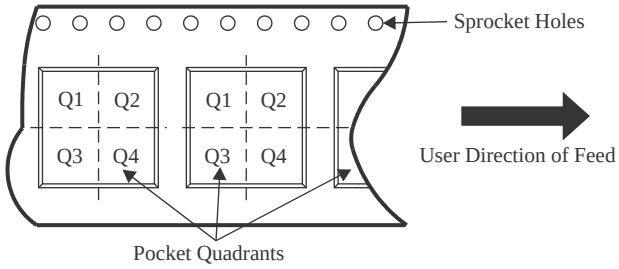


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

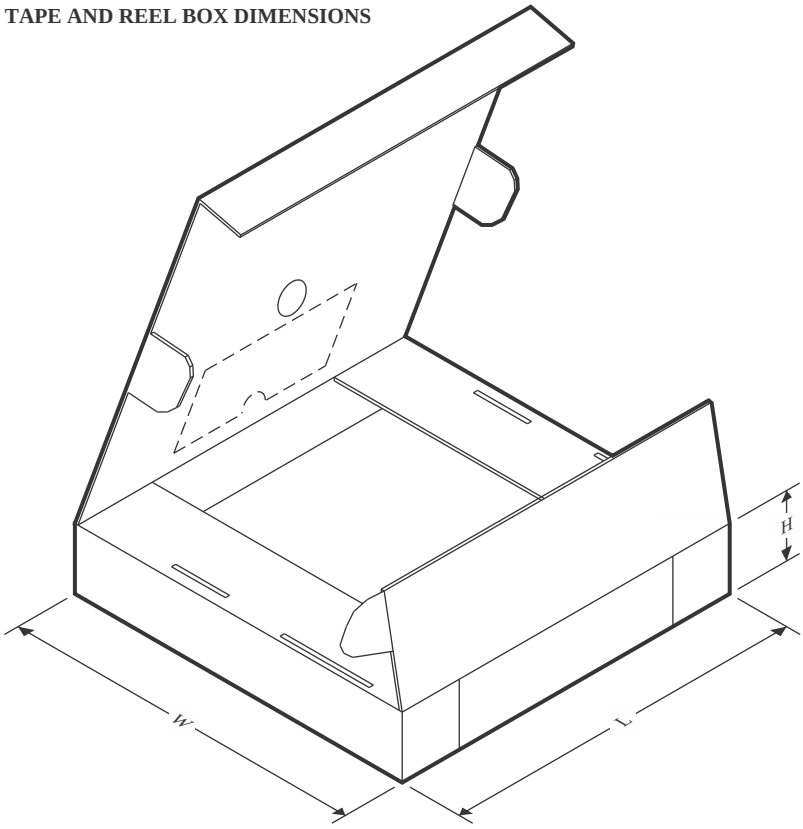
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65276VDAPR	HTSSOP	DAP	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1
TPS65276VRHHR	VQFN	RHH	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65276VRHHT	VQFN	RHH	36	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65276VRHHTG4	VQFN	RHH	36	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65276VDAPR	HTSSOP	DAP	32	2000	350.0	350.0	43.0
TPS65276VRHHR	VQFN	RHH	36	2500	367.0	367.0	38.0
TPS65276VRHHT	VQFN	RHH	36	250	210.0	185.0	35.0
TPS65276VRHHTG4	VQFN	RHH	36	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

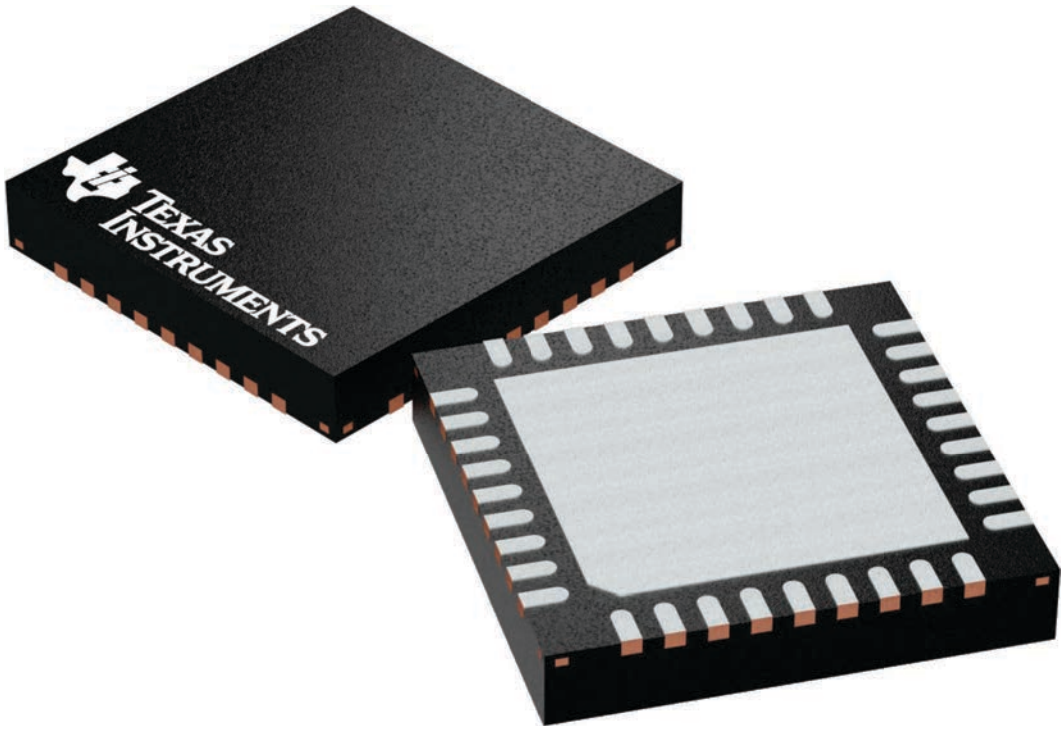
RHH 36

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



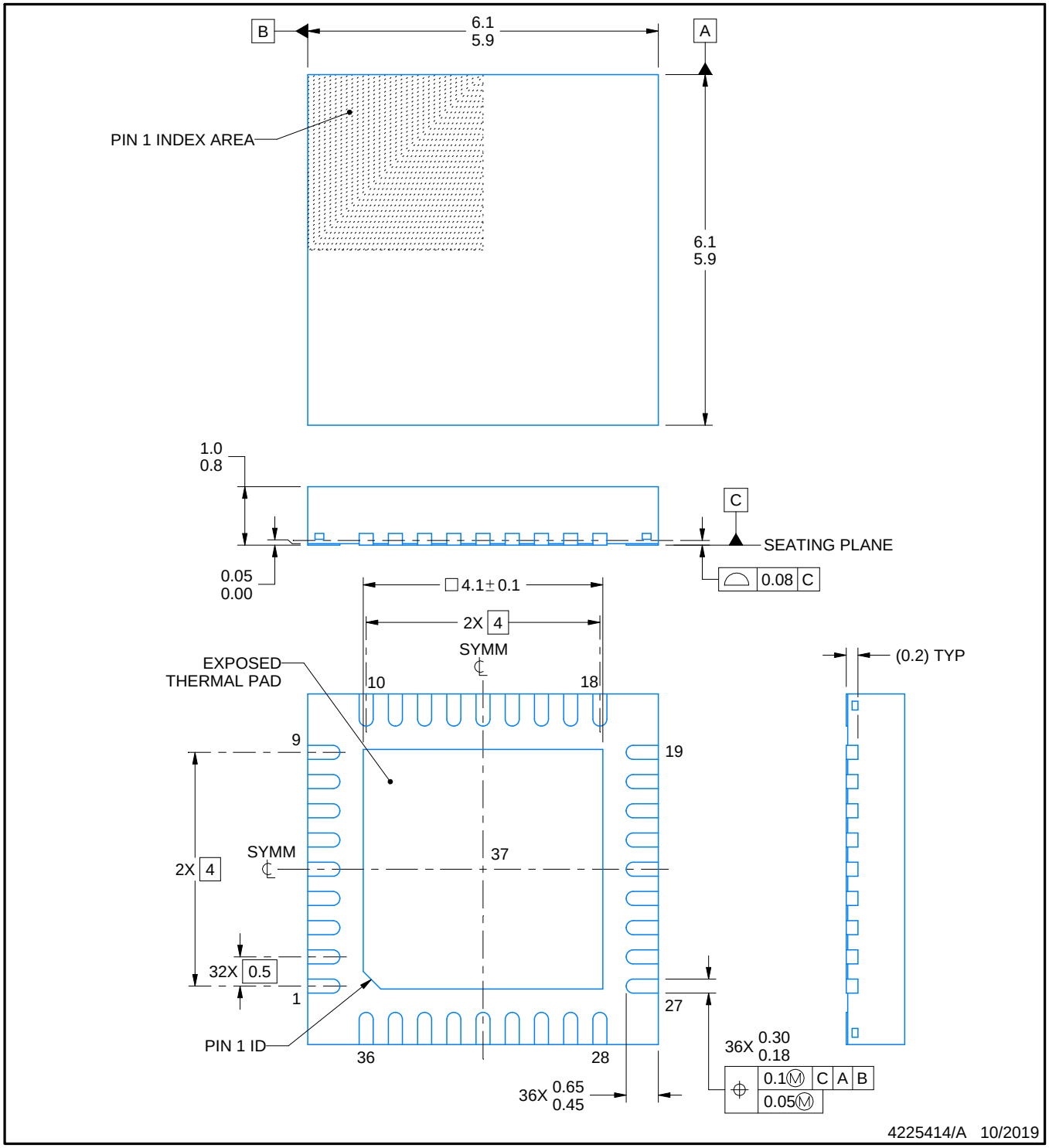
4225440/A

RHH0036B

PACKAGE OUTLINE

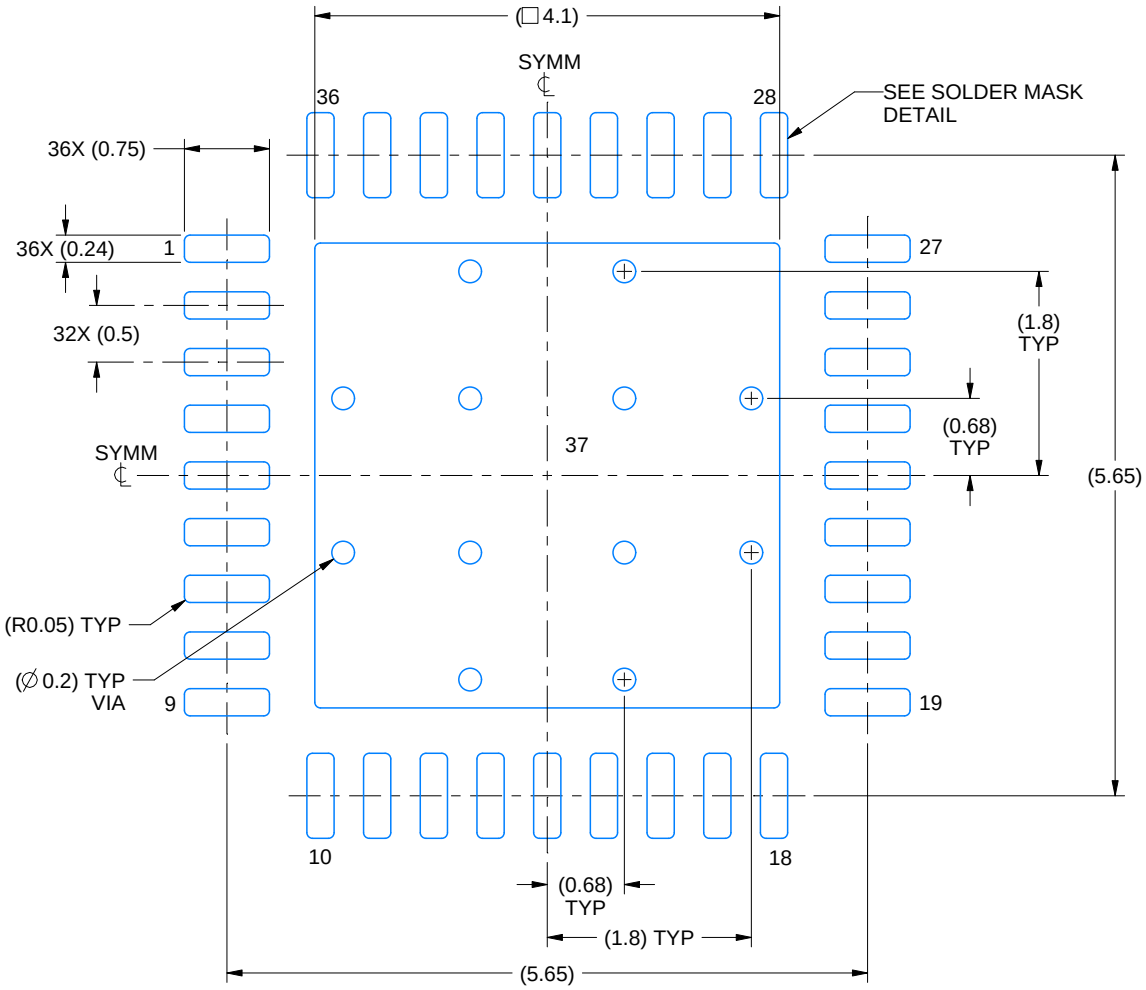
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

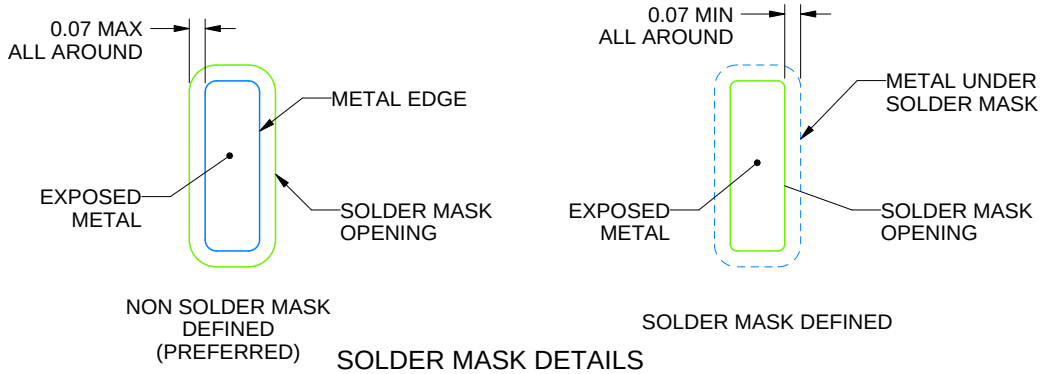


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

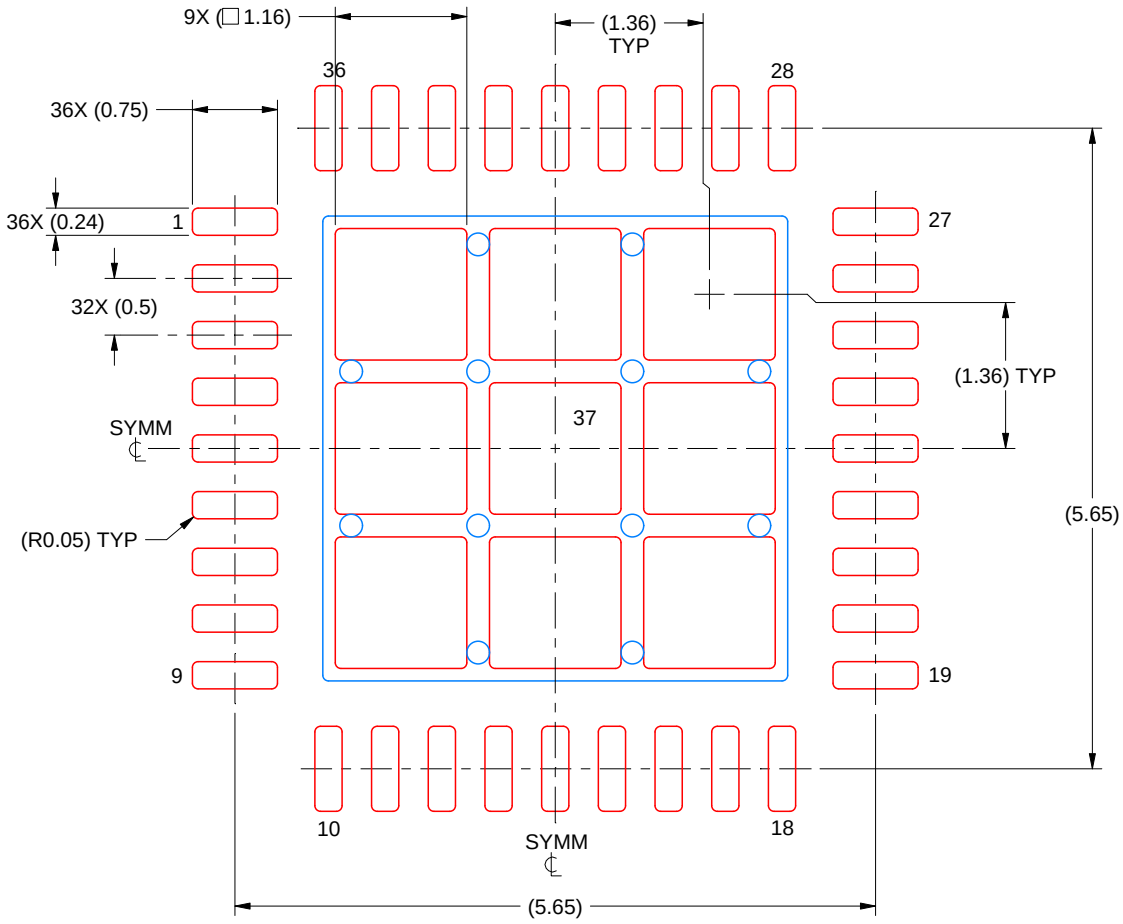


SOLDER MASK DETAILS

4225414/A 10/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 37
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225414/A 10/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

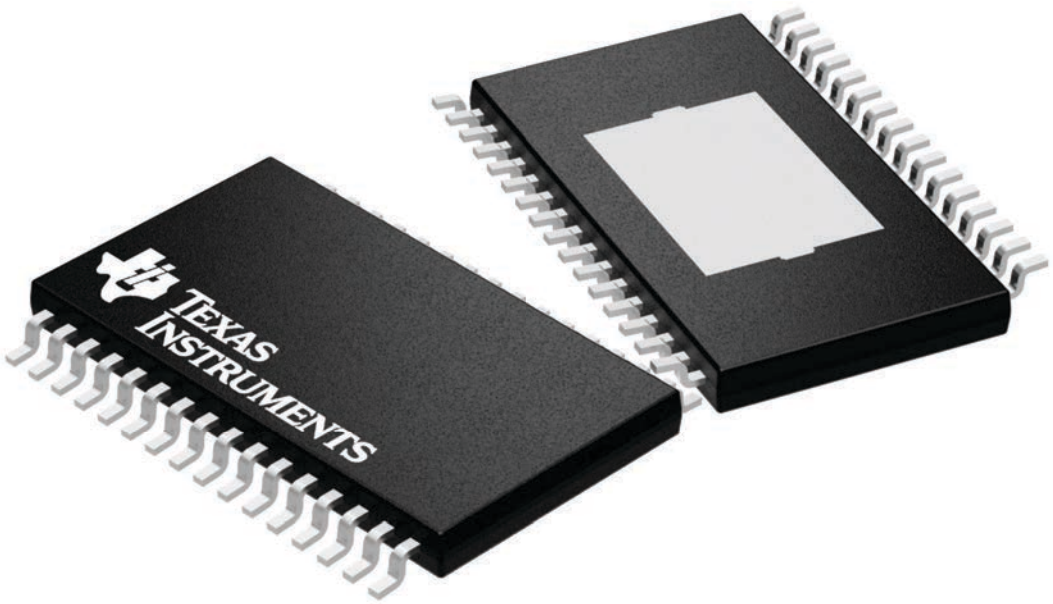
DAP 32

PowerPAD™ TSSOP - 1.2 mm max height

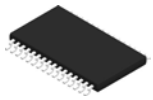
8.1 x 11, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225303/A

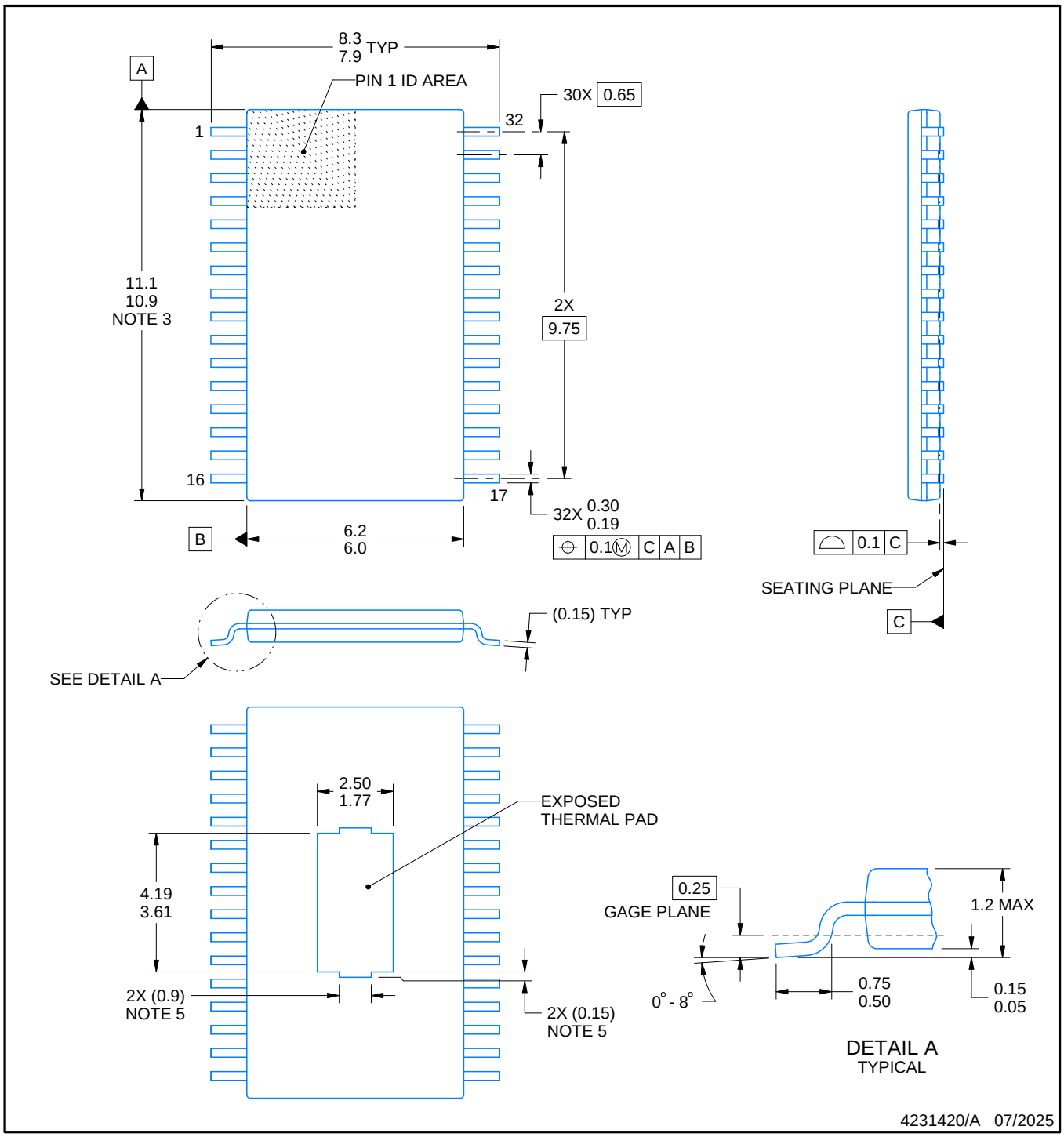


PACKAGE OUTLINE

DAP0032D

PowerPAD™ TSSOP - 1.2 mm max height

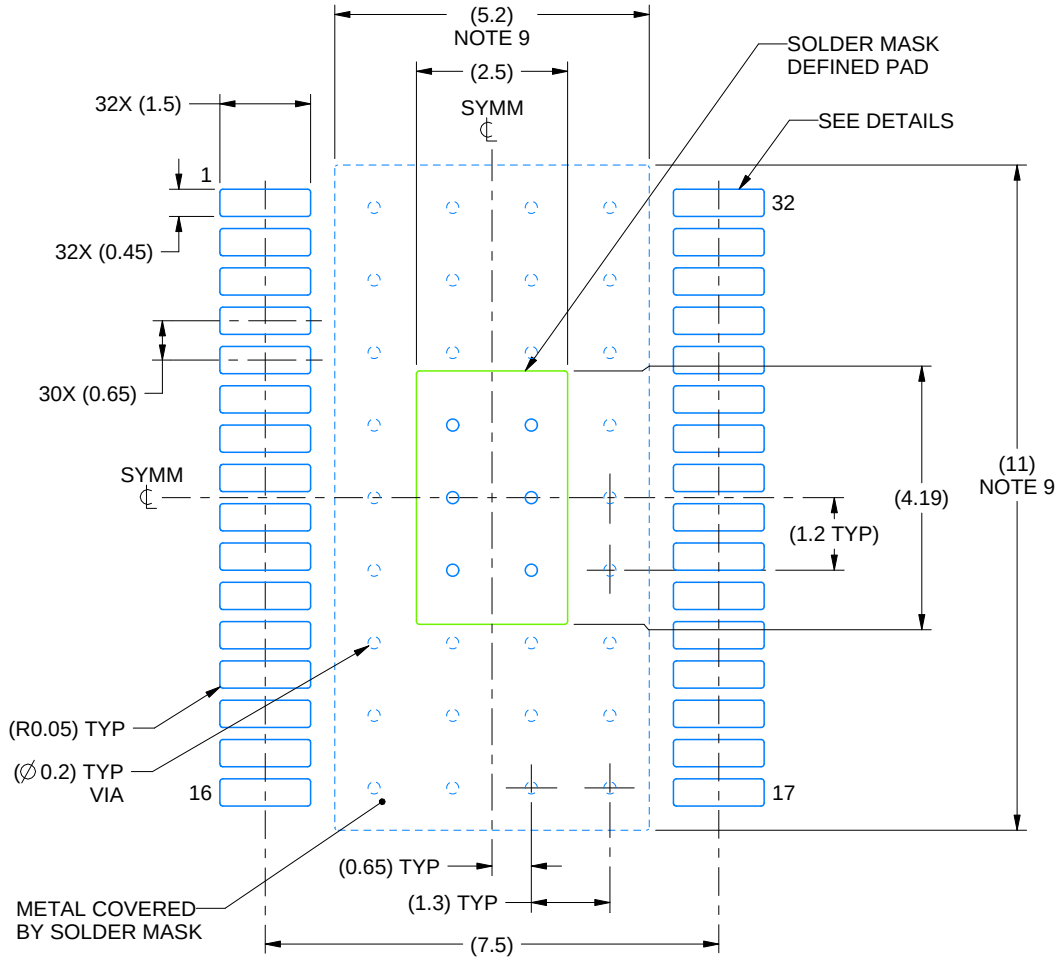
PLASTIC SMALL OUTLINE



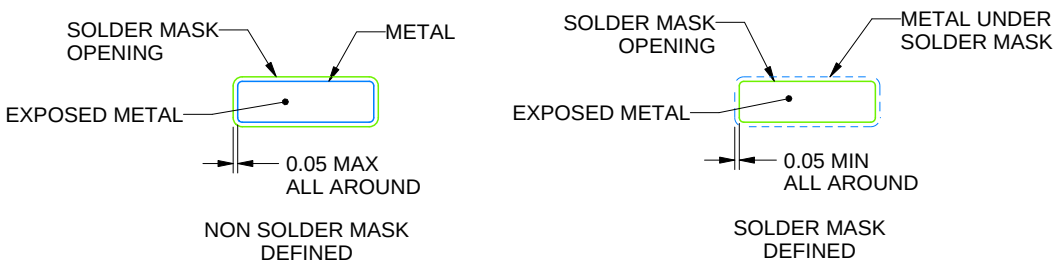
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

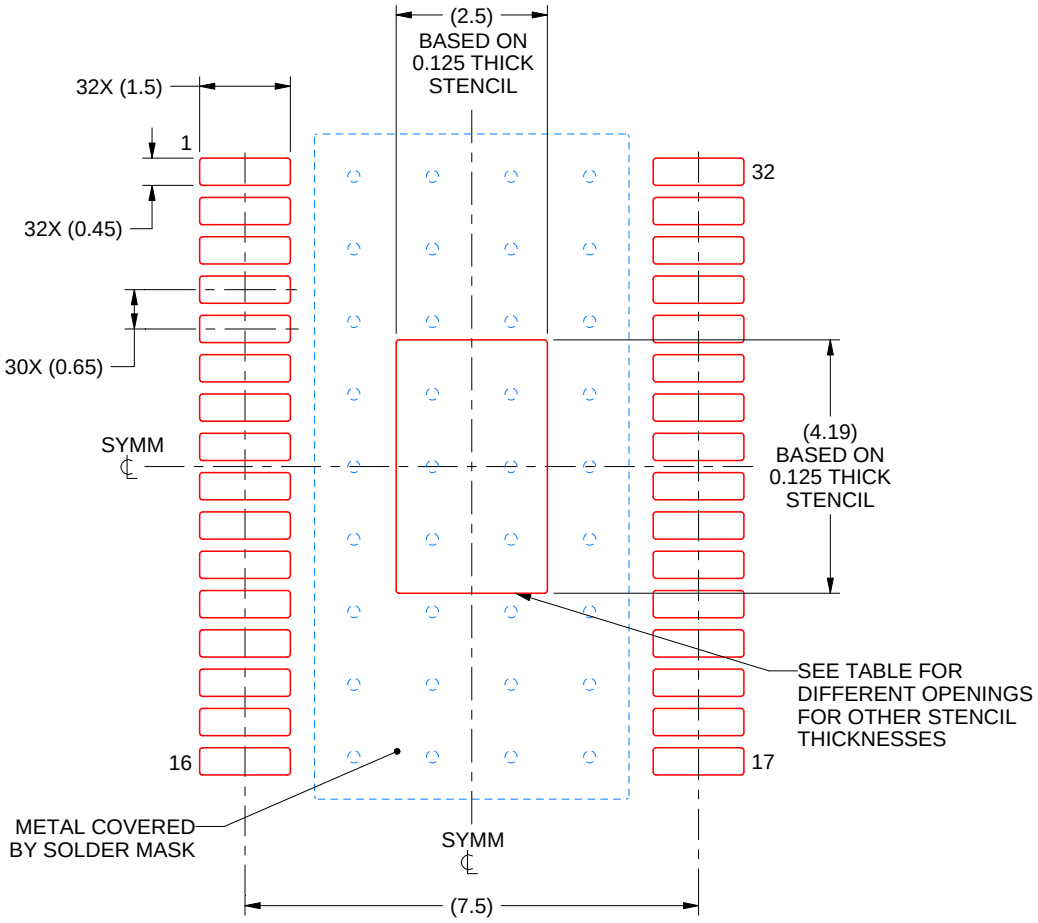


SOLDER MASK DETAILS
NOT TO SCALE

4231420/A 07/2025

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.80 X 4.68
0.125	2.50 X 4.19 (SHOWN)
0.15	2.28 X 3.83
0.175	2.11 X 3.54

4231420/A 07/2025

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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