# TPS65177/A 适用于所有尺寸 TV 的完全 I²C 可编程 6 通道 LCD 偏置 IC，具有栅极脉冲调制功能

## 1 特性

- 使能/禁用
  - TPS65177： $V_I$ 掉电再上电
  - TPS65177A：$V_I$ 掉电再上电或 EN 引脚
- 8.6V 到 14.7V 输入电压范围
- 非同步升压转换器 ($V_{(AVDD)}$)
  - 集成隔离开关
  - 13.5V 到 19.8V 输出电压 (I²C)
  - 15V 默认输出电压
  - 4.25A 开关电流限制 (I²C)
  - 高压应力模式 (I²C)
- 同步降压转换器 ($V_{(HAVDD)}$)
  - 4.8V 到 11.1V 输出电压 (I²C)
  - 7.5V 默认输出电压
  - 1.7A 开关电流限制
  - 高压应力模式 (I²C)
- 非同步降压转换器 ($V_{(IO)}$)
  - 2.2V 到 3.7V 输出电压 (I²C)
  - 2.5V 默认输出电压
  - 3A 开关电流限制
- 同步降压转换器 ($V_{(CORE)}$)
  - 0.8V 到 3.3V 输出电压 (I²C)
  - 1V 默认输出电压
  - 2.5A 开关电流限制
- 正电荷泵控制器 ($V_{(GH)}$)
  - 20V 到 40V 输出电压 (I²C)
  - 28V 默认输出电压
  - 温度补偿偏移：0V 到 15V (I²C)
  - 4V 默认偏移（28V 到 32V）
- 负电荷泵控制器 ($V_{(GL)}$)
  - –14.5V 到 –5.5V 输出电压 (I²C)
  - –7.9V 默认输出电压
- 栅极脉冲调制 (GPM)
  - 低至 0V、5V、10V 或 15V (I²C)
  - 0V 默认放电电压
- $V_{(GH)}$ 的温度补偿
- 热关断
- I²C 兼容接口
- EEPROM 存储器
- 6mm × 6mm × 1mm 40 引脚超薄四方扁平无引线 (VQFN) 封装

## 2 应用

- GIP (Gate-in-Panel) 液晶显示屏 (LED) 电视 (TV)
- 非 GIP LCD TV

## 3 说明

TPS65177/A 可提供 GIP (Gate-in-Panel) 或非 GIP 薄膜晶体管 (TFT)-LCD 面板所需的所有电源轨。所有输出电压均可通过 I²C 编程设定。

$V_{(IO)}$ 和 $V_{(CORE)}$ 用于 T-CON，$V_{(AVDD)}$ 和 $V_{(HAVDD)}$ 用于拉电流驱动器和伽马缓冲器，$V_{(GH)}$ 和 $V_{(GL)}$ 用于栅极驱动器或电平转换器。为了与非 GIP 技术搭配使用，实现了栅极脉冲调制 (GPM)；为了与 GIP 技术搭配使用，可对 $V_{(GH)}$ 轨进行温度补偿。此外，还针对 $V_{(AVDD)}$ 和 $V_{(HAVDD)}$ 提供了一种高压应力模式 (HVS)，并且实现了一个集成式 $V_{(AVDD)}$ 隔离开关。$V_{(CORE)}$、$V_{(HAVDD)}$、$V_{(GH)}$、$V_{(GL)}$、GPM 和 $V_{(GH)}$ 温度补偿可通过 I²C 编程来使能与禁用。

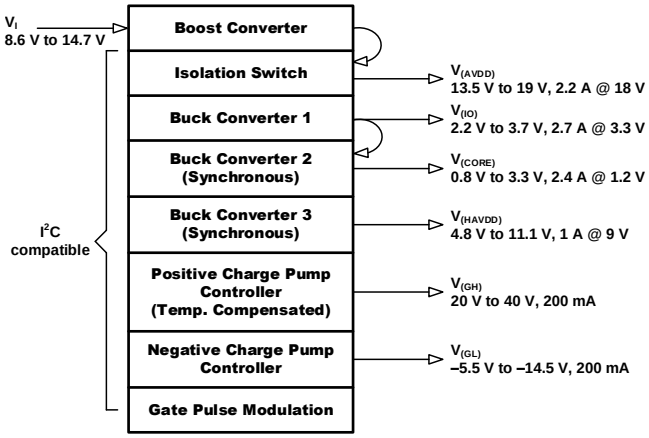
单一 BOM（物料清单）可涵盖多种面板类型和尺寸，这些面板所需的输出电压可以在生产时进行编程并存储于非易失性集成存储器中。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| TPS65177 | VQFN（40 引脚） | 6.00mm x 6.00mm |
| TPS65177A | VQFN（40 引脚） | 6.00mm x 6.00mm |

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

方框图




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

**Changes from Revision B (January 2016) to Revision C** — **Page**

- 已添加 TPS65177A 器件并已更改 特性 描述，多张图片的颜色 ... 1

**Changes from Revision A (July 2012) to Revision B** — **Page**

- 已添加 *ESD 额定值表，特性 描述部分，器件功能模式部分，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分。* ... 1
- Added text to the *Power-Up* section, " If the EN pin is not connected to VIN..." ... 14

**Changes from Original (March 2012) to Revision A** — **Page**

- Changed $P_R$ equation ... 28
- Deleted Inverting Doubler: $V_{GL_max}$ equation ... 29
- Deleted Inverting Doubler: $V_{GL_max}$ equation ... 29
- Deleted Inverting Doubler: $P_{DIS}$ equation ... 30
- Deleted Inverting Doubler: $P_{DIS}$ equation ... 30
- Changed $P_R$ equation ... 31
- Changed Figure 46, Figure 47, ... 53
- Changed Figure 48 ... 56


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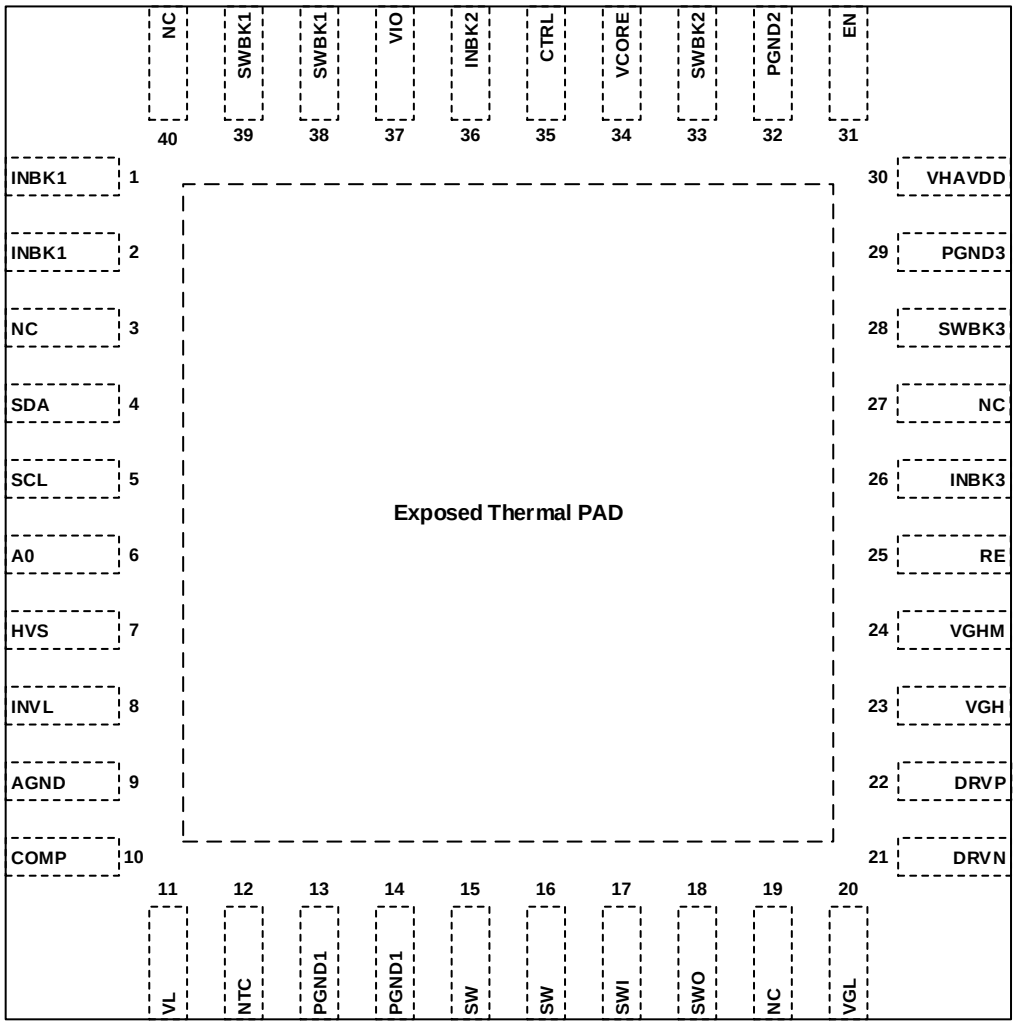
# 5 Pin Configuration and Functions

**RHA Package**
**40 Pin (VQFN)**
**Top View**




## Pin Functions

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| INBK1 | 1, 2 | — | Buck 1 converter ($V_{(IO)}$) supply pin. This pin is internally connected to INBK3. Place a buffer capacitor close to this pin. |
| NC | 3 | — | Not connected. |
| SDA | 4 | I / O | $I^2C$ data pin. |
| SCL | 5 | I | $I^2C$ clock pin. |
| A0 | 6 | I | $I^2C$ address select pin. |
| HVS | 7 | I | Boost and Buck 3 converter High Voltage Stress Mode enable pin. |
| INVL | 8 | — | Internal logic supply pin. Place a buffer capacitor close to this pin. |
| AGND | 9 | — | Analog Ground pin. Internal circuitry uses this ground. |
| COMP | 10 | I / O | Boost converter ($V_{(AVDD)}$) compensation pin. |
| VL | 11 | I / O | Internal 5 V regulator output pin. Connect a buffer capacitor to this pin. |
| NTC | 12 | I | Thermal Resistor sense pin. |

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## Pin Functions (continued)

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| PGND1 | 13, 14 | — | Boost converter ($V_{(AVDD)}$) Power Ground pin. |
| SW | 15, 16 | O | Boost converter ($V_{(AVDD)}$) switch pin. Avoid long traces to the diode and inductor because this trace carries switching waveforms that generate noise. |
| SWI | 17 | I | Isolation Switch input pin. |
| SWO | 18 | O | Isolation Switch output pin. |
| NC | 19 | — | Not connected. |
| VGL | 20 | I | Negative Charge Pump ($V_{(GL)}$) voltage sense pin. |
| DRVN | 21 | O | Negative Charge Pump ($V_{(GL)}$) base drive pin. |
| DRVP | 22 | I | Positive charge pump ($V_{(GH)}$) base drive pin. |
| VGH | 23 | I | Positive charge pump ($V_{(GH)}$) output voltage sense and Gate Pulse Modulation supply pin. |
| VGHM | 24 | I / O | Gate Pulse Modulation output pin. |
| RE | 25 | O | Slope adjustment of Gate Pulse Modulation. |
| INBK3 | 26 | — | Buck 3 converter ($V_{(HAVDD)}$) supply pin. This pin is internally connected to INBK1. Place a buffer capacitor close to this pin. |
| NC | 27 | — | Not connected. |
| SWBK3 | 28 | O | Buck 3 Converter ($V_{(HAVDD)}$) switch pin. Avoid long traces to the inductor because this trace carries switching waveforms that generate noise. |
| PGND3 | 29 | — | Buck 3 Converter ($V_{(HAVDD)}$) Power Ground pin. |
| VHAVDD | 30 | I | Buck 3 Converter ($V_{(HAVDD)}$) voltage sense pin. |
| EN | 31 | I | Enable of Isolation Switch, Boost converter and Buck 3 converter. |
| PGND2 | 32 | — | Buck 2 converter ($V_{(CORE)}$) Power Ground pin. |
| SWBK2 | 33 | O | Buck 2 converter ($V_{(CORE)}$) switch pin. Avoid long traces to the inductor because this trace carries switching waveforms that generate noise. |
| VCORE | 34 | I | Buck 2 converter ($V_{(CORE)}$) output voltage sense pin. |
| CTRL | 35 | I | Gate Pulse Modulation control pin. |
| INBK2 | 36 | — | Buck 2 converter ($V_{(CORE)}$) supply pin. Place a buffer capacitor close to this pin. |
| VIO | 37 | I | Buck 1 converter ($V_{(IO)}$) output voltage sense pin. |
| SWBK1 | 38, 39 | O | Buck 1 converter ($V_{(IO)}$) switch pin. Avoid long traces to the diode and inductor because this trace carries switching waveforms that generate noise. |
| NC | 40 | — | Not connected. |
| Exposed thermal pad | | — | The Exposed thermal pad is connected to AGND. |


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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

| | | VALUE | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| Pin Voltage (2) | VIO, INBK1, HVS, INVL, INBK3, SWBK3, VHAVDD, SW, SWI, SWO | –0.3 | 20 | V |
| | SWBK1 | –2 | 18 | V |
| | COMP, EN, A0, SDA, SCL, CTRL, SWBK2, VCORE, INBK2, DRVN, NTC | –0.3 | 7 | V |
| | VL | –0.3 | 5.5 | V |
| | DRVP, VGH, VGHM, RE | –0.3 | 40 | V |
| | VGL | –15 | 0.3 | V |
| Operating junction temperature range | | –40 | 150 | °C |
| Storage temperature range, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) With respect to the GND pin.

## 6.2 ESD Ratings

| | | VALUE | UNIT |
|---|---|---|---|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | ±2000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101 (2) | ±700 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_I$ | Supply input voltage range | 8.6 | 12 | 14.7 | V |
| $C_{(VL)}$ | Internal 5 V regulator (VL) buffer capacitance (after DC-Bias derating) | 0.1 | 1 | 4.7 | µF |
| **BOOST CONVERTER** | | | | | |
| $V_{(AVDD)}$ | Boost output voltage range | 13.5 | | 19.8 | V |
| L | Boost inductor (inductor value that can be used) | 4.7 | 6.8 | 10 | µH |
| $C_I$ | Input capacitor placed at the inductor (ceramic capacitor value) | 4.7 | 10 | | µF |
| $C_{(SWI)}$ | Isolation Switch input capacitor (ceramic capacitor value) | 4.7 | 10 | 100 | µF |
| $C_{(SWO)}$ | Isolation Switch output capacitor (ceramic capacitor value) | 20 | 40 | 200 | µF |
| **BUCK 1 CONVERTER** | | | | | |
| $V_{(IO)}$ | Buck 1 output voltage range | 2.2 | | 3.7 | V |
| L | Buck 1 inductor (inductor value that can be used) | 4.7 | 6.8 | 10 | µH |
| $C_I$ | Buck 1 input capacitor (ceramic capacitor value) | 4.7 | 10 | | µF |
| $C_{OUT}$ | Buck 1 output capacitor (ceramic capacitor value) | 20 | 30 | 100 | µF |
| **BUCK 2 CONVERTER** | | | | | |
| $V_{(CORE)}$ | Buck 2 output voltage range | 0.8 | | 3.3 | V |
| L | Buck 2 inductor (inductor value that can be used) | 4.7 | 6.8 | 10 | µH |
| $C_I$ | Buck 2 input capacitor (ceramic capacitor value) | 4.7 | 10 | | µF |
| $C_{OUT}$ | Buck 2 output capacitor (ceramic capacitor value) | 10 | 20 | 50 | µF |
| **BUCK 3 CONVERTER** | | | | | |
| $V_{(HAVDD)}$ | Buck 3 output voltage range | 4.8 | | 11.1 | V |
| L | Buck 3 inductor (inductor value that can be used) | 4.7 | 6.8 | 10 | µH |
| $C_{IN}$ | Buck 3 input capacitor (ceramic capacitor value) | 4.7 | 10 | | µF |
| $C_{OUT}$ | Buck 3 output capacitor (ceramic capacitor value) | 4.7 | 10 | 50 | µF |
| **NEGATIVE CHARGE PUMP CONTROLLER** | | | | | |
| $V_{(GL)}$ | Controller output voltage range | –5.5 | | –14.5 | V |
| $C_{(FLY)}$ | Flying capacitor (ceramic capacitor value) | 0.1 | 0.47 | 4.7 | µF |
| $R_{(switch)}$ | Resistance to the switch pin | 0 | 2.2 | 20 | Ω |
| $C_{OUT}$ | Output capacitor (ceramic capacitor value) | 1 | 4.7 | 50 | µF |
| **POSITIVE CHARGE PUMP CONTROLLER** | | | | | |
| $V_{(GH)}$ | Controller output voltage range | 20 | | 40 | V |
| $V_{(GH_offset)}$ | Temperature compensation $V_{(GH)}$ positive offset | 0 | | 15 | V |
| $C_{(FLY)}$ | Flying capacitor (ceramic capacitor value) | 0.1 | 0.47 | 4.7 | µF |
| $R_{(switch)}$ | Resistance to the switch pin | 0 | 2.2 | 20 | Ω |
| $C_{OUT}$ | Output capacitor (ceramic capacitor value) | 1 | 4.7 | 50 | µF |
| **TEMPERATURE** | | | | | |
| $T_A$ | Operating ambient temperature | –40 | | 85 | °C |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC[(1)] | | RHA (VQFN) 40 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 32.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 20.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 7.9 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 7.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 2.6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.


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## 6.5 Electrical Characteristics

$V_I$ = 12 V, EN = 3.3 V, $V_{(AVDD)}$ = 18 V, $V_{(HAVDD)}$ = 9 V, $V_{(IO)}$ = 3.3 V, $V_{(CORE)}$ = 1.2 V, $V_{(GH)}$ = 28 V, $V_{(GL)}$ = –10.3 V, $T_A$ = –40°C to 85°C, typical values are at $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | | |
| $V_I$ | Operating input voltage | | | 8.6 | | 14.7 | V |
| $V_{IT+}$ | Undervoltage lockout threshold (UVLO) | | $V_I$ rising | 8 | 8.3 | 8.6 | V |
| $V_{IT-}$ | | | Hysteresis $V_I$ falling | | 0.75 | | V |
| | Thermal shutdown | | Junction temperature rising | | 150 | | ºC |
| **LOGIC SIGNALS** | | | | | | | |
| $V_{IH}$ | High-level input voltage | EN, HVS, SDA, SCL, A0, CTRL | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | EN, HVS, A0, CTRL | | | | 1 | V |
| | | SDA, SCL | | | | 0.9 | V |
| **INTERNAL REGULATOR** | | | | | | | |
| $V_{(VL)}$ | Internal supply | | | 4.9 | 5 | 5.1 | V |
| **ISOLATION SWITCH** | | | | | | | |
| $r_{DS(ON)}$ | MOSFET on-resistance | | $I_{(SWI)}$ = 1 A | | 100 | | mΩ |
| **BOOST CONVERTER ($V_{(AVDD)}$)** | | | | | | | |
| | Switching frequency | | | 600 | 750 | 900 | kHz |
| $V_{(AVDD)}$ | Output voltage range | | | 13.5 | 18 | 19 | V |
| | Output voltage range for max. 500h | | | | | 19.8 | V |
| | High Voltage Stress Mode $V_{(AVDD)}$ positive offset | | | 0 | | 3 | V |
| | Switch overvoltage protection | | At SW pin, $V_{(AVDD)}$ rising | 20.5 | | 22.5 | V |
| | Output voltage tolerance | | At $T_J$ = 0 ºC to 85 ºC | | | 1% | |
| | Feedback input bias current | | | | 350 | 600 | µA |
| $r_{DS(on)}$ | MOSFET on-resistance | | $I_{(SW)}$ = current limit | | 100 | 200 | mΩ |
| | MOSFET current limit | | At $T_J$ = 0 ºC to 85 ºC | 4.25 | 5 | 5.75 | A |
| | MOSFET current limit negative offset | | | 0 | | 2.8 | A |
| | Line Regulation | | 8.6 V ≤ $V_I$ ≤ 14.7 V, $I_{OUT}$ = 500 mA | | 0.001 | | %/V |
| | Load Regulation | | 1 mA ≤ $I_{OUT}$ ≤ 2 A | | 0.08 | | %/A |
| **BUCK1 CONERTER ($V_{(IO)}$)** | | | | | | | |
| | Switching frequency | | | 600 | 750 | 900 | kHz |
| $V_{(IO)}$ | Output voltage range | | | 2.2 | 3.3 | 3.7 | V |
| | Output voltage tolerance | | At $T_J$ = 0 ºC to 85ºC | | | 2% | |
| I | Feedback input bias current | | | | 10 | 200 | µA |
| $r_{DS(on)}$ | MOSFET on-resistance | | $I_{(SWBK1)}$ = current limit | | 200 | 300 | mΩ |
| | MOSFET current limit | | At $T_J$ = 0 ºC to 85 ºC | 2.8 | 3.5 | 4.2 | A |
| | Line Regulation | | 8.6 V ≤ $V_I$ ≤ 14.7 V, $I_{OUT}$ = 500 mA | | 0.002 | | %/V |
| | Load Regulation | | 1 mA ≤ $I_{OUT}$ ≤ 2 A | | 0.07 | | %/A |
| **BUCK2 CONVERTER ($V_{(CORE)}$)** | | | | | | | |
| | Switching frequency | | | 0.5 | 1 | 2 | MHz |
| $V_{(CORE)}$ | Output voltage range | | | 0.8 | 1.2 | 3.3 | V |
| | Output voltage tolerance | | At $T_J$ = 0 ºC to 85 ºC | | | 2% | |
| | Feedback input bias current | | | | 20 | 200 | µA |
| $r_{DS(on)}$ | MOSFET on-resistance | | $I_{(SWBK2)}$ = current limit | | 175 | 300 | mΩ |
| | MOSFET current limit | | At $T_J$ = 0 ºC to 85 ºC | 2.5 | 3 | 3.5 | A |
| | Line Regulation | | 2.2 V ≤ $V_I$ ≤ 3.7 V, $I_{OUT}$ = 500 mA | | 0.001 | | %/V |
| | Load Regulation | | 1 mA ≤ $I_{OUT}$ ≤ 1.5 A | | 0.2 | | %/A |

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## Electrical Characteristics (continued)

$V_I$ = 12 V, EN = 3.3 V, $V_{(AVDD)}$ = 18 V, $V_{(HAVDD)}$ = 9 V, $V_{(IO)}$ = 3.3 V, $V_{(CORE)}$ = 1.2 V, $V_{(GH)}$ = 28 V, $V_{(GL)}$ = –10.3 V, $T_A$ = –40°C to 85°C, typical values are at $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **BUCK3 CONVERTER ($V_{(HAVDD)}$)** | | | | | | |
| | Switching frequency | | 0.5 | 1 | 2 | MHz |
| $V_{(HAVDD)}$ | Output voltage range | | 4.8 | 9 | 11.1 | V |
| | Output Voltage Stress Mode $V_{(HAVDD)}$ positive offset | | 0 | | 1.5 | V |
| | Output voltage tolerance | At $T_J$ = 0 ºC to 85 ºC | | | 1.5% | |
| | Feedback input bias current | | | 90 | 200 | µA |
| $r_{DS(on)}$ | MOSFET on-resistance | $I_{(SWBK3)}$ = current limit | | 300 | 500 | mΩ |
| | MOSFET current limit | At $T_J$ = 0 ºC to 85 ºC | 1.2 | 1.5 | 1.8 | A |
| | Line Regulation | 8.6 V ≤ $V_I$ ≤ 14.7 V, $I_{OUT}$ = 500 mA | | 0.002 | | %/V |
| | Load Regulation | 1 mA ≤ $I_{OUT}$ ≤ 1 A | | 0.05 | | %/A |
| **NEGATIVE CHARGE PUMP CONTROLLER ($V_{(GL)}$)** | | | | | | |
| $V_{(GL)}$ | Output voltage range | | –5.5 | –10.3 | –14.5 | V |
| | Output voltage tolerance | At $T_J$ = 0 ºC to 85 ºC | | | 2.5% | |
| | Feedback input bias current | | | 50 | 200 | µA |
| $I_{(DRVN)}$ | Max. DRVN drive current | $V_{(DRVN)}$ = 0.6 V | 5 | | 10 | mA |
| | Resistor DRVN to GND | | 50 | 100 | 200 | kΩ |
| | Line Regulation | 8.6 V ≤ $V_I$ ≤ 14.7 V, $I_{OUT}$ = 50 mA | | 0.015 | | %/V |
| | Load Regulation | 1 mA ≤ $I_{OUT}$ ≤ 100 mA | | 0.002 | | %/mA |
| **POSITIVE CHARGE PUMP CONTROLLER ($V_{(GH)}$)** | | | | | | |
| $V_{(GH)}$ | Output voltage range | | 20 | 28 | 35 | V |
| $V_{(GH_offset)}$ | Temp. compensation $V_{(GH)}$ positive offset | $V_{(GH_offset)}$ = 8 V | 0 | 8 | 15 | V |
| | Max. output voltage including $V_{(GH_offset)}$ | | | | 40 | V |
| | Output voltage tolerance | At $T_J$ = 0 ºC to 85 ºC | | | 2.5% | |
| | Feedback input bias current | | | 120 | 200 | µA |
| $I_{(DRVP)}$ | Max. DRVP drive current | $V_{(DRVP)}$ = 17 V | 5 | | 10 | mA |
| | Line Regulation | 8.6 V ≤ $V_I$ ≤ 14.7 V, $I_{OUT}$ = 50 mA | | 0.001 | | %/V |
| | Load Regulation | 1 mA ≤ $I_{OUT}$ ≤ 100 mA | | 0.001 | | %/mA |
| **GATE PULSE MODULATION ($V_{(GHM)}$)** | | | | | | |
| | Gate Pulse Modulation falling limit | $V_{(GHM)}$ = 15 V | 0 | 5 | 15 | V |
| $r_{DS(ON)M1}$ | VGH to VGHM on-resistance | CTRL = 3.3 V, $I_{(VGHM)}$ = 20 mA, $V_{(GH)}$ = 28 V | | 3 | 5 | Ω |
| $r_{DS(ON)M2}$ | VGHM to RE on-resistance | CTRL = GND, $I_{(RE)}$ = 20 mA, $V_{(GHM)}$ = 15 V | | 3 | 5 | Ω |
| | CTRL to VGHM propagation delay | CTRL rising | 150 | 250 | 360 | ns |


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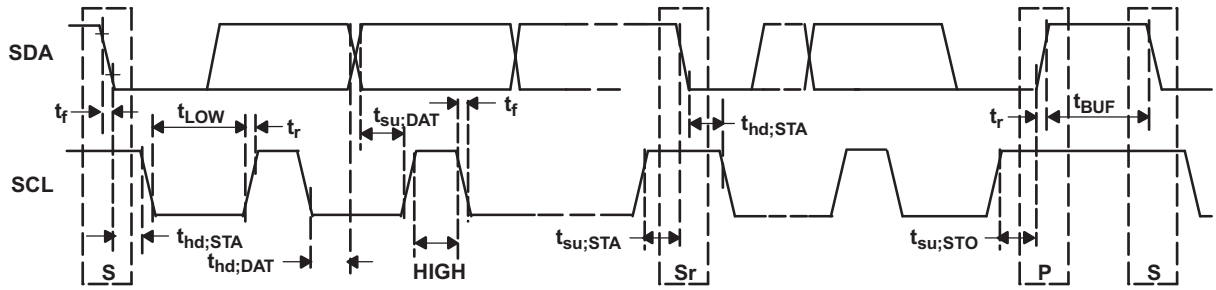
## 6.6 I²C Interface Timing Characteristics (1)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | Standard mode | | | 100 | kHz |
| | | Fast mode | | | 400 | kHz |
| | | Fast mode plus | | | 1 | MHz |
| $t_{LOW}$ | LOW period of the SCL clock | Standard mode | 4.7 | | | µs |
| | | Fast mode | 1.3 | | | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | Standard mode | 4.0 | | | µs |
| | | Fast mode | 600 | | | ns |
| $t_{BUF}$ | Bus free time between a STOP and START condition | Standard mode | 4.7 | | | µs |
| | | Fast mode | 1.3 | | | µs |
| $t_{hd:STA}$ | Hold time for a repeated START condition | Standard mode | 4.0 | | | µs |
| | | Fast mode | 600 | | | ns |
| $t_{su:STA}$ | Setup time for a repeated START condition | Standard mode | 4.7 | | | µs |
| | | Fast mode | 600 | | | ns |
| $t_{su:STO}$ | Setup time for STOP condition | Standard mode | 4.0 | | | µs |
| | | Fast mode | 600 | | | ns |
| $t_{hd:DAT}$ | Data hold time | Standard mode | 0 | | 3.45 | µs |
| | | Fast mode | 0 | | 0.9 | µs |
| $t_{su:DAT}$ | Data setup time | Standard mode | 250 | | | ns |
| | | Fast mode | 100 | | | ns |
| $C_B$ | Capacitive load for SDA and SCL | | | | 400 | pF |
| $t_{RCL1}$ | Rise time of SCL signal after a repeated START condition and after an acknowledge bit | Standard mode | $20 + 0.1C_B$ | | 1000 | ns |
| | | Fast mode | $20 + 0.1C_B$ | | 1000 | ns |
| $t_{RCL}$ | Rise time of SCL signal | Standard mode | $20 + 0.1C_B$ | | 1000 | ns |
| | | Fast mode | $20 + 0.1C_B$ | | 300 | ns |
| $t_{FCL}$ | Fall time of SCL signal | Standard mode | $20 + 0.1C_B$ | | 300 | ns |
| | | Fast mode | $20 + 0.1C_B$ | | 300 | ns |
| $t_{RDA}$ | Rise time of SDA signal | Standard mode | $20 + 0.1C_B$ | | 1000 | ns |
| | | Fast mode | $20 + 0.1C_B$ | | 300 | ns |
| $t_{FDA}$ | Fall time of SDA signal | Standard mode | $20 + 0.1C_B$ | | 300 | ns |
| | | Fast mode | $20 + 0.1C_B$ | | 300 | ns |

(1) Industry standard I²C timing characteristics. Not tested in production.

## 6.7 I²C Timing Diagram



## 6.8 Typical Characteristics

$V_I$ = 12 V unless otherwise noted.

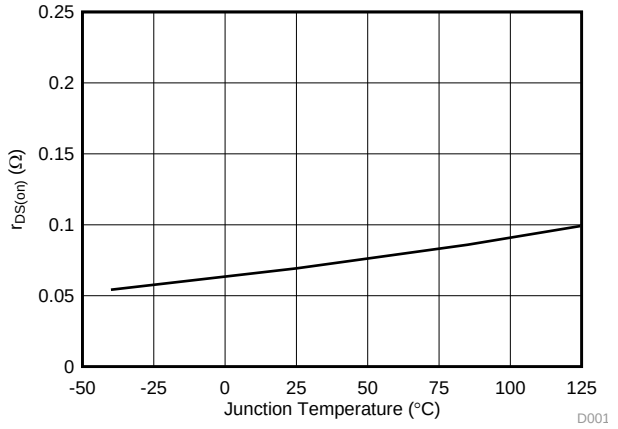



**Figure 1. $V_{(AVDD)}$ Boost Converter NMOS $r_{DS(on)}$**

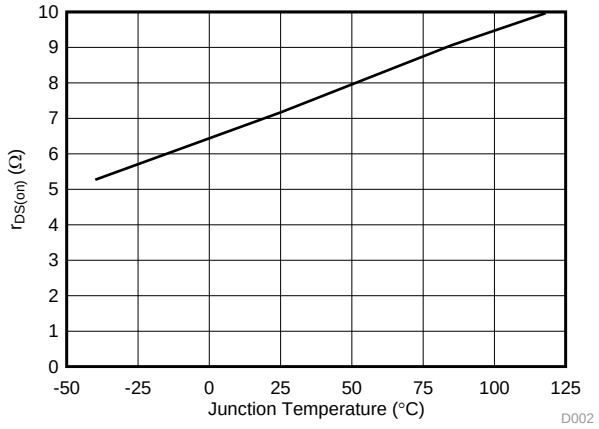



**Figure 2. $V_{(AVDD)}$ Boost Converter PMOS $r_{DS(on)}$**

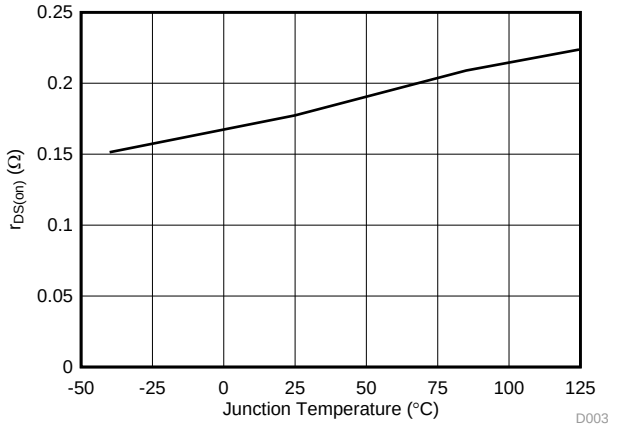



**Figure 3. $V_{(IO)}$ Buck 1 Converter NMOS $r_{DS(on)}$**

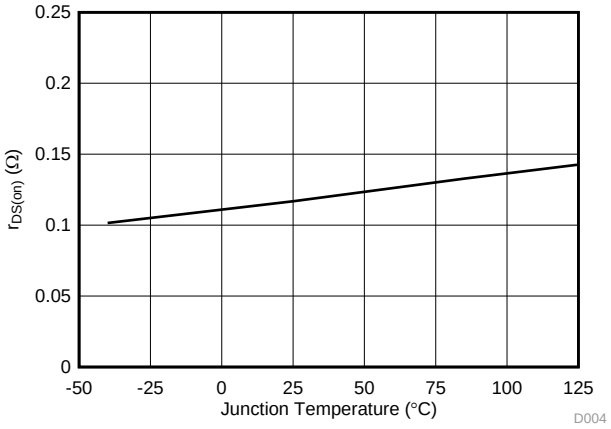



**Figure 4. $V_{(CORE)}$ Buck 2 Converter NMOS $r_{DS(on)}$**

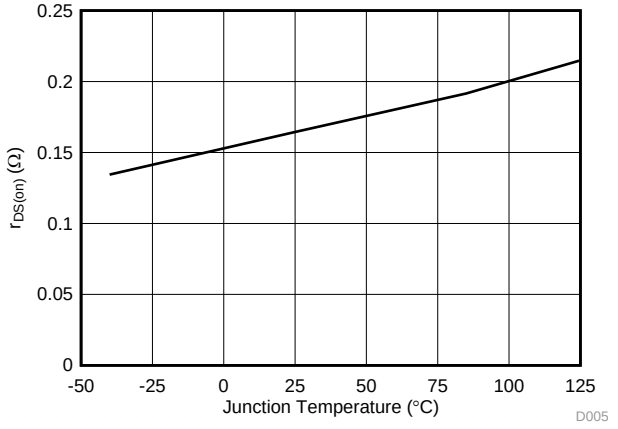



**Figure 5. $V_{(CORE)}$ Buck 2 Converter PMOS $r_{DS(on)}$**

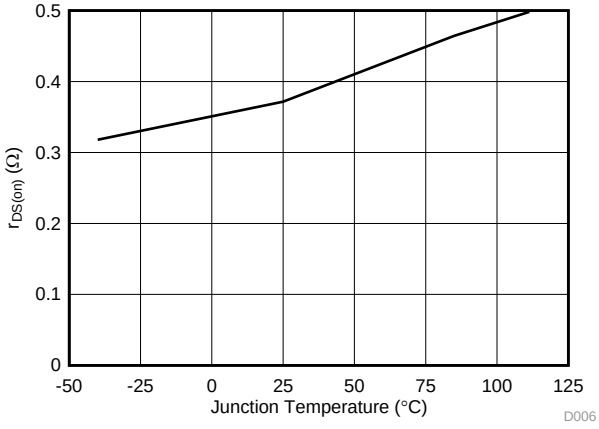



**Figure 6. $V_{(HAVDD)}$ Buck 3 Converter NMOS $r_{DS(on)}$**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## Typical Characteristics (continued)

$V_I$ = 12 V unless otherwise noted.

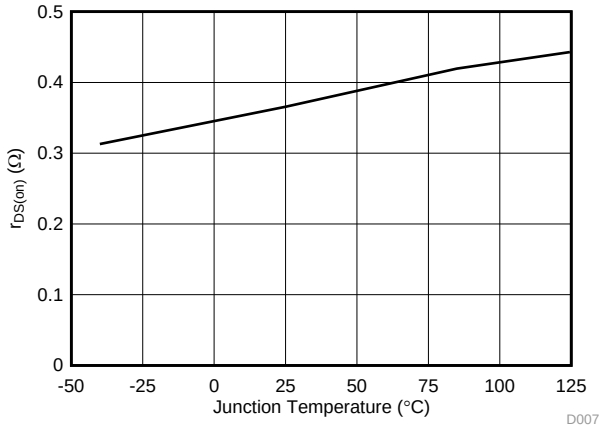


**Figure 7. $V_{(HAVDD)}$ Buck 3 Converter PMOS $r_{DS(on)}$**

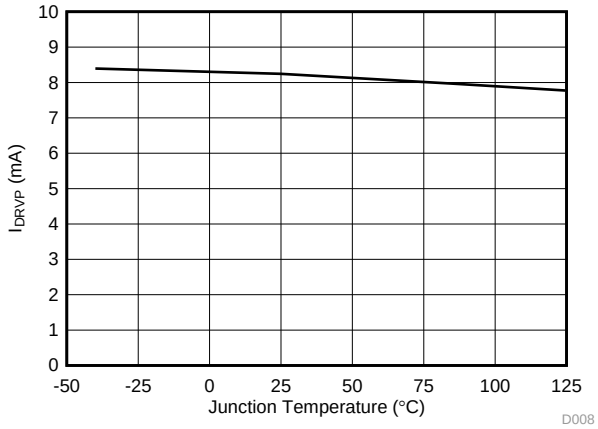


**Figure 8. $V_{(GH)}$ charge-pump DRVP drive current**

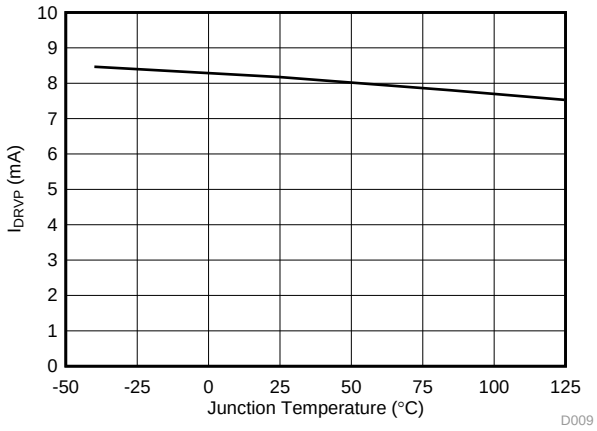


**Figure 9. $V_{(GL)}$ charge-pump DRVN drive current**

# 7 Detailed Description

## 7.1 Overview

The TPS65177/A provides all supply rails needed by a GIP (Gate-in-Panel) or non-GIP TFT-LCD panel. All output voltages are $I^2C$ programmable.

$V_{(IO)}$ and $V_{(CORE)}$ for the T-CON, $V_{(AVDD)}$ and $V_{(HAVDD)}$ for the Source Driver and the Gamma Buffer, $V_{(GH)}$ and $V_{(GL)}$ for the Gate Driver or the Level Shifter. For use with non-GIP technology Gate Pulse Modulation (GPM) is implemented, for use with GIP technology the $V_{(GH)}$ rail can be temperature compensated. Furthermore a High Voltage Stress Mode (HVS) for $V_{(AVDD)}$ and $V_{(HAVDD)}$ and an integrated $V_{(AVDD)}$ Isolation Switch is implemented. $V_{(CORE)}$, $V_{(HAVDD)}$, $V_{(GH)}$, $V_{(GL)}$, GPM and the $V_{(GH)}$ temperature compensation can be enabled and disabled by $I^2C$ programming.

A single BOM (Bill of Materials) can cover several panel types and sizes whose desired output voltage levels can be programmed in production and stored in a non-volatile integrated memory.


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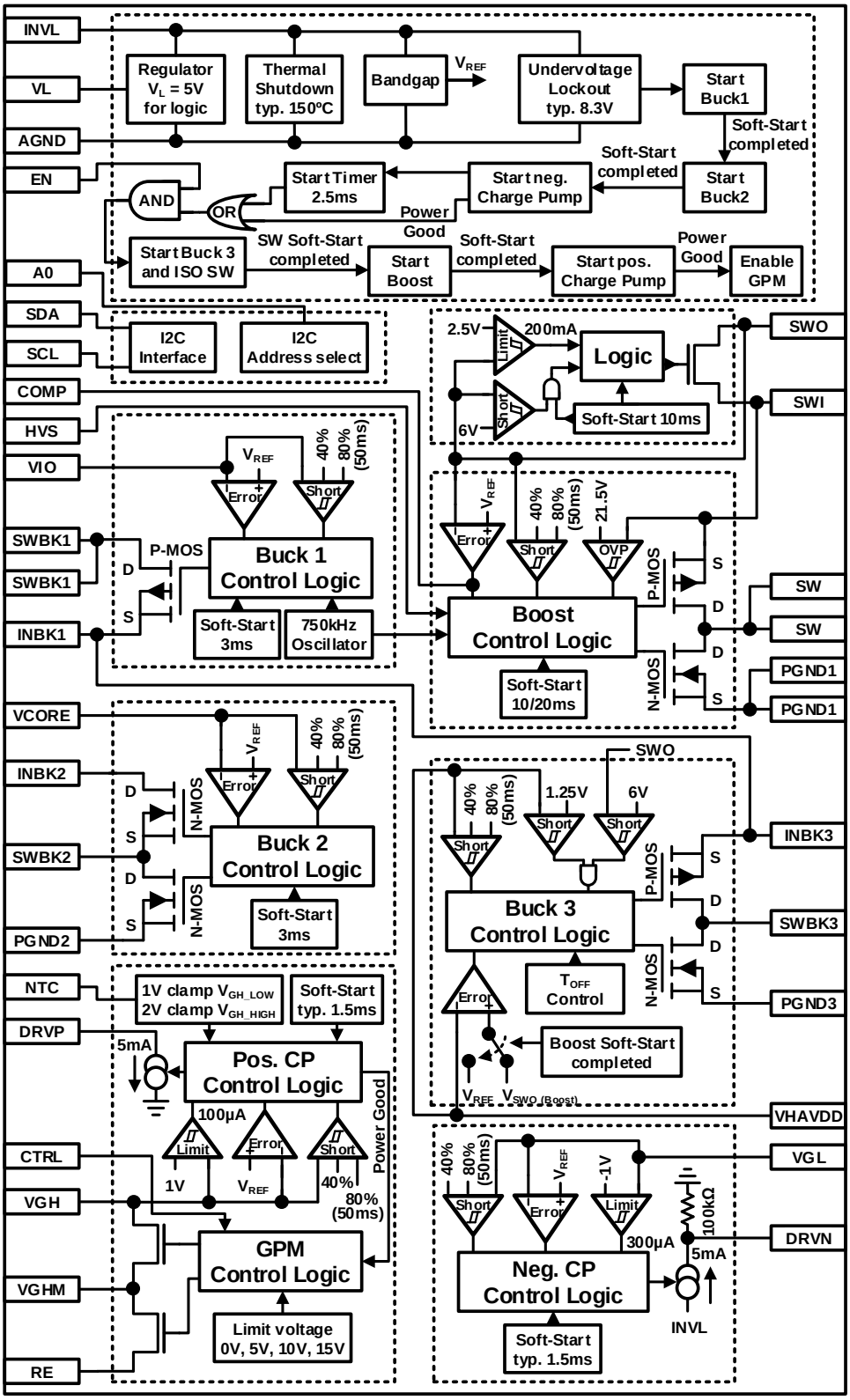
## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Power-Up

When $V_I$ rises above the UVLO (undervoltage lockout) the device loads the stored values in the non-volatile Initial Value register into the volatile DAC register. When all data is written the power-up sequencing starts with enabling the buck 1 converter ($V_{(IO)}$), which ramps up its output voltage in 3 ms. When the output is in regulation the buck 2 converter ($V_{(CORE)}$) starts and ramps up its output voltage in 3 ms, when its output voltage is in regulation the negative charge pump controller starts and $V_{(GL)}$ is declining in typ. 1.5 ms until the output voltage is in regulation. In case $V_{(GL)}$ is driven by the boost switch pin (SW) $V_{(GL)}$ starts declining when the boost starts switching.

When the enable pin (EN) is pulled “high” the isolation switch closes smoothly so that after typ. 10 ms its output ($V_{(AVDD)}$) is at $V_I$ level, then the boost converter ($V_{(AVDD)}$) starts and its output voltage ($V_{(AVDD)}$) ramps linearly in 10 ms or 20 ms (programmable by $I^2C$) until it is in regulation. Then the positive charge pump controller starts and $V_{(GH)}$ is rising in typ. 1.5 ms until the output voltage is in regulation. To ensure proper sequencing even if EN is pulled “high” already at the beginning (e.g. connected to $V_I$) the start of the boost converter $V_{(AVDD)}$ is blocked until $V_{(GL)}$ is Power Good or 2.5 ms have passed since $V_{(GL)}$ was enabled.

If the EN pin is not connected to $V_I$, the device detects a collapsed $V_{(AVDD)}$ voltage about 40 ms after EN is pulled low. This function prevents the panel to restart without a proper power supply reset. The device partially shuts down as described in the *Short-Circuit and Overload Protection* section. The device is in a latched state and only a power cycle can restart the $V_{(AVDD)}$, $V_{(HAVDD)}$, $V_{(GH)}$ and $V_{(GL)}$ rail.

When $V_{(GL)}$ is driven by the boost switch pin (SW) the EN-pin should be connected to $V_I$, otherwise $V_{(GL)}$ detects a short when EN is pulled low as the $V_{(GL)}$ voltage collapses. $V_{(GL)}$ collapses because the supporting switch node (SW) stops switching and the device partially shuts down as described in the *Short-Circuit and Overload Protection* section. The device is in a latched state and only a power cycle can restart the $V_{(AVDD)}$, $V_{(HAVDD)}$, $V_{(GH)}$ and $V_{(GL)}$ rail.

The buck 2 and buck 3 converter as the negative and positive charge pump controller can be disabled by $I^2C$. If disabled they are skipped in the sequencing (e.g. disabled buck 2 → buck 1 is in regulation → start neg. CP).

The Gate Pulse Modulation block is disabled when $V_I$ is below UVLO or EN is “low” and enabled when $V_{(GH)}$ is in regulation. When the block is disabled by UVLO the high side switch of the Gate Pulse Modulation is turned on and the output VGHM is connected to the VGH pin, when the block is disabled by pulling the EN pin “low” the low side switch is turned on and the output VGHM is connected to the RE pin.

#### *7.3.1.1 TPS65177*

If the EN pin is not connected to $V_I$, the device detects a collapsed $V_{(AVDD)}$ voltage about 40 ms after EN is pulled low. This function prevents the panel to restart without a proper power supply reset. The device partially shuts down as described in the *Short-Circuit and Overload Protection* section. The device is in a latched state and only a power cycle can restart the $V_{(AVDD)}$, $V_{(HAVDD)}$, $V_{(GH)}$ and $V_{(GL)}$ rail.

#### *7.3.1.2 TPS65177A*

The device can be restarted without a power cycle, however note that when $V_{(GL)}$ is driven by the boost switch pin (SW) the EN-pin should be connected to $V_I$. If the EN-pin is not connected to $V_I$ the $V_{(GL)}$ protection detects a short when EN is pulled low as the $V_{(GL)}$ voltage collapses. $V_{(GL)}$ collapses because the supporting switch node (SW) stops switching and the device partially shuts down as described in the *Short-Circuit and Overload Protection* section. The device is in a latched state and only a power cycle can restart the $V_{(AVDD)}$, $V_{(HAVDD)}$, $V_{(GH)}$ and $V_{(GL)}$ rail.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## Feature Description (continued)

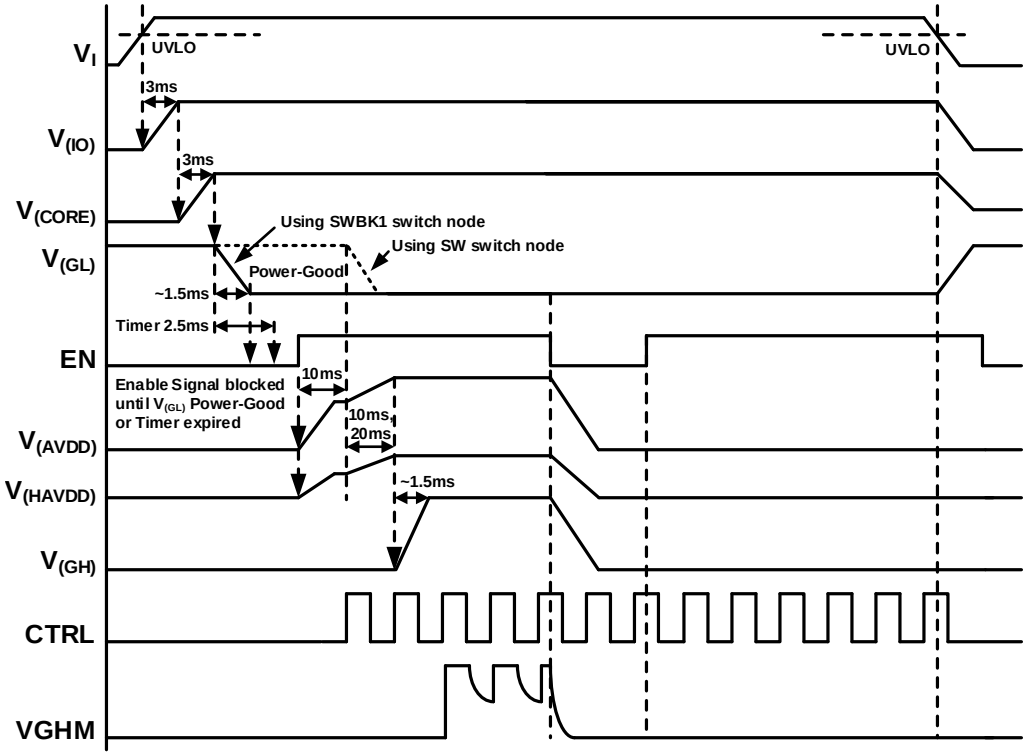


**Figure 10. TPS65177 Power-up Sequencing**

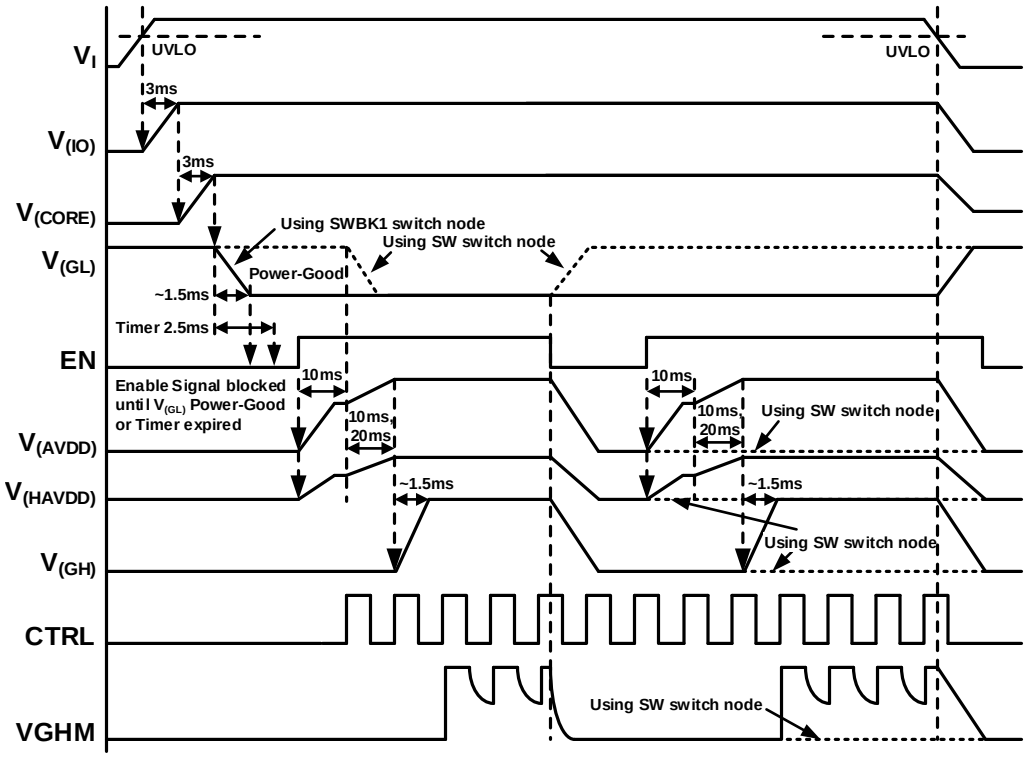


**Figure 11. TPS65177A Power-up Sequencing**

## Feature Description (continued)

### 7.3.2 Power-Down

When $V_I$ falls below the UVLO threshold all blocks are disabled and the discharge rate is given by the output load and the output capacitors. The Gate Pulse Modulation output $V_{(GHM)}$ follows $V_{(GH)}$.

### 7.3.3 Thermal Shutdown

A thermal shutdown is implemented to prevent damage because of excessive heat and power dissipation. Once a temperature of typically 150 ºC is exceeded the device shuts down and stays off. $V_I$ must fall below Undervoltage lockout threshold (UVLO) to reset the thermal shutdown.

### 7.3.4 Undervoltage Lockout

To avoid mis-operation of the device at low input voltages an undervoltage lockout is included, which shuts down the device at voltages lower than typically 8.3 V.

### 7.3.5 Short-Circuit and Overload Protection

#### *7.3.5.1 Boost Converter ($V_{(AVDD)}$):*

| | | |
|---|---|---|
| When $V_{(SWO)}$ < 40% of its nominal value | → | Shut down Boost, Isolation Switch, Buck3, neg. and pos. Charge Pump controller (Buck 1 and Buck 2 keep working) → latched condition, only triggering UVLO enables the device again. |
| When $V_{(SWO)}$ < 80% of its nominal value for longer than 50 ms (overload) | → | Shut down Boost, Isolation Switch, Buck3, neg. and pos. Charge Pump controller (Buck 1 and Buck 2 keep working) → latched condition, only triggering UVLO enables the device again. |

#### *7.3.5.2 Buck 1 Converter ($V_{(IO)}$):*

| | | |
|---|---|---|
| When $V_{(IO)}$ < 40% of its nominal value | → | Shut down the whole device → latched condition, only triggering UVLO enables the device again. |
| When $V_{(IO)}$ < 80% of its nominal value for longer than 50 ms (overload) | → | Shut down the whole device → latched condition, only triggering UVLO enables the device again. |

#### *7.3.5.3 Buck 2 Converter ($V_{(CORE)}$):*

| | | |
|---|---|---|
| When $V_{(CORE)}$ < 40% of its nominal value | → | Shut down the whole device → latched condition, only triggering UVLO enables the device again. |
| When $V_{(CORE)}$ < 80% of its nominal value for longer than 50 ms (overload) | → | Shut down the whole device → latched condition, only triggering UVLO enables the device again. |

#### *7.3.5.4 Buck 3 Converter ($V_{(HAVDD)}$):*

| | | |
|---|---|---|
| When $V_{(HAVDD)}$ < 40% of its nominal value | → | Shut down Buck3, Isolation Switch, Boost, neg. and pos. Charge Pump controller (Buck 1 and Buck 2 keep working) → latched condition, only triggering UVLO enables the device again. |


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## Feature Description (continued)

| | | |
|---|---|---|
| When $V_{(HAVDD)}$ < 80% of its nominal value for longer than 50 ms (overload) | → | Shut down Buck3, Isolation Switch, Boost, neg. and pos. Charge Pump controller (Buck 1 and Buck 2 keep working) → latched condition, only triggering UVLO enables the device again. |

#### *7.3.5.5 Positive Charge-Pump Controller ($V_{(GH)}$):*

| | | |
|---|---|---|
| When $V_{(GH)}$ < 40% of its nominal value | → | Shut down pos. Charge Pump, Isolation Switch, Boost, Buck3, neg. Charge Pump controller (Buck1 and Buck2 keep working) → latched condition, only triggering UVLO enables the device again. |
| When $V_{(GH)}$ < 80% of its nominal value for longer than 50 ms (overload) | → | Shut down pos. Charge Pump, Isolation Switch, Boost, Buck3, neg. Charge Pump controller (Buck1 and Buck2 keep working) → latched condition, only triggering UVLO enables the device again. |

#### *7.3.5.6 Negative Charge-Pump Controller ($V_{(GL)}$):*

| | | |
|---|---|---|
| When $V_{(GL)}$ < 40% of its nominal value | → | Shut down neg. Charge Pump, Isolation Switch, Boost, Buck3, pos. Charge Pump controller (Buck1 and Buck2 keep working) → latched condition, only triggering UVLO enables the device again. |
| When $V_{(GL)}$ < 80% of its nominal value for longer than 50 ms (overload) | → | Shut down neg. Charge Pump, Isolation Switch, Boost, Buck3, pos. Charge Pump controller (Buck1 and Buck2 keep working) → latched condition, only triggering UVLO enables the device again. |

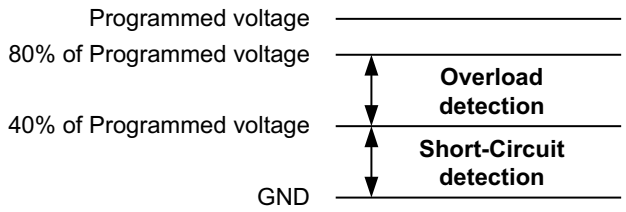


**Figure 12. Short-Circuit Levels Overview**

## 7.4 Device Functional Modes

### 7.4.1 Boost Converter ($V_{(AVDD)}$)

The quasi-synchronous current mode boost converter operates with Pulse Width Modulation (PWM) with a fixed frequency of 750 kHz. For maximum design flexibility and stability with different external components, the converter uses external loop compensation by a simple RC circuit. The converter has an input-to-output switch at the output rail to disconnect its output.

#### *7.4.1.1 Soft-Start*

The boost converter is enabled by the EN-pin, the startup is done in two steps:

1. **Input-to-output isolation switch soft-start**
   The isolation switch is turned on slowly in 10 ms
2. **Boost converter soft-start**
   When the isolation switch is fully turned on (after 10 ms) the boost converter starts switching and ramps up

## Device Functional Modes (continued)

its output voltage $V_{(AVDD)}$ from $V_I$ to the programmed voltage value in 10 or 20 ms (programmable by I2C).

#### *7.4.1.2 Compensation*

The regulator loop can be compensated by adjusting the external RC circuit connected to the COMP pin. The COMP-pin is the output of the transconductance error amplifier. The compensation capacitor adjusts the low frequency gain and the resistor the high frequency gain. Lower output voltages require a higher gain and therefore a smaller compensation capacitor. A good start working for most applications is $C_{(COMP)}$ = 470 pF and $R_{(COMP)}$ = 75 kΩ. In case of a high noise level an additional 22-pF capacitor can be put between the COMP-pin and GND to filter the high frequency noise. The cut-off frequency can be calculated as follows:

$$f_Z = \frac{1}{2 \times \pi \times R_{COMP} \times C_{COMP}} \tag{1}$$

#### *7.4.1.3 Setting the Output Voltage $V_{(AVDD)}$*

The output voltage is programmable by $I^2C$ between 13.5 V and 19.8 V in 100 mV steps.

#### *7.4.1.4 High Voltage Stress Mode (HVS)*

By pulling the HVS-pin "high" an $I^2C$ programmable offset voltage is added to the set boost and buck 3 converters output voltage $V_{(AVDD)}$ and $V_{(HAVDD)}$. The offset voltages are programmable independently.

#### *7.4.1.5 Programmable Current Limit*

The current limit of typ. 5 A can be reduced by $I^2C$ programming in 400 mA steps down to 2.2 A to support smaller inductors with lower saturation current.

#### *7.4.1.6 Design Procedure*

The first step in the design procedure is to verify whether the maximum possible output current of the boost converter supports the specific application requirements.

1. Converter Duty Cycle: $D = 1 - \frac{V_{IN} \times \eta}{V_{AVDD}}$
2. Inductor ripple current: $\Delta I_L = \frac{V_{IN} \times D}{f_s \times L}$
3. Maximum output current: $I_{OUT_max} = \left( I_{LIM_min} - \frac{\Delta I_L}{2} \right) \times (1 - D)$
4. Peak switch current: $I_{SWPEAK} = \frac{I_{OUT}}{1 - D} + \frac{\Delta I_L}{2}$

η = Estimated boost converter efficiency (use the number from the efficiency plots or 0.9 as an estimation)
$f_s$ = Switching frequency (typ. 750 kHz)
L = Selected inductor value (typ. 6.8 µH)
$I_{LIM_min}$: Minimum current limit
$I_{SWPEAK}$ = Peak switch current for the used output current (must be < $I_{LIM_min}$ = 4.25 A)
$\Delta I_L$ = Inductor peak-to-peak ripple current

The peak switch current $I_{SWPEAK}$ is the current that the integrated switch, the inductor and the external Schottky diode have to be able to handle. The calculation must be done for the minimum input voltage where the peak switch current is the highest.


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## Device Functional Modes (continued)

### 7.4.1.7 Inductor Selection

| | | |
|---|---|---|
| **Inductor value:** | 4.7 µH ≤ L ≤ 10 µH | The higher the inductor value the lower the inductor current ripple and the output voltage ripple but the slower the transient response. |
| **Saturation current:** | $I_{SAT} \geq I_{SWPEAK}$ or $I_{SAT} \geq I_{LIM_max}$ | The inductor saturation current must be higher than the switch peak current for the max. peak output current or as a more conservative approach higher than the max. switch current limit. |
| **DC resistance:** | The lower the inductors resistance the lower the losses and the higher the efficiency. | |

| INDUCTANCE | SUPPLIER(1) | COMPONENT CODE | SIZE (L x W x H mm) | DCR Typ. (mΩ) | $I_{SAT}$ (A) |
|---|---|---|---|---|---|
| 6.8 µH | Sumida | CDRH105R | 10.5 x 10.3 x 5.1 | 14 | 5.4 |
| 6.8 µH | Sumida | CDRH10D43R | 10.8 x 10.5 x 4.5 | 20 | 7 |
| 10 µH | Sumida | CDRH10D43R | 10.8 x 10.5 x 4.5 | 26 | 5.2 |
| 6.8 µH | Chilisin | SCDS105R | 10.5 x 10.3 x 5.1 | 14 | 5.4 |
| 6.8 µH | Chilisin | SCDS104R | 10.5 x 10.3 x 4 | 21 | 5 |
| 10 µH | Chilisin | SCDS105R | 10.5 x 10.3 x 5.1 | 22 | 4.45 |

(1) See *Third-Party Products* disclaimer

### 7.4.1.8 Rectifier Diode Selection

#### 7.4.1.8.1 Diode Type

Schottky or Super Barrier Rectifier (SBR) for better efficiency

#### 7.4.1.8.2 Forward Voltage

The lower the forward voltage $V_F$ the higher the efficiency and the lower the diode temperature.

#### 7.4.1.8.3 Reverse Voltage

$V_R$ must be higher than the output voltage and should be higher than the OVP voltage 22.5 V

#### 7.4.1.8.4 Thermal Characteristics

The diode must be able to handle the dissipated power of:

$$P_D = V_F \times I_{OUT} \quad (2)$$

**Table 1. Diodes**

| $V_R$ / $I_{AVG}$ | $V_F$ Typ. at 25°C | COMPONENT CODE | $R_{\theta JL}$ | SIZE | SUPPLIER(1) |
|---|---|---|---|---|---|
| 30 V / 3 A | 0.39 V at 3 A | SBR3U30P1 | 5 °C/W | PowerDI® 123 | Diodes |
| 30 V / 3 A | 0.39 V at 3 A | SSM33LSPT | 18 °C/W | SMA-S | Chenmko |
| 40 V / 3 A | 0.38 V at 3 A | SSM34LAS | 18 °C/W | SMA-S | Chenmko |
| 40 V / 2 A | 0.5 V at 2 A | SSM24APT | 20 °C/W | SMA-S | Chenmko |

(1) See *Third-Party Products* disclaimer

### 7.4.1.9 Output Capacitor Selection

For best output voltage filtering, low ESR ceramic capacitors are recommended. Four 10 µF (or two 22 µF) ceramic capacitors work for most applications. To improve the load transient response more capacitance can be added. Between the rectifier diode and the SWI-pin one 10 µF capacitor is required.

To calculate the output voltage ripple the following equations can be used:

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$$\Delta V_{C_RIPPLE} = \frac{V_{AVDD} - V_{IN}}{V_{AVDD} \times f_S} \times \frac{I_{OUT}}{C_{OUT}} + \Delta V_{C_ESR} \qquad \Delta V_{C_ESR} = I_{SWPEAK} \times R_{C_ESR} \tag{3}$$

| CAPACITOR | VOLTAGE RATING | TEMPERATURE CHARACTERISTICS | SUPPLIER(1) | COMPONENT CODE |
|---|---|---|---|---|
| 10 µF / 1206 | 25 V | X5R | Murata | GRM31CR61E106KA12 |
| 10 µF / 1206 | 25 V | X7R | Taiyo Yuden | TMK316AB7106KL |

(1) See *Third-Party Products* disclaimer.

### 7.4.2 Buck 1 Converter ($V_{(IO)}$)

The non-synchronous current mode buck 1 converter operates with Pulse Width Modulation (PWM) with a fixed frequency of 750 kHz. The converter features integrated soft-start, bootstrap and compensation to minimize external component and pin count.

The buck 1 converter operates in Discontinuous Conduction Mode (DCM) or Continuous Conduction Mode (CCM) depending on the load current. For low load currents the converter operates in DCM. In this mode the inductor current reaches 0 A when the switch is turned off. With increasing load current the inductor current finally does not reach 0 A anymore but is always positive and then the converter operates in CCM. The switch node waveforms for DCM and CCM operation are shown in Figure 23 and Figure 24. The ringing during DCM (at light load) is normal for this operating mode, it occurs because of parasitic capacitance in the PCB layout. Because there is very little energy contained in the ringing waveform it does not significantly affect EMI performance.

Minimum output current for DCM: $I_{DCM} = \frac{V_{IN} - V_{IO}}{2 \times L \times f_S} \times \frac{V_{IO}}{V_{IN}}$

For low load currents when the minimum on time is not sufficient, the buck 1 converter uses a skip mode to be able to regulate its output voltage $V_{(IO)}$. During the skip mode the converter switches for a few cycles to raise the output voltage then it stops switching until the output voltage falls below a given threshold and the converter starts switching again. Due to this behavior the output voltage ripple can be slightly higher during skip mode.

#### *7.4.2.1 Soft-Start*

The buck 1 converter is enabled with the undervoltage lockout (UVLO). It starts switching and ramps up its output voltage $V_{(IO)}$ linearly in 3 ms to the programmed voltage value.

#### *7.4.2.2 Setting the Output Voltage $V_{(IO)}$*

The output voltage is programmable by $I^2C$ between 2.2 V and 3.7 V in 100 mV steps.

#### *7.4.2.3 Design Procedure*

The first step in the design procedure is to verify whether the maximum possible output current of the buck 1 converter supports the specific application requirements. Because the buck 2 converter is supplied by the buck 1 converter and the negative charge pump is driven from the buck 1 converter's switch node the effective output current $I_{(IO)}$ is higher than the buck 1 output current alone.

1. Converter Duty Cycle: $D = \frac{V_{IO}}{V_{IN} \times \eta}$
2. Inductor ripple current: $\Delta I_L = \frac{(V_{IN} - V_{IO}) \times D}{f_S \times L}$
3. Maximum output current: $I_{OUT_max} = I_{LIM_min} - \frac{\Delta I_L}{2}$
4. Peak switch current: $I_{SWPEAK} = I_{OUT} + \frac{\Delta I_L}{2}$
5. Effective output current: $I_{BUCK1_EFFECTIVE} = I_{OUT_BUCK1} + I_{IN_BUCK2} + \frac{V_{IN} \times I_{GL}}{V_{IO}}$


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η = Estimated boost converter efficiency (use the number from the efficiency plots or 0.8 as an estimation)
$f_s$ = Switching frequency (typ. 750 kHz)
L = Selected inductor value (typ. 6.8 µH)
$I_{LIM_min}$: Minimum current limit (3 A)
$I_{SWPEAK}$ = Peak switch current for the used output current (must be < $I_{LIM_min}$ = 3 A)
$\Delta I_L$ = Inductor peak-to-peak ripple current

The peak switch current $I_{SWPEAK}$ is the current that the integrated switch, the inductor and the external Schottky diode have to be able to handle. The calculation must be done for the maximum input voltage where the peak switch current is the highest.

#### *7.4.2.4 Inductor Selection*

| | | |
|---|---|---|
| **Inductor value:** | 4.7 µH ≤ L ≤ 10 µH | The higher the inductor value the lower the inductor current ripple and the output voltage ripple but the slower the transient response. |
| **Saturation current:** | $I_{SAT} \geq I_{SWPEAK}$ or $I_{SAT} \geq I_{LIM_max}$ | The inductor saturation current must be higher than the switch peak current for the max. peak output current or as a more conservative approach higher than the max. switch current limit. |
| **DC resistance:** | The lower the inductors resistance the lower the losses and the higher the efficiency. | |

| INDUCTANCE | SUPPLIER(1) | COMPONENT CODE | SIZE (L x W x H mm) | DCR Typ. (mΩ) | $I_{SAT}$ (A) |
|---|---|---|---|---|---|
| 6.8 µH | Sumida | CDRH8D43 | 8.3 x 8.3 x 4.5 | 20 | 4.4 |
| 10 µH | Sumida | CDRH8D43 | 8.3 x 8.3 x 4.5 | 29 | 4 |
| 6.8 µH | Chilisin | SCPS0740T | 7.5 x 7.8 x 4 | 28 | 3.9 |

(1) See *Third-Party Products* disclaimer

#### *7.4.2.5 Rectifier Diode Selection*

##### 7.4.2.5.1 Diode Type

Schottky or Super Barrier Rectifier (SBR) for better efficiency

##### 7.4.2.5.2 Forward Voltage

The lower the forward voltage $V_F$ the higher the efficiency and the lower the diode temperature.

##### 7.4.2.5.3 Reverse Voltage

$V_R$ must be higher than the output voltage

##### 7.4.2.5.4 Forward Current

The average rectified forward current $I_{AVG}$ must be higher than $I_{OUT} \times (1 – D)$

##### 7.4.2.5.5 Thermal Characteristics

The diode must be able to handle the dissipated power of:

$$P_D = V_F \times I_{OUT} \times (1 – D) \quad (4)$$

**Table 2. Diodes**

| $V_R$ / $I_{AVG}$ | $V_F$ typ. at 25°C | COMPONENT CODE | $R_{\theta JL}$ | SIZE | SUPPLIER(1) |
|---|---|---|---|---|---|
| 30 V / 3 A | 0.39 V at 3 A | SBR3U30P1 | 5 °C/W | PowerDI® 123 | Diodes |
| 30 V / 3 A | 0.39 V at 3 A | SSM33LSPT | 18 °C/W | SMA-S | Chenmko |
| 40 V / 3 A | 0.38 V at 3 A | SSM34LAS | 18 °C/W | SMA-S | Chenmko |
| 40 V / 2 A | 0.5 V at 2 A | SSM24APT | 20 °C/W | SMA-S | Chenmko |

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#### 7.4.2.6 Output Capacitor Selection

For best output voltage filtering low ESR ceramic capacitors are recommended. Three 10 µF (or two 22 µF) ceramic capacitors work for most applications. To improve the load transient response more capacitance can be added.

To calculate the output voltage ripple the following equations can be used:

$$\Delta V_{C_RIPPLE} = \frac{V_{IO}}{V_{IN} \times f_S} \times \frac{I_{OUT}}{C_{OUT}} + \Delta V_{C_ESR} \qquad \Delta V_{C_ESR} = I_{SW\,PEAK} \times R_{C_ESR} \tag{5}$$

| CAPACITOR | VOLTAGE RATING | TEMPERATURE CHARACTERISTICS | SUPPLIER (1) | COMPONENT CODE |
|---|---|---|---|---|
| 10 µF / 1206 | 6.3 V | X5R | Murata | GRM219R60J106KE19 |
| 10 µF / 1206 | 6.3 V | X7R | Taiyo Yuden | JMK212AB7106KG |

(1) See *Third-Party Products* disclaimer

### 7.4.3 BUCK 2 CONVERTER ($V_{(CORE)}$)

The synchronous current mode buck 2 converter operates with Pulse Frequency Modulation (PFM) with a fixed off-time and a typ. frequency of 1 MHz. The converter features integrated soft-start, bootstrap and compensation to minimize external component and pin count. It is supplied by the buck 1 converter's output.

If not needed the buck 2 converter can be disabled by $I^2C$.

#### 7.4.3.1 Soft-Start

The buck 2 converter is enabled when the buck 1 converter is in regulation. It starts switching and ramps up its output voltage $V_{(CORE)}$ linearly in 3ms to the programmed voltage value.

#### 7.4.3.2 Setting the Output Voltage $V_{(CORE)}$

The output voltage is programmable by $I^2C$ between 0.8 V and 3.3 V in 100 mV steps.

#### 7.4.3.3 Design Procedure

The first step in the design procedure is to verify whether the maximum possible output current of the buck 2 converter supports the specific application requirements.

1. Switching frequency: $f_S = \frac{(V_{IO} - V_{CORE}) \times (1.17 V_{CORE} + 0.22)}{V_{IO}} \text{MHz}$
2. Converter Duty Cycle: $D = \frac{V_{CORE}}{V_{IO} \times \eta}$
3. Inductor ripple current: $\Delta I_L = \frac{(V_{IO} - V_{CORE}) \times D}{f_S \times L}$
4. Maximum output current: $I_{OUT_max} = I_{LIM_min} - \frac{\Delta I_L}{2}$
5. Peak switch current: $I_{SWPEAK} = I_{OUT} + \frac{\Delta I_L}{2}$

η = Estimated boost converter efficiency (use the number from the efficiency plots or 0.8 as an estimation)
L = Selected inductor value (typ. 6.8 µH)
$I_{LIM_min}$: Minimum current limit (2.5A)
$I_{SWPEAK}$ = Peak switch current for the used output current (must be < $I_{LIM_min}$ = 2.5 A)
$\Delta I_L$ = Inductor peak-to-peak ripple current

The peak switch current $I_{SWPEAK}$ is the current that the switch and the inductor have to be able to handle.


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#### 7.4.3.4 Inductor Selection

| | | |
|---|---|---|
| **Inductor value:** | 4.7µH ≤ L ≤ 10µH | The higher the inductor value the lower the inductor current ripple and the output voltage ripple but the slower the transient response. |
| **Saturation current:** | $I_{SAT} \geq I_{SWPEAK}$ or $I_{SAT} \geq I_{LIM_max}$ | The inductor saturation current must be higher than the switch peak current for the max. peak output current or as a more conservative approach higher than the max. switch current limit. |
| **DC resistance:** | The lower the inductors resistance the lower the losses and the higher the efficiency. | |

| INDUCTANCE | SUPPLIER(1) | COMPONENT CODE | SIZE (L x W x H mm) | DCR typ. (mΩ) | $I_{SAT}$ (A) |
|---|---|---|---|---|---|
| 4.7 µH | Sumida | CDRH5D28R/HP | 6.2 x 6.2 x 3 | 35 | 3.7 |
| 6.8 µH | Sumida | CDRH5D28R/HP | 6.2 x 6.2 x 3 | 49 | 3.1 |
| 4.7 µH | Chilisin | SCPS0725T | 7.8 x 7.7 x 2.5 | 40 | 4 |
| 6.8 µH | Chilisin | SCPS0725T | 7.8 x 7.7 x 2.5 | 66 | 3.5 |
| 4.7 µH | Chilisin | LVS606028 | 6.2 x 6.2 x 2.2 | 38 | 3.7 |
| 6.8 µH | Chilisin | LVS606028 | 6.2 x 6.2 x 2.2 | 50 | 3.1 |
| 4.7 µH | Mag Layers | MSCDRI-7025AL | 8 x 8 x 2.5 | 45 | 3.5 |
| 6.8 µH | Mag Layers | MSCDRI-7025AL | 8 x 8 x 2.5 | 63 | 3.1 |

(1) See *Third-Party Products* disclaimer

#### 7.4.3.5 Output Capacitor Selection

For best output voltage filtering low ESR ceramic capacitors are recommended. Three 10 µF (or one 22 µF) ceramic capacitors work for most applications. To improve the load transient response more capacitance can be added.

To calculate the output voltage ripple the following equations can be used:

$$\Delta V_{C_RIPPLE} = \frac{V_{CORE}}{V_{IO} \times f_S} \times \frac{I_{OUT}}{C_{OUT}} + \Delta V_{C_ESR} \qquad \Delta V_{C_ESR} = I_{SWPEAK} \times R_{C_ESR} \tag{6}$$

| CAPACITOR | VOLTAGE RATING | TEMPERATURE CHARACTERISTICS | SUPPLIER(1) | COMPONENT CODE |
|---|---|---|---|---|
| 10 µF / 1206 | 6.3 V | X5R | Murata | GRM219R60J106KE19 |
| 10 µF / 1206 | 6.3 V | X7R | Taiyo Yuden | JMK212AB7106KG |

(1) See *Third-Party Products* disclaimer

### 7.4.4 Buck 3 Converter ($V_{(HAVDD)}$)

The synchronous current mode buck 3 converter operates with Pulse Frequency Modulation (PFM) with a fixed off-time and a typ. frequency of 1 MHz. The converter features integrated soft-start, bootstrap and compensation to minimize external component and pin count.

If not needed the buck 3 converter can be disabled by $I^2C$.

#### 7.4.4.1 Soft-Start

The buck 3 converter is enabled together with the boost converter. It starts switching and ramps up its output voltage $V_{(HAVDD)}$ to the programmed voltage value tracking the boost converters output voltage $V_{(AVDD)}$.

#### 7.4.4.2 Setting the Output Voltage $V_{(HAVDD)}$

The output voltage is programmable by $I^2C$ between 4.8 V and 11.1 V in 100 mV steps.

#### 7.4.4.3 High Voltage Stress Mode (HVS)

By pulling the HVS-pin “high” an $I^2C$ programmable offset voltage is added to the set boost and buck 3 converters output voltage $V_{(AVDD)}$ and $V_{(HAVDD)}$. The offset voltages are programmable independently.

#### 7.4.4.4 Design Procedure

The first step in the design procedure is to verify whether the maximum possible output current of the buck 3 converter supports the specific application requirements.

1. Switching frequency: $f_S = \frac{0.76 \times V_{HAVDD} \times V_{IN} - V_{HAVDD}}{V_{IN}} MHz$
2. Converter Duty Cycle: $D = \frac{V_{HAVDD}}{V_{IN} \times \eta}$
3. Inductor ripple current: $\Delta I_L = \frac{(V_{IN} - V_{HAVDD}) \times D}{f_S \times L}$
4. Maximum output current: $I_{OUT_max} = I_{LIM_min} - \frac{\Delta I_L}{2}$
5. Peak switch current: $I_{SWPEAK} = I_{OUT} + \frac{\Delta I_L}{2}$

$\eta$ = Estimated boost converter efficiency (use the number from the efficiency plots or 0.8 as an estimation)
$f_S$: Switching frequency (typ. 1 MHz)
L = Selected inductor value (typ. 6.8 µH)
$I_{LIM_min}$: Minimum current limit (1.7 A)
$I_{SWPEAK}$ = Peak switch current for the used output current (must be < $I_{LIM_min}$ = 1.7 A)
$\Delta I_L$ = Inductor peak-to-peak ripple current

The peak switch current $I_{SWPEAK}$ is the current that the switch and the inductor have to be able to handle.

#### 7.4.4.5 Inductor Selection

| | | |
|---|---|---|
| **Inductor value:** | 4.7 µH ≤ L ≤ 10 µH | The higher the inductor value the lower the inductor current ripple and the output voltage ripple but the slower the transient response. |
| **Saturation current:** | $I_{SAT} \geq I_{SWPEAK}$ or $I_{SAT} \geq I_{LIM_max}$ | The inductor saturation current must be higher than the switch peak current for the max. peak output current or as a more conservative approach higher than the max. switch current limit. |
| **DC resistance:** | The lower the inductors resistance the lower the losses and the higher the efficiency. | |

| INDUCTANCE | SUPPLIER(1) | COMPONENT CODE | SIZE (L x W x H mm) | DCR typ. (mΩ) | $I_{SAT}$ (A) |
|---|---|---|---|---|---|
| 4.7 µH | Chilisin | SCDS6D28T | 7 x 7 x 3 | 25 | 2.5 |
| 6.8 µH | Chilisin | SCDS6D28T | 7 x 7 x 3 | 40 | 2.1 |
| 4.7 µH | Chilisin | SCPS0725T | 7.8 x 7.7 x 2.5 | 40 | 4 |
| 6.8 µH | Chilisin | SCPS0725T | 7.8 x 7.7 x 2.5 | 66 | 3.5 |
| 4.7 µH | Chilisin | LVS404018 | 4.2 x 4.2 x 2 | 90 | 2 |
| 6.8 µH | Chilisin | LVS404018 | 4.2 x 4.2 x 2 | 110 | 1.6 |
| 4.7 µH | Mag Layers | MSCDRI-7025AL | 8 x 8 x 2.5 | 45 | 3.5 |
| 6.8 µH | Mag Layers | MSCDRI-7025AL | 8 x 8 x 2.5 | 63 | 3.1 |

(1) See *Third-Party Products* disclaimer

#### 7.4.4.6 Output Capacitor Selection

For best output voltage filtering low ESR ceramic capacitors are recommended. One 10 µF ceramic capacitor works for most applications. To improve the load transient response more capacitance can be added.

To calculate the output voltage ripple the following equations can be used:


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$$\Delta V_{C_RIPPLE} = \frac{V_{HAVDD}}{V_{IN} \times f_S} \times \frac{I_{OUT}}{C_{OUT}} + \Delta V_{C_ESR} \qquad \Delta V_{C_ESR} = I_{SW\,PEAK} \times R_{C_ESR} \tag{7}$$

| CAPACITOR | VOLTAGE RATING | TEMPERATURE CHARACTERISTICS | SUPPLIER(1) | COMPONENT CODE |
|---|---|---|---|---|
| 10 µF / 1206 | 16 V | X5R | Murata | GRM31CR61C106KA88 |
| 10 µF / 1206 | 16 V | X7R | Taiyo Yuden | EMK316AB7106KL |

(1) See *Third-Party Products* disclaimer

### 7.4.5 Positive Charge Pump Controller ($V_{(GH)}$) with Temperature Compensation

The positive charge pump is driven from the boost converter's switch node and regulated by controlling the current through an external PNP transistor. The controller is optimized for transistors with a DC gain ($h_{FE}$) between 100 and 300, a base drive current up to 5 mA is supported. A temperature compensation for its output voltage $V_{(GH)}$ is implemented and the levels of the output voltages are programmed by $I^2C$.

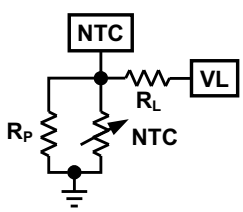
The positive charge pump and the temperature compensation function can be disabled by $I^2C$ separately.

#### *7.4.5.1 Soft-Start*

The positive charge pump controller is enabled when the boost converter is in regulation. The output voltage $V_{(GH)}$ ramps up to the programmed voltage in typ. 1.5 ms.

#### *7.4.5.2 Setting the Output Voltage $V_{(GH)}$*

The low voltage $V_{(GH_LOW)}$ at high temperature is programmed directly by $I^2C$ from 20 V to 35 V in 1 V steps, the high voltage $V_{(GH_HIGH)}$ at low temperature is programmed with a positive offset voltage of 1 V steps relative to $V_{(GH_LOW)}$. An external NTC thermistor with a resistor network ($R_P$ and $R_L$) sets the temperatures when $V_{(GH_LOW)}$ ($V_{NTC} \leq 1$ V, hot) and $V_{(GH_HIGH)}$ ($V_{NTC} \geq 2$ V, cold) are reached. To achieve a linear curve between $V_{(GH_LOW)}$ and $V_{(GH_HIGH)}$ a suitable linearalization resistor parallel to the NTC must be used.




$R_{T0}$ is the resistance at an absolute temperature $T_0$ in Kelvin (normally 25°C)
T is the temperature in Kelvin (°C + 273.15 K/°C)
B is a material constant provided by the NTC supplier

$$R_{NTC}(T) = R_{T_0} \times e^{-B \times \left(\frac{1}{T_0} - \frac{1}{T}\right)}$$

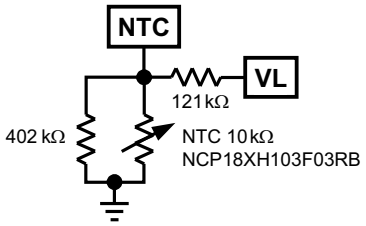
$V_L$: Internal supply voltage $V_L = 5$ V

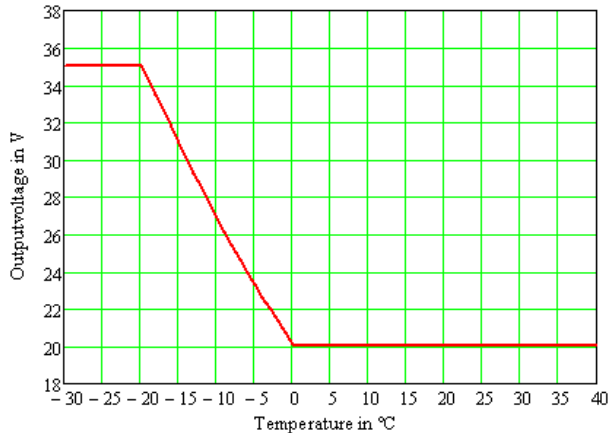
$R_{NTC}(T_{HOT})$: NTC resistance hot

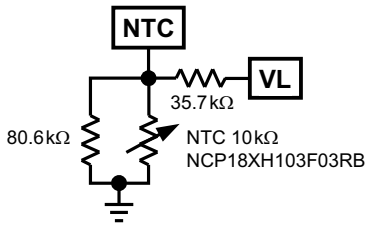
$R_{NTC}(T_{COLD})$: NTC resistance cold

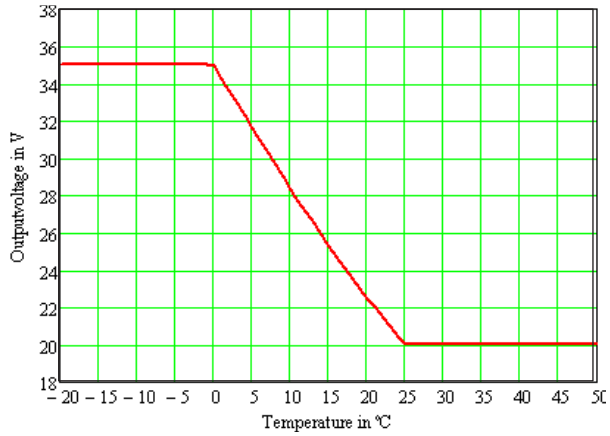
$$R_P = \frac{V_L \times R_{NTC}(T_{HOT}) \times R_{NTC}(T_{COLD})}{V_L \times R_{NTC}(T_{COLD}) - 2V_L \times R_{NTC}(T_{HOT}) + 2R_{NTC}(T_{HOT}) - 2R_{NTC}(T_{COLD})}$$

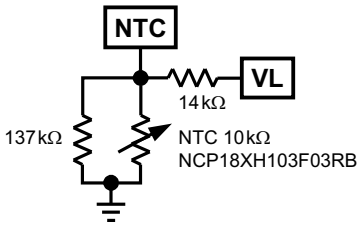
$$R_L = \frac{R_P \times R_{NTC}(T_{HOT}) \times (V_L - 1V)}{R_P + R_{NTC}(T_{HOT})}$$



### *7.4.5.3 Design Procedure*

1. Supported max. output voltage

   The maximum possible output voltage is calculated as follows:

Doubler Mode: $$V_{GH_max} = V_{INPUT} + V_{AVDD} - 2V_F - V_Q - R \times I_{GH} \times \left(\frac{1}{D} + \frac{1}{1-D}\right) - \frac{I_{GH}}{C \times f_S}$$

Tripler Mode: $$V_{GH_max} = V_{INPUT} + 2V_{AVDD} - 4V_F - V_Q - 2R \times I_{GH} \times \left(\frac{1}{D} + \frac{1}{1-D}\right) - \frac{2I_{GH}}{C \times f_S}$$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$V_F$: Diode forward voltage
R: Switch node resistor
$V_{INPUT}$: Transistor emitter voltage
D: Boost duty cycle
C: Flying capacitor value
$f_S$: Boost switching frequency (750kHz)
$V_Q$: Collector-emitter saturation voltage

2. Diode selection

Diode type: No specific type required

Forward voltage: The lower the forward voltage $V_F$ the higher the maximum output voltage

Reverse voltage: $V_R$ must be higher than the switching voltage applied at the flying capacitor

Forward current: The average forward current $I_{AVG}$ must be higher than the output current $I_{OUT}$

Thermal characteristics: The diode must be able to handle the dissipated power of $P_D = V_F \times I_{OUT}$

Peak currents of up to some amps through the diodes can occur during start-up for a few cycles. This condition lasts for <1ms and can be tolerated by many diodes whose repetitive peak current rating is much lower.

| $V_R$ / $I_{AVG}$ | $V_F$ typ. at 25°C | COMPONENT CODE | $R_{\theta JA}$ | SIZE | SUPPLIER(1) |
|---|---|---|---|---|---|
| 85 V / 150 mA | 1.1 V at 150 mA | BAV99TPT | | SOT-416 | Chenmko |
| 75 V / 300 mA | 1 V at 150 mA | BAV99W | 625 °C/W | SOT-323 | Diodes |
| 75 V / 215 mA | 1.1 V at 150 mA | BAV99BDWPT | 625 °C/W | SOT-363 | Chenmko |
| 75 V / 300 mA | 1 V at 150 mA | BAV99BRW | 625 ºC/W | SOT-363 | Diodes |
| 75 V / 300 mA | 1 V at 150 mA | BAV99T | 833 ºC/W | SOT-523 | Diodes |
| 30 V / 1 A | 0.47 V at 1 A | CH511H-30PT | 625 ºC/W | SOT-323 | Chenmko |
| 40 V / 200 mA | 0.9 V at 200 mA | BAS40W-04 | 625 ºC/W | SOT-323 | Diodes |
| 40 V / 200 mA | 0.9 V at 200 mA | BAS40-04T | 833 ºC/W | SOT-523 | Diodes |
| 30 V / 200 mA | 0.65 V at 200 mA | BAT54SW | 625 ºC/W | SOT-323 | Diodes |
| 30 V / 200 mA | 0.65 V at 200 mA | BAT54ST | 833 ºC/W | SOT-523 | Diodes |
| 75 V / 300 mA | 1 V at 200 mA | MMBD7000 | 357 ºC/W | SOT-23 | Diodes |

(1) See *Third-Party Products* disclaimer

3. Transistor selection

DC gain ($h_{FE}$): At least 35 when the transistors collector current is equal to the output current, for good performance 75 to 200 is recommended

Collector-Emitter voltage: $V_{CEO}$ must be at least the input voltage (Emitter voltage) + switching voltage $V_{AVDD}$

DC Collector current: Must be higher than the output current $I_{OUT}$ / (1 – boost duty cycle)

Thermal characteristics: The transistor must be able to handle the dissipated power of:

Doubler Mode:
$$P_{DIS} = \left(V_{INPUT} + V_{AVDD} - 2V_F - V_{GH}\right) \times I_{GH} - R \times I_{GH}^2 \times \left(\frac{1}{D^2} + \frac{1}{(1-D)^2}\right) - \frac{I_{GH}}{C \times f_S}$$

Tripler Mode:
$$P_{DIS} = \left(V_{INPUT} + 2V_{AVDD} - 4V_F - V_{GH}\right) \times I_{GH} - 2R \times I_{GH}^2 \times \left(\frac{1}{D^2} + \frac{1}{(1-D)^2}\right) - \frac{2I_{GH}}{C \times f_S}$$

$V_{INPUT}$: Input voltage
$V_F$: Diode forward voltage
$I_{GH}$: Mean output current
D: Boost duty cycle
R: Switch node resistor
C: Flying capacitor value

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$f_S$: Boost switching frequency (750kHz)

The total power dissipation of the chosen package is specified with a very good thermal designed PCB. The specified max. power dissipation can only be dissipated if the cooling area at the PCB is big enough. The total area should be at least 5 $cm^2$ it can be spread over different layers when using many vias.

| $V_{CEO}$ / $I_C$ | $h_{FE}$ min…max. | $V_{CEsat}$ | COMPONENT CODE | $P_{tot}$ | SIZE | SUPPLIER (1) |
|---|---|---|---|---|---|---|
| –60 V / –600 mA | 100…300 at –150 mA | –150 mV | CHT2907XPT | 1.2 W | SOT-89 | Chenmko |
| –40 V / –200 mA | 60…300 at –50 mA | –200 mV | CH3906XPT | 1.2 W | SOT-89 | Chenmko |
| –50 V /–2 A | 70…240 at –500 mA | –150 mV | KTA1666 | 1 W | SOT-89 | KEC |
| –60 V / –1 A | 50…200 at –500 mA | –300 mV | KTA1668 | 1 W | SOT-89 | KEC |
| –60 V / –600 mA | 100…300 at –150 mA | –150 mV | PZT2907AT1 | 1.5 W | SOT-223 | ON Semi |

(1) See *Third-Party Products* disclaimer

4. Base-Emitter resistor selection

   A 100-kΩ base-emitter resistor is required to ensure proper operation. It is needed to ensure that the transistor can be turned off completely. Too low resistor value reduce the maximum base drive current.

5. Flying capacitor selection

   A flying capacitor of 470 nF is appropriate for most applications. Larger capacitances have a smaller voltage drop ΔV at the end of each switching cycle and support therefore higher output voltages and currents. The voltage rating must be at least the switching voltage $V_{(AVDD)}$.

   C: Flying capacitor value

   $f_S$: Boost switching frequency (750kHz)

$$\Delta V = \frac{I_{GH}}{C \times f_S}$$

| CAPACITOR | VOLTAGE RATING | TEMPERATURE CHARACTERISTICS | SUPPLIER (1) | COMPONENT CODE |
|---|---|---|---|---|
| 470 nF / 0603 | 25 V | X7R | Murata | GRM188R71E474KA12 |
| 470 nF / 0603 | 25 V | X5R | Taiyo Yuden | TMK107BJ474KA |

(1) See *Third-Party Products* disclaimer

6. Switch node resistor selection

   For less boost converter disturbance and therefore lower boost output voltage ripple $\Delta V_{(AVDD)}$ and lower diode current spikes a resistor should be added in the switching path. The higher the resistance the lower the disturbances and the peak currents but also the lower the maximum output current and the higher the resistors power dissipation $P_R$. A 1 Ω to 2.2 Ω resistor is appropriate for most applications.

   $I_{GH}$: $V_{GH}$ mean output current
   D: Boost converter duty cycle
   R: Switch node resistor

$$P_R = R \times I_{GH}^2 \times \left(\frac{1}{D} + \frac{1}{1-D}\right)$$

#### *7.4.5.4 Output Capacitor Selection*

For best output voltage filtering low ESR ceramic capacitors are recommended. One 4.7 µF ceramic capacitor works for most applications. To improve the load transient response more capacitance can be added.

| CAPACITOR | VOLTAGE RATING | TEMPERATURE CHARACTERISTICS | SUPPLIER (1) | COMPONENT CODE |
|---|---|---|---|---|
| 4.7 µF / 1206 | 50 V | X7R | Murata | GRM31CR71H475KA12 |
| 4.7 µF / 1206 | 50 V | X5R | Taiyo Yuden | UMK316BJ475KL |

(1) See *Third-Party Products* disclaimer

### 7.4.6 Negative Charge Pump Controller ($V_{(GL)}$)

The negative charge pump usually is driven from the buck 1 converter's switch node but can also be connected to the boost converter's switch node and regulated by controlling the current through an external NPN transistor. The controller is optimized for transistors with a DC gain ($h_{FE}$) between 100 and 300, a base drive current up to 5 mA is supported.


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The negative charge pump can be disabled by $I^2C$.

**TPS65177A:**

When $V_{(GL)}$ is driven by the boost switch pin (SW) the EN-pin should be connected to $V_I$, otherwise $V_{(GL)}$ detects a short when EN is pulled low as the $V_{(GL)}$ voltage collapses. $V_{(GL)}$ collapses because the supporting switch node (SW) stops switching and the device partially shuts down as described in the *Short-Circuit and Overload Protection* section. The device is in a latched state and only a power cycle can restart the $V_{(AVDD)}$, $V_{(HAVDD)}$, $V_{(GH)}$ and $V_{(GL)}$ rail.

#### 7.4.6.1 Soft-Start

The negative charge pump controller is enabled when the buck 2 converter is in regulation. The output voltage $V_{(GL)}$ ramps up to the programmed voltage in typ. 1.5 ms.

#### 7.4.6.2 Setting the Output Voltage $V_{(GL)}$

The output voltage is programmable by $I^2C$ between –14.5 V and –5.5 V in 600 mV steps.

#### 7.4.6.3 Design Procedure

1. Supported max. output voltage

   The maximum possible negative output voltage is calculated as follows:

   *Using buck 1 converter's switch node:*

   Inverter: $$V_{GL_max} = V_{INPUT} - V_{IN} + 2V_F + V_Q + R \times I_{GL} \times \left(\frac{1}{D} + \frac{1}{1-D}\right) + \frac{I_{GL}}{C \times f_S}$$

   $V_{INPUT}$: Transistor emitter node voltage
   $V_F$: Diode forward voltage
   R: Switch node resistor
   D: Buck duty cycle
   C: Flying capacitor value
   $f_S$: Boost and Buck1 switching frequency (750kHz)
   $V_Q$: Collector-emitter saturation voltage

   *Using boost converter's switch node:*

   Inverter: $$V_{GL_max} = V_{INPUT} - V_{AVDD} + 2V_F + V_Q + \frac{R \times I_{GL}^2}{D \times (1-D)} + \frac{I_{GL}}{C \times f_S}$$

2. Diode selection

   Diode type: No specific type required

   Forward voltage: The lower the forward voltage $V_F$ the higher the maximum output voltage

   Reverse voltage: $V_R$ must be higher than the switching voltage applied at the flying capacitor $V_{IN}$ or $V_{AVDD}$

   Forward current: The average forward current $I_{AVG}$ must be higher than the output current $I_{OUT}$

   Thermal characteristics: The diode must be able to handle the dissipated power of $P_D = V_F \times I_{OUT}$

   Peak currents of up to some amps through the diodes can occur during start-up for a few cycles. This condition lasts for < 1 ms and can be tolerated by many diodes whose repetitive peak current rating is much lower.

| $V_R$ / $I_{AVG}$ | $V_F$ typ. at 25°C | COMPONENT CODE | $R_{\theta JA}$ | SIZE | SUPPLIER (1) |
|---|---|---|---|---|---|
| 85 V / 150 mA | 1.1 V at 150 mA | BAV99TPT | | SOT-416 | Chenmko |
| 75 V / 300 mA | 1 V at 150 mA | BAV99W | 625 °C/W | SOT-323 | Diodes |
| 75 V / 215 mA | 1.1 V at 150 mA | BAV99BDWPT | 625 °C/W | SOT-363 | Chenmko |
| 75 V / 300 mA | 1 V at 150 mA | BAV99BRW | 625 ºC/W | SOT-363 | Diodes |
| 75 V / 300 mA | 1 V at 150 mA | BAV99T | 833 ºC/W | SOT-523 | Diodes |

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| $V_R$ / $I_{AVG}$ | $V_F$ typ. at 25°C | COMPONENT CODE | $R_{\theta JA}$ | SIZE | SUPPLIER(1) |
|---|---|---|---|---|---|
| 30 V / 1 A | 0.47 V at 1 A | CH511H-30PT | 625 ºC/W | SOT-323 | Chenmko |
| 40 V / 200 mA | 0.9 V at 200 mA | BAS40W-04 | 625 ºC/W | SOT-323 | Diodes |
| 40 V / 200 mA | 0.9 V at 200 mA | BAS40-04T | 833 ºC/W | SOT-523 | Diodes |
| 30 V / 200 mA | 0.65 V at 200 mA | BAT54SW | 625 ºC/W | SOT-323 | Diodes |
| 30 V / 200 mA | 0.65 V at 200 mA | BAT54ST | 833 ºC/W | SOT-523 | Diodes |
| 75 V / 300 mA | 1 V at 200 mA | MMBD7000 | 357 ºC/W | SOT-23 | Diodes |

3. Transistor selection

DC gain ($h_{FE}$): At least 35 when the transistors collector current is equal to the output current, for good performance 75 to 200 is recommended

Collector-Emitter voltage: $V_{CEO}$ must be at least the input voltage (Emitter voltage) + switching voltage $V_I$ or $V_{(AVDD)}$

DC Collector current: Must be higher than the output current $I_{OUT}$ / (1 – buck duty cycle) or $I_{OUT}$ / boost duty cycle

Thermal characteristics: The transistor must be able to handle the dissipated power of:

*Using buck 1 converter's switch node:*

Inverter: $$P_{DIS} = \left(V_{IN} - V_{INPUT} - 2V_F - \left|V_{GL}\right|\right) \times I_{GL} - R \times I_{GL}^2 \times \left(\frac{1}{D^2} + \frac{1}{(1-D)^2}\right) - \frac{I_{GL}}{C \times f_S}$$

$V_F$: Diode forward voltage
$V_{INPUT}$: Input voltage
$I_{GL}$: Mean output current
R: Switch node resistor
D: Buck duty cycle
C: Flying capacitor value
$f_S$: Boost and Buck 1 switching frequency (750kHz)

*Using boost converter's switch node:*

Inverter: $$P_{DIS} = \left(V_{AVDD} - V_{INPUT} - 2V_F - \left|V_{GL}\right|\right) \times I_{GL} - R \times I_{GL}^2 \times \left(\frac{1}{D^2} + \frac{1}{(1-D)^2}\right) - \frac{I_{GL}}{C \times f_S}$$

The total power dissipation of the chosen package is specified with a very good thermal designed PCB. The specified max. power dissipation can only be dissipated if the cooling area at the PCB is big enough. The total area should be at least 5 $cm^2$ it can be spread over different layers when using many vias.

| $V_{CEO}$ / $I_C$ | $h_{FE}$ min…max. | $V_{CEsat}$ | COMPONENT CODE | $P_{tot}$ | SIZE | SUPPLIER(1) |
|---|---|---|---|---|---|---|
| 40 V / 600 mA | 100…300 at 150 mA | 150 mV | CHT2222XPT | 1.2 W | SOT-89 | Chenmko |
| 40 V / 200 mA | 60…300 at 50 mA | 100 mV | CH3904XPT | 1.2 W | SOT-89 | Chenmko |
| 80 V / 400 mA | 50…240 at 200 mA | 100 mV | KTC4374 | 1 W | SOT-89 | KEC |
| 30 V / 1.5 A | 100…320at 500 mA | 150 mV | KTC4375 | 1 W | SOT-89 | KEC |
| 30 V / 800 mA | 50…320 at 500 mA | 150 mV | KTC4376 | 1 W | SOT-89 | KEC |
| 40 V / 600 mA | 40…300 at 500 mA | 500 mV | PZT2222AT1 | 1.5 W | SOT-223 | ON Semi |
| 40 V / 200 mA | 60…300 at 50 mA | 200 mV | PZT3904T1G | 1.5 W | SOT-223 | ON Semi |

(1) See *Third-Party Products* disclaimer

4. Base-Emitter resistor selection

A 100 kΩ base-emitter (DRVN-pin to GND) resistor is integrated to ensure proper operation there is no external resistor needed. It is needed to ensure that the transistor can be turned off completely.

5. Flying capacitor selection

A flying capacitor of 470 nF is appropriate for most applications. Larger capacitances have a smaller voltage drop ΔV at the end of each switching cycle and support therefore higher output voltages and currents. The voltage rating must be at least the switching voltage $V_I$ (using buck 1 switch) or $V_{(AVDD)}$ (using boost switch).


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C: Flying capacitor value
$f_S$: Buck 1 or Boost switching frequency (750 kHz) $\Delta V = \frac{I_{GL}}{C \times f_S}$

| CAPACITOR | VOLTAGE RATING | TEMPERATURE CHARACTERISTICS | SUPPLIER (1) | COMPONENT CODE |
|---|---|---|---|---|
| 470 nF / 0603 | 25 V | X7R | Murata | GRM188R71E474KA12 |
| 470 nF / 0603 | 25 V | X5R | Taiyo Yuden | TMK107BJ474KA |

(1) See *Third-Party Products* disclaimer

6. Switch node resistor selection

For less buck 1 or boost converter disturbance and therefore lower buck 1 or boost output voltage ripple $\Delta V_{(IO)}$ or $\Delta V_{(AVDD)}$ and lower diode current spikes a resistor should be added in the switching path. The higher the resistance the lower the disturbances and the peak currents but also the lower the maximum output current and the higher the resistors power dissipation. A 1 Ω to 2.2 Ω resistor is appropriate for most applications

$I_{GL}$: $V_{GL}$ mean output current
D: Boost converter duty cycle
R: Switch node resistor

$$P_R = R \times I_{GL}^2 \times \left(\frac{1}{D} + \frac{1}{1-D}\right)$$

#### *7.4.6.4 Output Capacitor Selection*

For best output voltage filtering low ESR ceramic capacitors are recommended. One 4.7µF ceramic capacitor works for most applications. To improve the load transient response more capacitance can be added.

| CAPACITOR | VOLTAGE RATING | TEMPERATURE CHARACTERISTICS | SUPPLIER (1) | COMPONENT CODE |
|---|---|---|---|---|
| 4.7 µF / 1206 | 16 V | X5R | Murata | GRM21BR61C475KA88 |
| 4.7 µF / 1206 | 16 V | X7R | Taiyo Yuden | EMK212B7475KG |

(1) See *Third-Party Products* disclaimer

### 7.5 Gate Pulse Modulation ($V_{(GHM)}$)

The Gate Pulse Modulation is controlled by the CTRL-pin, except during start-up and shut-down. During start-up $V_{(GHM)}$ is kept at low state ($V_{(GHM)} = V_{(RE)}$) until Power Good of the positive charge pump $V_{(GH)}$ is reached, at shut-down $V_{(GHM)}$ follows $V_{(GH)}$ ($V_{(GHM)} = V_{(GH)}$).

If not needed the Gate Pulse Modulation can be disabled by $I^2C$.

CTRL = 'high' → $V_{(GHM)} = V_{(GH)}$

CTRL = 'low' → $V_{(GHM)} = V_{(RE)}$ (discharges through RE resistor)

The slope at which $V_{(GHM)}$ discharges is set by the external resistor connected to the RE-pin, the internal MOSFET $R_{DS(ON)}$ (typ. 3 Ω) and the gate line capacitance connected to the VGHM-pin. The RE resistor must be connected to GND and it must also be able to handle the power dissipation.

A Gate Pulse Modulation limit voltage can be set by $I^2C$ programming. When the limit voltage is reached the discharging of VGHM through RE is stopped and the VGHM output is high impedance until CTRL goes "high" again, see Figure 13.

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## Gate Pulse Modulation ($V_{(GHM)}$) (continued)

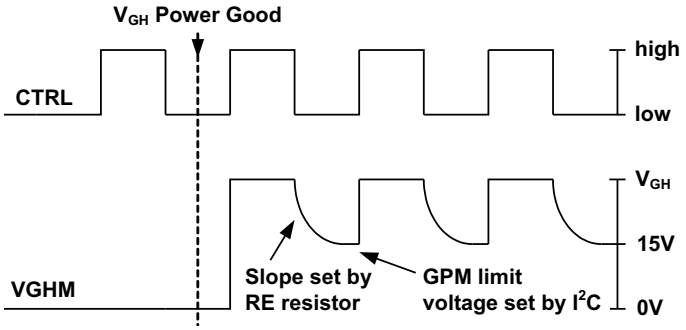


**Figure 13. Gate Pulse Modulation**


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## 7.6 Programming

### 7.6.1 I²C Serial Interface Description

The TPS65177/A communicates through an industry standard 2-wire I²C interface to receive data in slave mode. The I²C serial interface was developed by Philips Semiconductor (see I²C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is among other things responsible for generating the SCL signal and the slave device address to communicate with a certain device. A slave device receives and/or transmits data on the bus under control of the master device. A START condition send by the master initiates a new data transfer to the slave devices. Transitioning SDA from high to low while SCL remains high generates a START condition. A STOP condition ends a data transfer to the selected slave device. Transitioning SDA from low to high while SCL remains high generates a STOP condition (see Figure 14).

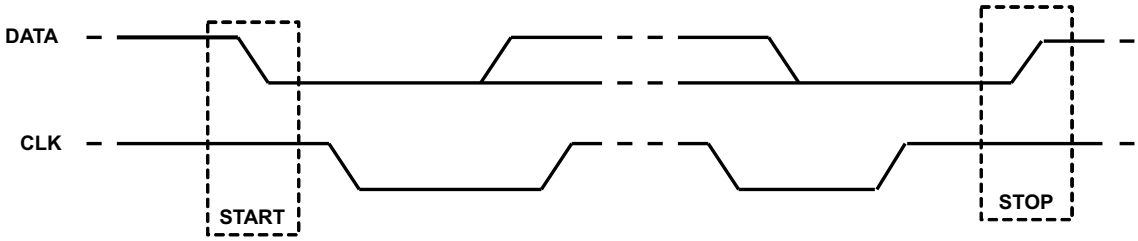


**Figure 14. START and STOP Conditions**

The TPS65177/A works as a slave and supports the standard mode (100 kbps) and fast mode (400 kbps) data transfer mode, as defined in the I²C-Bus specification. The data transfer protocol for standard and fast mode is exactly the same. The TPS65177/A supports 7-bit addressing. The device 7-bit address is defined as '010000X' (see Figure 15) where the bit X can be selected depending on the address pin configuration of A0 ("high" = 1, "low" = 0). The LSB enables the write or read function ("high" = read, "low" = write).

| (MSB) | TPS65177 Address | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 | A0 | R/$\overline{W}$ |

**Figure 15. TPS65177/A Slave Address Byte**

The master generates the SCL pulses, transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that the data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 16). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an Acknowledge, ACK, (see Figure 17) by pulling the SDA line low during the entire high period of the SCL cycle. Upon detecting this Acknowledge, the master knows that communication link with a slave has been established.

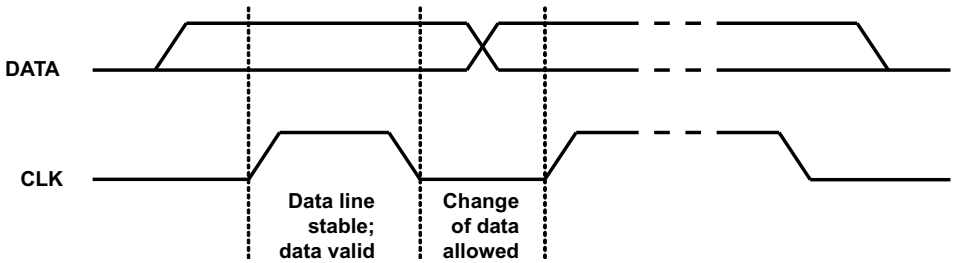


**Figure 16. Bit Transfer on the Serial Interface**

## Programming (continued)

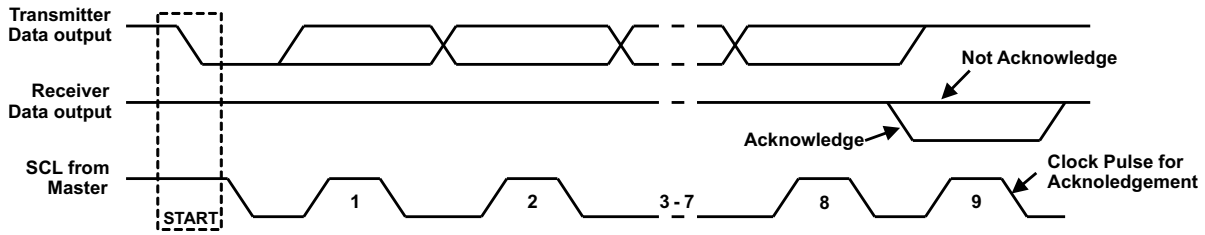


**Figure 17. Acknowledge on the I²C Bus**

The master generates further SCL cycles to either transmit data to the slave (R/W bit = 0) or receive data from the slave (R/W bit = 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To terminate the data transfer, the master generates the STOP condition by pulling the SDA line from low to high while the SCL line is high (see Figure 18). This releases the bus and stops the communication link with the addressed slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released and they wait for a START condition followed by a matching slave address.

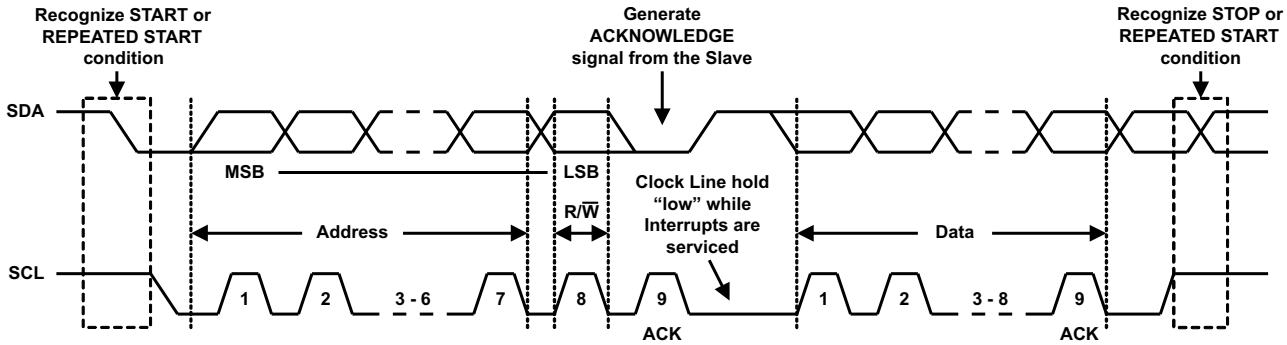


**Figure 18. I²C Bus Protocol**

Attempting to read data from register addresses not listed in the following section will result in 00h being read out.

### 7.6.2 Memory Description

A non-volatile EEPROM containing the initial values of the DACs and a volatile memory containing the DACs settings is implemented in the TPS65177/A. The non-volatile memory is called the Initial Value Register (IVR) and the volatile memory is called DAC Register (DR). The non-volatile IVR and the volatile DR are accessed by the same address. A Control Register (CR) is implemented to select if the IVR or the DR is addressed.

### 7.6.3 Read / Write Description

To read the volatile memory (DR) data the LSB (EE/$\overline{DR}$) of the Control Register (CR) must be set to 0, to read the non-volatile EEPROM (IVR) data the LSB of the Control Register (CR) must be set to 1, then the data of the selected memory can be read.

To write data into the non-volatile EEPROM (IVR) all data registers (00h ~ 0Ch) must be programmed first and then the MSB (WED) of the Control Register (CR) must be set to 1. A dead time of 50ms is initiated during which all the register data (00h ~ 0Ch) is stored into the non-volatile EEPROM. It is not possible to write single DAC register data to the EEPROM. There should be not data flow at the I²C bus during that time because the I²C interface of the TPS65177/A is momentarily not responding. When the 50ms have passed the WED bit is automatically reset to 0.


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## Programming (continued)

### 7.6.4 Write Operation

#### *7.6.4.1 Write Single Byte to the DAC Register (DR):*

1. Master sends START condition on the bus
2. Master sends the TPS65177/A address 010000$A_0$ and R/$\overline{W}$ bit = Low
   TPS65177/A will Acknowledge this byte
3. Send DAC register address (e.g. 01h, address of $V_{AVDD}$)
   TPS65177/A will Acknowledge this byte
4. Send the data byte to be written to the DAC register
   TPS65177/A will Acknowledge this byte
5. Master sends STOP condition on the bus

Example: Writing 0Fh (15 V) to the DAC address 01h (Boost converter $V_{(AVDD)}$)

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| START | 0 | 1 | 0 | 0 | 0 | 0 | $A_0$ | 0 | SLAVE ACK | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | SLAVE ACK | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | SLAVE ACK | STOP |

#### *7.6.4.2 Write Multiple Bytes to the DAC Register (DR):*

1. Master sends START condition on the bus
2. Master sends the TPS65177/A address 010000$A_0$ and R/$\overline{W}$ bit = Low
   TPS65177/A will Acknowledge this byte
3. Send DAC register address (e.g. 01h, address of $V_{AVDD}$)
   TPS65177/A will Acknowledge this byte
4. Send the data byte to be written to the DAC register
   TPS65177/A will Acknowledge this byte
5. Master continues sending data bytes to be written to the DA registers
   (DAC register address pointer will automatically increase)
6. Master sends STOP condition on the bus

Example: Writing 0Fh, 05h, 00h to the DAC addresses 01h, 02h, 03h ($V_{(AVDD)}$, HVS, Current limit)

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| START | 0 | 1 | 0 | 0 | 0 | 0 | $A_0$ | 0 | SLAVE ACK | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | SLAVE ACK | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | SLAVE ACK | |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SLAVE ACK | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STOP | | | | | | | | | | |

#### *7.6.4.3 Write All DAC Register (DR) Data to EEPROM (EE):*

1. Master sends START condition on the bus
2. Master sends the TPS65177/A address 010000$A_0$ and R/$\overline{W}$ bit = Low
   TPS65177/A will Acknowledge this byte
3. Send Control register (CR) address of FFh
   TPS65177/A will Acknowledge this byte
4. Send 1xxxxxxx to enable data copy from DAC registers (DR) to EEPROM (EE)
   TPS65177/A will Acknowledge this byte
5. Master sends STOP condition on the bus

Example: Writing all DAC registers data to the EEPROM

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| START | 0 | 1 | 0 | 0 | 0 | 0 | $A_0$ | 0 | SLAVE ACK | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | SLAVE ACK | 1 | x | x | x | x | x | x | x | SLAVE ACK | STOP |

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### 7.6.5 READ OPERATION

#### *7.6.5.1 Read single data from DAC register (DR):*

1. Master sends START condition on the bus
2. Master sends the TPS65177/A address 010000$A_0$ and R/$\overline{W}$ bit = Low
   TPS65177/A will Acknowledge this byte
3. Send Control register (CR) address of FFh
   TPS65177/A will Acknowledge this byte
4. Send data byte of 00h (EE/ $\overline{DR}$ bit) to specify that the data is read from the DAC register
   TPS65177/A will Acknowledge this byte
5. Master sends STOP condition on the bus
6. Master sends START condition on the bus
7. Master sends the TPS65177/A address 010000$A_0$ and R/$\overline{W}$ bit = Low
   TPS65177/A will Acknowledge this byte
8. Send desired DAC register address to be read (00h~0Ch or FEh)
   TPS65177/A will Acknowledge this byte
9. Master re-sends START condition on the bus
10. Master sends the TPS65177/A address 010000$A_0$ and R/$\overline{W}$ bit = High
    TPS65177/A will Acknowledge this byte
11. Read data from DAC register
    Master will not-Acknowledge this byte
12. Master sends STOP condition on the bus

Example: Reading data from the DAC register (DR) address 01h ($V_{(AVDD)}$)

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| START | 0 | 1 | 0 | 0 | 0 | 0 | $A_0$ | 0 | SLAVE ACK | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | SLAVE ACK | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SLAVE ACK | STOP |
| START | 0 | 1 | 0 | 0 | 0 | 0 | $A_0$ | 0 | SLAVE ACK | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | SLAVE ACK | | | | | | | | | | |
| START | 0 | 1 | 0 | 0 | 0 | 0 | $A_0$ | 1 | SLAVE ACK | D | D | D | D | D | D | D | D | MASTER N-ACK | STOP | | | | | | | | | |


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#### *7.6.5.2 Read Multiple Data from DAC Register (DR):*

1. Master sends START condition on the bus
2. Master sends the TPS65177/A address 010000$A_0$ and R/$\overline{W}$ bit = Low
   TPS65177/A will Acknowledge this byte
3. Send Control register (CR) address of FFh
   TPS65177/A will Acknowledge this byte
4. Send data byte of 00h (EE/ $\overline{DR}$ bit) to specify that the data is read from the DAC register
   TPS65177/A will Acknowledge this byte
5. Master sends STOP condition on the bus
6. Master sends START condition on the bus
7. Master sends the TPS65177/A address 010000$A_0$ and R/$\overline{W}$ bit = Low
   TPS65177/A will Acknowledge this byte
8. Send desired DAC register address to be read (00h~0Ch or FEh)
   TPS65177/A will Acknowledge this byte
9. Master re-sends START condition on the bus
10. Master sends the TPS65177/A address 010000$A_0$ and R/$\overline{W}$ bit = High
    TPS65177/A will Acknowledge this byte
11. Continue read data from the DAC register, the address pointer will increase automatically
    Master will not-Acknowledge this byte
12. Master will not-acknowledge (N-ACK) after received the last reading data
13. Master sends STOP condition on the bus

Writing 0Fh, 05h, 00h to the DAC addresses 01h, 02h, 03h ($V_{(AVDD)}$, HVS, Current limit)

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| START | 0 | 1 | 0 | 0 | 0 | 0 | $A_0$ | 0 | SLAVE ACK | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | SLAVE ACK | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SLAVE ACK | STOP |
| START | 0 | 1 | 0 | 0 | 0 | 0 | $A_0$ | 0 | SLAVE ACK | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | SLAVE ACK | | | | | | | | | | |
| START | 0 | 1 | 0 | 0 | 0 | 0 | $A_0$ | 1 | SLAVE ACK | D | D | D | D | D | D | D | D | MASTER ACK | D | D | D | D | D | D | D | D | MASTER ACK | |
| | D | D | D | D | D | D | D | D | MASTER N-ACK | STOP | | | | | | | | | | | | | | | | | | |

#### *7.6.5.3 Read Single Data to EEPROM (EE):*

1. Master sends START condition on the bus
2. Master sends the TPS65177/A address 010000$A_0$ and R/$\overline{W}$ bit = Low
   TPS65177/A will Acknowledge this byte
3. Send Control register (CR) address of FFh
   TPS65177/A will Acknowledge this byte
4. Send data byte of 00h (EE/ $\overline{DR}$ bit) to specify that the data is read from the EEPROM
   TPS65177/A will Acknowledge this byte
5. Master sends STOP condition on the bus
6. Master sends START condition on the bus
7. Master sends the TPS65177/A address 010000$A_0$ and R/$\overline{W}$ bit = Low
   TPS65177/A will Acknowledge this byte
8. Send desired EEPROM register address to be read (00h~0Ch or FEh)
   TPS65177/A will Acknowledge this byte
9. Master re-sends START condition on the bus
10. Master sends the TPS65177/A address 010000$A_0$ and R/$\overline{W}$ bit = High
    TPS65177/A will Acknowledge this byte
11. Read data from EEPROM
    Master will not-Acknowledge this byte
12. Master sends STOP condition on the bus

Example: Reading data from the EEPROM (EE) addresses 01h, 02h, 03h ($V_{(AVDD)}$, HVS, Current limit)

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| START | 0 | 1 | 0 | 0 | 0 | 0 | $A_0$ | 0 | SLAVE ACK | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | SLAVE ACK | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | SLAVE ACK | STOP |
| START | 0 | 1 | 0 | 0 | 0 | 0 | $A_0$ | 0 | SLAVE ACK | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | SLAVE ACK | | | | | | | | | | |
| START | 0 | 1 | 0 | 0 | 0 | 0 | $A_0$ | 0 | SLAVE ACK | D | D | D | D | D | D | D | D | MASTER N-ACK | STOP | | | | | | | | | |


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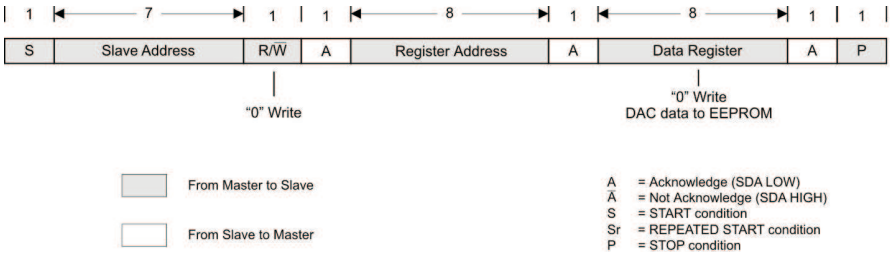
#### *7.6.5.4 Read Multiple Data to EEPROM (EE):*

1. Master sends START condition on the bus
2. Master sends the TPS65177/A address 010000$A_0$ and R/$\overline{W}$ bit = Low
   TPS65177/A will Acknowledge this byte
3. Send Control register (CR) address of FFh
   TPS65177/A will Acknowledge this byte
4. Send data byte of 00h (EE/ $\overline{DR}$ bit) to specify that the data is read from the EEPROM
   TPS65177/A will Acknowledge this byte
5. Master sends STOP condition on the bus
6. Master sends START condition on the bus
7. Master sends the TPS65177/A address 010000$A_0$ and R/$\overline{W}$ bit = Low
   TPS65177/A will Acknowledge this byte
8. Send desired EEPROM register address to be read (00h~0Ch or FEh)
   TPS65177/A will Acknowledge this byte
9. Master re-sends START condition on the bus
10. Master sends the TPS65177/A address 010000$A_0$ and R/$\overline{W}$ bit = High
    TPS65177/A will Acknowledge this byte
11. Continue read data from the EEPROM, the address pointer will increase automatically
    Master will not-Acknowledge this byte
12. Master will not-acknowledge (N-ACK) after received the last reading data
13. Master sends STOP condition on the bus

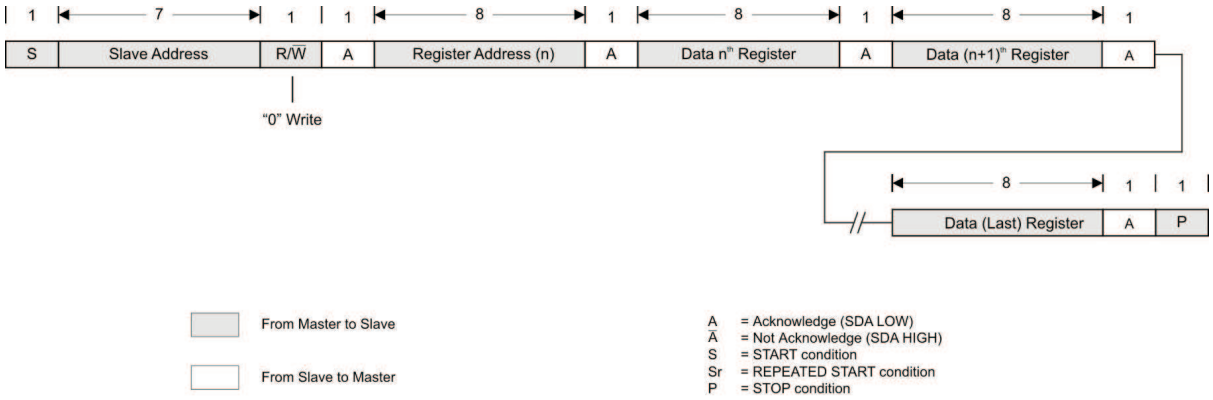
Example: Reading data from the EEPROM (EE) addresses 01h, 02h, 03h ($V_{(AVDD)}$, HVS, Current limit)

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| START | 0 | 1 | 0 | 0 | 0 | 0 | $A_0$ | 0 | SLAVE ACK | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | SLAVE ACK | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | SLAVE ACK | STOP |
| START | 0 | 1 | 0 | 0 | 0 | 0 | $A_0$ | 0 | SLAVE ACK | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | SLAVE ACK | | | | | | | | | | |
| START | 0 | 1 | 0 | 0 | 0 | 0 | $A_0$ | 1 | SLAVE ACK | D | D | D | D | D | D | D | D | MASTER N-ACK | D | D | D | D | D | D | D | D | MASTER ACK | |
| | D | D | D | D | D | D | D | D | MASTER N-ACK | STOP | | | | | | | | | | | | | | | | | | |

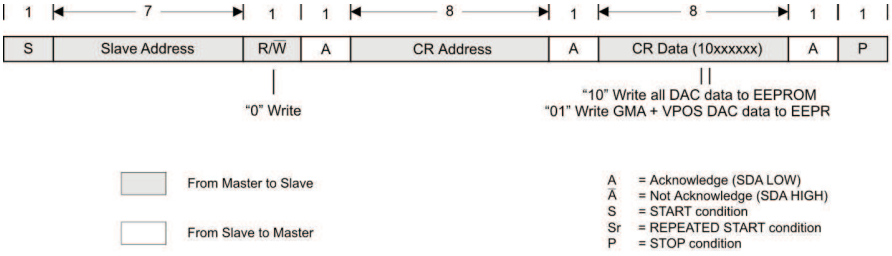
### 7.6.6 Write Single Data to DAC:



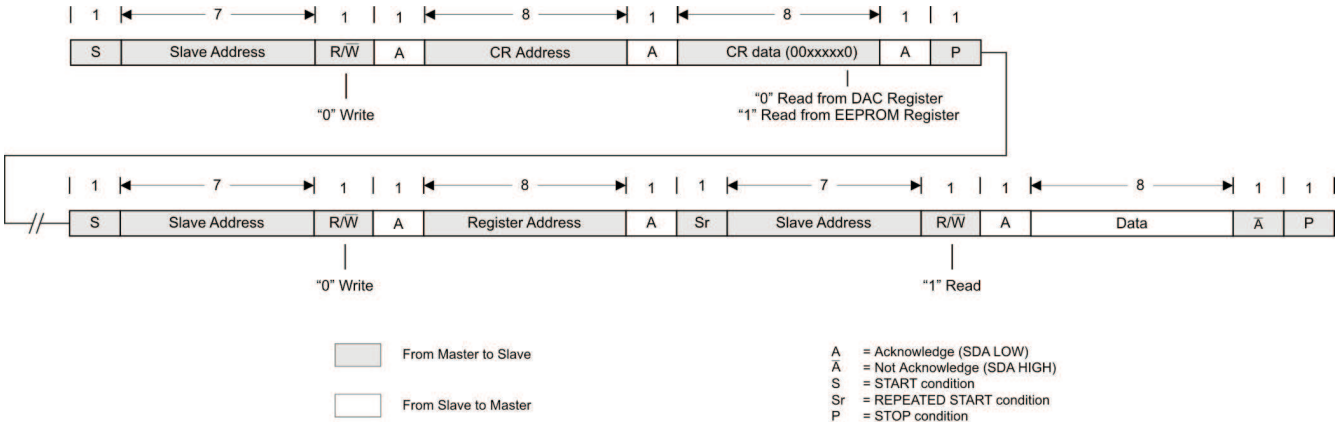

### 7.6.7 Write Multiple Data to DAC (Auto Increment Address):




### 7.6.8 Write all DAC Data to EEPROM:




### 7.6.9 Read Single Data From DAC / EEPROM:





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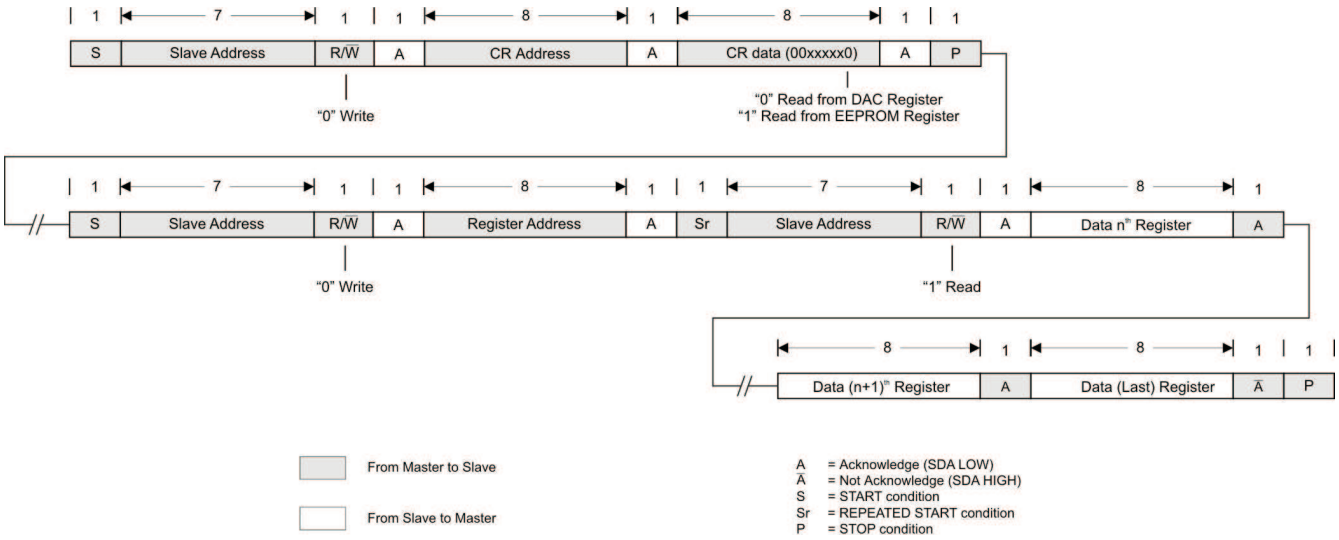
### 7.6.10 Read Multiple Data fFom DAC / EEPROM (Auto Increment Address):



## 7.7 Register Map

### 7.7.1 Registers and DAC Settings

**Table 3. Device address with A0 selection pin (A0 = 0 or 1)**

| MSB | TPS65177/A Address | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 | A0 | R/$\overline{W}$ |

**Table 4. Control Register FFh (Factory value 00h)**

| MSB | Address FFh | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| WED (Write EEPROM Data) | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | EE/ $\overline{DR}$ (Read EEPROM or DR) |

**Table 5. Register Map**

| Register | Name | Address | Factory value | Bit count | Steps count |
|---|---|---|---|---|---|
| Cannel | Channel Disable | 00h | 00h | 6 | 64 |
| Boost | Output voltage $V_{(AVDD)}$ | 01h | 0Fh | 6 | 64 |
| | HVS offset | 02h | 05h | 4 | 16 |
| | Current Limit | 03h | 00h | 3 | 8 |
| | Soft-start time | 04h | 00h | 1 | 2 |
| Buck 1 | Output voltage $V_{(IO)}$ | 05h | 03h | 4 | 16 |
| Buck 2 | Output voltage $V_{(CORE)}$ | 06h | 02h | 5 | 32 |
| Buck 3 | Output voltage $V_{(HAVDD)}$ | 07h | 1Bh | 6 | 64 |
| Pos. CP | Output voltage $V_{(GH_L)}$ | 08h | 08h | 4 | 16 |
| | $V_{(GH_L)}$ to $V_{(GH_H)}$ offset voltage $V_{(GH_OFS)}$ | 09h | 04h | 4 | 16 |
| GPM | GPM limit voltage | 0Ah | 00h | 2 | 4 |
| Neg. CP | Output voltage $V_{(GL)}$ | 0Bh | 04h | 4 | 16 |
| Buck 3 | HVS offset | 0Ch | 00h | 4 | 16 |
| Memory | Memory write remain time | FEh | Fh | 4 | 16 |
| Control | Control register | FFh | 00h | 8 | 256 |

#### *7.7.1.1 Channel Register (with factory value) – 00h (00h)*

| MSB | Address 00h | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | 0 | 0 | 0 | 0 | 0 | 0 |

| MSB | Address 00h | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | $V_{(CORE)}$ | $V_{(HAVDD)}$ | $V_{(GH)}$ | $V_{(GL)}$ | GPM | NTC |
| | | Enable: 0 | Enable: 0 | Enable: 0 | Enable: 0 | Enable: 0 | Enable: 0 |
| | | Disable:1 | Disable:1 | Disable:1 | Disable:1 | Disable:1 | Disable:1 |

#### *7.7.1.2 Boost Output Voltage $V_{(AVDD)}$ Register (with factory value) – 01h (0Fh)*

| MSB | Address 01h | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | 0 | 0 | 1 | 1 | 1 | 1 |

| DAC Value | $V_{(AVDD)}$ | DAC Value | $V_{(AVDD)}$ | DAC Value | $V_{(AVDD)}$ | DAC Value | $V_{(AVDD)}$ |
|---|---|---|---|---|---|---|---|
| 00h | 13.5 V | 10h | 15.1 V | 20h | 16.7 V | 30h | 18.3 V |
| 01h | 13.6 V | 11h | 15.2 V | 21h | 16.8 V | 31h | 18.4 V |
| 02h | 13.7 V | 12h | 15.3 V | 22h | 16.9 V | 32h | 18.5 V |
| 03h | 13.8 V | 13h | 15.4 V | 23h | 17.0 V | 33h | 18.6 V |
| 04h | 13.9 V | 14h | 15.5 V | 24h | 17.1 V | 34h | 18.7 V |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| DAC Value | $V_{(AVDD)}$ | DAC Value | $V_{(AVDD)}$ | DAC Value | $V_{(AVDD)}$ | DAC Value | $V_{(AVDD)}$ |
|---|---|---|---|---|---|---|---|
| 05h | 14.0 V | 15h | 15.6 V | 25h | 17.2 V | 35h | 18.8 V |
| 06h | 14.1 V | 16h | 15.7 V | 26h | 17.3 V | 36h | 18.9 V |
| 07h | 14.2 V | 17h | 15.8 V | 27h | 17.4 V | 37h | 19.0 V |
| 08h | 14.3 V | 18h | 15.9 V | 28h | 17.5 V | 38h | 19.1 V |
| 09h | 14.4 V | 19h | 16.0 V | 29h | 17.6 V | 39h | 19.2 V |
| 0Ah | 14.5 V | 1Ah | 16.1 V | 2Ah | 17.7 V | 3Ah | 19.3 V |
| 0Bh | 14.6 V | 1Bh | 16.2 V | 2Bh | 17.8 V | 3Bh | 19.4 V |
| 0Ch | 14.7 V | 1Ch | 16.3 V | 2Ch | 17.9 V | 3Ch | 19.5 V |
| 0Dh | 14.8 V | 1Dh | 16.4 V | 2Dh | 18.0 V | 3Dh | 19.6 V |
| 0Eh | 14.9 V | 1Eh | 16.5 V | 2Eh | 18.1 V | 3Eh | 19.7 V |
| 0Fh | 15.0 V | 1Fh | 16.6 V | 2Fh | 18.2 V | 3Fh | 19.8 V |

#### *7.7.1.3 Boost HVS Offset Voltage Register (with factory value) – 02h (05h)*

| MSB | Address 01h | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | Reserved | 0 | 1 | 0 | 1 |

| DAC Value | $V_{(OFFSET)}$ | DAC Value | $V_{(OFFSET)}$ | DAC Value | $V_{(OFFSET)}$ | DAC Value | $V_{(OFFSET)}$ |
|---|---|---|---|---|---|---|---|
| 00h | 0.0 V | 04h | 0.8 V | 08h | 1.6 V | 0Ch | 2.4 V |
| 01h | 0.2 V | 05h | 1.0 V | 09h | 1.8 V | 0Dh | 2.6 V |
| 02h | 0.4 V | 06h | 1.2 V | 0Ah | 2.0 V | 0Eh | 2.8 V |
| 03h | 0.6 V | 07h | 1.4 V | 0Bh | 2.2 V | 0Fh | 3.0 V |

#### *7.7.1.4 Boost Current Limit Negative Offset Current Register (with factory value) – 03h (00h)*

| MSB | Address 03h | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | Reserved | Reserved | 0 | 0 | 0 |

| DAC Value | $I_{(OFFSET)}$ | DAC Value | $I_{(OFFSET)}$ | DAC Value | $I_{(OFFSET)}$ | DAC Value | $I_{(OFFSET)}$ |
|---|---|---|---|---|---|---|---|
| 00h | 0.0 A | 02h | 0.8 A | 04h | 1.6 A | 06h | 2.4 A |
| 01h | 0.4 A | 03h | 1.2 A | 05h | 2.0 A | 07h | 2.8 A |

#### *7.7.1.5 Boost Soft-start Time Register (with factory value) – 04h (00h)*

| MSB | Address 04h | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | 0 |

| DAC Value | Time |
|---|---|
| 00h | 10 ms |
| 01h | 20 ms |

#### *7.7.1.6 Buck 1 Output Voltage $V_{(IO)}$ Register (with factory value) – 05h (03h):*

| MSB | Address 05h | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | Reserved | 0 | 0 | 1 | 1 |

| DAC Value | $V_{(IO)}$ | DAC Value | $V_{(IO)}$ | DAC Value | $V_{(IO)}$ | DAC Value | $V_{(IO)}$ |
|---|---|---|---|---|---|---|---|
| 00h | 2.2 V | 04h | 2.6 V | 08h | 3.0 V | 0Ch | 3.4 V |
| 01h | 2.3 V | 05h | 2.7 V | 09h | 3.1 V | 0Dh | 3.5 V |
| 02h | 2.4 V | 06h | 2.8 V | 0Ah | 3.2 V | 0Eh | 3.6 V |
| 03h | 2.5 V | 07h | 2.9 V | 0Bh | 3.3 V | 0Fh | 3.7 V |

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### 7.7.1.7 Buck 2 Output Voltage $V_{(CORE)}$ Register (with factory value) – 06h (02h)

| MSB | Address 06h | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | 0 | 0 | 0 | 1 | 0 |

| DAC Value | $V_{(CORE)}$ | DAC Value | $V_{(CORE)}$ | DAC Value | $V_{(CORE)}$ | DAC Value | $V_{(CORE)}$ |
|---|---|---|---|---|---|---|---|
| 00h | 0.8 V | 07h | 1.5 V | 0Eh | 2.2 V | 15h | 2.9 V |
| 01h | 0.9 V | 08h | 1.6 V | 0Fh | 2.3 V | 16h | 3.0 V |
| 02h | 1.0 V | 09h | 1.7 V | 10h | 2.4 V | 17h | 3.1 V |
| 03h | 1.1 V | 0Ah | 1.8 V | 11h | 2.5 V | 18h | 3.2 V |
| 04h | 1.2 V | 0Bh | 1.9 V | 12h | 2.6 V | 19h | 3.3 V |
| 05h | 1.3 V | 0Ch | 2.0 V | 13h | 2.7 V | | |
| 06h | 1.4 V | 0Dh | 2.1 V | 14h | 2.8 V | | |

### 7.7.1.8 Buck 3 Output Voltage $V_{(HAVDD)}$ Register (with factory value) – 07h (1Bh)

| MSB | Address 07h | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | 0 | 1 | 1 | 0 | 1 | 1 |

| DAC Value | $V_{(HAVDD)}$ | DAC Value | $V_{(HAVDD)}$ | DAC Value | $V_{(HAVDD)}$ | DAC Value | $V_{(HAVDD)}$ |
|---|---|---|---|---|---|---|---|
| 00h | 4.8 V | 10h | 6.4 V | 20h | 8.0 V | 30h | 9.6 V |
| 01h | 4.9 V | 11h | 6.5 V | 21h | 8.1 V | 31h | 9.7 V |
| 02h | 5.0 V | 12h | 6.6 V | 22h | 8.2 V | 32h | 9.8 V |
| 03h | 5.1 V | 13h | 6.7 V | 23h | 8.3 V | 33h | 9.9 V |
| 04h | 5.2 V | 14h | 6.8 V | 24h | 8.4 V | 34h | 10.0 V |
| 05h | 5.3 V | 15h | 6.9 V | 25h | 8.5 V | 35h | 10.1 V |
| 06h | 5.4 V | 16h | 7.0 V | 26h | 8.6 V | 36h | 10.2 V |
| 07h | 5.5 V | 17h | 7.1 V | 27h | 8.7 V | 37h | 10.3 V |
| 08h | 5.6 V | 18h | 7.2 V | 28h | 8.8 V | 38h | 10.4 V |
| 09h | 5.7 V | 19h | 7.3 V | 29h | 8.9 V | 39h | 10.5 V |
| 0Ah | 5.8 V | 1Ah | 7.4 V | 2Ah | 9.0 V | 3Ah | 10.6 V |
| 0Bh | 5.9 V | 1Bh | 7.5 V | 2Bh | 9.1 V | 3Bh | 10.7 V |
| 0Ch | 6.0 V | 1Ch | 7.6 V | 2Ch | 9.2 V | 3Ch | 10.8 V |
| 0Dh | 6.1 V | 1Dh | 7.7 V | 2Dh | 9.3 V | 3Dh | 10.9 V |
| 0Eh | 6.2 V | 1Eh | 7.8 V | 2Eh | 9.4 V | 3Eh | 11.0 V |
| 0Fh | 6.3 V | 1Fh | 7.9 V | 2Fh | 9.5 V | 3Fh | 11.1 V |

### 7.7.1.9 Pos. Charge Pump Low Output Voltage $V_{(GH_L)}$ Register (with factory value) – 08h (08h):

| MSB | Address 08h | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | Reserved | 1 | 0 | 0 | 0 |

| DAC Value | $V_{(GH_L)}$ | DAC Value | $V_{(GH_L)}$ | DAC Value | $V_{(GH_L)}$ | DAC Value | $V_{(GH_L)}$ |
|---|---|---|---|---|---|---|---|
| 00h | 20 V | 04h | 24 V | 08h | 28 V | 0Ch | 32 V |
| 01h | 21 V | 05h | 25 V | 09h | 29 V | 0Dh | 33 V |
| 02h | 22 V | 06h | 26 V | 0Ah | 30 V | 0Eh | 34 V |
| 03h | 23 V | 07h | 27 V | 0Bh | 31 V | 0Fh | 35 V |


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#### 7.7.1.10 Positive Charge Pump Low Output Voltage $V_{(GH_L)}$ to $V_{(GH_H)}$ Positive Offset Voltage $V_{(GH_OFS)}$ Register (with factory value) – 09h (04h):

| MSB | Address 09h | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | Reserved | 0 | 1 | 0 | 0 |

| DAC Value | $V_{(GH_L)}$ | DAC Value | $V_{(GH_L)}$ | DAC Value | $V_{(GH_L)}$ | DAC Value | $V_{(GH_L)}$ |
|---|---|---|---|---|---|---|---|
| 00h | 0 V | 04h | 4 V | 08h | 8 V | 0Ch | 12 V |
| 01h | 1 V | 05h | 5 V | 09h | 9 V | 0Dh | 13 V |
| 02h | 2 V | 06h | 6 V | 0Ah | 10 V | 0Eh | 14 V |
| 03h | 3 V | 07h | 7 V | 0Bh | 11 V | 0Fh | 15 V |

#### 7.7.1.11 Gate Pulse Modulation Limit Voltage Register (with factory value) – 0Ah (00h)

| MSB | Address 0Ah | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | 0 | 0 |

| DAC Value | Limit | DAC Value | Limit |
|---|---|---|---|
| 00h | 0 V | 02h | 10 V |
| 01h | 5 V | 03h | 15 V |

#### 7.7.1.12 Negative Charge Pump Output Voltage $V_{(GL)}$ Register (with factory value) – 0Bh (04h)

| MSB | Address 05h | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | Reserved | 0 | 1 | 0 | 0 |

| DAC Value | $V_{(GL)}$ | DAC Value | $V_{(GL)}$ | DAC Value | $V_{(GL)}$ | DAC Value | $V_{(GL)}$ |
|---|---|---|---|---|---|---|---|
| 00h | –5.5 V | 04h | –7.9 V | 08h | –10.3 V | 0Ch | –12.7 V |
| 01h | –6.1 V | 05h | –8.5 V | 09h | –10.9 V | 0Dh | –13.3 V |
| 02h | –6.7 V | 06h | –9.1 V | 0Ah | –11.5 V | 0Eh | –13.9 V |
| 03h | –7.3 V | 07h | –9.7 V | 0Bh | –12.1 V | 0Fh | –14.5 V |

#### 7.7.1.13 Buck 3 HVS Offset Voltage Register (with factory value) – 0Ch (00h):

| MSB | Address 0Ch | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | Reserved | 0 | 0 | 0 | 0 |

| DAC Value | $V_{(OFFSET)}$ | DAC Value | $V_{(OFFSET)}$ | DAC Value | $V_{(OFFSET)}$ | DAC Value | $V_{(OFFSET)}$ |
|---|---|---|---|---|---|---|---|
| 00h | 0.0 V | 04h | 0.4 V | 08h | 0.8 V | 0Ch | 1.2 V |
| 01h | 0.1 V | 05h | 0.5 V | 09h | 0.9 V | 0Dh | 1.3 V |
| 02h | 0.2 V | 06h | 0.6 V | 0Ah | 1.0 V | 0Eh | 1.4 V |
| 03h | 0.3 V | 07h | 0.7 V | 0Bh | 1.1 V | 0Fh | 1.5 V |

#### 7.7.1.14 Memory Write Remain Time Register (with factory value) – FEh (0Fh):

| MSB | Address FEh | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | Reserved | 1 | 1 | 1 | 1 |

| DAC Value | Remaining Writes | DAC Value | Remaining Writes | DAC Value | Remaining Writes | DAC Value | Remaining Writes |
|---|---|---|---|---|---|---|---|
| 00h | 0 | 04h | 4 | 08h | 8 | 0Ch | 12 |
| 01h | 1 | 05h | 5 | 09h | 9 | 0Dh | 13 |
| 02h | 2 | 06h | 6 | 0Ah | 10 | 0Eh | 14 |
| 03h | 3 | 07h | 7 | 0Bh | 11 | 0Fh | EEPROM |

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# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

Figure 19 shows a typical application circuit suitable for supplying LCD panels with GIP or non-GIP technology.

## 8.2 Typical Applications

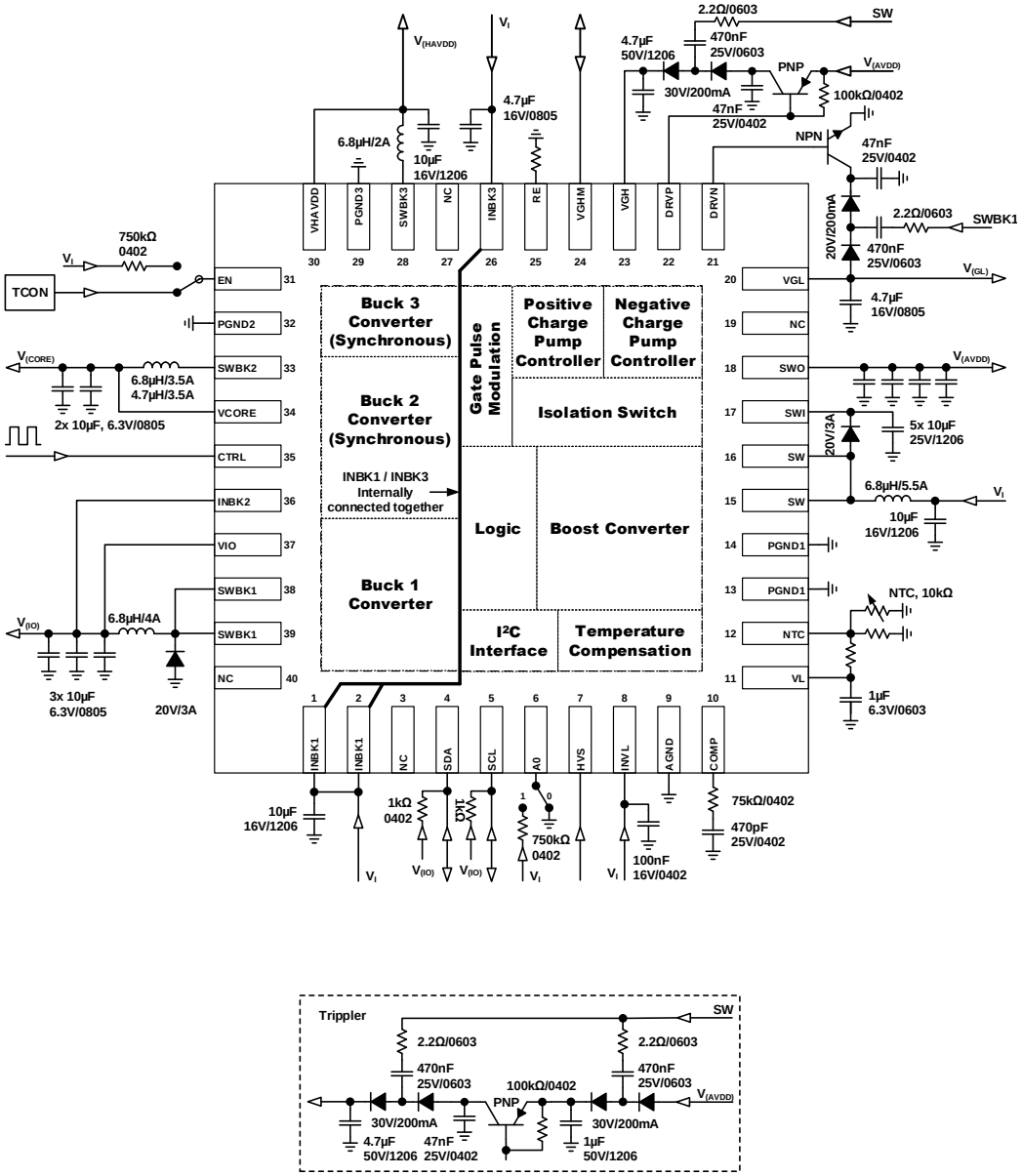


**Figure 19. Typical Application**


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## Typical Applications (continued)

### 8.2.1 Design Requirements

For this design example, use the values shown in Table 6

**Table 6. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| Voltage | $V_I$ = 12 V, $V_{(AVDD)}$ = 18 V, $V_{(HAVDD)}$ = 9 V, $V_{(IO)}$ = 3.3 V, $V_{(CORE)}$ = 1.2 V, $V_{(GH)}$ = 28 V, $V_{(GL)}$ = –10.3 V |
| Switching Frequency | Boost, Buck 1 = 750 kHz, Buck2, Buck 3 = 1 MHz |

### 8.2.2 Detailed Design Procedure

See the *Device Functional Modes* section for the detailed design procedure.

### 8.2.3 Application Curves

| PARAMETER | CONDITIONS | FIGURE |
|---|---|---|
| **SEQUENCING** | | |
| Power-on $V_{(GL)}$ driven by Buck 1 switch node | $V_I$ = 12 V, $V_{(IO)}$ = 3.3 V, $V_{(CORE)}$ = 1.2 V, $V_{(AVDD)}$ = 18 V, $V_{(HAVDD)}$ = 9 V, $V_{(GH)}$ = 28 V, $V_{(GL)}$ = –10.3 V | Figure 20 |
| Power-on $V_{(GL)}$ driven by Boost switch node | $V_I$ = 12 V, $V_{(IO)}$ = 3.3 V, $V_{(CORE)}$ = 1.2 V, $V_{(AVDD)}$ = 18 V, $V_{(HAVDD)}$ = 9 V, $V_{(GH)}$ = 28 V, $V_{(GL)}$ = –10.3 V | Figure 21 |
| **Buck 1 Converter ($V_I$ = 12 V, L = 6.8 µH, $C_{OUT}$ = 30 µF)** | | |
| Efficiency vs. load current | $V_{(IO)}$ = 3.3 V | Figure 22 |
| PWM switching – light load | $V_{(IO)}$ = 3.3 V / 10 mA | Figure 23 |
| PWM switching – normal load | $V_{(IO)}$ = 3.3 V / 500 mA | Figure 24 |
| Load Transient response | $V_{(IO)}$ = 3.3 V / 100 mA → 500 mA | Figure 25 |
| **Buck 2 Converter ($V_I$ = 3.3 V, L = 4.7 µH, $C_{OUT}$ = 20 µF)** | | |
| Efficiency vs. load current | $V_{(CORE)}$ = 1.2 V | Figure 26 |
| PWM switching – light load | $V_{(CORE)}$ = 1.2 V / 10 mA | Figure 27 |
| PWM switching – normal load | $V_{(CORE)}$ = 1.2 V / 500 mA | Figure 28 |
| Load Transient response | $V_{(CORE)}$ = 1.2 V / 10 mA → 300 mA | Figure 29 |
| **Buck 3 Converter ($V_I$ = 12 V, L = 6.8 µH, $C_{OUT}$ = 10 µF)** | | |
| Efficiency vs. load current | $V_{(HAVDD)}$ = 9 V | Figure 30 |
| PWM switching – light load sourcing | $V_{(HAVDD)}$ = 9 V / 10 mA | Figure 31 |
| PWM switching – light load sinking | $V_{(HAVDD)}$ = 9 V / -10 mA | Figure 32 |
| PWM switching –normal load sourcing | $V_{(HAVDD)}$ = 9 V / 500 mA | Figure 33 |
| PWM switching – normal load sinking | $V_{(HAVDD)}$ = 9 V / -500 mA | Figure 34 |
| Load Transient response | $V_{(HAVDD)}$ = 9 V / 0 mA → 300 mA → 0 mA → -350 mA | Figure 35 |
| **Boost Converter ($V_I$ = 12 V, L = 6.8 µH, $C_{(ISOSW)}$ = 10 µF, $C_{OUT}$ = 40 µF)** | | |
| Efficiency vs. load current | $V_{(AVDD)}$ = 18 V | Figure 36 |
| PWM switching – light load | $V_{(AVDD)}$ = 18 V / 10 mA | Figure 37 |
| PWM switching – normal load | $V_{(AVDD)}$ = 18 V / 500 mA | Figure 38 |
| Load Transient response | $V_{(AVDD)}$ = 18 V / 100 mA → 500 mA | Figure 39 |
| **Positive Charge-Pump ($V_I$ = 12 V, Diode = BAV99, $R_{(SW)}$ = 2.2 Ω, Transistor = KTA1666, $C_{OUT}$ = 4.7 µF)** | | |
| Light load operation | $V_{(GH)}$ = 28 V / 10 mA | Figure 40 |
| Normal load operation | $V_{(GH)}$ = 28 V / 50 mA | Figure 41 |
| Load Transient response | $V_{(GH)}$ = 28 V / 10 mA → 50 mA | Figure 42 |
| **Negative Charge-Pump ($V_I$ = 12 V, Diode = BAV99, $R_{(SW)}$ = 2.2 Ω, Transistor = KTC4376, $C_{OUT}$ = 4.7 µF)** | | |
| Light load operation | $V_{(GL)}$ = –7.9 V / 10 mA | Figure 43 |
| Normal load operation | $V_{(GL)}$ = –7.9 V / 50 mA | Figure 44 |
| Load Transient response | $V_{(GL)}$ = –7.9 V / 10 mA → 50 mA | Figure 45 |

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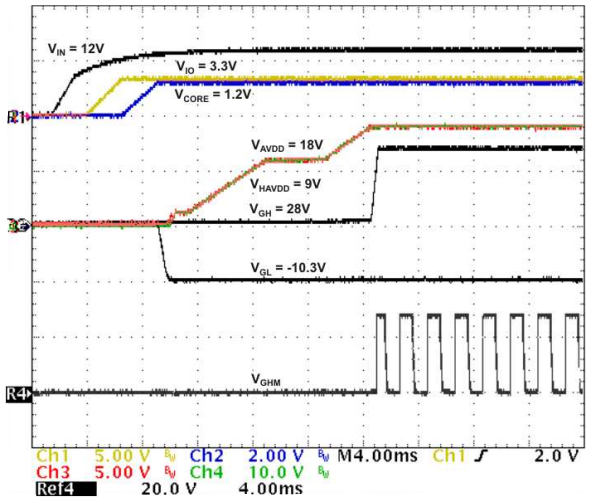


**Figure 20. Startup Sequencing $V_{(GL)}$ Driven By Buck 1**

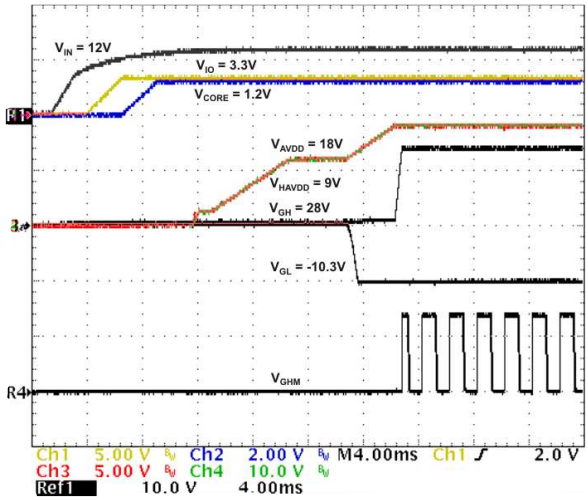


**Figure 21. Startup Sequencing $V_{(GL)}$ Driven By Boost**

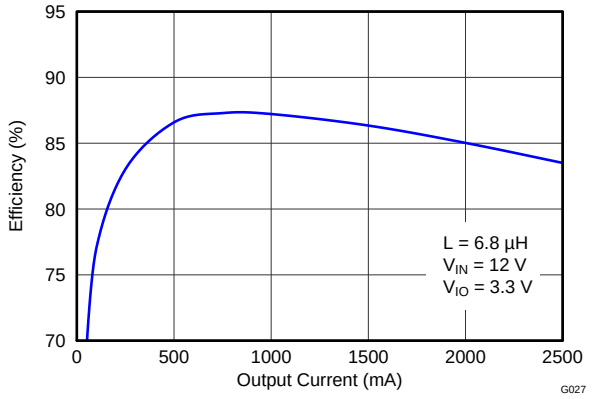


**Figure 22. Buck 1 ($V_{(IO)}$) Efficiency vs Load Current**

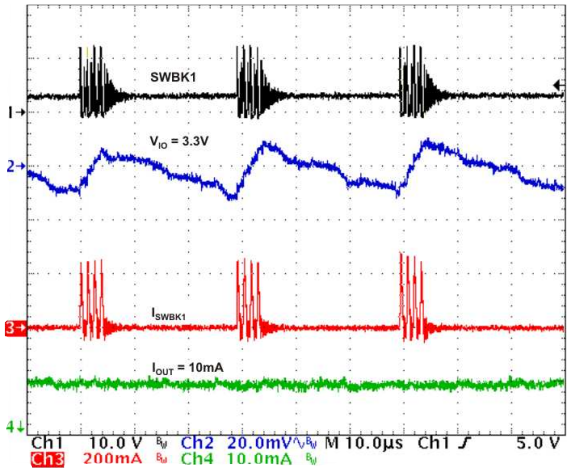


**Figure 23. Buck 1 ($V_{(IO)}$) PWM Switching – Light Load**

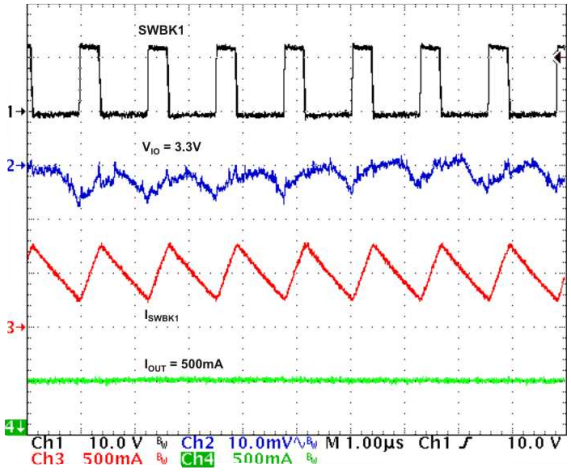


**Figure 24. Buck 1 ($V_{(IO)}$) PWM Switching – Normal Load**

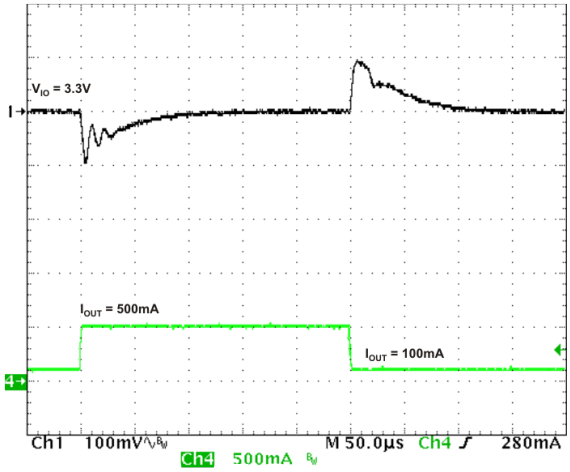


**Figure 25. Buck 1 ($V_{(IO)}$) Load Transient Response**


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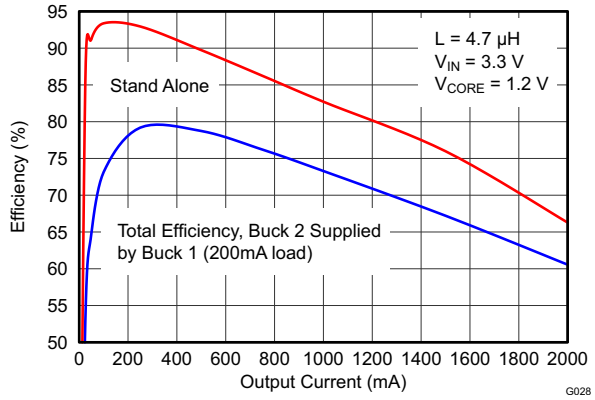


**Figure 26. Buck 2 ($V_{(CORE)}$) Efficiency vs Load Current**

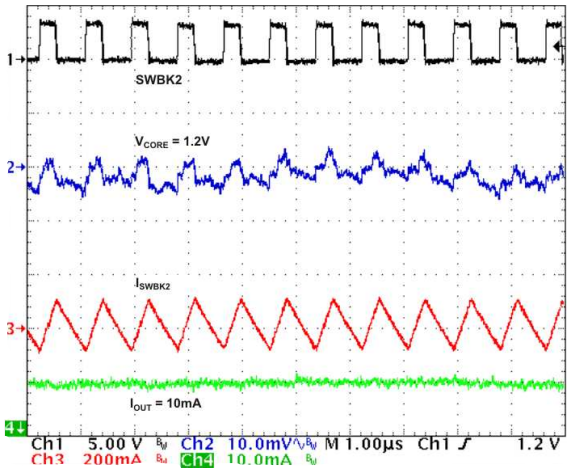


**Figure 27. Buck 2 ($V_{(CORE)}$) PWM Switching – Light Load**

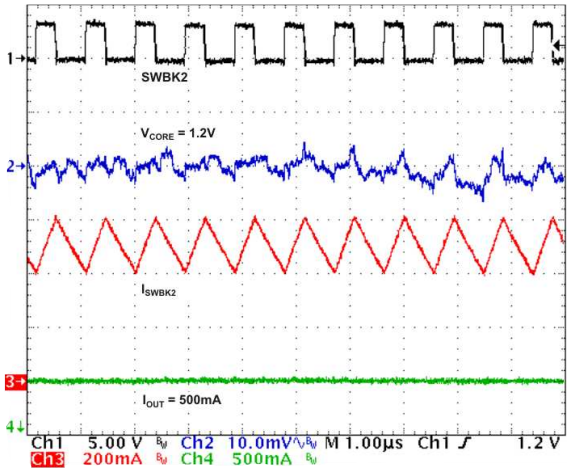


**Figure 28. Buck 2 ($V_{(CORE)}$) PWM Switching – Normal Load**

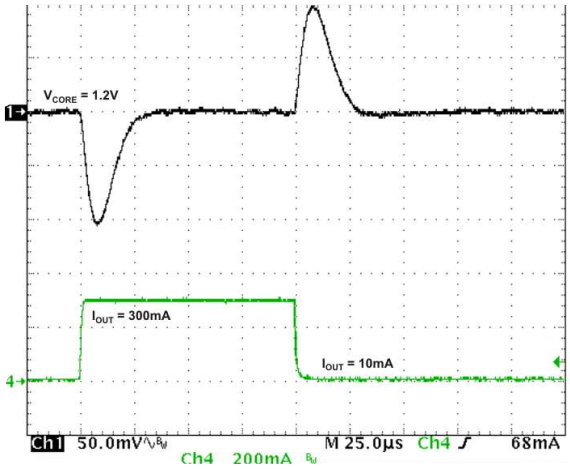


**Figure 29. Buck 2 ($V_{(CORE)}$) Load Transient Response**

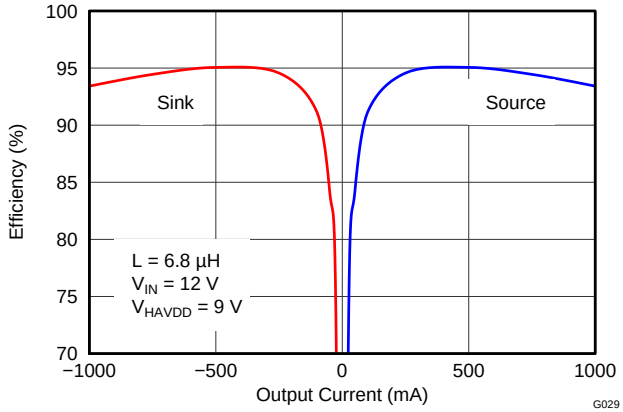


**Figure 30. Buck 3 ($V_{(HAVDD)}$) Efficiency vs Load Current**

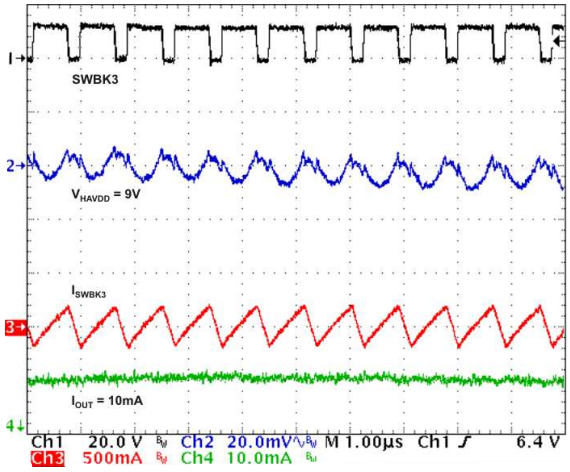


**Figure 31. Buck 3 ($V_{(HAVDD)}$) PWM – Light Load Source**

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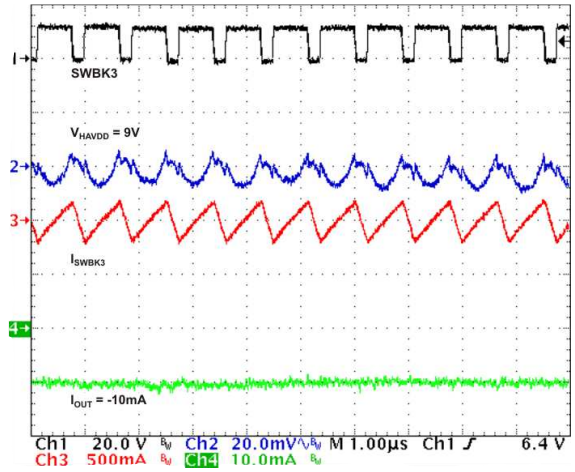


**Figure 32. Buck 3 ($V_{(HAVDD)}$) PWM – Light Load Sink**

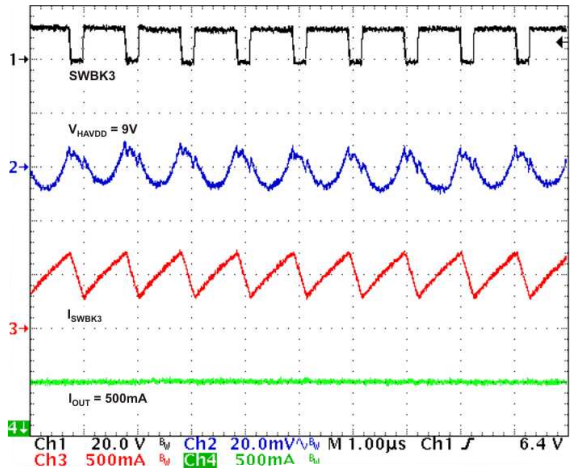


**Figure 33. Buck 3 ($V_{(HAVDD)}$) PWM – Normal Load Source**

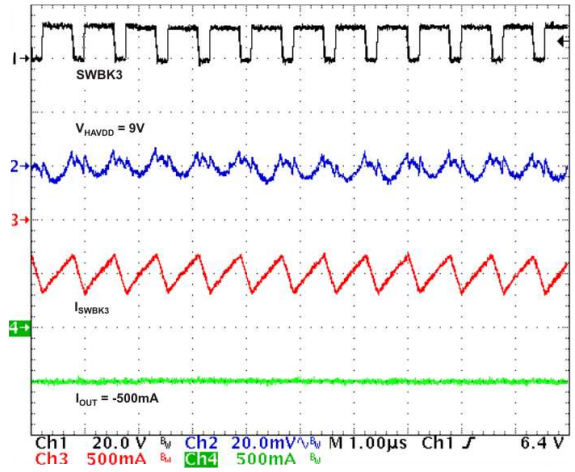


**Figure 34. BUCK 3 ($V_{(HAVDD)}$) PWM – Normal Load Sink**

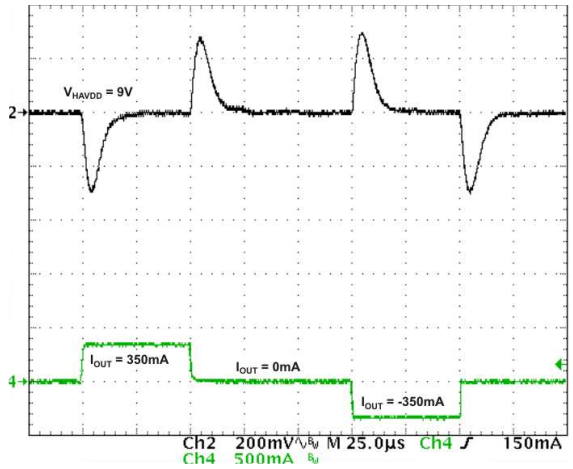


**Figure 35. BUCK 3 ($V_{(HAVDD)}$) Load Transient Response**

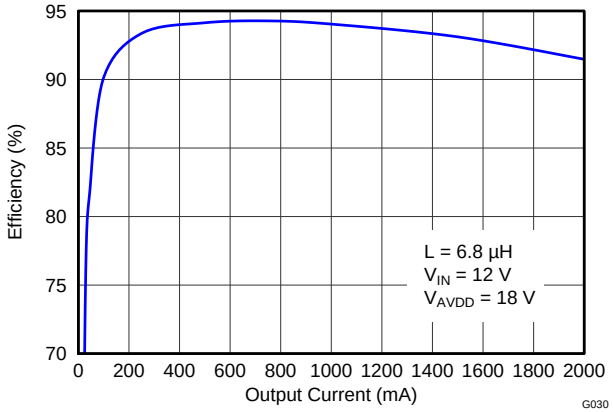


**Figure 36. Boost ($V_{(AVDD)}$) Efficiency vs Load Current**

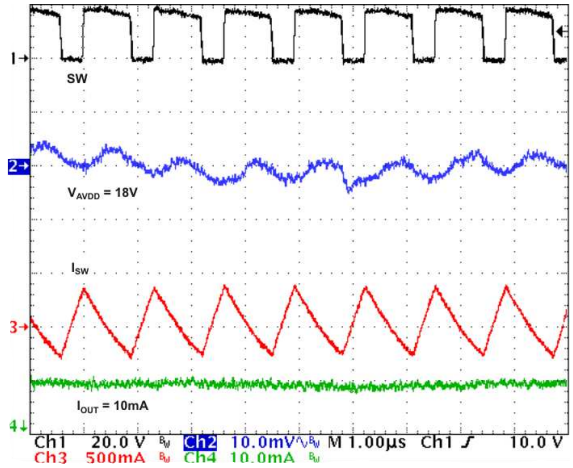


**Figure 37. Boost ($V_{(AVDD)}$) PWM Switching – Light Load**


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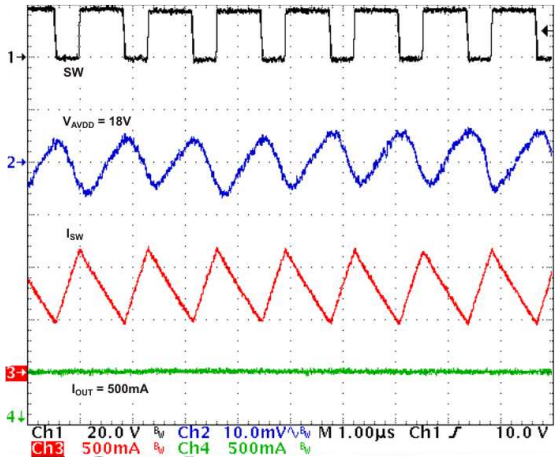


Figure 38. Boost ($V_{(AVDD)}$) PWM Switching – Normal Load

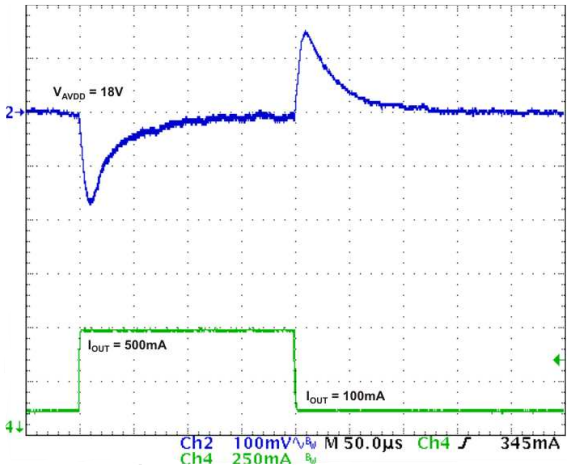


Figure 39. Boost ($V_{(AVDD)}$) Load Transient Response

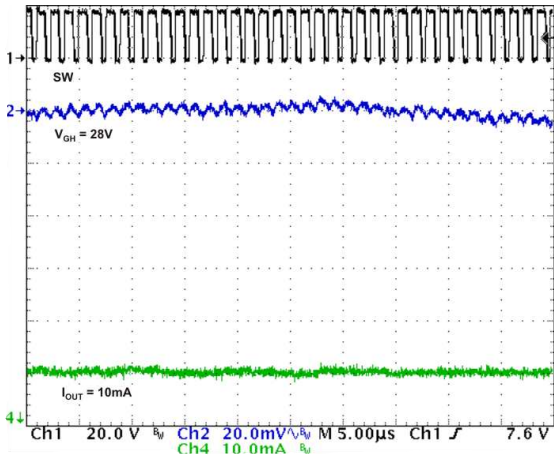


Figure 40. Positive Charge-Pump ($V_{(GH)}$) Light Load

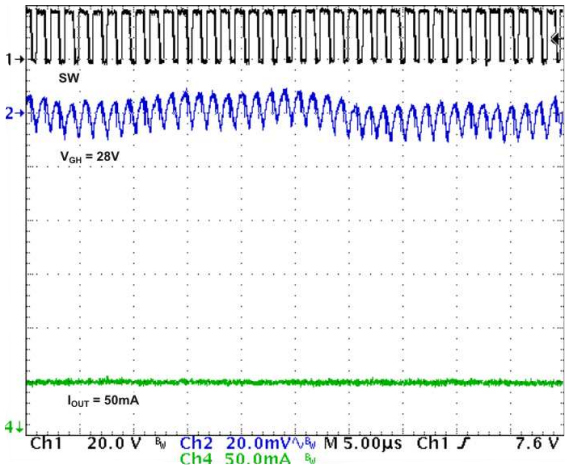


Figure 41. Positive Charge-Pump ($V_{(GH)}$) Normal Load

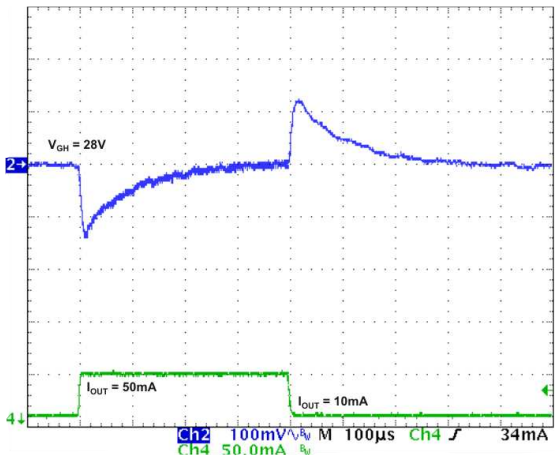


Figure 42. Positive CP ($V_{(GH)}$) Load Transient Response

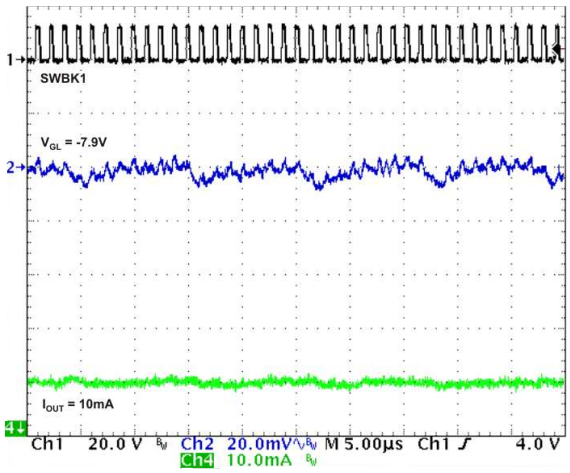


Figure 43. Negative Charge-Pump ($V_{(GL)}$) Light Load

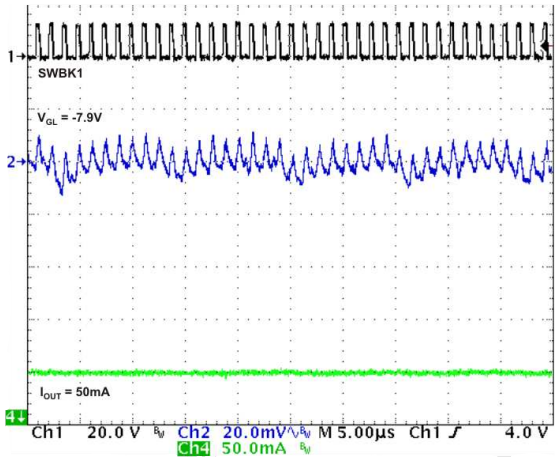


**Figure 44. Negative Charge-Pump ($V_{(GL)}$) Normal Load**

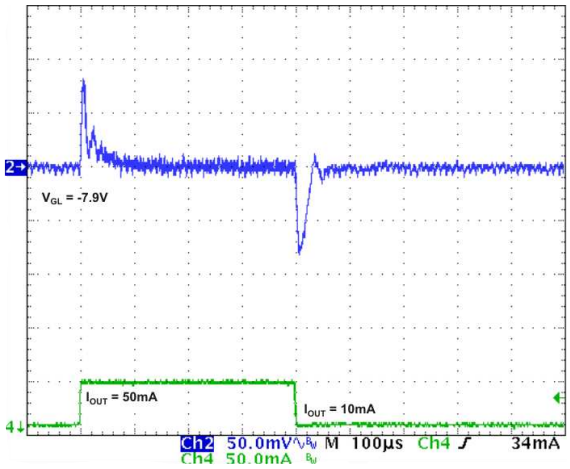


**Figure 45. Negative CP ($V_{(GL)}$) Load Transient Response**


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## 8.3 System Examples

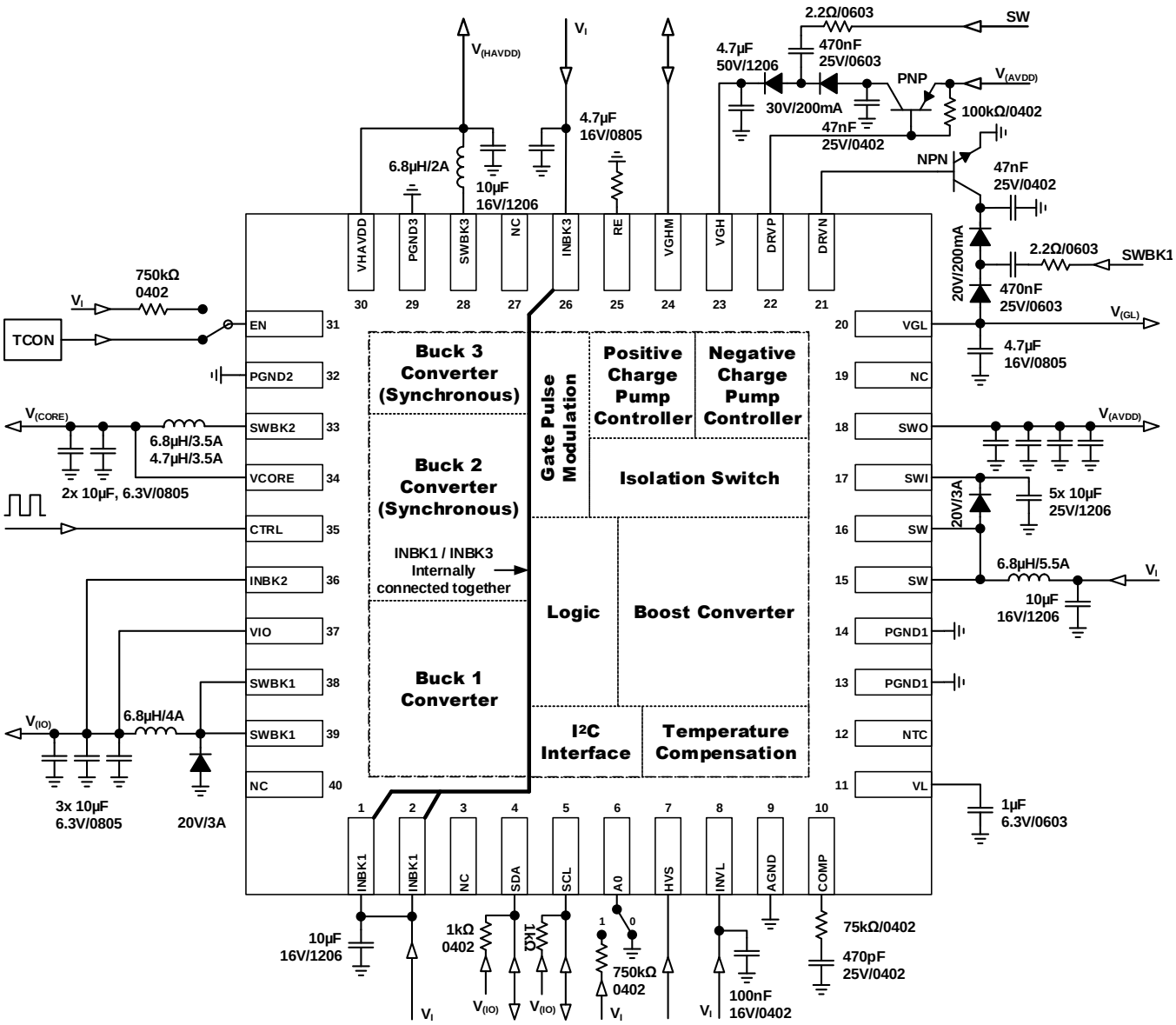


**Figure 46. $V_{(GH)}$ Temperature Compensation Disabled (by $I^2C$)**

## System Examples (continued)

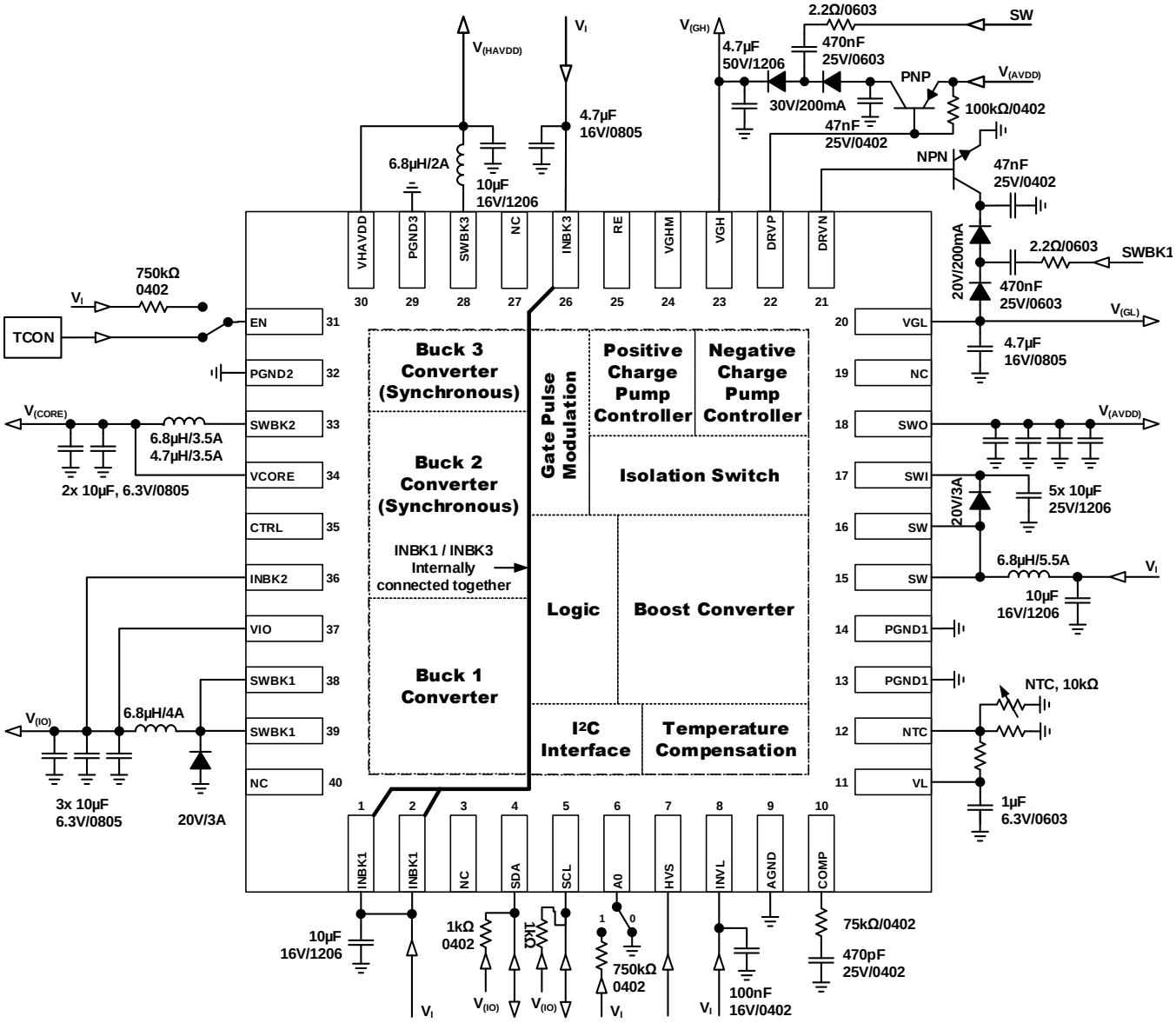


**Figure 47. Gate Pulse Modulation Disabled (by I²C)**


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### System Examples (continued)

For best input voltage filtering low ESR ceramic capacitors are recommended. For better input voltage filtering the capacitor values can be increased.

- **Internal logic:** 100 nF close to the INVL-pin
- **Boost converter:** 10 µF near the inductor
- **Buck 1 converter:** 10 µF close to the INBK1-pins
- **Buck 2 converter:** 4.7 µF close to the INBK2-pin (also one of the Buck 2 output capacitors can be used)
- **Buck 3 converter:** 4.7 µF close to the INBK3-pin

**Table 7. Input Capacitor Selection**

| CAPACITOR | VOLTAGE RATING | TEMPERATURE CHARACTERISTICS | SUPPLIER (1) | COMPONENT CODE |
|---|---|---|---|---|
| 100 nF / 0402 | 16 V | X5R | Murata | GRM155R61C104KA88 |
| 100 nF / 0402 | 16 V | X5R | Taiyo Yuden | EMK105BJ104KV |
| 4.7 µF / 0402 | 6.3 V | X5R | Murata | GRM155R60J475ME87 |
| 4.7 µF / 0402 | 6.3 V | X5R | Taiyo Yuden | JMK105BBJ475MV |
| 4.7 µF / 0805 | 16 V | X5R | Murata | GRM21BR61C475KA88 |
| 4.7 µF / 0805 | 16 V | X5R | Taiyo Yuden | EMK212ABJ475KG |
| 10 µF / 1206 | 16 V | X5R | Murata | GRM31CR61C106KA88 |
| 10 µF / 1206 | 16 V | X7R | Taiyo Yuden | EMK316AB7106KL |

(1) See *Third-Party Products* disclaimer.

## 9 Power Supply Recommendations

The device is designed to operate with input supplies from 8.6 V to 14.7 V. The input supply should be stable and free of noise if the device's full performance is to be achieved.

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# 10 Layout

## 10.1 Layout Guideline

The PCB layout is a very important step in the power supply design. Following points should be considered.

- Place red marked components first and as close as possible to the device, keep red lines short.
- The bolder the line the wider the trace should be on the PCB because bold lines carry high currents.
- The input capacitors for INBK1, INBK3 and INVL should be placed as close as possible to the IC.
- For $V_{(AVDD)}$ the line SW, Diode, SWI as well as the connection PGND to SWI capacitor should be kept short and low resistive.
- The compensation network for the Boost converter $V_{(AVDD)}$ must be placed as close as possible to the IC and connected by short lines to COMP and AGND to avoid noise coupling.
- For $V_{(IO)}$ the line SWBK1, Diode, GND of INBK1 capacitor should be kept short and low resistive.
- For $V_{(CORE)}$ an additional input capacitor should be used when the $V_{(IO)}$ output capacitor line is longer than 1 cm or a wide connection line is not possible to stabilize the input voltage.
- Feedback lines starting at the output capacitors should be routed through a non noisy area away from switching traces. If possible the feedback lines should be kept short to reduce noise coupling.
- Inductors can be placed further away from the IC to avoid IC heating through the inductor.
- All IC Grounds (AGND, PGNDx) must be connected to the Exposed Thermal PAD.
- Avoid vias in Power lines when possible because of their high inductance and resistance.
- The Exposed Thermal PAD of the QFN package must be soldered to a big GND cooling area. For good thermal conduction to the cooling area as much as possible vias should be used to keep the device cool.
- The thermal resistor NTC should be placed away from heat sources. For most accurate environment temperature measurement the NTC must be placed at the coldest point of the PCB.

## 10.2 Layout Example

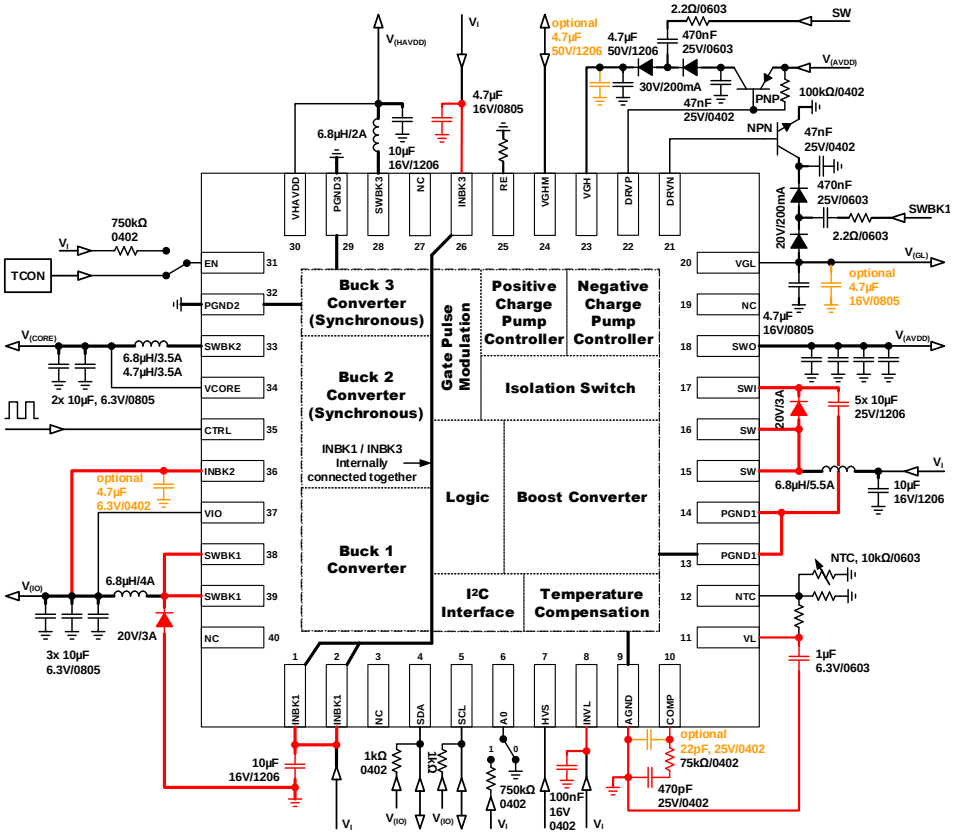


**Figure 48. Example Layout**


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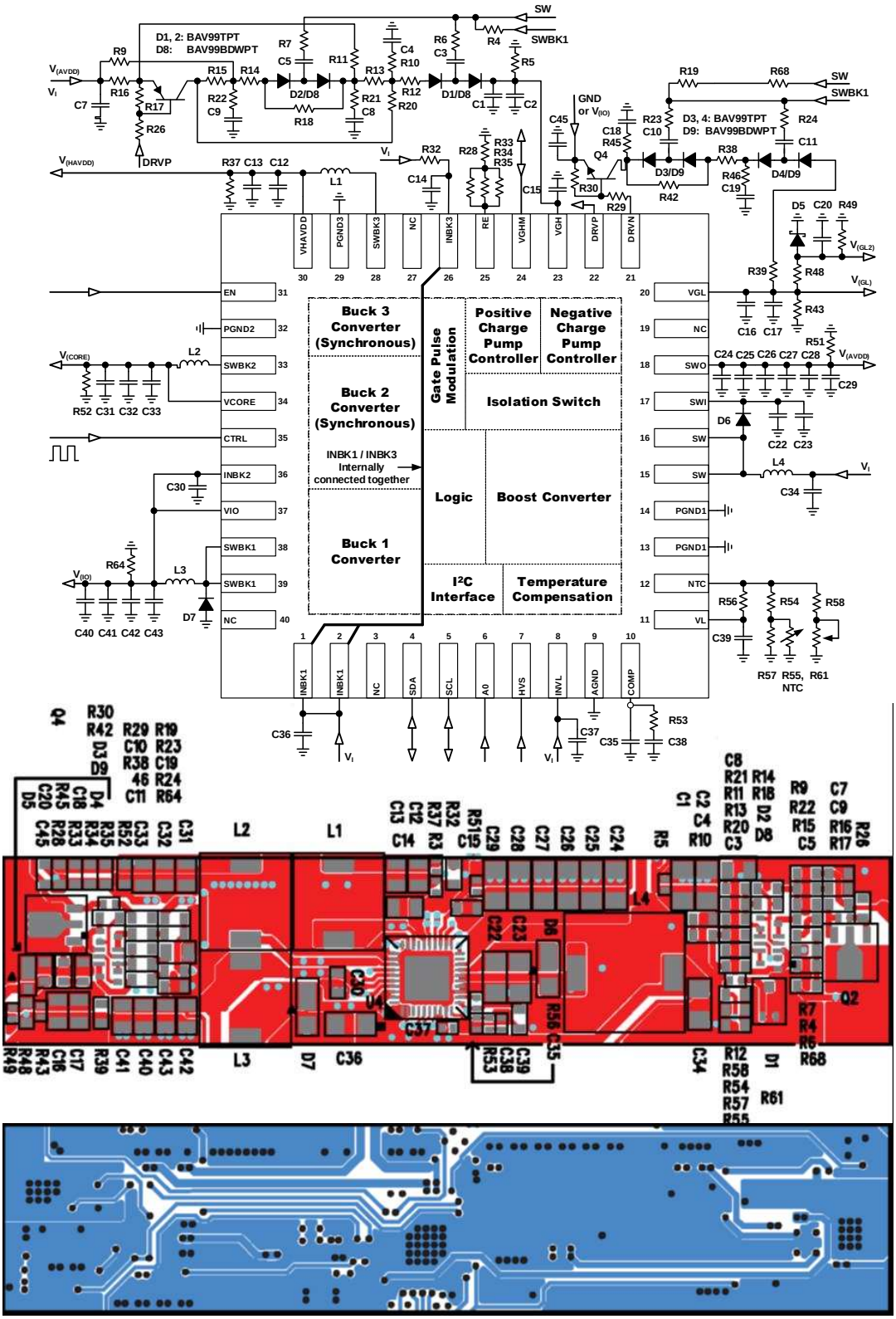
## Layout Example (continued)




Options can be removed if not needed

**Figure 49. Sample 2-layer Layout**

# 11 器件和文档支持

## 11.1 相关链接

以下表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **8.** 相关链接

| 器件 | 产品文件夹 | 样片与购买 | 技术文章 | 工具与软件 | 支持与社区 |
|---|---|---|---|---|---|
| TPS65177 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| TPS65177A | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |

## 11.2 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

## 11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

## 11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。要获得这份数据表的浏览器版本，请查阅左侧的导航栏。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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS65177ARHAR | Active | Production | VQFN (RHA) \| 40 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 150 | TPS 65177A |
| TPS65177ARHAR.A | Active | Production | VQFN (RHA) \| 40 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 150 | TPS 65177A |
| TPS65177RHAR | NRND | Production | VQFN (RHA) \| 40 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | TPS 65177 |
| TPS65177RHAR.A | NRND | Production | VQFN (RHA) \| 40 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | TPS 65177 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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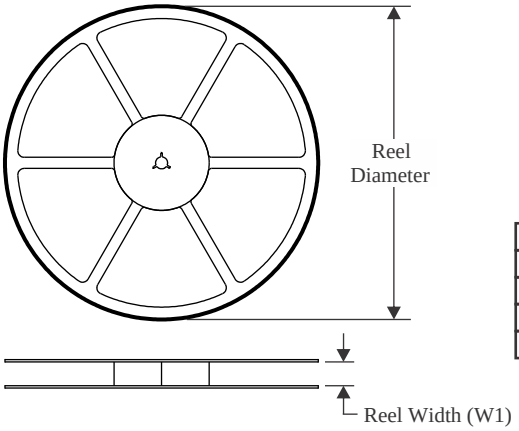
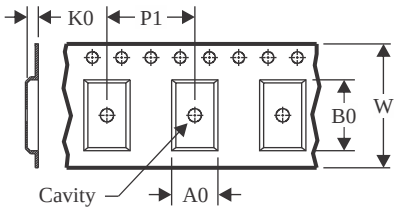
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

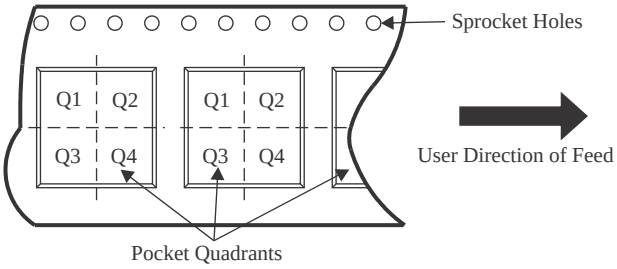



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

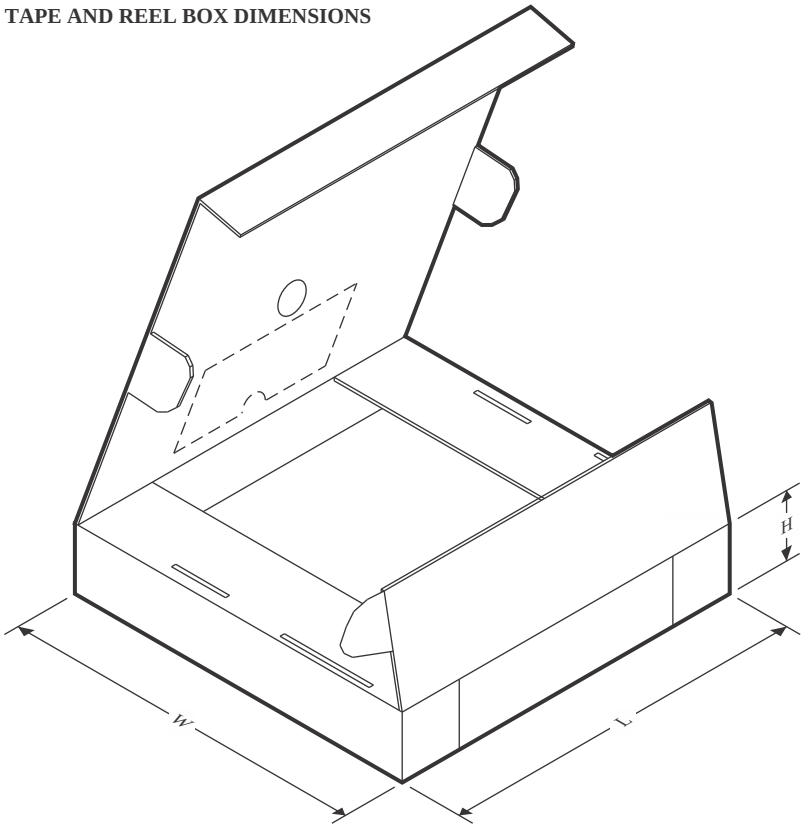
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS65177ARHAR | VQFN | RHA | 40 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS65177RHAR | VQFN | RHA | 40 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |

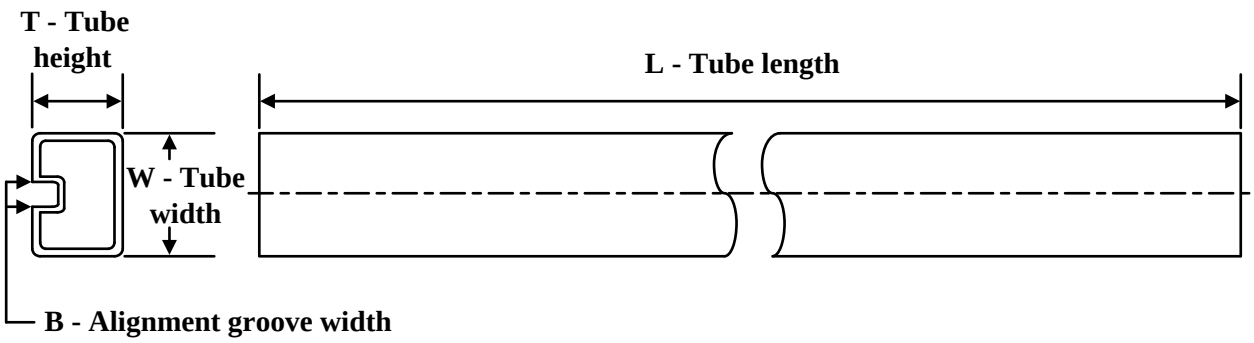
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS65177ARHAR | VQFN | RHA | 40 | 2500 | 552.0 | 367.0 | 38.0 |
| TPS65177RHAR | VQFN | RHA | 40 | 2500 | 552.0 | 367.0 | 38.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| TPS65177ARHAR | RHA | VQFN | 40 | 2500 | 381.5 | 7.92 | 2286 | 0 |
| TPS65177ARHAR.A | RHA | VQFN | 40 | 2500 | 381.5 | 7.92 | 2286 | 0 |
| TPS65177RHAR | RHA | VQFN | 40 | 2500 | 381.5 | 7.92 | 2286 | 0 |
| TPS65177RHAR.A | RHA | VQFN | 40 | 2500 | 381.5 | 7.92 | 2286 | 0 |

# GENERIC PACKAGE VIEW

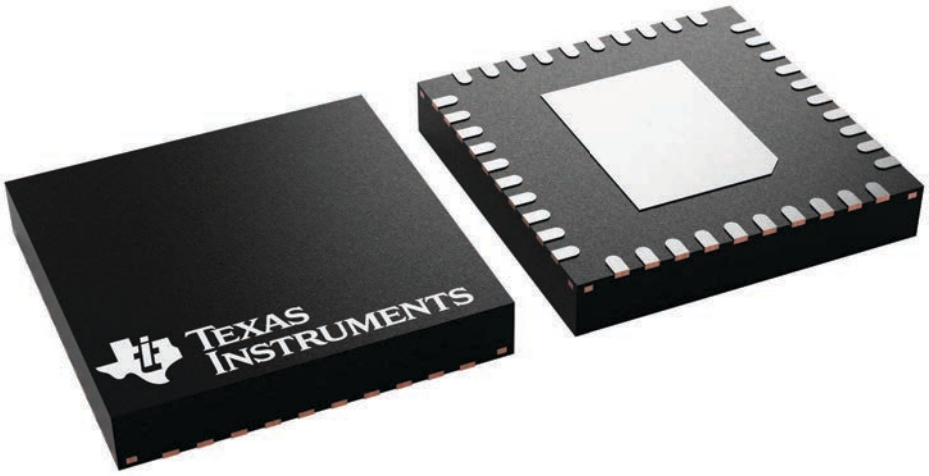
## RHA 40

## VQFN - 1 mm max height

**6 x 6, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4225870/A

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