TPS63025x 高电流、高效单电感器降压-升压转换器

1 特性

- 支持降压和升压运行间自动和无缝转换的实际降压或升压运行
- 输入电压范围 2.3V 至 5.5V
- 2A 持续输出电流：V_{IN} ≥ 2.7V，V_{OUT} = 3.3V
- 可调和固定输出电压
- 在降压或升压模式中效率高达 95%，而在 V_{IN} = V_{OUT} 时，效率高达 97%
- 2.5MHz 典型开关频率
- 运行静态电流 35μA
- 集成软启动
- 省电模式
- 真正关断功能
- 输出电容器放电功能
- 过热保护和过流保护
- 宽电容值选择
- 小型 1.766mm x 2.086mm，20 引脚晶圆级芯片尺寸 (WCSP) 封装

2 应用范围

- 手机、智能电话
- 平板个人电脑
- 个人电脑和智能手机配件
- 负载点稳压
- 电池供电类应用

3 说明

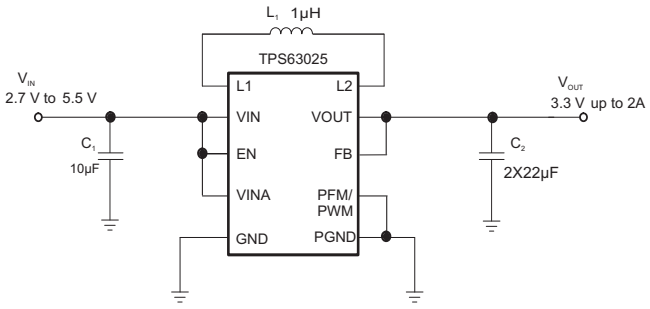
TPS63025 是一款高效、低静态电流降压-升压转换器，此转换器适用于输入电压会高于或低于输出的应用。 输出电流在升压模式中会高达 2A，而在降压模式中会高达 4A。 开关内的最大平均电流被限制在 4A（典型值）。 TPS63025 根据输入电压在降压或升压模式之间自动切换，以便在整个输入电压范围内调节输出电压，从而确保两个模式间的无缝转换。 此降压-升压转换器基于一个使用同步整流的固定频率、脉宽调制 (PWM) 控制器以获得最高效率。 在低负载电流情况下，此转换器进入省电模式，以便在整个负载电流范围内保持高效率。 有一个使用户能够在自动 PFM/PWM 模式运行和强制 PWM 运行之间进行选择的 PFM/PWM 引脚。 在 PWM 模式期间，通常使用一个 2.5MHz 的固定频率。 使用一个外部电阻分压器可对输出电压进行编程，或者在芯片上对输出电压进行内部固定。 转换器可被禁用以最大限度地减少电池消耗。 在关断期间，负载从电池上断开。 此器件采用 20 引脚，1.766mm x 2.086 mm，WCSP 封装。

器件信息(1)

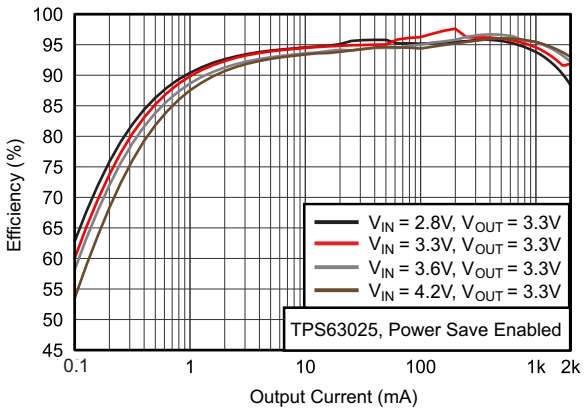
产品型号	封装	封装尺寸（标称值）
TPS630250	芯片尺寸球状引脚栅格阵列 (DSBGA) (20)	1.766mm x 2.086mm
TPS630251		
TPS630252		

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

4 典型应用



效率与输出电流间的关系



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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5 修订历史记录

Changes from Original (May 2014) to Revision A **Page**

- 已将标题的产品型号从 TPS63025 改为 TPS630250，TPS630251，TPS630252 ... 1
- Changed Load Regulation Typ spec from "125 mV/A" to "2.5 mV/A" ... 5

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6 Device Comparison Table

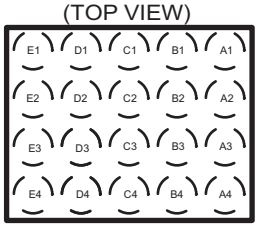
PART NUMBER (1)	VOUT
TPS630250YFF	Adjustable
TPS630251YFF	2.9V
TPS630252YFF	3.3V

(1) For all available packages, see the orderable addendum at the end of the datasheet.

7 Pin Configuration and Functions

WCSP
20-Pin
YFF

(TOP VIEW)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VOUT	A1,A2,A3	PWR	Buck-boost converter output
FB	A4	IN	Voltage feedback of adjustable version, must be connected to VOUT on fixed output voltage versions
L2	B1,B2,B3	PWR	Connection for Inductor
PFM/PWM	B4	IN	set low for PFM mode, set high for forced PWM mode. It must not be left floating
PGND	C1,C2,C3	PWR	Ground for Power stage
GND	C4	PWR	Ground for Control stage
L1	D1,D2,D3	PWR	Connection for Inductor
EN	D4	IN	Enable input. Set high to enable and low to disable. It must not be left floating.
VIN	E1,E2,E3	PWR	Supply voltage for power stage
VINA	E4	PWR	Supply voltage for control stage.

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8 Specifications

8.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		
		MIN	MAX	UNIT
Voltage(2)	L2(3), VOUT, FB	–0.3	4	V
	VIN, L1(3), EN, VINA, PFM/PWM	–0.3	7	V
Input current	Continuos average current into L1(4)		2.7	A
Operating junction temperature, T_J		–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are DC-voltages with respect to ground terminal.
(3) L2, L1 voltage can exceed Absolute Maximum ratings during normal operation. As long as the device is operated within recommend operating conditions device reliability is not affected.
(4) Maximum continuos average input current 3.5A, under those condition do not exceed 105°C for more than 25% operating time.

8.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	700	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions(1)

		MIN	TYP	MAX	UNIT
VIN	Input Voltage Range	2.3		5.5	V
VOUT	Output Voltage	2.3		3.6	V
L	Inductance (2)	0.5	1	1.3	µH
C_{out}	Output Capacitance(3)	20			µF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating virtual junction temperature	–40		125	°C

(1) Refer to the Application Information section for further information
(2) Effective inductance value at operating condition. The nominal value given matches a typical inductor to be chosen to meet the inductance required.
(3) Due to the dc bias effect of ceramic capacitors, the effective capacitance is lower then the nominal value when a voltage is applied. This is why the capacitance is specified to allow the selection of the nominal capacitor required with the dc bias effect for this type of cap. The nominal value given matches a typical capacitor to be chosen to meet the minimum capacitance required.

8.4 Thermal Information

THERMAL METRIC(1)		TPS63025x YFF 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	10.1	
ψ_{JT}	Junction-to-top characterization parameter	1.4	
ψ_{JB}	Junction-to-board characterization parameter	9.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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8.5 Electrical Characteristics

T_J=-40°C to 125°C, typical values are at T_A=25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY							
V_{IN}	Input voltage range			2.3		5.5	V
V_{IN_Min}	Minimum input voltage to turn on into full load		I_{OUT}=2A		2.8		V
I_{OUT}	Continuos Output Current (1)				2		A
I_Q	Quiescent current	V_{IN}	I_{OUT}=0mA, EN=V_{IN}=3.6V, V_{OUT}=3.3V T_J=-40°C to 85°C, not switching		35	70	µA
		V_{OUT}				12	µA
I_{sd}	Shutdown current		EN=low, T_J=-40°C to 85°C		0.1	2	µA
UVLO	Under voltage lockout threshold		V_{IN} falling	1.6	1.7	1.9	V
	Under voltage lockout hysteresis				180		mV
	Thermal shutdown		Temperature rising		140		°C
	Thermal Shutdown hysteresis				20		°C
LOGIC SIGNALS EN, PFM/PWM							
V_{IH}	High level input voltage		V_{IN}=2.3V to 5.5V	1.2			V
V_{IL}	Low level input voltage		V_{IN}=2.3V to 5.5V			0.4	V
I_{lkg}	Input leakage current		EN=GND or V_{IN}		0.01	0.2	µA
OUTPUT							
V_{OUT}	Output Voltage range			2.3		3.6	V
V_{FB}	TPS630250 Feedback regulation voltage				0.8		V
V_{FB}	TPS630250 Feedback voltage accuracy (2)		PWM mode	-1%		1%	
V_{FB}	TPS630250 Feedback voltage accuracy (2)		PFM mode	-1%	1.3%	+3%	
V_{OUT}	TPS630251 Output voltage accuracy (2)		PWM mode	2.871	2.9	2.929	V
V_{OUT}	TPS630251 Output voltage accuracy (2)		PFM mode	2.871	2.938	2.987	V
V_{OUT}	TPS630252 Output voltage accuracy (2)		PWM mode	3.267	3.3	3.333	V
V_{OUT}	TPS630252 Output voltage accuracy (2)		PFM mode	3.267	3.343	3.399	V
$I_{PWM/PFM}$	Output current to enter PFM mode		V_{IN} =3V; V_{OUT} = 3.3V		350		mA
I_{FB}	Feedback input bias current		V_{FB} = 0.8V		10	100	nA
$R_{DS_Buck(on)}$	High side FET on-resistance		V_{IN}=3.0V, V_{OUT}=3.3V		35		mΩ
	Low side FET on-resistance		V_{IN}=3.0V, V_{OUT}=3.3V		50		mΩ
$R_{DS_Boost(on)}$	High side FET on-resistance		V_{IN}=3.0V, V_{OUT}=3.3V		25		mΩ
	Low side FET on-resistance		V_{IN}=3.0V, V_{OUT}=3.3V		50		mΩ
I_{IN}	Average input current limit (3)		V_{IN}=3.0V, V_{OUT}=3.3V T_J=65°C to 125°C	3.5	4.5	5	A
f_s	Switching Frequency				2.5		MHz
R_{ON_DISC}	Discharge ON-Resistance		EN=low		120		Ω
	Line regulation		V_{IN}=2.8V to 5.5V, I_{OUT}=2A		7.4		mV/V
	Load regulation		V_{IN}=3.6V,I_{OUT}=0A to 2A		2.5		mV/A

(1) For minimum and maximum output current in a specific working point see Figure 1 and Equation 1 trough Equation 4.
(2) Conditions: L=1 µH, C_{OUT}= 2 × 22 µF.
(3) For variation of this parameter with Input voltage and temperature see Figure 1.

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8.6 Timing Requirements

T_J=-40°C to 125°C, typical values are at T_A=25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
t_{SS}	Soft-start time	V_{OUT}=EN=low to high, Buck mode V_{IN}=3.6V, V_{OUT}=3.3V, I_{OUT}=2A		450		µs
		V_{OUT}=EN=low to high, Boost mode V_{IN}=2.8V, V_{OUT}=3.3V, I_{OUT}=2A		700		µs
t_d	Start up delay	Time from when EN=high to when device starts switching		100		µs

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8.7 Typical Characteristics

Table 1. Table Of Graphs

DESCRIPTION		FIGURE
Minimum average input current	vs Input voltage (TPS63025, V_{OUT} = 3.3V)	Figure 1
Efficiency	vs Output current (TPS63025, Power Save Enabled, V_{OUT} = 3.3V)	Figure 2
	vs Output current (TPS63025, Power Save Disabled, V_{OUT} = 3.3V)	Figure 3
	vs Output current (TPS63025, Power Save Enabled, V_{OUT} = 2.9V)	Figure 4
	vs Output current (TPS63025, Power Save Disabled, V_{OUT} = 2.9V)	Figure 5
	vs Input voltage (TPS63025, Power Save Enabled, V_{OUT} = 3.3V, I_{OUT} = {10mA; 20mA; 1A; 2A})	Figure 6
	vs Input voltage (TPS63025, Power Save Disabled, V_{OUT} = 3.3V, I_{OUT} = {10mA; 20mA; 1A; 2A})	Figure 7
	vs Input voltage (TPS63025, Power Save Enabled, V_{OUT} = 2.9V, I_{OUT} = {10mA; 20mA; 1A; 2A})	Figure 8
	vs Input voltage (TPS63025, Power Save Disabled, V_{OUT} = 2.9V, I_{OUT} = {10mA; 20mA; 1A; 2A})	Figure 9
Output voltage	vs Output current (TPS63025, V_{IN} =2.8V, 3,3V, 3.6V, 4.2V, V_{OUT} = 3.3V)	Figure 10
	vs Output current (TPS63025, V_{IN} =2.8V, 3,3V, 3.6V, 4.2V, V_{OUT} = 3.3V)	Figure 11

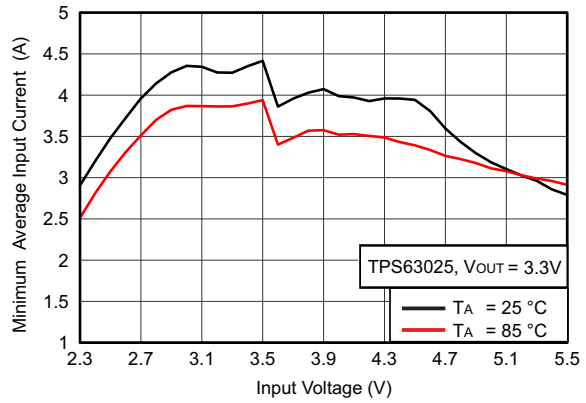


Figure 1. Minimum Average Input Current vs Input Voltage

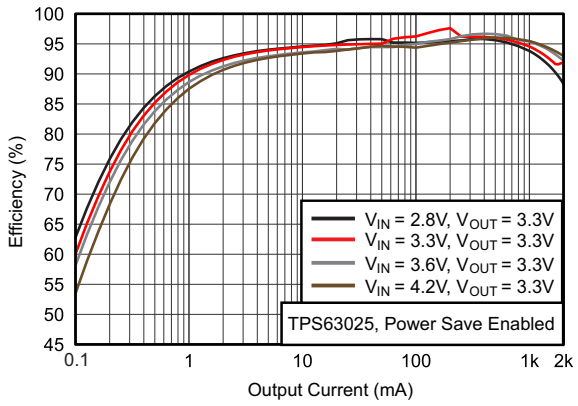


Figure 2. Efficiency vs Output Current

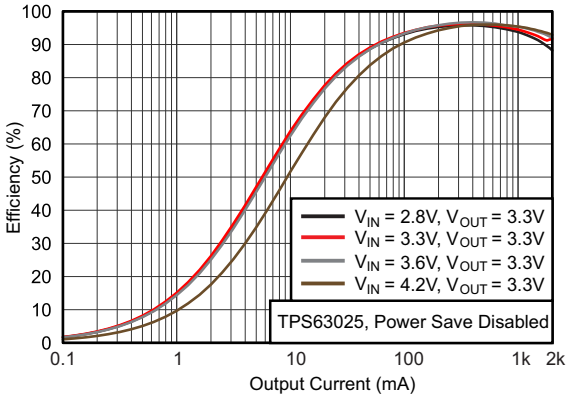


Figure 3. Efficiency vs Output Current

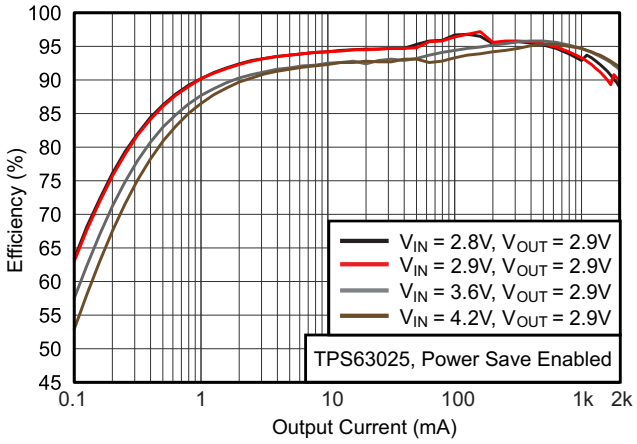


Figure 4. Efficiency vs Output Current

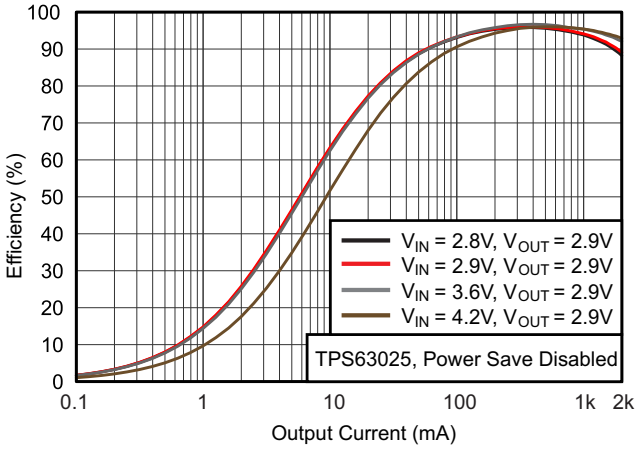


Figure 5. Efficiency vs Output Current

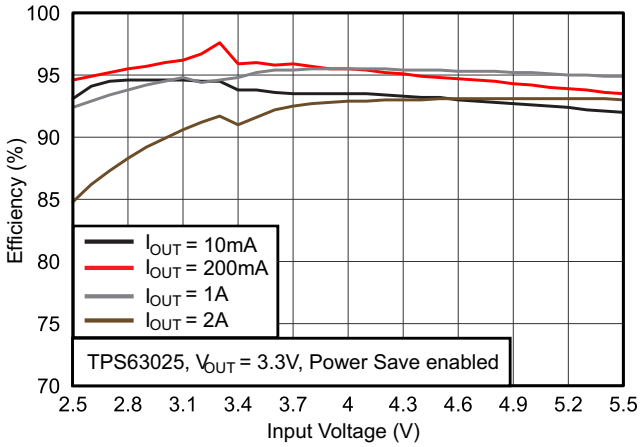


Figure 6. Efficiency vs Input Voltage

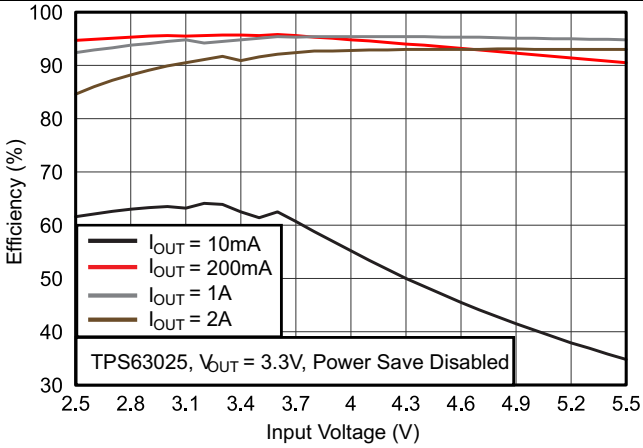


Figure 7. Efficiency vs Input Voltage

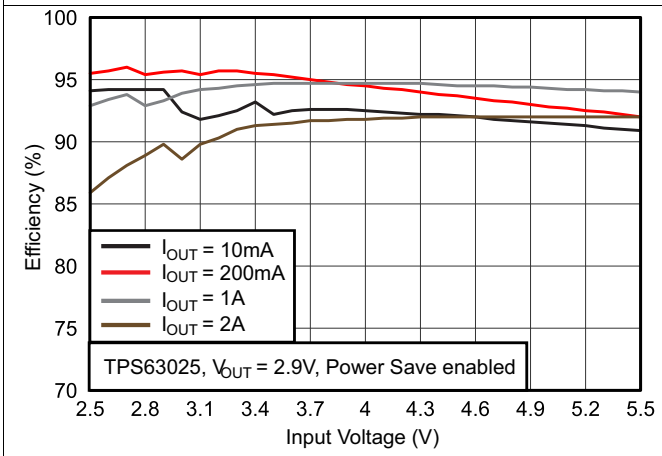


Figure 8. Efficiency vs Input Voltage

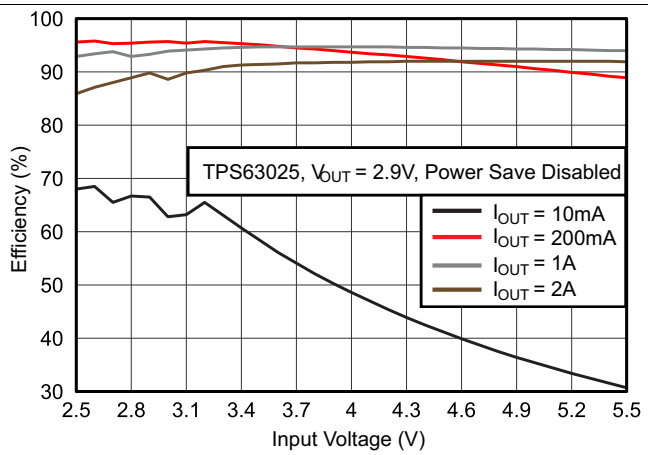


Figure 9. Efficiency vs Input Voltage

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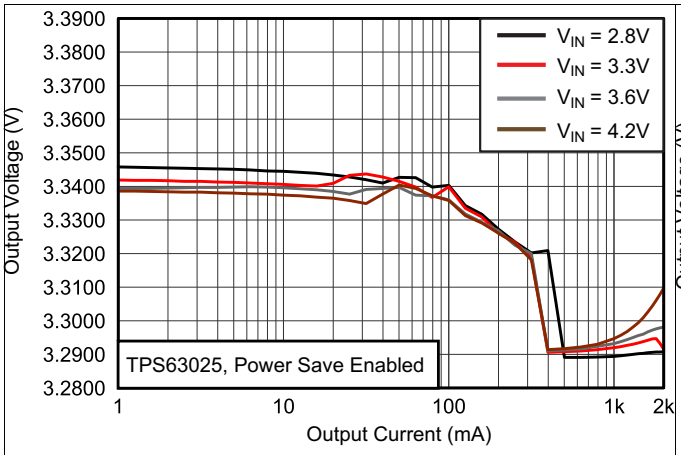


Figure 10. Output Voltage vs Output Current

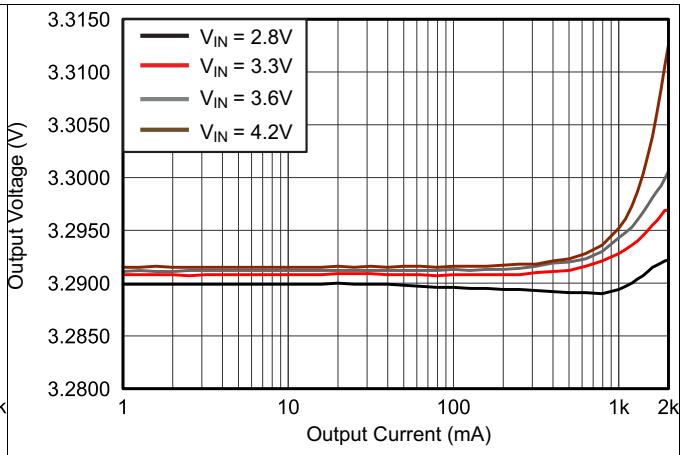


Figure 11. Output Voltage vs Output Current

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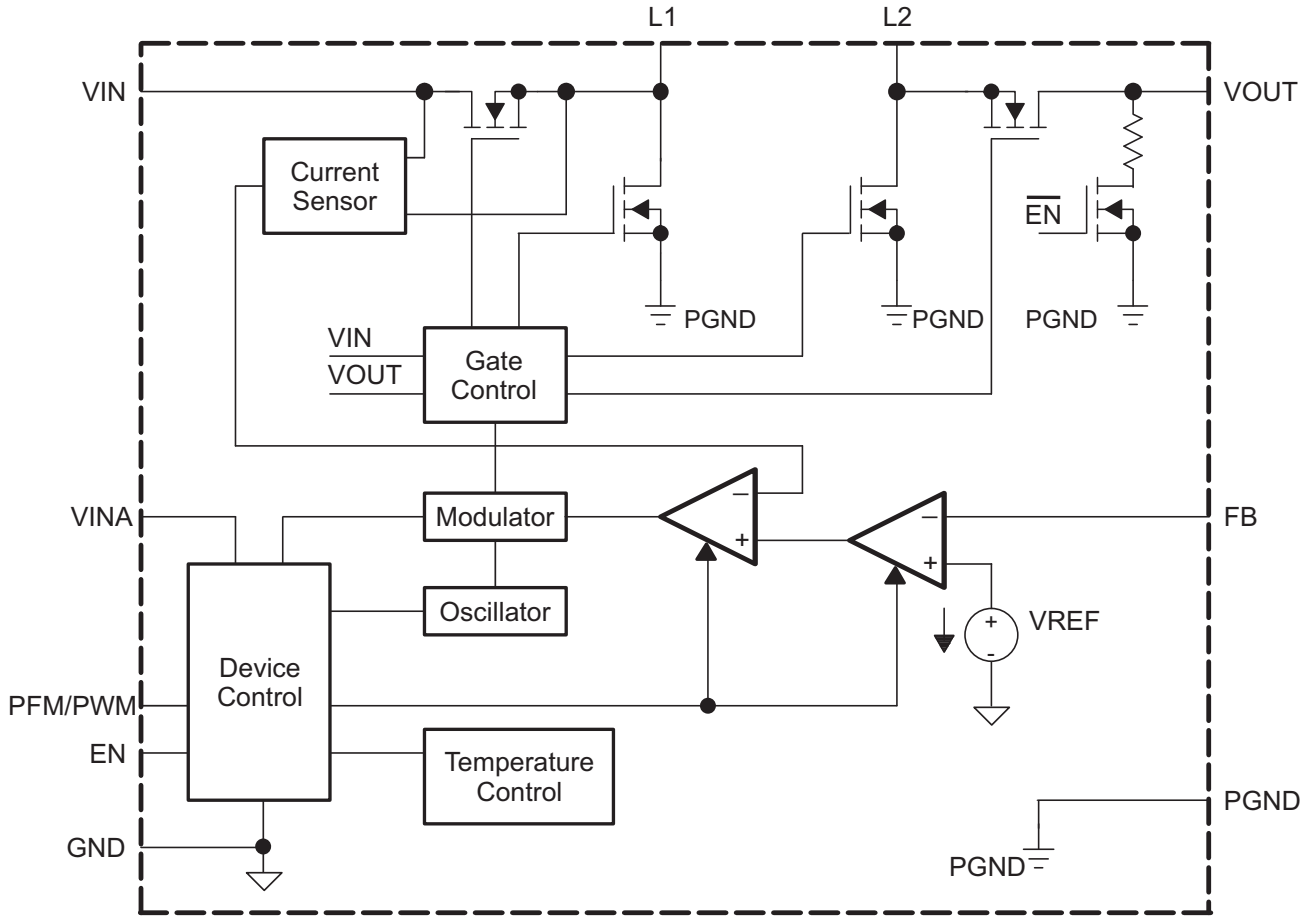
9 Detailed Description

9.1 Overview

The TPS63025 use 4 internal N-channel MOSFETs to maintain synchronous power conversion at all possible operating conditions. This enables the device to keep high efficiency over the complete input voltage and output power range. To regulate the output voltage at all possible input voltage conditions, the device automatically switches from buck operation to boost operation and back as required by the configuration. It always uses one active switch, one rectifying switch, one switch is held on, and one switch held off. Therefore, it operates as a buck converter when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. There is no mode of operation in which all 4 switches are switching at the same time. Keeping one switch on and one switch off eliminates their switching losses. The RMS current through the switches and the inductor is kept at a minimum, to minimize switching and conduction losses. Controlling the switches this way allows the converter to always keep higher efficiency.

The device provides a seamless transition from buck to boost or from boost to buck operation.

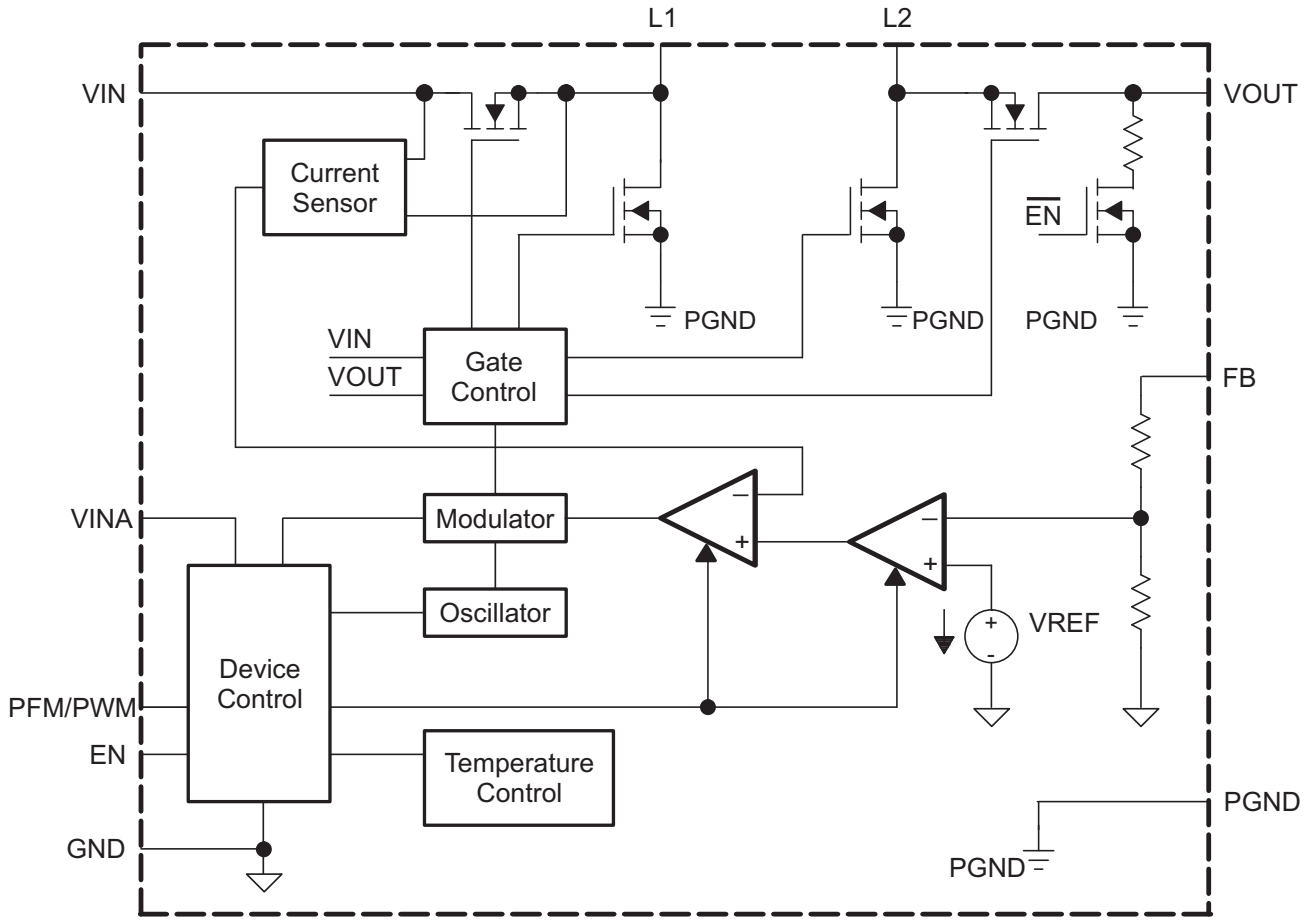
9.2 Functional Block Diagram



Functional Block Diagram (Adjustable Output Voltage)

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Functional Block Diagram (continued)



Functional Block Diagram (Fixed Output Voltage)

9.3 Feature Description

9.3.1 Control Loop Description

The controller circuit of the device is based on an average current mode topology. The average inductor current is regulated by a fast current regulator loop which is controlled by a voltage control loop. Figure 12 shows the control loop.

The non inverting input of the transconductance amplifier, Gmv, is assumed to be constant. The output of Gmv defines the average inductor current. The inductor current is reconstructed by measuring the current through the high side buck MOSFET. This current corresponds exactly to the inductor current in boost mode. In buck mode the current is measured during the on time of the same MOSFET. During the off time, the current is reconstructed internally starting from the peak value reached at the end of the on time cycle. The average current is then compared to the desired value and the difference, or current error, is amplified and compared to the buck or the boost sawtooth ramp. Depending on which of the two ramps the Gmc amplified output crosses either the Buck MOSFETs or the Boost MOSFETs will be activated. When the input voltage is close to the output voltage, one buck cycle is always followed by a boost cycle. In this condition, no more than three cycles in a row of the same mode are allowed. This control method in the buck-boost region ensures a robust control and the highest efficiency.

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Feature Description (continued)

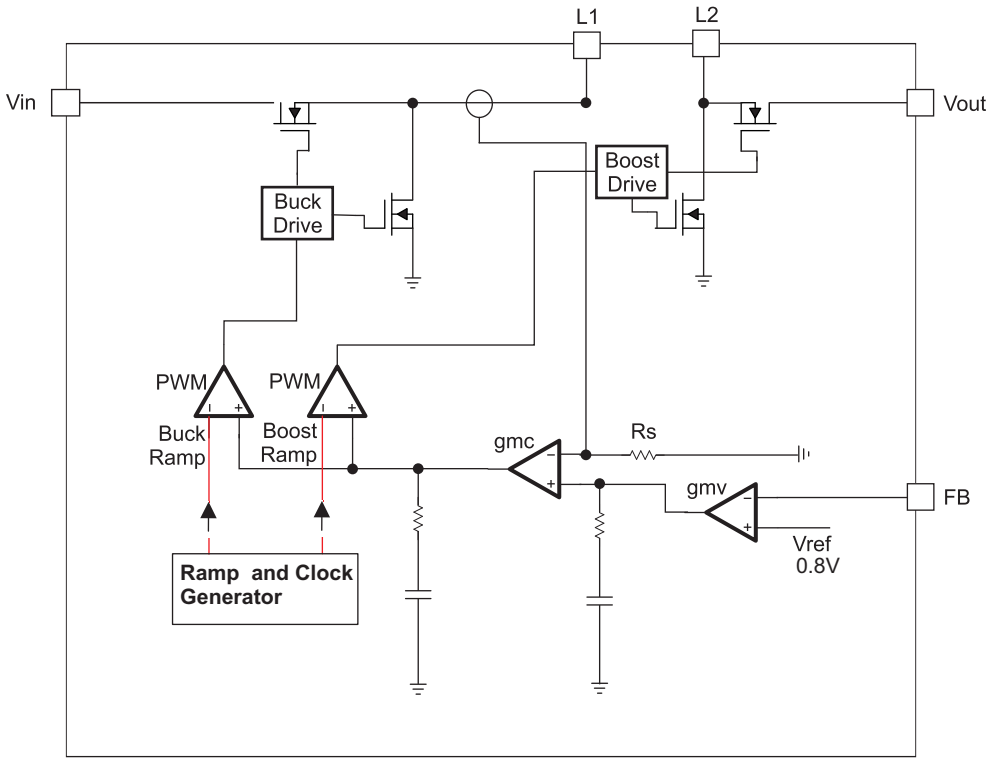


Figure 12. Average Current Mode Control

9.3.2 Device Enable

The device is put into operation when the EN pin is set high. It is put into shutdown mode when the EN pin is set low. In shutdown mode, the regulator stops switching, all internal control circuitry is switched off, and the load is disconnected from the input. This means that during shutdown, the output voltage can drop below the input voltage.

9.3.3 Output Discharge Function

When the device is disabled by pulling enable low and the supply voltage is still applied, a transistor is turned on, and discharge the output capacitor. This means, if there is no supply voltage applied the output discharge function is also disabled. The transistor which is responsible of the discharge function, when turned on, operates like an equivalent 120Ω resistor, ensuring typically less than 10ms discharge time for 20uF output capacitance and a 3.3V output.

9.3.4 Soft Start

To minimize inrush current and output voltage overshoot during start up, the device implements a soft start.

At turn on, the input current raises in a controlled manner until the output voltage reaches regulation.

During soft-start, the input current follows the current used to charge an internal soft start capacitor, this creates a linear and controlled increase of Vout.

The soft start time, is measured as the time from when the EN pin is asserted to when the output voltage has reached 90% of it's nominal value. It is typically less than 1ms. There is typically a 100µs delay time from when the EN pin is asserted to when the device starts the switching activity.

The soft start time depends on the load current, the input voltage, and the output capacitor. The soft start time in boost mode is longer then the time in buck mode.

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Feature Description (continued)

Thanks to its innovative soft start circuit, the device smoothly ramps up the input current bringing the output voltage to its regulated value without overshoot, even if a large capacitor is connected at the output. This specific case is never confused with a short circuit condition. The inductor current is able to increase and always guarantee soft start unless a real short circuit is applied at the output.

9.3.5 Short Circuit Protection

The TPS63025 provides short circuit protection to protect itself and the application. When the output voltage does not increase above 1.2V, the device assumes a short circuit at the output and keeps the input current controlled to protect itself and the application. In short circuit, the input current limit is kept at 3A

9.3.6 Undervoltage Lockout

An undervoltage lockout function prevents device start-up if the supply voltage on VIN and VINA is lower than its threshold (see electrical characteristics table). When in operation, the device automatically enters shutdown mode if the voltage on VIN and VINA drops below the undervoltage lockout threshold. The device automatically restarts, if the input voltage recovers above the hysteresis amount.

9.3.7 Supply and Ground

The TPS63025 provides two input pins (VIN and VINA) and two ground pins (PGND and GND).

The VIN pin supplies the input power, while the VINA pin provides voltage for the control circuits. A similar approach is used for the ground pins. GND and PGND are used to avoid ground shift problems due to the high currents in the switches. The reference for all control functions is the GND pin. The power switches are connected to PGND. Both grounds must be connected on the PCB at only one point, ideally, close to the GND pin.

9.3.8 Overtemperature Protection

The device has a built-in temperature sensor which monitors the internal IC temperature. If the temperature exceeds the programmed threshold (see electrical characteristics table) the device stops operating. As soon as the IC temperature has decreased below the programmed threshold, it starts operating again. There is a built-in hysteresis to avoid unstable operation at IC temperatures at the overtemperature threshold.

9.3.9 Current Limit

The current limit varies depending on the difference between the input and output voltage. The maximum value of average input current is obtained at the highest difference.

Given the curves provided in Figure 1, it is possible to calculate the output current reached in boost mode, using Equation 1 and Equation 2 and in buck mode using Equation 3 and Equation 4.

$$\text{Duty Cycle Boost} \quad D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{1}$$

$$\text{Output Current Boost} \quad I_{OUT} = \eta \times I_{IN} (1-D) \tag{2}$$

$$\text{Duty Cycle Buck} \quad D = \frac{V_{OUT}}{V_{IN}} \tag{3}$$

$$\text{Output Current Buck} \quad I_{OUT} = (\eta \times I_{IN}) / D \tag{4}$$

With,

η = Estimated converter efficiency (use the number from the efficiency curves or 0.90 as an assumption)
I_{IN}=Minimum average input current (Figure 1)

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9.4 Device Functional Modes

9.4.1 Power Save Mode Operation

Depending on the load current, in order to provide the best efficiency over the complete load range, the device works in PWM mode at load currents of approximately 350mA or higher. At lighter loads, the device switches automatically into Power Save Mode to reduce power consumption and extend battery life. The PFM/PWM pin is used to select between the two different operation modes. To enable Power Save Mode, the PFM/PWM pin must be set low.

During Power Save Mode, the part operates with a reduced switching frequency and lowest supply current to maintain high efficiency. The output voltage is monitored with a comparator at every clock cycle by the thresholds comp low and comp high. When the device enters Power Save Mode, the converter stops operating and the output voltage drops. The slope of the output voltage depends on the load and the output capacitance. When the output voltage reaches the comp low threshold, at the next clock cycle the device ramps up the output voltage again, by starting operation. Operation can last for one or several pulses until the comp high threshold is reached. At the next clock cycle, if the load is still lower than about 350mA, the device switches off again and the same operation is repeated. Instead, if at the next clock cycle, the load is above 350mA, the device automatically switches to PWM mode.

In order to keep high efficiency in PFM mode, there is only a comparator active to keep the output voltage regulated. The AC ripple in this condition is increased, compared to the PWM mode. The amplitude of this voltage ripple in the worst case scenario is 50mV pk-pk, (typically 30mV pk-pk), with 20µF effective output capacitance. In order to avoid a critical voltage drop when switching from 0A to full load, the output voltage in PFM mode is typically 1.3% above the nominal value in PWM mode. Dynamic Voltage Positioning allows the converter to operate with a small output capacitor and still have a low absolute voltage drop during heavy load transients.

Power Save Mode is disabled by setting the PFM/PWM pin high.

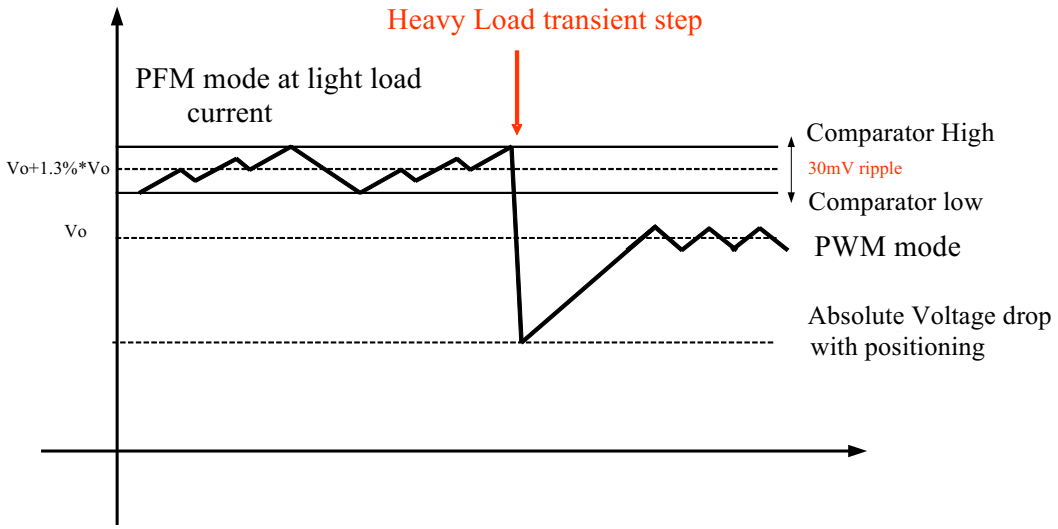


Figure 13. Power Save Mode Operation

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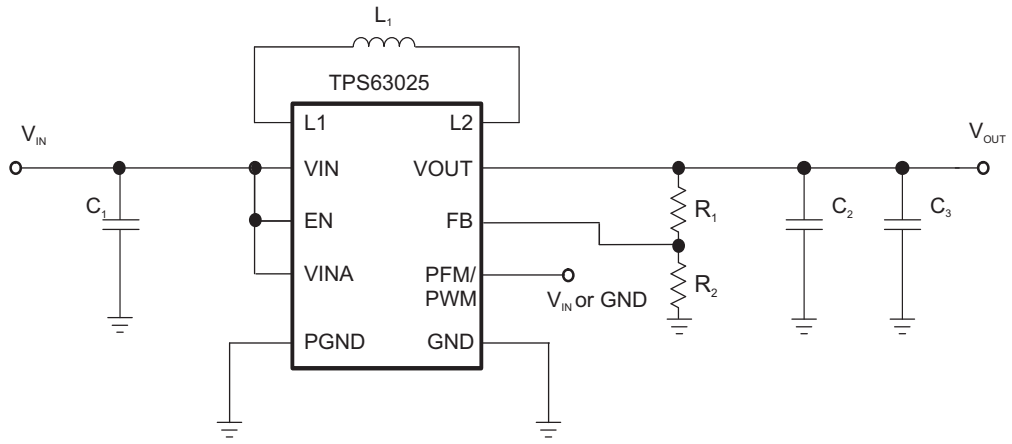
10 Application and Implementation

10.1 Application Information

The devices are designed to operate from an input voltage supply range between 2.3V and 5.5V with a maximum output current of 2A. The TPS63025 device operates in PWM mode for medium to heavy load conditions and in power save mode at light load currents.

In PWM mode the TPS63025 converter operates with the nominal switching frequency of 2.5MHz. As the load current decreases, the converter enters power save mode, reducing the switching frequency and minimizing the IC quiescent current to achieve high efficiency over the entire load range.

10.2 Typical Application



10.2.1 Design Requirements

The TPS63025 series of buck-boost converter has internal loop compensation. Therefore, the external LC filter has to be selected according to the internal compensation. Nevertheless, it's important to consider, that the effective inductance, due to inductor tolerance and current derating can vary between +20% and -30%. The same for the capacitance of the output filter: the effective capacitance can vary between +20% and -50% of the specified datasheet value, due to capacitor tolerance and bias voltage. For this reason Table 3 shows the capacitance and inductance value allowed

10.2.2 Detailed Design Procedure

Table 2. List Of Components(1)

REFERENCE	DESCRIPTION	MANUFACTURER
	TPS63025	Texas Instruments
L1	Shielded, Composite, 1µH, 8.75A, 13mΩ,SMD	XAL4020-102MEB, Colicraft
C1,C2	10 µF 6.3V, 0603, X5R ceramic	GRM188R60J106ME84D, Murata
C3	CAP, CERM,47uF, 6.3V, +/-20%, X5R,0805	GRM219R60J476ME44D, Murata
R1	Depending on the output voltage at adjustable output voltage version, 0 Ω at fixed 3.3V or 2.9V	
R2	Depending on the output voltage at adjustable output voltage version, not used at fixed 3.3V or 2.9V	

(1) See *Third-Party Products Disclaimer*

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10.2.2.1 Output Filter Design

Table 3. Matrix of Output Capacitor and Inductor Combinations

NOMINAL INDUCTOR VALUE [µH](1)	NOMINAL OUTPUT CAPACITOR VALUE [µF](2)				
	44	47	66	88	100
0.680			+	+	+
1.0	+(3)	+	+	+	+
1.5			+	+	+

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by 20% and –30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by 20% and –50%.
(3) Typical application. Other check mark indicates recommended filter combinations

10.2.2.2 Inductor Selection

For high efficiencies, the inductor should have a low dc resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a high impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. To avoid saturation of the inductor, the peak current for the inductor in steady state operation is calculated using Equation 1. Only the equation which defines the switch current in boost mode is shown, because this provides the highest value of current and represents the critical current value for selecting the right inductor.

$$\text{Duty Cycle Boost} \qquad D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{5}$$

$$I_{PEAK} = \frac{Iout}{\eta \times (1 - D)} + \frac{Vin \times D}{2 \times f \times L} \tag{6}$$

Where,

D =Duty Cycle in Boost mode
f = Converter switching frequency (typical 2.5MHz)
L = Inductor value
η = Estimated converter efficiency (use the number from the efficiency curves or 0.90 as an assumption)

Note: The calculation must be done for the minimum input voltage which is possible to have in boost mode

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. It's recommended to choose an inductor with a saturation current 20% higher than the value calculated using Equation 6. The following inductors are recommended for use:

The inductor value also affects the stability of the feedback loop. In particular the boost transfer function exhibits a right half-plane zero, whose frequency is inverse proportional to the inductor value and the load current. This means as the inductance and load current increase, the right half plane zero decreases in frequency. This could degrade the phase margin of the feedback loop. It is recommended to choose the inductor's value in order to have the frequency of the right half plane zero >300kHz. The frequency of the RHPZ can be calculated using Equation 7.

$$f_{RHPZ} = \frac{(1 - D)^2 \times Vout}{2\pi \times Iout \times L} \tag{7}$$

With,

D =Duty Cycle in Boost mode

Note: The calculation must be done for the minimum input voltage which is possible to have in boost mode

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Table 4. List of Recommended Inductors(1)

INDUCTOR VALUE	COMPONENT SUPLIER	SIZE (LxWxH mm)	Isat/DCR
1 µH	Coilcraft XAL4020-102ME	4 X 4 X 2.10	4.5A/10mΩ
1 µH	Toko, DFE322512C	3.2 X 2.5 X 1.2	4.7A/34mΩ
1 µH	TDK, SPM4012	4.4 X 4.1 X 1.2	4.1A/38mΩ
1 µH	Wuerth, 74438334010	3 X 3 X 1.2	6.6A/42.10mΩ
0.6 µH	Coilcraft XFL4012-601ME	4 X 4 X 1.2	5A/17.40mΩ
0.68µH	Wuerth,744383340068	3 X 3 X 1.2	7.7A/36mΩ

(1) See *Third-Party Products Desclaimer*

10.2.2.3 Capacitor Selection

10.2.2.3.1 *Input Capacitor*

At least a 10µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. An X5R or X7R ceramic capacitor placed as close as possible to the VIN and PGND pins of the IC is recommended. This capacitance can be increased without limit.

10.2.2.3.2 *Output Capacitor*

For the output capacitor, use of a small ceramic capacitors placed as close as possible to the VOUT and PGND pins of the IC is recommended. The recommended nominal output capacitance value is 20µF with a variance as outlined in Table 4.

There is also no upper limit for the output capacitance value. Larger capacitors causes lower output voltage ripple as well as lower output voltage drop during load transients.

10.2.2.4 Setting The Output Voltage

When the adjustable output voltage version TPS630250 is used, the output voltage is set by an external resistor divider. The resistor divider must be connected between VOUT, FB and GND. When the output voltage is regulated properly, the typical value of the voltage at the FB pin is 800mV. The current through the resistive divider should be about 10 times greater than the current into the FB pin. The typical current into the FB pin is 0.1µA, and the voltage across the resistor between FB and GND, R_2, is typically 800 mV. Based on these two values, the recommended value for R2 should be lower than 180kΩ, in order to set the divider current at 4µA or higher. It is recommended to keep the value for this resistor in the range of 180kΩ. From that, the value of the resistor connected between VOUT and FB, R1, depending on the needed output voltage (V_{OUT}), can be calculated using Equation 8:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (8)$$

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10.2.3 Application Curves

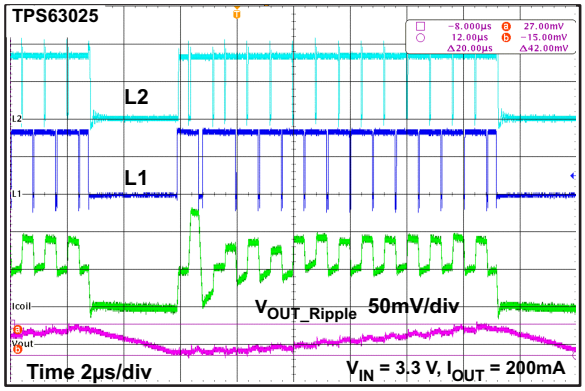


Figure 14. Output Voltage Ripple in Buck-Boost Mode and PFM to PWM Transition

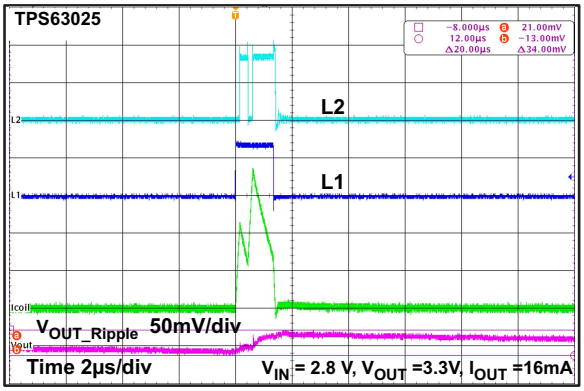


Figure 15. Output Voltage Ripple in Boost Mode and PFM Operation

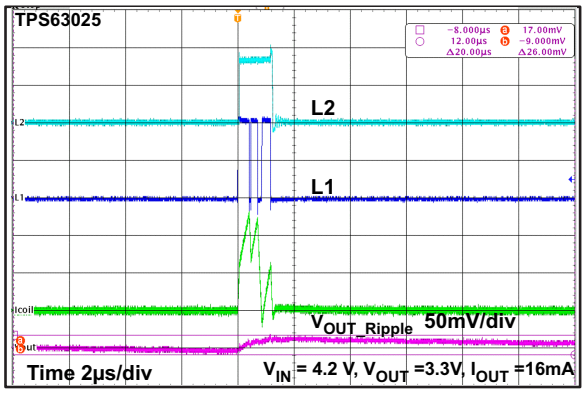


Figure 16. Output Voltage Ripple in Buck Mode and PFM Operation

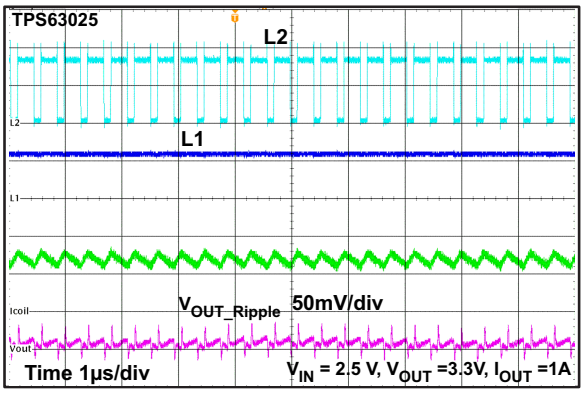


Figure 17. Switching Waveforms in Boost Mode and PWM Operation

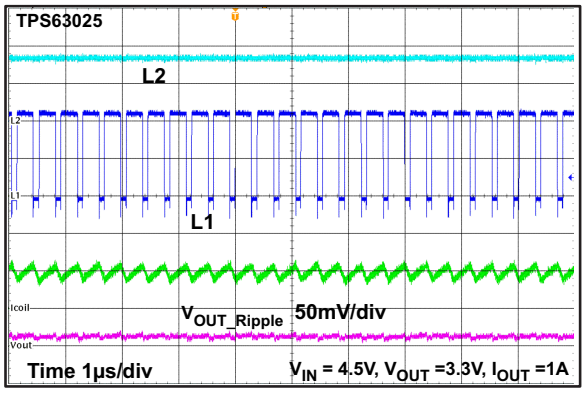


Figure 18. Switching Waveforms in Buck Mode and PWM Operation

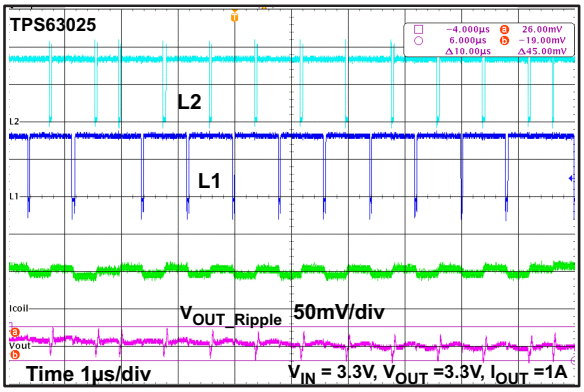


Figure 19. Switching Waveforms in Buck-Boost Mode and PWM Operation

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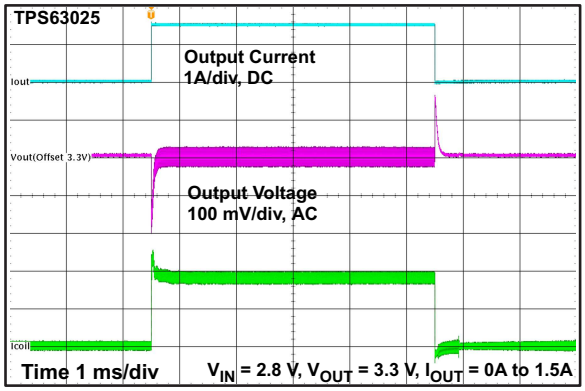


Figure 20. Load Transient Response Boost Mode

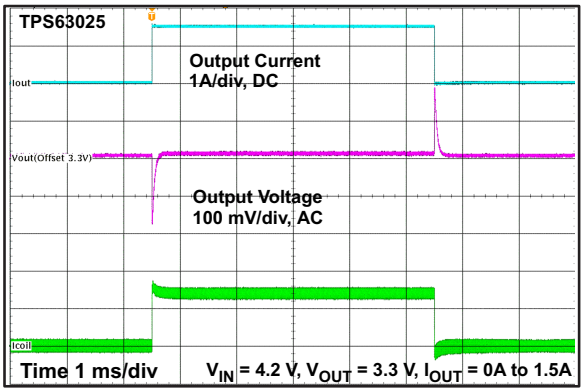


Figure 21. Load Transient Response Buck Mode

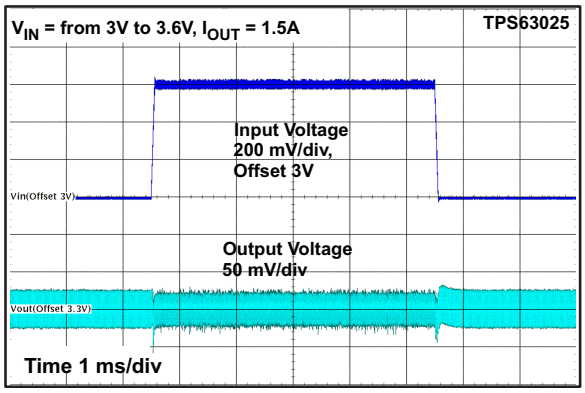


Figure 22. Line Transient Response

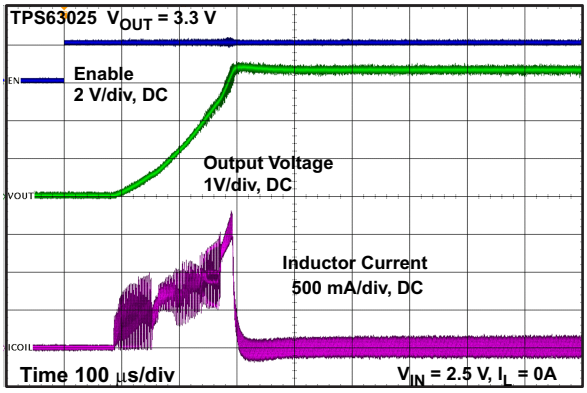


Figure 23. Start Up After Enable

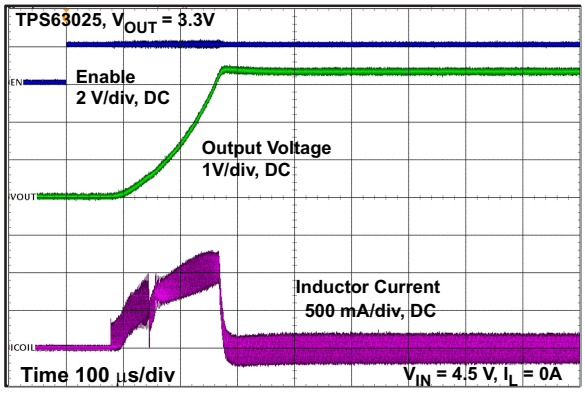


Figure 24. Start Up After Enable

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11 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.3V and 5.5 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS63025 converter additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

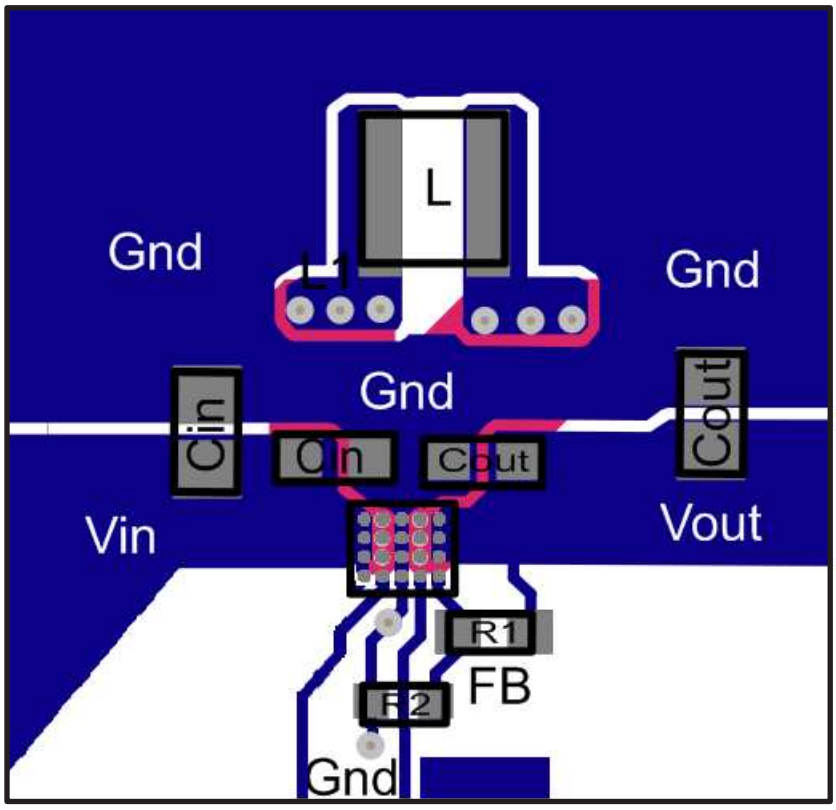
12 Layout

12.1 Layout Guidelines

The PCB layout is an important step to maintain the high performance of the TPS63025 devices.

- Place input and output capacitors, along with the inductor, as close as possible to the IC which keeps the traces short. Routing these traces direct and wide results in low trace resistance and low parasitic inductance.
- Use a common-power GND.
- Properly connect the low side of the input and output capacitors to the power GND to avoid a GND potential shift.
- The sense trace connected to FB is signal trace. Keep these trace away from L1 and L2 nodes.
- Use care to avoid noise induction. By a direct routing, parasitic inductance can be kept small.
- Use GND layers for shielding if needed.

12.2 Layout Example



12.3 Thermal Information

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

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Thermal Information (continued)

Two basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: *Thermal Characteristics Application Note* (SZZA017), and *IC Package Thermal Metrics Application Note* (SPRA953).

13 器件和文档支持

13.1 器件支持

13.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

13.2 文档支持

13.2.1 相关文档

相关文档如下：

《TPS63025EVM-553 用户指南，TPS63025 高电流、高效率单电感器降压-升压转换器》，SLVUA24

13.3 相关链接

以下表格列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，以及样片或购买的快速访问。

Table 5. 相关链接

部件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS630250	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS630251	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS630252	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

13.4 Trademarks

All trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

14 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS630250RNCR	Active	Production	VQFN-HR (RNC) | 14	3000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	63025P
TPS630250RNCR.A	Active	Production	VQFN-HR (RNC) | 14	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	63025P
TPS630250RNCT	Active	Production	VQFN-HR (RNC) | 14	250 | SMALL T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	63025P
TPS630250RNCT.A	Active	Production	VQFN-HR (RNC) | 14	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	63025P
TPS630250YFFR	Active	Production	DSBGA (YFF) | 20	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS 630250
TPS630250YFFR.A	Active	Production	DSBGA (YFF) | 20	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS 630250
TPS630250YFFT	Active	Production	DSBGA (YFF) | 20	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS 630250
TPS630250YFFT.A	Active	Production	DSBGA (YFF) | 20	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS 630250
TPS630251YFFR	Active	Production	DSBGA (YFF) | 20	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS 630251
TPS630251YFFR.A	Active	Production	DSBGA (YFF) | 20	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS 630251
TPS630251YFFT	Active	Production	DSBGA (YFF) | 20	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS 630251
TPS630251YFFT.A	Active	Production	DSBGA (YFF) | 20	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS 630251
TPS630252YFFR	Active	Production	DSBGA (YFF) | 20	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS 630252
TPS630252YFFR.A	Active	Production	DSBGA (YFF) | 20	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS 630252
TPS630252YFFT	Active	Production	DSBGA (YFF) | 20	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS 630252
TPS630252YFFT.A	Active	Production	DSBGA (YFF) | 20	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS 630252

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

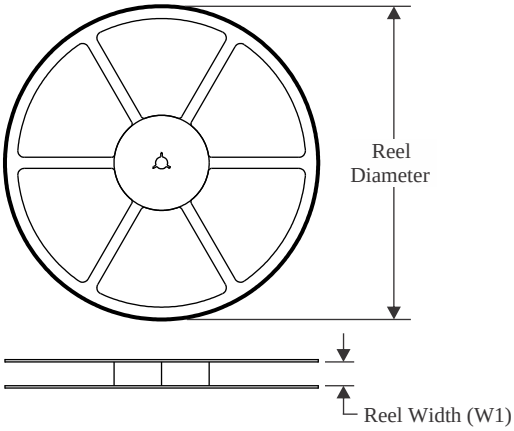
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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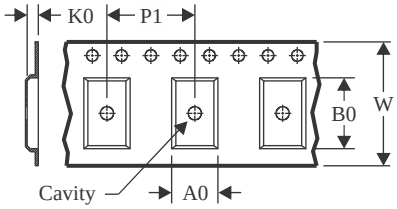
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

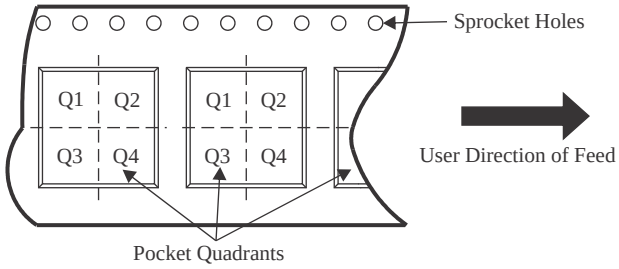


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

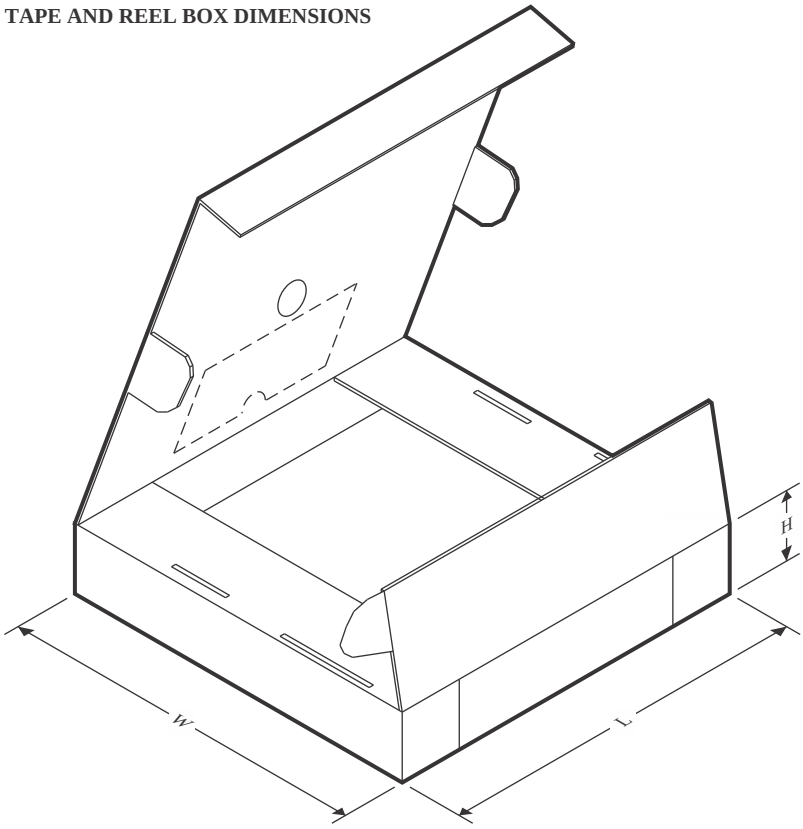
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS630250RNCT	VQFN-HR	RNC	14	250	180.0	12.4	2.8	3.3	1.2	8.0	12.0	Q1
TPS630250YFFR	DSBGA	YFF	20	3000	180.0	8.4	1.89	2.2	0.69	4.0	8.0	Q1
TPS630250YFFT	DSBGA	YFF	20	250	180.0	8.4	1.89	2.2	0.69	4.0	8.0	Q1
TPS630251YFFR	DSBGA	YFF	20	3000	180.0	8.4	1.89	2.2	0.69	4.0	8.0	Q1
TPS630251YFFT	DSBGA	YFF	20	250	180.0	8.4	1.89	2.2	0.69	4.0	8.0	Q1
TPS630252YFFR	DSBGA	YFF	20	3000	180.0	8.4	1.89	2.2	0.69	4.0	8.0	Q1
TPS630252YFFT	DSBGA	YFF	20	250	180.0	8.4	1.89	2.2	0.69	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

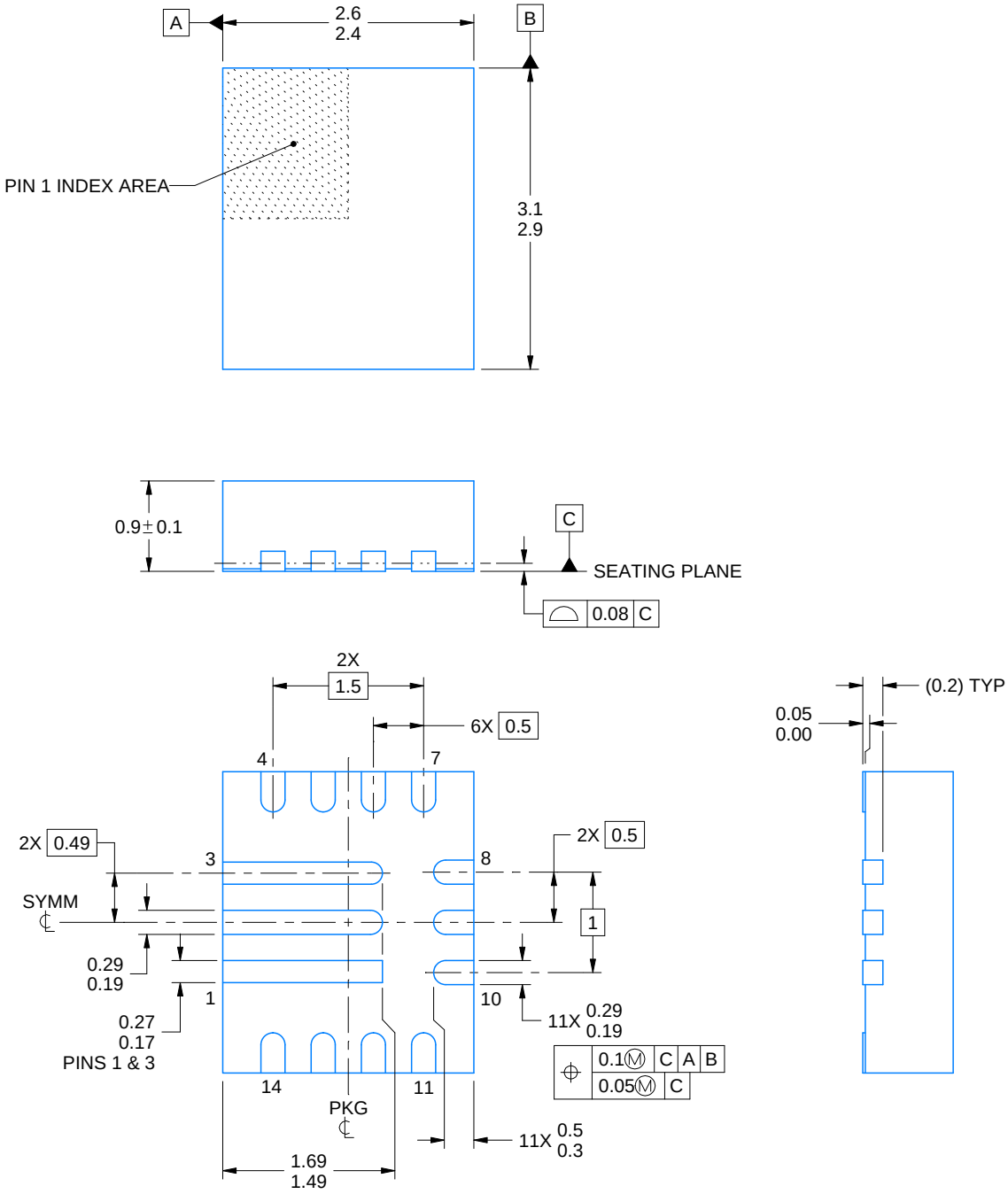
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS630250RNCT	VQFN-HR	RNC	14	250	341.0	182.0	80.0
TPS630250YFFR	DSBGA	YFF	20	3000	182.0	182.0	20.0
TPS630250YFFT	DSBGA	YFF	20	250	182.0	182.0	20.0
TPS630251YFFR	DSBGA	YFF	20	3000	182.0	182.0	20.0
TPS630251YFFT	DSBGA	YFF	20	250	182.0	182.0	20.0
TPS630252YFFR	DSBGA	YFF	20	3000	182.0	182.0	20.0
TPS630252YFFT	DSBGA	YFF	20	250	182.0	182.0	20.0

PACKAGE OUTLINE

RNC0014A

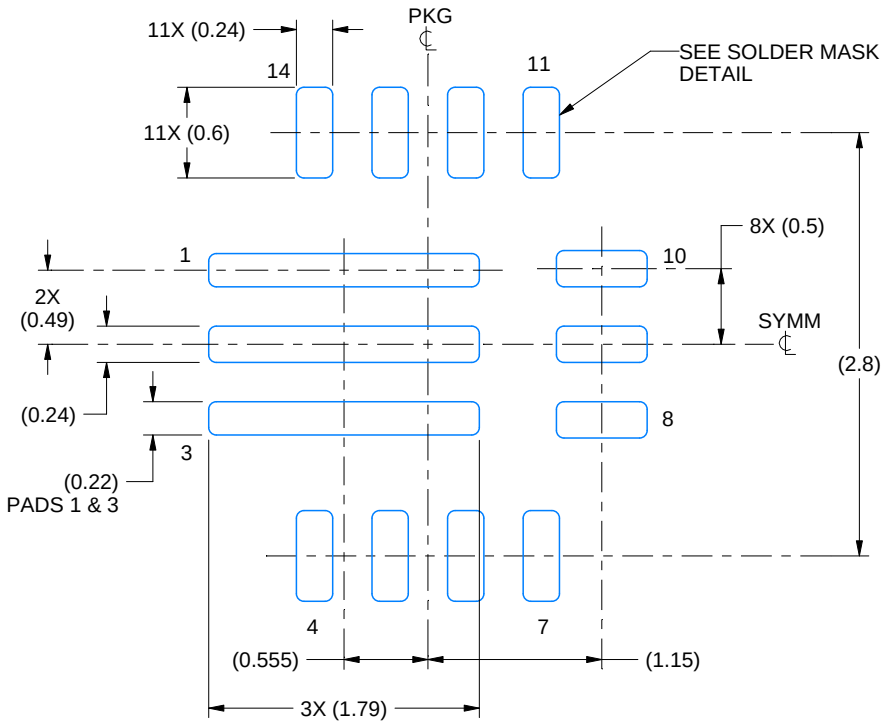
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

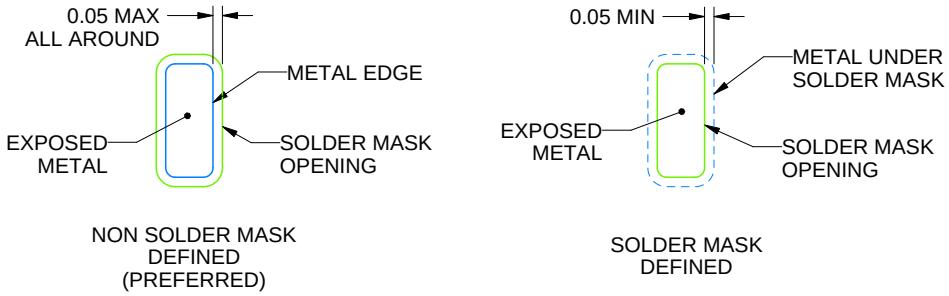


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

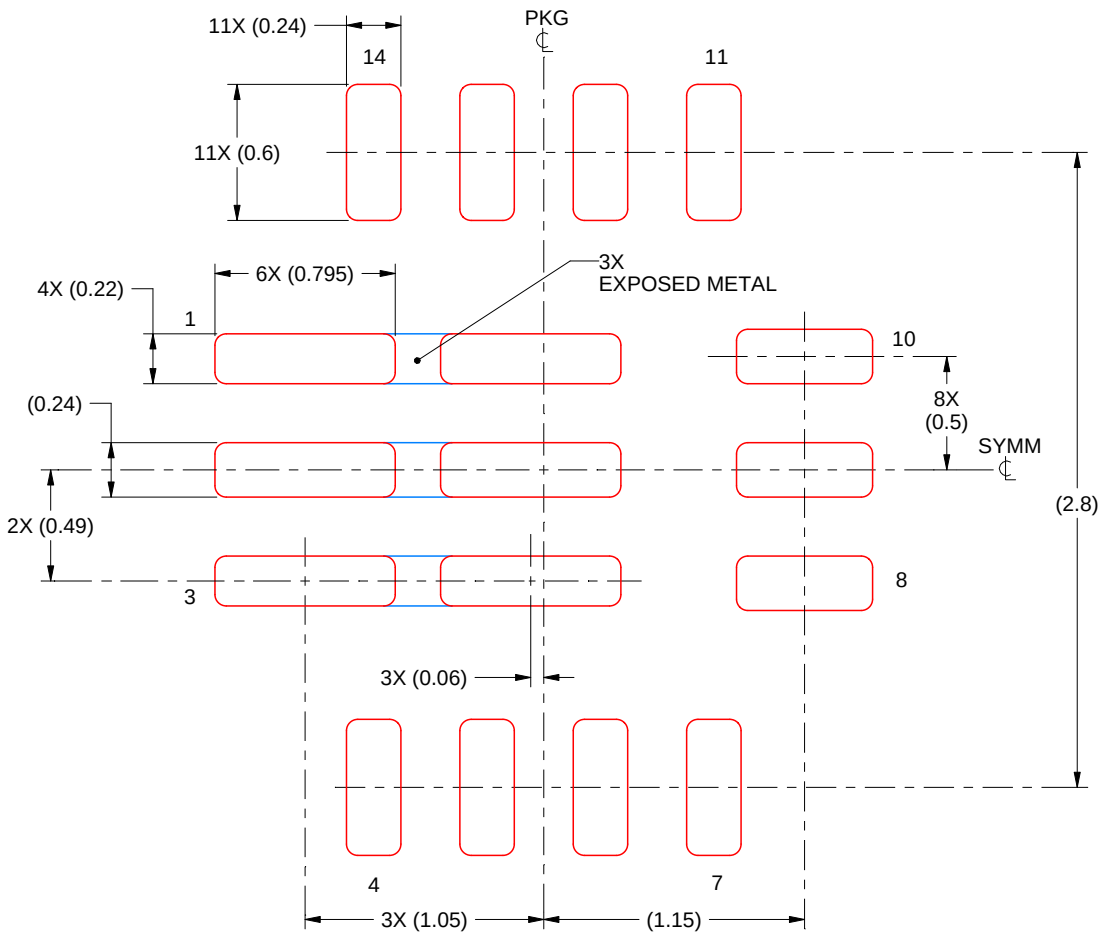


SOLDER MASK DETAILS

4221630/C 04/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

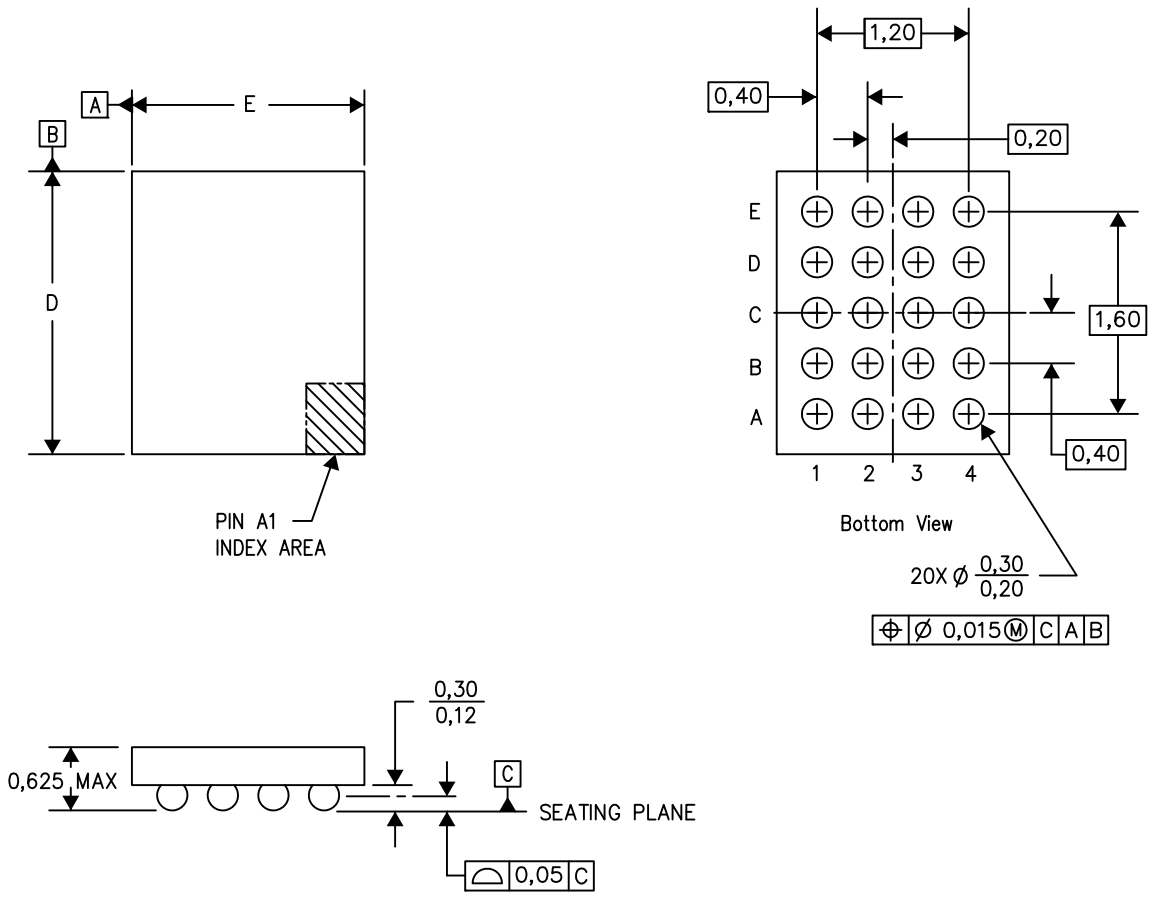
FOR EXPOSED PADS 1-3
89% PRINTED SOLDER COVERAGE BY AREA
SCALE:30X

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NOTES: (continued)

5. For alternate stencil design recommendations, see IPC-7525 or board assembly site preference.

YFF (R–XBGA–N20) DIE–SIZE BALL GRID ARRAY



D: Max = 2.116 mm, Min =2.056 mm

E: Max = 1.796 mm, Min =1.736 mm

4207625–9/AO 12/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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