TPS62A01, TPS62A01A, TPS62A02, TPS62A02A, TPS62A02N, TPS62A02NA
ZHCSN71E – DECEMBER 2021 – REVISED JUNE 2024

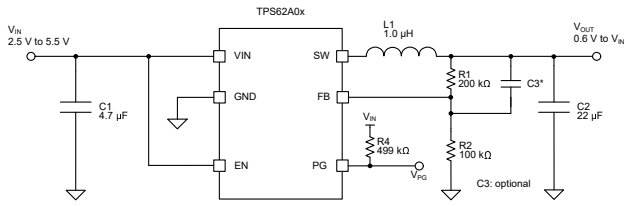
TPS62A0x、TPS62A0xA 和 TPS62A02Nx 采用 SOT-563 和 SOT-23 封装的 1A 和 2A 高效同步降压转换器

1 特性

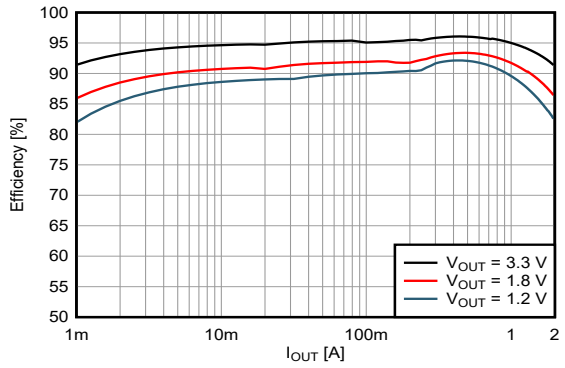
- 输入电压范围为 2.5V 至 5.5V
- 0.6V 至 V_{IN} 可调节输出电压范围
- 180mΩ/120mΩ 低 R_{DSON} 开关 (1A DRL)
- 100mΩ/67mΩ 低 R_{DSON} 开关（1A DDC，2A）
- < 23μA 静态电流
- 1% 反馈精度（0°C 至 125°C）
- 100% 模式运行
- 2.4MHz 开关频率
- 支持节电模式或 PWM 选项
- 电源正常状态输出引脚（可选）
- 短路保护 (HICCUP)
- 内部软启动
- 有源输出放电
- 热关断保护
- 与 TLV62585 (DRL) 引脚对引脚兼容
- 与 TLV62569 (DDC) 引脚对引脚兼容

2 应用

- 机顶盒、电视应用
- IP 网络摄像头、多功能打印机
- 无线路由器、固态硬盘
- 电池供电的应用
- 通用负载点电源



典型应用



效率与输出电流间的关系曲线（电压为 $5V_{IN}$ 时）
(TPS62A02x)

3 说明

TPS62A0x 系列器件是同步直流/直流降压转换器，经过优化可实现高效率和紧凑型设计尺寸。此器件集成了能够传送高达 2A 输出电流的开关。在中等负载至重负载条件下，该器件在脉宽调制 (PWM) 模式下以 2.4MHz 开关频率运行。在轻载情况下，这些器件自动进入节能模式 (PSM)，从而在整个负载电流范围内保持高效率。关断时，电流消耗量也最低。该器件系列的 TPS62A0xA 型号在整个负载电流范围内以强制 PWM 模式运行。

TPS62A0x 器件通过一个外部电阻分压器提供可调节输出电压。内部软启动电路可限制启动期间的浪涌电流。内置的其他特性包括过流保护、热关断保护和电源正常指示（可选）。这些器件采用 SOT563 和 SOT23-6 封装。

封装信息

器件型号	封装(1)	封装尺寸(2)
TPS62A01x	DRL（SOT-563，6）	1.60mm × 1.60mm
	DDC（SOT-23，6）	2.90mm × 2.80mm
TPS62A02x	DRL（SOT-563，6）	1.60mm × 1.60mm
	DDC（SOT-23，6）	2.90mm × 2.80mm
TPS62A02Nx	DRL（SOT-563，6）	1.60mm × 1.60mm

(1) 有关更多信息，请参阅节 11。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。

器件信息

器件型号(1)	运行模式	输出电流	引脚 6
TPS62A01	PSM、PWM	1A	PG
TPS62A01A	FPWM		
TPS62A02	PSM、PWM	2A	
TPS62A02A	FPWM		
TPS62A02N	PSM、PWM		OUT
TPS62A02NA	FPWM		

(1) 请参阅*器件比较表*。

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4 Device Comparison Table

Device Number	Output Current	Package	Operation Mode	Pin 6
TPS62A01DRLR	1A	SOT-563, 6	PSM, PWM	PG
TPS62A01ADRLR			FPWM	
TPS62A02DRLR	2A		PSM, PWM	
TPS62A02ADRLR			FPWM	
TPS62A02NDRLR			PSM, PWM	OUT
TPS62A02NADRLR			FPWM	
TPS62A01PDDCR	1A	SOT-23, 6	PSM, PWM	PG
TPS62A01APDDCR			FPWM	
TPS62A02PDDCR	2A		PSM, PWM	
TPS62A02APDDCR			FPWM	

5 Pin Configuration and Functions

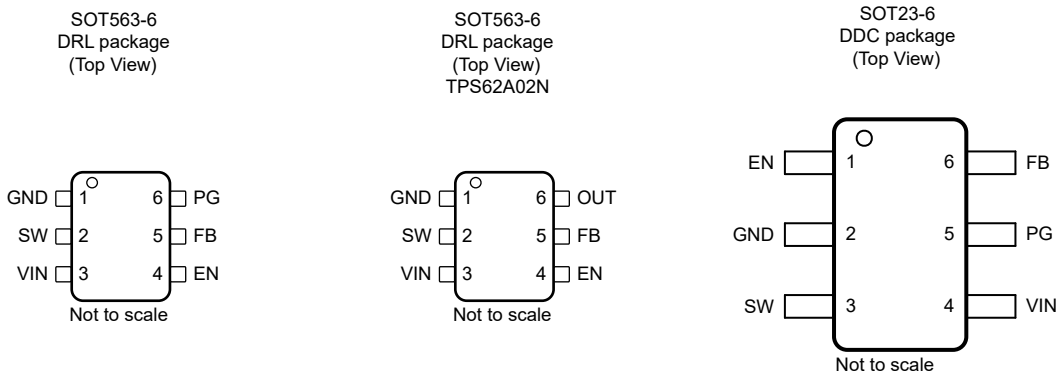


图 5-1. 6-Pin DRL SOT-563 Package (Top View), 6-Pin DDC SOT-23 Package (Top View)

表 5-1. Pin Functions

Pin Number			Type(1)	Description
Name	SOT563-6	SOT23-6		
EN	4	1	I	Device enable logic input. Logic high enables the device. Logic low disables the device and turns the device into shutdown. Do not leave the pin floating.
FB	5	6	I	Feedback pin for the internal control loop. Connect this pin to an external feedback divider.
GND	1	2	G	Ground pin.
PG	6	5	O	Power-good open-drain output pin. The pullup resistor cannot be connected to any voltage higher than 5.5V. If unused, leave the pin open or connect to GND.
OUT(2)		/	I	Output voltage sense pin.
SW	2	3	O	Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter to this pin.
VIN	3	4	I	Input voltage pin. Connect the input capacitor as close as possible between V_{IN} and GND.

(1) I = Input, O = Output, G = Ground.
(2) Only for TPS62A0x**N** versions.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage(2)	VIN, EN, PG	–0.3	6.5	V
	SW, DC	–0.3	V_{IN} + 0.3	V
	SW, transient < 10 ns	–3.0	10	V
	FB	–0.3	3	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range		2.5		5.5	V
V_{OUT}	Output voltage range		0.6		V_{IN}	V
I_{OUT}	Output current range	TPS62A01	0		1	A
I_{OUT}	Output current range (1)	TPS62A02	0		2	A
L	Effective inductance			1.0		µH
C_{OUT}	Output capacitance	V_{OUT} < 1.2 V		44		µF
C_{OUT}	Output capacitance	1.2 V ≤ V_{OUT} < 1.8 V		22		µF
C_{OUT}	Output capacitance	V_{OUT} ≥ 1.8 V		10		µF
I_{PG}	Power Good input current capability		0		1	mA
T_J	Operating junction temperature		–40		125	°C

(1) Operating continuously at 2-A with input voltages < 3.3V or at ambient temperatures > 85 °C might result in thermal shutdown, per EVM measurements.

6.4 Thermal Information

THERMAL METRIC(1)		TPS62A0x DRL 6 PINS	TPS62A0x DDC 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	157.3	132.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	92.2	74.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.6	45.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.0	25.5	°C/W

6.4 Thermal Information（续）

THERMAL METRIC[1]		TPS62A0x DRL 6 PINS	TPS62A0x DDC 6 PINS	UNIT
ψ_{JB}	Junction-to-board characterization parameter	45.0	45.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.

6.5 Electrical Characteristics

T_J = –40°C to +125°C, V_{IN} = 2.5 V to 5.5 V. Typical values are at T_J = 25°C and V_{IN} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{Q(VIN)}$	VIN quiescent current	Non-switching; V_{EN} = High; V_{FB} = 610 mV; TPS62A01xDRL		20		µA
$I_{Q(VIN)}$	VIN quiescent current	Non-switching; V_{EN} = High; V_{FB} = 610 mV; TPS62A01xDDC; TPS62A02		23		µA
$I_{SD(VIN)}$	VIN shutdown supply current	V_{EN} = Low		0.01	2	µA
UVLO						
$V_{UVLO(R)}$	VIN UVLO rising threshold	V_{IN} rising	2.3	2.4	2.5	V
$V_{UVLO(F)}$	VIN UVLO falling threshold	V_{IN} falling	2.2	2.3	2.4	V
ENABLE						
$V_{EN(R)}$	EN voltage rising threshold	EN rising; enable switching	1.2			V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching			0.4	V
$V_{EN(LKG)}$	EN Input leakage current	V_{EN} = 5 V			100	nA
REFERENCE VOLTAGE						
V_{FB}	FB voltage	T_J = 0°C to 125°C, PWM mode	594	600	606	mV
V_{FB}	FB voltage	PWM mode	591	600	609	mV
$I_{FB(LKG)}$	FB input leakage current	V_{FB} = 0.6 V			100	nA
SWITCHING FREQUENCY						
$f_{SW(FCCM)}$	Switching frequency, FPWM operation	V_{IN} = 5 V; V_{OUT} = 1.8 V		2400		kHz
STARTUP						
	Internal fixed soft-start time	From EN = High to V_{FB} = 0.56 V			1	ms
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	TPS62A01xDRL; V_{IN} = 5 V		180		mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	TPS62A01xDRL; V_{IN} = 5 V		120		mΩ
$R_{DSON(HS)}$	High-side MOSFET on-resistance	V_{IN} = 5 V; TPS62A01xDDC; TPS62A02		100		mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	V_{IN} = 5 V; TPS62A01xDDC; TPS62A02		67		mΩ
OVERCURRENT PROTECTION						
$I_{HS(OC)}$	High-side peak current limit	TPS62A01	1.3	1.8		A
$I_{LS(OC)}$	Low-side valley current limit	TPS62A01		1.8		A
$I_{HS(OC)}$	High-side peak current limit	TPS62A02	2.7	3.4		A
$I_{LS(OC)}$	Low-side valley current limit	TPS62A02xDRL		4.2		A
$I_{LS(OC)}$	Low-side valley current limit	TPS62A02xDDC		3.15		A
POWER GOOD						
V_{PGTH}	Power Good threshold	PG low, FB falling		93.5		%
V_{PGTH}	Power Good threshold	PG high, FB rising		96		%
	PG delay falling			35		µs
	PG delay rising			10		µs
$I_{PG(LKG)}$	PG pin Leakage current when open drain output is high	V_{PG} = 5 V			100	nA
	PG pin output low-level voltage	I_{PG} = 1 mA			400	mV

6.5 Electrical Characteristics（续）

T_J = –40°C to +125°C, V_{IN} = 2.5 V to 5.5 V. Typical values are at T_J = 25°C and V_{IN} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT DISCHARGE						
	Output discharge current on SW pin	V_{IN} = 3 V, V_{OUT} = 2.0 V; TPS62A01xDRL		60		mA
	Output discharge current on SW pin	V_{IN} = 3 V, V_{OUT} = 2.0 V; TPS62A01xDDC; TPS62A02		76		mA
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold	Temperature rising		170		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis			20		°C

6.6 Typical Characteristics

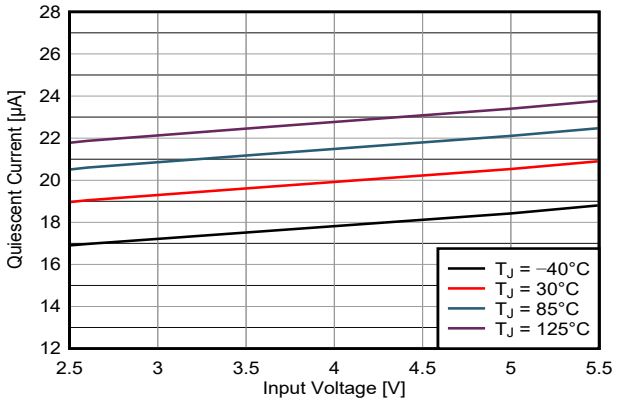


图 6-1. Quiescent Current vs Input Voltage (TPS62A01)

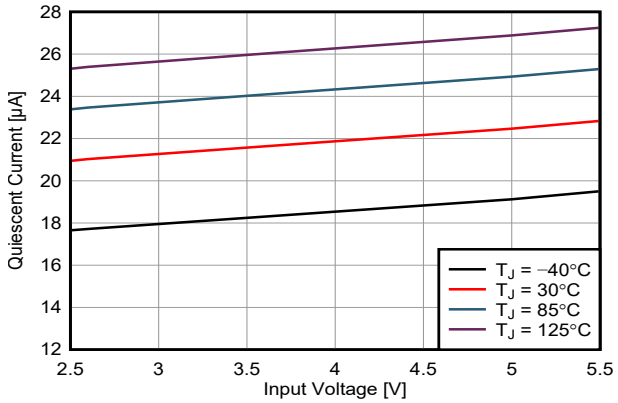


图 6-2. Quiescent Current vs Input Voltage (TPS62A02)

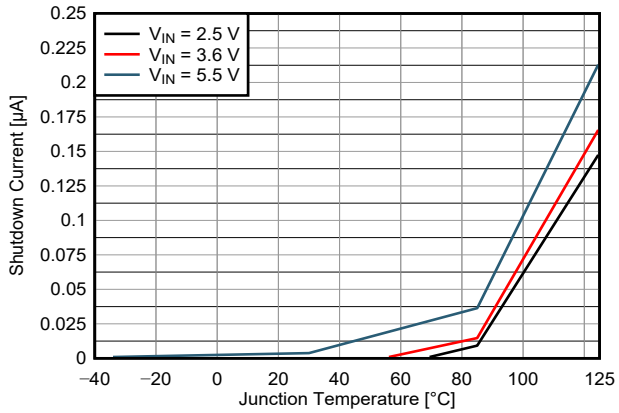


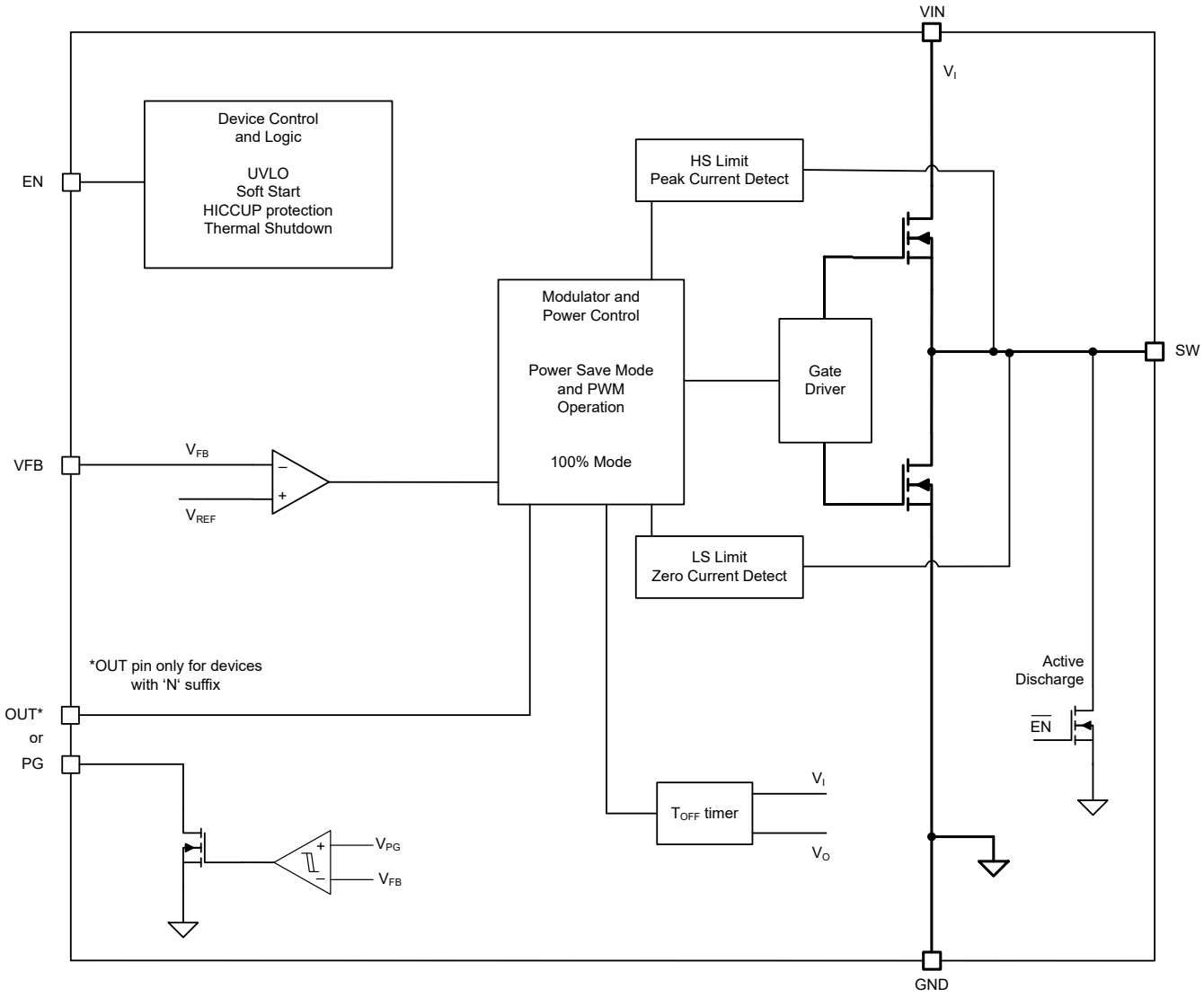
图 6-3. Shutdown Current vs Junction Temperature

7 Detailed Description

7.1 Overview

The TPS62A0x is a high-efficiency synchronous step-down converter. The device operates with an adaptive off time with a peak current control scheme. The device operates typically at 2.4MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. Based on the V_{IN}/V_{OUT} ratio, a simple circuit sets the required off time for the low-side MOSFET, making the switching frequency relatively constant regardless of the variation of the input voltage, output voltage, and load current.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Save Mode

The device automatically enters power save mode to improve efficiency at light load when the inductor current becomes discontinuous. In power save mode, the converter reduces the switching frequency and minimizes current consumption. In power save mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor or adding a feedforward capacitor.

7.3.2 100% Duty Cycle Low Dropout Operation

The device offers low input-to-output voltage difference by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. The minimum input voltage to maintain output regulation, depending on the load current and output voltage, is calculated as:

$$V_{IN(MIN)} = V_{OUT} + I_{OUT} \times (R_{DS(ON)} + R_L) \quad (1)$$

where

- $R_{DS(ON)}$ = High-side FET on-resistance
- R_L = Inductor ohmic resistance (DCR)

7.3.3 Soft Start

After enabling the device, internal soft-start circuitry ramps up the output voltage, which reaches the nominal output voltage during start-up time, avoiding excessive inrush current and creating a smooth voltage rise slope. Internal soft-start circuitry also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

The TPS62A0x is able to start into a prebiased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to the nominal value.

7.3.4 Switch Current Limit and Short-Circuit Protection (HICCUP)

The switch current limit prevents the device from high inductor current and drawing excessive current from the battery or input rail. Due to internal propagation delay, the AC peak current can exceed the static current limit during that time. Excessive current can occur with a shorted or saturated inductor, an overload or shorted output circuit condition. If the inductor current reaches the threshold I_{LIM}, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current with an adaptive off time.

When this switch current limit is triggered 32 times, the device stops switching to protect the output. The device then automatically starts a new start-up after a typical delay time of 100µs has passed. This is named HICCUP short-circuit protection. The device repeats this mode until the high load condition disappears. HICCUP protection is also enabled during the start-up.

7.3.5 Undervoltage Lockout

To avoid misoperation of the device at low input voltages, an undervoltage lockout (UVLO) is implemented, which shuts down the device at voltages lower than V_{UVLO}.

7.3.6 Thermal Shutdown

The device goes into thermal shutdown and stops switching when the junction temperature exceeds T_{JSD}. When the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically.

7.4 Device Functional Modes

7.4.1 Enable and Disable

The device is enabled by setting the EN input to a logic High. Accordingly, a logic Low disables the device. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the set point voltage. The EN input must be terminated and not be left floating.

7.4.2 Power Good

The TPS62A0x (except devices with 'N' suffix) has a built-in power-good (PG) feature to indicate whether the output voltage has reached the target and the device is ready. The PG signal can be used for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor to any voltage up to the recommended input voltage level. PG is low when the device is turned off due to EN, UVLO (undervoltage lockout), or thermal shutdown. VIN must remain present for the PG pin to stay low. If not used, the power-good

can be tie to GND or left open. The PG indicator has a de-glitch to avoid the signal indicating glitches or transient responses from the loop.

表 7-1. Power-Good indicator Functional Table

Logic Signals				PG Status
V_I	EN Pin	Thermal Shutdown	V_O	
V_I > UVLO	HIGH	NO	V_O on target	High Impedance
			V_O < target	LOW
			YES	LOW
		YES	x	LOW
	LOW	x	x	LOW
V_I < 1.8V	x	x	x	Undefined

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Application

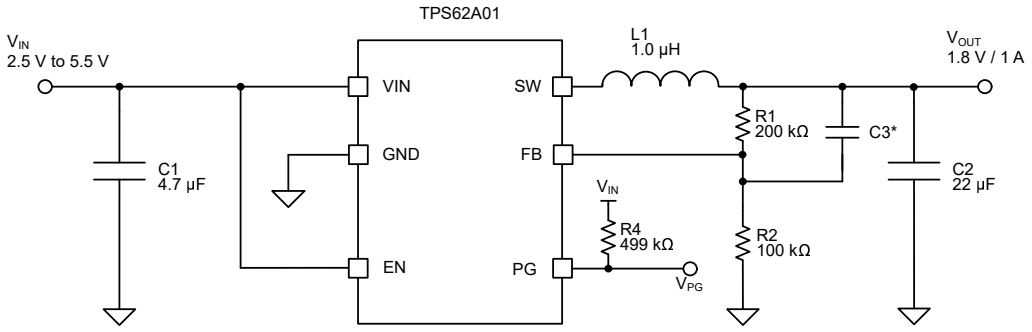


图 8-1. TPS62A01 Typical Application Circuit

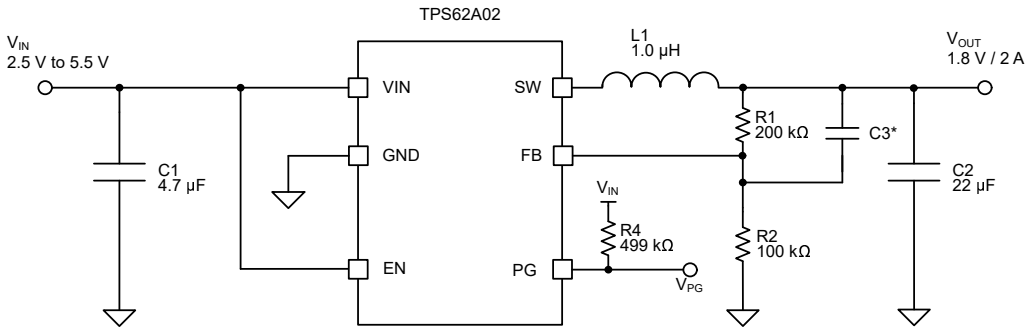


图 8-2. TPS62A02 Typical Application Circuit

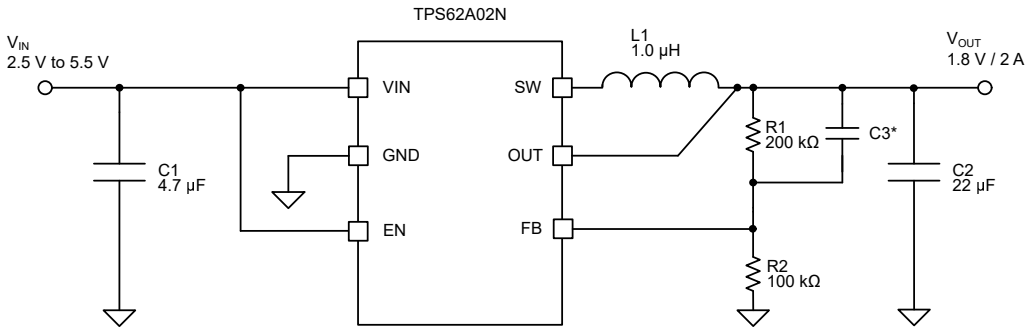


图 8-3. TPS62A02N Typical Application Circuit

*C3 is optional

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 as the input parameters

表 8-1. Design Parameters

Design Parameter	Example Value
Input voltage	2.5V to 5.5V
Output voltage	1.8V
Maximum output current	1.0A, 2.0A

表 8-2 lists the components used for the example.

表 8-2. List of Components

Reference	Description	Manufacturer(1)
C1	4.7µF, Ceramic Capacitor, 10V, X7R, size 0805, GRM21BR71A475KA73L	Murata
C2	22µF, Ceramic Capacitor, 10V, X7R, size 0805, GRM21BZ71A226KE15L	Murata
L1	1µH, Power Inductor, DFE252012F-1R0M (1A) / XGL3520-102MEC (2A)	Murata / Coilcraft
R1, R2	Chip resistor, 1%, size 0603	Std.
C3	Optional, 120pF if needed	Std.

(1) See the *Third-Party Products Disclaimer*.

8.2.2 Detailed Design Procedure

8.2.2.1 Setting the Output Voltage

The output voltage is set by an external resistor divider according to 方程式 2.

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R2 \times \left(\frac{V_{OUT}}{0.6\,V} - 1\right) \quad (2)$$

R2 must not be higher than 100kΩ to provide acceptable noise sensitivity.

8.2.2.2 Output Filter Design

The inductor and output capacitor together provide a low-pass filter. To simplify this process, 表 8-3 outlines possible inductor and capacitor value combinations. Checked cells represent combinations that are proven for stability by simulation and lab test. Check further combinations for each individual application.

表 8-3. Matrix of Output Capacitor and Inductor Combinations for TPS62A01 and TPS62A02

V_{OUT} [V]	L [µH](1)	C_{OUT} [µF](2)		
		10	22	2 × 22
0.6 ⩽ V_{OUT} < 1.2	1		+	++(3)
1.2 ⩽ V_{OUT} < 1.8			++(3)	+
1.8 ⩽ V_{OUT}		+(4)	++(3)	+

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and –30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by +20% and –50%.
(3) This LC combination is the standard value and recommended for most applications.
(4) The minimum C_{OUT} of 10µF does not support an additional feedforward capacitor.

A 0.47uH inductor can also be used with the same recommended output capacitors for the TPS62A02x. In case a lower output ripple is desired, higher output capacitance can help reduce the ripple.

8.2.2.3 Input and Output Capacitor Selection

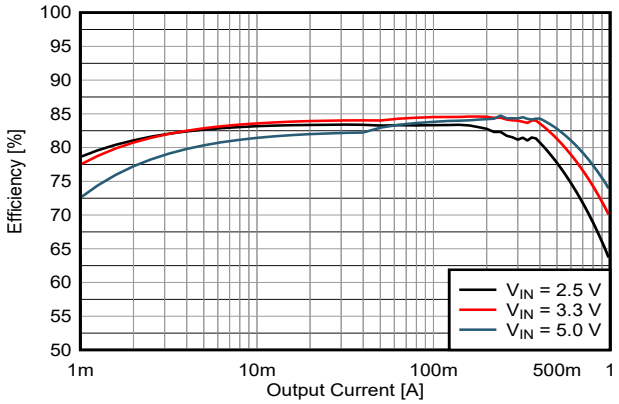
The architecture of the TPS62A0x allows use of tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are thus recommended. To keep resistance up to high frequencies and to achieve narrow capacitance variation with temperature, TI recommends to use X7R or X5R dielectric.

The input capacitor is the low impedance energy source for the converter that helps provide stable operation. TI recommends a low-ESR multilayer ceramic capacitor for best filtering. For most applications, a 4.7 µF input capacitor is sufficient; a larger value reduces input voltage ripple.

The TPS62A0x is designed to operate with an output capacitor of 10 µF to 47 µF, depending on the selected output voltage, as outlined in 表 8-3.

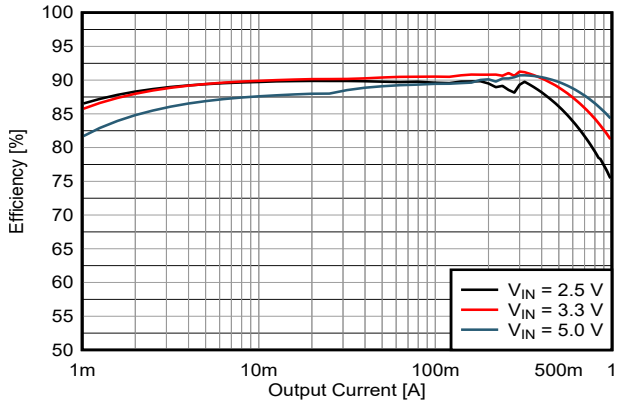
A feedforward capacitor reduces the output ripple in PSM and improves the load transient response. A 120pF capacitor is good for the 1.8V output typical application.

8.2.3 Application Curves



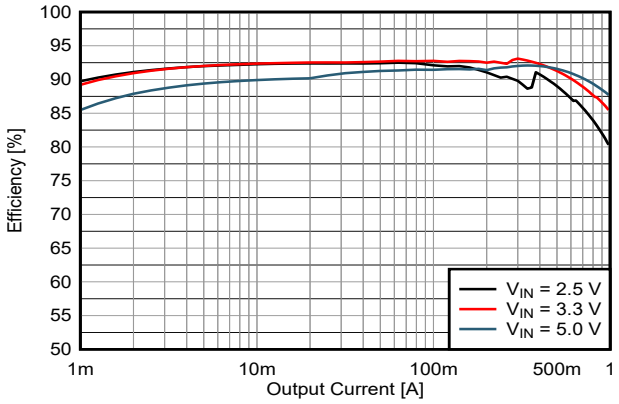
TPS62A01 (PSM/PWM) SOT-563 (DRL)

图 8-4. 0.6V Output Efficiency



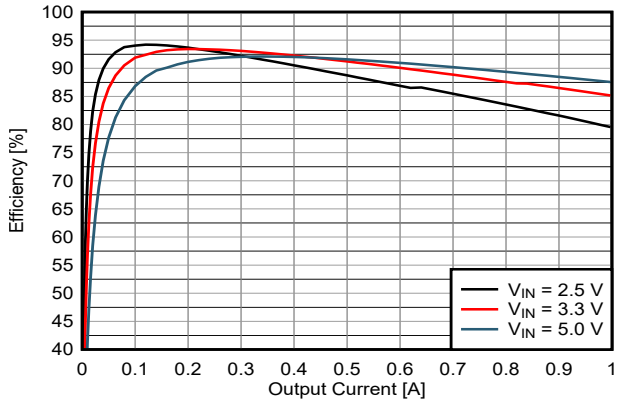
TPS62A01 (PSM/PWM) SOT-563 (DRL)

图 8-5. 1.2V Output Efficiency



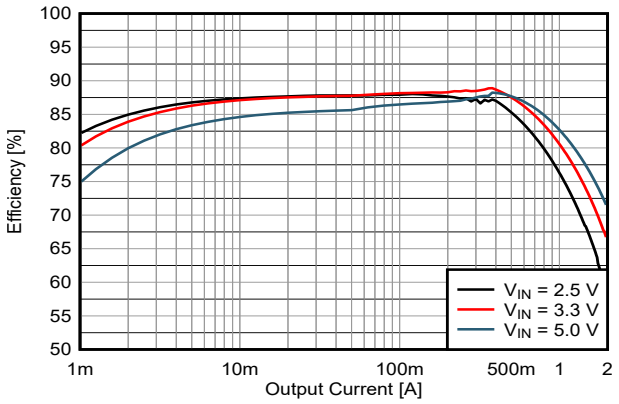
TPS62A01 (PSM/PWM) SOT-563 (DRL)

图 8-6. 1.8V Output Efficiency



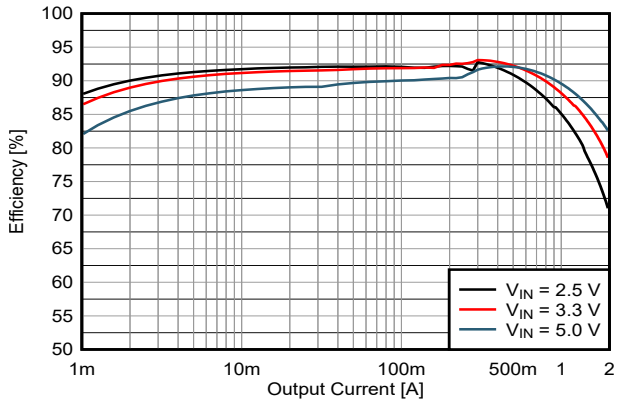
TPS62A01A (FPWM) SOT-563 (DRL)

图 8-7. 1.8V Output Efficiency



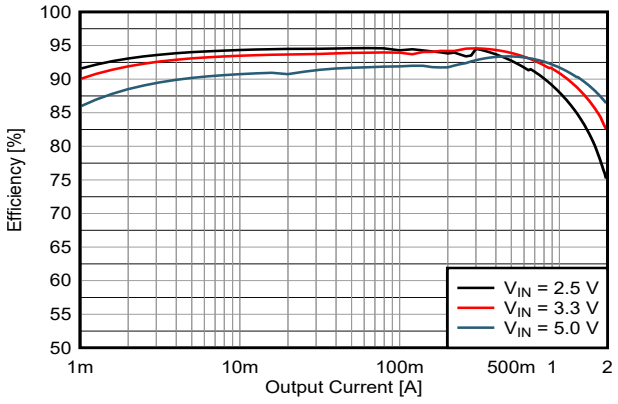
TPS62A02 (PSM/PWM) SOT-563 (DRL)

图 8-8. 0.6V Output Efficiency



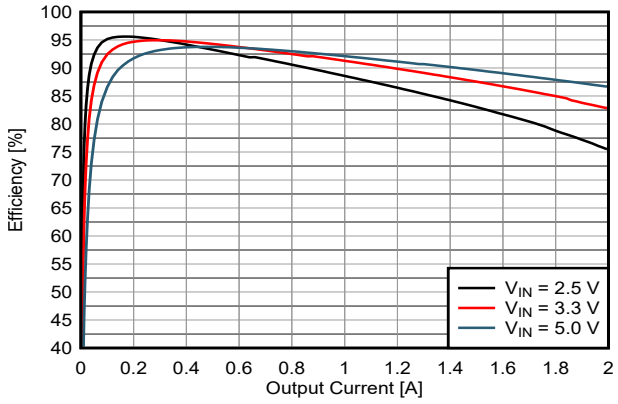
TPS62A02 (PSM/PWM) SOT-563 (DRL)

图 8-9. 1.2V Output Efficiency



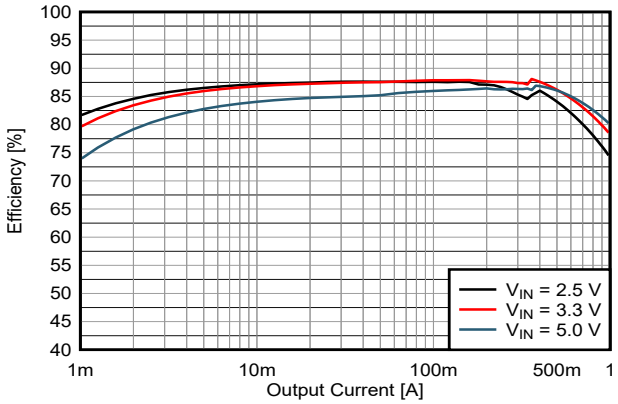
TPS62A02 (PSM/PWM) SOT-563 (DRL)

图 8-10. 1.8V Output Efficiency



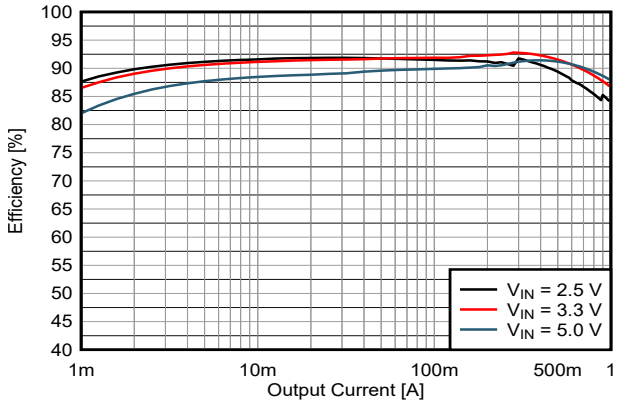
TPS62A02A (FPWM) SOT-563 (DRL)

图 8-11. 1.8V Output Efficiency



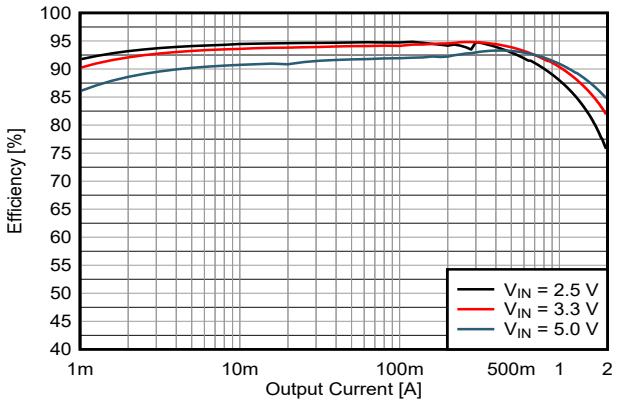
TPS62A01 (PSM/PWM) SOT-23 (DDC)

图 8-12. 0.6V Output Efficiency



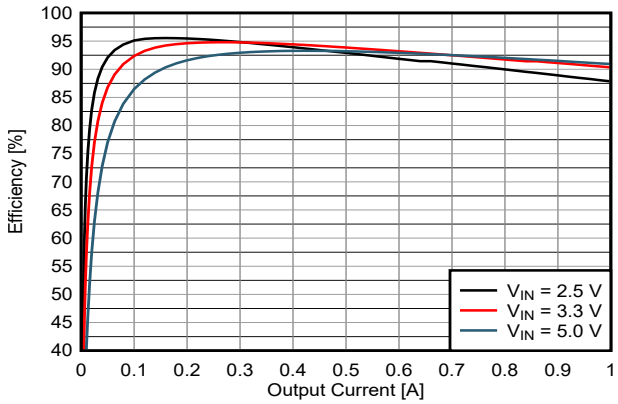
TPS62A01 (PSM/PWM) SOT-23 (DDC)

图 8-13. 1.2V Output Efficiency



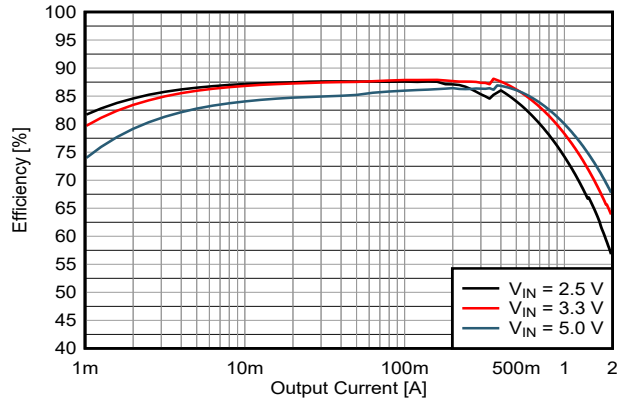
TPS62A01 (PSM/PWM) SOT-23 (DDC)

图 8-14. 1.8V Output Efficiency



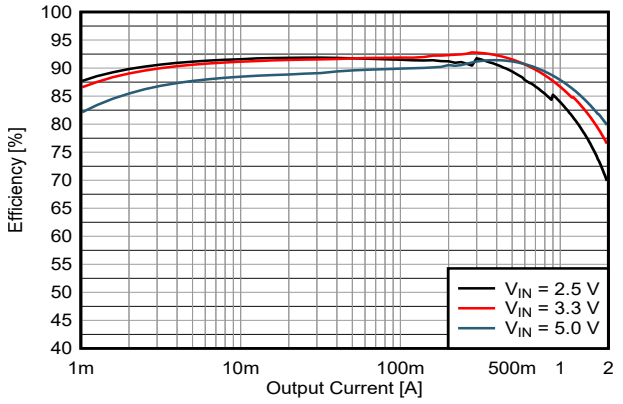
TPS62A01A (FPWM) SOT-23 (DDC)

图 8-15. 1.8V Output Efficiency



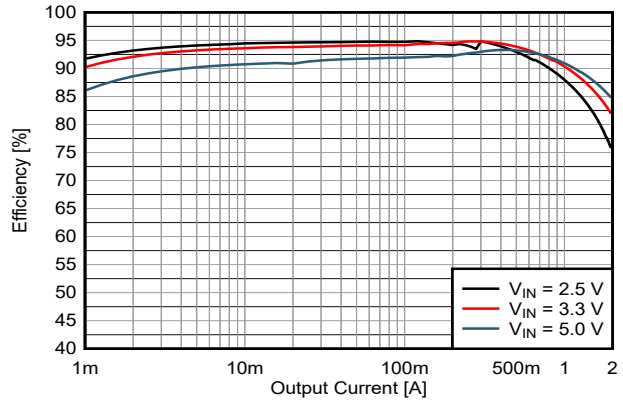
TPS62A02 (PSM/PWM) SOT-23 (DDC)

图 8-16. 0.6V Output Efficiency



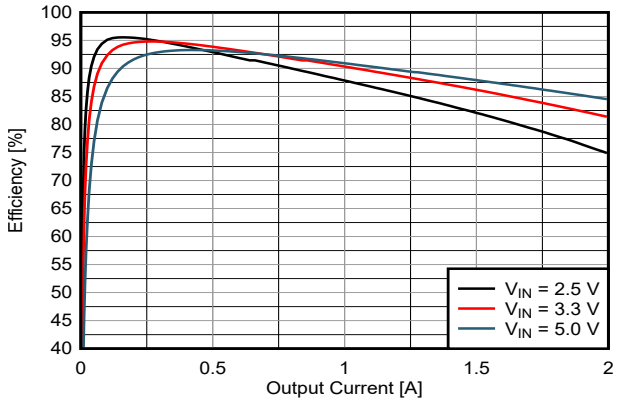
TPS62A02 (PSM/PWM) SOT-23 (DDC)

图 8-17. 1.2V Output Efficiency



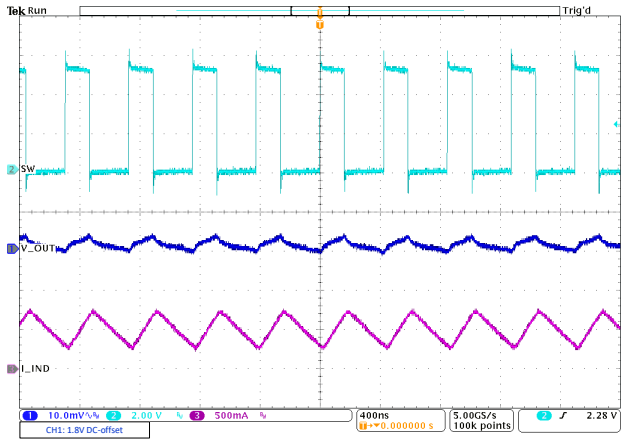
TPS62A02 (PSM/PWM) SOT-23 (DDC)

图 8-18. 1.8V Output Efficiency



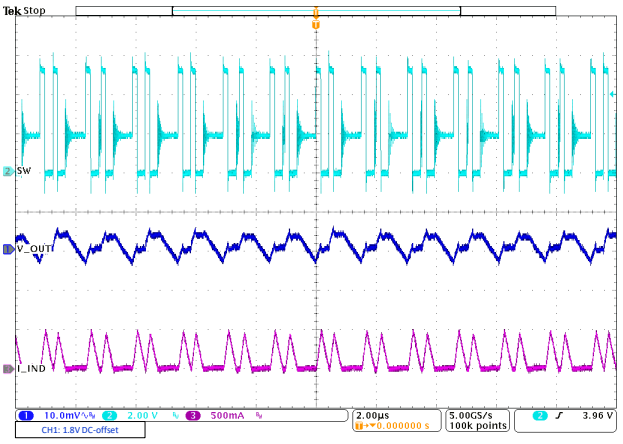
TPS62A02A (FPWM) SOT-23 (DDC)

图 8-19. 1.8V Output Efficiency



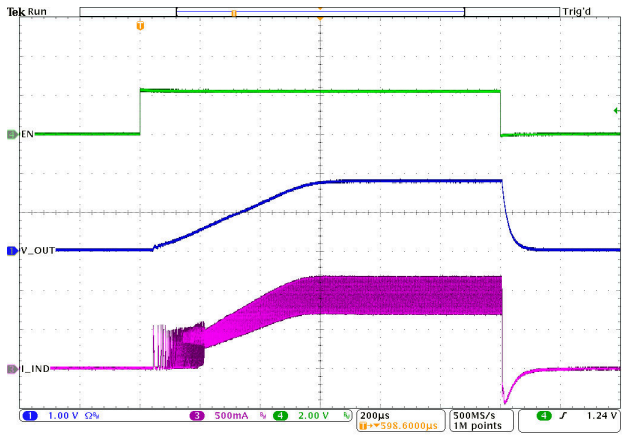
I_{OUT} = 500 mA

图 8-20. PWM Operation



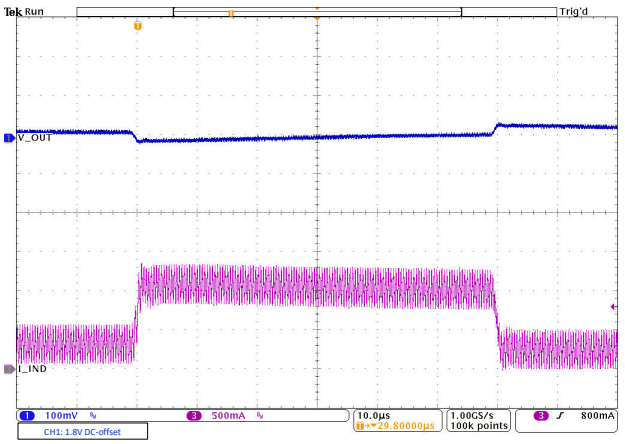
I_{OUT} = 100 mA

图 8-21. Power Save Mode Operation



I_{OUT} = 1 A

图 8-22. Start-Up with Load



Load step: 0.3 A to 1 A

图 8-23. Load Transient

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.5V to 5.5V. Make sure that the input power supply has a sufficient current rating for the application.

8.4 Layout

8.4.1 Layout Guidelines

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the TPS62A01x and TPS62A02x devices.

- Place the input and output capacitors and the inductor as close as possible to the IC. This action keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- Connect the low side of the input and output capacitors properly to the GND pin to avoid a ground potential shift.
- The sense traces connected to FB is a signal trace. Take special care to avoid noise being induced. Keep these traces away from SW nodes.
- Use a common ground. GND layers can be used for shielding.

See 图 8-24 and 图 8-25 for the recommended PCB layout.

8.4.2 Layout Example

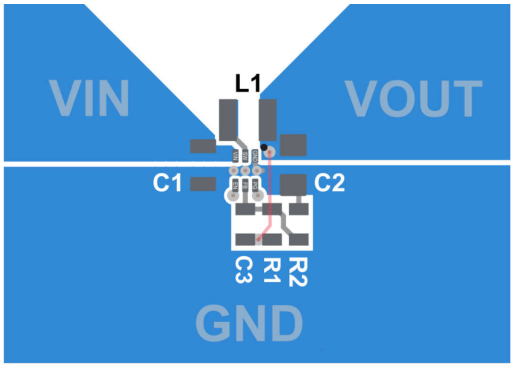


图 8-24. TPS62A0x (SOT563) PCB Layout Recommendation

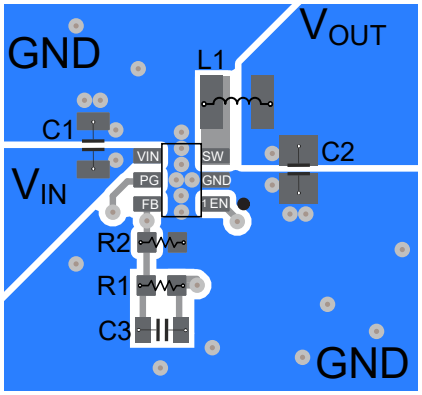


图 8-25. TPS62A0x (SOT23-6) PCB Layout Recommendation

9 Device and Documentation Support

9.1 Device Support

9.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (April 2024) to Revision E (June 2024)	Page
• Changed device status of TPS62A02Nx versions and devices in DDC package from preview to production throughout the data sheet	3

Changes from Revision C (December 2023) to Revision D (April 2024)	Page
• 在整个数据表中添加了带有“N”后缀的器件	1
• Changed absolute maximum voltage of VIN, EN and PG from 6V to 6.5V	4
• Updated block diagram to include devices with 'N' suffix (OUT instead of PG)	8

Changes from Revision B (July 2022) to Revision C (December 2023)	Page
• Added DDC package option throughout the data sheet	3
• Changed ESD Ratings CDM row from showing testing was per JESD22-C101 to show that testing was per JS-002	4
• Changed block diagram PG circuit by swapping V_{PG} and V_{FB}	8

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62A01ADRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	1J8
TPS62A01ADRLR.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1J8
TPS62A01APDDCR	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	A01AP
TPS62A01APDDCR.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	A01AP
TPS62A01DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	1J7
TPS62A01DRLR.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1J7
TPS62A01PDDCR	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	A01P
TPS62A01PDDCR.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	A01P
TPS62A02ADRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	1JM
TPS62A02ADRLR.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1JM
TPS62A02APDDCR	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	A02AP
TPS62A02APDDCR.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	A02AP
TPS62A02DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	1JL
TPS62A02DRLR.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1JL
TPS62A02NADRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	1SC
TPS62A02NADRLR.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1SC
TPS62A02NDRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1SB
TPS62A02NDRLR.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1SB
TPS62A02PDDCR	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	A02P
TPS62A02PDDCR.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	A02P

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS62A01, TPS62A01A, TPS62A02, TPS62A02A :

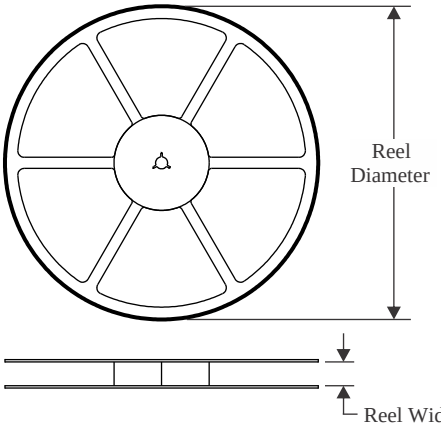
- Automotive : TPS62A01-Q1, TPS62A01A-Q1, TPS62A02-Q1, TPS62A02A-Q1

NOTE: Qualified Version Definitions:

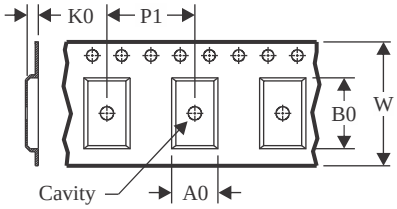
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

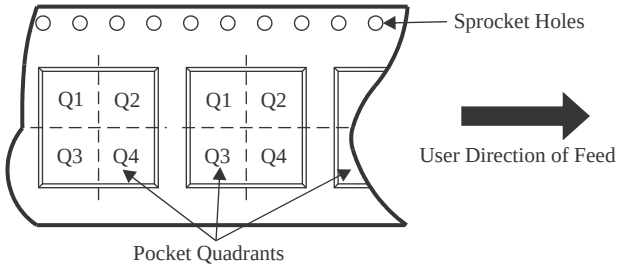


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

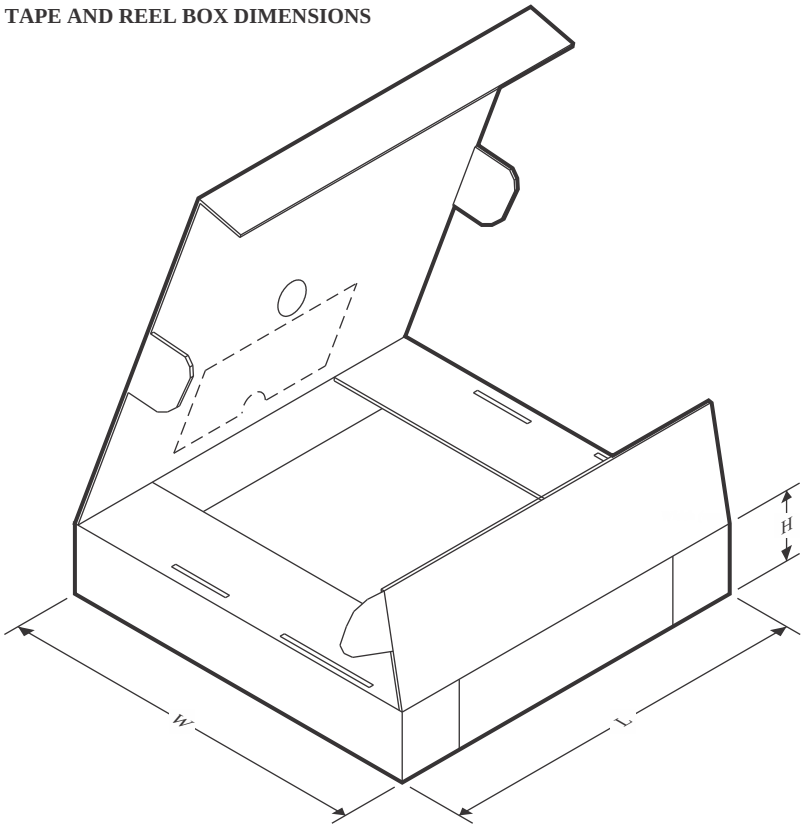
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62A01ADRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPS62A01APDDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62A01DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPS62A01PDDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62A02ADRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPS62A02APDDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62A02DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.8	1.8	0.75	4.0	8.0	Q3
TPS62A02DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.8	1.8	0.75	4.0	8.0	Q3
TPS62A02DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPS62A02NADRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPS62A02NDRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPS62A02PDDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

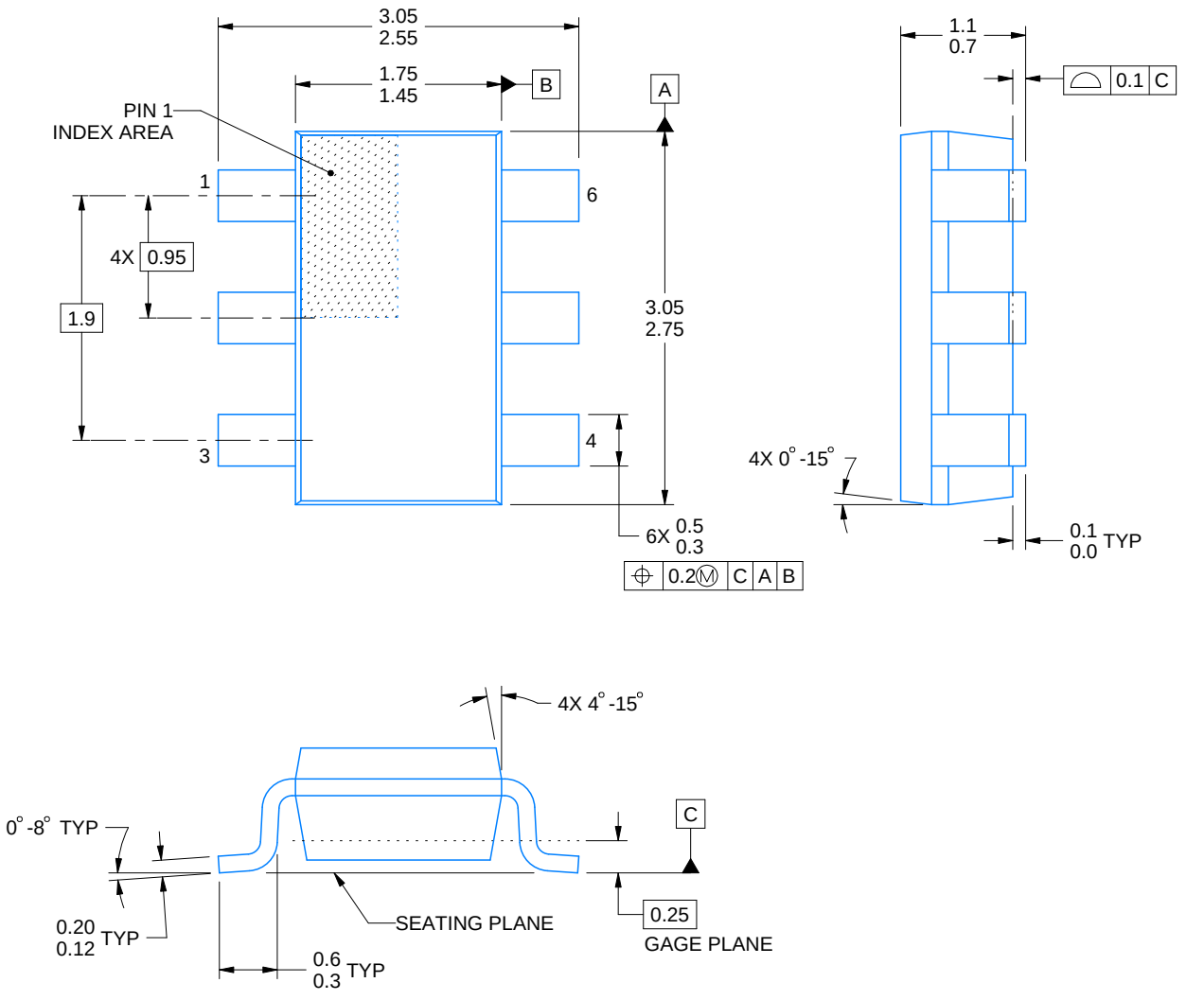
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62A01ADRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS62A01APDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TPS62A01DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS62A01PDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TPS62A02ADRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS62A02APDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TPS62A02DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS62A02DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS62A02DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS62A02NADRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS62A02NDRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS62A02PDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DDC0006A

SOT-23 - 1.1 max height

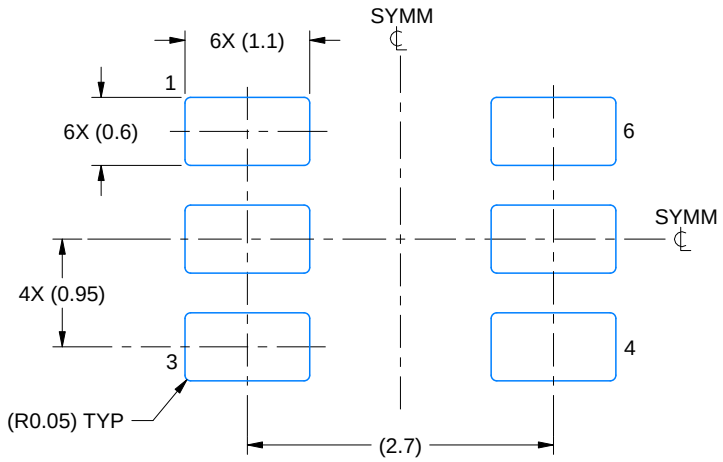
SMALL OUTLINE TRANSISTOR



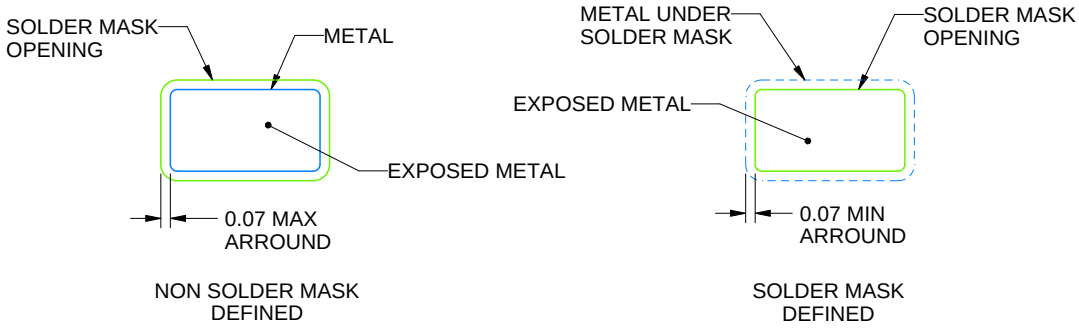
4214841/E 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

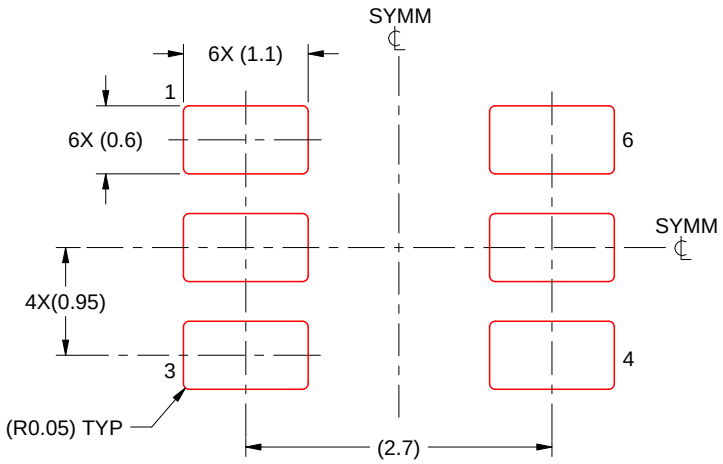


SOLDERMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

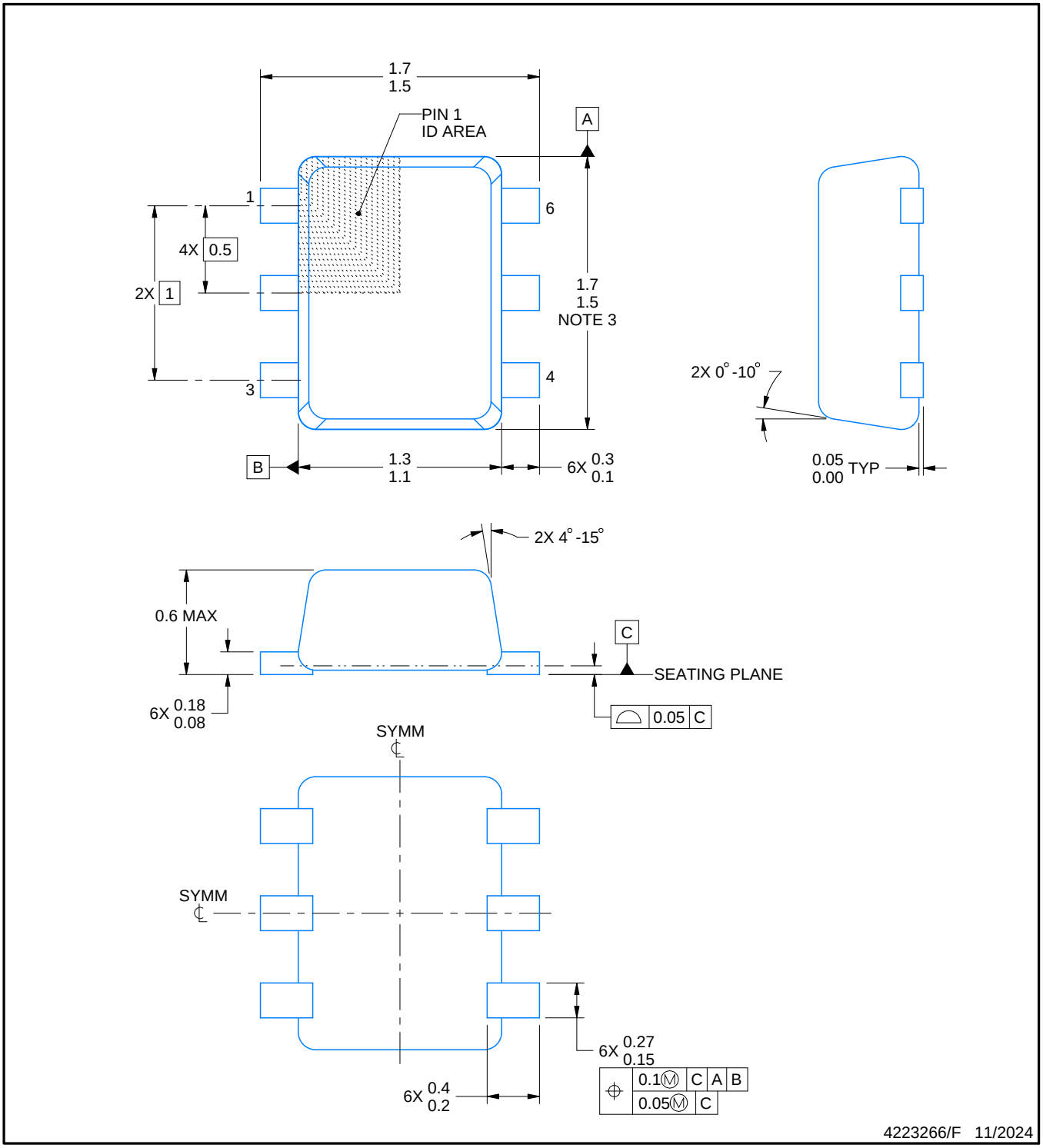
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

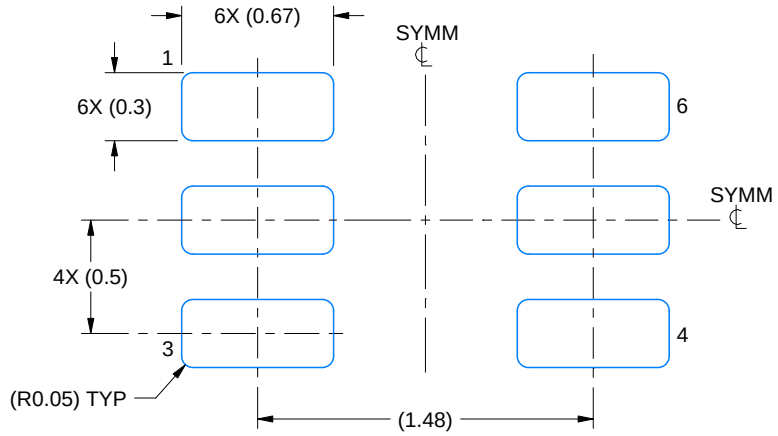
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

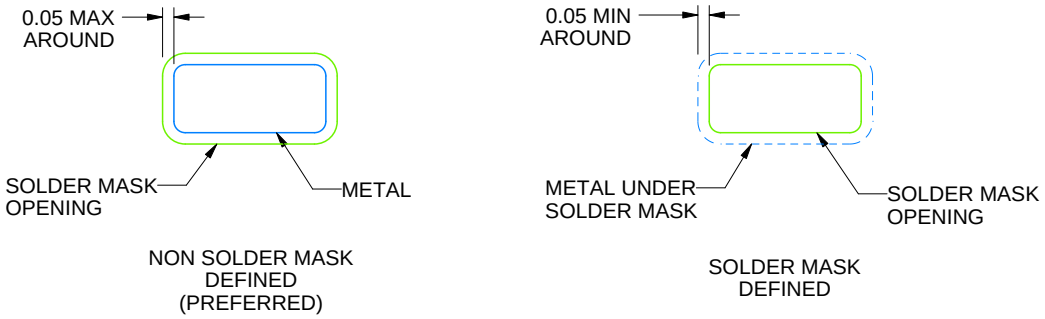
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/F 11/2024

NOTES: (continued)

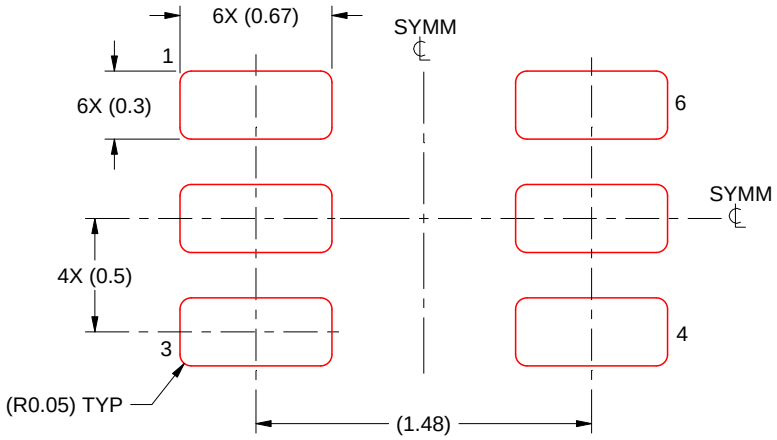
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月