TPS62125 使能阈值和迟滞可调节的 3V 至 17V、300mA 降压转换器

1 特性

- 宽输入电压范围：3V 至 17V
- 具有可调节阈值和迟滞的输入电源电压监控器 (SVS)，仅消耗 6μA 静态电流
- 1.2V 至 10V 宽输出电压范围
- 静态电流典型值为 13μA
- 关断电流典型值为 350nA
- 无缝转换节能模式
- DCS-Control™机制
- 低输出纹波电压
- 高达 1MHz 的开关频率
- 在 V_{IN}和 V_{OUT}范围内的最高效率
- 与 TPS62160/70 引脚到引脚兼容
- 100% 占空比模式
- 电源正常开漏输出
- 输出放电功能
- 2mm x 2mm、8 引脚晶圆级小外形无引线 (WSON) 小型封装

2 应用

- 嵌入式处理
- 由 4 节碱性电池、1 至 4 节锂离子电池供电的 应用
- 9V 至 15V 待机电源
- 能量采集
- 逆变器（负 V_{OUT}）

3 说明

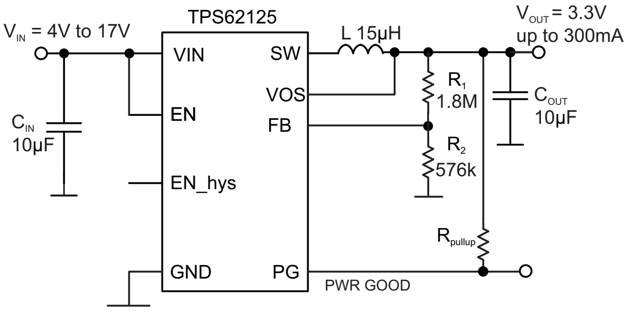
TPS62125 器件是一款高效同步降压转换器，针对低功耗/超低功耗 应用 进行了优化，输出电流高达 300mA。该器件的宽输入电压范围为 3V 至 17V，可支持由 4 节碱性电池、1 至 4 节锂离子电池串联配置以及 9V 至 15V 电压供电的 应用的输出电流传感电阻器和运算放大器而得以实现。该器件具备一个精密的低功耗使能比较器，其可用作输入电源电压监视器 (SVS)，以满足系统特定的上电和断电要求。该使能比较器仅消耗 6μA 静态电流并 具备 典型值为 1.2V 的精确阈值以及可调节迟滞。借助此特性，该转换器能够从由太阳能板或者电流回路等高阻抗源供电的储能电容中提取电能，以生成电源轨。凭借其 DCS-Control 机制，该转换器可在节能模式下运行，从而在整个负载电流范围内保持最高效率。在轻载条件下，该转换器能够以脉频调制 (PFM) 模式运行并在负载电流较大时自动无缝转换至脉宽调制 (PWM) 模式。该 DCS-Control™ 机制已针对 PFM 模式下的低输出纹波电压进行了优化，从而最大限度地降低输出噪声 并 获得优异的交流负载稳压性能。开漏电源正常输出表示正在对输出电压进行稳压。

器件信息[1]

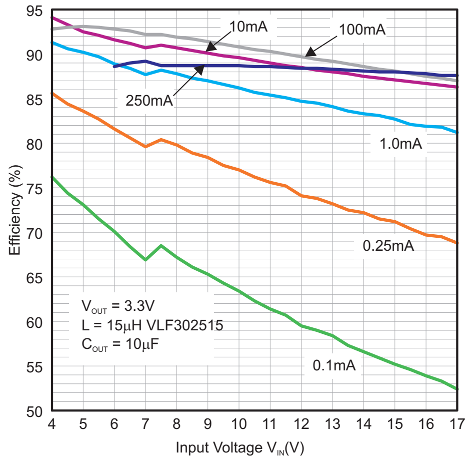
器件型号	封装	封装尺寸（标称值）
TPS62125	WSON (8)	2.00mm x 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用电路原理图



效率与输入电压间的关系



目录

4 修订历史记录

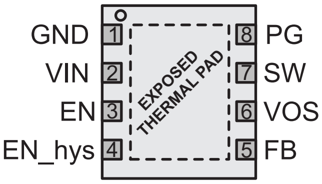
注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (July 2015) to Revision E	Page
• Added SW node AC abs max ratings	4

Changes from Revision C (December 2013) to Revision D	Page
• 已添加 *引脚配置和功能部分*，*ESD 额定值表*，*特性 说明 部分*，*器件功能模式*，*应用和实施部分*，*电源相关建议部分*，*布局部分*，*器件和文档支持部分以及机械、封装和可订购信息部分*	1

5 Pin Configuration and Functions

DSG Package
8-Pin WSON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	3	IN	Input pin for the enable comparator. Pulling this pin to GND turns the device into shutdown mode. The DC/DC converter is enabled once the rising voltage on this pin trips the enable comparator threshold, $V_{TH\ EN\ ON}$ of typ. 1.2 V. The DC/DC converter is turned off once a falling voltage on this pin trips the threshold, $V_{TH\ EN\ OFF}$ of typ. 1.15 V. The comparator threshold can be increased by connecting an external resistor to pin EN_hys. See also application section. This pin must be terminated.
EN_hys	4	OUT	Enable hysteresis open-drain output. This pin is pulled to GND when the voltage on the EN pin is below the comparator threshold $V_{TH\ EN\ ON}$ of typ. 1.2 V and the comparator has not yet tripped. The pin is high impedance once the enable comparator has tripped and the voltage at the pin EN is above the threshold $V_{TH\ EN\ ON}$. The pin is pulled to GND once the falling voltage on the EN pin trips the threshold $V_{TH\ EN\ OFF}$ (1.15 V typical). This pin can be used to increase the hysteresis of the enable comparator. If not used, tie this pin to GND, or leave it open.
FB	5	IN	This is the feedback pin for the regulator. An external resistor divider network connected to this pin sets the output voltage. In case of fixed output voltage option, the resistor divider is integrated and the pin need to be connected directly to the output voltage.
GND	1	PWR	GND supply pin.
PG	8	OUT	Open drain power good output. This pin is internally pulled to GND when the device is disabled or the output voltage is below the PG threshold. The pin is floating when the output voltage is in regulation and above the PG threshold. For power good indication, the pin can be connected via a pull up resistor to a voltage rail up to 10 . The pin can sink a current up to 0.4 mA and maintain the specified high/low voltage levels. It can be used to discharge the output capacitor with up to 10 mA. In this case the current into the pin must be limited with an appropriate pull up resistor. More details can be found in the application section. If not used, leave the pin open, or connect to GND.
SW	7	OUT	This is the switch pin and is connected to the internal MOSFET switches. Connect the inductor to this pin. Do not tie this pin to VIN, VOUT or GND.
VIN	2	PWR	V_{IN} power supply pin.
VOS	6	IN	This is the output voltage sense pin for the DCS-Control circuitry. This pin must be connected to the output voltage of the DC/DC converter.
Exposed Thermal PAD	–	–	This pad must be connected to GND.

6 Specifications

6.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
Pin voltage[2]	VIN	–0.3	20	V
	SW (DC)	–0.3	V_{IN} + 0.3V	V
	SW (AC, less than 10ns)[3]	-3.0	23.5	V
	EN	–0.3	V_{IN} + 0.3	V
	FB	–0.3	3.6	V
	VOS, PG	–0.3	12	V
	EN_hys	–0.3	7	V
Power good sink current	I_{PG}		10	mA
EN_hys sink current	I_{EN_hys}		3	mA
Maximum operating junction temperature, T_J		–40	125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal GND.
(3) While switching

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage		3		17	V
	Output current capability	3 V ≤ V_{IN} < 6 V			200	mA
		6 V ≤ V_{IN} ≤ 17 V			300	
T_A	Operating ambient temperature (1) (Unless Otherwise Noted)		–40		85	°C
T_J	Operating junction temperature,		–40		125	°C

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$) and the maximum power dissipation of the device in the application ($P_{D(max)}$); for more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.4 Thermal Information

THERMAL METRIC[1]		TPS62125	UNIT
		DSG (WSON)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	93.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted), V_{IN} = 12 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range(1)		3		17	V
V_{OUT}	Output voltage range		1.2		10	V
I_Q	Quiescent current	I_{OUT} = 0 mA, device not switching, EN = V_{IN}, regulator sleeps		13	23	µA
		I_{OUT} = 0 mA, device switching, V_{IN} = 7.2 V, V_{OUT} = 1.2 V, L = 22 µH		14		µA
		V_{IN} = 5 V, EN = 1.1 V, enable comparator active, device DC/DC converter off		6	11	µA
I_{Active}	Active mode current consumption	V_{IN} = 5 V = V_{OUT}, T_A = 25°C, high-side MOSFET switch fully turned on (100% mode)		230	275	µA
I_{SD}	Shutdown current(2)	Enable comparator off, EN < 0.4 V, V_{OUT} = SW = 0 V, V_{IN} = 5 V		0.35	2.4	µA
V_{UVLO}	Undervoltage lockout threshold	Falling V_{IN}		2.8	2.85	V
		Rising V_{IN}		2.9	2.95	V
ENABLE COMPARATOR THRESHOLD AND HYSTERESIS (EN, EN_hys)						
$V_{TH\ EN\ ON}$	EN pin threshold rising edge	3 V ≤ V≤ 17 V	1.16	1.20	1.24	V
$V_{TH\ EN\ OFF}$	EN pin threshold falling edge		1.12	1.15	1.19	V
$V_{TH\ EN\ Hys}$	EN pin hysteresis $_{IN}$			50		mV
$I_{IN\ EN}$	Input bias current into EN pin	EN = 1.3 V		0	50	nA
V_{EN_hyst}	EN_hys pin output low	I_{EN_hyst} = 1 mA, EN = 1.1 V			0.4	V
$I_{IN\ EN\_hyst}$	Input bias current into EN_hyst pin	EN_hyst = 1.3 V		0	50	nA
POWER SWITCH						
$R_{DS(ON)}$	High-side MOSFET ON-resistance	V_{IN} = 3 V, I = 100 mA		2.4	4	Ω
		V_{IN} = 12 V, I = 100 mA		1.5	2.6	
	Low-side MOSFET ON-resistance	V_{IN} = 3 V, I = 100 mA		0.75	1.3	
		V_{IN} = 12 V, I = 100 mA		0.6	1	
I_{LIMF}	Switch current limit high-side MOSFET	V_{IN} = 12 V	600	750	900	mA
T_{SD}	Thermal shutdown	Increasing junction temperature		150		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		20		°C
OUTPUT						
t_{ONmin}	Minimum ON-time	V_{IN} = 5 V, V_{OUT} = 2.5 V		500		ns
t_{OFFmin}	Minimum OFF-time	V_{IN} = 5 V		60		ns
V_{REF_FB}	Internal reference voltage of error amplifier			0.808		V
V_{FB}	Feedback voltage accuracy	Referred to internal reference (V_{REF_FB})	–2.5%	0%	2.5%	
	Feedback voltage line regulation	I_{OUT} = 100 mA, 5 V ≤ V_{IN} ≤ 17 V, V_{OUT} = 3.3 V(3)		–0.05		%/V
	Feedback voltage load regulation	V_{OUT} = 3.3 V; I_{OUT} = 1 mA to 300 mA, V_{IN} = 12 V(3)		–0.004		%/mA
I_{IN_FB}	Input bias current into FB pin	V_{FB} = 0.8 V		0	50	nA
t_{Start}	Regulator start-up time	Time from EN high to device starts switching, V_{IN} = 5 V		50		µs
t_{Ramp}	Output voltage ramp time	Time to ramp up V_{OUT} = 1.8 V, no load		200		
I_{LK_SW}	Leakage current into SW pin(4)	VOS = V_{IN} = V_{SW} = 1.8 V, EN = GND, device in shutdown mode		1.8	2.85	µA
I_{IN_VOS}	Bias current into VOS pin			0	50	nA

(1) The part is functional down to the falling UVLO (Undervoltage Lockout) threshold
(2) Current into VIN pin
(3) V_{OUT} = 3.3 V, L = 15 µH, C_{OUT} = 10 µF
(4) An internal resistor divider network with typ. 1 MΩ total resistance is connected between SW pin and GND.

Electrical Characteristics (continued)

T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted), V_{IN} = 12 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD OUTPUT (PG)						
V_{TH_PG}	Power good threshold voltage	Rising V_{FB} feedback voltage	93%	95%	97%	
		Falling V_{FB} feedback voltage	87%	90%	93%	
V_{OL}	PG pin output low voltage	Current into PG pin I_{PG}= 0.4 mA			0.3	V
V_{OH}	PG pin output high voltage	Open drain output, external pullup resistor			10	V
I_{IN_PG}	Bias current into PG pin	$V_{(PG)}$ = 3 V, EN = 1.3 V, FB = 0.85 V		0	50	nA

6.6 Typical Characteristics

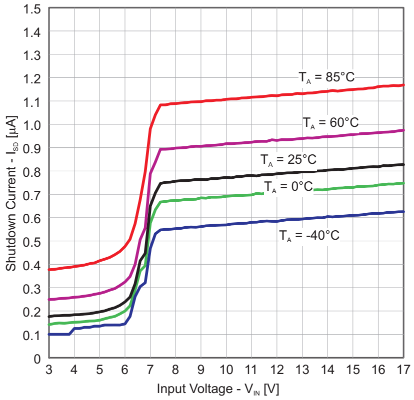


Figure 1. Shutdown Current vs. Input Voltage

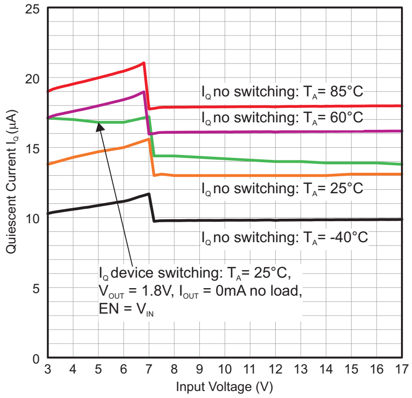


Figure 2. Quiescent Current vs. Input Voltage

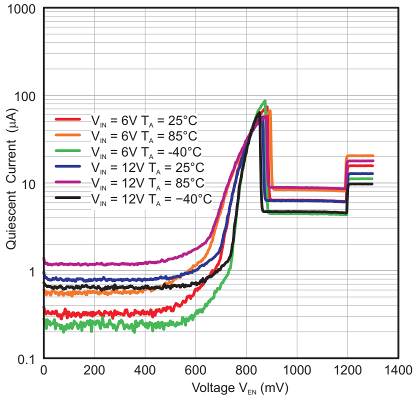


Figure 3. Quiescent Current vs. EN Voltage, Rising V_{EN}

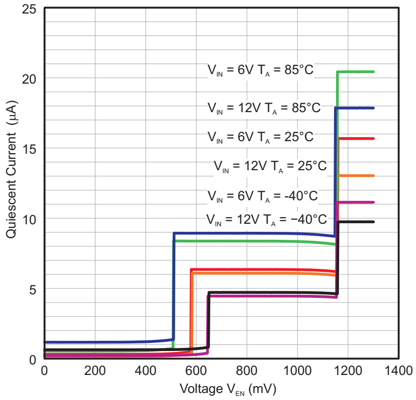


Figure 4. Quiescent Current vs. V_{EN} Voltage, Falling V_{EN}

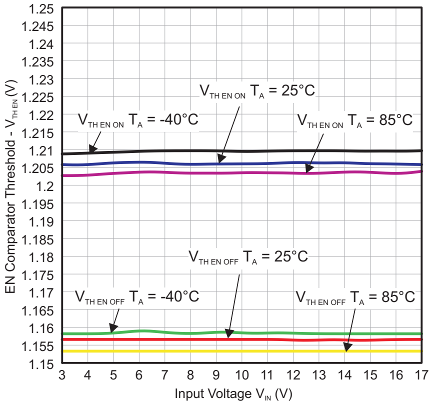


Figure 5. EN Comparator Thresholds vs. Input Voltage

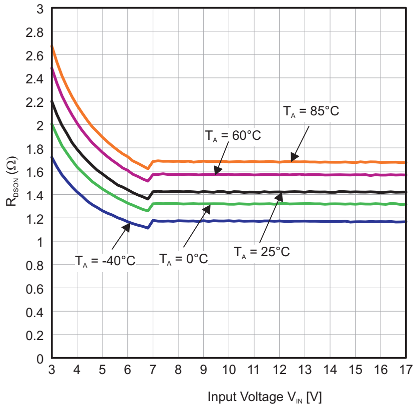


Figure 6. R_{DSON} High-Side Switch

Typical Characteristics (continued)

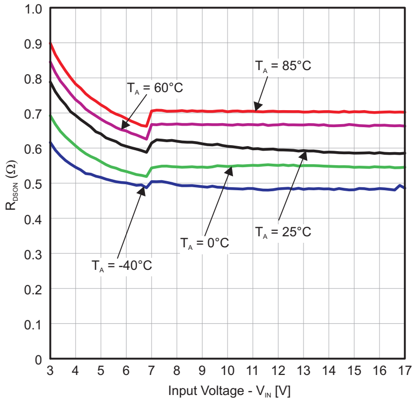


Figure 7. R_{DSON} Low-Side Switch (Rectifier)

7 Detailed Description

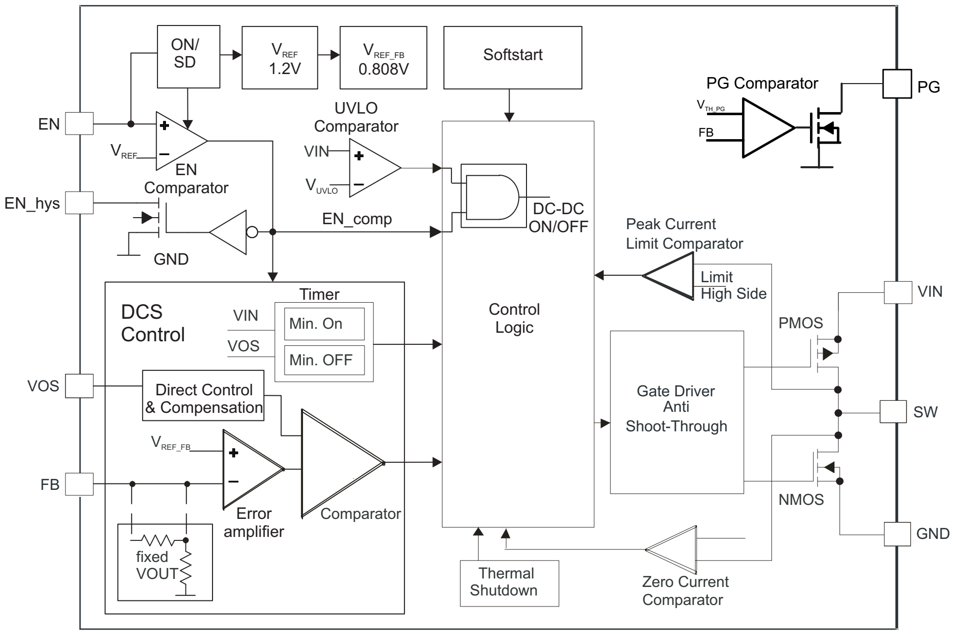
7.1 Overview

The TPS62125 high-efficiency synchronous switch mode buck converter includes TI's DCS-Control (**D**irect **C**ontrol with **S**eamless Transition into Power-Save Mode), an advanced regulation topology, which combines the advantages of hysteretic and voltage mode control. Characteristics of DCS-Control are excellent AC load regulation and transient response, low-output ripple voltage and a seamless transition between PFM and PWM mode operation.

DCS-Control includes an AC loop which senses the output voltage (VOS pin) and directly feeds the information to a fast comparator stage. This comparator sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. In order to achieve accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors. The DCS-Control topology supports pulse width modulation (PWM) mode for medium and high load conditions and a power-save mode at light loads. During PWM mode, it operates in continuous conduction. The switch frequency is up to 1 MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter seamless enters power-save mode to maintain high efficiency down to very light loads. In power-save mode the switching frequency varies linearly with the load current. Because DCS-Control supports both operation modes within one single building block, the transition from PWM to power-save mode is seamless without effects on the output voltage. The TPS62125 offers both excellent DC voltage and superior load transient regulation, combined with very low-output voltage ripple, minimizing interference with RF circuits.

At high load currents the converter operates in quasi fixed frequency PWM mode operation and at light loads in pulse frequency modulation (PFM) mode to maintain highest efficiency over the full load current range. In PFM mode, the device generates a single switching pulse to ramp up the inductor current and recharge the output capacitor, followed by a sleep period where most of the internal circuits are shutdown to achieve a quiescent current of typically 13 µA. During this time, the load current is supported by the output capacitor. The duration of the sleep period depends on the load current and the inductor peak current.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Lockout

In addition to the EN comparator, the device includes an under-voltage lockout circuit which prevents the device from misoperation at low input voltages. Both circuits are fed to an AND gate and prevents the converter from turning on the high-side MOSFET switch or low-side MOSFET under undefined conditions. The UVLO threshold is set to 2.9 V typical for rising V_{IN} and 2.8 V typical for falling V_{IN}. The hysteresis between rising and falling UVLO threshold ensures proper start-up. Fully functional operation is permitted for an input voltage down to the falling UVLO threshold level. The converter starts operation again once the input voltage trips the rising UVLO threshold level and the voltage at the EN pin trips $V_{TH\_EN\_ON}$.

7.3.2 Enable Comparator (EN / EN_hys)

The EN pin is connected to an on/shutdown detector (ON/SD) and an input of the enable comparator. With a voltage level of 0.4 V or less at the EN pin, the ON/SD detector turns the device into Shutdown mode and the quiescent current is reduced to typically 350 nA. In this mode the EN comparator as well the entire internal-control circuitry are switched off. A voltage level of typical 900 mV (rising) at the EN pin triggers the on/shutdown detector and activates the internal reference V_{REF} (typical 1.2 V), the EN comparator and the UVLO comparator. In applications with slow rising voltage levels at the EN pin, the quiescent current profile before this trip point needs to be considered, see Figure 3. Once the ON/SD detector has tripped, the quiescent current consumption of the device is typical 6 µA. The TPS62125 starts regulation once the voltage at the EN pin trips the threshold $V_{EN\_TH\ ON}$ (typical 1.2 V) and the input voltage is above the UVLO threshold. It enters softstart and ramps up the output voltage. For proper operation, the EN pin must be terminated and must not be left floating. The quiescent current consumption of the TPS62125 is typical 13 µA under no load condition (not switching). See Figure 1. The DC/DC regulator stops operation once the voltage on the EN pin falls below the threshold $V_{EN\_TH\ OFF}$ (typical 1.15 V) or the input voltage falls below UVLO threshold. The enable comparator features a built in hysteresis of typical 50 mV. This hysteresis can be increased with an external resistor connected to pin EN_hys.

7.3.3 Power Good Output and Output Discharge (PG)

The power good output (PG pin) is an open drain output. The circuit is active once the device is enabled. It is driven by an internal comparator connected to the FB pin voltage and an internal reference. The PG output provides a high level (open drain high impedance) once the feedback voltage exceeds typical 95% of its nominal value. The PG output is driven to low level once the FB pin voltage falls below typical 90% of its nominal value V_{REF_FB}. The PG output goes high (high impedance) with a delay of typically 2 µs. A pull up resistor is needed to generate a high level. The PG pin can be connected via a pull up resistors to a voltage up to 10 V. This pin can also be used to discharge the output capacitor. See section Application Information for more details.

The PG output is pulled low if the voltage on the EN pin falls below the threshold $V_{EN\_TH\ OFF}$ or the input voltage is below the undervoltage lockout threshold UVLO.

7.3.4 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 150°C (typical) the device goes into thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned-off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis.

7.4 Device Functional Modes

7.4.1 Pulse Width Modulation (PWM) Operation

The TPS62125 operates with pulse width modulation in continuous conduction mode (CCM) with a nominal switching frequency of about 1 MHz. The frequency variation in PWM mode is controlled and depends on V_{IN}, V_{OUT} and the inductance. The device operates in PWM mode as long the output current is higher than half the inductor's ripple current. To maintain high efficiency at light loads, the device enters power-save mode at the boundary to discontinuous conduction mode (DCM). This happens if the output current becomes smaller than half the inductor's ripple current.

Device Functional Modes (continued)

7.4.2 Power-Save Mode

With decreasing load current, the TPS62125 transitions seamlessly from PWM mode to power-save mode once the inductor current becomes discontinuous. This ensures a high efficiency at light loads. In power-save mode the converter operates in pulse frequency modulation (PFM) mode and the switching frequency decreases linearly with the load current. DCS-Control features a small and predictable output voltage ripple in power-save mode. The transition between PWM mode and power-save mode occurs seamlessly in both directions.

The minimum ON-time T_{ONmin} for a single pulse can be estimated by:

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times 1\mu s \tag{1}$$

Therefore the peak inductor current in PFM mode is approximately:

$$I_{LPFMpeak} = \frac{(V_{IN} - V_{OUT})}{L} \times T_{ON}$$

where

- T_{ON}: High-side MOSFET switch on time [µs]
- V_{IN}: Input voltage [V]
- V_{OUT}: Output voltage [V]
- L : Inductance [µH]
- $I_{LPFMpeak}$: PFM inductor peak current [mA] (2)

The transition from PFM mode to PWM mode operation and back occurs at a load current of approximately 0.5 x $I_{LPFMpeak}$.

The maximum switching frequency can be estimated by:

$$f_{SW\max} \approx \frac{1}{1\mu s} = 1MHz \tag{3}$$

7.4.3 100% Duty Cycle Low Dropout Operation

The device increases the ON-time of the high-side MOSFET switch as the input voltage comes close to the output voltage in order to keep the output voltage in regulation. This reduces the switching frequency.

With further decreasing input voltage V_{IN}, the high-side MOSFET switch is turned on completely. In this case, the converter provides a low input-to-output voltage difference. This is particularly useful in applications with a widely variable supply voltage to achieve longest operation time by taking full advantage of the whole supply voltage span.

The minimum input voltage to maintain output voltage regulation depends on the load current and output voltage, and can be calculated as:

$$V_{\mathrm{Im}in} = V_{OUT\min} + I_{OUT} \times (R_{DSON\max} + R_L)$$

where

- I_{OUT}: Output current
- $R_{DS(ON)max}$: Maximum high-side switch $R_{DS(ON)}$
- R_L: DC resistance of the inductor
- V_{OUTmin}: Minimum output voltage the load can accept (4)

7.4.4 Soft-Start

The TPS62125 has an internal soft-start circuit which controls the ramp up of the output voltage and limits the inrush current during start-up. This limits input voltage drop.

Device Functional Modes (continued)

The soft-start system generates a monotonic ramp up of the output voltage and reaches an output voltage of 1.8 V typical within 240 µs after the EN pin was pulled high. For higher output voltages, the ramp up time of the output voltage can be estimated with a ramp up slew rate of about 12 mV/us. TPS62125 is able to start into a prebiased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to its nominal value. In case the output voltage is higher than the nominal value, the device starts switching once the output has been discharged by an external load or leakage current to its nominal output voltage value.

During start-up the device can provide an output current of half of the high-side MOSFET switch current limit I_{LIMF}. Large output capacitors and high load currents may exceed the current capability of the device during start-up. In this case the start-up ramp of the output voltage will be slower.

7.4.5 Short-Circuit Protection

The TPS62125 integrates a high-side MOSFET switch current limit, I_{LIMF}, to protect the device against a short circuit. The current in the high-side MOSFET switch is monitored by a current limit comparator and once the current reaches the limit of I_{LIMF} , the high-side MOSFET switch is turned off and the low-side MOSFET switch is turned on to ramp down the inductor current. The high-side MOSFET switch is turned on again once the zero current comparator trips and the inductor current has become zero. In this case, the output current is limited to half of the high-side MOSFET switch current limit, 0.5 x I_{LIMF}, typ. 300mA.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS62125 is a high-efficiency synchronous step-down converter providing a wide output voltage range from 1.2 V to 10 V.

8.2 Typical Application

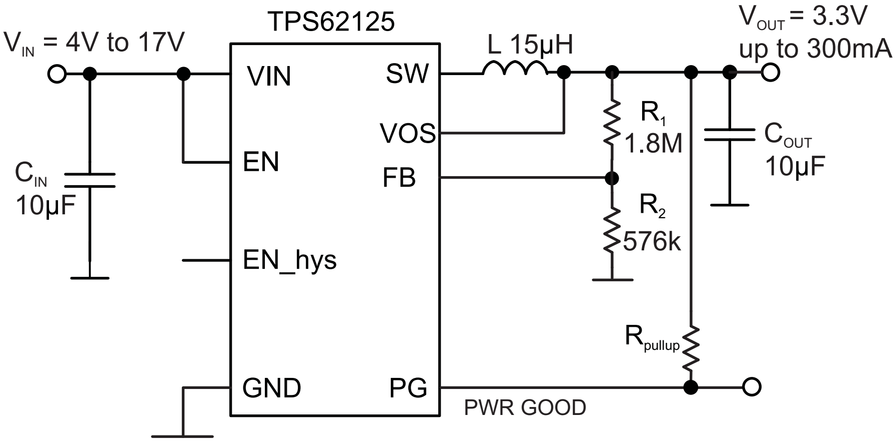


Figure 8. TPS62125 3.3-V Output Voltage Configuration

8.2.1 Design Requirements

The device operates over an input voltage range from 3 V to 17 V. The output voltage is adjustable using an external feedback divider.

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Setting

The output voltage can be calculated by:

$$V_{OUT} = V_{REF\_FB} \times \left(1 + \frac{R_1}{R_2}\right)$$

$$V_{OUT} = 0.8V \times \left(1 + \frac{R_1}{R_2}\right)$$

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{0.8V} - 1\right) \tag{5}$$

Typical Application (continued)

The internal reference voltage for the error amplifier, V_{REF_FB}, is nominal 0.808 V. However for the feedback resistor divider selection, it is recommended to use the value 0.800 V as the reference. Using this value, the output voltage sets 1% higher and provides more headroom for load transients as well for line and load regulation. The current through the feedback resistors R_1 and R_2 should be higher than 1 µA. In applications operating over full temperature range or in noisy environments, this current may be increased for robust operation. However, higher currents through the feedback resistors impact the light load efficiency of the converter.

Table 1 shows a selection of suggested values for the feedback divider network for most common output voltages.

Table 1. Suggested Values for Feedback Divider Network

OUTPUT VOLTAGE	1.2 V	1.8 V	3.3 V	5 V	6.7 V	8 V
R1 [kΩ]	180	300	1800	1100	1475	1800
R2 [kΩ]	360	240	576	210	200	200

8.2.2.2 Enable Threshold and Hysteresis Setting

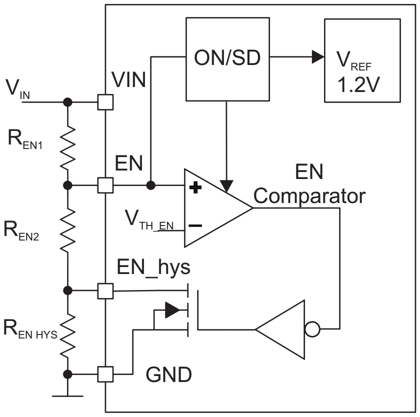


Figure 9. Using the Enable Comparator Threshold and Hysteresis for an Input SVS (Supply Voltage Supervisor)

The enable comparator can be used as an adjustable input supply voltage supervisor (SVS) to start and stop the DC/DC converter depending on the input voltage level. The input voltage level, $V_{IN\_startup}$, at which the device starts up is set by the resistors R_{EN1} and R_{EN2} and can be calculated by :

$$V_{IN\_startup} = V_{EN\_TH\_ON} \times \left(1 + \frac{R_{EN1}}{R_{EN2}}\right) = 1.2V \times \left(1 + \frac{R_{EN1}}{R_{EN2}}\right) \tag{6}$$

The resistor values R_{EN1} and R_{EN2} can be calculated by:

$$R_{EN1} = R_{EN2} \times \left(\frac{V_{IN\_startup}}{V_{EN\_TH\_ON}} - 1\right) = R_{EN2} \times \left(\frac{V_{IN\_startup}}{1.2V} - 1\right) \tag{7}$$

$$R_{EN2} = \frac{R_{EN1}}{\left(\frac{V_{IN\_startup}}{V_{EN\_TH\_ON}} - 1\right)} = \frac{R_{EN1}}{\left(\frac{V_{IN\_startup}}{1.2V} - 1\right)} \tag{8}$$

The input voltage level V_{IN_stop} at which the device will stop operation is set by R_{EN1}, R_{EN2} and $R_{EN\ HYS}$ and can be calculated by:

$$V_{IN\_stop} = V_{EN\_TH\_OFF} \times \left(1 + \frac{R_{EN1}}{R_{EN2} + R_{EN\_hys}}\right) = 1.15V \times \left(1 + \frac{R_{EN1}}{R_{EN2} + R_{EN\_hys}}\right) \quad (9)$$

The resistor value R_{EN_hys} can be calculated according to:

$$R_{EN\_hys} = \frac{R_{EN1}}{\left(\frac{V_{IN\_stop}}{V_{EN\_TH\_OFF}} - 1\right)} - R_{EN2} = \frac{R_{EN1}}{\left(\frac{V_{IN\_stop}}{1.15V} - 1\right)} - R_{EN2} \quad (10)$$

The current through the resistors R_{EN1}, R_{EN2}, and $R_{EN\ HYS}$ should be higher than 1 µA. In applications operating over the full temperature range and in noisy environments, the resistor values can be reduced to smaller values.

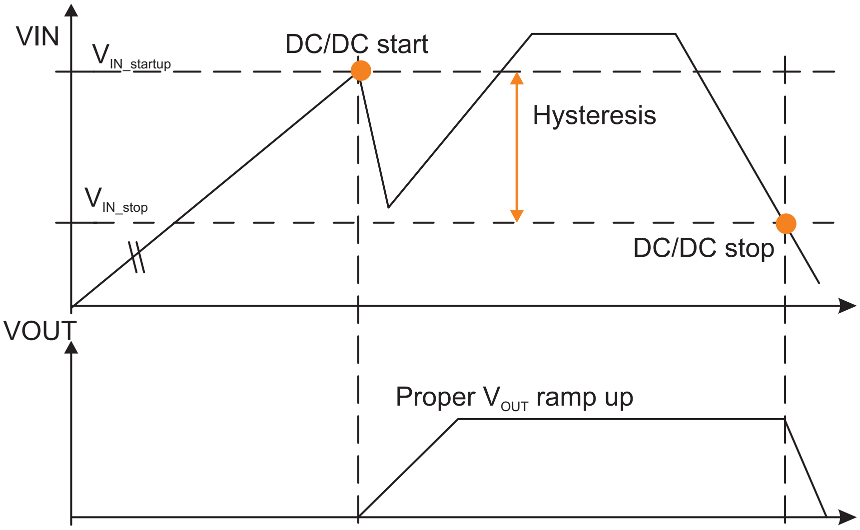


Figure 10. Using the EN Comparator as Input SVS for Proper V_{OUT} Ramp Up

8.2.2.3 Power Good (PG) Pullup and Output Discharge Resistor

The power good open collector output needs an external pull up resistor to indicate a high level. The pull up resistor can be connected to a voltage level up to 10 V. The output can sink current up to 0.4 mA with specified output low level of less than 0.3 V. The lowest value for the pull up resistor can be calculated by:

$$R_{Pullup\,\min} = \frac{V_{OUT} - 0.3V}{0.0004A} \quad (11)$$

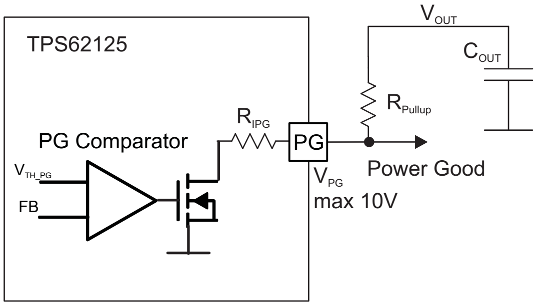


Figure 11. PG Open Collector Output

The PG pin can be used to discharge the output capacitor. The PG output has an internal resistance R_{IPG} of typical 600 Ω and minimum 400 Ω. The maximum sink current into the PG pin is 10 mA. In order to limit the discharge current to the maximum allowable sink current into the PG pin, the external pull up resistor $R_{Pull\ up}$ can be calculated to:

$$R_{Pullup\,\min} = \frac{V_{OUT}}{I_{PG\_\max}} - R_{IPG\_\min} = \frac{V_{OUT}}{0.01A} - 400\Omega \tag{12}$$

In case a negative value is calculated, the external pull up resistor can be removed and the PG pin can be directly connected to the output.

8.2.2.4 Output Filter Design (Inductor and Output Capacitor)

The external components have to fulfill the needs of the application, but also the stability criteria of the devices control loop. The TPS62125 is optimized to work within a range of L and C combinations. The LC output filter inductance and capacitance have to be considered together, creating a double pole, responsible for the corner frequency of the converter. Table 2 can be used to simplify the output filter component selection.

Table 2. Recommended LC Output Filter Combinations

INDUCTOR VALUE [µH] (1)	OUTPUT CAPACITOR VALUE [µF] (2)			
	10 µF	2 x 10 µF	22 µF	47 µF
V_{OUT} 1.2 V - 1.8 V				
15	√	√	√	√
22	√ (3)	√	√	√
V_{OUT} 1.8 V - 3.3 V				
15	√ (3)	√	√	√
22	√ (3)	√	√	√
V_{OUT} 3.3 V - 5 V				
10		√	√	√
15		√ (3)	√ (3)	√
22				
V_{OUT} 5 V - 10 V				
10		√ (3)	√ (3)	√
15		√	√	√
22		√	√	√

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by 20% and -30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by 20% and -50%.
(3) This LC combination is the standard value and recommended for most applications.

More detailed information on further LC combinations can be found in application note SLVA515.

8.2.2.5 Inductor Selection

The inductor value affects its peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple and the efficiency. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT} and can be estimated according to Equation 13.

Equation 14 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 14. This is recommended because during heavy load transient the inductor current will rise above the calculated value. A more conservative way is to select the inductor saturation current according to the high-side MOSFET switch current limit I_{LIMF}.

$$\Delta I_L = \frac{(V_{IN} - V_{OUT})}{L} \times T_{ON} \tag{13}$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2}$$

where

- T_{ON}: See Equation 1
- L: Inductance
- ΔI_L: Peak to Peak inductor ripple current
- I_{Lmax}: Maximum Inductor current (14)

In DC/DC converter applications, the efficiency is essentially affected by the inductor AC resistance (i.e. quality factor) and by the inductor DCR value. To achieve high-efficiency operation, take care in selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance (R_{DC}) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

The following inductor series from different suppliers have been used with the TPS62125.

Table 3. List of Inductors

INDUCTANCE [µH]	DCR [Ω]	DIMENSIONS [mm^3]	INDUCTOR TYPE	SUPPLIER
10 / 15	0.33 max / 0.44 max.	3.3 x 3.3 x 1.4	LPS3314	Coilcraft
22	0.36 max.	3.9 x 3.9 x 1.8	LPS4018	Coilcraft
15	0.33 max.	3.0 x 2.5 x 1.5	VLF302515	TDK
10/15	0.44 max / 0.7 max.	3.0 x 3.0 x 1.5	LPS3015	Coilcraft
10	0.38 typ.	3.2 × 2.5 × 1.7	LQH32PN	Murata

8.2.2.6 Output Capacitor Selection

Ceramic capacitors with low ESR values provide the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At light load currents the converter operates in power-save mode and the output voltage ripple is dependent on the output capacitor value and the PFM peak inductor current. Higher output capacitor values minimize the voltage ripple in PFM Mode and tighten DC output accuracy in PFM mode. In order to achieve specified regulation performance and low-output voltage ripple, the DC-bias characteristic of ceramic capacitors must be considered. The effective capacitance of ceramic capacitors drops with increasing DC-bias voltage. Due to this effect, it is recommended for output voltages above 3.3 V to use at least 1 x 22-µF or 2 x 10-µF ceramic capacitors on the output.

8.2.2.7 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For most applications, a 10-µF ceramic capacitor is recommended. The voltage rating and DC bias characteristic of ceramic capacitors need to be considered. The input capacitor can be increased without any limit for better input voltage filtering.

For applications powered from high impedance sources, a tantalum polymer capacitor should be used to buffer the input voltage for the TPS62125. Tantalum polymer capacitors provide a constant capacitance vs. DC bias characteristic compared to ceramic capacitors. In this case, a 10-µF ceramic capacitor should be used in parallel to the tantalum polymer capacitor to provide low ESR.

Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or V_{IN} step on the input can induce large ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part by exceeding the maximum ratings. In case the power is supplied via a connector e.g. from a wall adapter, a hot-plug event can cause voltage overshoots on the VIN pin exceeding the absolute maximum ratings and can damage the device, too. In this case a tantalum polymer capacitor or overvoltage protection circuit reduces the voltage overshoot, see Figure 45.

Table 4 shows a list of input/output capacitors.

Table 4. List of Capacitors

CAPACITANCE [µF]	SIZE	CAPACITOR TYPE	USAGE	SUPPLIER
10	0805	GRM21B 25V X5R	C_{IN} /C_{OUT}	Murata
10	0805	GRM21B 16V X5R	C_{OUT}	Murata
22	1206	GRM31CR61 16V X5R	C_{OUT}	Murata
22	B2 (3.5x2.8x1.9)	20TQC22MYFB	C_{IN} / input protection	Sanyo

8.2.3 Application Curves

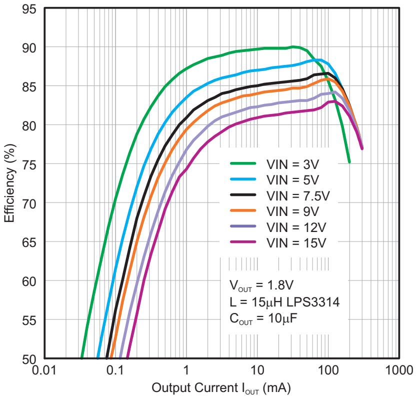


Figure 12. Efficiency vs. Output Current V_{OUT} = 1.8 V

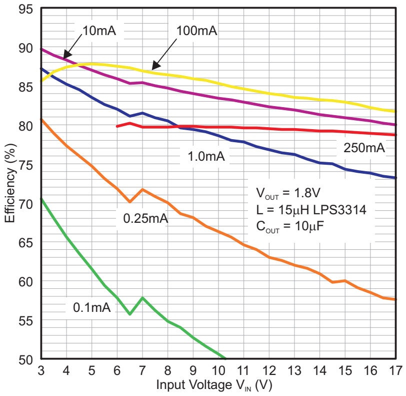


Figure 13. Efficiency vs. Input Voltage, V_{OUT} = 1.8 V

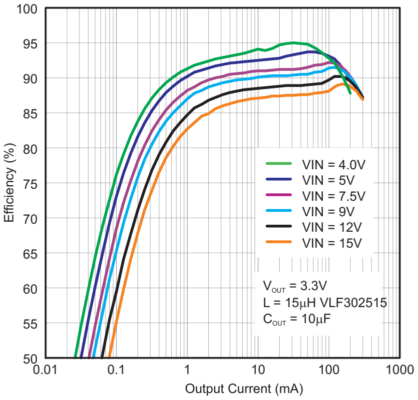


Figure 14. Efficiency vs. Output current, V_{OUT} = 3.3 V

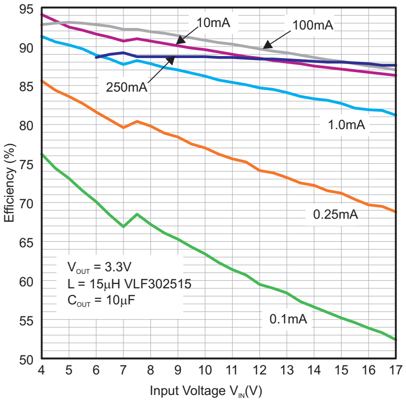


Figure 15. Efficiency vs. Input voltage, V_{OUT} = 3.3 V

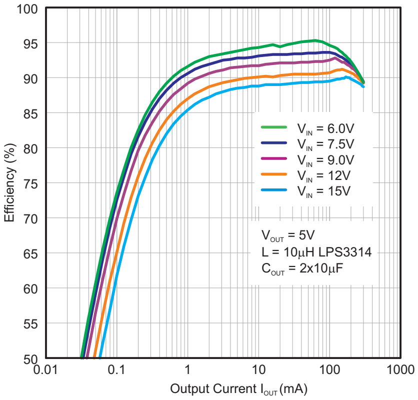


Figure 16. Efficiency vs. Output Current, V_{OUT} = 5 V

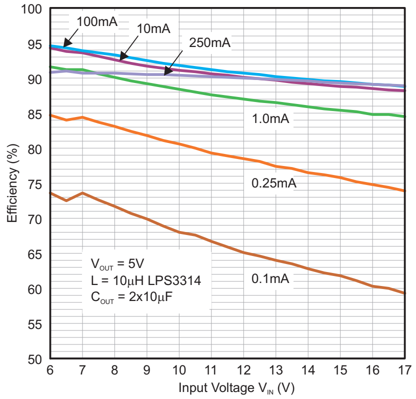


Figure 17. Efficiency vs. Input Voltage, V_{OUT} = 5 V

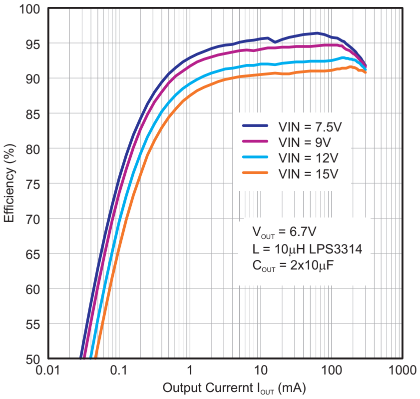


Figure 18. Efficiency vs. Output current, V_{OUT} = 6.8 V

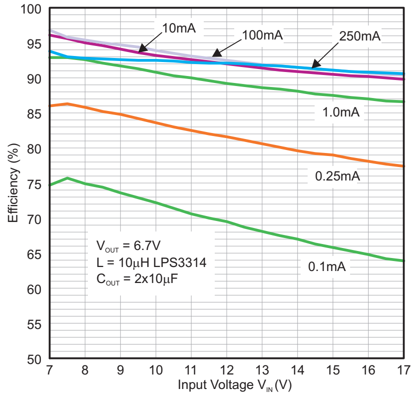


Figure 19. Efficiency vs. Input Voltage, V_{OUT} = 6.8 V

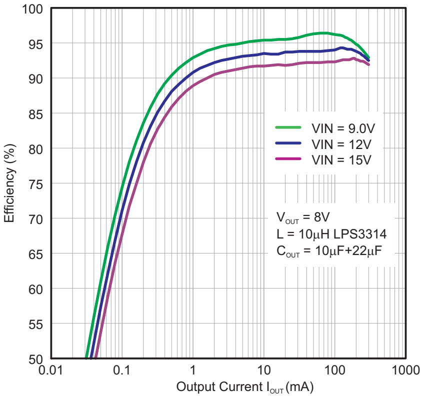


Figure 20. Efficiency vs. Output Current, V_{OUT} = 8 V

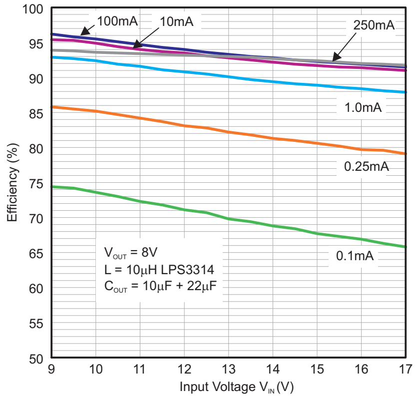


Figure 21. Efficiency vs. Input Voltage, V_{OUT} = 8 V

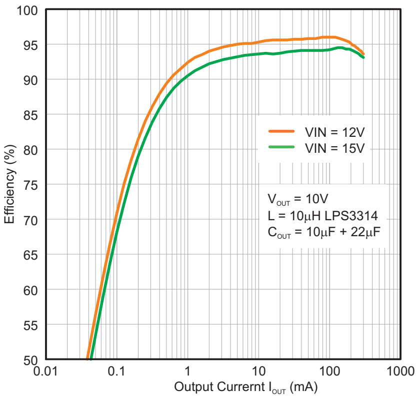


Figure 22. Efficiency vs. Output Current, V_{OUT} = 10 V

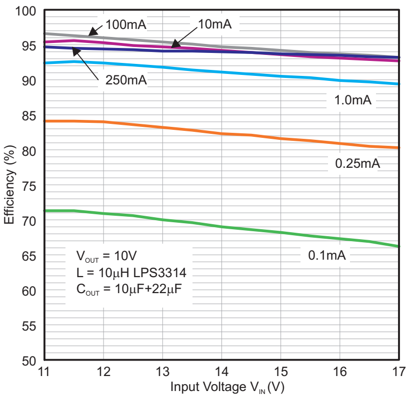


Figure 23. Efficiency vs. Input Voltage, V_{OUT} = 10 V

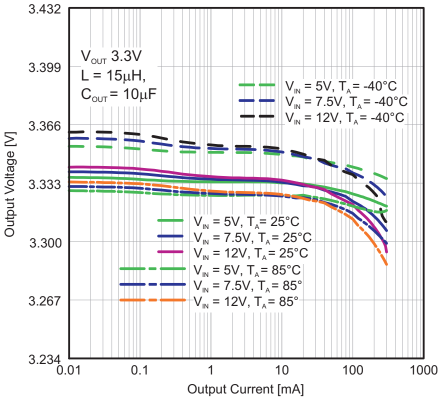


Figure 24. Output Voltage vs. Output Current, V_{OUT} = 3.3 V

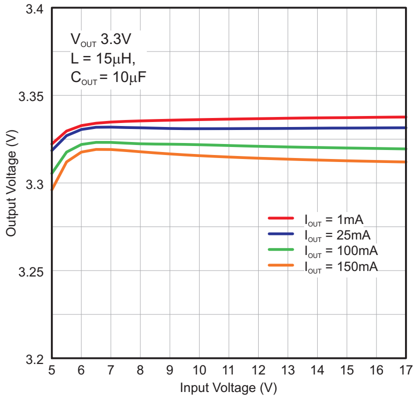


Figure 25. Output Voltage vs. Input Voltage, V_{OUT} = 3.3 V

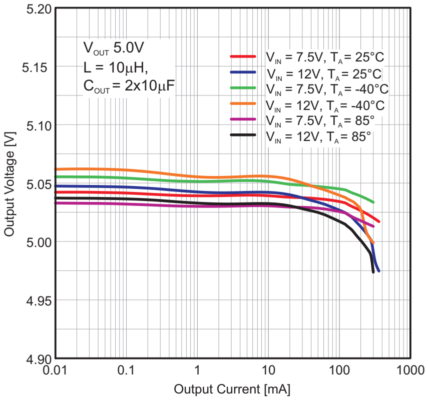


Figure 26. Output Voltage vs. Output current, V_{OUT} = 5 V

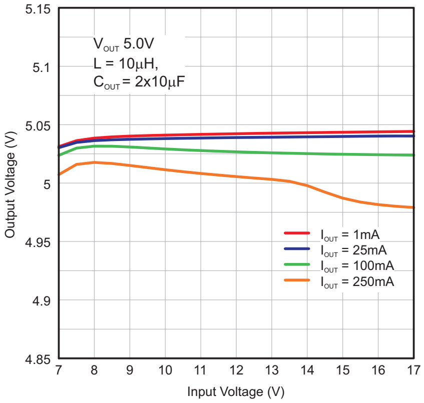


Figure 27. Output Voltage vs. Input Voltage, V_{OUT} = 5 V

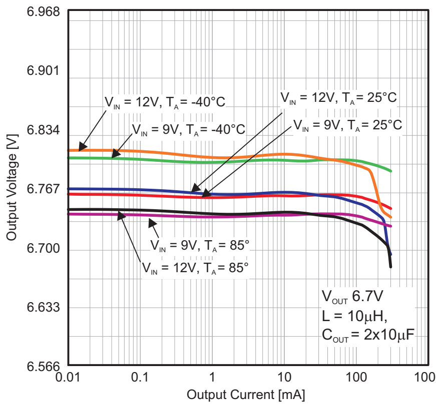


Figure 28. Output Voltage vs. Output Current, V_{OUT} = 6.7 V

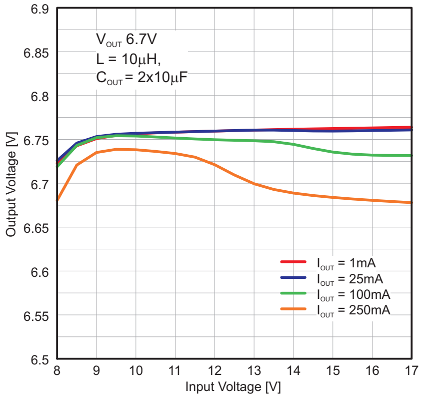


Figure 29. Output voltage vs. Input voltage, V_{OUT} = 6.7 V

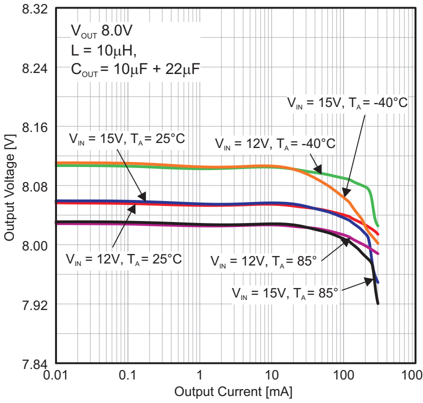


Figure 30. Output Voltage vs. Output Current, V_{OUT} = 8 V

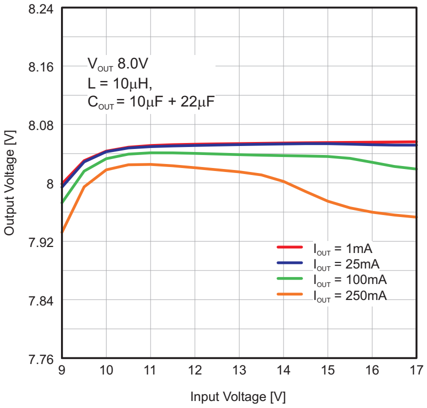


Figure 31. Output Voltage vs. Input Voltage, V_{OUT} = 8 V

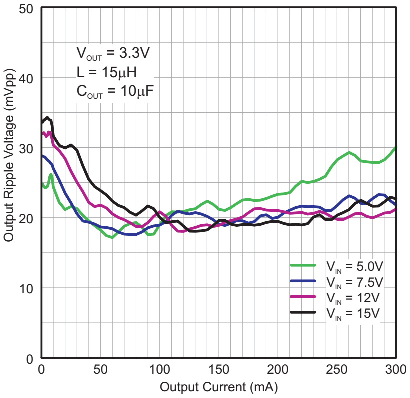


Figure 32. Output Ripple Voltage vs. Output Current, V_{OUT} = 3.3 V

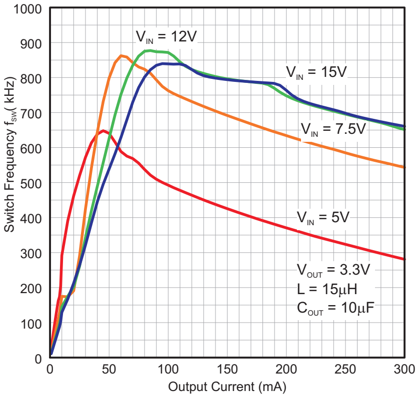


Figure 33. Switch Frequency vs. Output Current, V_{OUT} = 3.3 V

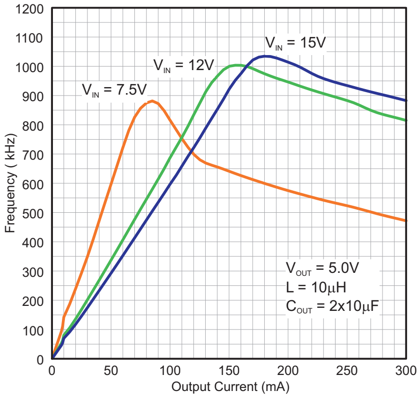


Figure 34. Switch Frequency vs. Output Current, V_{OUT} 5 V

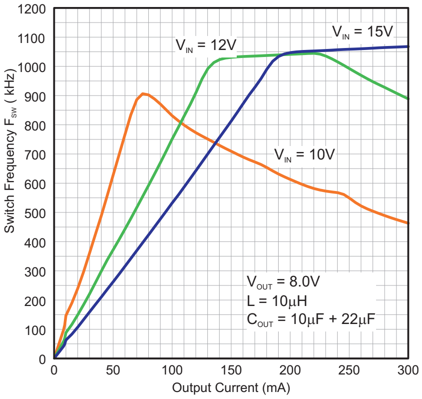


Figure 35. Switch Frequency vs. Output Current, V_{OUT} = 8 V

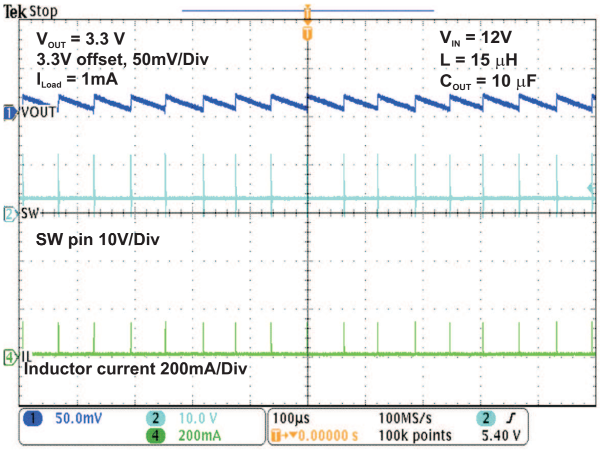


Figure 36. Power-Save Mode V_{OUT}= 3.3 V, I_{OUT} = 1 mA

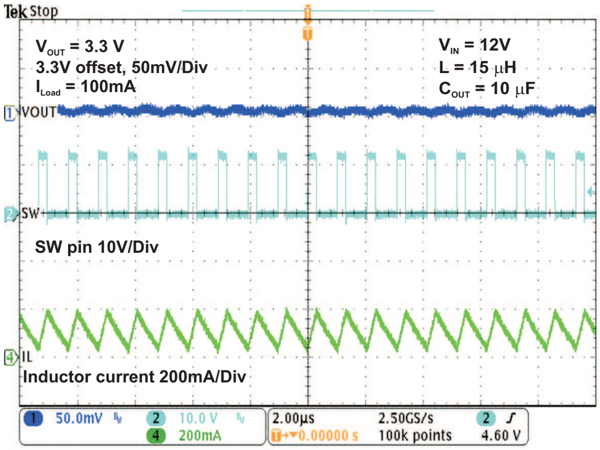


Figure 37. PWM Mode V_{OUT}= 3.3 V, I_{OUT} = 100 mA

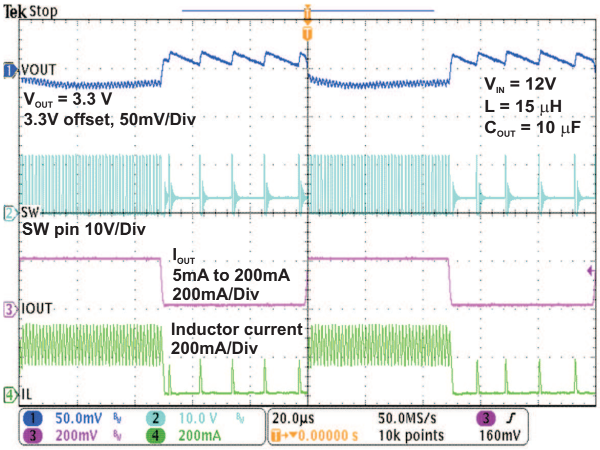


Figure 38. Load Transient 5 mA to 200 mA, V_{OUT} = 3.3 V

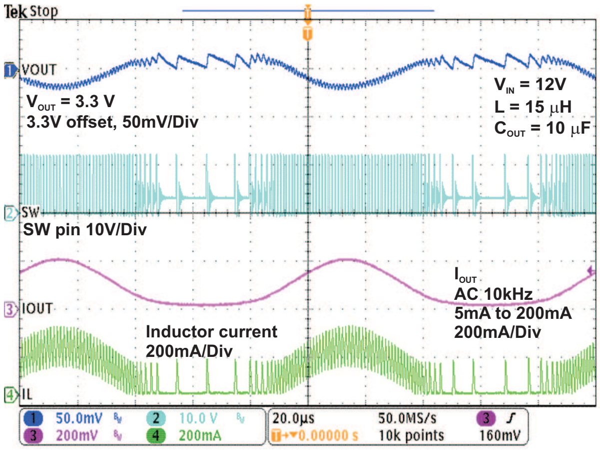


Figure 39. AC Load Regulation, V_{OUT} = 3.3 V

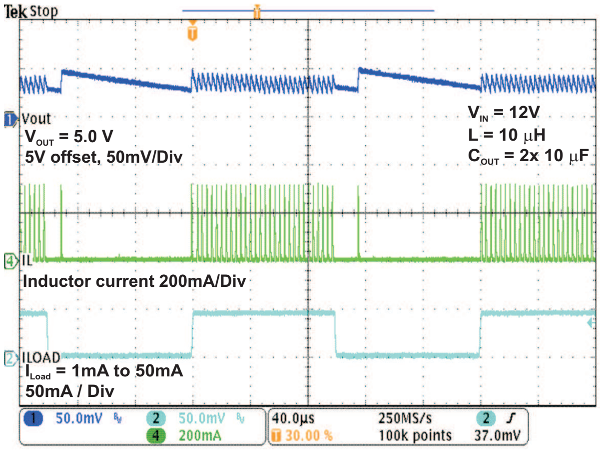


Figure 40. Load Transient 1 mA to 50 mA, V_{OUT} = 5 V

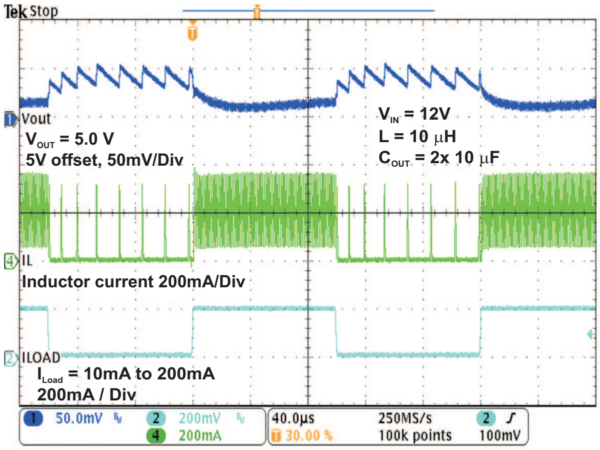


Figure 41. Load Transient 10 mA to 200 mA, V_{OUT} = 5 V

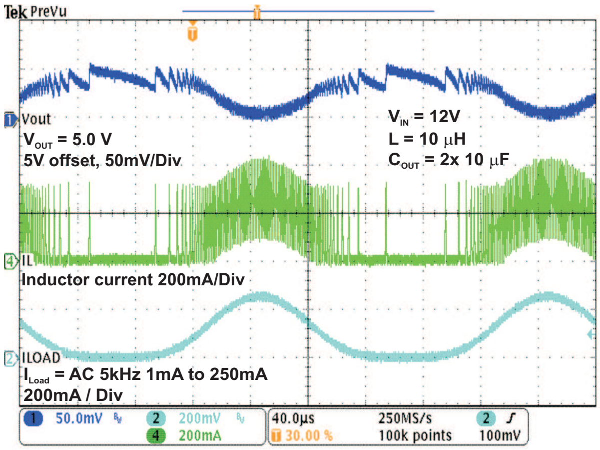


Figure 42. AC Load Regulation V_{OUT} = 5 V

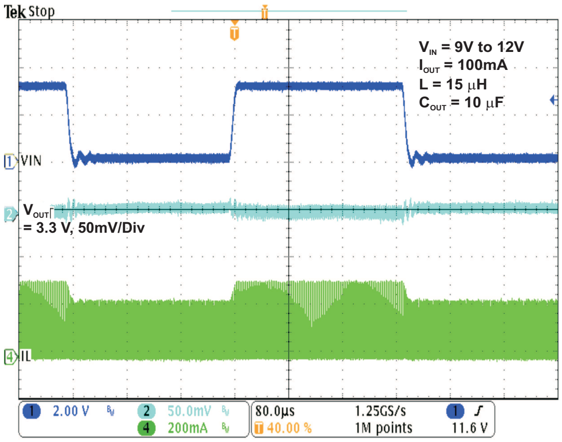


Figure 43. Line Transient Response V_{IN} = 9 V to 12 V

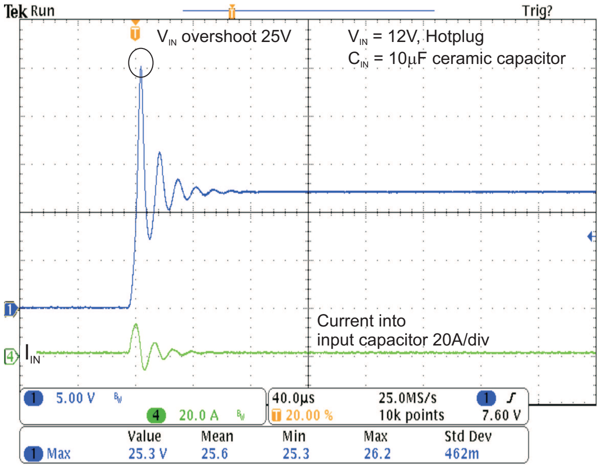


Figure 44. V_{IN} Hotplug Overshoot

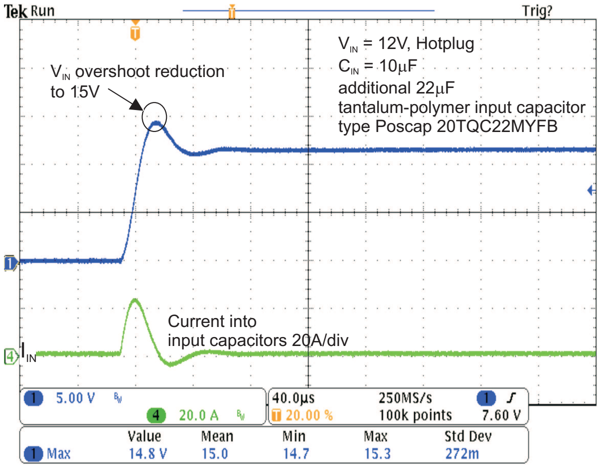


Figure 45. V_{IN} Hotplug Overshoot Reduction With Poscap

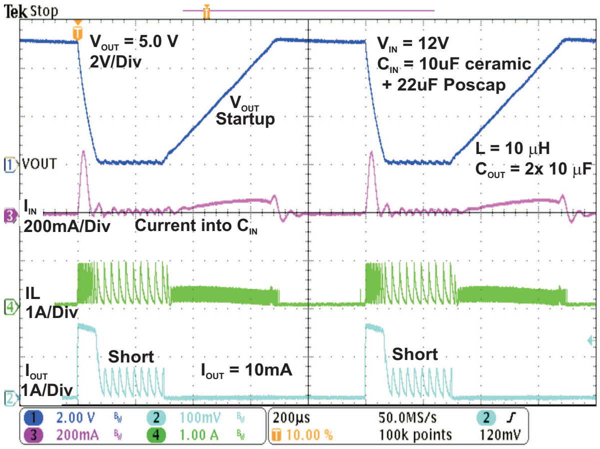


Figure 46. Short Circuit and Overcurrent Protection

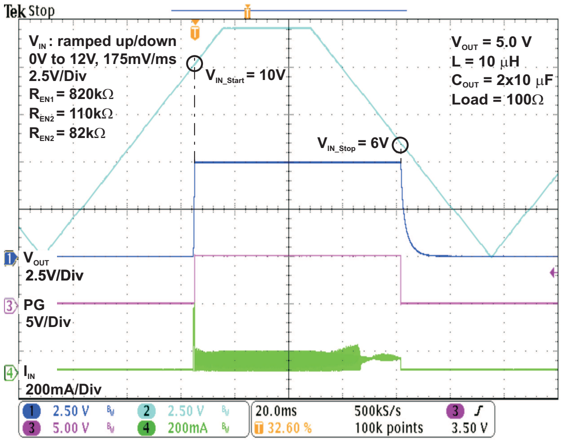


Figure 47. Input Supply Voltage Supervisor (SVS), V_{OUT} = 5 V

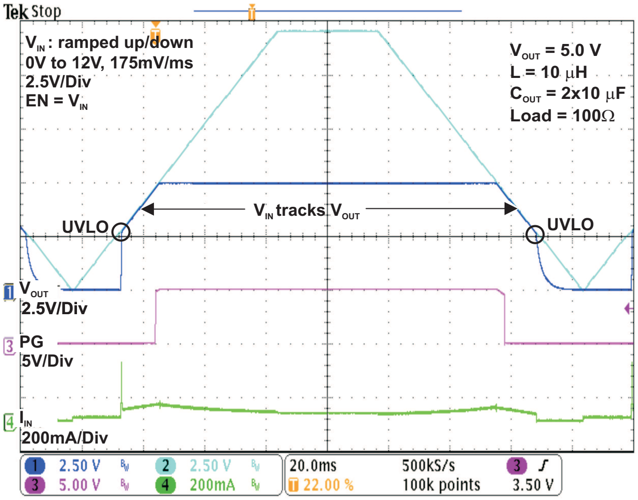


Figure 48. Operation With EN = V_{IN}, V_{IN} Tracks V_{OUT}

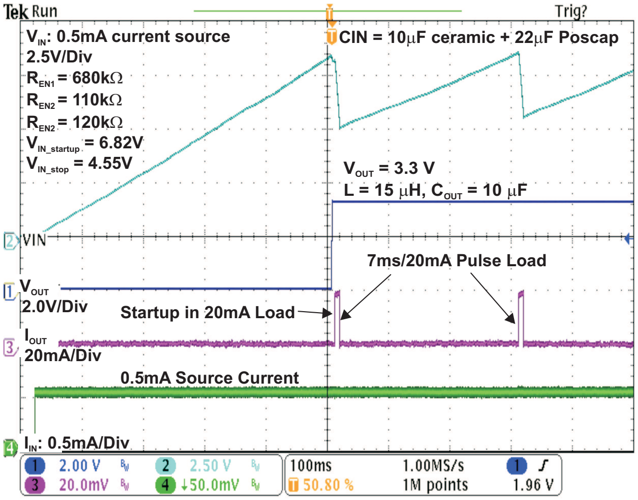


Figure 49. 0.5 mA Current Source, 20 mA Pulse Load

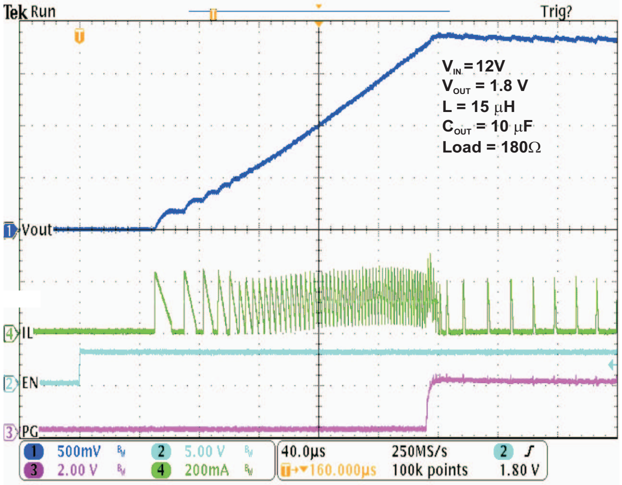


Figure 50. Start-Up 1.8 V V_{OUT}

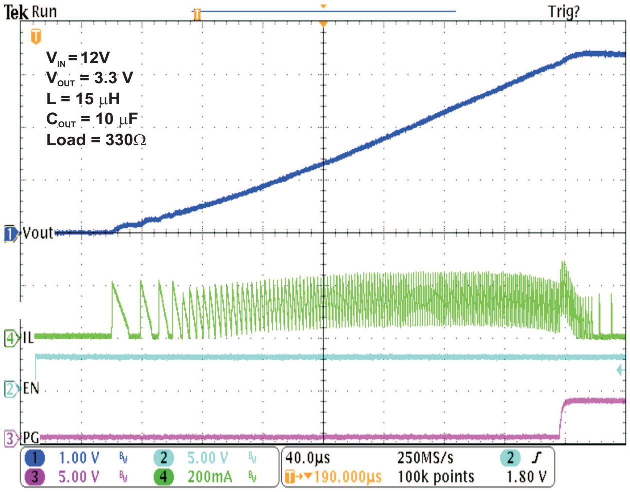


Figure 51. Start-Up 3.3 V V_{OUT}

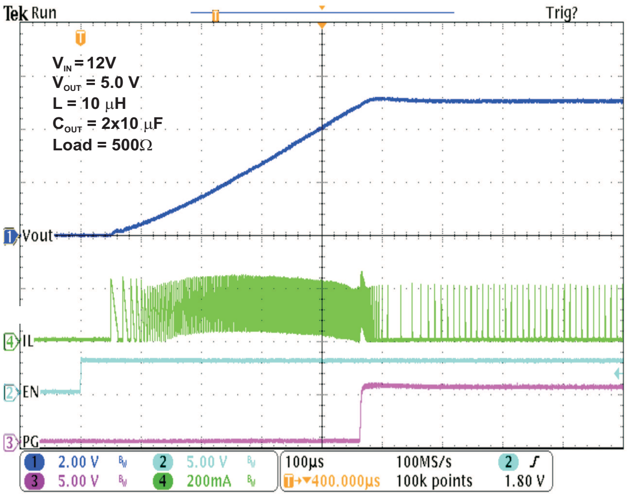


Figure 52. Start-Up 5 V V_{OUT}

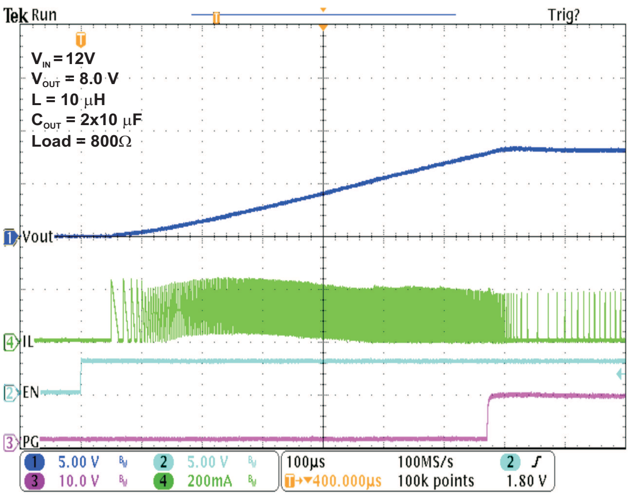


Figure 53. Start-Up 8 V V_{OUT}

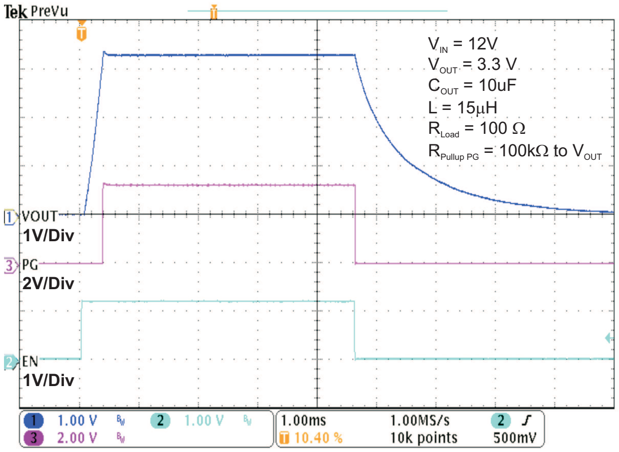


Figure 54. V_{OUT} Ramp Up/Down With EN On/Off

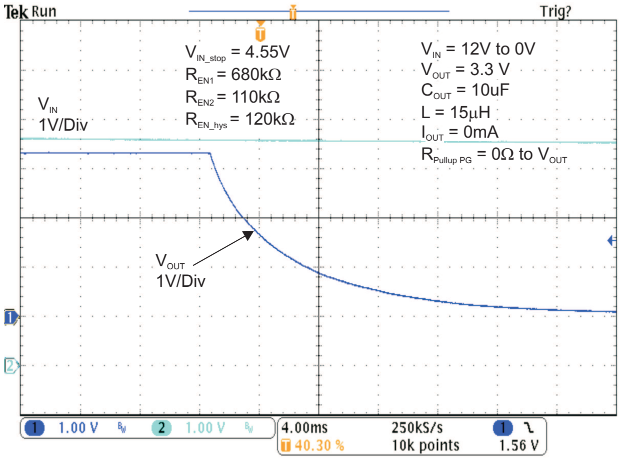


Figure 55. Output Discharge Using PG Pin, Triggered by EN Comparator

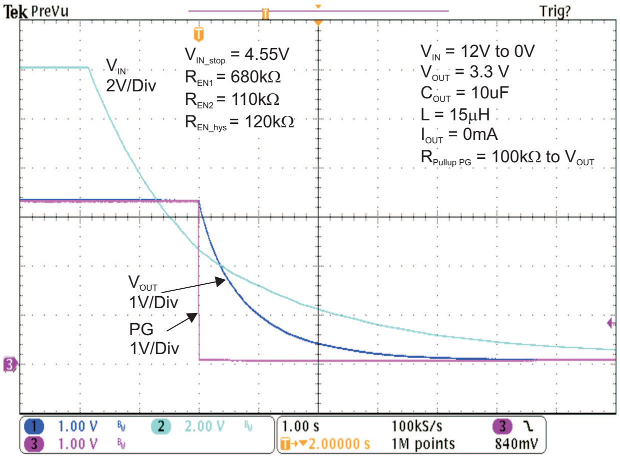


Figure 56. V_{OUT} Ramp Down With Falling V_{IN}, See Schematic Figure 59

8.3 System Examples

8.3.1 TPS62125 5-V Output Voltage Configuration

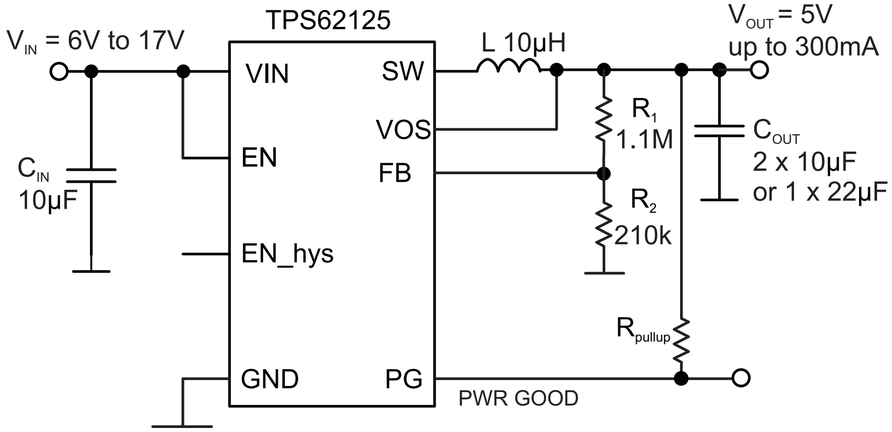


Figure 57. TPS62125 5-V Output Voltage Configuration

8.3.2 TPS62125 5-V V_{OUT}

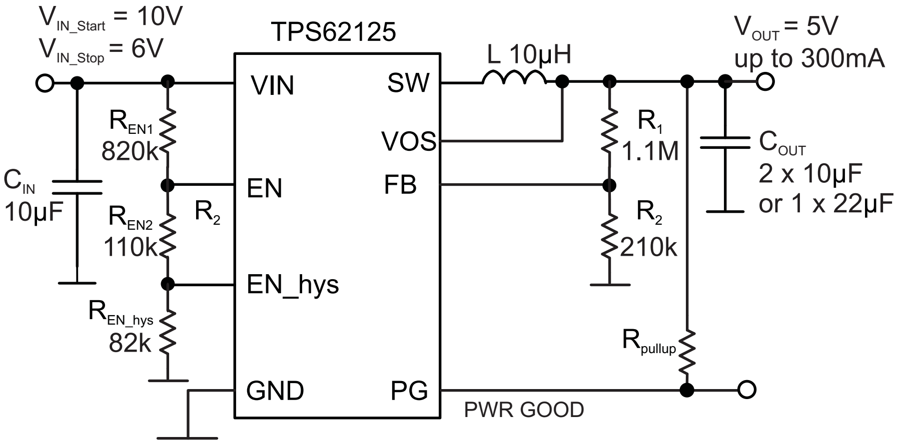


Figure 58. TPS62125 5-V V_{OUT}, Start-up Voltage V_{IN_Start} = 10 V, Stop Voltage V_{IN_Stop} = 6 V, See Figure 47

8.3.3 TPS62125 Operation From a Storage Capacitor Charged From a 0.5 mA Current Source

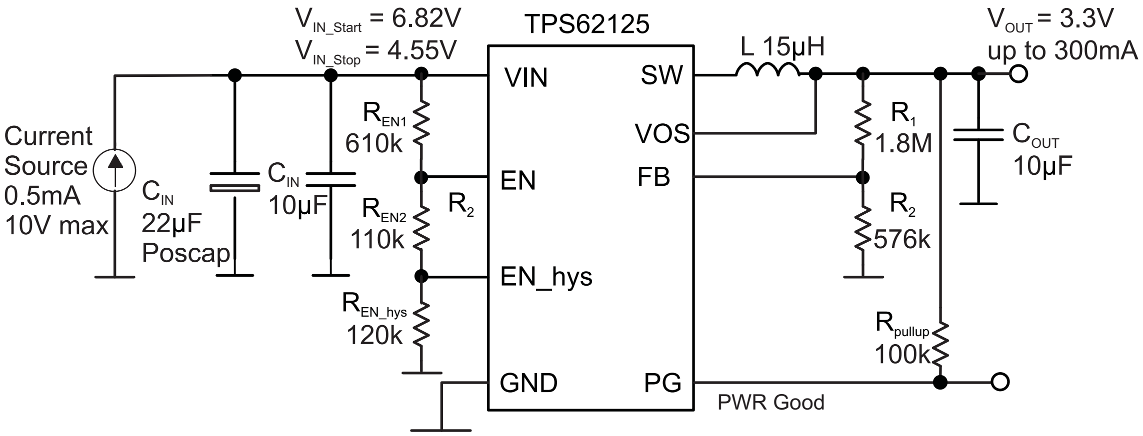


Figure 59. TPS62125 Operation From a Storage Capacitor Charged From a 0.5 mA Current Source, V_{OUT} = 3.3 V, See Figure 49

System Examples (continued)

8.3.4 5 V to –5 V Inverter Configuration

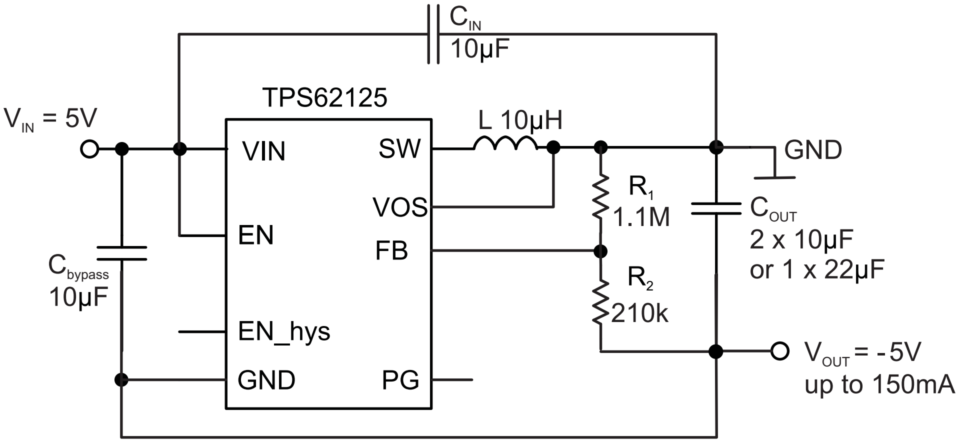


Figure 60. 5 V to –5 V Inverter Configuration, See SLVA514

9 Power Supply Recommendations

The TPS62125 has no special requirements for its input power supply. The input power supply's output current needs to be rated according to the supply voltage, output voltage, and output current of the TPS62125.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Take care in the board layout to get the specified performance. If the layout is not carefully done, the regulator could show frequency variations, poor line and/or load regulation, stability issues as well as EMI problems. It is critical to provide a low-inductance, low-impedance ground path. Therefore, use wide and short traces for the paths conducting AC current of the DC/DC converter. The area of the AC current loop (input capacitor – TPS62125 – inductor – output capacitor) should be routed as small as possible to avoid magnetic field radiation. Therefore the input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor. Use a common power GND node and a different node for the signal GND to minimize the effects of ground noise. Keep the common path to the GND pin, which returns both the small signal components and the high current of the output capacitors as short as possible to avoid ground noise. A well proven practice is to merge small signal GND and power GND path at the exposed thermal pad. The FB divider network and the FB line should be routed away from the inductor and the SW node to avoid noise coupling. The VOS line should be connected as short as possible to the output, ideally to the V_{OUT} terminal of the inductor. Keep the area of the loop VOS node – inductor – SW node small. The exposed thermal pad must be soldered to the circuit board for mechanical reliability and to achieve appropriate power dissipation.

10.2 Layout Example

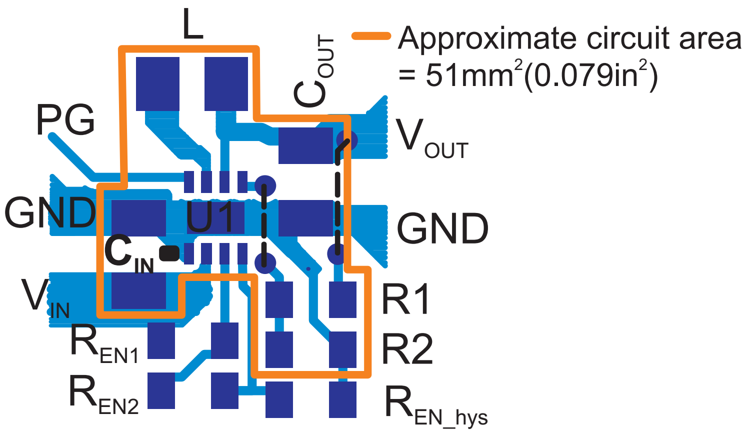


Figure 61. EVM Board Layout

11 器件和文档支持

11.1 器件支持

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设计支持	***TI* 参考设计支持** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

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这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62125DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SAQ
TPS62125DSGR.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SAQ
TPS62125DSGRG4	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SAQ
TPS62125DSGRG4.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SAQ
TPS62125DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SAQ
TPS62125DSGT.B	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SAQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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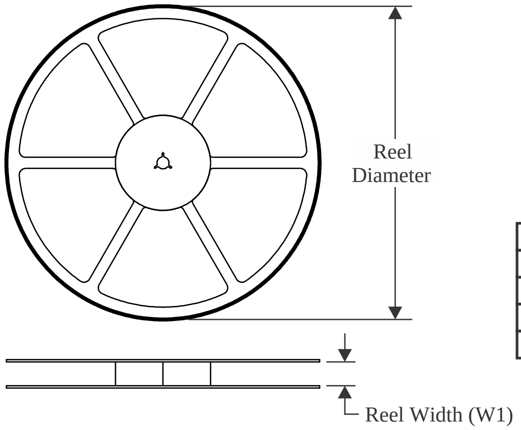
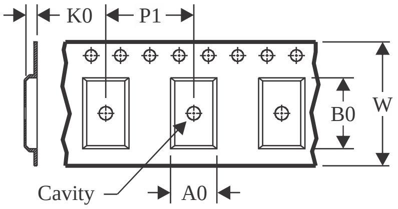
TAPE AND REEL INFORMATION

REEL DIMENSIONS

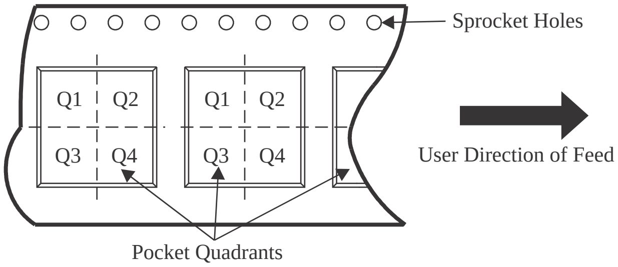


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

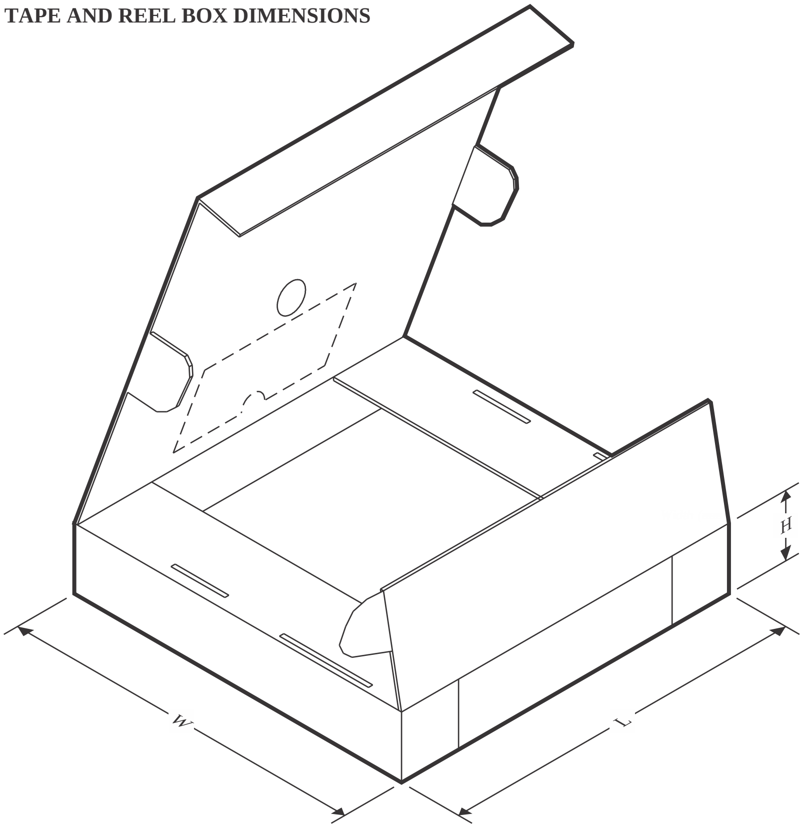
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62125DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62125DSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62125DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62125DSGR	WSON	DSG	8	3000	213.0	191.0	35.0
TPS62125DSGRG4	WSON	DSG	8	3000	213.0	191.0	35.0
TPS62125DSGT	WSON	DSG	8	250	213.0	191.0	35.0

GENERIC PACKAGE VIEW

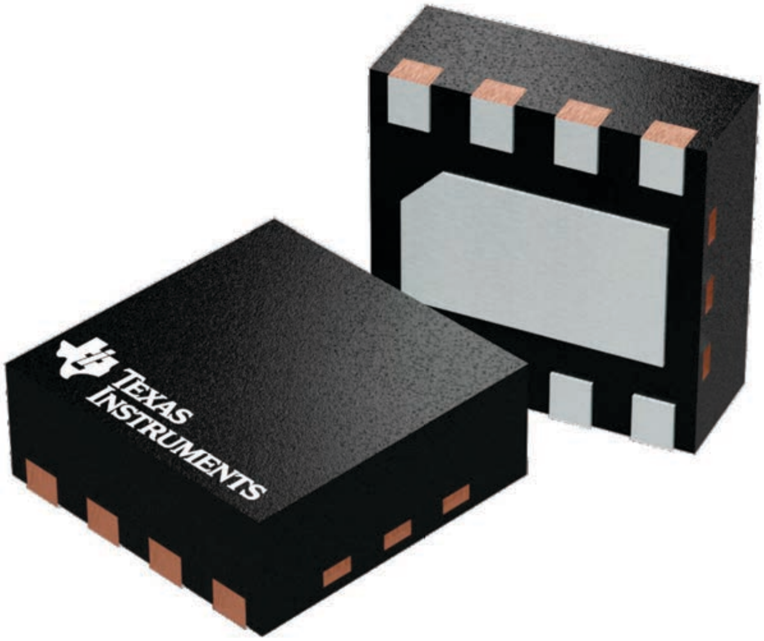
DSG 8

WSON - 0.8 mm max height

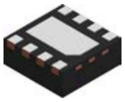
2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224783/A

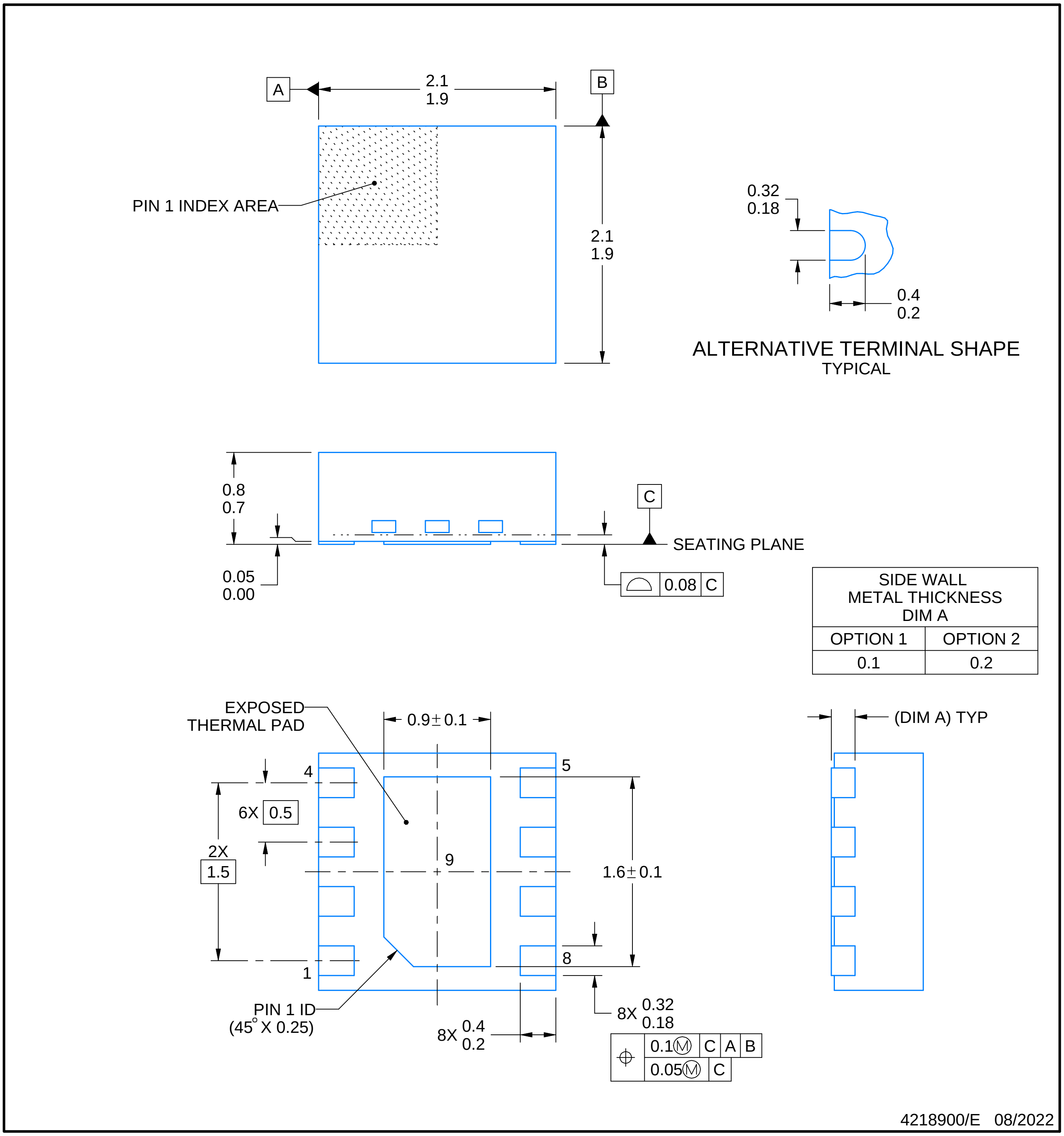


PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

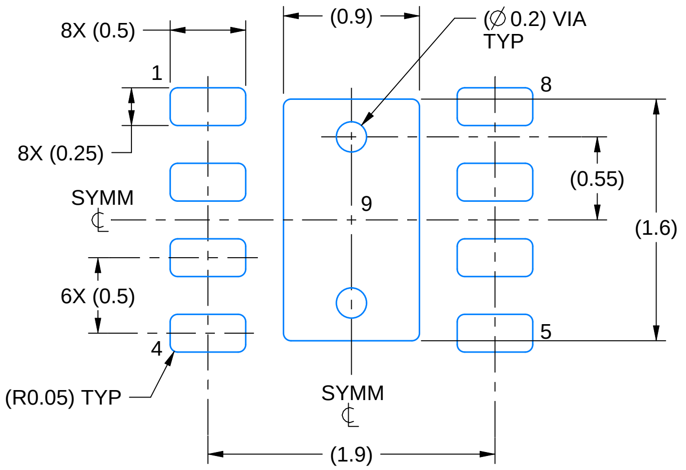


SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

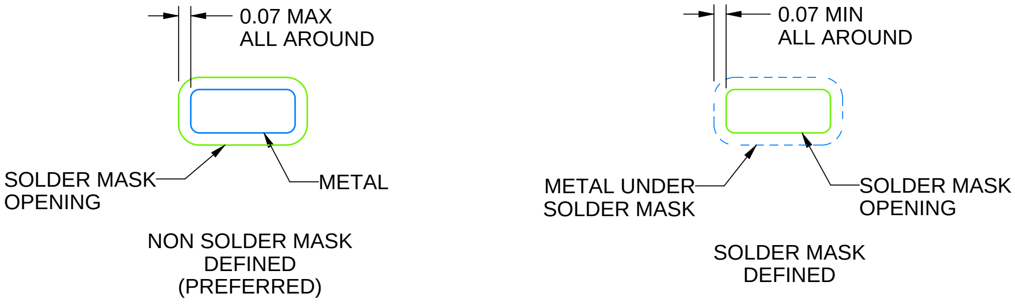
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



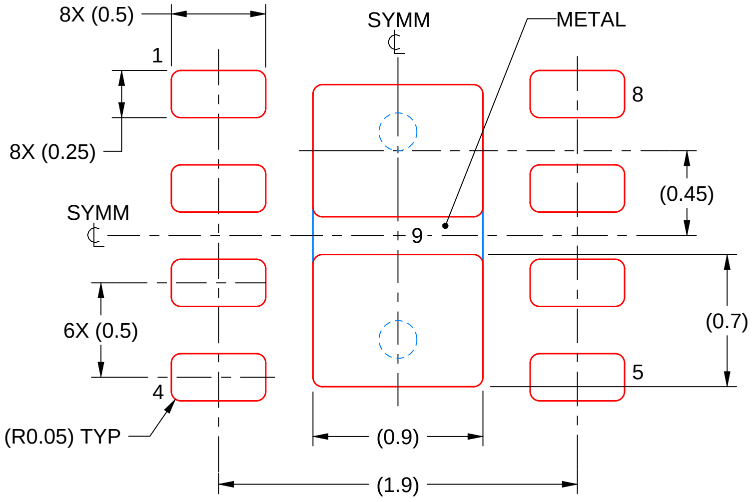
LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

最后更新日期：2025 年 10 月