TEXAS INSTRUMENTS
TPS61169
ZHCSD24B – OCTOBER 2014 – REVISED JUNE 2024

TPS61169 采用 PWM 控制的 38V 高电流升压 WLED 驱动器

1 特性

- 2.7V 至 5.5V 输入电压
- 集成 40V、1.8A MOSFET
- 驱动高达 38V 的 LED 灯串
- 1.2A 最小开关电流限制
- 1.2MHz 开关频率
- 204mV 基准电压
- 内部补偿
- PWM 亮度控制
- LED 开路保护
- 欠压保护
- 内置软启动
- 热关断
- 效率高达 90%

2 应用

- 智能手机背光照明
- 平板电脑背光照明
- PDA、掌上电脑、GPS 接收器
- 便携式媒体播放器、便携式电视
- 适合小尺寸和中等尺寸显示屏的白色 LED 背光照明
- 手持式数据终端 (EPOS)
- 手持式医疗设备
- 恒温器显示屏
- 血糖仪
- 闪光灯
- 冰箱和冷冻柜

3 说明

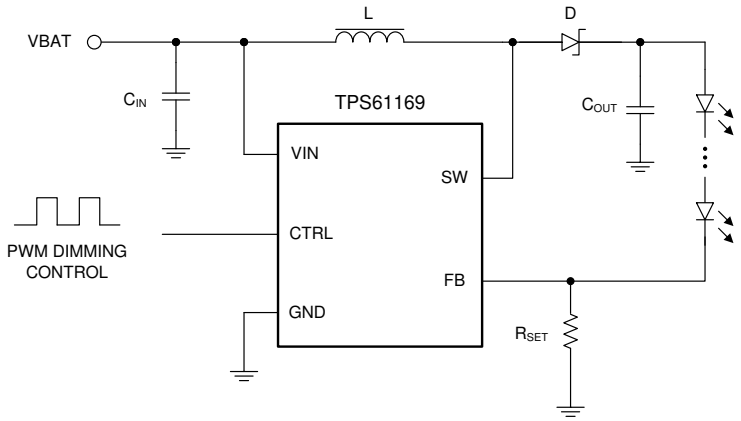
TPS61169 配备额定电压为 40V 的集成开关 FET，是一款可驱动串联 LED 的升压转换器。该升压转换器具有一个 40V、1.8A 内部 MOSFET，最低电流限值为 1.2A，可针对小型至大型面板背光照明驱动单个 LED 或并联 LED 灯串。如*简化原理图* 中所示，默认白光 LED 电流通过外部传感器电阻 R_{SET} 进行设置，反馈电压被调节至 204mV。运行期间，LED 电流可通过施加到 CTRL 引脚上的脉宽调制 (PWM) 信号加以控制，该信号的占空比决定反馈基准电压。TPS61169 不会突发 LED 电流，因此不会在输出电容器上产生可闻噪声。为提供最佳保护，该器件配备集成的 LED 开路保护，即在 LED 开路状态下禁用 TPS61169，以防止输出电压超过器件的最大绝对电压额定值。

TPS61169 采用节省空间的 5 引脚 SC70 封装。

器件信息(1)

器件型号	封装	本体尺寸 (标称值)
TPS61169	SOT (5)	2.00mm × 1.25mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化原理图

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4 Pin Configuration and Functions

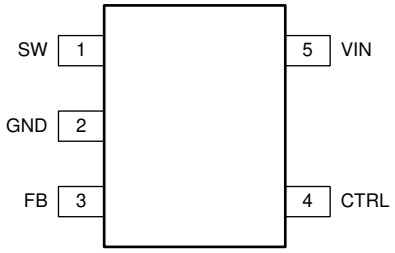


图 4-1. DCK Package 5-Pin SC70 (Top View)

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1	SW	I	Drain connection of the internal power FET.
2	GND	O	Ground
3	FB	I	Feedback pin for current. Connect the sense resistor from FB to GND.
4	CTRL	I	PWM dimming signal input
5	VIN	I	Supply input pin

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VIN, CTRL, PWM, FB	–0.3	7	V
	SW	–0.3	40	
P_D	Continuous power dissipation	See Thermal Information Table		
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7		5.5	V
V_{OUT}	Output voltage	V_{IN}		38	V
L	Inductor	4.7		10	µH
C_I	Input capacitor	1			µF
C_O	Output capacitor	1		10	µF
F_{PWM}	PWM dimming signal frequency	5		100	kHz
D_{PWM}	PWM dimming signal duty cycle	1%		100%	
T_J	Operating junction temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		TPS61169 DCK (SC70) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	263.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance(3)	76.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance(4)	51.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)	50.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

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(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).

5.5 Electrical Characteristics

Over operating free-air temperature range, V_{IN} = 3.6V, CTRL = V_{IN} (unless otherwise specified).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		2.7		5.5	V
V_{VIN_UVLO}	Undervoltage lockout threshold	V_{IN} falling V_{IN} rising		2	2.3 2.6	V
V_{VIN_HYS}	V_{IN} UVLO hysteresis			200		mV
I_{Q_VIN}	Operating quiescent current into V_{IN}	Device enable, switching 1.2MHz and no load,		0.3	0.45	mA
I_{SD}	Shutdown current	CTRL = GND		1	2	μA
CONTROL LOGIC AND TIMING						
V_H	CTRL Logic high voltage		1.2			V
V_L	CTRL Logic Low voltage				0.4	V
R_{PD}	CTRL pin internal pull-down resistor			300		KΩ
t_{SD}	CTRL logic low time to shutdown	CTRL high to low			2.5	ms
VOLTAGE AND CURRENT REGULATION						
V_{REF}	Voltage feedback regulation voltage	Duty = 100%, $T_A \geqslant 25°C$	188	204	220	mV
I_{FB}	FB pin bias current	V_{FB} = 204mV			2.5	μA
t_{REF}	V_{REF} filter time constant			1		ms
POWER SWITCH						
$R_{DS(ON)}$	N-channel MOSFET on-resistance			0.35	0.7	Ω
I_{LN_NFET}	N-channel leakage current	V_{SW} = 35V			1	μA
SWITCHING FREQUENCY						
f_{SW}	Switching frequency	V_{IN} = 3V	0.75	1.2	1.5	MHz
PROTECTION AND SOFT START						
I_{LIM}	Switching MOSFET current limit	D = D_{MAX} , $T_A \leqslant 85°C$	1.2	1.8	2.4	A
I_{LIM_Start}	Switching MOSFET start-up current limit	$T_A \leqslant 85°C$		0.72		A
t_{Half_LIM}	Time step for half current limit			6.5		ms
V_{OVP_SW}	Output voltage overvoltage threshold		36	37.5	39	V
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			160		°C
T_{hys}	Thermal shutdown hysteresis			15		°C

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5.6 Typical Characteristics

At T_A = 25°C, unless otherwise noted.

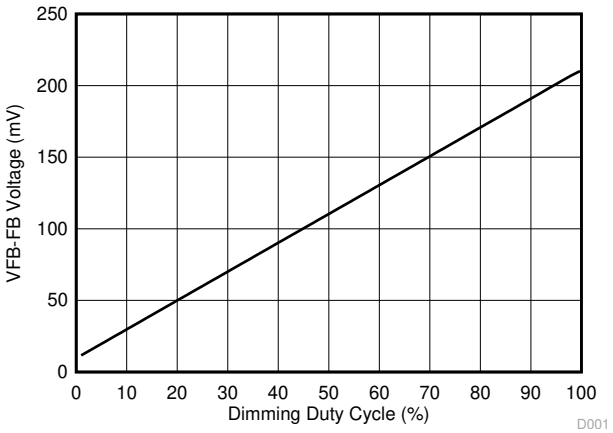


图 5-1. FB Voltage vs Dimming Duty Cycle

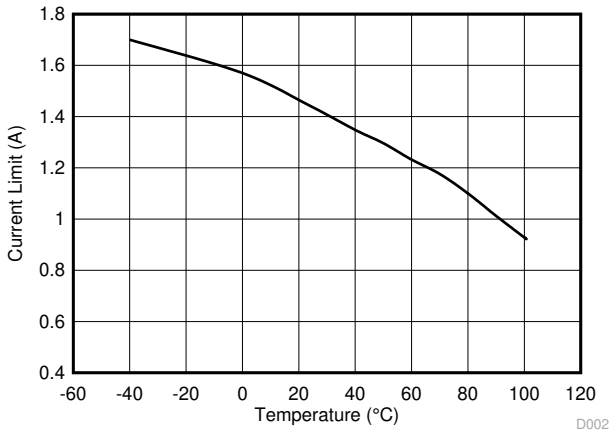


图 5-2. Current Limit vs Temperature

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6 Detailed Description

6.1 Overview

The TPS61169 is a high-efficiency, high-output voltage boost converter in small package size. The device integrates 40V/1.8A switch FET and is designed for output voltage up to 39V with a switch peak current limit of 1.2A minimum. Its large driving capability can drive single or parallel LED strings for small to large size panel backlighting.

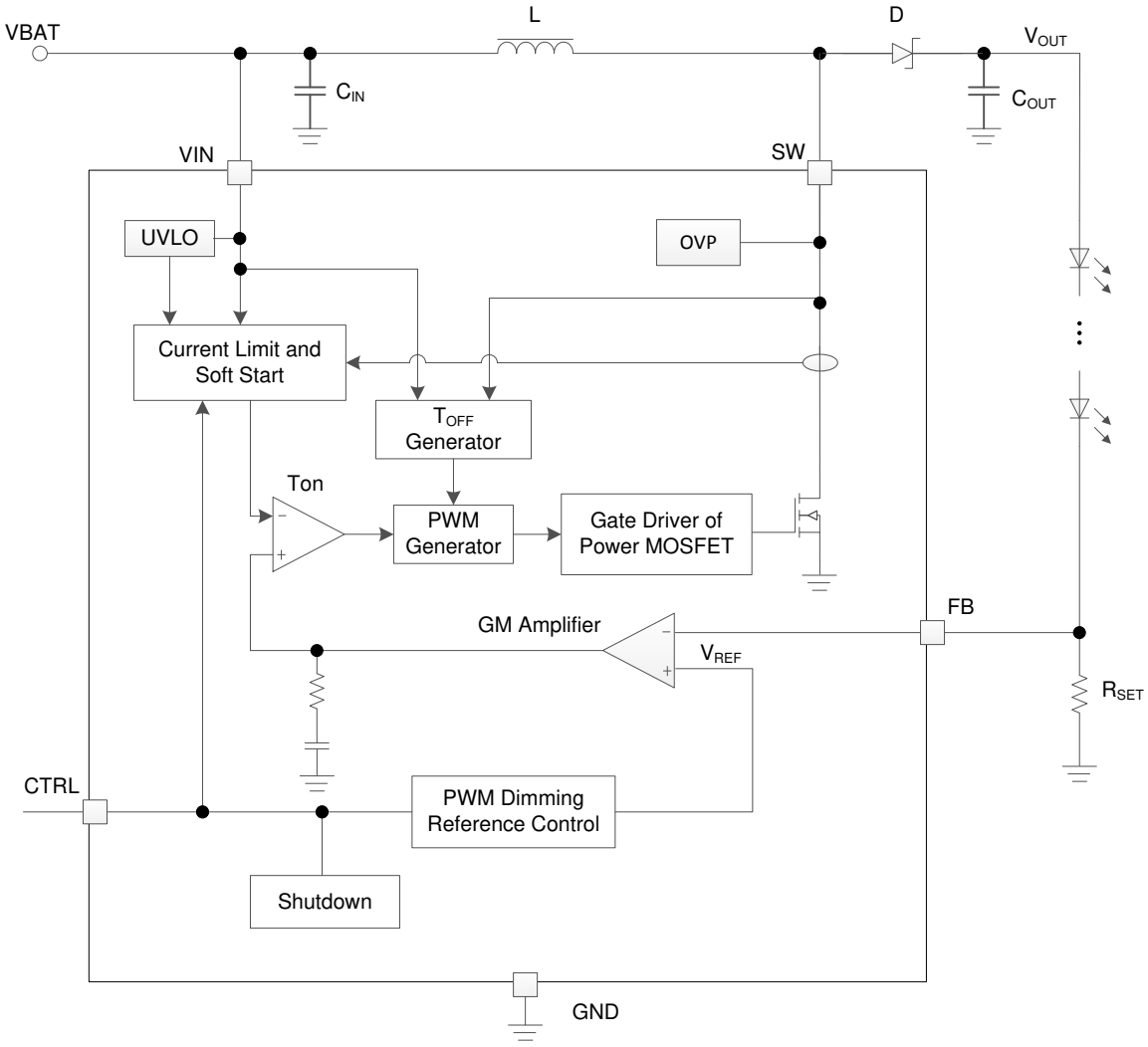
The TPS61169 operates in a current mode scheme with quasi-constant frequency. It is internally compensated for maximum flexibility and stability. The switching frequency is 1.2MHz, and the minimum input voltage is 2.7V. During the on-time, the current rises into the inductor. When the current reaches a threshold value set by the internal GM amplifier, the power switch MOSFET is turned off. The polarity of the inductor changes and forward biases the schottky diode which lets the current flow towards the output of the boost converter. The off-time is fixed for a certain V_{IN} and V_{OUT}, and therefore maintains the same frequency when varying these parameters.

However, for different output loads, the frequency slightly changes due to the voltage drop across the RDS(ON) of the power switch MOSFET, this has an effect on the voltage across the inductor and thus on t_{ON} (t_{OFF} remains fixed). The fixed off-time maintains a quasi-fixed frequency that provides better stability for the system over a wider range of input and output voltages than conventional boost converters. The TPS61169 topology has also the benefits of providing very good load and line regulations, and excellent line and load transient responses.

The feedback loop regulates the FB pin to a low reference voltage (204mV typical), reducing the power dissipation in the current sense resistor.

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6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Soft Start-Up

Soft-start circuitry is integrated into the device to avoid high inrush current spike during start-up. After the device is enabled, the GM amplifier output voltage ramps up very slowly, which ensures that the output voltage rises slowly to reduce the input current. During this period, the switch current limit is set to 0.72A. After around 6.5ms, the switch current limit changes back to I_{LIM}, and the FB pin voltage ramps up to the reference voltage slowly. These features ensure the smooth start-up and minimize the inrush current. See 图 7-9 for a typical example.

6.3.2 Open LED Protection

Open LED protection circuitry prevents the device from damage as the result of white LED disconnection. The TPS61169 monitors the voltage at the SW pin and FB pin during each switching cycle. The circuitry turns off the switch FET and shuts down the device when both of the following conditions persist for 3 switching cycles: (1) the SW voltage exceeds the VOVP threshold, and (2) the FB voltage is less than 30mV. As the result, the output voltage falls to the level of the input supply. The device remains in shutdown mode until it is enabled by toggling the CTRL pin.

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6.3.3 Shutdown

The TPS61169 enters shutdown mode when the CTRL voltage is logic low for more than 2.5ms. During shutdown, the input supply current for the device is less than 2 μA (max). Although the internal switch FET does not switch in shutdown, there is still a DC current path between the input and the LEDs through the inductor and Schottky diode. The minimum forward voltage of the LED array must exceed the maximum input voltage to ensure that the LEDs remain off in shutdown.

6.3.4 Current Program

The FB voltage is regulated by a low 204mV reference voltage. The LED current is programmed externally using a current-sense resistor in series with the LED string(s). The value of the R_{SET} is calculated using:

$$I_{LED} = \frac{V_{FB}}{R_{SET}} \quad (1)$$

where

- I_{LED} = total output current of LED string(s)
- V_{FB} = regulated voltage of FB pin
- R_{SET} = current sense resistor

The output current tolerance depends on the FB accuracy and the current sensor resistor accuracy.

6.3.5 LED Brightness Dimming

The TPS61169 receives PWM dimming signal at CTRL pin to control the total output current. When the CTRL pin is constantly high, the FB voltage is regulated to 204mV typically. When the duty cycle of the input PWM signal is low, the regulation voltage at FB pin is reduced, and the total output current is reduced; therefore, it achieves LED brightness dimming. The relationship between the duty cycle and FB regulation voltage is given by:

$$V_{FB} = Duty \times 204\ mV \quad (2)$$

where

- Duty = Duty cycle of the PWM signal
- 204mV = internal reference voltage

Thus, the user can easily control the WLED brightness by controlling the duty cycle of the PWM signal.

As shown in 图 6-1, the device chops up the internal 204mV reference voltage at the duty cycle of the PWM signal. The pulse signal is then filtered by an internal low-pass filter. The output of the filter is connected to the GM amplifier as the reference voltage for the FB pin regulation. Therefore, although a PWM signal is used for brightness dimming, only the WLED DC current is modulated, which is often referred as analog dimming. This eliminates the audible noise which often occurs when the LED current is pulsed in replica of the frequency and duty cycle of PWM control. Unlike other methods which filter the PWM signal for analog dimming, TPS61169 regulation voltage is independent of the PWM logic voltage level which often has large variations.

For optimum performance, use the PWM dimming frequency in the range of 5kHz to 100kHz. If the PWM frequency is lower than 5kHz, it is out of the low pass filter's filter range, the FB regulation voltage ripple becomes large, causing large output ripple and may generate audible noise.

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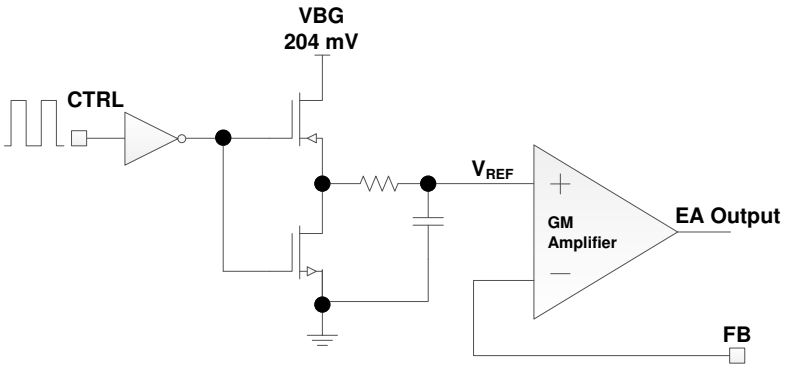


图 6-1. Programmable FB Voltage Using PWM Signal

6.3.6 Undervoltage Lockout

An undervoltage lockout prevents operation of the device at input voltages below typical 2V. When the input voltage is below the undervoltage threshold, the device is shut down, and the internal switch FET is turned off. If the input voltage rises by undervoltage lockout hysteresis, the device restarts.

6.3.7 Thermal Foldback and Thermal Shutdown

When TPS61169 drives heavy load for large size panel applications, the power dissipation increases a lot and the device junction temperature may reach a very high value, affecting the device function and reliability. In order to lower the thermal stress, the TPS61169 features a thermal foldback function. When the junction temperature is higher than 100°C, the switch current limit I_{LIM} is reduced automatically as 图 5-2 shows. This thermal foldback mechanism controls the power dissipation and keeps the junction temperature from rising to a very high value. If the typical junction temperature of 160°C is exceeded, an internal thermal shutdown turns off the device. The device is released from shutdown automatically when the junction temperature decreases by 15°C.

6.4 Device Functional Modes

6.4.1 Operation With CTRL

The enable rising edge threshold voltage is 1.2V. When the CTRL pin is held below that voltage the device is disabled and switching is inhibited. The the device's quiescent current is reduced in this state. When input voltage is above the UVLO threshold, and the CTRL pin voltage is increased above the rising edge threshold, the device becomes active. Switching enables, and the soft-start sequence initiates.

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7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

The TPS61169 device is a step-up DC-DC converter which can drive single or parallel LED strings for small- to large-size panel backlighting. This section includes a design procedure (*Detailed Design Procedure*) to select component values for the TPS61169 typical application (图 7-1).

7.2 Typical Application

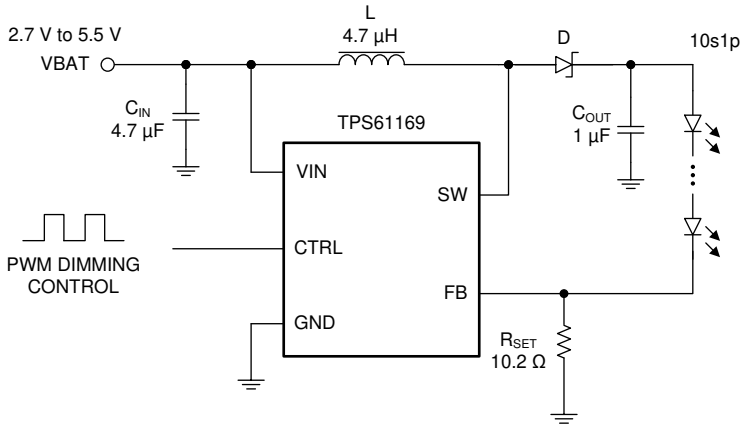


图 7-1. TPS61169 2.7V to 5.5V Input, 10 LEDs in Series Output Converter

7.2.1 Design Requirements

For this design example, use the parameters listed in 表 7-1 as the input parameters.

表 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.7V to 5.5V
Output, LED number in a string	10
Output, LED string number	1
Output, LED current per string	20mA

7.2.2 Detailed Design Procedure

7.2.2.1 Inductor Selection

The selection of the inductor affects power efficiency, steady state operation as well as transient behavior and loop stability. These factors make it the most important component in power regulator design. There are three important inductor specifications, inductor value, DC resistance and saturation current. Considering inductor value alone is not enough. The inductor value determines the inductor ripple current. Choose an inductor that can handle the necessary peak current without saturating. Follow 方程式 3 to 方程式 4 to calculate the peak current of the inductor. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage and maximum load current of application. In a boost regulator, the input DC current can be calculated as 方程式 3.

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$$I_{L(DC)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (3)$$

where

- V_{OUT} = boost output voltage
- I_{OUT} = boost output current
- V_{IN} = boost input voltage
- η = power conversion efficiency

The inductor current peak to peak ripple can be calculated as 方程式 4.

$$\Delta I_{L(P-P)} = \frac{1}{L \times \left(\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}}\right) \times F_S} \quad (4)$$

where

- $\Delta I_{L(PP)}$ = inductor peak-to-peak ripple
- L = inductor value
- F_S = boost switching frequency
- V_{OUT} = boost output voltage
- V_{IN} = boost input voltage

Therefore, the peak current $I_{L(P)}$ seen by the inductor is calculated with 方程式 5.

$$I_{L(P)} = I_{L(DC)} + \frac{\Delta I_{L(P-P)}}{2} \quad (5)$$

Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0A value depending on how the inductor vendor defines saturation current. Using an inductor with a smaller inductance value forces discontinuous PWM when the inductor current ramps down to zero before the end of each switching cycle. This reduces the boost converter's maximum output current, causes large input voltage ripple and reduces efficiency. Large inductance value provides much more output current and higher conversion efficiency. For these reasons, a 4.7 µH to 10 µH inductor value range is recommended, and 4.7 µH inductor is recommended for higher than 5V input voltage by considering inductor peak current and loop stability. 表 7-2 lists the recommended inductor for the TPS61169.

表 7-2. Recommended Inductors for TPS61169

PART NUMBER	L (µH)	DCR MAX (mΩ)	SATURATION CURRENT (A)	SIZE (L x W x H mm)	VENDOR
LPS4018-472ML	4.7	125	1.9	4 × 4 × 1.8	Coilcraft
LPS4018-103ML	10	200	1.3	4 × 4 × 1.8	Coilcraft
PCMB051H-4R7M	4.7	85	4	5.4 × 5.2 × 1.8	Cyntec
PCMB051H-100M	10	155	3	5.4 × 5.2 × 1.8	Cyntec

7.2.2.2 Schottky Diode Selection

The TPS61169 demands a low forward voltage, high-speed and low capacitance Schottky diode for optimum efficiency. Ensure that the diode average and peak current rating exceeds the average output current and peak inductor current. In addition, the diode reverse breakdown voltage must exceed the open LED protection voltage. ONSemi NSR0240 is recommended for the TPS61169.

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7.2.2.3 Output Capacitor Selection

The output capacitor is mainly selected to meet the requirement for the output ripple and loop stability. This ripple voltage is related to capacitor capacitance and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated with 方程式 6:

$$C_{OUT} = \frac{(V_{OUT} - V_{IN}) \times I_{OUT}}{V_{OUT} \times F_S \times V_{ripple}} \quad (6)$$

where

- V_{ripple} = peak-to-peak output ripple

The additional part of the ripple caused by ESR is calculated using: $V_{ripple_ESR} = I_{OUT} \times R_{ESR}$

Due to its low ESR, V_{ripple_ESR} could be neglected for ceramic capacitors, a 1μF to 4.7μF capacitor is recommended for typical application.

7.2.2.4 LED Current Set Resistor

The LED current set resistor can be calculated by 方程式 1.

7.2.2.5 Thermal Considerations

The allowable IC junction temperature must be considered under normal operating conditions. This restriction limits the power dissipation of the TPS61169. The allowable power dissipation for the device can be determined by 方程式 7:

$$P_D = \frac{T_J - T_A}{R_{\theta JA}} \quad (7)$$

where

- T_J is allowable junction temperature given in recommended operating conditions
- T_A is the ambient temperature for the application
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient given in Power Dissipation Table

The TPS61169 device also features a thermal foldback function to reduce the thermal stress automatically.

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7.3 Application Curves

Typical application condition is as in 图 7-1, V_{IN} = 3.6V, R_{SET} = 10.2Ω, L = 4.7µH, C_{OUT} = 1µF, 10 LEDs in series (unless otherwise specified).

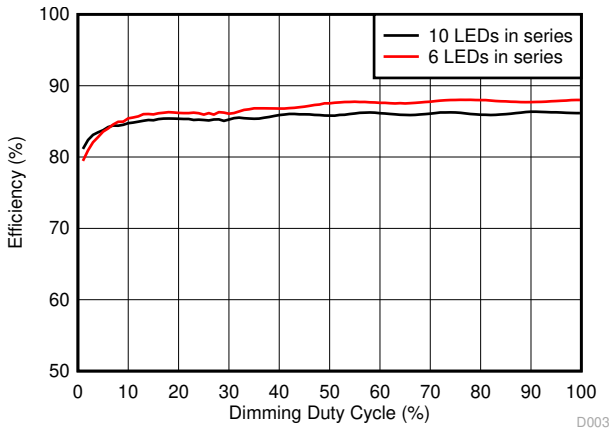
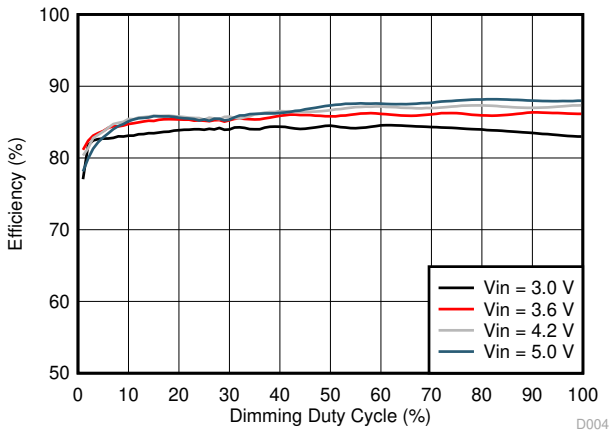
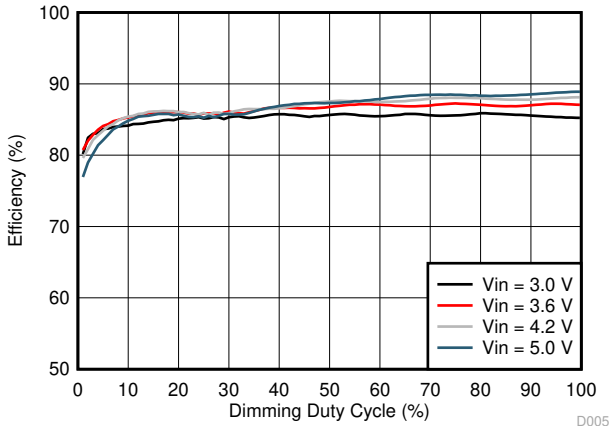


图 7-2. Efficiency vs Dimming Duty Cycle



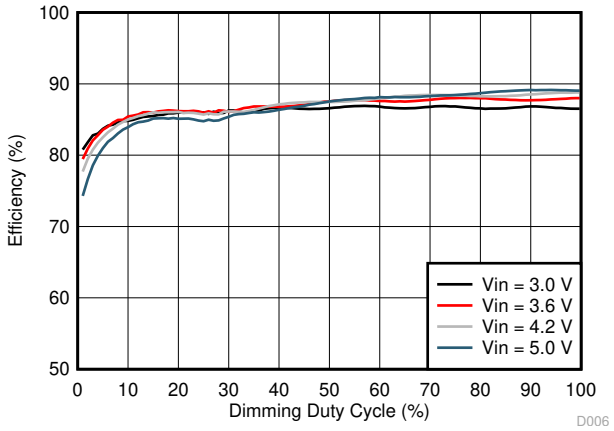
10 LEDs in series

图 7-3. Efficiency vs Dimming Duty Cycle



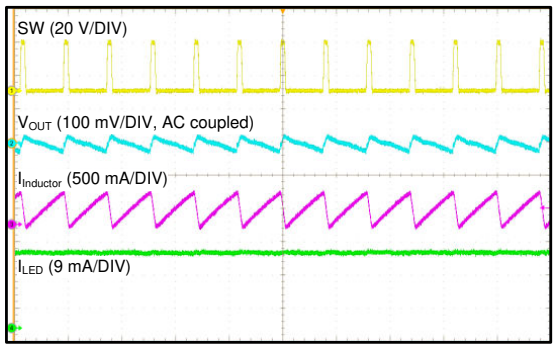
8 LEDs in series

图 7-4. Efficiency vs Dimming Duty Cycle



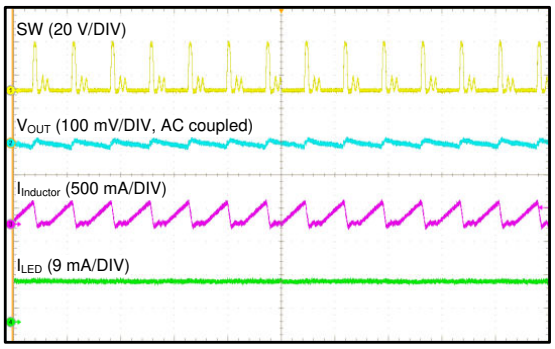
6 LEDs in series

图 7-5. Efficiency vs Dimming Duty Cycle



Time = 1µs/DIV

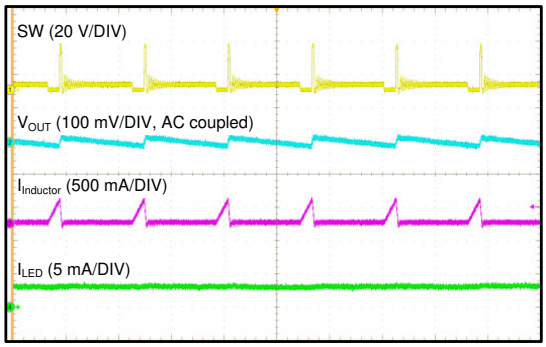
图 7-6. Switching-Dimming Duty = 100%



Time = 1µs/DIV

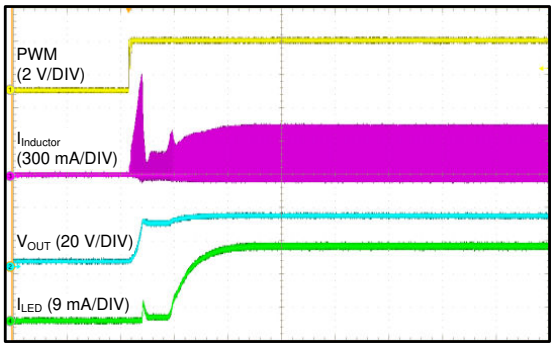
图 7-7. Switching-Dimming Duty = 50%

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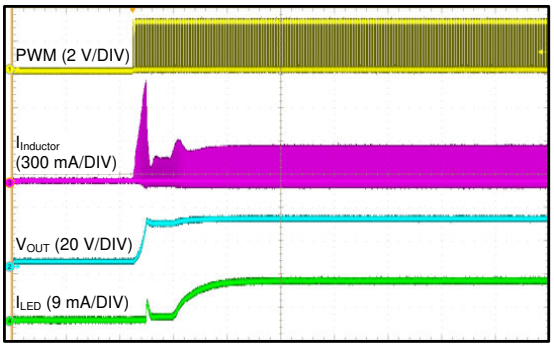
Time = 2µs/DIV

图 7-8. Switching-Dimming Duty = 10%



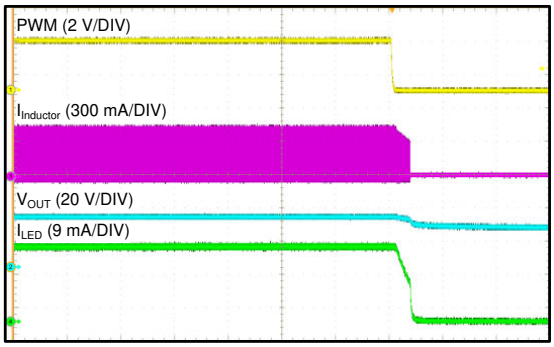
Time = 2ms/DIV

图 7-9. Start-Up Dimming Duty = 100%



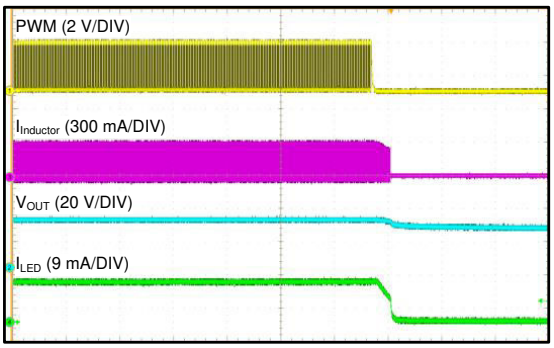
Time = 2ms/DIV

图 7-10. Start-Up Dimming Duty = 50%



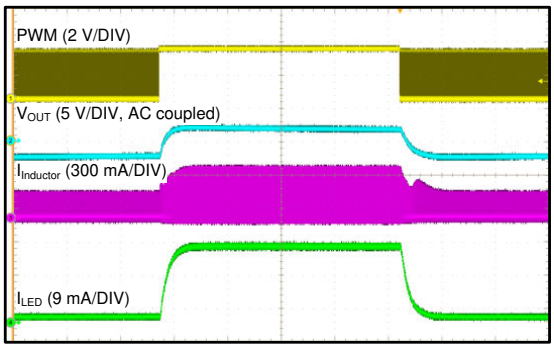
Time = 2ms/DIV

图 7-11. Shutdown Dimming Duty = 100%



Time = 2ms/DIV
Duty = 50%

图 7-12. Shutdown Dimming



Time = 5ms/DIV
Duty = 1%-100%-1%

图 7-13. Dimming Transient-Dimming

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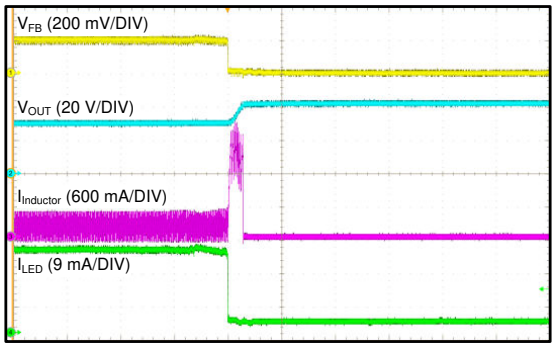


图 7-14. Open LED Protection

7.4 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.7V and 5.5V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS61169 device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

7.5 Layout

7.5.1 Layout Guidelines

As for all switching power supplies, especially those high frequency and high current ones, layout is an important design step. If layout is not carefully done, the regulator could suffer from instability as well as noise problems. Therefore, use wide and short traces for high current paths. The input capacitor C_{IN} must be close to VIN pin and GND pin in order to reduce the input ripple seen by the device. If possible choose higher capacitance value for it. The SW pin carries high current with fast rising and falling edge; therefore, the connection between the SW pin to the inductor must be kept as short and wide as possible. The output capacitor C_{OUT} must be put close to VOUT pin. It is also beneficial to have the ground of C_{OUT} close to the GND pin because there is large ground return current flowing between them. FB resistor must be put close to FB pin. When laying out signal ground, TI recommends using short traces separated from power ground traces, and connect them together at a single point close to the GND pin.

7.5.2 Layout Example

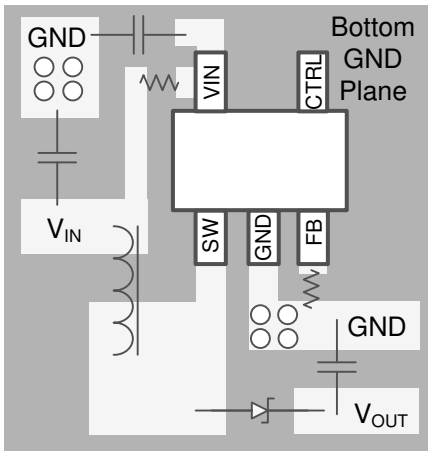


图 7-15. TPS61169 Board Layout

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8 Device and Documentation Support

8.1 Device Support

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.4 Trademarks

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (March 2016) to Revision B (June 2024)	Page

Changes from Revision * (October 2014) to Revision A (March 2016)	Page
• 向第 1 页上的“应用”部分添加了新项	1
• Changed *Handling Ratings* to *ESD Ratings* table; move storage temperature range from *Handling Ratings* to *Abs Max* table	4

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS61169DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN | POST-PLAT AG SPOT	Level-1-260C-UNLIM	-40 to 85	SZL
TPS61169DCKR.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	POST-PLAT AG SPOT	Level-1-260C-UNLIM	-40 to 85	SZL
TPS61169DCKRG4.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

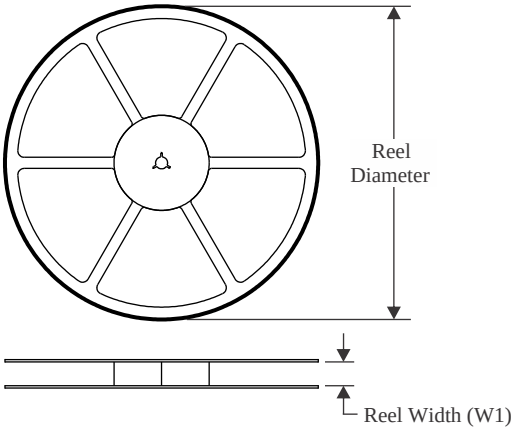
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

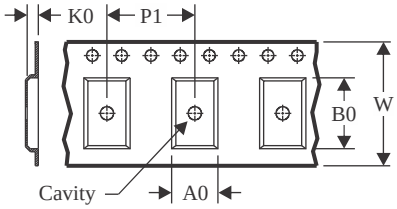
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

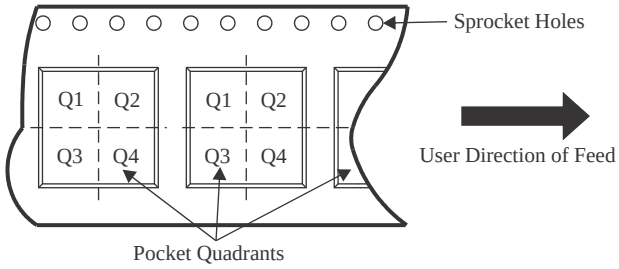


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

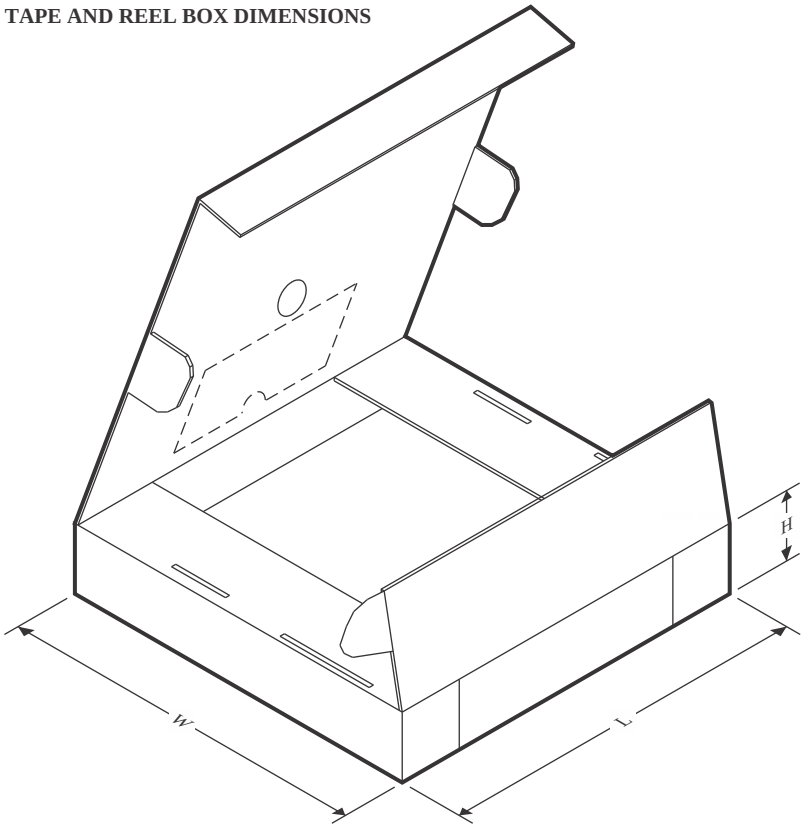
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61169DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
TPS61169DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

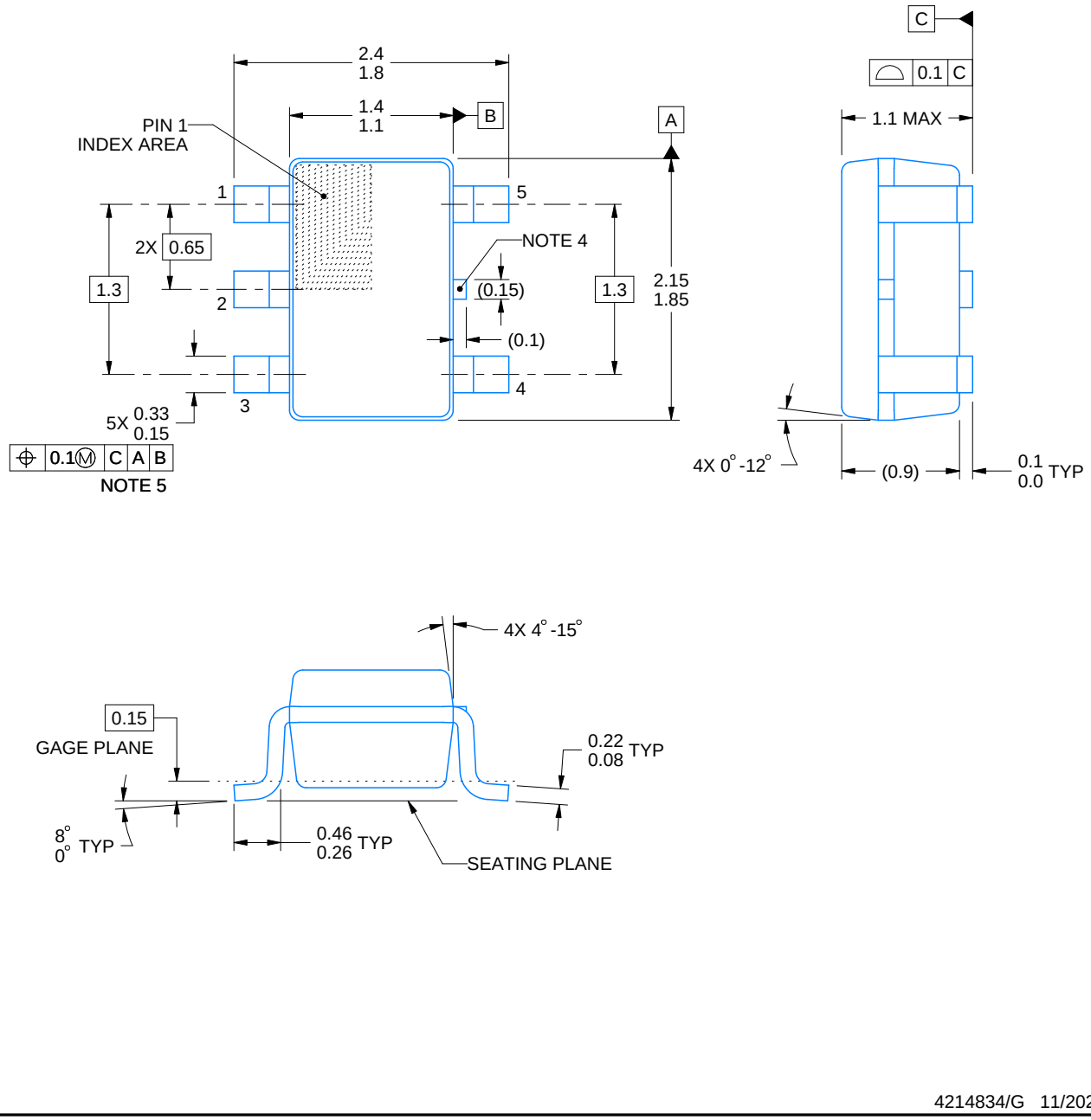
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61169DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
TPS61169DCKR	SC70	DCK	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

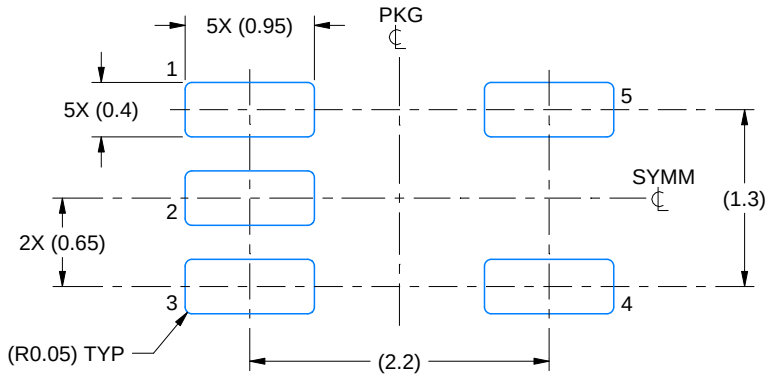
SMALL OUTLINE TRANSISTOR



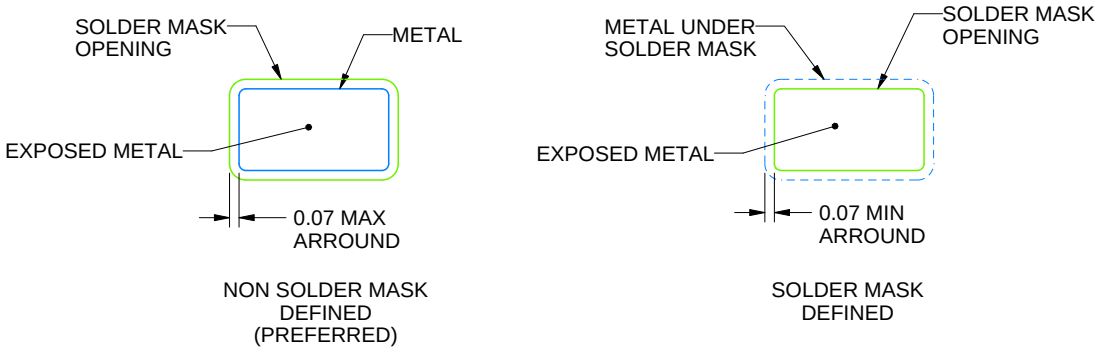
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

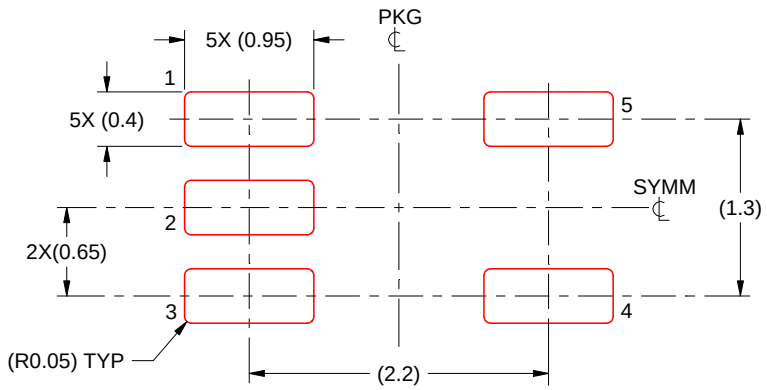


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月