TPS60204、TPS60205 稳压 3.3V、100mA 低纹波电荷泵低功耗直流/直流转换器

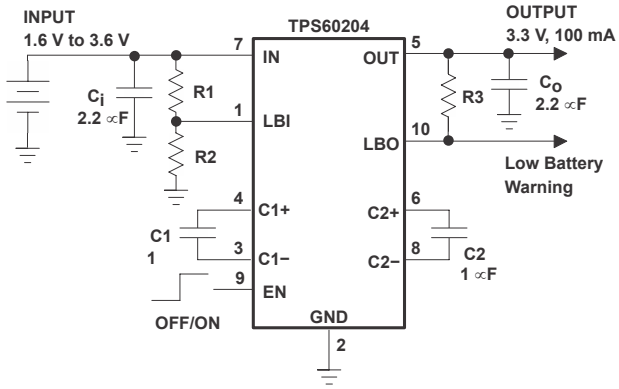
1 特性

- 在 1.8V 至 3.6V 输入电压范围内提供 3.3V 稳压输出电压，输出电流高达 100mA
- 采用推挽拓扑实现小于 $5mV_{(PP)}$ 的输出电压纹波
- 集成电池低电量检测器和电源正常状态检测器
- 开关频率可与外部时钟信号同步
- 以高达 90% 的效率和 35 µA 的静态电源电流延长电池使用时间
- 由于不使用电感器，因此易于设计、低成本、低 EMI 电源
- 关断电流为 0.05 µA，电池与负载在关断模式下隔离
- 紧凑型转换器解决方案，采用超小型 10 引脚 MSOP 封装，仅需四个外部电容器
- 提供评估模块 (TPS60200EVM-145)

2 应用

在电池供电的应用中用电感器替换直流/直流转换器，例如：

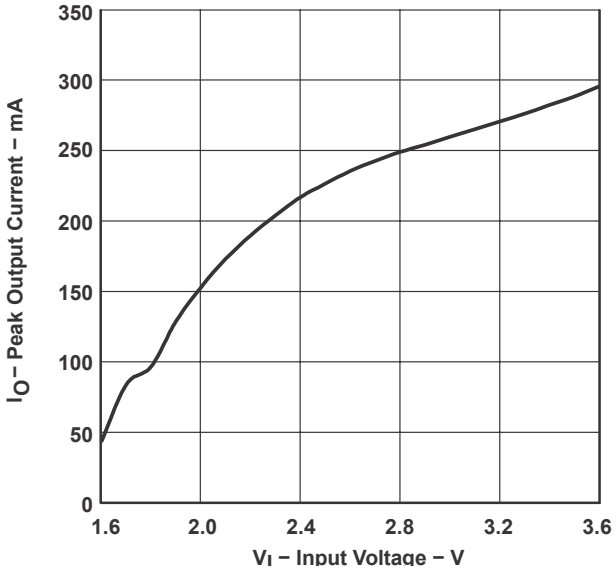
- 两节电池转换到 3.3V
- MP3 便携式音频播放器
- 电池供电的微处理器系统
- 备用电池升压转换器
- PDA、整理器和无绳电话
- 手持仪表
- 血糖仪和其他医疗仪器



典型应用电路及电池低电量警告

3 说明

TPS6020x 升压稳压电荷泵可在 1.8V 至 3.6V 的输入电压范围内生成 3.3V ±4% 的输出电压。此类器件通常由两节碱性电池、镍镉电池或镍氢电池供电，可在低至 1.6V 的最小电源电压下运行。输入电压为 2V 时，持续输出电流至少为 100mA。构建一个完整的低纹波直流/直流转换器只需要四个外部电容器。两个单端电荷泵的推挽工作模式可确保在电流持续传输到输出端时实现低输出电压纹波。



TPS60204 峰值输出电流输入电压

Table of Contents

4 Revision History

Changes from Revision A (September 2001) to Revision B (May 2023)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1

5 说明（续）

这些器件以新开发的 LinSkip 模式运行。在此工作模式下，一旦输出电流超过大约 7mA 的 LinSkip 阈值，器件就会从轻负载下省电的脉冲跳跃模式无缝切换到低噪声的恒定频率线性稳压模式。即使在脉冲跳跃模式下，输出纹波也会保持在非常低的水平，因为电荷泵的输出电阻仍处于稳压状态。

可以使用 EN 引脚对三种工作模式进行编程。EN = 低电平将禁用器件、关断所有内部电路并将输出与输入断开。EN = 高电平将启用器件并编程为从内部振荡器运行。如果 EN 有时钟计时，则器件与外部时钟信号同步运行；因此，可以控制开关谐波并将其最小化。这些器件包括一个电池低电量检测器，可在电池电压降至用户定义的阈值电压以下时发出警告；或者包括一个电源正常状态检测器，在输出电压达到其标称值的大约 90% 时就会激活该检测器。

器件提供具有电池低电量检测器或电源正常状态检测器的版本供选择。该直流/直流转换器无需电感器，因此系统的 EMI 可降至最低。该器件采用小型 10 引脚 MSOP 封装 (DGS)。

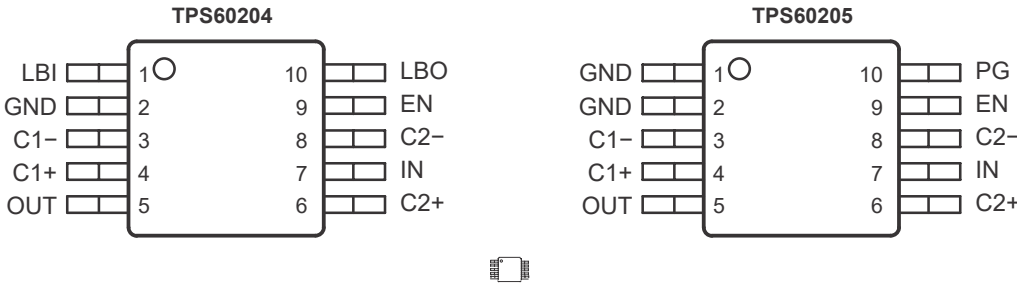
表 5-1. 提供的选项

T_A	器件型号(1)	DGS 封装标识	输出电流 (mA)	输出电压	器件特性
−40°C 至 85°C	TPS60204DGS	AFB	100	3.3	电池低电量检测器
	TPS60205DGS	AFC	100	3.3	电源正常状态检测器

(1) DGS 封装可采用带卷形式供货。向器件类型添加 R 后缀（例如 TPS60204DGSR）可以按每卷带 2500 个器件的数量订货。

6 Pin Configuration and Functions

DGS PACKAGES



ACTUAL SIZE
3.05 mm x 4.98 mm

表 6-1. Pin Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
C1+	4		Positive terminal of the flying capacitor C1
C1-	3		Negative terminal of the flying capacitor C1
C2+	6		Positive terminal of the flying capacitor C2
C2-	8		Negative terminal of the flying capacitor C2
EN	9	I	Device-enable input. Three operating modes can be programmed with the EN pin. − EN = Low disables the device. Output and input are isolated in the shutdown. − EN = High lets the device run from the internal oscillator. − If an external clock signal is applied to the EN pin, the device is in syncmode and runs synchronized at the frequency of the external clock signal.
GND	2		Ground
IN	7	I	Supply input. Bypass IN to GND with a capacitor of the same size as C_o.
LBI/GND	1	I	Low-battery detector input for the TPS60204. A low-battery warning is generated at the LBO pin when the voltage on LBI drops below the threshold of 1.18 V. Connect LBI to GND if the low-battery detector function is not used. For the TPS60205, this pin has to be connected to ground (GND pin).
LBO/PG	10	O	Open-drain low-battery detector output for the TPS60204. This pin is pulled low if the voltage on LBI drops below the threshold of 1.18 V. A pullup resistor should be connected between LBO and OUT or any other logic supply rail that is lower than 3.6 V. Open-drain power-good detector output for the TPS60205. As soon as the voltage on OUT reaches about 90% of it is nominal value this pin goes active high. A pullup resistor should be connected between PG and OUT or any other logic supply rail that is lower than 3.6 V.
OUT	5	O	Regulated 3.3-V power output. Bypass OUT to GND with the output filter capacitor C_o.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	IN to GND	-0.3	3.6	V
	EN, PG to GND	-0.3	3.6	
	LBI, LBO to GND	-0.3	3.6	
Output voltage	OUT to GND	-0.3	3.6	V
	C1+, C2+ to GND	-0.3	V_O + 0.3	V
	C1-, C2- to GND	-0.3	V_I + 0.3	
Output current	OUT		150	mA
Storage temperature	T_{stg}	-55	150	°C
Maximum junction temperature	T_J		150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Dissipation Rating

PACKAGE(1)	$T_A \leqslant 25$ ℃ POWER RATING	DERATING FACTOR ABOVE T_A=25℃	T_A=70℃ POWER RATING	T_A = 85℃ POWER RATING
DGS	424mW	3.4mW/℃	187mW	136mW

(1) The thermal resistance junction to ambient of the DGS package is R_{TH-JA} = 294℃/W

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Input voltage range	V_I	1.6		3.6	V
Input capacitor	C_i		2.2		µF
Flying capacitors	C1, C2		1		µF
Output capacitor	C_o		2.2		µF
Operating junction temperature	T_J	-40		125	℃

7.4 Electrical Characteristics

electrical characteristics at C_i = 2.2 µF, C1 = C2 = 1 µF, C_O = 2.2 µF, T_A = −40°C to 85°C, V_I = 2.4 V, EN = V_I (unless otherwise noted) over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{O(MAX)}$	Maximum continuous output current	V_I = 2 V	100			mA
V_O	Output voltage	1.6 V < V_I < 1.8 V, 0 < I_O < 0.25 × $I_{O(MAX)}$	3			V
		1.8 V < V_I < 2 V, 0 < I_O < 0.5 × $I_{O(MAX)}$	3.17		3.43	
		2 V < V_I < 3.3 V, 0 < I_O < $I_{O(MAX)}$	3.17		3.43	
		3.3 V < V_I < 3.6 V, 0 < I_O < $I_{O(MAX)}$	3.17		3.47	
V_{PP}	Output voltage ripple	I_O = $I_{O(MAX)}$		5		mV_{PP}

7.4 Electrical Characteristics (continued)

electrical characteristics at C_i = 2.2 µF, C1 = C2 = 1 µF, C_O = 2.2 µF, T_A = −40°C to 85°C, V_I = 2.4 V, EN = V_I (unless otherwise noted) over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(Q)}$	Quiescent current (no-load input current)	I_O = 0 mA, V_I = 1.8 V to 3.6 V		35	70	µA
$I_{(SD)}$	Shutdown supply current	EN = 0 V		0.05	1	
$f_{(OSC)}$	Internal switching frequency		200	300	400	kHz
$f_{(SYNC)}$	External clock signal frequency		400	600	800	
	External clock signal duty cycle		30%		70%	
V_{IL}	EN input low voltage	V_I = 1.6 V to 3.6 V			0.3 × V_I	V
V_{IH}	EN input high voltage	V_I = 1.6 V to 3.6 V	0.7 × V_I			
$I_{lkg(EN)}$	EN input leakage current	EN = 0 V or V_I		0.01	0.1	µA
	Output capacitor auto discharge time	EN is set from V_I to GND, Time until V_O < 0.5 V		0.6		ms
	Output leakage current in shutdown	EN = 0 V, T_A = −40 to 85°C			5	µA
		EN = 0 V, T_A ≤ 65°C			3	
	LinSkip threshold	V_I = 2.2 V		7		mA
	Output load regulation	10 mA < I_O < $I_{O(MAX)}$; T_A = 25°C			0.01	%/mA
	Output line regulation	2 V < V_I < 3.3 V, I_O = 0.5 x $I_{O(MAX)}$, T_A = 25°C		0.6		%/V
$I_{(SC)}$	Short circuit current	V_I = 2.4 V, V_O = 0 V		60		mA

7.5 Electrical Characteristics TPS60204

electrical characteristics for low-battery comparator of device TPS60204 at T_A = −40°C to 85°C, V_I = 2.4 V and EN = V_I (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(LBI)}$	LBI trip voltage	V_I = 1.6 V to 2.2 V, T_C = 0°C to 70°C	1.13	1.18	1.23	V
	LBI trip voltage hysteresis	For rising voltage at LBI		10		mV
$I_{I(LBI)}$	LBI input current	$V_{(LBI)}$ = 1.3 V		2	50	nA
$V_{O(LBO)}$	LBO output voltage low	$V_{(LBI)}$ = 0 V, $I_{(LBO)}$ = 1 mA			0.4	V
$I_{lkg(LBO)}$	LBO leakage current	$V_{(LBI)}$ = 1.3 V, $V_{(LBO)}$ = 3.3 V		0.01	0.1	µA

备注

During start-up of the converter the LBO output signal is invalid for the first 500 µs.

7.6 Electrical Characteristics TPS60205

electrical characteristics for power-good comparator of device TPS60205 at T_A = −40°C to 85°C, V_I = 2.4 V and EN = V_I (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(PG)}$	Power-good trip voltage	T_C = 0°C to 70°C	0.87 × V_O	0.91 × V_O	0.95 × V_O	V
$V_{hys(PG)}$	Power-good trip voltage hysteresis	V_O decreasing, T_C = 0°C to 70°C		1%		
$V_{O(PG)}$	Power-good output voltage Low	V_O = 0 V, $I_{(PG)}$ = 1 mA			0.4	V
$I_{lkg(PG)}$	Power-good leakage current	V_O = 3.3 V, $V_{(PG)}$ = 3.3 V		0.01	0.1	µA

备注

During start-up of the converter the PG output signal is invalid for the first 500 μs.

7.7 Typical Characteristics

表 7-1. Table of Graphs

			FIGURES
η	Efficiency	vs Output current (TPS60204, TPS60205)	7-1
		vs Input voltage	7-2
I_Q	Quiescent supply current	vs Input voltage	7-3
V_O	Output voltage	vs Output current	7-4
		vs Input voltage	7-5
V_O	Output voltage ripple	vs Time	7-6, 7-7, 7-8
	Start-up timing		7-9
	Load transient response		7-10, 7-11
I_O	Peak output current	vs Input voltage	7-12

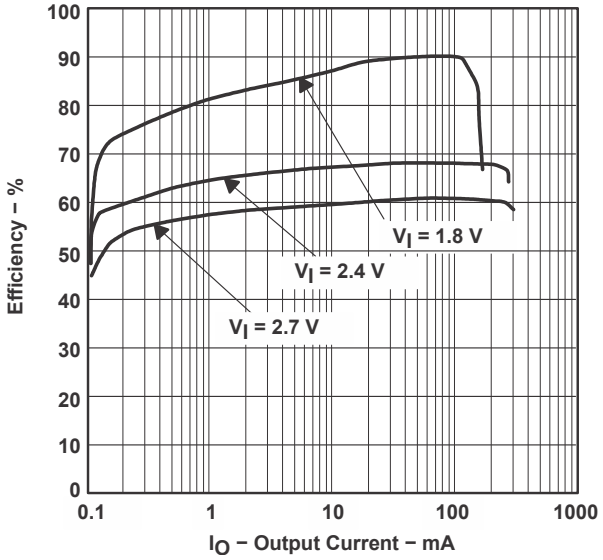


图 7-1. TPS60204, TPS60205 Efficiency vs Output Current

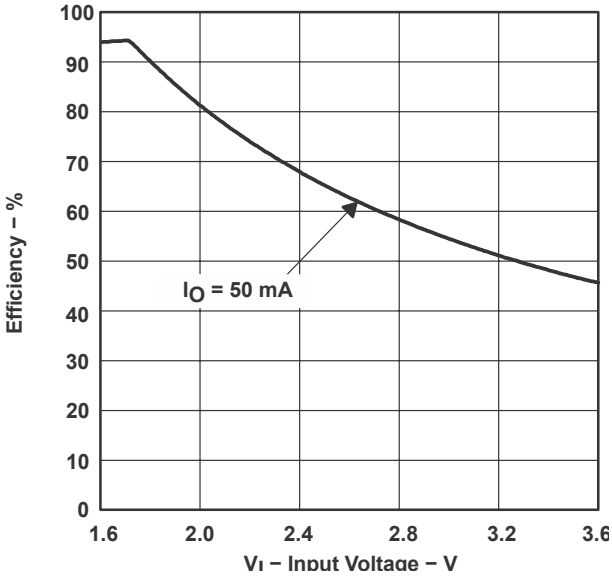


图 7-2. Efficiency vs Input Voltage

7.7 Typical Characteristics (continued)

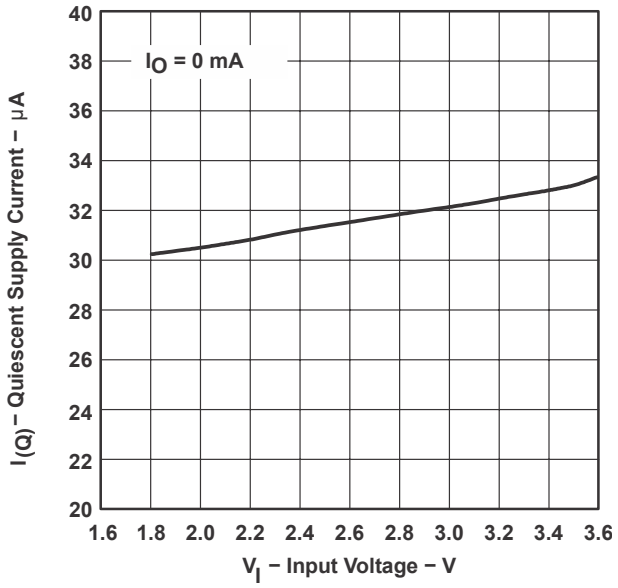


图 7-3. Quiescent Supply Current vs Input Voltage

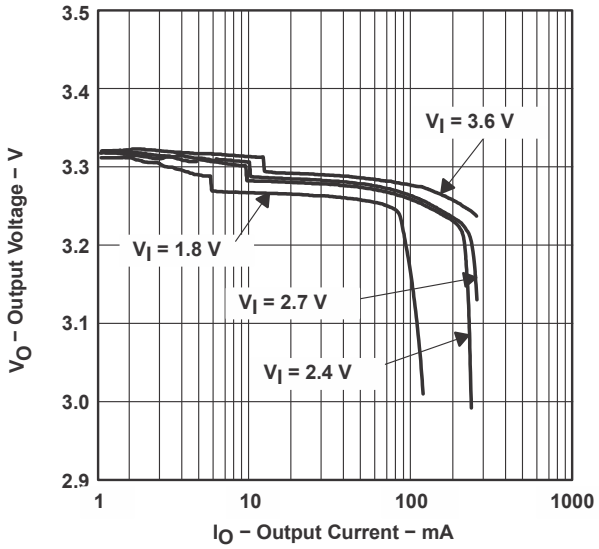


图 7-4. Output Voltage vs Output Current

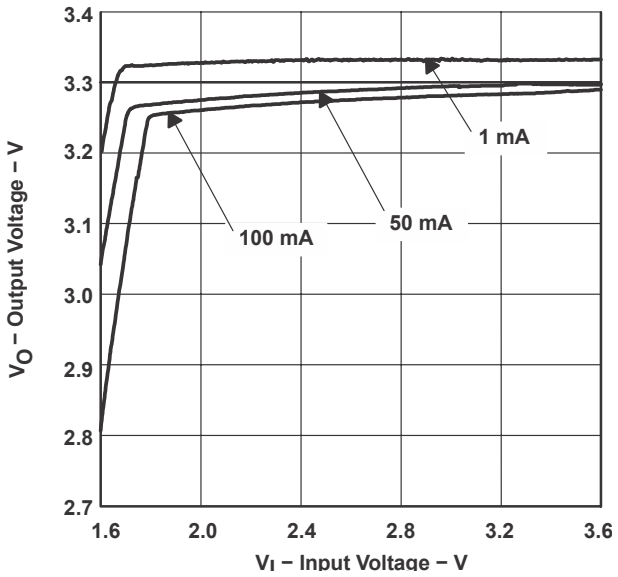


图 7-5. Output Voltage vs Input Voltage

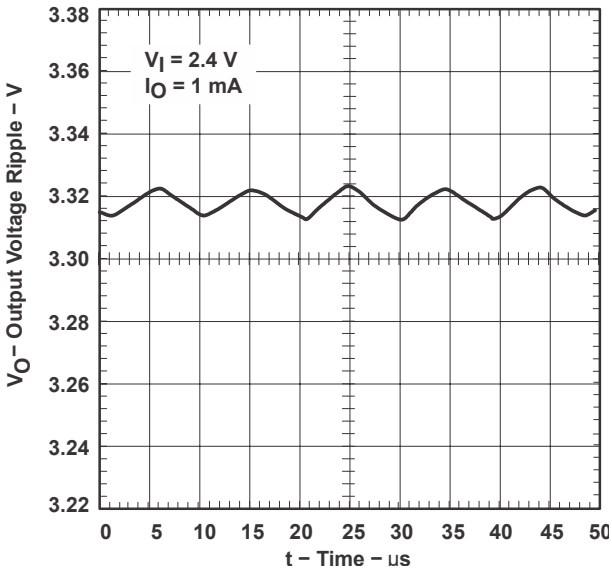


图 7-6. Output Voltage Ripple vs Time

7.7 Typical Characteristics (continued)

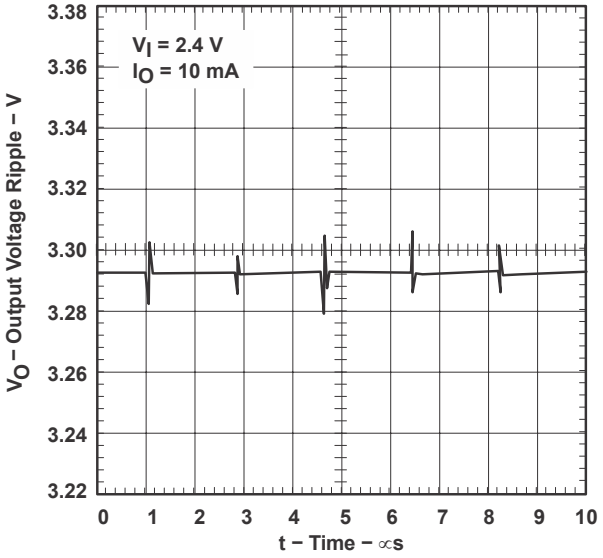


图 7-7. Output Voltage Ripple vs Time

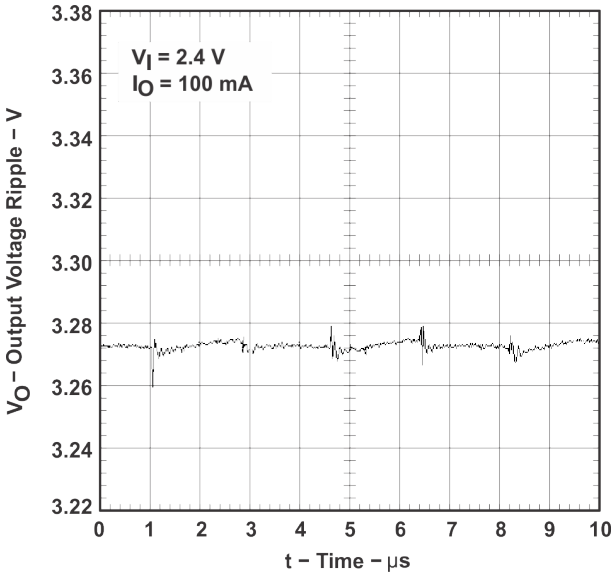


图 7-8. Output Voltage Ripple vs Time

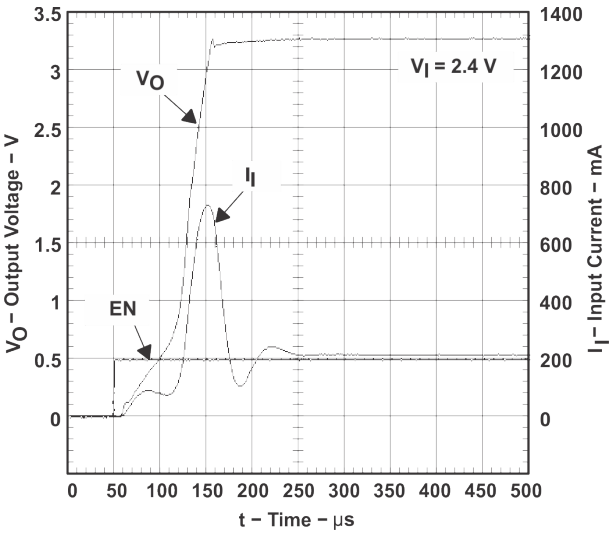


图 7-9. Start-Up Timing

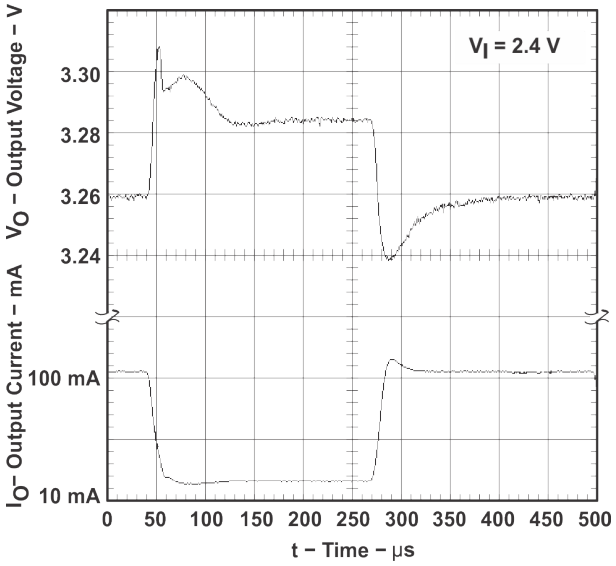


图 7-10. Load Transient Response

7.7 Typical Characteristics (continued)

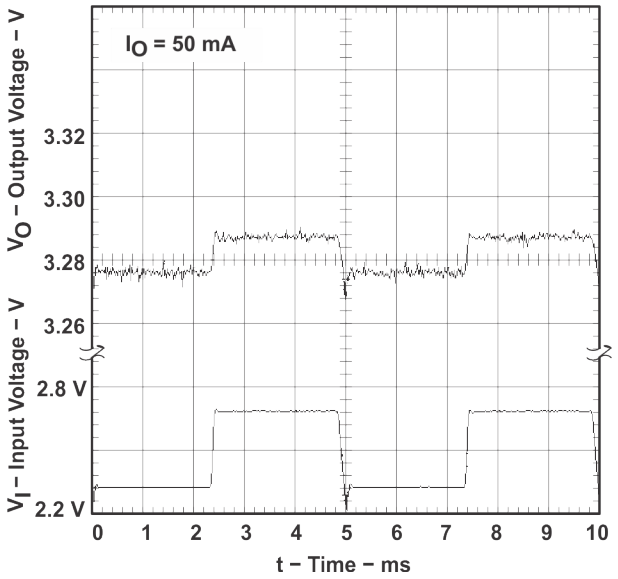


图 7-11. Line Transient Response

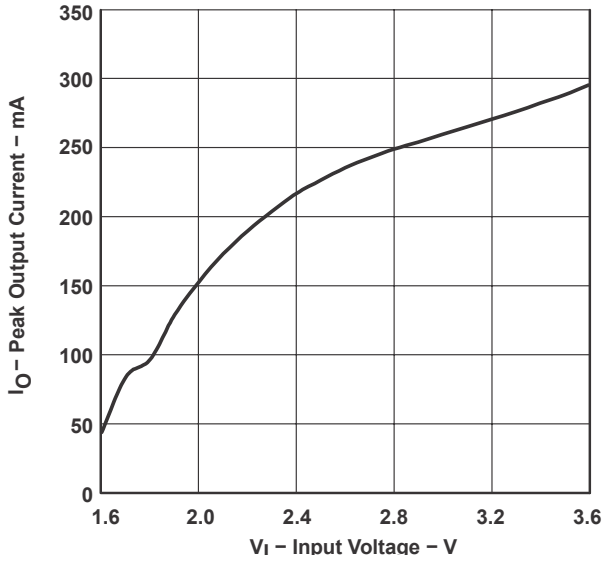


图 7-12. Peak Output Current vs Input Voltage

8 Detailed Description

Operating Principle

The TPS6020x charge pumps provide a regulated 3.3-V output from a 1.8-V to 3.6-V input. They deliver up to 100-mA load current while maintaining the output at 3.3 V ±4%. Designed specifically for space critical battery powered applications, the complete converter requires only four external capacitors. The device is using the push-pull topology to achieve lowest output voltage ripple. The converter is also optimized for smallest board space. It makes use of small sized capacitors, with the highest output current rating per output capacitance and package size.

The TPS6020x circuits consist of an oscillator, a 1.18-V voltage reference, an internal resistive feedback circuit, an error amplifier, two charge pump power stages with high current MOSFET switches, a shutdown/start-up circuit, and a control circuit (see functional block diagrams).

Push-pull Operating Mode

The two single-ended charge pump power stages operate in the so-called push-pull operating mode, i.e., they operate with a 180°C phase shift. Each single-ended charge pump transfers charge into its transfer capacitor (C1 or C2) in one half of the period. During the other half of the period (transfer phase), the transfer capacitor is placed in series with the input to transfer its charge to Co. While one single-ended charge pump is in the charge phase, the other one is in the transfer phase. This operation assures an almost constant output current which ensures a low output ripple.

If the clock were to run continuously, this process would eventually generate an output voltage equal to two times the input voltage (hence the name voltage doubler). In order to provide a regulated fixed output voltage of 3.3 V, the TPS6020x devices use either pulse-skip or constant-frequency linear-regulation control mode. The mode is automatically selected based on the output current. If the load current is below the LinSkip current threshold, it switches into the power-saving pulse-skip mode to boost efficiency at low output power.

Constant-frequency Mode

When the output current is higher then the LinSkip current threshold, the charge pump runs continuously at the switching frequency $f_{(OSC)}$. The control circuit, fed from the error amplifier, controls the charge on C1 and C2 by controlling the gates and hence the rDS(ON) of the integrated MOSFETs. When the output voltage decreases, the gate drive increases, resulting in a larger voltage across C1 and C2. This regulation scheme minimizes output ripple. Since the device switches continuously, the output signal contains well-defined frequency components, and the circuit requires smaller external capacitors for a given output ripple. However, constant-frequency mode, due to higher operating current, is less efficient at light loads. For this reason, the device switches seamlessly into the pulse-skip mode when the output current drops below the LinSkip current threshold.

Pulse-skip Mode

The regulator enters the pulse-skip mode when the output current is lower than the LinSkip current threshold of 7 mA. In the pulse-skip mode, the error amplifier disables switching of the power stages when it detects an output voltage higher than 3.3 V. The controller skips switching cycles until the output voltage drops below 3.3 V. Then the error amplifier reactivates the oscillator and switching of the power stages starts again. A 30-mV output voltage offset is introduced in this mode.

The pulse-skip regulation mode minimizes operating current because it does not switch continuously and deactivates all functions except the voltage reference and error amplifier when the output is higher than 3.3 V. Even in pulse-skip mode the $r_{DS(ON)}$ of the MOSFETs is controlled. This way the energy per switching cycle that is transferred by the charge pump from the input to the output is limited to the minimum that is necessary to sustain a regulated output voltage, with the benefit that the output ripple is kept to a minimum. When switching is disabled from the error amplifier, the load is also isolated from the input.

Start Up and Shutdown

During start-up, i.e. when EN is set from logic low to logic high, the output capacitor is directly connected to IN and charged up with a limited current until the output voltage VO reaches 0.8 × VI. When the start-up comparator detects this limit, the converter begins switching. This precharging of the output capacitor guarantees a short start-up time. In addition, the inrush current into an empty output capacitor is limited. The converter can start into a full load, which is defined by a 33-Ω or 66-Ω resistor, respectively.

Driving EN low disables the converter. This disables all internal circuits and reduces the supply current to only 0.05 µA. The device exits shutdown once EN is set high. When the device is disabled, the load is isolated from the input. This is an important feature in battery operated products because it extends the products shelf life.

Synchronization to an External Clock Signal

The operating frequency of the charge pump is limited to 400 kHz in order to avoid interference in the sensitive 455-kHz IF band. The device can either run from the integrated oscillator, or an external clock signal can be used to drive the charge pump. The maximum frequency of the external clock signal is 800 kHz. The switching frequency used internally to drive the charge pump power stages is half of the external clock frequency. The external clock signal is applied to the EN pin. The device will switch off if the signal on EN is hold low for more than 10 µs.

When the load current drops below the LinSkip current threshold, the devices will enter the pulse-skip mode but stay synchronized to the external clock signal.

Low-battery Detector (TPS60204)

The low-battery comparator trips at 1.18 V ±4% when the voltage on pin LBI ramps down. The voltage $V_{(TRIP)}$ at which the low-battery warning is issued can be adjusted with a resistive divider as shown in Figure 2. The sum of resistors R1 and R2 is recommended to be in the 100-kΩ to 1-MΩ range. When choosing R1 and R2, be aware of the input leakage current into the LBI pin.

LBO is an open drain output. An external pullup resistor to OUT, or any other voltage rail in the appropriate range, in the 100-kΩ to 1-MΩ range is recommended. During start-up, the LBO output signal is invalid for the first 500 µs. LBO is high impedance when the device is disabled. If the low-battery comparator function is not used, connect LBI to ground and leave LBO unconnected. The low-battery detector is disabled when the device is switched off.

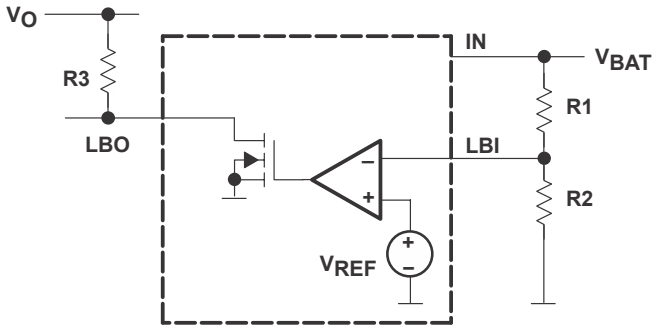


图 8-1. Programming of the Low-Battery Comparator Trip Voltage

A 100-nF ceramic capacitor should be connected in parallel to R2 if large line transients are expected. These voltage drops can inadvertently trigger the low-battery comparator and produce a wrong low-battery warning signal at the LBO pin.

Formulas to calculate the resistive divider for low-battery detection, with V_{LBI} = 1.13 V to 1.23 V and the sum of resistors R1 and R2 equal 1 MΩ:

$$R2 = 1\,M\Omega \times \frac{V_{LBI}}{V_{Bat}} \quad (1)$$

$$R1 = 1\,M\Omega - R2 \quad (2)$$

Formulas to calculate the minimum and maximum battery voltage:

$$V_{Bat(min)} = V_{LBI(min)} \times \frac{R1_{(min)} + R2_{(max)}}{R2_{(min)}} \quad (3)$$

$$V_{Bat(max)} = V_{LBI(max)} \times \frac{R1_{(max)} + R2_{(min)}}{R2_{(min)}} \quad (4)$$

表 8-1. Recommended Values for the Resistive Divider From the E96 Series (±1%)

V_{IN} / V	R1 / kΩ	R2 / kΩ	$V_{TRIP(MIN)}$/V	$V_{TRIP(MAX)}$ /V
1.6	267	750	1.524	1.677
1.7	301	681	1.620	1.785
1.8	340	649	1.710	1.887
1.9	374	619	1.799	1.988
2.0	402	576	1.903	2.106

Power-good Detector (TPS60205)

The power-good output is an open-drain output that pulls low when the output is out of regulation. When the output rises to within 90% of its nominal voltage, the power-good output is released. Power-good is high impedance in shutdown. In normal operation, an external pullup resistor must be connected between PG and OUT, or any other voltage rail in the appropriate range. The resistor should be in the 100-kΩ to 1-MΩ range. If the PG output is not used, it should remain unconnected.

8.1 Functional Block Diagrams

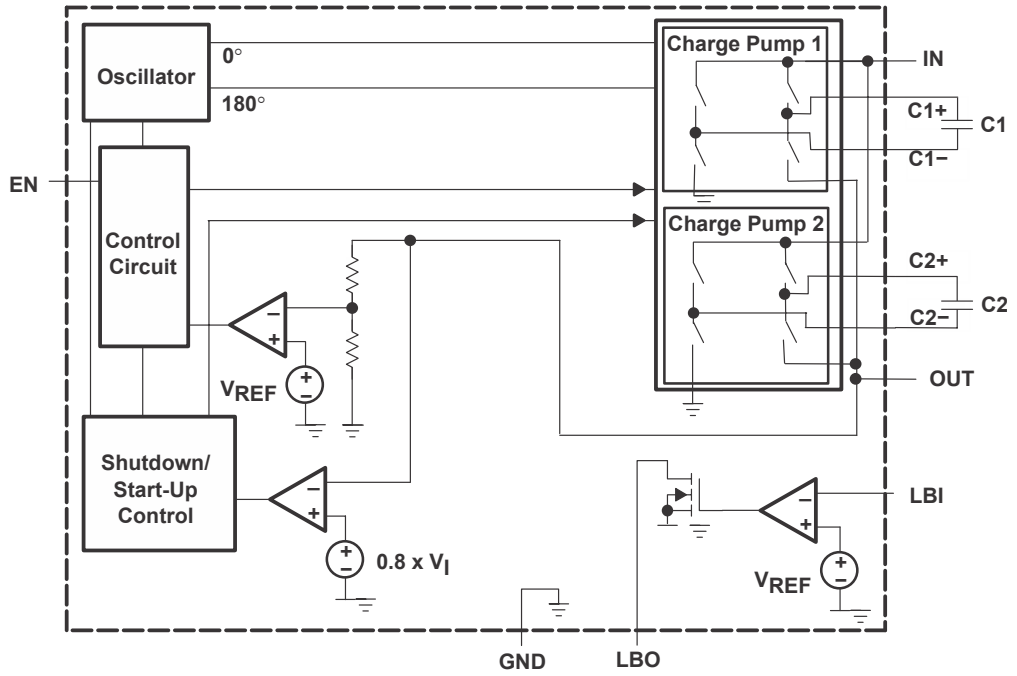


图 8-2. TPS60204 With Low-Battery Detector

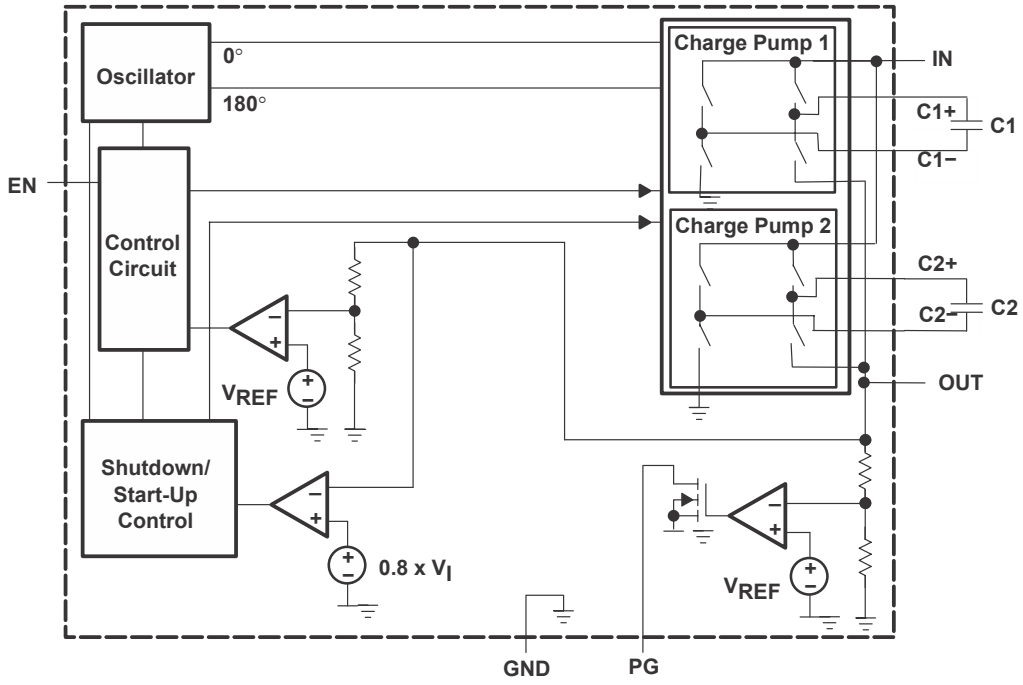


图 8-3. TPS60205 With Power-Good Detector

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

Capacitor Selection

The TPS6020x devices require only four external capacitors to achieve a very low output voltage ripple. The capacitor values are closely linked to the required output current. Low ESR (<0.1 Ω) capacitors should be used at input and output. In general, the transfer capacitors (C1 and C2) will be the smallest; a 1-µF value is recommended for maximum load operation. With smaller capacitor values, the maximum possible load current is reduced and the LinSkip threshold is lowered.

The input capacitor improves system efficiency by reducing the input impedance. It also stabilizes the input current of the power source. The input capacitor should be chosen according to the power supply used and the distance from the power source to the converter IC. Ci is recommended to be about two to four times as large as the flying capacitors C1 and C2.

The output capacitor (C_o) should be at minimum the size of the input capacitor. The minimum required capacitance is 2.2 µF. Larger values will improve the load transient performance and will reduce the maximum output ripple voltage.

Only ceramic capacitors are recommended for input, output, and flying capacitors. Depending on the material used to manufacture them, ceramic capacitors might lose their capacitance over temperature and voltage. Ceramic capacitors of type X7R or X5R material will keep their capacitance over temperature and voltage, whereas Z5U- or Y5V-type capacitors will decrease in capacitance. Table 2 lists the recommended capacitor values.

表 9-1. Recommended Capacitor Values (Ceramic X5R and X7R)

LOAD CURRENT, I_L /mA	FLYING CAPACITORS, C1/C2 / µF	INPUT CAPACITOR, C_i / µF	OUTPUT CAPACITOR, C_o / µF	OUTPUT VOLTAGE RIPPLE IN LINEAR MODE, $V_{(P-P)}$/mV	OUTPUT VOLTAGE RIPPLE IN SKIP MODE, $V_{(P-P)}$ /mV
0-100	1	2.2	2.2	3	20
0-100	1	4.7	4.7	3	10
0-100	1	2.2	10	3	7
0-100	2.2	4.7	4.7	3	10
0-50	0.47	2.2	2.2	3	20
0-25	0.22	2.2	2.2	5	15
0-10	0.1	2.2	2.2	5	15

表 9-2. Recommended Capacitor Types

MANUFACTURER	PART NUMBER	SIZE	CAPACITANCE	TYPE
Taiyo Yuden	UMK212BJ104MG	0805	0.1 µF	Ceramic
	EMK212BJ224MG	0805	0.22 µF	Ceramic
	EMK212BJ474MG	0805	0.47 µF	Ceramic
	LMK212BJ105KG	0805	1 µF	Ceramic
	LMK212BJ225MG	0805	2.2 µF	Ceramic
	EMK316BJ225KL	1206	2.2 µF	Ceramic
	LMK316BJ475KL	1206	4.7 µF	Ceramic
	JMK316BJ106ML	1206	10 µF	Ceramic
AVX	0805ZC105KAT2A	0805	1 µF	Ceramic
	1206ZC225KAT2A	1206	2.2 µF	Ceramic

表 9-3. Recommended Capacitor Manufacturers

MANUFACTURER	CAPACITOR TYPE	INTERNET SITE
Taiyo Yuden	X7R/X5R ceramic	Website
AVX	X7R/X5R ceramic	Website

Device Family Products

Other charge pump dc-dc converters in this family are:

表 9-4. Product Identification

PART NUMBER	DESCRIPTION
TPS60100	2-cell to regulated 3.3 V, 200-mA low-noise charge pump
TPS60101	2-cell to regulated 3.3 V, 100-mA low-noise charge pump
TPS60110	3-cell to regulated 5.0 V, 300-mA low-noise charge pump
TPS60111	3-cell to regulated 5.0 V, 150-mA low-noise charge pump
TPS60120	2-cell to regulated 3.3 V, 200-mA high efficiency charge pump with low battery comparator
TPS60121	2-cell to regulated 3.3 V, 200-mA high efficiency charge pump with power-good comparator
TPS60122	2-cell to regulated 3.3 V, 100-mA high efficiency charge pump with low battery comparator
TPS60123	2-cell to regulated 3.3 V, 100-mA high efficiency charge pump with power-good comparator
TPS60130	3-cell to regulated 5.0 V, 300-mA high efficiency charge pump with low battery comparator
TPS60131	3-cell to regulated 5.0 V, 300-mA high efficiency charge pump with low battery comparator
TPS60132	3-cell to regulated 5.0 V, 150-mA high efficiency charge pump with low battery comparator
TPS60133	3-cell to regulated 5.0 V, 150-mA high efficiency charge pump with power-good comparator
TPS60140	2-cell to regulated 5.0 V, 100-mA charge pump voltage tripler with low battery comparator
TPS60141	2-cell to regulated 5.0 V, 100-mA charge pump voltage tripler with power-good comparator

9.2 Typical Application

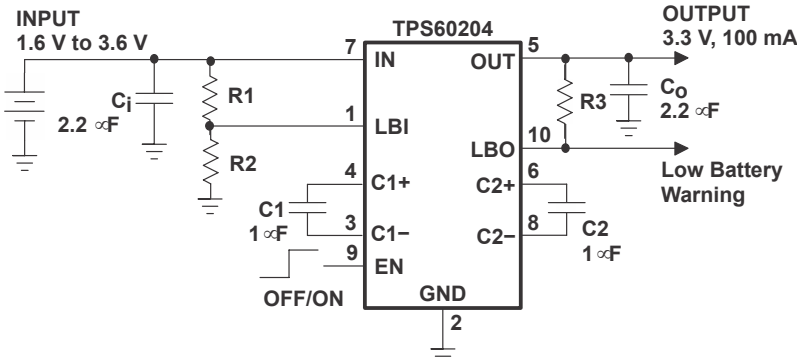


图 9-1. Typical Operating Circuit TPS60204 With Low-Battery Detector

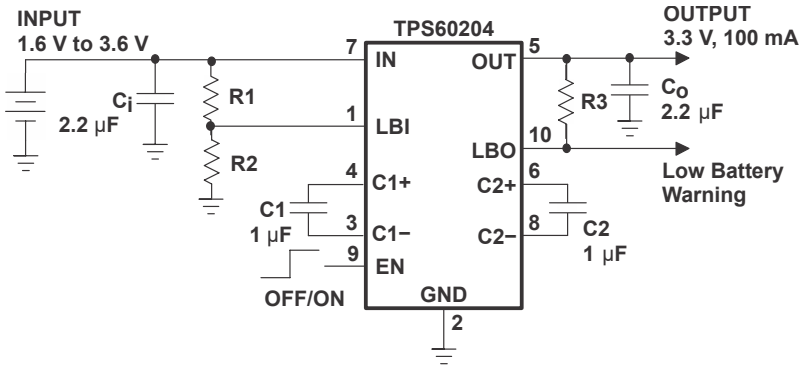


图 9-2. Typical Operating Circuit TPS60205 With Power-Good Detector

9.3 Power Dissipation

The power dissipated in the TPS6020x devices depends mainly on input voltage and output current and is approximated by:

$$P_{(DISS)} = I_O \times (2 \times V_I - V_O) \tag{5}$$

for

$$I_{(Q)} < I_O \tag{6}$$

By observing equation 5, it can be seen that the power dissipation is worst for highest input voltage V_I and highest output current I_O. For an input voltage of 3.6 V and an output current of 100 mA the calculated power dissipation $P_{(DISS)}$ is 390 mW. This is also the point where the charge pump operates with its lowest efficiency.

With the recommended maximum junction temperature of 125°C and an assumed maximum ambient operating temperature of 85°C, the maximum allowed thermal resistance junction to ambient of the system can be calculated.

$$R_{\theta JA(max)} = \frac{T_{J(MAX)} - T_A}{P_{DISS(max)}} = \frac{125℃ - 85℃}{390\ mW} = 102℃/W \tag{7}$$

P_{DISS} must be less than that allowed by the package rating. The thermal resistance junction to ambient of the used 10-pin MSOP is 294°C/W for an unsoldered package. The thermal resistance junction to ambient with the IC soldered to a printed circuit using a board layout as described in the application information section, the $R_{\Theta JA}$ is typically 200°C/W, which is higher than the maximum value calculated above. However, in a battery powered

application, both V_I and T_A will typically be lower than the worst case ratings used in equation 6 , and power dissipation should not be a problem in most applications.

9.4 Layout and Board Space

Careful board layout is necessary due to the high transient currents and switching frequency of the converter. All capacitors should be placed in close proximity to the device. A PCB layout proposal for a one-layer board is given in Figure 17. There is no specific EVM available for the TPS60204. However, the TPS60200EVM−145 can be used to evaluate the device.

The evaluation module for the TPS60200 can be ordered under product code TPS60200EVM−145. The EVM uses the layout shown in Figure 17. All components including the pins are shown. The EVM is built so that it can be connected to a 14-pin dual inline socket, therefore, the space needed for the IC, the external parts, and eight pins is 17,9 mm x 10,2 mm = 182,6 mm^2.

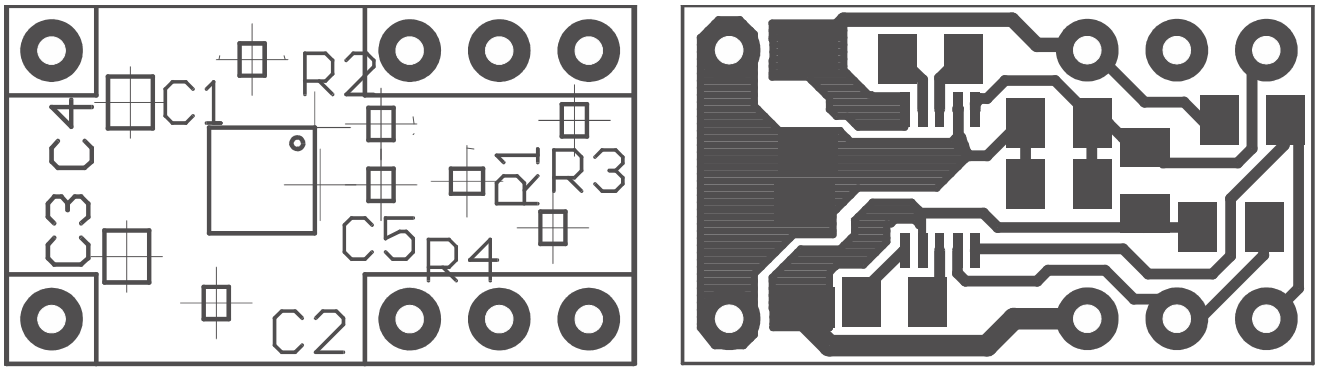


图 9-3. Recommended Component Placement and Board Layout

表 9-5. Component Identification

IC1	TPS60204
C1, C2	Flying capacitors
C3	Input capacitors
C4	Output capacitors
C5	Stabilization capacitor for LBI
R1, R2	Resistive divider for LBI
R3	Pullup resistor for LBO
R4	Pullup resistor for EN

Capacitor C5 should be included if large line transients are expected. This capacitor suppresses toggling of the LBO due to these line changes.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Device Support

10.2 Documentation Support

10.2.1 Related Documentation

10.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

10.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
TPS60204DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFB
TPS60204DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFB
TPS60205DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFC
TPS60205DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFC

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

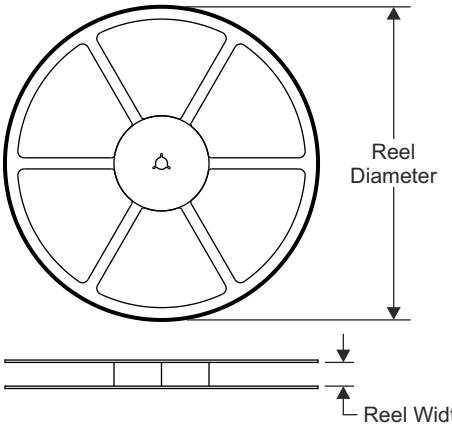
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

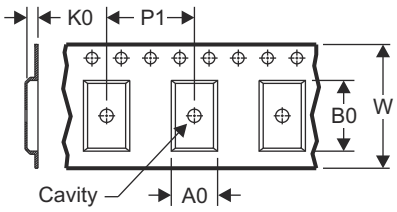
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

11.2 Tape and Reel Information

REEL DIMENSIONS

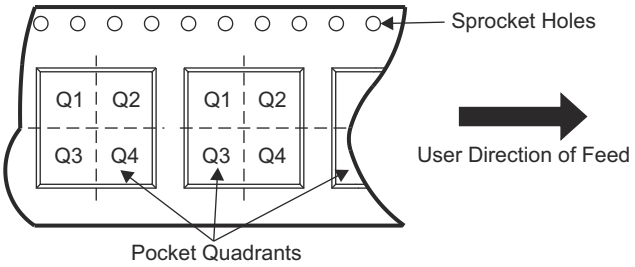


TAPE DIMENSIONS



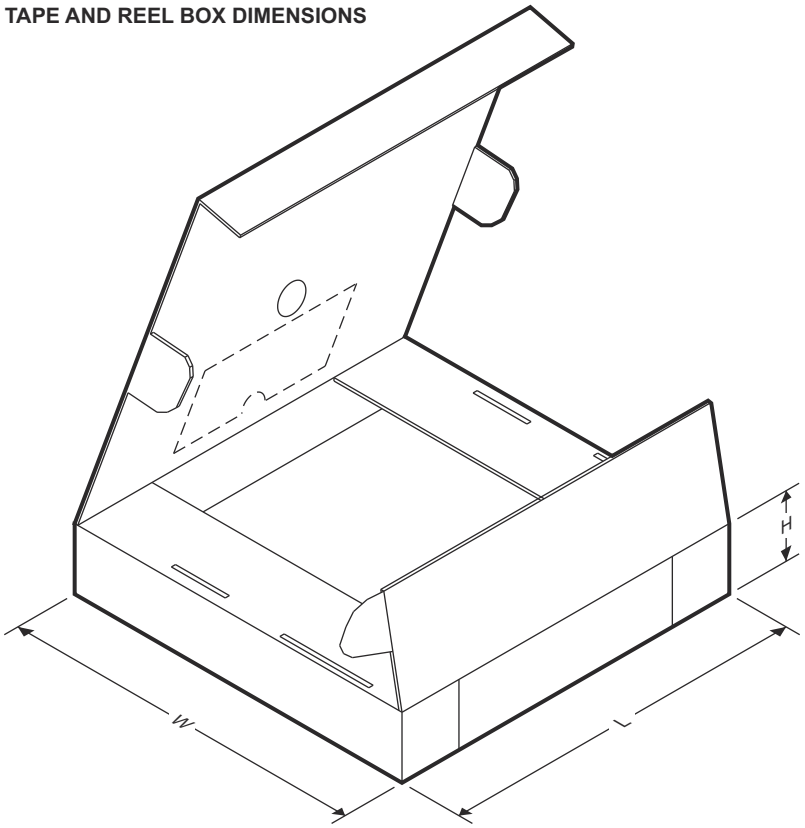
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS60204DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS60205DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS60204DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS60205DGSR	VSSOP	DGS	10	2500	350.0	350.0	

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS60204DGS	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFB
TPS60204DGS.A	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFB
TPS60204DGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFB
TPS60204DGSR.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFB
TPS60205DGS	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFC
TPS60205DGS.A	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFC
TPS60205DGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFC
TPS60205DGSR.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFC

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

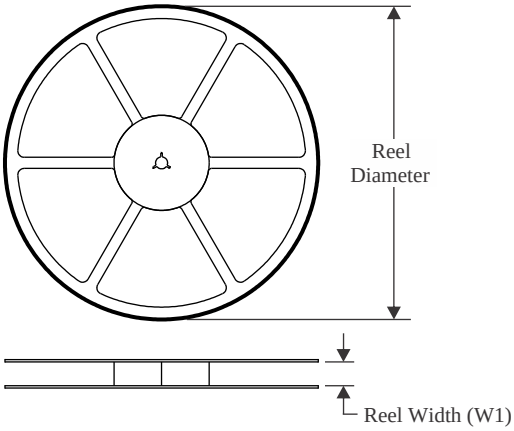
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

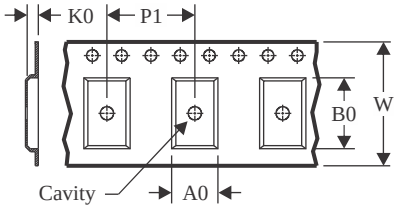
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
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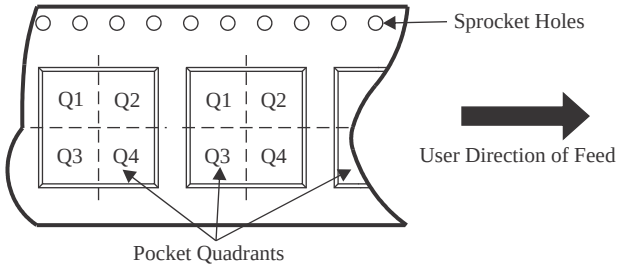
P1	Pitch between successive cavity centers

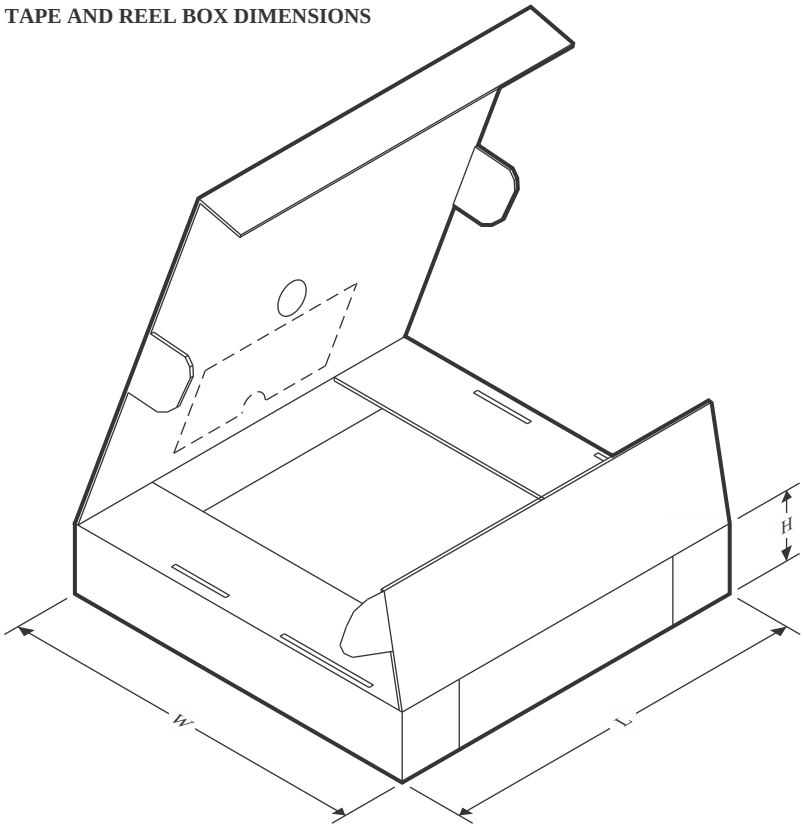
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS60204DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS60205DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

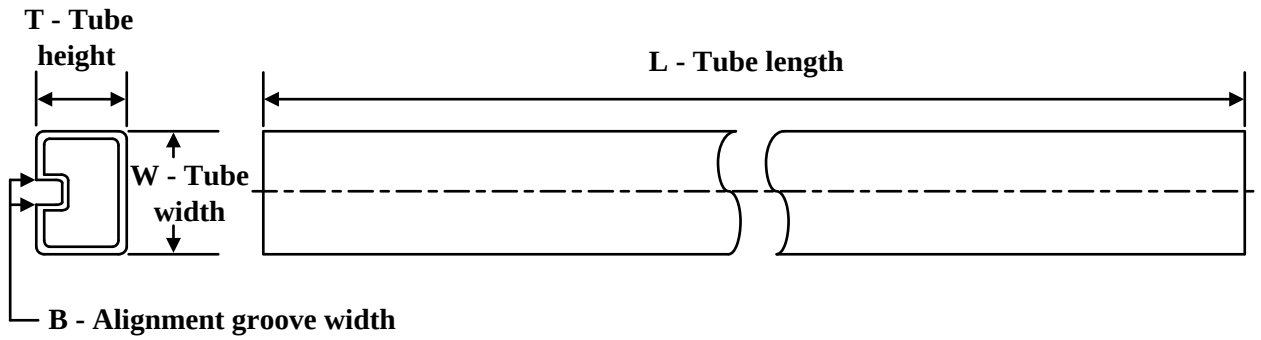
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS60204DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS60205DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

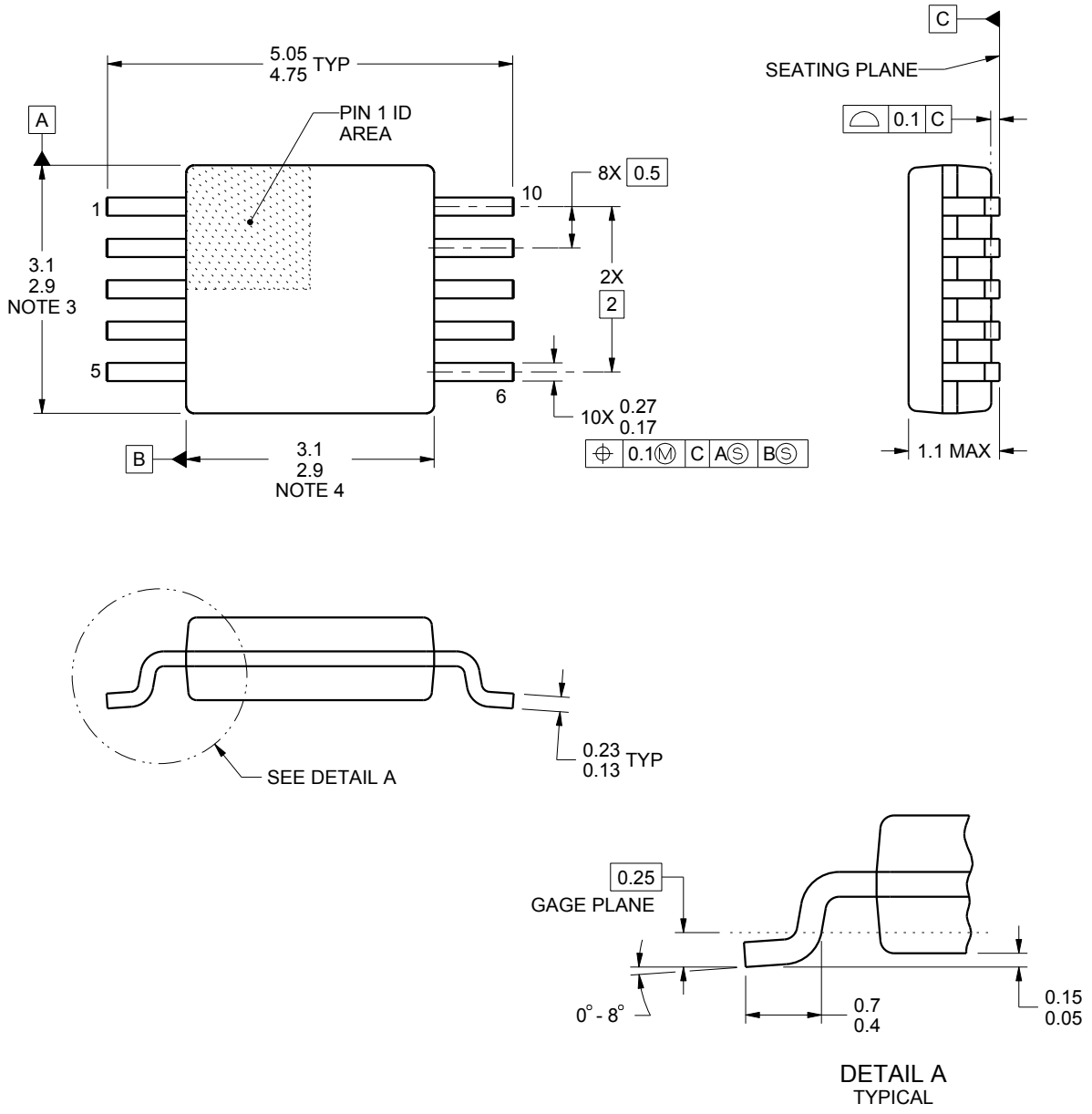
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS60204DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS60204DGS.A	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS60205DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS60205DGS.A	DGS	VSSOP	10	80	331.47	6.55	3000	2.88

PACKAGE OUTLINE

DGS0010A

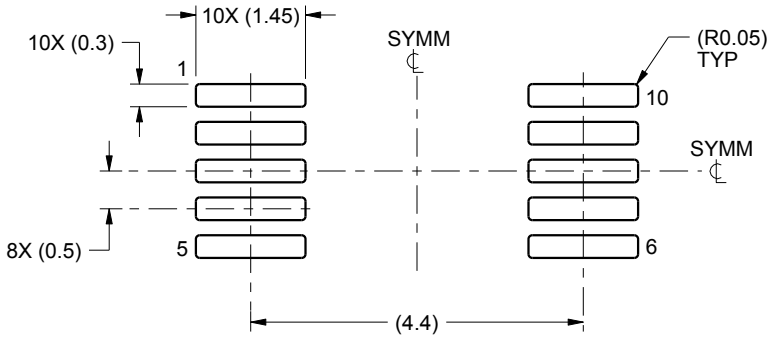
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

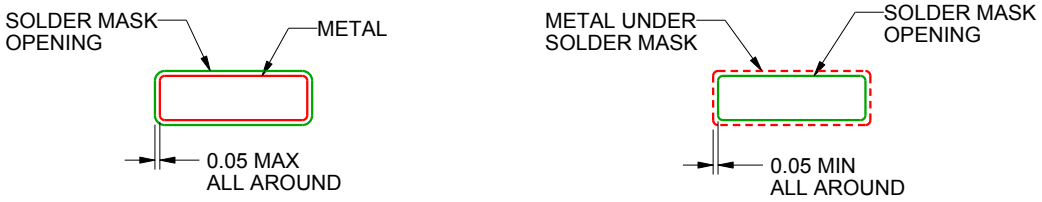


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

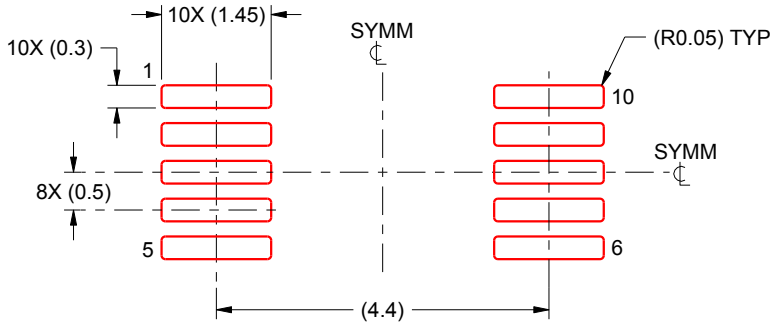


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月