# 适用于汽车应用高频 CPU 内核电源的 TPS59603-Q1 同步降压 FET 驱动器

## 1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 器件温度等级 1：-40°C 至 125°C
  - 器件人体放电模式静电放电 (ESD) 分类等级 H2
  - 器件的组件充电模式 ESD 分类等级 C3B
- 针对已优化连续传导模式 (CCM) 的精简死区时间驱动电路
- 针对已优化断续传导模式 (DCM) 效率的自动零交叉检测
- 针对已优化轻负载效率的多个低功耗模式
- 为了实现高效运行的经优化信号路径延迟
- 集成 BST 开关驱动强度针对低 RdsON FET 进行了优化
- 针对 5V FET 驱动器进行了优化
- 转换输入电压范围 ($V_{IN}$)：2.5V 至 28V
- 具有可湿性侧面和散热焊盘的 2mm × 2mm、8 引脚、WSON 封装

## 2 应用

- 使用高频 CPU 的汽车后座娱乐 (RSE) 平板电脑
- 汽车 ADAS 处理器内核电源

## 3 说明

TPS59603-Q1 驱动器针对高频 CPU $V_{CORE}$ 应用进行了优化，具有 降低 死区时间驱动和自动零交越等高级特性，可用于在整个负载范围内优化效率。

$\overline{SKIP}$ 引脚提供 CCM 操作选项，以支持输出电压的受控管理。此外，TPS59603-Q1 支持两种低功耗模式。借助于脉宽调制 (PWM) 输入三态，静态电流被减少至 130µA，并支持立即响应。当 $\overline{SKIP}$ 被保持在三态时，电流被减少至 8µA（恢复切换通常需要 20µs）。此驱动器与合适的德州仪器 (TI) 控制器配对使用，能够成为出色的高性能电源系统。

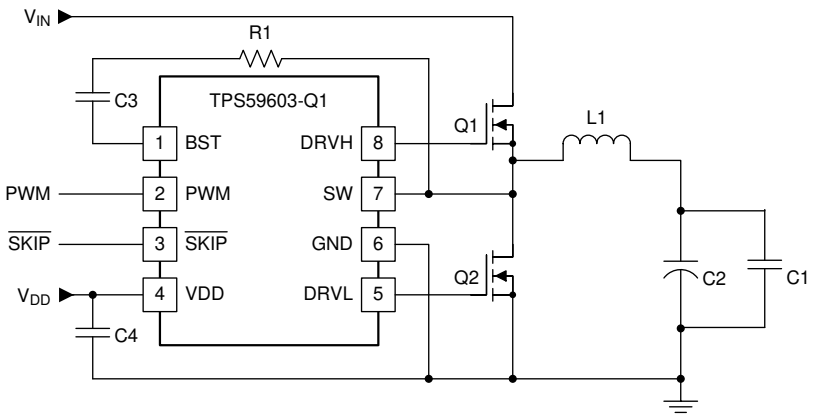
TPS59603-Q1 器件采用节省空间的耐热增强型 8 引脚、2mm x 2mm 可湿性侧面 WSON 封装，工作温度范围为 -40°C 至 125°C。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| TPS59603-Q1 | WSON (8) | 2.00mm × 2.00mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化应用



# 目录



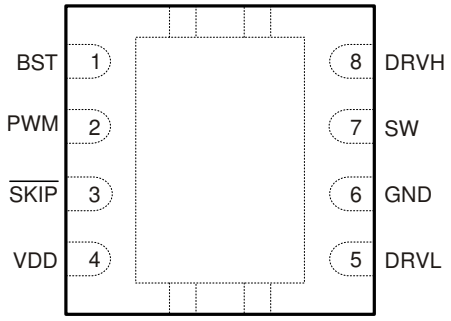
## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

| Changes from Original (January 2020) to Revision A | Page |
|---|---|
| • 已更改 更改了“相关文档”部分的超链接 | 14 |

# 5 Pin Configuration and Functions

**DSG Package**
**8-Pin WSON**
**Top View**




**Pin Functions**

| PIN | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| BST | 1 | I | High-side N-channel FET bootstrap voltage input; power supply for high-side driver |
| DRVH | 8 | O | High-side N-channel gate drive output |
| DRVL | 5 | O | Synchronous low-side N-channel gate drive output |
| GND | 6 | G | Synchronous low-side N-channel gate drive return and device reference |
| PWM | 2 | I | PWM input. A tri-state voltage on this pin turns off both the high-side (DRVH) and low-side drivers (DRVL) |
| $\overline{\text{SKIP}}$ | 3 | I | When $\overline{\text{SKIP}}$ is LO, the zero crossing comparator is active. The power chain enters discontinuous conduction mode when the inductor current reaches zero. When $\overline{\text{SKIP}}$ is HI, the zero crossing comparator is disabled, and the driver outputs follow the PWM input. A tri-state voltage on $\overline{\text{SKIP}}$ puts the driver into a very-low power state. |
| SW | 7 | I/O | High-side N-channel gate drive return. Also, zero-crossing sense input |
| VDD | 4 | I | 5-V power supply input; decouple to GND with a ceramic capacitor with a value of 1 µF or greater |
| Thermal Pad | | G | Tie to system GND plane with multiple vias |

(1) I = Input, O = Output, G = Ground

# 6 Specifications

## 6.1 Absolute Maximum Ratings(1) (2)

over operating free-air temperature (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input voltage | VDD | –0.3 | 6 | V |
| | PWM, $\overline{SKIP}$ | –0.3 | 6 | |
| Output voltage | BST | –0.3 | 35 | V |
| | BST (transient <20 ns) | –0.3 | 38 | |
| | BST to SW; DRVH to SW | –0.3 | 6 | |
| | SW | –2 | 30 | |
| | DRVH, SW (transient <20 ns) | –5 | 38 | |
| | DRVL | –0.3 | 6 | |
| Ground pins | GND to PAD | –0.3 | 0.3 | V |
| Operating junction temperature, $T_J$ | | –40 | 125 | °C |
| Storage temperature range, $T_{stg}$ | | –55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002(1) | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | ±750 | |

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Input voltage | VDD | 4.5 | 5 | 5.5 | V |
| | PWM, $\overline{SKIP}$ | –0.1 | | 5.5 | |
| Output voltage | BST | –0.1 | | 34 | V |
| | BST to SW; DRVH to SW | –0.1 | | 5.5 | |
| | SW | –1 | | 28 | |
| | DRVL | –0.1 | | 5.5 | |
| Ground pins | GND to PAD | –0.1 | | 0.1 | V |
| Operating junction temperature, $T_J$ | | –40 | | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | TPS59603-Q1 WSON (DSG) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 63.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 74.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 34.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 2.0 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 34.9 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 11.7 | °C/W |

(1) 有关传统和新热指标的更多信息，请参见应用报告《*半导体和 IC 封装热指标*》（文献编号：SPRA953）。

## 6.5 Electrical Characteristics

These specifications apply for –40°C ≤ $T_J$ ≤ 125°C, and $V_{VDD}$ = 5 V unless otherwise specified.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **VDD INPUT SUPPLY** | | | | | | |
| $I_{CC}$ | Supply current (operating) | $V_{\overline{SKIP}}$ = $V_{VDD}$ or $V_{\overline{SKIP}}$ = 0 V, PWM = High | | 160 | 600 | µA |
| | | $V_{\overline{SKIP}}$ = $V_{VDD}$ or $V_{\overline{SKIP}}$ = 0 V, PWM = Low | | 250 | | |
| | | $V_{\overline{SKIP}}$ = $V_{VDD}$ or $V_{\overline{SKIP}}$ = 0 V, PWM = Float | | 130 | | |
| | | $V_{\overline{SKIP}}$ = Float | | 8 | | |
| **VDD UNDERVOLTAGE LOCKOUT (UVLO)** | | | | | | |
| $V_{UVLO}$ | UVLO threshold | Rising threshold | | | 4.19 | V |
| | | Falling threshold | 3.65 | | | |
| $V_{UVHYS}$ | UVLO hysteresis | | | 0.2 | | V |
| **PWM AND $\overline{SKIP}$ I/O SPECIFICATIONS** | | | | | | |
| $R_I$ | Input impedance | Pullup to VDD | | 1.7 | | MΩ |
| | | Pulldown (to GND) | | 800 | | kΩ |
| $V_{IL}$ | Low-level input voltage | | | | 0.6 | V |
| $V_{IH}$ | High-level input voltage | | 2.70 | | | V |
| $V_{IHH}$ | Hysteresis | | | 0.2 | | V |
| $V_{TS}$ | Tri-state voltage | | 1.3 | | 2.0 | V |
| $t_{THOLD(off1)}$ | Tri-state activation time (falling) PWM | | | 60 | | ns |
| $t_{THOLD(off2)}$ | Tri-state activation time (rising) PWM | | | 60 | | ns |
| $t_{TSKF}$ | Tri-state activation time (falling) $\overline{SKIP}$ | | | 1 | | µs |
| $t_{TSKR}$ | Tri-state activation time (rising) $\overline{SKIP}$ | | | 1 | | µs |
| $t_{3RD(PWM)}$ | Tri-state exit time PWM | | | | 100 | ns |
| $t_{3RD(\overline{SKIP})}$ | Tri-state exit time $\overline{SKIP}$ | | | | 50 | µs |
| **HIGH-SIDE GATE DRIVER (DRVH)** | | | | | | |
| $t_{R(DRVH)}$ | Rise time | DRVH rising, $C_{DRVH}$ = 3.3 nF; 20% to 80% | | 30 | | ns |
| $t_{RPD(DRVH)}$ | Rise time propogation delay | $C_{DRVH}$ = 3.3 nF | | 40 | | ns |
| $R_{SRC}$ | Source resistance | Source resistance, ($V_{BST}$– $V_{SW}$) = 5 V, high state, ($V_{BST}$ – $V_{DRVH}$) = 0.1 V | | 2 | 4 | Ω |
| $t_{F(DRVH)}$ | Fall time | DRVH falling, $C_{DRVH}$ = 3.3 nF | | 8 | | ns |
| $t_{FPD(DRVH)}$ | Fall-time propagation delay | $C_{DRVH}$ = 3.3 nF | | 25 | | ns |
| $R_{SNK}$ | Sink resistance | Sink resistance, ($V_{BST}$ – $V_{SW}$) forced to 5 V, low state ($V_{DRVH}$ – $V_{SW}$) = 0.1 V | | 0.5 | 1.6 | Ω |
| $R_{DRVH}$ | DRVH to SW resistance(1) | | | 100 | | kΩ |

(1) Specified by design. Not production tested.

## Electrical Characteristics (接下页)

These specifications apply for –40°C ≤ $T_J$ ≤ 125°C, and $V_{VDD}$ = 5 V unless otherwise specified.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **LOW-SIDE GATE DRIVER (DRVL)** | | | | | | |
| $t_{R(DRVL)}$ | Rise time | DRVL rising, $C_{DRVL}$ = 3.3 nF; 20% to 80% | | 15 | | ns |
| $t_{RPD(DRVL)}$ | Rise time propagation delay | $C_{DRVL}$ = 3.3 nF | | 35 | | ns |
| $R_{SRC}$ | Source resistance | Source resistance, ($V_{VDD}$–GND) = 5 V, high state, ($V_{VDD}$ – $V_{DRVL}$) = 0.1 V | | 1.5 | 3 | Ω |
| $t_{F(DRVL)}$ | Fall time | DRVL falling, $C_{DRVL}$ = 3.3 nF | | 10 | | ns |
| $t_{FPD(DRVL)}$ | Fall-time propagation delay | $C_{DRVL}$= 3.3 nF | | 15 | | ns |
| $R_{SNK}$ | Sink resistance | Sink resistance, ($V_{VDD}$– GND) = 5 V, low state, ($V_{DRVL}$ – GND) = 0.1 V | | 0.4 | 1.6 | Ω |
| $R_{DRVL}$ | DRVL to GND resistance(1) | | | 100 | | kΩ |
| **GATE DRIVER DEAD-TIME** | | | | | | |
| $t_{R(DT)}$ | Rising edge | | 0 | 20 | 40 | ns |
| $t_{F(DT)}$ | Falling edge | | 0 | 10 | 25 | ns |
| **ZERO CROSSING COMPARATOR** | | | | | | |
| $V_{ZX}$ | Zero crossing offset | SW voltage rising | –2.25 | 0 | 2.00 | mV |
| **BOOTSTRAP SWITCH** | | | | | | |
| $V_{FBST}$ | Forward voltage | $I_F$ = 10 mA | | 120 | 240 | mV |
| $I_{RLEAK}$ | Reverse leakage | ($V_{BST}$ – $V_{VDD}$) = 25 V | | | 2 | µA |
| $R_{DS(on)}$ | On-resistance | | | 12 | 24 | Ω |

## 6.6 Typical Characteristics

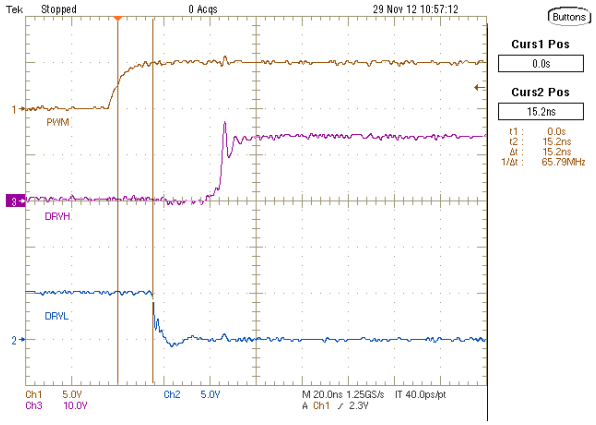



图 1. PWM High to DRVL Low

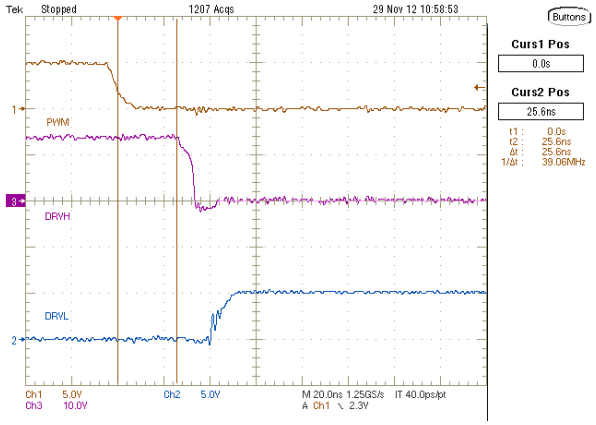



图 2. PWM Low to DRVH Low

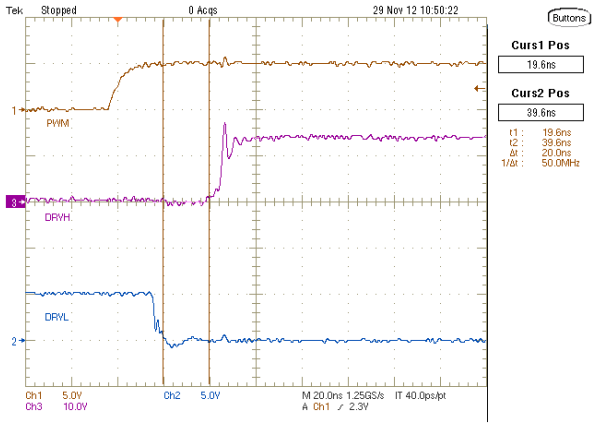



图 3. DRVL Low to DRVH High

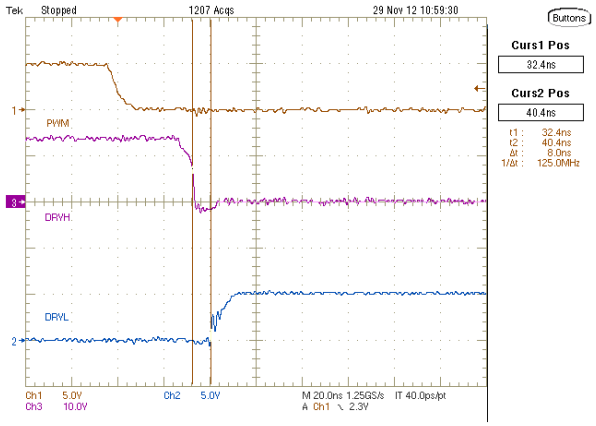



图 4. DRVH Low to DRVL High

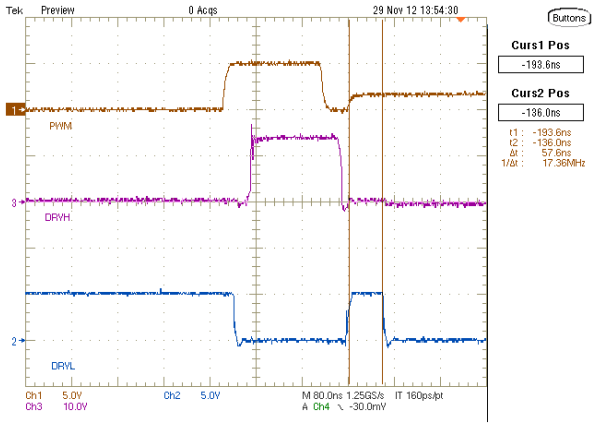



图 5. PWM Low to Tri-State

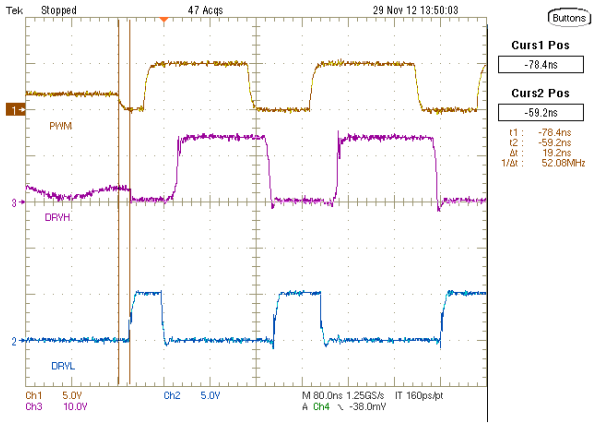



图 6. PWM Tri-State to Low

## Typical Characteristics (接下页)

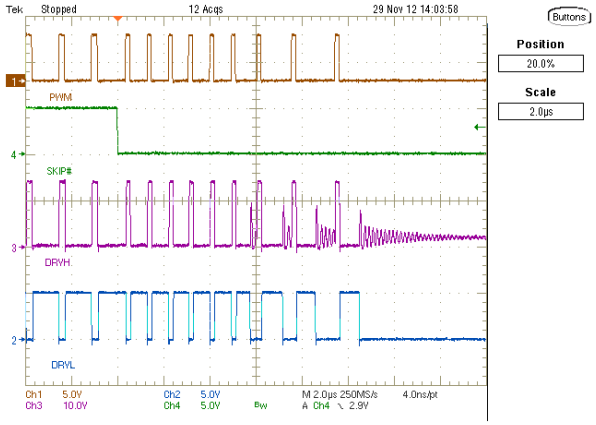



图 7. SKIP Mode Entry

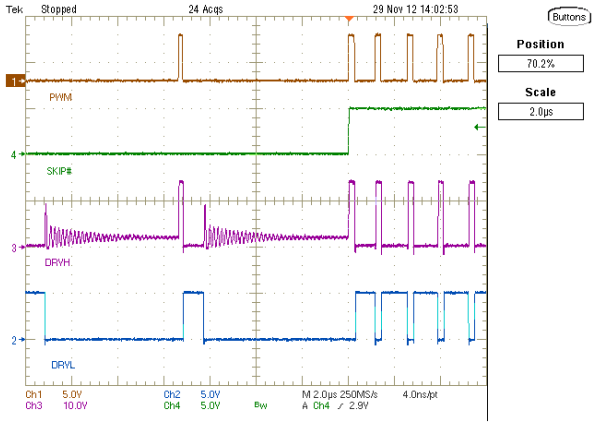



图 8. SKIP Mode Exit

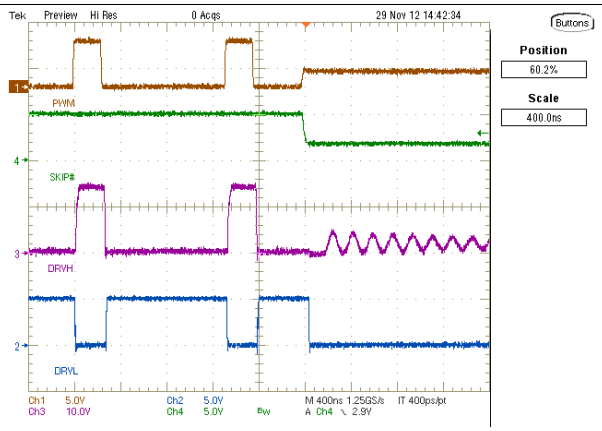



图 9. Very-Low-Power Mode Entry

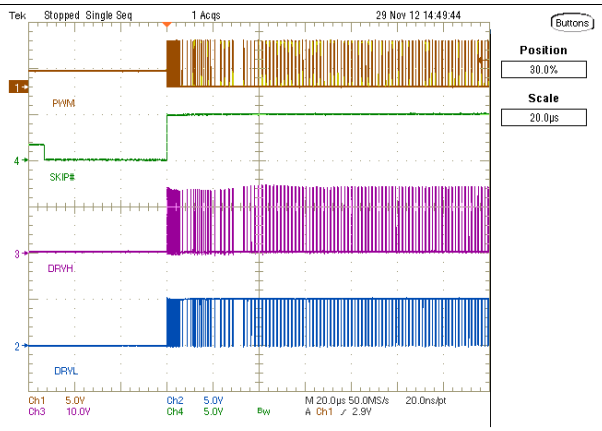
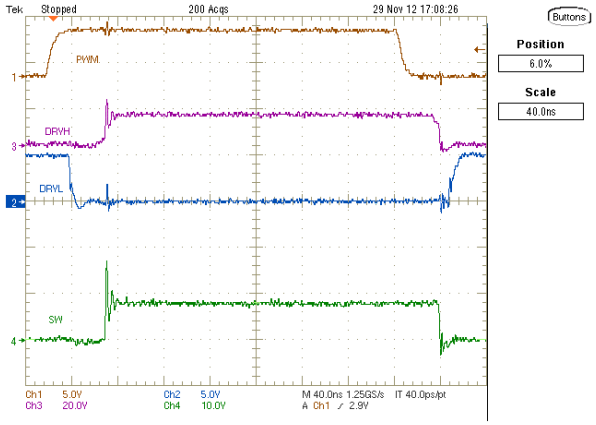
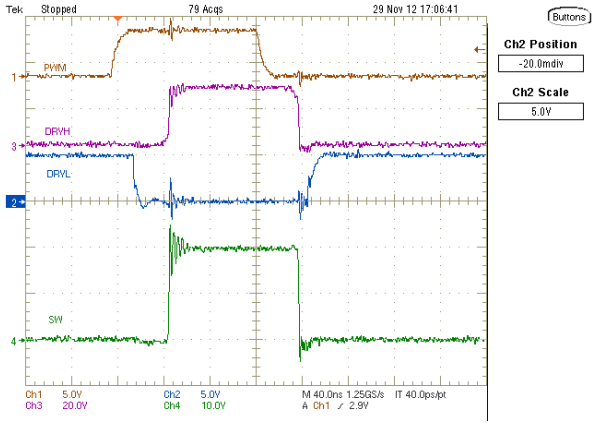



图 10. Very-Low-Power Mode Exit




$V_{IN}$ = 8 V

图 11. SW Node-Ringing




$V_{IN}$ = 20 V

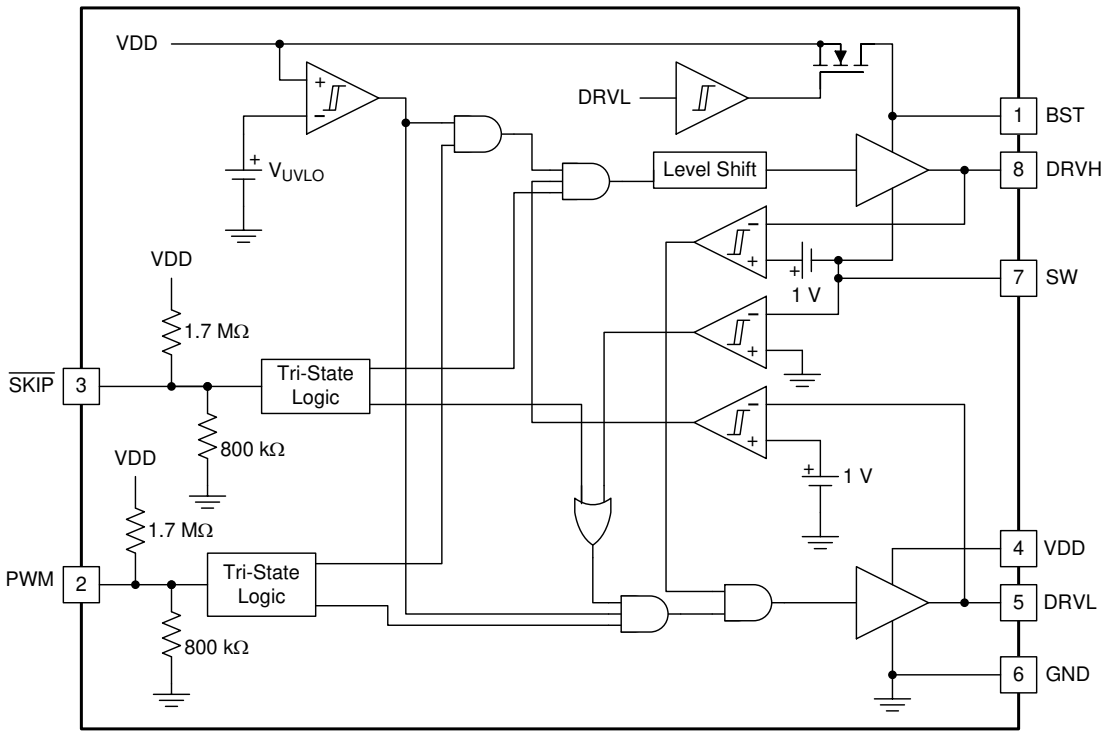
图 12. SW Node-Ringing

# 7 Detailed Description

## 7.1 Overview

The TPS59603-Q1 device is a synchronous-buck MOSFET driver designed to drive both high-side and low-side MOSFETs. It allows high-frequency operation with current driving capability matched to the application. The integrated boost switch is internal. The TPS59603-Q1 device employs dead-time reduction control and shoot-through protection, which helps avoid simultaneous conduction of high-side and low-side MOSFETs. Also, the drivers improve light-load efficiency with integrated DCM-mode operation using adaptive crossing detection. Typical applications yield a steady-state duty cycle of 60% or less. For high steady-state duty cycle applications, including a small external Schottky diode may help to ensure sufficient charging of the bootstrap capacitor.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

### 7.3.1 UVLO Protection

The UVLO comparator evaluates the VDD voltage level. As $V_{VDD}$ rises, both DRVH and DRVL hold actively low at all times until $V_{VDD}$ reaches the higher UVLO threshold ($V_{UVLO\_H}$). Then, the driver becomes operational and responds to PWM and $\overline{SKIP}$ commands. If VDD falls below the lower UVLO threshold ($V_{UVLO\_L}$ = $V_{UVLO\_H}$ – Hysteresis), the device disables the driver and drives the outputs of DRVH and DRVL actively low. 图 13 shows this function.

**CAUTION**

Do not start the driver in the very low power mode ($\overline{SKIP}$ = Tri-state).

## Feature Description (接下页)

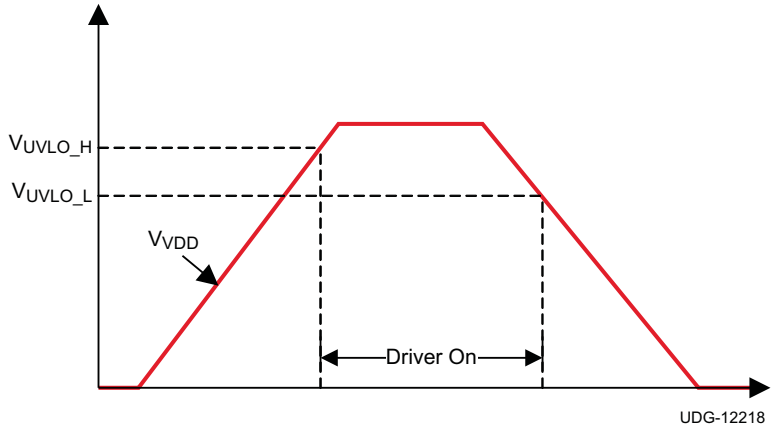



**图 13. UVLO Operation**

### 7.3.2 PWM Pin

The PWM pin incorporates an input tri-state function. The device forces the gate driver outputs to low when PWM is driven into the tri-state window and the driver enters a low power state with zero exit latency. The pin incorporates a weak pullup to maintain the voltage within the tri-state window during low-power modes. Operation into and out of a tri-state condition follows the timing diagram outlined in 图 14.

When VDD reaches the UVLO_H level, a tri-state voltage range (window) is set for the PWM input voltage. The window is defined as the PWM voltage range between PWM logic high ($V_{IH}$) and logic low ($V_{IL}$) thresholds. The device sets high-level input voltage and low-level input voltage threshold levels to accommodate both 3.3-V (typical) and 5-V (typical) PWM drive signals.

When the PWM exits the tri-state condition, the driver enters CCM for a period of 4 µs, regardless of the state of the $\overline{SKIP}$ pin. Typical operation requires this time period in order for the auto-zero comparator to resume.

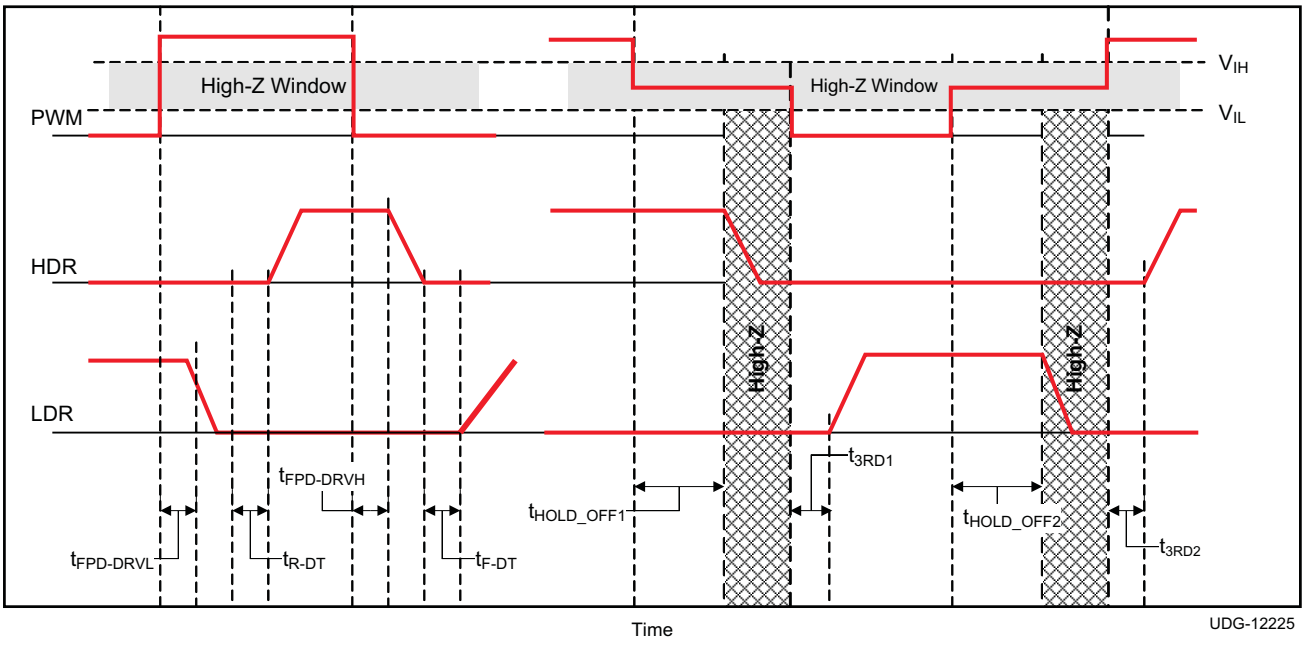



**图 14. PWM Tri-State Timing Diagram**

## Feature Description (接下页)

### 7.3.3 $\overline{\text{SKIP}}$ Pin

The $\overline{\text{SKIP}}$ pin incorporates the input tri-state buffer as PWM. The function is somewhat different. When $\overline{\text{SKIP}}$ is low, the zero crossing (ZX) detection comparator is enabled, and DCM mode operation occurs if the load current is less than the critical current. When $\overline{\text{SKIP}}$ is high, the ZX comparator disables, and the converter enters FCCM mode. When the $\overline{\text{SKIP}}$ pin is in a tri-state condition, typical operation forces the gate driver outputs low and the driver enters a very-low-power state. In the low-power state, the UVLO comparator remains off to reduce quiescent current. When the $\overline{\text{SKIP}}$ pin voltage is pulled either low or high, the driver wakes up and is able to accept PWM pulses in less than 50 µs.

表 1 shows the logic functions of UVLO, PWM, $\overline{\text{SKIP}}$, DRVH, and DRVL.

**表 1. Logic Functions**

| UVLO | PWM | $\overline{\text{SKIP}}$ | DRVL | DRVH | MODE |
|---|---|---|---|---|---|
| Active | — | — | Low | Low | Disabled |
| Inactive | Low | Low | High(1) | Low | DCM(1) |
| Inactive | Low | High | High | Low | FCCM |
| Inactive | High | H or L | Low | High | |
| Inactive | Tri-state | H or L | Low | Low | Low power |
| Inactive | — | Tri-state | Low | Low | Very-low power |

(1) Until zero crossing protection occurs.

#### *7.3.3.1 Zero Crossing (ZX) Operation*

The zero crossing comparator is adaptive for improved accuracy. As the output current decreases from a heavy load condition, the inductor current also reduces and eventually arrives at a *valley*, where it touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The SW pin detects the zero-current condition. When this zero inductor current condition occurs, the ZX comparator turns off the rectifying MOSFET.

### 7.3.4 Adaptive Dead-Time Control and Shoot-Through Protection

The driver utilizes an anti-shoot-through and adaptive dead-time control to minimize low-side body diode conduction time and maintain high efficiency. When the PWM input voltage becomes high, the low-side MOSFET gate voltage begins to fall after a propagation delay. At the same time, DRVL voltage is sensed, and high-side driving voltage starts to increase after DRVL voltage is lower than a proper threshold.

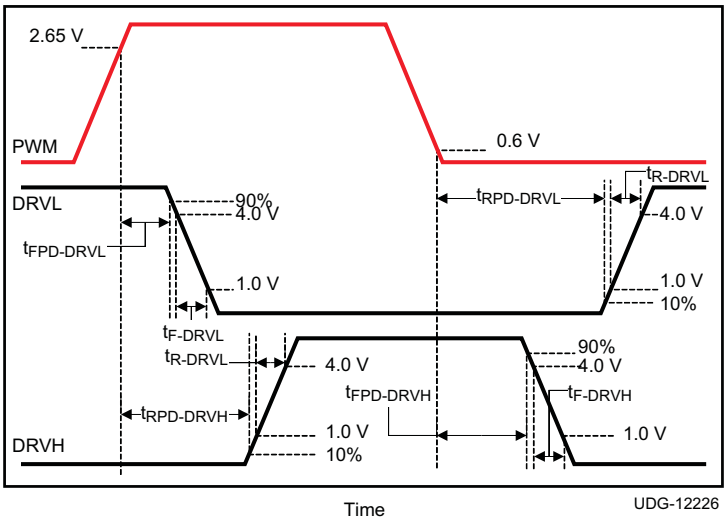



**图 15. Rise and Fall Timing and Propagation Delay Definitions**

Typical operation manages to near zero the dead-time between the low-side gate turn-off to high-side gate voltage turn-on, and high-side gate turn-off to low-side gate turn-on, in order to avoid simultaneous conduction of both MOSFETs, as well as to reduce body diode conduction and recovery losses. This operation also reduces ringing on the leading edge of the SW waveform.

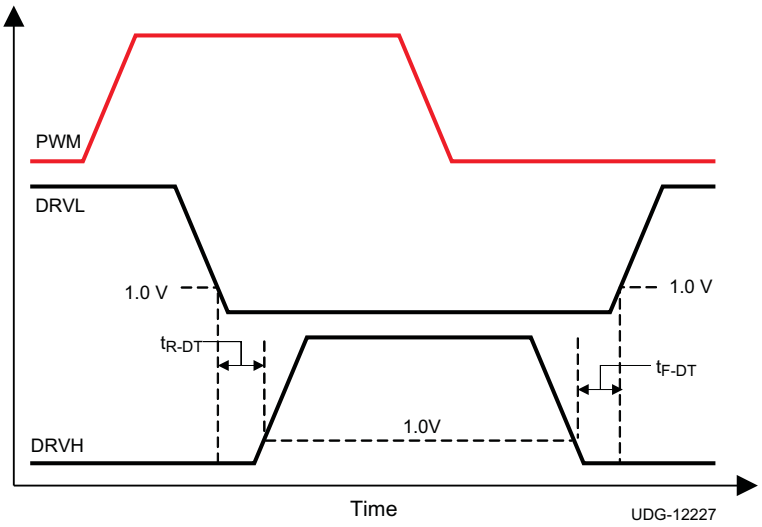



**图 16. Dead-Time Definitions**

### 7.3.5 Integrated Boost-Switch

To maintain a BST-SW voltage close to VDD (to get lower conduction losses on the high-side FET), the conventional diode between the VDD pin and BST pin is replaced by a FET, which is gated by the DRVL signal.

## 7.4 Device Functional Modes

The TPS59603-Q1 device operates in CCM mode when the $\overline{\text{SKIP}}$ pin is high, and it enters DCM mode when the $\overline{\text{SKIP}}$ pin is low. When both the $\overline{\text{SKIP}}$ pin and the PWM pin are in a tri-state condition, it forces the gate driver outputs low and the driver enters a very-low-power state.

# 8 Power Supply Recommendations

The voltage range for the VDD pin is between 4.5 V and 5.5 V. A 5-V power supply is recommended for the VDD pin of the TPS59603-Q1 device.

# 9 Layout

## 9.1 Layout Guidelines

To improve the switching characteristics and design efficiency, these layout rules must be considered:

- Locate the driver as close as possible to the MOSFETs.
- Locate the VDD and bootstrap capacitors as close as possible to the driver.
- Pay special attention to the GND trace. Use the thermal pad of the package as the GND by connecting it to the GND pin. The GND trace or pad from the driver goes directly to the source of the MOSFET, but should not include the high current path of the main current flowing through the drain and source of the MOSFET.
- Use a similar rule for the switch-node as for the GND.
- Use wide traces for DRVH and DRVL closely following the related SW and GND traces. A width of between 80 and 100 mils is preferable where possible.
- Place the bypass capacitors as close as possible to the driver.
- Avoid PWM and enable traces going close to the SW and pad where high dV/dT voltage can induce significant noise into the relatively high-impedance leads.

A poor layout can decrease the reliability of the entire system.

## 9.2 Layout Recommendation

图 17 above shows the primary current loops in each phase, numbered in order of importance.

The most important loop to minimize the area of is loop 1, the path from the input capacitor through the high and low-side FETs, and back to the capacitor through ground.

Loop 2 is from the inductor through the output capacitor, ground, and Q2. The layout of the low-side gate drive (Loops 3a and 3b) is important. The guidelines for the gate drive layout are:

- Make the low-side gate drive length as short as possible (1 inch or less preferred).
- Make the DRVL width to length ratio of 1:10, wider (1:5) if possible.
- If changing layers is necessary, use at least two vias.

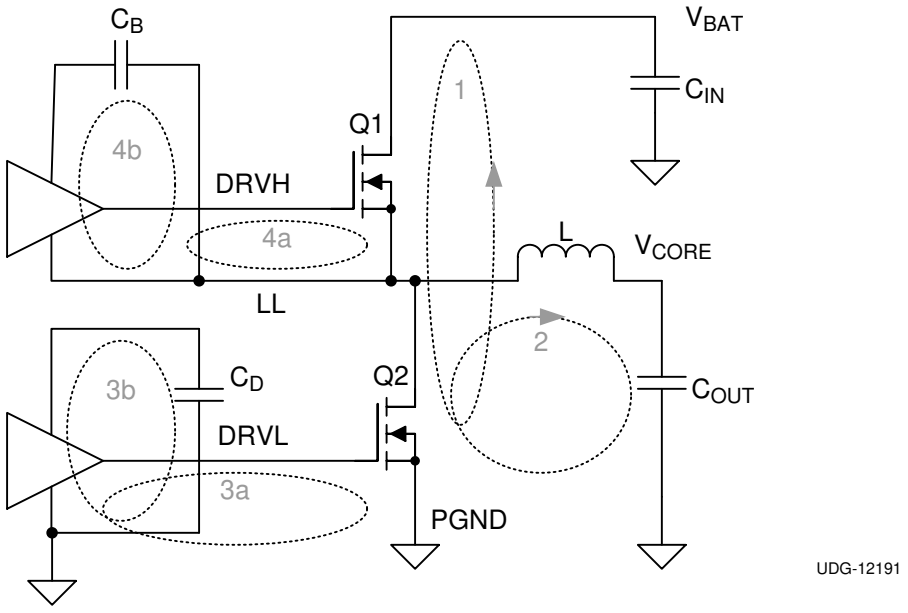



**图 17. Layout recommendations to minimize major Current loops**

# 10 器件和文档支持

## 10.1 器件支持

### 10.1.1 开发支持

有关 Power Stage Designer，请转到常用开关模式电源的 Power Stage Designer™ 工具

## 10.2 文档支持

### 10.2.1 相关文档

《适用于汽车 ADAS 应用的 TPS59632-Q1 2.5V 至 24V、三相/两相/单相降压无驱动器控制器》数据表

## 10.3 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 10.4 商标

E2E is a trademark of Texas Instruments.

## 10.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

## 10.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 11 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS59603QDSGRQ1 | Active | Production | WSON (DSG) \| 8 | 3000 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | 603Q |
| TPS59603QDSGRQ1.A | Active | Production | WSON (DSG) \| 8 | 3000 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | 603Q |
| TPS59603QDSGTQ1 | Active | Production | WSON (DSG) \| 8 | 250 \| SMALL T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | 603Q |
| TPS59603QDSGTQ1.A | Active | Production | WSON (DSG) \| 8 | 250 \| SMALL T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | 603Q |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

# GENERIC PACKAGE VIEW

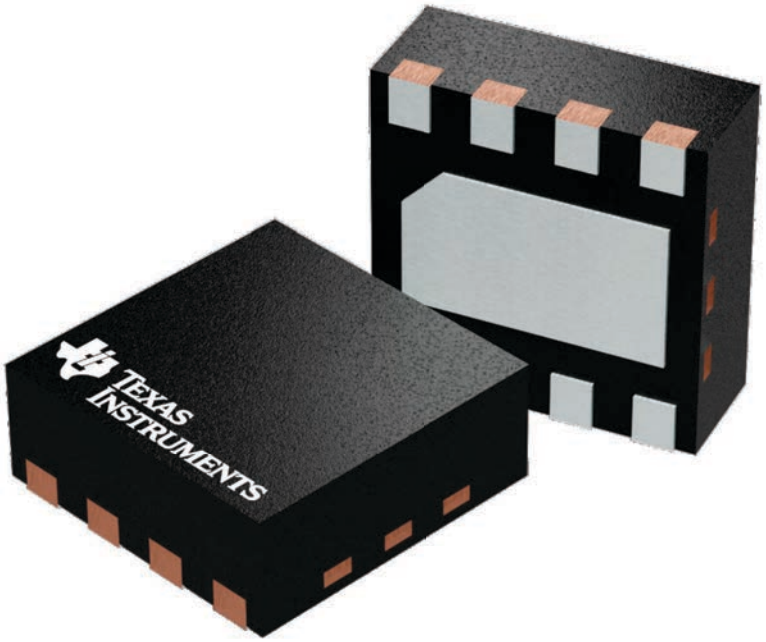
## DSG 8

## WSON - 0.8 mm max height

**2 x 2, 0.5 mm pitch**

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



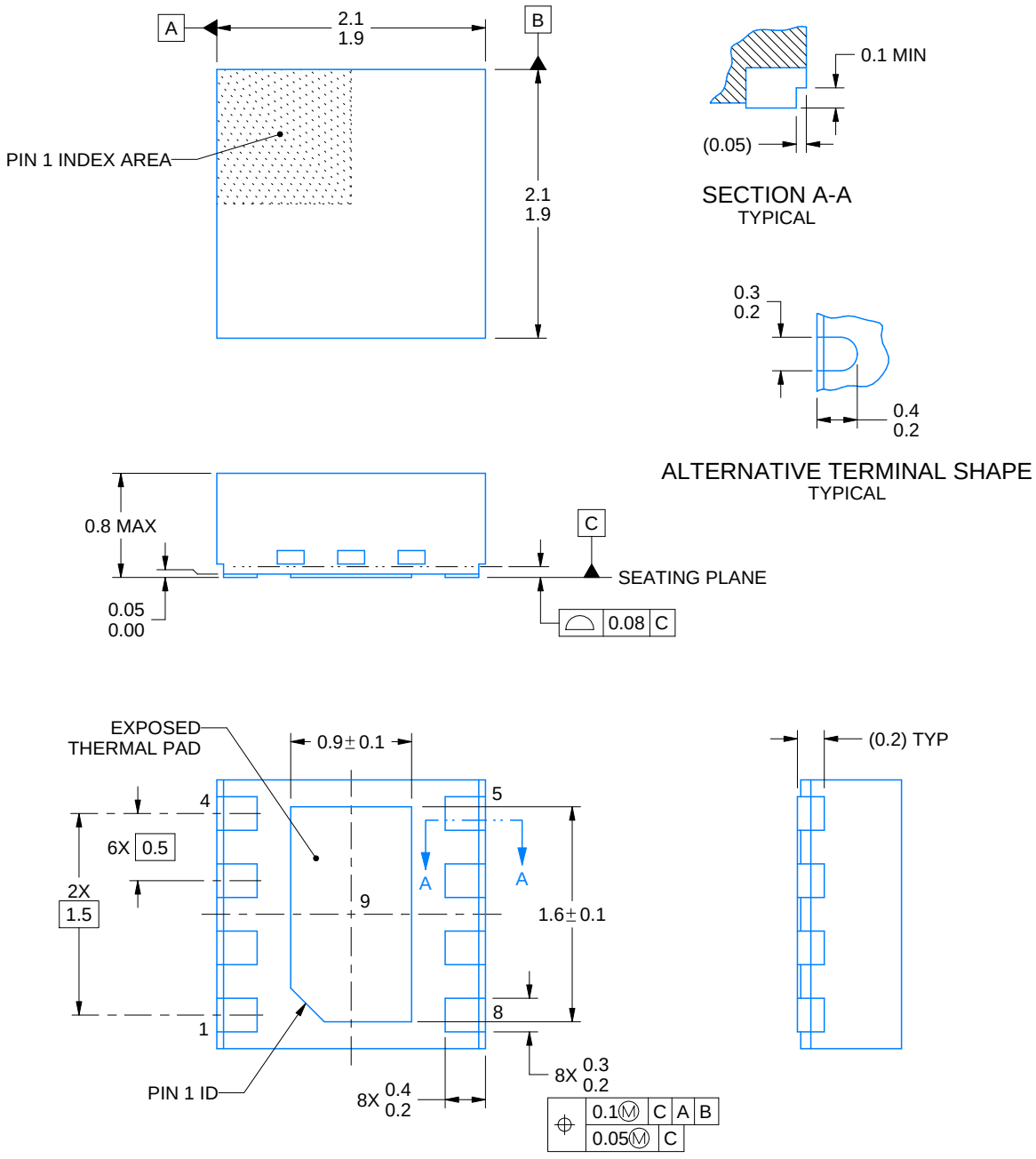

4224783/A

# PACKAGE OUTLINE

## DSG0008B

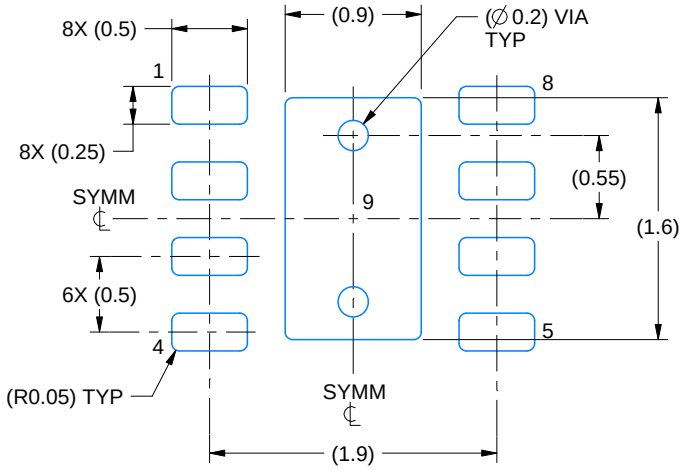
## WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

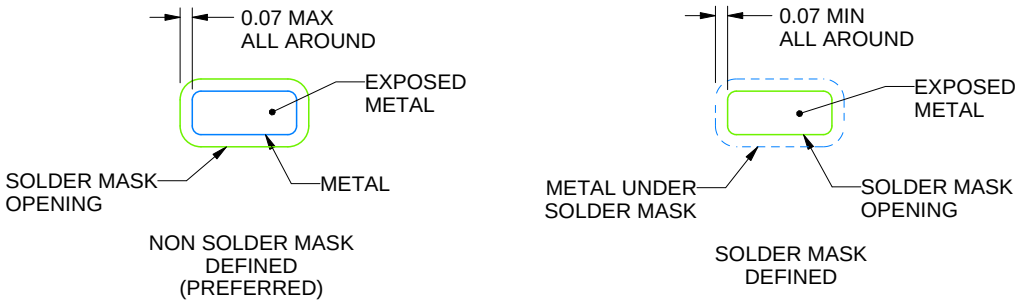



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X




SOLDER MASK DETAILS

4222124/E 05/2020

NOTES: (continued)

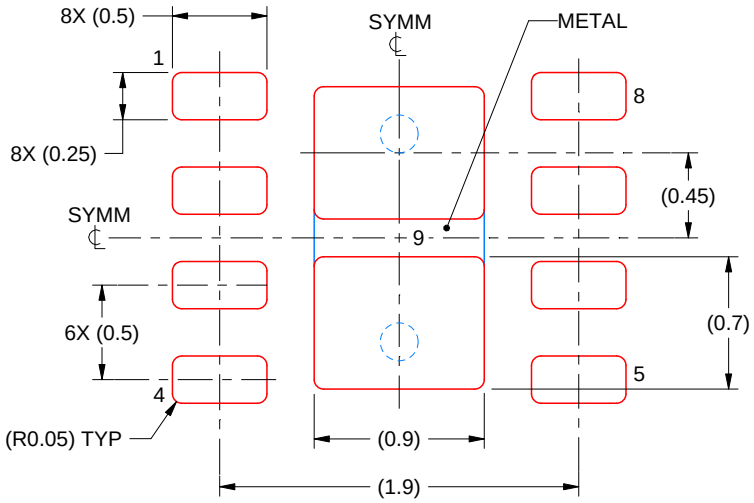
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

## DSG0008B

## WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222124/E 05/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# 重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。



最后更新日期：2025 年 10 月