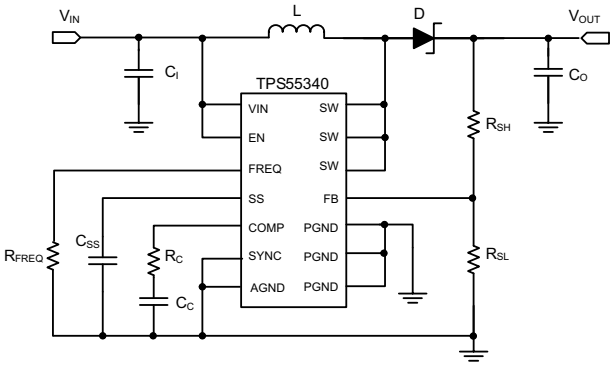
TPS55340 集成式 5A 宽输入范围升压/SEPIC/反激式直流/直流稳压器

1 特性

- 内部 5A、40V 低侧 MOSFET 开关
- 2.9V 至 32V 输入电压范围
- ±0.7% 基准电压
- 0.5mA 静态工作电流
- 2.7μA 关断电源电流
- 固定频率电流模式 PWM 控制
- 频率在 100kHz 至 1.2MHz 之间可调
- 可与外部时钟同步
- 软启动时间可调节
- 用于在轻负载时实现较高效率的脉冲跳跃模式
- 逐周期电流限制、热关断和 UVLO 保护
- QFN-16 (3mm × 3mm) 和 HTSSOP-14 封装，带有 PowerPAD™
- 宽 T_J 运行范围：–40°C 至 150°C
- 使用 TPS55340 并借助 WEBENCH Power Designer 创建定制设计方案

2 应用

- 3.3V、5V、12V、24V 功率转换
- 升压、SEPIC 和反激式拓扑结构
- 适用于平板电脑和便携式个人电脑的 Thunderbolt 端口、USB Type-C 功率传输和电源扩展坞
- 工业电源系统
- ADSL 调制解调器



典型应用（升压）

3 说明

TPS55340 是一款具有集成式 5A、40V 电源开关的单片非同步开关稳压器。此器件可配置成多种标准开关稳压器拓扑，包括升压、SEPIC 和隔离反激式。此器件具有一个宽输入电压范围，可支持由多节电池或经 3.3V、5V、12V 和 24V 稳压电源轨供电的应用。

TPS55340 使用电流模式 PWM（脉宽调制）控制来调节输出电压，并装有一个内部振荡器。PWM 的开关频率由一个外部电阻器或者同步至一个外部时钟信号进行设定。用户可在 100kHz 至 1.2MHz 之间对开关频率进行设定。

此器件具有可编程软启动功能，可限制启动期间的浪涌电流，并且还具有其他内置保护特性，包括逐周期过流限制和热关断。

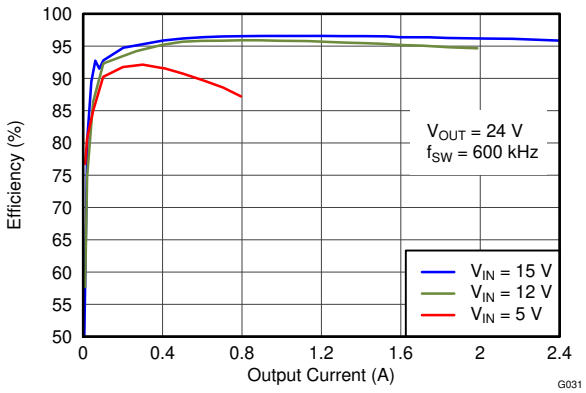
TPS55340 采用具有 PowerPAD 的小型 3mm × 3mm 16 引脚 QFN 封装以及 14 引脚 HTSSOP 封装，增强了热性能。

采用 HTSSOP-14 封装的 5A、40V TPS55340 升压转换器与 3A、40V TPS61175 能够实现引脚对引脚兼容，并且将最大输入电压从 18V 扩展至 32V。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
TPS55340	HTSSOP (14)	5.00mm × 4.40mm
	WQFN (16)	3.00mm × 3.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。



效率与输出电流间的关系

Table of Contents

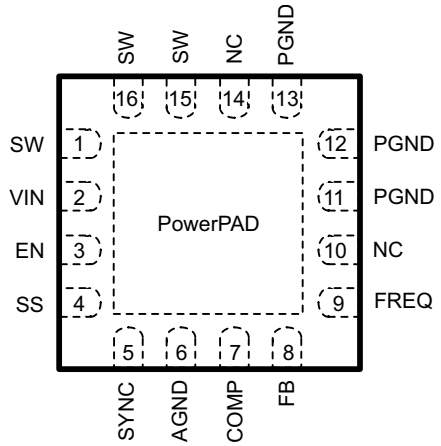
4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (June 2019) to Revision E (September 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1

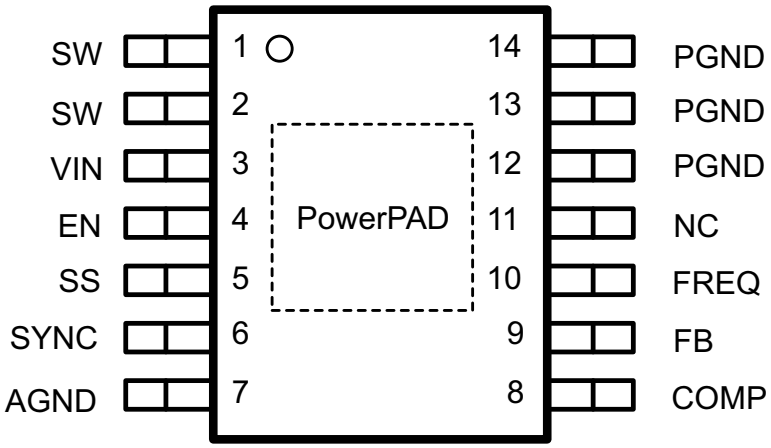
Changes from Revision C (October 2014) to Revision D (June 2019)	Page
• Added text note under pin configuration diagrams.	3

5 Pin Configuration and Functions



TI recommends connecting NC with AGND.

图 5-1. RTE Package 16-Pin WQFN Top View



TI recommends connecting NC with AGND.

图 5-2. PWP Package 14-Pin HTSSOP (Top View)

表 5-1. Pin Functions

PIN			DESCRIPTION
NAME	QFN-16	HTSSOP-14	
AGND	6	7	Signal ground of the IC
COMP	7	8	Output of the transconductance error amplifier. An external RC network connected to this pin compensates the regulator feedback loop.
EN	3	4	Enable pin. When the voltage of this pin falls below the enable threshold for more than 1 ms, the IC turns off.
FB	8	9	Error amplifier input and feedback pin for positive voltage regulation. Connect to the center tap of a resistor divider to program the output voltage.
FREQ	9	10	Switching frequency program pin. An external resistor connected between the FREQ pin and AGND sets the switching frequency.
NC	10, 14	11	Reserved pin that must be connected to ground
PGND	11, 12, 13	12, 13, 14	Power ground of the IC. It is connected to the source of the internal power MOSFET switch.
PowerPAD	—	—	The PowerPAD should be soldered to the AGND. If possible, use thermal vias to connect to internal ground plane for improved power dissipation.
SS	4	5	Soft-start programming pin. A capacitor between the SS pin and AGND pin programs soft-start timing.
SW	1, 15, 16	1, 2	SW is the drain of the internal power MOSFET. Connect SW to the switched side of the boost or SEPIC inductor or the flyback transformer.
SYNC	5	6	Switching frequency synchronization pin. An external clock signal can be used to set the switching frequency between 200 kHz and 1.0 MHz. If not used, this pin should be tied to AGND.
VIN	2	3	The input supply pin to the IC. Connect VIN to a supply voltage between 2.9 V and 32 V. It is acceptable for the voltage on the pin to be different from the boost power stage input.

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltages on pin VIN(2)	– 0.3	34	V
Voltage on pin EN(2)	– 0.3	34	V
Voltage on pins FB, FREQ, and COMP(2)	– 0.3	3	V
Voltage on pin SS(2)	– 0.3	5	V
Voltage on pin SYNC(2)	– 0.3	7	V
Voltage on pin SW(2)	– 0.3	40	V
Operating junction temperature	– 40	150	°C
Storage temperature, T_{stg}	– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under 节 6.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.9		32	V
V_{OUT}	Output voltage range	V_{IN}		38	V
V_{EN}	EN voltage range	0		32	V
V_{SYN}	External switching frequency logic input range	0		5	V
T_A	Operating free-air temperature	– 40		125	°C
T_J	Operating junction temperature	– 40		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS55340		UNIT
		QFN (16 PINS)	HTSSOP (14 PINS)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.3	43.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.7	33.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	14.5	28.3	
ψ_{JT}	Junction-to-top characterization parameter	0.4	1.3	
ψ_{JB}	Junction-to-board characterization parameter	14.5	28.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.5	3.9	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

V_{IN} = 5 V, T_J = –40°C to 150°C, unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage range		2.9		32	V
I_Q	Operating quiescent current into V_{IN}	Device nonswitching, V_{FB} = 2 V		0.5		mA
I_{SD}	Shutdown current	EN = GND		2.7	10	μA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling		2.5	2.7	V
V_{hys}	Undervoltage lockout hysteresis		120	140	160	mV
ENABLE AND REFERENCE CONTROL						
V_{EN}	EN threshold voltage	EN rising input	0.9	1.08	1.30	V
V_{EN}	EN threshold voltage	EN falling input	0.74	0.92	1.125	V
V_{ENh}	EN threshold hysteresis			0.16		V
R_{EN}	EN pulldown resistor		400	950	1600	kΩ
T_{off}	Shutdown delay, SS discharge	EN high to low		1.0		ms
V_{SYNh}	SYN logic high voltage		1.2			V
V_{SYNl}	SYN logic low voltage				0.4	V
VOLTAGE AND CURRENT CONTROL						
V_{REF}	Voltage feedback regulation voltage		1.204	1.229	1.254	V
		T_A = 25°C	1.220	1.229	1.238	
I_{FB}	Voltage feedback input bias current	T_A = 25°C		1.6	20	nA
I_{sink}	COMP pin sink current	V_{FB} = V_{REF} + 200 mV, V_{COMP} = 1 V		42		μA
I_{source}	COMP pin source current	V_{FB} = V_{REF} – 200 mV, V_{COMP} = 1 V		42		μA
V_{CCLP}	COMP pin clamp voltage	High Clamp, V_{FB} = 1 V		3.1		V
		Low Clamp, V_{FB} = 1.5 V		0.75		
V_{CTH}	COMP pin threshold	Duty cycle = 0%		1.04		V
G_{ea}	Error amplifier transconductance		240	360	440	μS
R_{ea}	Error amplifier output resistance			10		MΩ
f_{ea}	Error amplifier crossover frequency			500		kHz
FREQUENCY						
f_{SW}	Frequency	R_{FREQ} = 480 kΩ	75	94	130	kHz
		R_{FREQ} = 80 kΩ	460	577	740	
		R_{FREQ} = 40 kΩ	920	1140	1480	
D_{max}	Maximum duty cycle	V_{FB} = 1.0 V, R_{FREQ} = 80 kΩ	89%	96%		
V_{FREQ}	FREQ pin voltage			1.25		V
T_{min_on}	Minimum on pulse width	R_{FREQ} = 80 kΩ		77		ns
POWER SWITCH						
$R_{DS(ON)}$	N-channel MOSFET on-resistance	V_{IN} = 5 V		60	110	mΩ
		V_{IN} = 3 V		70	120	
I_{LN_NFET}	N-channel leakage current	V_{DS} = 25 V, T_A = 25°C			2.1	μA
OCP and SS						
I_{LIM}	N-channel MOSFET current limit	D = D_{max}	5.25	6.6	7.75	A
I_{SS}	Soft-start bias current	V_{SS} = 0 V		6		μA
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			165		°C

V_{IN} = 5 V, T_J = –40°C to 150°C, unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{hysteresis}$	Thermal shutdown threshold hysteresis			15		°C

6.6 Typical Characteristics

V_{IN} = 5 V, T_A = 25°C (unless otherwise noted)

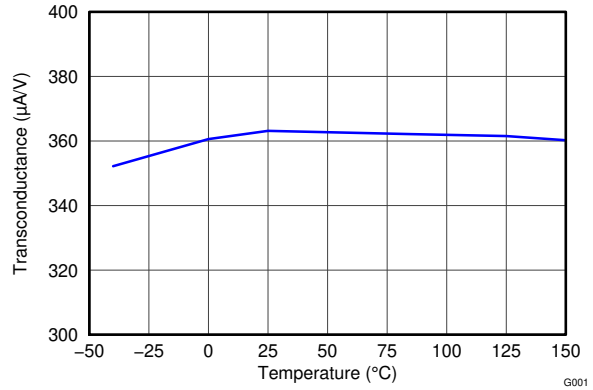


图 6-1. Error Amplifier Transconductance vs Temperature

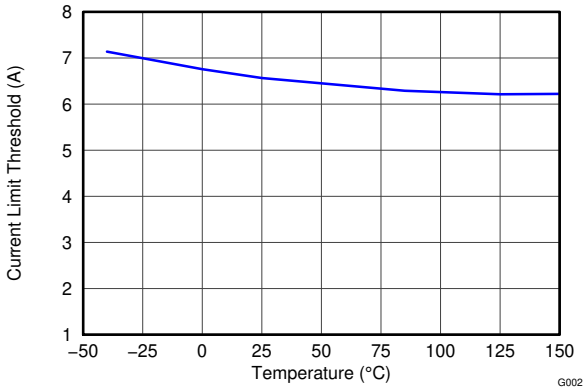


图 6-2. Switch Current Limit vs Temperature

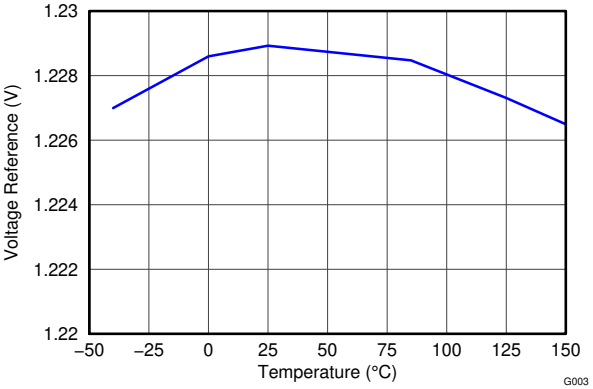


图 6-3. Feedback Voltage Reference vs Temperature

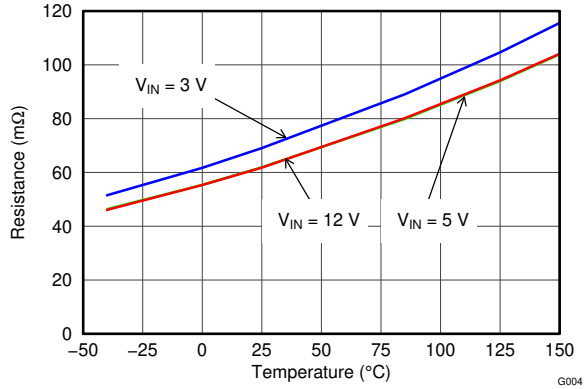


图 6-4. $R_{DS(ON)}$ vs Temperature

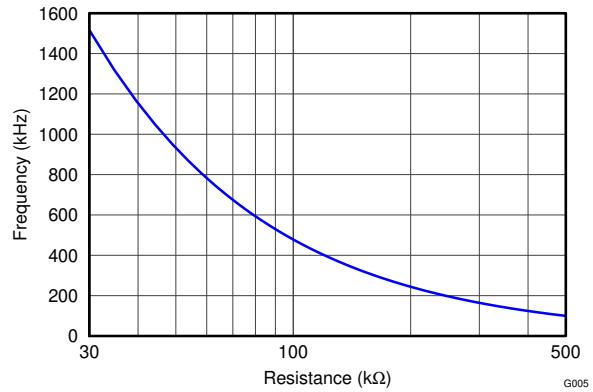


图 6-5. Frequency vs FREQ Resistance

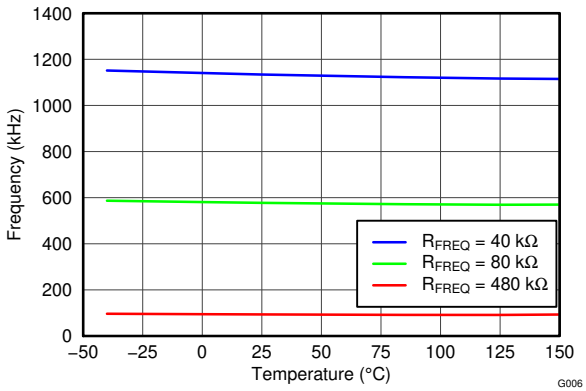


图 6-6. Frequency vs Temperature

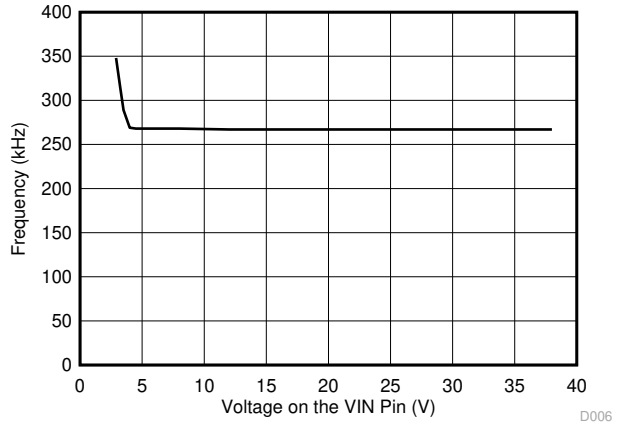


图 6-7. Minimum Switching Frequency for Quick Recovery from Frequency Foldback

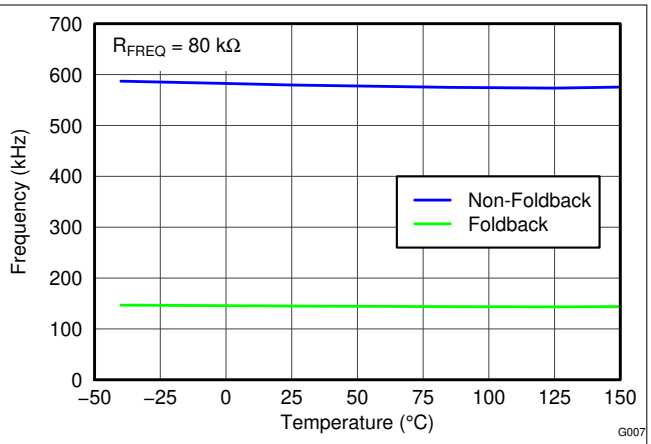


图 6-8. Nonfoldback Frequency vs Foldback Frequency

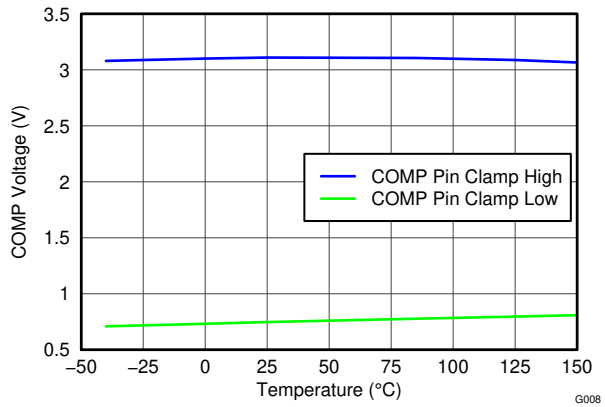


图 6-9. COMP Clamp Voltage vs Temperature

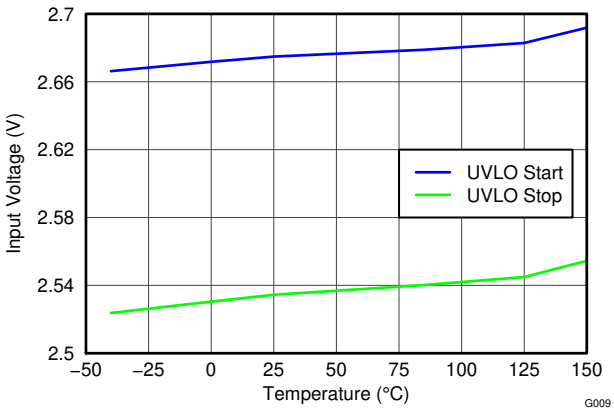


图 6-10. Input Voltage UVLO vs Temperature

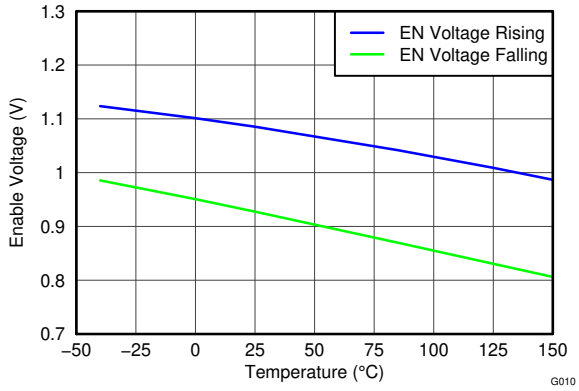


图 6-11. Enable Voltage vs Temperature

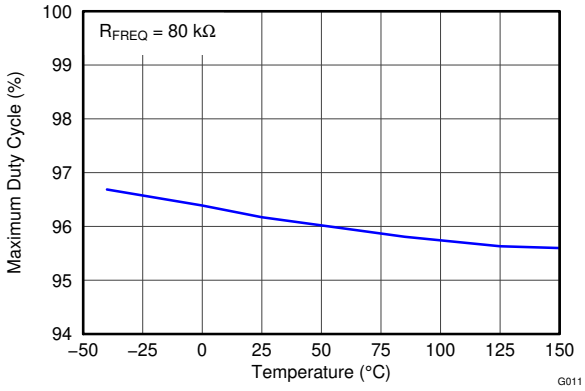


图 6-12. Maximum Duty Cycle vs Temperature

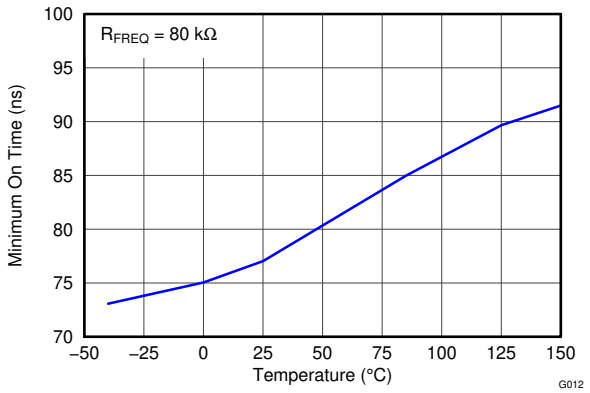


图 6-13. Minimum On-Time vs Temperature

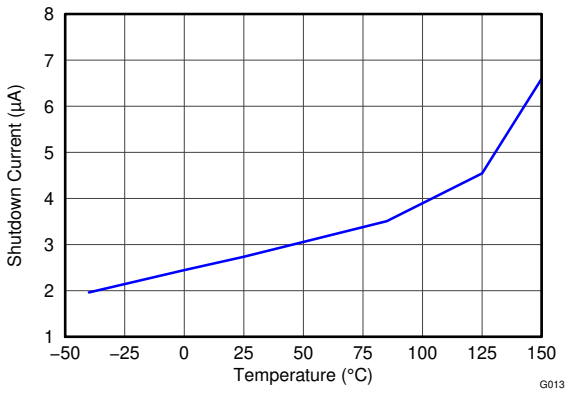


图 6-14. Shutdown Current vs Temperature

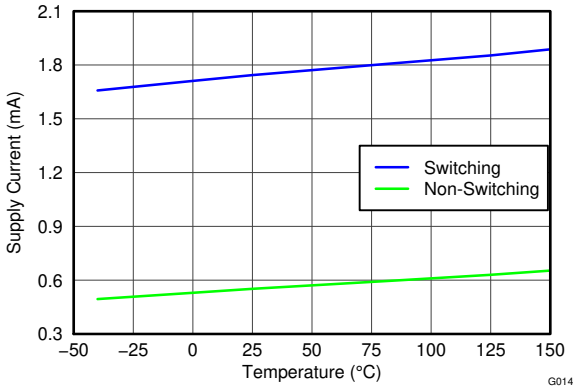


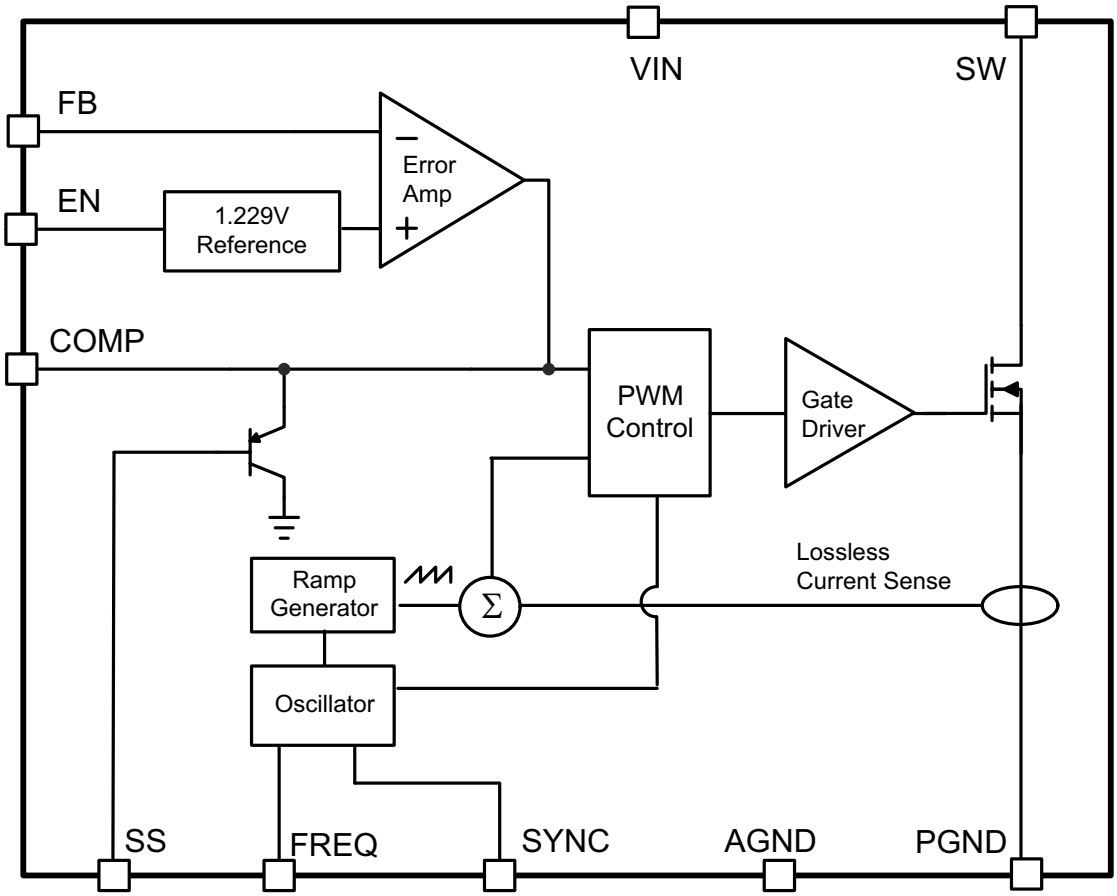
图 6-15. Supply Current vs Temperature

7 Detailed Description

7.1 Overview

The TPS55340 device is a monolithic, nonsynchronous, switching regulator with an integrated 5-A, 40-V power switch. The device can be configured in several standard switching-regulator topologies, including boost, SEPIC, and isolated flyback. The device has a wide input voltage range to support applications with input voltage from multicell batteries or regulated 3.3-V, 5-V, 12-V, and 24-V power rails.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operation

If designed as a boost converter, the TPS55340 device regulates the output with current-mode, pulse-width-modulation (PWM) control. The PWM control circuitry turns on the switch at the beginning of each oscillator clock cycle. The input voltage is applied across the inductor and stores the energy as inductor current ramps up. During this portion of the switching cycle, the load current is provided by the output capacitor. When the inductor current reaches a threshold level set by the error amplifier output, the power switch turns off and the external Schottky diode is forward biased to allow the inductor current to flow to the output. The inductor transfers stored energy to replenish the output capacitor and supply the load current. This operation repeats every switching cycle. The duty cycle of the converter is determined by the PWM control comparator which compares the error amplifier output and the current signal. The oscillator frequency is programmed by the external resistor or synchronized to an external clock signal.

A ramp signal from the oscillator is added to the inductor current ramp to provide slope compensation. Slope compensation is required to avoid subharmonic oscillation that is intrinsic to peak-current mode control at duty cycles higher than 50%. If the inductor value is too small, the internal slope compensation may not be adequate to maintain stability.

The PWM control feedback loop regulates the FB pin to a reference voltage through a transconductance error amplifier. The output of the error amplifier is connected to the COMP pin. An external RC compensation network connected to the COMP pin is chosen for feedback loop stability and optimum transient response.

7.3.2 Switching Frequency

The switching frequency is set by a resistor (R_{FREQ}) connected to the FREQ pin of the TPS55340. The relationship between the timing resistance R_{FREQ} and frequency is shown in the 图 6-5. Do not leave this pin open. A resistor must always be connected from the FREQ pin to ground for proper operation. The resistor value required for a desired frequency can be calculated using 方程式 1.

$$R_{FREQ}(k\Omega) = 57500 \times f_{sw}(kHz)^{-1.03} \quad (1)$$

For the given resistor value, the corresponding frequency can be calculated by 方程式 2.

$$f_{sw}(kHz) = 41600 \times R_{FREQ}(k\Omega)^{-0.97} \quad (2)$$

The TPS55340 switching frequency can be synchronized to an external clock signal that is applied to the SYNC pin. The required logic levels of the external clock are shown in 节 *6.3*. The recommended duty cycle of the clock is in the range of 10% to 90%. A resistor must be connected from the FREQ pin to ground when the converter is synchronized to the external clock and the external clock frequency must be within ±20% of the corresponding frequency set by the resistor. For example, if the frequency programmed by the FREQ pin resistor is 600 kHz, the external clock signal should be in the range of 480 kHz to 720 kHz.

With a switching frequency below 280 kHz (typical) after the TPS55340 enters frequency foldback as described in 节 *7.3.3*, if a load remains when the overcurrent condition is removed, then the output may not recover to the set value. For the output to return to the set value, the load must be removed completely or the TPS55340 power cycled with the EN pin or VIN pin. Select a nominal switching frequency of 350 kHz for quicker recovery from frequency foldback.

7.3.3 Overcurrent Protection and Frequency Foldback

The TPS55340 provides cycle-by-cycle overcurrent protection that turns off the power switch once the inductor current reaches the overcurrent limit threshold. The PWM circuitry resets itself at the beginning of the next switch cycle. During an overcurrent event, the output voltage begins to drop as a function of the load on the output. When the FB voltage through the feedback resistors drops lower than 0.9 V, the switching frequency is automatically reduced to 1/4 of the normal value. 图 6-8 shows the nonfoldback frequency with an 80-kΩ timing resistor and the corresponding foldback frequency. The switching frequency does not return to normal until the overcurrent condition is removed and the FB voltage increases above 0.9 V. The frequency foldback feature is disabled during soft-start.

7.3.3.1 Minimum On-Time and Pulse Skipping

The TPS55340 PWM control system has a minimum PWM pulse width of 77 ns (typical). This minimum on-time determines the minimum duty cycle of the PWM for any set switching frequency. When the voltage regulation loop of the TPS55340 requires a minimum on-time pulse width less than 77 ns, the IC enters pulse skipping mode. In this mode, the device will hold the power switch off for several switching cycles to prevent the output voltage from rising above the desired regulated voltage. This operation typically occurs in light load conditions when the PWM operates in discontinuous conduction mode. Pulse skipping increases the output ripple as shown in 图 8-7.

7.3.4 Voltage Reference and Setting Output Voltage

An internal voltage reference provides a precise 1.229-V voltage reference at the error amplifier noninverting input. To set the output voltage, select the FB pin resistor R_{SH} and R_{SL} according to 方程式 3.

$$V_{OUT} = 1.229\,V \times \left(\frac{R_{SH}}{R_{SL}} + 1 \right) \tag{3}$$

7.3.5 Soft-Start

The TPS55340 has a built-in soft-start circuit which significantly reduces the start-up current spike and output voltage overshoot. When the IC is enabled, an internal bias current source (6 µA, typical) charges a capacitor (C_{SS}) on the SS pin. The voltage at the capacitor clamps the output of the internal error amplifier that determines the peak current and duty cycle of PWM controller. Limiting the peak switch current during start-up with a slow ramp on the SS pin will reduce in-rush current and output voltage overshoot. Once the capacitor reaches 1.8 V, the soft-start cycle is completed and the soft-start voltage no longer clamps the error amplifier output. When the EN is pulled low for at least 1 ms, the IC enters the shutdown mode and the SS capacitor is discharged through a 5-kΩ resistor to prepare for the next soft-start sequence.

7.3.6 Slope Compensation

The TPS55340 has internal slope compensation to prevent subharmonic oscillations. The sensed current slope of boost converter can be expressed as 方程式 4:

$$S_n = \frac{V_{IN}}{L} \times R_{SENSE} \tag{4}$$

The slope compensation dv/dt can be calculated using 方程式 5.

$$S_e = \frac{0.32\,V / R_{FREQ}}{16 \times (1 - D) \times 6\,pF} + \frac{0.5\,\mu A}{6\,pF} \tag{5}$$

In a converter with current mode control, in addition to the output voltage feedback loop, the inner current loop including the inductor current sampling effect as well as the slope compensation on the small signal response should be taken into account, which can be modeled as seen in 方程式 6:

$$He(s) = \frac{1}{1 + \frac{s \times \left[\left(1 + \frac{S_e}{S_n} \right) \times (1 - D) - 0.5 \right]}{f_{sw}} + \frac{s^2}{\left(\pi \times f_{sw} \right)^2}} \tag{6}$$

where

- R_{SENSE} (15 mΩ) is the equivalent current sense resistor.
- R_{FREQ} is timing resistor used to set frequency.
- D is the duty cycle.

Note

If S_n << S_e, the converter operates in voltage mode control rather than current mode control, and 方程式 6 is no longer valid.

7.3.7 Enable and Thermal Shutdown

The TPS55340 enters shutdown when the EN voltage is less than 0.68 V (minimum) for more than 1 ms. In shutdown, the input supply current for the device is less than 10 µA (maximum). The EN pin has an internal 950-kΩ pulldown resistor to disable the device if the pin is floating.

An internal thermal shutdown turns off the device when the junction temperature exceeds 165°C (typical). The device will restart when the junction temperature drops by 15°C.

7.3.8 Undervoltage Lockout (UVLO)

An undervoltage lockout circuit prevents mis-operation of the device at input voltages below 2.5 V (typical). When the input voltage is below the UVLO threshold, the device remains off and the internal power MOSFET is turned off. The UVLO threshold is set below minimum operating voltage of 2.9 V to ensure that a transient V_{IN} dip will not cause the device to reset. For the input voltages between UVLO threshold and 2.9 V, the device tries to operate, but the electrical specifications are not assured.

7.4 Device Functional Modes

7.4.1 Operation With V_{IN} < 2.9 V (Minimum V_{IN})

The TPS55340 device operates with input voltages above 2.9 V. The typical UVLO voltage (turning off) is 2.5 V and the TPS55340 device remains off at input voltages lower than that point. For the input voltages between UVLO threshold and 2.9 V, the device tries to operate, but the electrical specifications are not ensured.

7.4.2 Operation With EN Control

The enable rising-edge threshold voltage is 1.08 V (typical) with 0.16 V hysteresis (typical). With the EN pin held below the turn-off voltage, the device is disabled and switching is inhibited. The IC quiescent current is reduced in this state. When the input voltage is above the UVLO threshold and the EN pin voltage increases above the rising edge threshold, the device becomes active. Switching enables and the soft-start sequence initiates. The TPS55340 device starts at the soft-start time determined by the external soft-start capacitor.

7.4.3 Operation at Light Loads

The device is designed to operate in high-efficiency, pulse-skipping mode under light load conditions. Discontinuous-conduction-mode (DCM) operation initiates when the switch current falls to 0 A. During DCM operation, the catch diode stops conducting when the switch current falls to 0 A. The switching node (the SW pin) waveform takes on the characteristics of DCM operation as shown in 图 8-6. As the load decreases further and when the voltage-regulation loop of TPS55340 device requires an on-time pulse width less than the minimum PWM pulse width of 77 ns (typical), the IC enters pulse-skipping mode. In this mode, the device holds the power switch off for several switching cycles to prevent the output voltage from rising too much above the desired regulated voltage.

8 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The TPS55340 device can be configured in several standard switching-regulator topologies, including boost, SEPIC, and isolated flyback. For example, the device configured in boost topology is widely used to convert a lower dc voltage to a higher dc voltage with a maximum available switching current of 5.25 A. Use the following design procedure to select component values for a boost converter design or SEPIC design for the TPS55340 device. Alternately, use the WEBENCH® software to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Applications

The following section provides a step-by-step design approach for configuring the TPS55340 as a voltage regulating boost converter, as shown in 图 8-1. When configured as SEPIC or flyback converter, a different design approach is required. A design example of SEPIC converter is provided in the next section.

8.2.1 Boost Converter

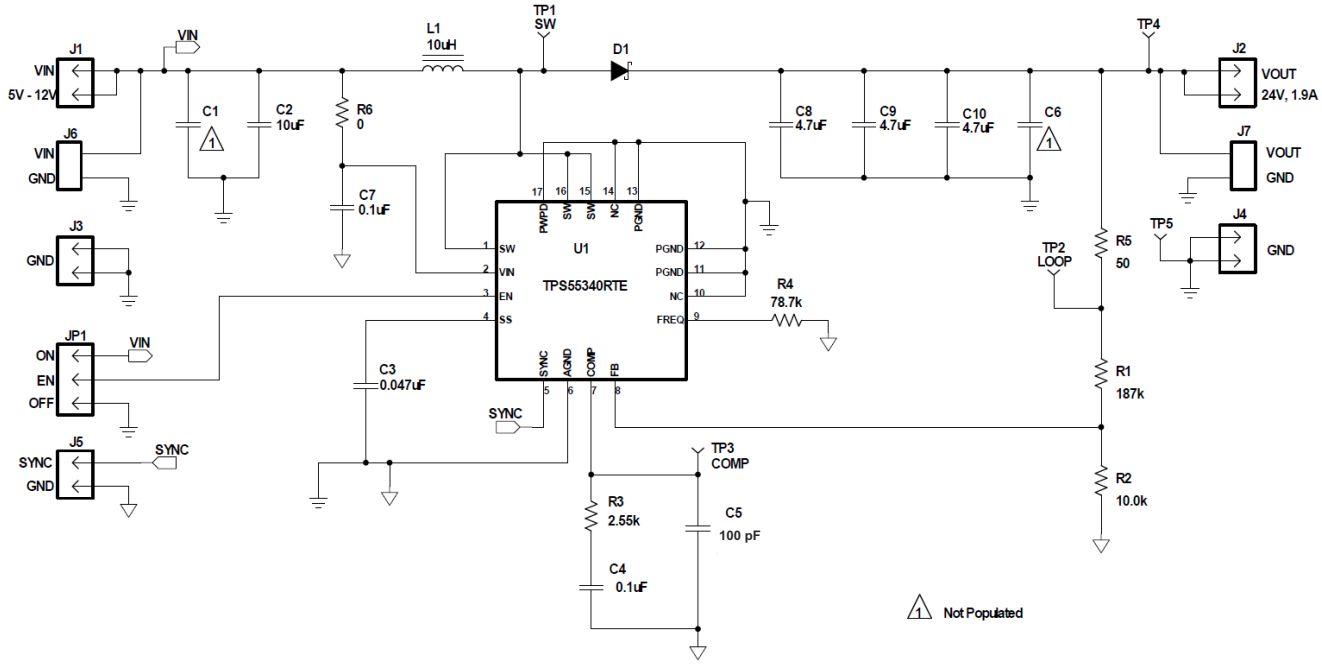


图 8-1. Boost Converter Application Schematic

8.2.1.1 Design Requirements

For this design example, use the parameters listed in 表 8-1. These parameters are typically determined at the system level.

表 8-1. Design Parameters

PARAMETER	VALUE
Output voltage	24 V
Input voltage	5 V to 12 V
Maximum output current	800 mA
Transient response 50% load step (ΔV_{OUT} = 3%)	960 mV
Output voltage ripple (0.5% of V_{OUT})	120 mV

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the TPS55340 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

8.2.1.2.2 Selecting the Switching Frequency (R4)

The first step is to decide on a switching frequency for the regulator. There are tradeoffs to consider for a higher or lower switching frequency. A higher switching frequency allows for lower valued inductor and smaller output capacitors leading to the smallest solution size. A lower switching frequency will result in a larger solution size but better efficiency. The user will typically set the frequency for the minimum tolerable efficiency to avoid excessively large external components.

A switching frequency of 600 kHz is a good trade-off between efficiency and solution size. The appropriate resistor value is found from the resistance versus frequency graph of 图 6-5, or calculated using 方程式 1. R4 is calculated to be 78.4 kΩ and the nearest standard value resistor of 78.7 kΩ is selected. A resistor must be placed from the FREQ pin to ground, even if an external oscillation is applied for synchronization.

8.2.1.2.3 Determining the Duty Cycle

The input-to-output voltage conversion ratio of the TPS55340 is limited by the worst case maximum duty cycle of 89% and the minimum duty cycle which is determined by the minimum on-time of 77 ns and the switching frequency. The minimum duty cycle can be estimated with 方程式 7. With a 600-kHz switching frequency the minimum duty cycle is 4%.

$$D_{PS} = T_{ON}\ \text{min} \times f_{sw} \tag{7}$$

The duty cycle at which the converter operates is dependent on the mode in which the converter is running. If the converter is running in DCM, where the inductor current ramps to zero at the end of each cycle, the duty cycle varies with changes of the load much more than it does when running in continuous conduction mode (CCM). In CCM, where the inductor maintains a minimum dc current, the duty cycle is related primarily to the input and output voltages as computed below. Assume a 0.5-V drop V_D across the Schottky rectifier. At the minimum input of 5 V, the duty cycle will be 80%. At the maximum input of 12 V, the duty cycle is 51%.

$$D = \frac{V_{OUT} + V_D - V_{IN}}{V_{OUT} + V_D} \quad (8)$$

At light loads the converter will operate in DCM. In this case the duty cycle is a function of the load, input and output voltages, inductance, and switching frequency as computed below. This can be calculated only after an inductance is chosen in the following section. While operating in DCM with very light load conditions, the duty cycle demand will force the TPS55340 to operate with the minimum on-time. The converter will then begin pulse skipping which can increase the output ripple.

$$D = \frac{\sqrt{2 \times (V_{OUT} + V_D - V_{IN}) \times L \times I_{OUT} \times f_{SW}}}{V_{IN}} \quad (9)$$

All converters using a diode as the freewheeling or catch component have a load current level at which they transit from DCM to CCM. At this point the inductor current just falls to zero during the off-time of the power switch. At higher load currents, the inductor current does not fall to zero and diode and switch current assume a trapezoidal wave shape as opposed to a triangular wave shape. The load current boundary between discontinuous conduction and continuous conduction can be found for a set of converter parameters as follows:

$$I_{OUT(crit)} = \frac{(V_{OUT} + V_D - V_{IN}) \times V_{IN}^2}{2 \times (V_{OUT} + V_D)^2 \times f_{SW} \times L} \quad (10)$$

For loads higher than the result of 方程式 10, the duty cycle is given by 方程式 8. For loads less than the results of 方程式 10, the duty cycle is given by 方程式 9. For 方程式 7 through 方程式 10, the variable definitions are as follows:

- V_{OUT} is the output voltage of the converter in V.
- V_D is the forward conduction voltage drop across the rectifier or catch diode in V.
- V_{IN} is the input voltage to the converter in V.
- I_{OUT} is the output current of the converter in A.
- L is the inductor value in H.
- f_{SW} is the switching frequency in Hz.

Unless otherwise stated, the design equations that follow assume that the converter is running in CCM which typically results in a higher efficiency for the power levels of this converter.

8.2.1.2.4 Selecting the Inductor (L1)

The selection of the inductor affects steady-state operation as well as transient behavior and loop stability. These factors make it the most important component in power regulator design. There are three important inductor specifications: inductor value, dc resistance and saturation current. Considering inductor value alone is not enough. Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, the effective inductance can fall to a fraction of the zero current value.

The minimum value of the inductor should be able to meet the inductor current ripple (ΔI_L) requirement at worst case. In a boost converter, maximum inductor current ripple occurs at 50% duty cycle. For the applications where duty cycle is always smaller or larger than 50%, 方程式 12 should be used with the duty cycle closest to 50% and corresponding input voltage to calculate the minimum inductance. For applications that must operate with 50% duty cycle when input voltage is somewhere between the minimum and the maximum input voltage, 方程式 13 should be used. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum input current ($I_{IN}DC = I_L avg$). The maximum input current can be estimated with 方程式 11, with an estimated efficiency based on similar applications (η_{EST}). The inductor ripple current will be filtered by the output capacitor. Therefore, choosing high inductor ripple currents will impact the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor

ripple current. In general, the inductor ripple value (K_{IND}) is at the discretion of the designer. However, the following guidelines may be used.

For CCM operation, it is recommended to use K_{IND} values in the range of 0.2 to 0.4. Choosing K_{IND} closer to 0.2 results in a larger inductance value, maximizes the potential output current of the converter and minimizes EMI. Choosing K_{IND} closer to 0.4 results in a smaller inductance value, a physically smaller inductor, and improved transient response, but potentially worse EMI and lower efficiency. Using an inductor with a smaller inductance value may result in the converter operating in DCM. This reduces the maximum output current of the boost converter, causes larger input voltage and output voltage ripple, and reduced efficiency. For this design, choose K_{IND} = 0.3 and a conservative efficiency estimate of 85% with the minimum input voltage and maximum output current. 方程式 12 is used with the maximum input voltage because this corresponds to duty cycle closest to 50%. The maximum input current is estimated at 4.52 A and the minimum inductance is 7.53 µH. A standard value of 10 µH is chosen.

$$I_{IN}DC = \frac{V_{OUT} \times I_{OUT}}{\eta_{EST} \times V_{IN}\,min} \tag{11}$$

$$L_O\,min \geq \frac{V_{IN}}{I_{IN}DC \times K_{IND}} \times \frac{D}{f_{SW}} \quad , D \neq 50\%, V_{IN} \text{ with D closest to 50\%} \tag{12}$$

$$L_O\,min \geq \frac{(V_{OUT} + V_D)}{I_{IN}DC \times K_{IND}} \times \frac{1}{4 \times f_{SW}} \quad , D=50\% \tag{13}$$

After choosing the inductance, the required current ratings can be calculated. The inductor will be closest to its ratings with the minimum input voltage. The ripple with the chosen inductance is calculated with 方程式 14. The RMS and peak inductor current can be found with 方程式 15 and 方程式 16. For this design the current ripple is 663 mA, the RMS inductor current is 4.52 A, and the peak inductor current is 4.85 A. It is generally recommended for the peak inductor current rating of the selected inductor be 20% higher to account for transients during powerup, faults, or transient load conditions. The most conservative approach is to specify an inductor with a saturation current greater than the maximum peak current limit of the TPS55340. This helps to avoid saturation of the inductor. The chosen inductor is a Würth Elektronik 74437368100. It has a saturation current rating of 12.5 A, RMS current rating of 5.2 A, and typical DCR of 27.0 mΩ.

$$\Delta I_L = \frac{V_{IN}\,min}{L_O} \times \frac{D\,max}{f_{SW}} \tag{14}$$

$$I_L rms = \sqrt{(I_{IN}DC)^2 + \left(\frac{\Delta I_L}{12}\right)^2} \tag{15}$$

$$I_L peak = I_{IN}DC + \frac{\Delta I_L}{2} \tag{16}$$

The TPS55340 has built-in slope compensation to avoid subharmonic oscillation associated with current mode control. If the inductor value is too small, the slope compensation may not be adequate, and the loop can be unstable.

8.2.1.2.5 Computing the Maximum Output Current

The overcurrent limit for the integrated power MOSFET limits the maximum input current and thus the maximum input power for a given input voltage. Maximum output power is less than maximum input power due to power conversion losses. Therefore, the current limit setting, input voltage, output voltage, and efficiency can all change maximum current output (I_{OUT}max). The current limit clamps the peak inductor current; therefore, the ripple has to be subtracted to derive maximum dc current. Decreasing the K_{IND} or designing for a higher efficiency will increase the maximum output current. This can be evaluated with the chosen inductance or the

chosen K_{IND}. This should be evaluated with the minimum input voltage and minimum peak current limit (I_{LIM}) of 5.25 A.

$$I_{OUT}\,max = \frac{V_{IN}\,min \times \left(I_{LIM} - \frac{\Delta I_L}{2}\right) \times \eta_{EST}}{V_{OUT}} = \frac{V_{IN}\,min \times I_{LIM} \times \left(1 - \frac{K_{IND}}{2}\right) \times \eta_{EST}}{V_{OUT}} \quad (17)$$

In this design with a 5-V input boosted to a 24-V output and a 10- μ H inductor with an assumed Schottky forward voltage of 0.5 V and estimated efficiency of 85%, the maximum output current is 871 mA. With the 12-V input and increased estimated efficiency of 90%, the maximum output current increases to 2.13 A. This circuit was evaluated to its maximum output currents with both the minimum and maximum input voltage.

8.2.1.2.6 Selecting the Output Capacitors (C8, C9, C10)

At least 4.7 μF of ceramic-type X5R or X7R capacitance is recommended at the output. The output capacitance is mainly selected to meet the requirements for the output ripple (V_{RIPPLE}) and voltage change during a load transient. Then the loop is compensated for the output capacitor selected. The output capacitance should be chosen based on the most stringent of these criteria. The output ripple voltage is related to the capacitance and equivalent series resistance (ESR) of the output capacitor. Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by 方程式 18. If high ESR capacitors are used, it will contribute additional ripple. The maximum ESR for a specified ripple is calculated with 方程式 19. ESR ripple can be neglected for ceramic capacitors but must be considered if tantalum or electrolytic capacitors are used. The minimum ceramic output capacitance needed to meet a load transient requirement can be estimated by the 方程式 20. 方程式 21 can be used to calculate the RMS current that the output capacitor needs to support.

$$C_{OUT} \geq \frac{D\max \times I_{OUT}}{f_{SW} \times V_{RIPPLE}} \quad (18)$$

$$ESR \leq \frac{\left(V_{RIPPLE} - \frac{D\max \times I_{OUT}}{f_{SW} \times C_{OUT}}\right)}{\Delta I_L} \quad (19)$$

$$C_{OUT} \geq \frac{\Delta I_{TRAN}}{2 \times \pi \times f_{BW} \times \Delta V_{TRAN}} \quad (20)$$

$$I_{CO}rms = I_{OUT}\sqrt{\frac{D\max}{(1 - D\max)}} \quad (21)$$

Using 方程式 18 for this design, the minimum output capacitance for the specified 120-mV output ripple is 8.8 μF. For a maximum transient voltage change (ΔV_{TRAN}) of 960 mV with a 400-mA load transient (ΔI_{TRAN}) and a 6-kHz control loop bandwidth (f_{BW}) with 方程式 20, the minimum output capacitance is 11.1 μF. The most stringent criteria is the 11.1 μF for the required load transient. 方程式 21 gives a 1.58-A RMS current in the output capacitor. The capacitor should also be properly rated for the desired output voltage.

Care must be taken when evaluating ceramic capacitors that derate under dc bias, aging, and ac signal conditions. For example, larger form factor capacitors (in 1206 size) have self-resonant frequencies in the range of converter switching frequency. Self-resonance causes the effective capacitance to be significantly lower. The dc bias can also significantly reduce capacitance. Ceramic capacitors can lose as much as 50% of the capacitance when operated at the rated voltage. Therefore, allow a margin in selected capacitor voltage rating to ensure adequate capacitance at the required output voltage. For this example, three 4.7-μF, 50-V, 1210 X7R ceramic capacitors are used in parallel leading to a negligible ESR. Choosing 50-V capacitors instead of 35-V reduces the effects of dc bias and allows this example circuit to be rated for the maximum output voltage range of the TPS55340.

8.2.1.2.7 Selecting the Input Capacitors (C2, C7)

At least 4.7 µF of ceramic input capacitance is recommended. Additional input capacitance may be required to meet ripple and/or transient requirements. High-quality ceramic, type X5R or X7R are recommended to minimize capacitance variations over temperature. The capacitor must also have an RMS current rating greater than the maximum RMS input current of the TPS55340 calculated with 方程式 22. The input capacitor must also be rated greater than the maximum input voltage. The input voltage ripple can be calculated with 方程式 23.

$$I_{CI}rms = \frac{\Delta I_L}{\sqrt{12}} \tag{22}$$

$$V_I ripple = \frac{\Delta I_L}{4 \times f_{SW} \times C_{IN}} + \Delta I_L \times R_{CIN} \tag{23}$$

In the design example, the input RMS current is calculated to be 191 mA. The chosen input capacitor is a 10-µF, 35-V, 1210 X7R with 3-mΩ ESR. Although one with a lower voltage rating can be used, a 35-V rated capacitor was chosen to limit the affects of dc bias and to allow the circuit to be rated for the entire input range of the TPS55340. The input ripple is calculated to be 30 mV. An additional 0.1-µF, 50-V, 0603 X5R is located close to the VIN and GND pins for extra decoupling.

8.2.1.2.8 Setting Output Voltage (R1, R2)

To set the output voltage in either DCM or CCM, select the values of R1 and R2 according to the following equations:

$$V_{OUT} = 1.229\,V \times \left(\frac{R1}{R2} + 1\right) \tag{24}$$

$$R1 = R2 \times \left(\frac{V_{OUT}}{1.229\,V} - 1\right) \tag{25}$$

Considering the leakage current through the resistor divider and noise decoupling into the FB pin, an optimum value for R2 is around 10 kΩ. The output voltage tolerance depends on the V_{FB} accuracy and the tolerance of R1 and R2. In this example with a 24-V output using 方程式 25, R1 is calculated to 185.3 kΩ. The nearest standard value of 187 kΩ is used.

8.2.1.2.9 Setting the Soft-start Time (C7)

Choose the appropriate capacitor to set soft-start time and avoid overshoot. Increasing the soft-start time reduces the overshoot during startup. A 0.047-µF ceramic capacitor is used in this example.

8.2.1.2.10 Selecting the Schottky Diode (D1)

The high switching frequency of the TPS55340 demands high-speed rectification for optimum efficiency. Ensure that the average and peak current ratings of the diode exceed the average output current and peak inductor current. In addition, the reverse breakdown voltage of the diode must exceed the regulated output voltage. The diode must also be rated for the power dissipated which can be calculated with 方程式 26.

$$P_D = V_D \times I_{OUT} \tag{26}$$

In this conservative design example, the diode is chosen to be rated for the maximum output current of 2.13 A. During normal operation with 800-mA output current and assuming a Schottky diode drop of 0.5 V, the diode must be capable of dissipating 400 mW. The recommended minimum ratings for this design are a 40-V, 3-A diode. However, to improve the flexibility of this design, a Diodes Inc B540-13-F in an SMC package is used with voltage and current ratings of 40 V and 5 A.

8.2.1.2.11 Compensating the Control Loop (R3, C4, C5)

The TPS55340 requires external compensation which allows the loop response to be optimized for each application. The COMP pin is the output of the internal error amplifier. An external resistor R3 and ceramic capacitor C4 are connected to the COMP pin to provide a pole and a zero, shown in 图 8-1. This pole and zero, along with the inherent pole and zero of a boost converter, determine the closed-loop frequency response. This is important for converter stability and transient response. Loop compensation should be designed for the minimum operating voltage.

The following equations summarize the loop equations for the TPS55340 configured as a CCM boost converter. They include the power stage output pole (f_{OUT}) and the right-half-plane zero (f_{RHPZ}) of a boost converter calculated with 方程式 27 and 方程式 28, respectively. When calculating f_{OUT}, it is important to include the derating of ceramic output capacitors. In the example with an estimated 10.2-µF capacitance, these frequencies are calculated to be 980 kHz and 22.1 kHz, respectively. The dc gain (A) of the power stage is calculated with 方程式 29 and is 39.9 dB in this design. The compensation pole (f_P) and zero (f_Z) generated by R3, C4, and internal transconductance amplifier are calculated with 方程式 30 and 方程式 31, respectively.

Most CCM boost converters will have a stable control loop if f_Z is set slightly above f_P through proper sizing of R3 and C4. A good starting point is C4 = 0.1 µF and R3 = 2 kΩ. Increasing R3 or reducing C4 increases the closed-loop bandwidth, and therefore improves the transient response. Adjusting R3 and C4 in the opposite direction increases the phase and gain margin of the loop, which improves loop stability. It is generally recommended to limit the bandwidth of the loop to the lower of either 1/5 of the switching frequency f_{SW} or 1/3 the RHPZ frequency, f_{RHPZ} shown in 方程式 28. The spreadsheet tool located in the TPS55340 product folder at www.ti.com can also be used to aid in compensation design.

$$f_{OUT} \approx \frac{2}{2\pi \times R_{OUT} \times C_{OUT}} \tag{27}$$

$$f_{RHPZ} \approx \frac{R_{OUT}}{2\pi \times L} \times \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \tag{28}$$

$$A = \frac{1.229}{V_{OUT}} \times G_{ea} \times 10M\Omega \times \frac{V_{IN}}{V_{OUT} \times R_{SENSE}} \times R_{OUT} \times \frac{1}{2} \tag{29}$$

$$f_P = \frac{1}{2\pi \times 10M\Omega \times C4} \tag{30}$$

$$f_Z = \frac{1}{2\pi \times R3 \times C4} \tag{31}$$

$$f_{co1} = \frac{f_{SW}}{5} \tag{32}$$

$$f_{co2} = \frac{f_{RHPZ}}{3} \tag{33}$$

where

- C_{OUT} is the equivalent output capacitor (C_{OUT}= C8 + C9 + C10)
- R_{OUT} is the equivalent load resistance (V_{OUT}/I_{OUT})
- G_{ea} is the error amplifier transconductance located in 节 6.5
- R_{SENSE} (15 mΩ, typical) is the sense resistor in the current control loop
- f_{co1} and f_{co2} are possible bandwidths.

An additional capacitor from the COMP pin to GND (C5) can be used to place a high-frequency pole in the control loop. This is not always necessary with ceramic output capacitors. If a nonceramic output capacitor is used, there is an additional zero (f_{ZESR}) in the control loop which can be calculated with 方程式 35. The value of C5 and the pole created by C5 can be calculated with 方程式 36 and 方程式 34, respectively. Finally, if more phase margin is needed, an additional zero (f_{ZFF}) can be added by placing a capacitor (C_{FF}) in parallel with the top feedback resistor R1. It is recommended to place the zero at the target cross-over frequency or higher. The feed-forward capacitor also adds a pole at a higher frequency. The recommended value of C_{FF} can be calculated with 方程式 37.

$$f_{P2} = \frac{1}{2\pi \times R3 \times C5} \tag{34}$$

$$f_{ZESR} \approx \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \tag{35}$$

$$C5 = \frac{R_{ESR} \times C_{OUT}}{R3} \tag{36}$$

$$C_{FF} = \frac{1}{2\pi \times R1 \times f_{ZFF} \times \sqrt{\frac{V_{REF}}{V_{OUT}}}} \tag{37}$$

where

- R_{ESR} is the ESR of the output capacitor

If a network measurement tool is available, the most accurate compensation design can be achieved following this procedure. The power stage frequency response is first measured using a network analyzer at the minimum 5-V input and maximum 800-mA load. This measurement is shown in 图 8-2. In this design only one pole and one zero are used, so the maximum phase increase from the compensation will be 180 degrees. For a 60-degree phase margin, the power stage phase must be – 120 degrees at its lowest point. Based on the target 6-kHz bandwidth, the measured power stage gain, $K_{PS}(f_{BW})$, is 24.84 dB and the phase is – 110.3 degrees.

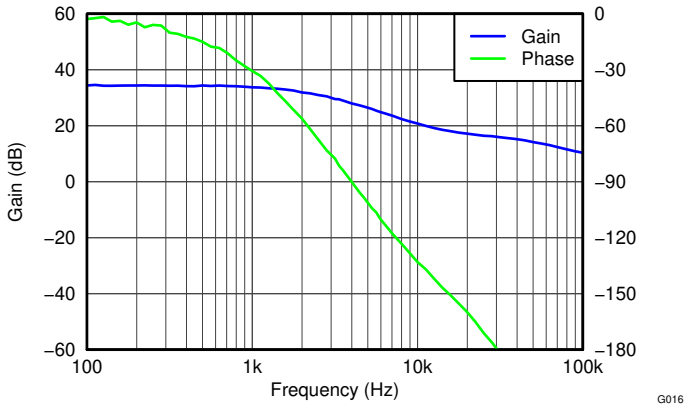


图 8-2. Power Stage Gain and Phase of the Boost Converter

R3 is then chosen to set the compensation gain to be the reciprocal of the power stage gain at the target bandwidth using 方程式 38. C4 is then chosen to place a zero at 1/10 the target bandwidth with 方程式 39. In this case, R3 is calculated to be 2.56 kΩ and the nearest standard value of 2.55 kΩ is used. C4 is calculated at 0.104 µF and the nearest standard value of 0.100 µF is used. Although not necessary because this design uses all ceramic capacitors, a 100-pF capacitor is selected for C5 to add a high-frequency pole at a frequency 100 times the target bandwidth.

$$R3 = \frac{1}{\left(Gea \times \frac{R2}{(R1 + R2)} \times 10^{\frac{K_{PS}(f_{BW})}{20}} \right)} \quad (38)$$

$$C4 = \frac{1}{2\pi \times R3 \times \frac{f_{BW}}{10}} \quad (39)$$

8.2.1.3 Application Curves

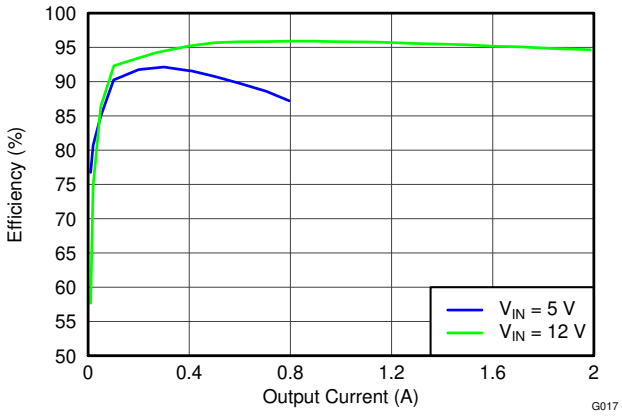


图 8-3. Efficiency vs Output Current

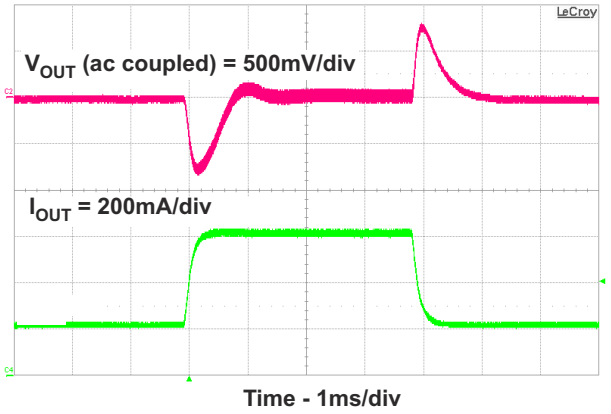


图 8-4. Load Transient Response

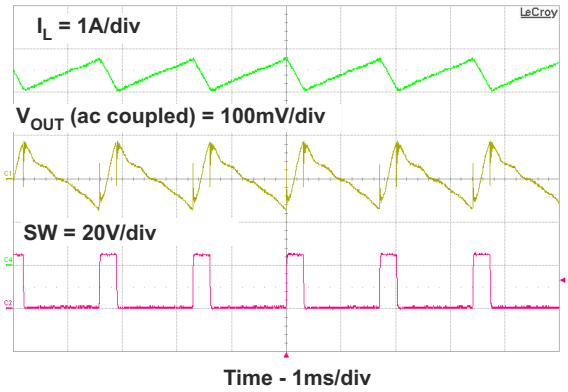


图 8-5. CCM PWM Operation

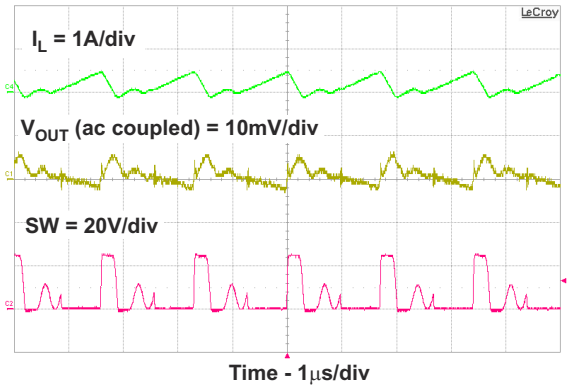


图 8-6. DCM PWM Operation

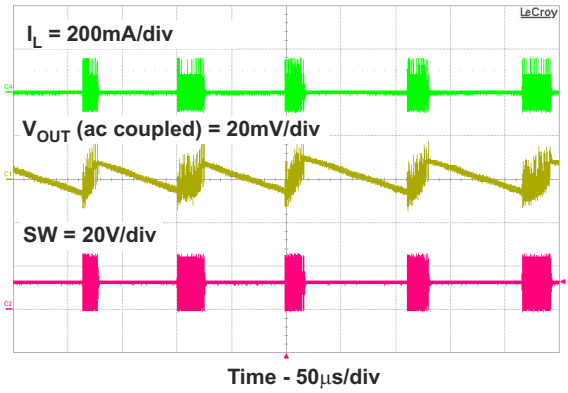


图 8-7. Pulse Skipping

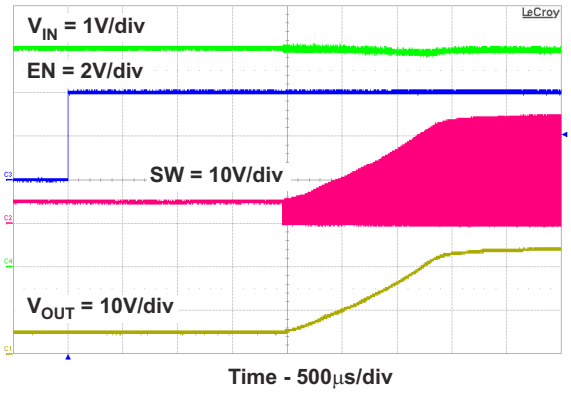


图 8-8. Start-Up

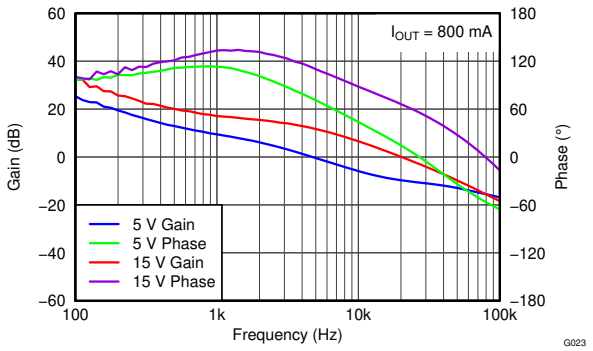


图 8-9. Closed-Loop Gain and Phase of the Boost Converter

8.2.2 SEPIC Converter

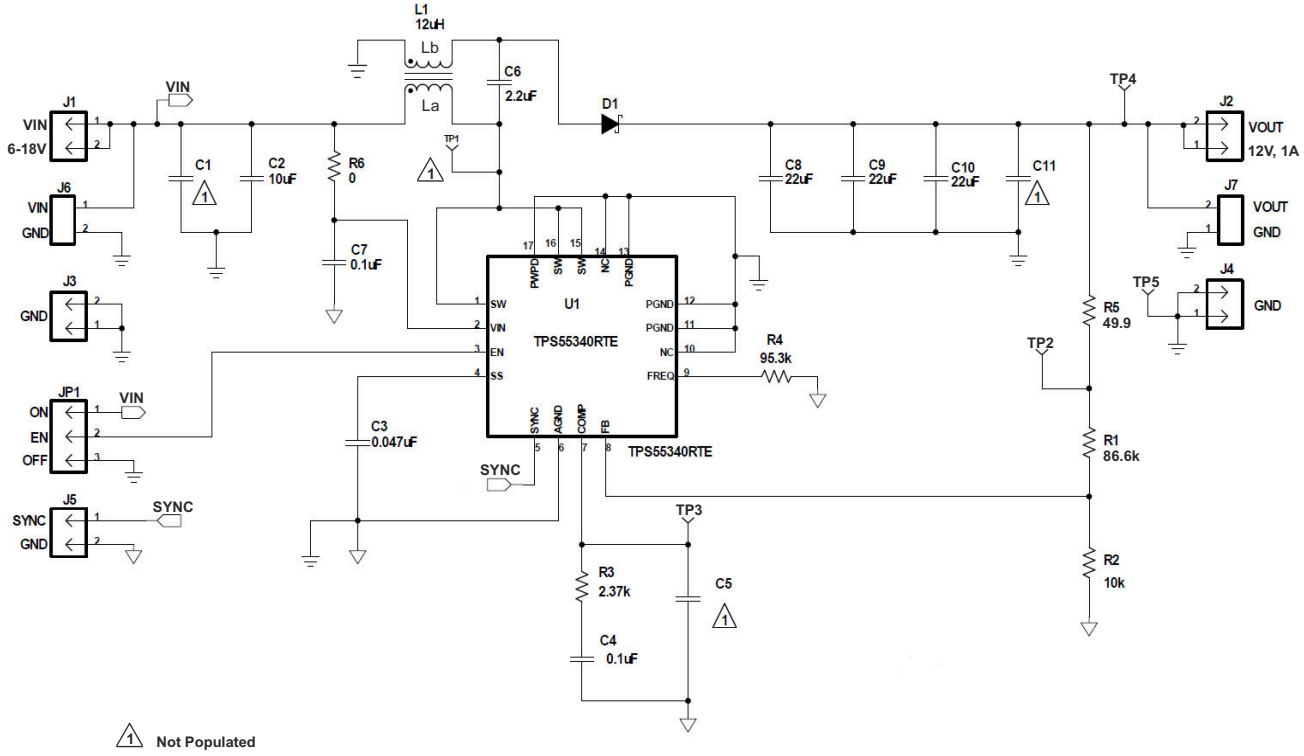


图 8-10. SEPIC Converter Application Schematic

8.2.2.1 Design Requirements

The parameters listed in 表 8-2 are used for a SEPIC converter design. These calculations are performed only for CCM operation. The use of a coupled inductor is assumed.

表 8-2. Design Parameters

PARAMETER	VALUE
Output voltage	12 V
Input voltage	6 V to 18 V, 12 V nominal
Maximum output current	1 A
Transient response 50% load step (ΔV_{OUT} = 4%)	480 mV
Output voltage ripple (0.5% of V_{OUT})	60 mV

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Selecting the Switching Frequency (R4)

A 500-kHz switching frequency (f_{SW}) is selected for this design. Using 方程式 1, R4 is calculated and the nearest standard value of 95.3 kΩ is used.

8.2.2.2.2 Duty Cycle

The duty cycle of a SEPIC converter is calculated with 方程式 40. With the 6-V minimum input voltage, the duty cycle is 68%; and with the 18-V maximum input voltage, the duty cycle is 41%.

$$D = \frac{V_{OUT} + V_D}{V_{OUT} + V_D + V_{IN}} \tag{40}$$

8.2.2.2.3 Selecting the Inductor (L1)

With an estimated 85% efficiency, the input current is calculated with 方程式 9 to be 2.35 A. With K_{IND} of 0.3 and the maximum 18-V input voltage, the minimum inductance is calculated to be 10.5 µH using 方程式 41. The nearest standard value of 12 µH is used. As mentioned previously, this equation assumes a coupled inductor is used.

$$L \geq \frac{V_{IN}\,max \times D\,min}{2 \times f_{SW} \times I_{IN}DC \times K_{IND}} \tag{41}$$

The inductor ripple current is recalculated to be 615 mA with 方程式 42. The peak current is calculated to be 3.69 A. The typical current limit is used as the saturation rating for the inductor used. The RMS current for La is approximately the average input current of 2.35 A. The RMS current for Lb is approximately the output current of 1 A. For this design, a CoilCraft MSD1260-123 is used with 6.86-A saturation, 74-mΩ DCR, and 3.12-A RMS current rating for one winding.

$$\Delta I_L = \frac{V_{IN}\,max \times D\,min}{2 \times f_{SW} \times L} \tag{42}$$

$$I_L peak = I_{La} peak + I_{Lb} peak = \left(I_{IN}DC + \frac{\Delta I_L}{2}\right) + \left(I_{OUT} + \frac{\Delta I_L}{2}\right) \tag{43}$$

8.2.2.2.4 Calculating the Maximum Output Current

The maximum output current with the minimum input voltage 6 V, chosen inductance 12 µH, 5.25-A minimum current limit, and estimated 85% efficiency is calculated to be 1.47 A using 方程式 44.

$$I_{OUT}\,max = \frac{\left(I_{LIM} - \Delta I_L\right)}{\left(\frac{V_{OUT}}{V_{IN}\,min \times \eta_{EST}} + 1\right)} = \frac{\left(I_{LIM} - I_{IN}DC \times K_{IND}\right)}{\left(\frac{V_{OUT}}{V_{IN}\,min \times \eta_{EST}} + 1\right)} \tag{44}$$

8.2.2.2.5 Selecting the Output Capacitors (C8, C9, C10)

To meet the 60-mV ripple specification, the minimum output capacitance is calculated to be 22.5 µF with 方程式 45. This design uses ceramic output capacitors and the effects of ESR are ignored. To meet the transient response of 500 mA with less than 480-mV voltage change and a 7-kHz control loop bandwidth, the minimum output capacitance is calculated to be 23.7 µF using 方程式 46. The RMS current is calculated with 方程式 22 to be 1.44 A. The output capacitors used in this design are 3 × 22 µF, 25 V, X7R 1210 ceramic capacitors. With voltage derating, the effective total output capacitance is estimated to be 30.4 µF.

$$C_{OUT} \geq \frac{Dmax \times I_{OUT}}{f_{SW} \times V_{RIPPLE}} \quad (45)$$

$$C_{OUT} \geq \frac{\Delta I_{TRAN}}{2\pi \times f_{BW} \times \Delta V_{TRAN}} \quad (46)$$

8.2.2.2.6 Selecting the Series Capacitor (C6)

The series capacitor is chosen to limit the ripple current to 5% of the maximum input voltage. Using 方程式 47 the minimum capacitance is 1.5 µF. Using 方程式 48 the RMS current is calculated to be 1.63 A. A 2.2-µF ceramic capacitor in a 1206 package is selected.

$$C_P \geq \frac{I_{OUT} \times Dmax}{0.05 \times V_{IN}max \times f_{SW}} \quad (47)$$

$$I_{CP}rms = I_{IN}DC \times \sqrt{\frac{(1-Dmax)}{Dmax}} \quad (48)$$

8.2.2.2.7 Selecting the Input Capacitor (C2, C7)

Based on the minimum 4.7-µF ceramic recommended for the TPS55340, a 10-µF X7R input capacitor is used with an additional 0.1 µF placed close to the VIN and GND pins. With an estimated 6-µF capacitance after voltage derating, the input ripple voltage is calculated to be 39.9 mV using 方程式 49. The RMS current of the input capacitance is calculated to be 0.177 A with 方程式 50.

$$V_{I}ripple = \frac{\Delta I_L}{4 \times f_{SW} \times C_{IN}} \quad (49)$$

$$I_{CI}rms = \frac{\Delta I_L}{\sqrt{12}} \quad (50)$$

8.2.2.2.8 Selecting the Schottky Diode (D1)

The selected diode must have a minimum breakdown voltage (V_{BR}) calculated with 方程式 51 which is 30.5 V in this design. The average current rating is recommended to be greater than the maximum output current. With the maximum 18-V input, average current is calculated to be 2.6 A using 方程式 17. The package must also be capable of handling the power dissipation. With an estimated 0.5-V forward voltage, power dissipation is calculated with 方程式 26 to be 500 mW. Diodes Inc B340B is chosen with a 40-V, 3-A rating in an SMB package.

$$V_{BR} = V_O + V_{IN}max + V_F \quad (51)$$

8.2.2.2.9 Setting the Output Voltage (R1, R2)

With R2 fixed at 10 kΩ using 方程式 25 the nearest standard value of 86.6 kΩ is chosen for R1.

8.2.2.2.10 Setting the Soft-start Time (C3)

The recommended 0.047-µF soft-start capacitor is used.

8.2.2.2.11 MOSFET Rating Considerations

In a SEPIC converter the MOSFET must be rated to handle the sum of the input and output voltages. In this design with the maximum input voltage of 18 V and output voltage of 12 V, the FET will see approximately 30 V. A 10% tolerance is recommended to account for any ringing. The 40-V rating of the TPS55340 power MOSFET comfortably satisfies this requirement.

8.2.2.2.12 Compensating the Control Loop (R3, C4)

This design was compensated by measuring the frequency response of the power stage at the lowest input voltage of 6 V and choosing the components for the desired bandwidth. The lowest right half plane zero (f_{RHPZ}) is calculated to be 36.7 kHz with 方程式 52. Using the recommendation to limit the bandwidth to 1/3 of f_{RHPZ}, the maximum recommended is 12.2 kHz.

$$f_{RHPZ} = \frac{\frac{V_{OUT}}{I_{OUT}}}{2 \times \pi \times L \times \left(\frac{D}{(1-D)}\right)^2} \quad (52)$$

This design also uses only one pole and one zero. To achieve approximately 60 degrees of phase margin, the power stage phase must be no lower than approximately –120 degrees at the desired bandwidth. To ensure a stable design, R3 was initially set to 1 kΩ and C4 was 1 µF. 图 8-11 shows the measurement of the power stage. At 7 kHz the power stage has a gain of 19.52 dB and phase of –118.1 degrees.

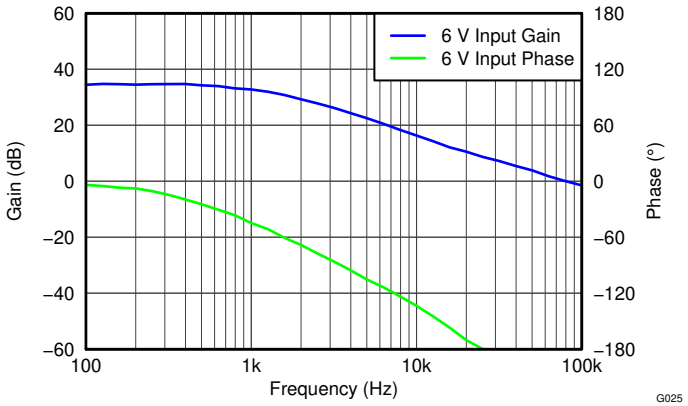


图 8-11. SEPIC Power Stage Gain and Phase

As there are no changes in the transconductance amplifier, the equations used to calculate the external compensation components in a boost design can be used in the SEPIC design. Using the maximum G_{ea} from the electrical specification of 440 µmho, 方程式 38 calculates the nearest standard value of R3 to be 2.37 kΩ. Using 方程式 39, C4 is calculated to the nearest standard value of 0.1 µF.

8.2.2.3 Application Curves

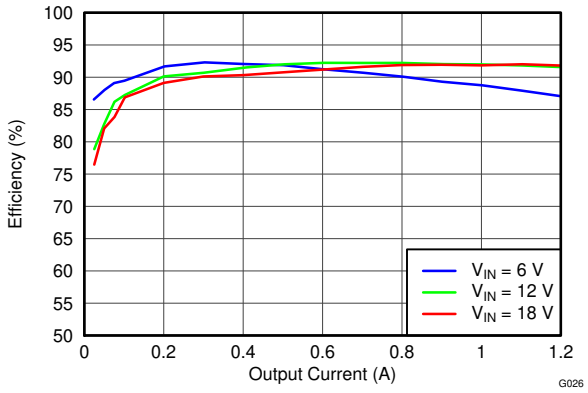


图 8-12. Efficiency vs Output Current

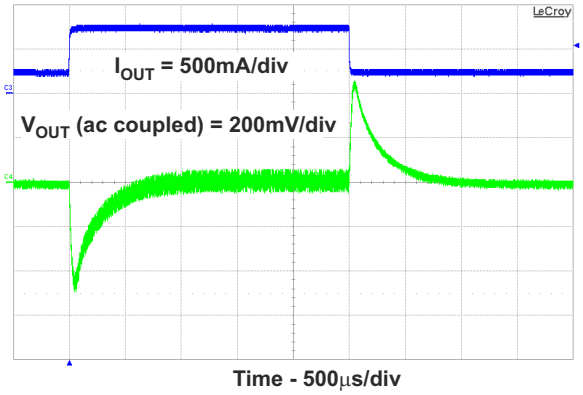


图 8-13. Load Transient Response

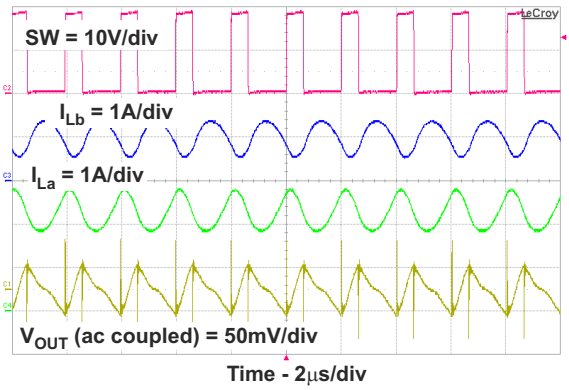


图 8-14. CCM PWM Operation

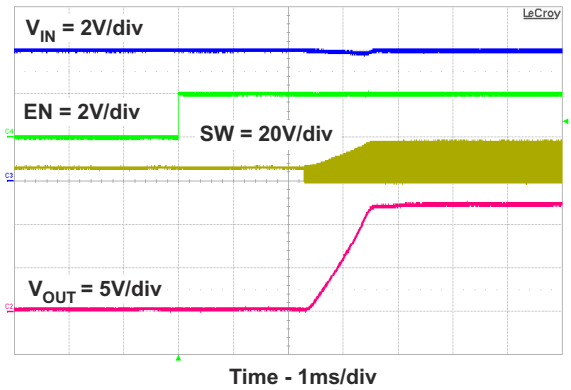


图 8-15. Output Voltage Soft-start

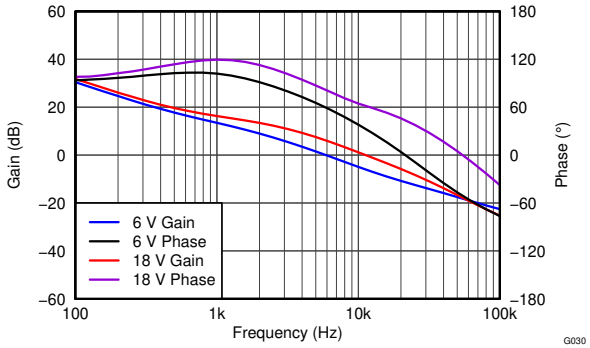


图 8-16. Closed-Loop Gain and Phase of the SEPIC Converter

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.9 V and 32 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS55340 converter additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 μF is a typical choice.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, especially those with high frequency and high switch current, printed-circuit board (PCB) layout is an important design step. If the layout is not carefully designed, the regulator can suffer from instability as well as noise problems. The following guidelines are recommended for good PCB layout.

- To prevent radiation of high-frequency resonance problems, use proper layout of the high-frequency switching path.
- Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize inter-plane coupling.
- The high current path, including the internal MOSFET switch, Schottky diode, and output capacitor, contains nanosecond rise times and fall times. Keep these rise times and fall times as short as possible.
- Place the VIN bypass capacitor as close to the VIN pin and the AGND pin as possible to reduce the IC supply ripple.
- Connect the AGND and PGND pins to thermal pad directly on the same layer.

10.2 Layout Example

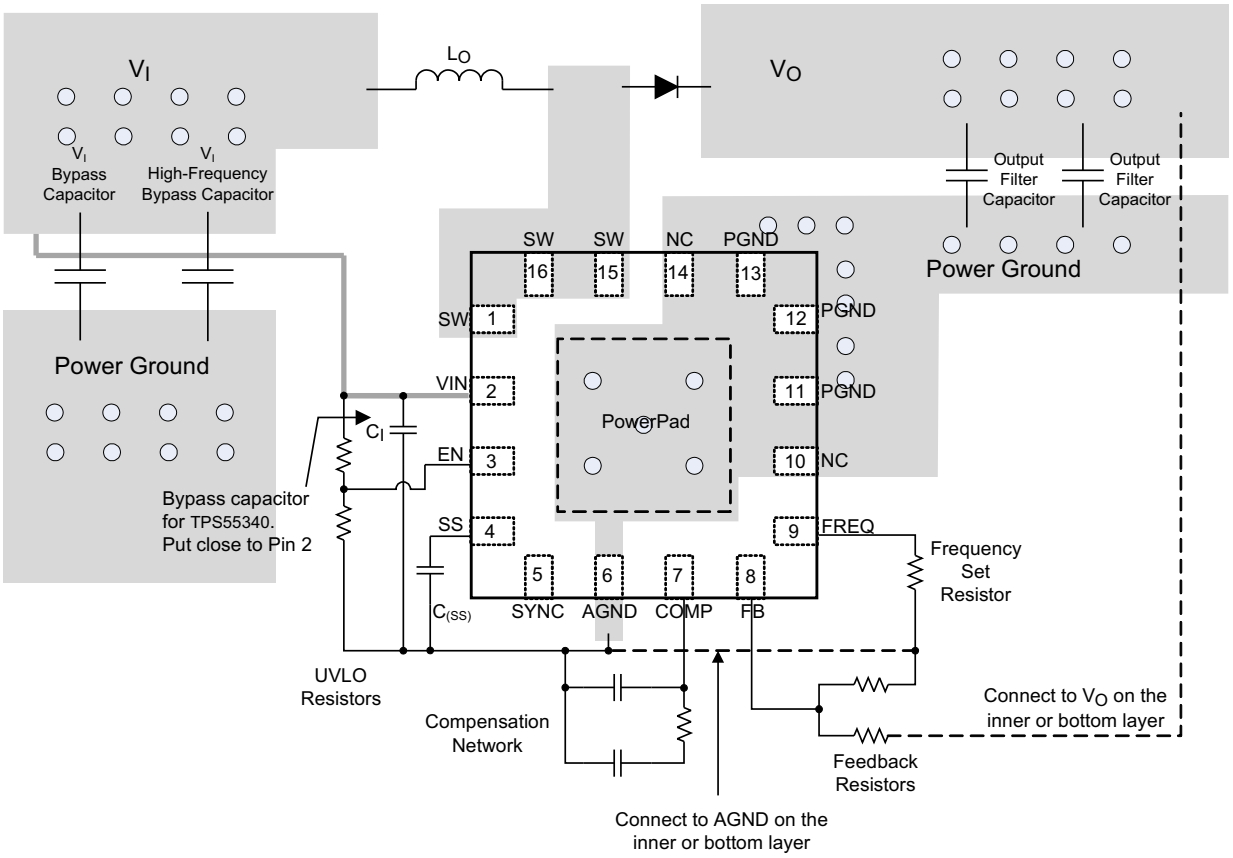


图 10-1. TPS55340 Layout Example

10.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. This restriction limits the power dissipation of the TPS55340. The TPS55340 features a thermally enhanced QFN package. This package includes a PowerPAD that improves the thermal capabilities of the package. The thermal resistance of the QFN package in any application greatly depends on the PCB layout and the PowerPAD connection. The PowerPAD must be soldered to the analog ground on the PCB. Use thermal vias underneath the PowerPAD to achieve good thermal performance.

11 Device and Documentation Support

11.1 Device Support

11.1.1 第三方产品免责声明

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11.1.2 Development Support

11.1.2.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the TPS55340 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS55340PWP	ACTIVE	HTSSOP	PWP	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	55340	Samples
TPS55340PWPR	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	55340	Samples
TPS55340RTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	55340	Samples
TPS55340RTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	55340	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

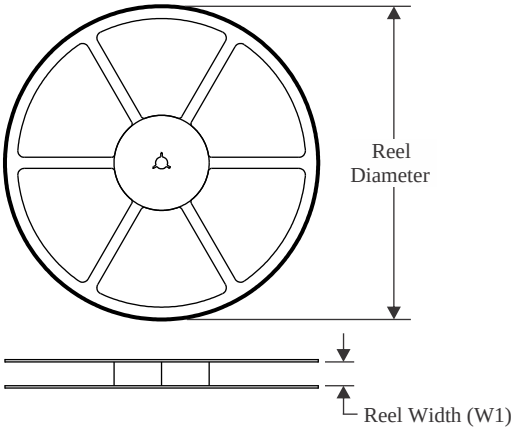
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

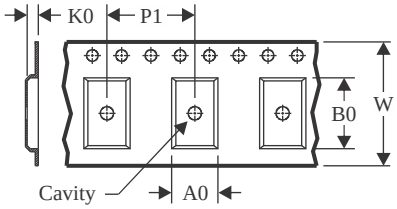
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

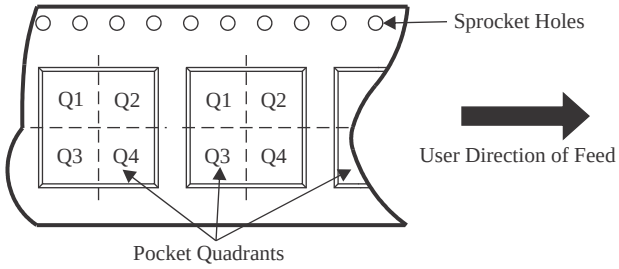


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

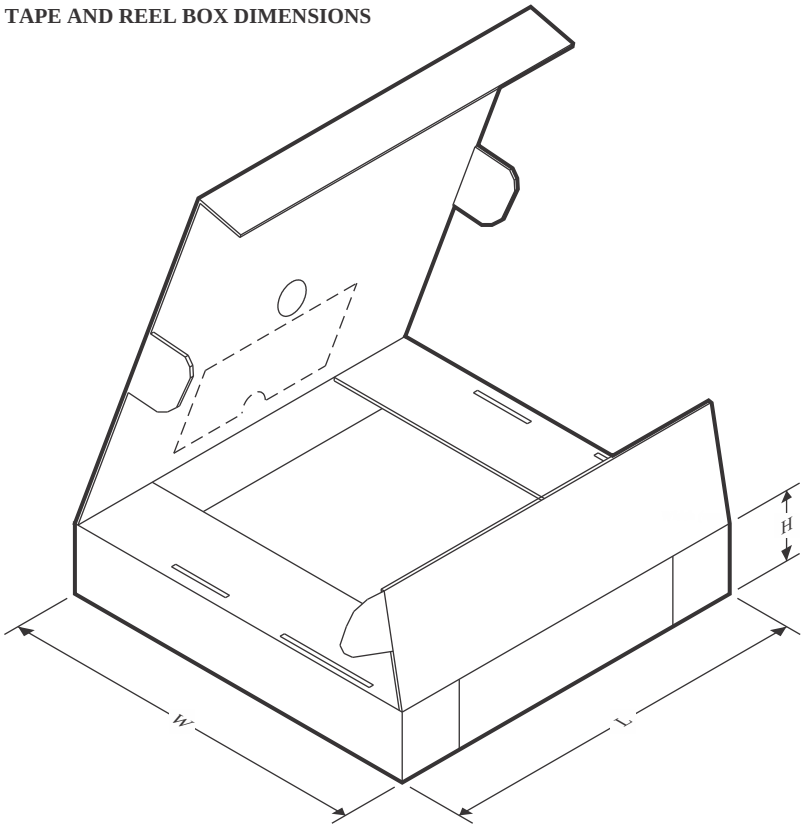
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS55340PWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS55340RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS55340RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

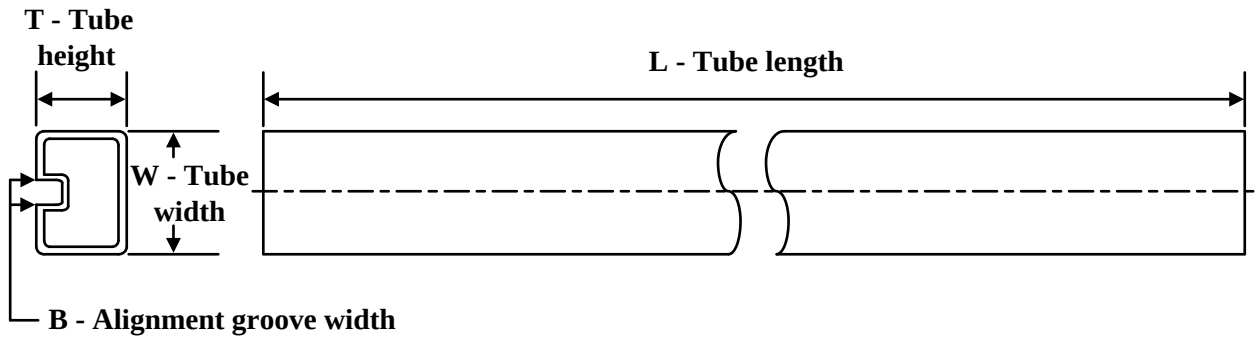
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS55340PWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0
TPS55340RTER	WQFN	RTE	16	3000	346.0	346.0	33.0
TPS55340RTET	WQFN	RTE	16	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS55340PWP	PWP	HTSSOP	14	90	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

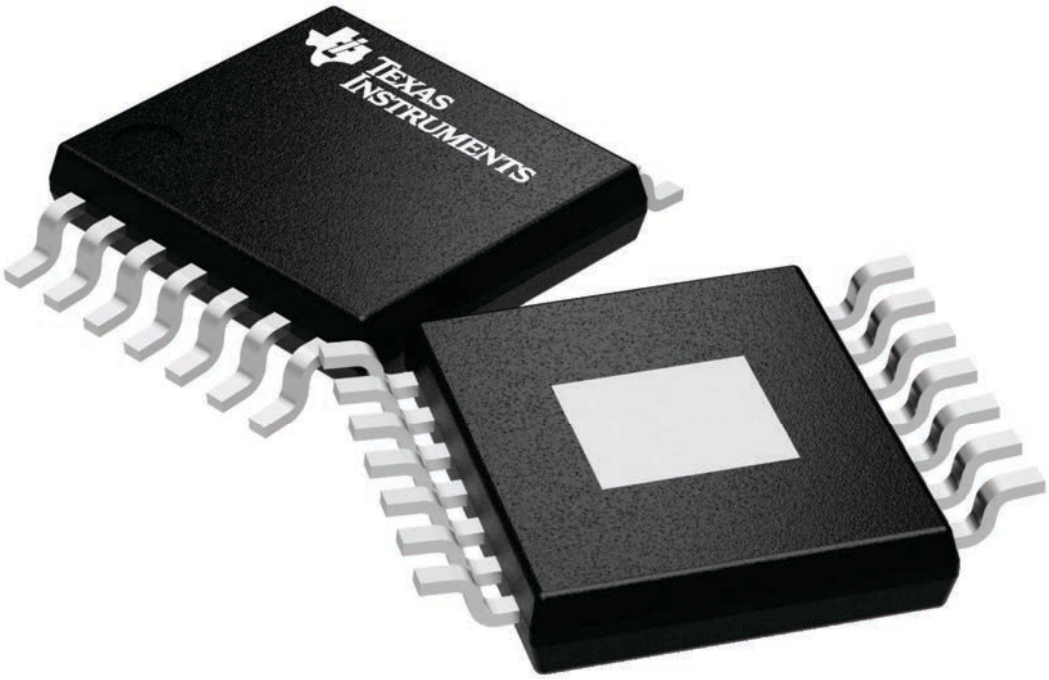
PWP 14

PowerPAD TSSOP - 1.2 mm max height

4.4 x 5.0, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



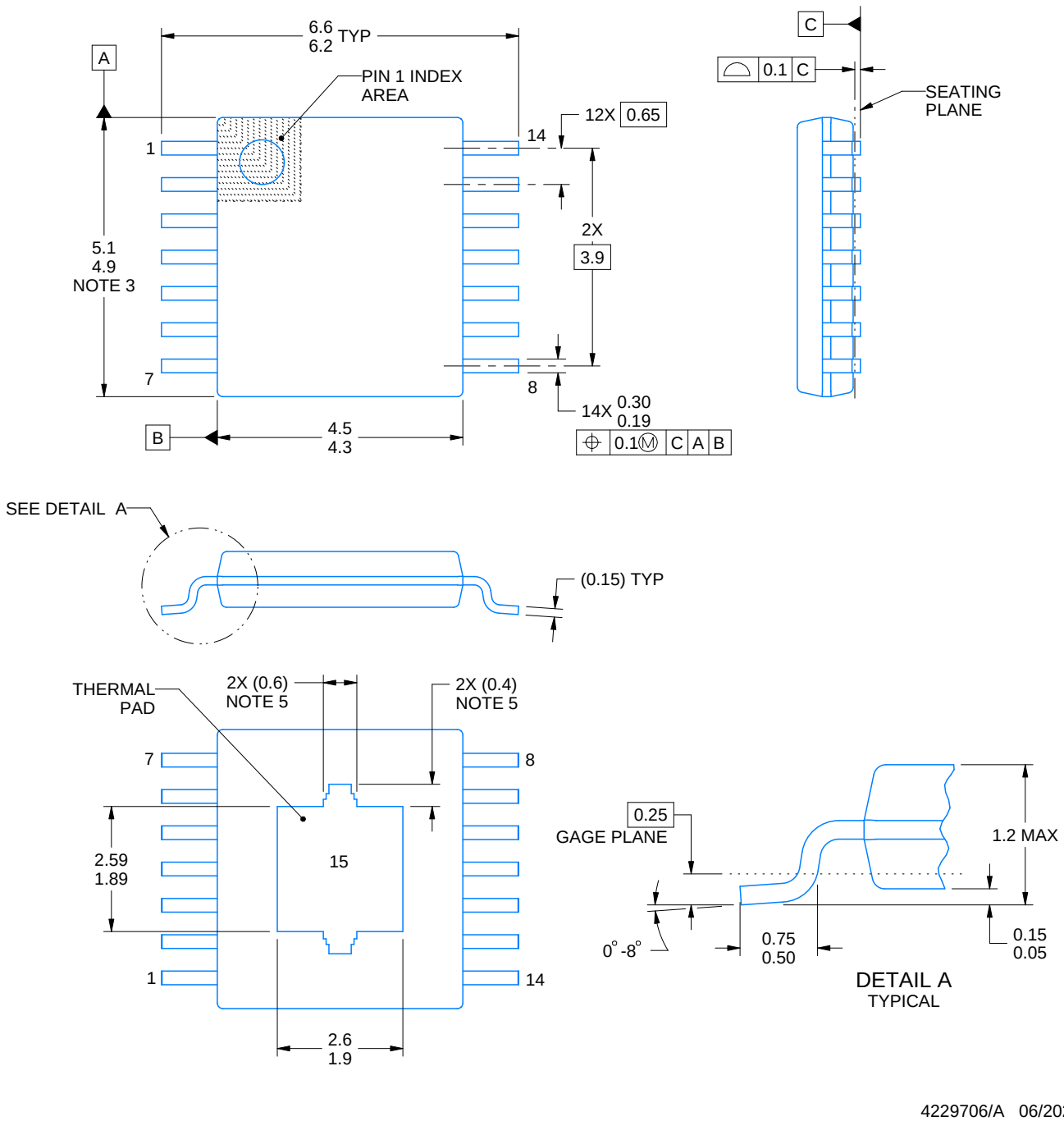
4224995/A

PACKAGE OUTLINE

PWP0014K

PowerPAD™ TSSOP - 1.2 mm max height

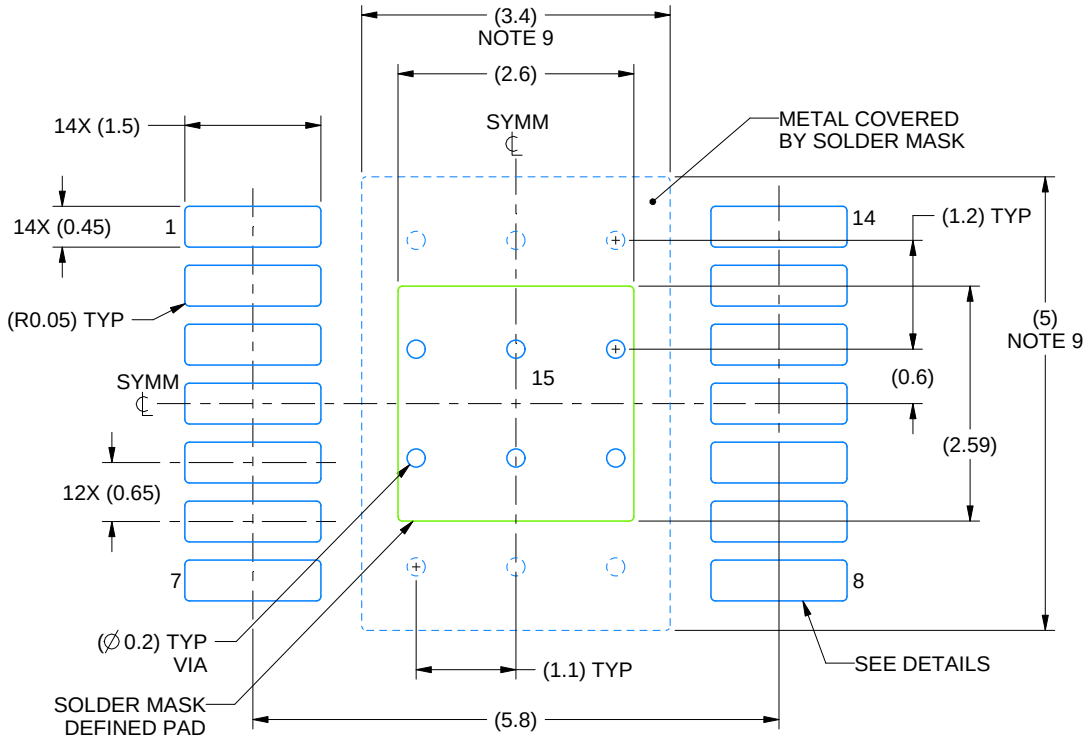
SMALL OUTLINE PACKAGE



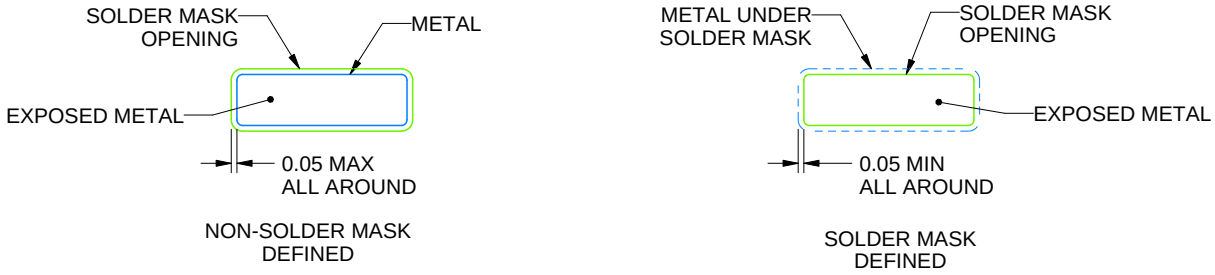
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

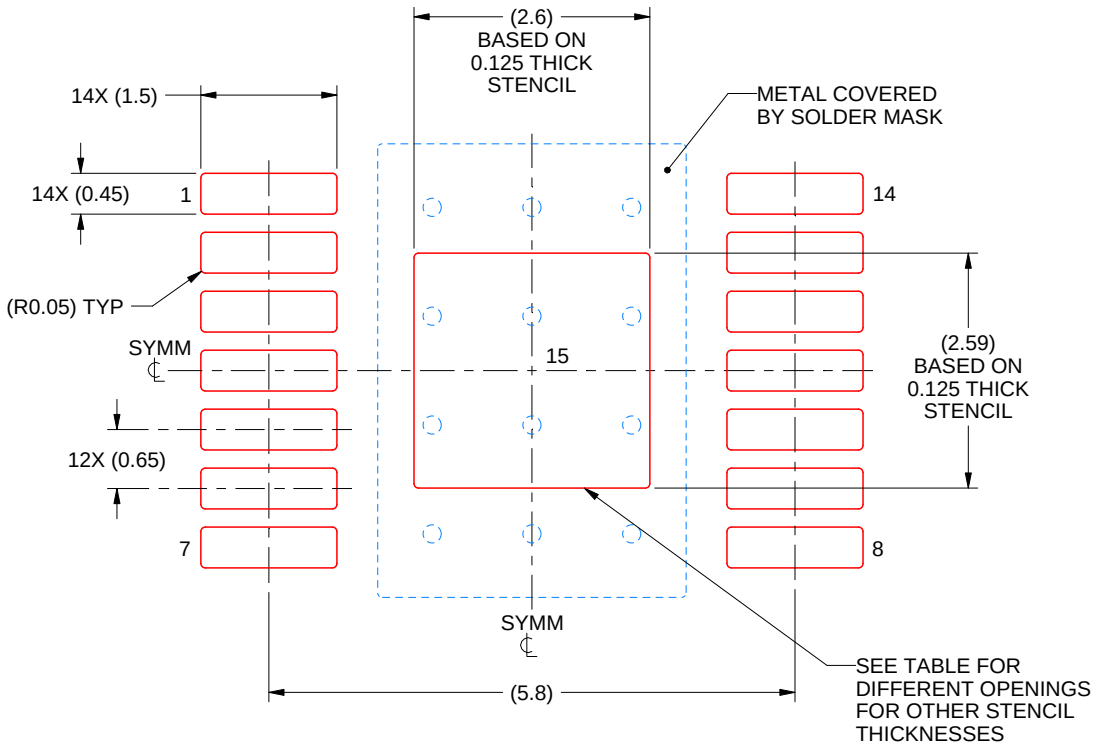


SOLDER MASK DETAILS

4229706/A 06/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 2.90
0.125	2.60 X 2.59 (SHOWN)
0.15	2.37 X 2.36
0.175	2.20 X 2.19

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

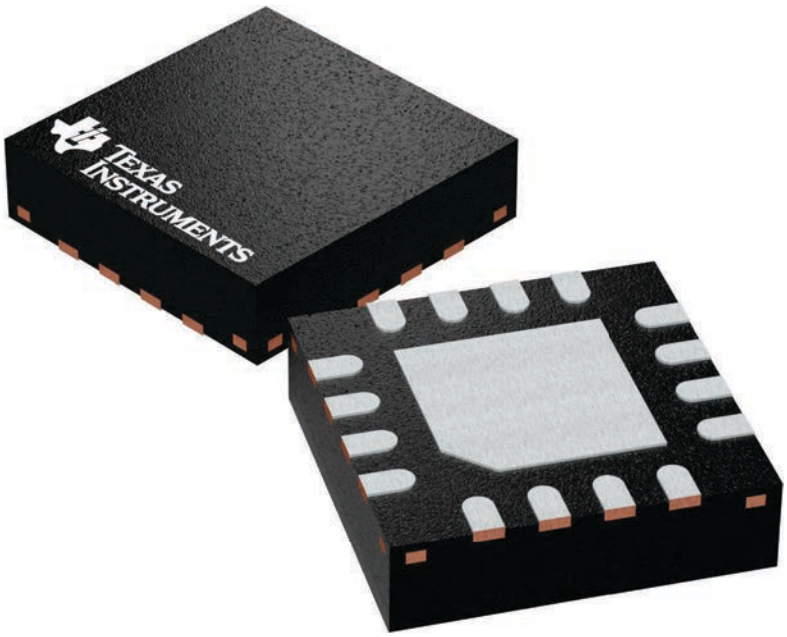
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

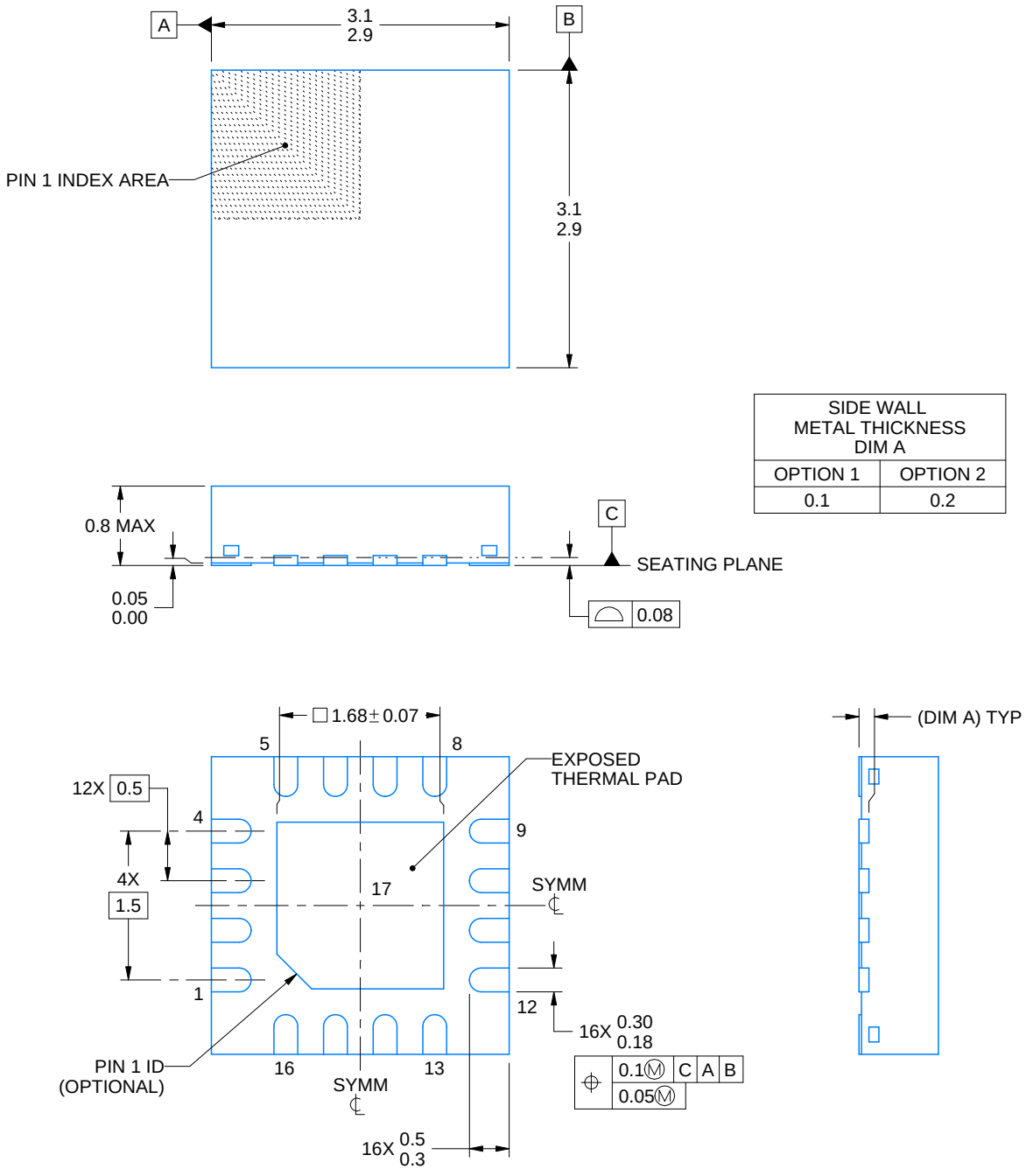


RTE0016C

PACKAGE OUTLINE

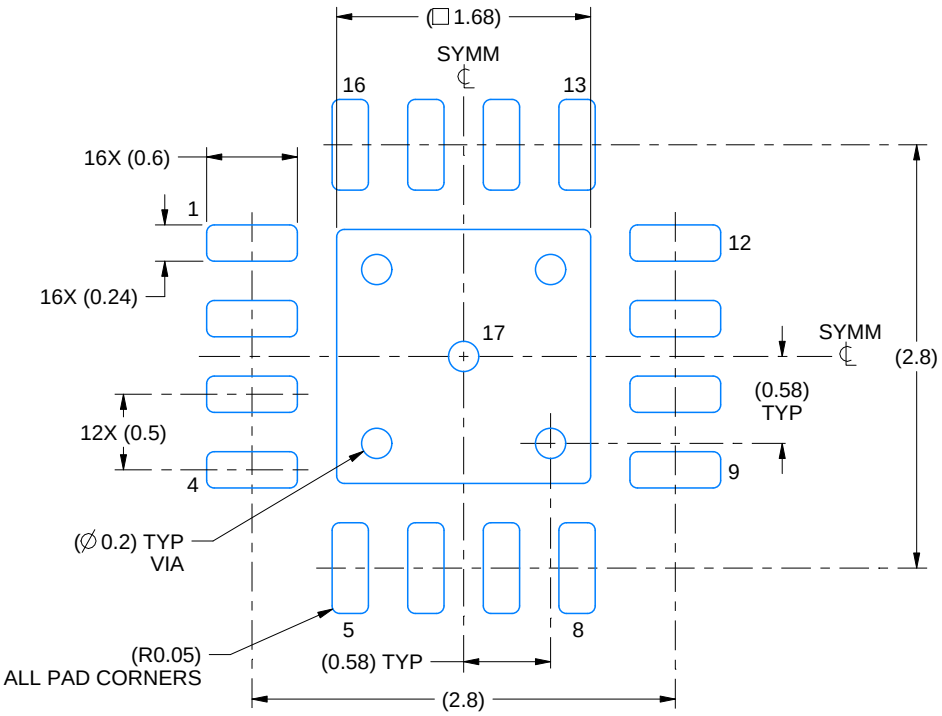
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

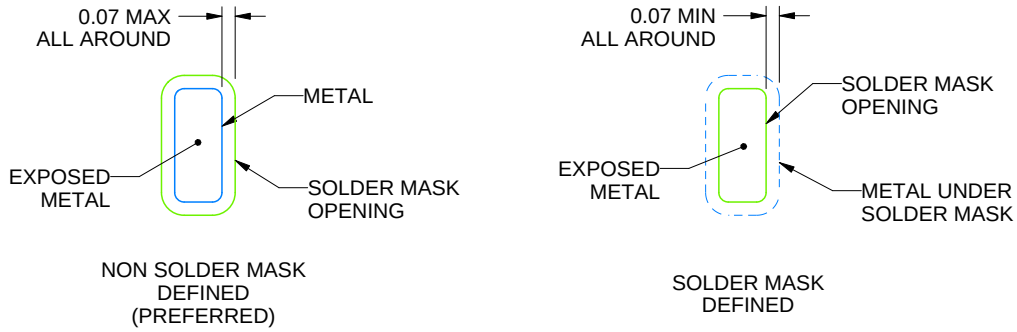


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

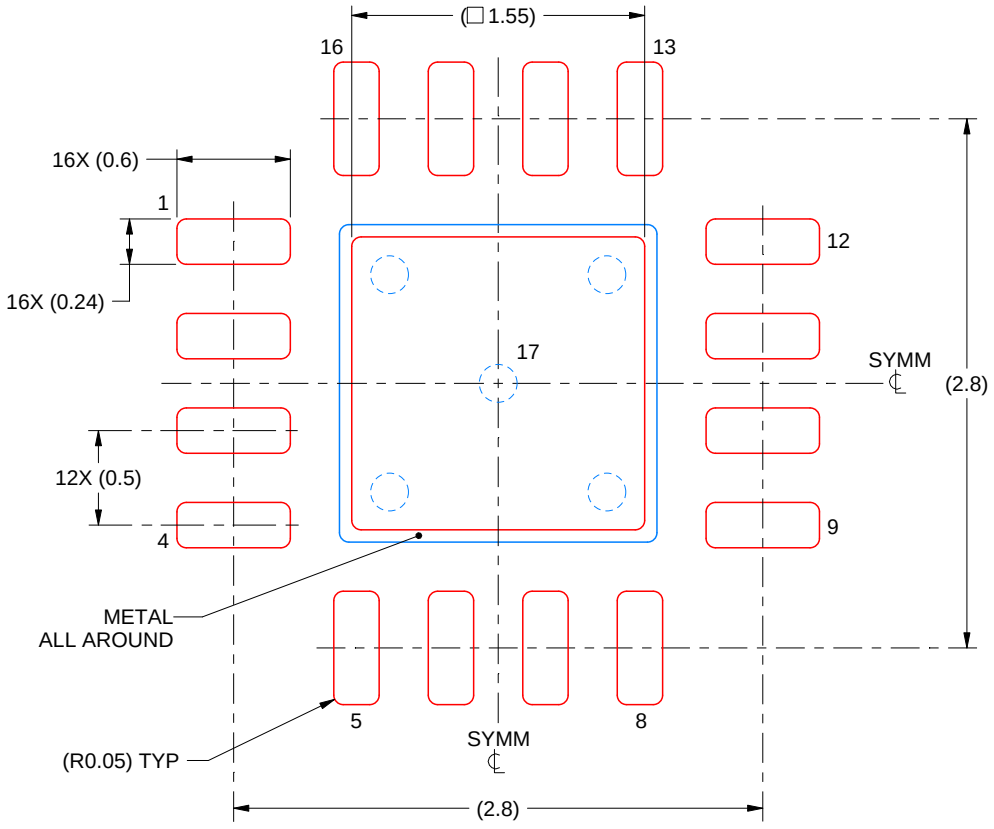


SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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