TPS54531 具有 Eco-mode 的 5A、28V 输入、SWIFT™ 降压转换器

1 特性

- 3.5V 至 28V 输入电压范围
- 可调节输出电压低至 0.8V
- 集成型 80mΩ 高侧 MOSFET 支持高达 5A 的持续输出电流
- 使用脉冲跳跃 Eco-mode 在轻负载条件下实现高效率
- 570kHz 固定开关频率
- 1μA 关断静态电流（典型值）
- 可调节慢启动限制浪涌电流
- 可编程 UVLO 阈值
- 过压瞬态保护
- 逐周期电流限制、频率折返和热关断保护
- 采用易于使用的耐热增强型 8 引脚 SO PowerPAD™ 集成电路封装
- 使用 TPS56637 以更小的封装实现更高的效率
- 使用 TPS54531 并借助 WEBENCH® Power Designer 创建定制设计方案

2 应用

- 消费类应用，例如机顶盒、CPE 设备、LCD 显示屏、外设和电池充电器
- 工业用和车载音频电源
- 5V、12V 和 24V 分布式电源系统

3 说明

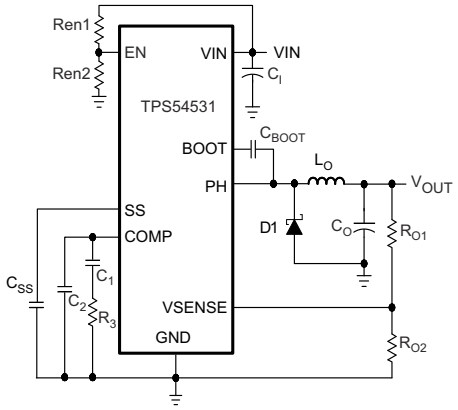
TPS54531 器件是一款 28V、5A 非同步降压转换器，集成有一个低 $R_{DS(on)}$ 的高侧 MOSFET。该器件会在轻负载时自动激活脉冲跳跃 Eco-mode 功能以提升效率。此外，1μA 的关断电源电流使得该器件适用于电池供电类应用。具有内部斜坡补偿的电流模式控制简化了外部补偿计算，并在允许使用陶瓷输出电容器的同时减少了元件数量。一个电阻分压器对输入欠压锁定的迟滞进行编程。过压瞬态保护电路可限制启动期间和瞬态条件下的电压过冲。逐周期电流限制机制、频率折返和热关断特性可在过载条件下对器件和负载施加保护。TPS54531 器件可采用 8 引脚 SO PowerPAD 集成电路封装，这些封装经过内部优化可改进热性能。

封装信息

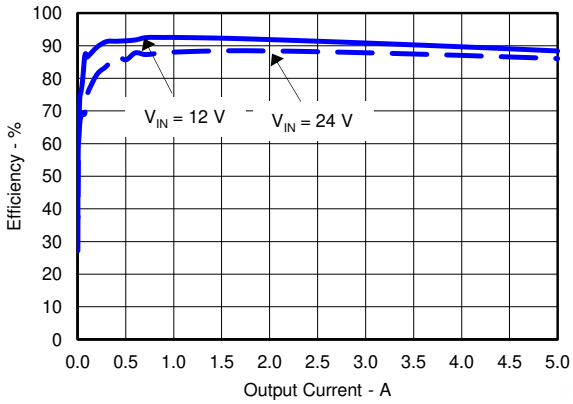
器件型号	封装(1)	封装尺寸(2)
TPS54531	DDA（SO PowerPAD，8）	4.9mm × 6mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



简化版原理图



TPS54531 效率

本资源的原文使用英文撰写。为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (October 2014) to Revision B (October 2023)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 在*特性* 中添加了 TPS56637 信息	1
• 将英文版中*封装信息* 表的列标题从 BODY SIZE 更改为 PACKAGE SIZE	1
• 更新了商标信息	1
• 在*特性* 部分添加了 WEBENCH 支持说明	1
• Moved storage temperature to the *Absolute Maximum Ratings* table	4
• Changed table title from *Handling Ratings* to *ESD Ratings*	4
• Added WEBENCH design steps	14
• Added WEBENCH information in the *Development Support* section	25

Changes from Revision * (May 2013) to Revision A (October 2014)	Page
• 添加了*处理额定值* 表、*特性说明* 部分、*器件功能模式* 部分、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分	1
• Added equation for I_{ripple} in the *Inductor Selection* section	15

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5 Pin Configuration and Functions

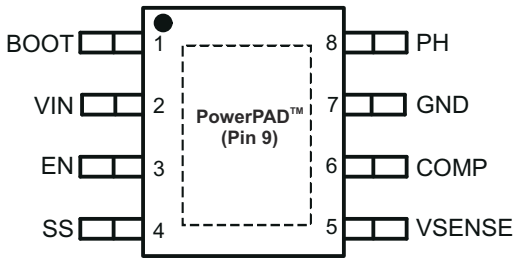


图 5-1. DDA Package, 8-Pin SO With PowerPAD™ Integrated Circuit Package Top View

表 5-1. Pin Functions

PIN		TYPE (1)	DESCRIPTION
NO.	NAME		
1	BOOT	O	A 0.1- μ F bootstrap capacitor is required between the BOOT and PH pins. If the voltage on this capacitor falls below the minimum requirement, the high-side MOSFET is forced to switch off until the capacitor is refreshed.
2	VIN	I	This pin is the 3.5- to 28-V input supply voltage.
3	EN	I	This pin is the enable pin. To disable, pull below 1.25 V. Float this pin to enable. Programming the input undervoltage lockout with two resistors is recommended.
4	SS	I	This pin is slow-start pin. An external capacitor connected to this pin sets the output rise time.
5	VSENSE	I	This pin is the inverting node of the transconductance (gm) error amplifier.
6	COMP	O	This pin is the error-amplifier output and the input to the PWM comparator. Connect frequency compensation components to this pin.
7	GND	—	Ground pin
8	PH	O	The PH pin is the source of the internal high-side power MOSFET.
9	PowerPAD integrated circuit package	—	For proper operation, the GND pin must be connected to the exposed pad.

(1) I = input, O = output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Voltage	VIN	–0.3	30	V
	EN	–0.3	6	
	BOOT		38	
	VSENSE	–0.3	3	
	COMP	–0.3	3	
	SS	–0.3	3	
Output Voltage	BOOT-PH		8	V
	PH	–0.6	30	
	PH (10 ns transient from ground to negative peak)		–5	
Source Current	EN		100	µA
	BOOT		100	mA
	VSENSE		10	µA
	PH	Current Limit		A
Sink Current	VIN	Current Limit		A
	COMP		100	µA
	SS		200	
Operating Junction Temperature		–40	150	°C
Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2	2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–1	1	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
	Operating Input Voltage on the VIN pin	3.5	28	V
T_J	Operating junction temperature	–40	150	°C

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6.4 Thermal Information

THERMAL METRIC(1)		DDA	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	55	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	31.5	
ψ_{JT}	Junction-to-top characterization parameter	14.9	
ψ_{JB}	Junction-to-board characterization parameter	31.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_J = –40°C to 150°C, VIN = 3.5V to 28V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
Internal undervoltage lockout threshold	Rising and falling			3.5	V
Shutdown supply current	EN = 0 V, VIN = 12 V, –40°C to 85°C		1	4	µA
Operating – non-switching supply current	VSENSE = 0.85 V		110	190	µA
ENABLE AND UVLO (EN PIN)					
Enable threshold	Rising and falling		1.25	1.35	V
Input current	Enable threshold – 50 mV		–1		µA
Input current	Enable threshold + 50 mV		–4		µA
VOLTAGE REFERENCE					
Voltage reference		0.772	0.8	0.828	V
HIGH-SIDE MOSFET					
On resistance	BOOT-PH = 3 V, VIN = 3.5 V		115	200	mΩ
	BOOT-PH = 6 V, VIN = 12 V		80	150	
ERROR AMPLIFIER					
Error amplifier transconductance (gm)	–2 µA < $I_{(COMP)}$ < 2 µA, $V_{(COMP)}$ = 1 V		92		µmhos
Error amplifier DC gain(1)	VSENSE = 0.8 V		800		V/V
Error amplifier unity gain bandwidth(1)	5 pF capacitance from COMP to GND pins		2.7		MHz
Error amplifier source/sink current	$V_{(COMP)}$ = 1 V, 100-mV overdrive		±7		µA
Switch current to COMP transconductance(1)	VIN = 12 V		20		A/V
SWITCHING FREQUENCY					
Switching Frequency	VIN = 12 V, 25°C	456	570	684	kHz
Minimum controllable on time	VIN = 12 V, 25°C		105	130	ns
Maximum controllable duty ratio(1)	BOOT-PH = 6 V	90%	93%		
PULSE SKIPPING Eco-mode					
Pulse skipping Eco-mode switch current threshold			160		mA
CURRENT LIMIT					
Current-limit threshold	VIN = 12 V	6.3	10.5		A
THERMAL SHUTDOWN					
Thermal Shutdown			165		°C
SLOW START (SS PIN)					
Charge current	$V_{(SS)}$ = 0.4 V		2		µA

(1) Specified by design

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6.6 Typical Characteristics

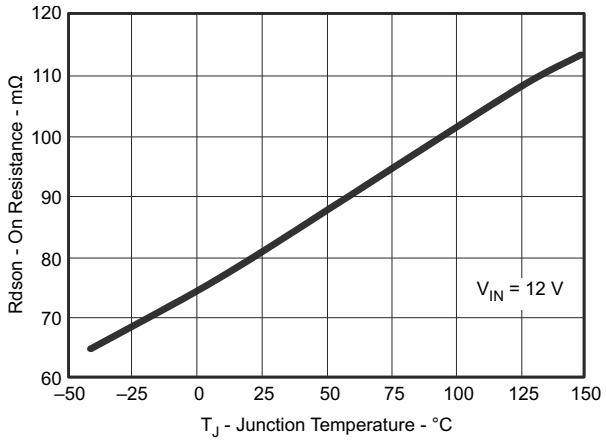


图 6-1. ON Resistance vs Junction Temperature

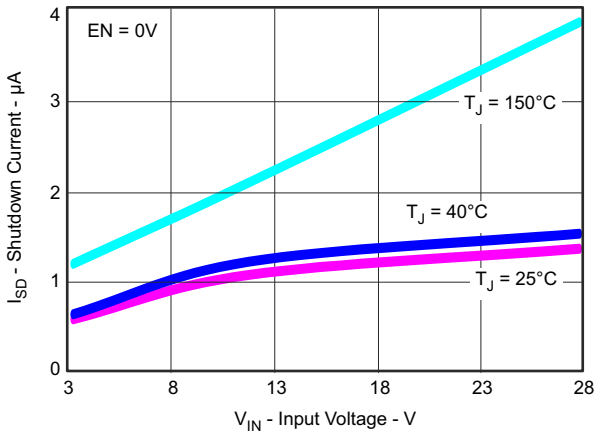


图 6-2. Shutdown Quiescent Current vs Input Voltage

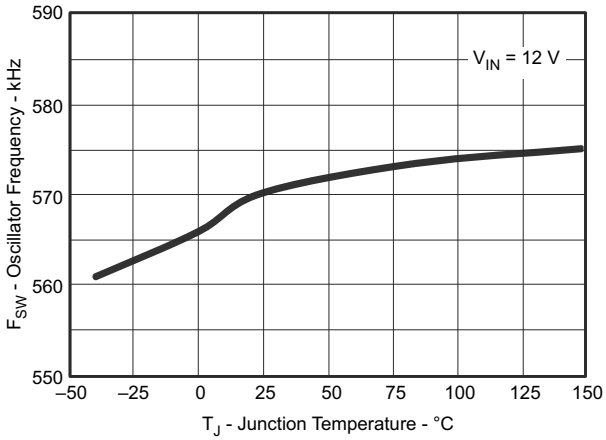


图 6-3. Switching Frequency vs Junction Temperature

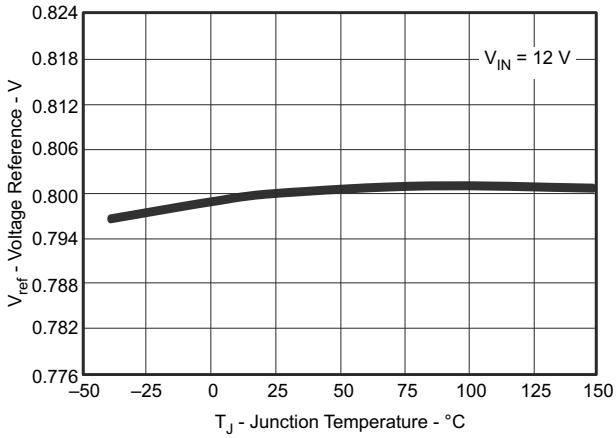


图 6-4. Voltage Reference vs Junction Temperature

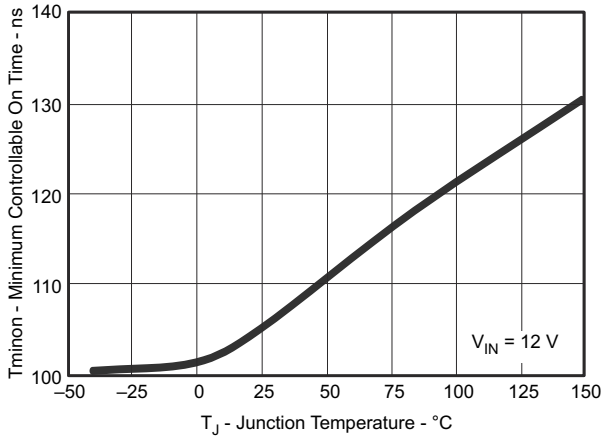


图 6-5. Minimum Controllable ON Time vs Junction Temperature

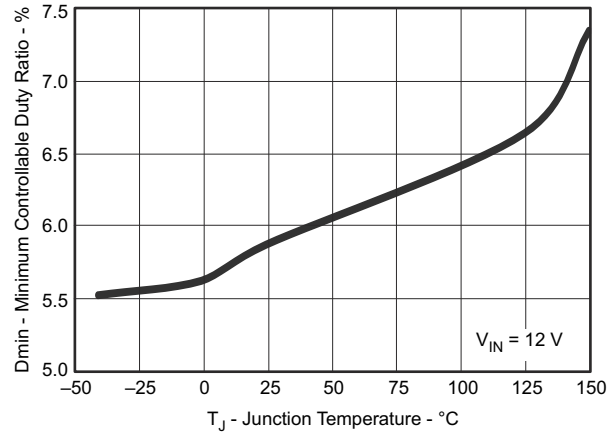


图 6-6. Minimum Controllable Duty Ratio vs Junction Temperature

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6.6 Typical Characteristics (continued)

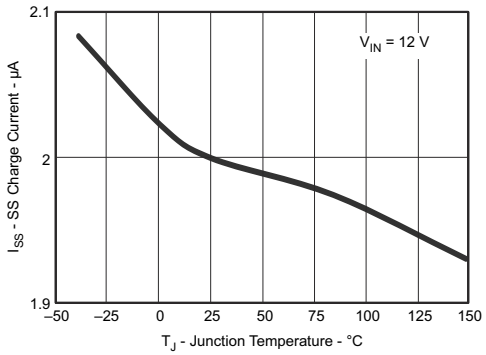


图 6-7. SS Charge Current vs Junction Temperature

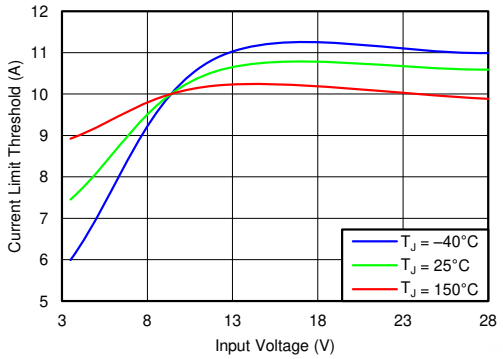


图 6-8. Current-Limit Threshold vs Input Voltage

7 Detailed Description

7.1 Overview

The TPS54531 device is a 28-V, 5-A, step-down (buck) converter with an integrated high-side n-channel MOSFET. To improve performance during line and load transients, the device implements a constant-frequency, current mode control which reduces output capacitance and simplifies external frequency compensation design. The TPS54531 device has a preset switching frequency of 570 kHz.

The TPS54531 device requires a minimum input voltage of 3.5 V for normal operation. The EN pin has an internal pullup current source that can be used to adjust the input-voltage undervoltage lockout (UVLO) with two external resistors. In addition, the pullup current provides a default condition when the EN pin is floating for the device to operate. The operating current is 110 μA (typical) when not switching and under no load. When the device is disabled, the supply current is 1 μA (typical).

The integrated 80-mΩ high-side MOSFET allows for high-efficiency power-supply designs with continuous output currents up to 5 A.

The TPS54531 device reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by an external capacitor on the BOOT to PH pin. The boot capacitor voltage is monitored by an UVLO circuit and turns the high-side MOSFET off when the voltage falls below a preset threshold of 2.1 V (typical). The output voltage can be stepped down to as low as the reference voltage.

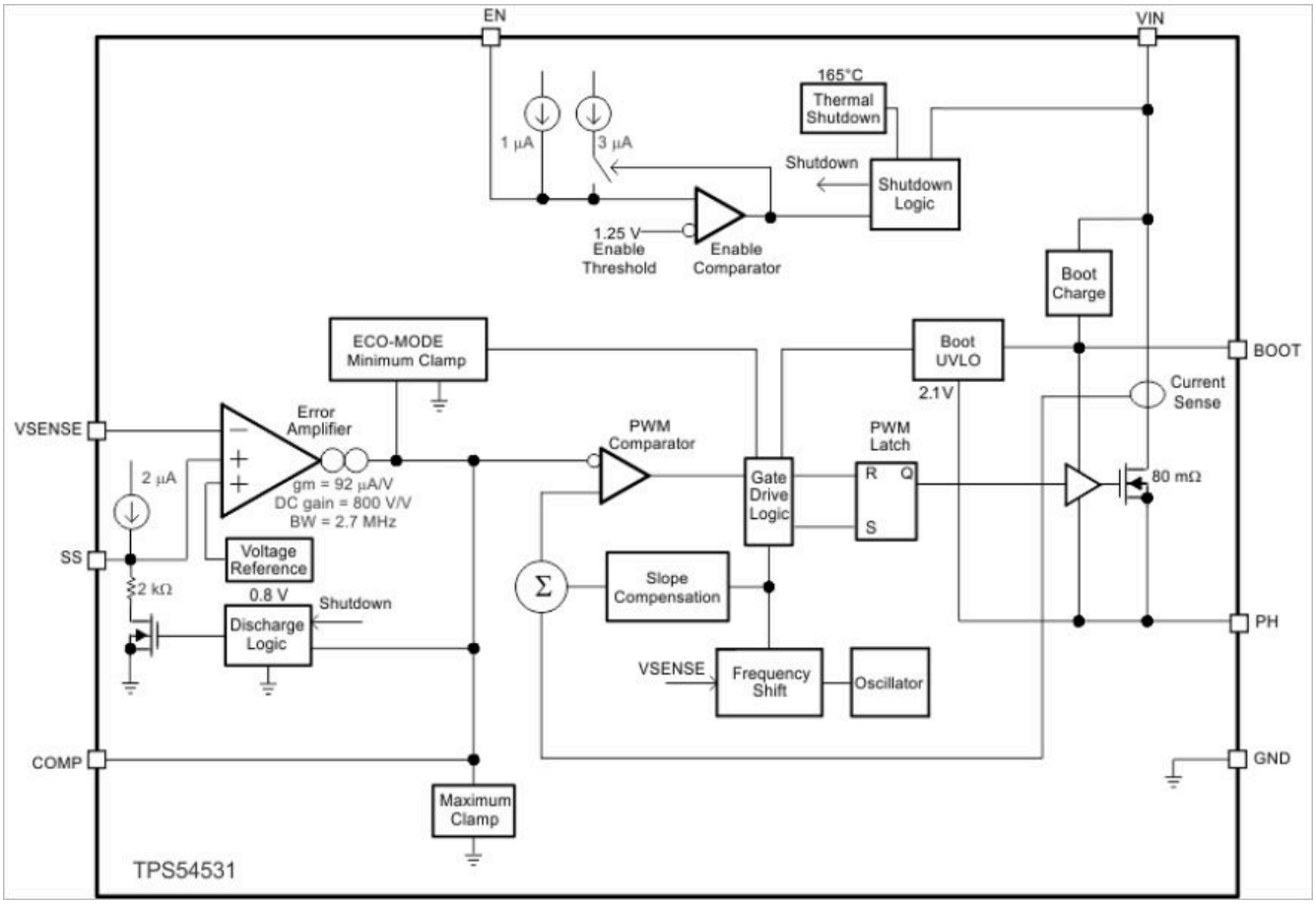
By adding an external capacitor, the slow-start time of the TPS54531 device can be adjustable which enables flexible output filter selection.

To improve the efficiency at light load conditions, the TPS54531 device enters a special pulse skipping Eco-mode when the peak inductor current drops below 160 mA (typical).

The frequency foldback reduces the switching frequency during start-up and overcurrent conditions to help control the inductor current. The thermal shutdown provides the additional protection under fault conditions.

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7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fixed-Frequency PWM Control

The TPS54531 device uses a fixed-frequency, peak-current mode control. The internal switching frequency of the TPS54531 device is fixed at 570 kHz.

7.3.2 Voltage Reference (V_{ref})

The voltage reference system produces a ±2% initial accuracy voltage reference (±3.5% over temperature) by scaling the output of a temperature stable bandgap circuit. The typical voltage reference is designed at 0.8 V.

7.3.3 Bootstrap Voltage (BOOT)

The TPS54531 device has an integrated boot regulator and requires a 0.1-µF ceramic capacitor between the BOOT and PH pins to provide the gate-drive voltage for the high-side MOSFET. A ceramic capacitor with an X7R- or X5R-grade dielectric is recommended because of the stable characteristics over temperature and voltage. To improve drop out, the TPS54531 device is designed to operate at 100% duty cycle as long as the BOOT-to-PH pin voltage is greater than 2.1 V (typical).

7.3.4 Enable and Adjustable Input Undervoltage Lockout (VIN UVLO)

The EN pin has an internal pullup current-source that provides the default condition of the TPS54531 device while operating when the EN pin floats.

The TPS54531 device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. Using an external VIN UVLO to add at least 500-mV hysteresis is recommended unless the VIN voltage is greater than

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(V_{OUT} + 2 V). To adjust the VIN UVLO with hysteresis, use the external circuitry connected to the EN pin as shown in 图 7-1. When the EN pin voltage exceeds 1.25 V, an additional 3 µA of hysteresis is added. Use 方程式 1 and 方程式 2 to calculate the resistor values required for the desired VIN UVLO threshold voltages. The V_{STOP} must always be greater than 3.5 V.

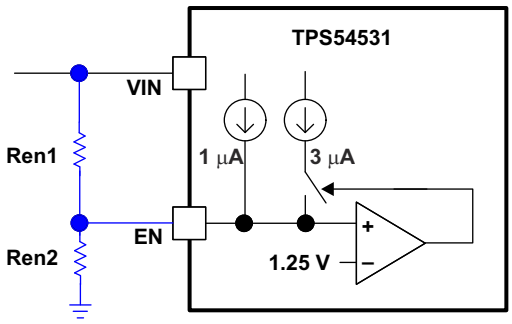


图 7-1. Adjustable Input Undervoltage Lockout

$$Ren1 = \frac{V_{START} - V_{STOP}}{3\mu A} \quad (1)$$

where

- V_{START} is the input start threshold voltage
- V_{STOP} is the input stop threshold voltage

$$Ren2 = \frac{V_{EN}}{\frac{V_{START} - V_{EN}}{Ren1} + 1\mu A} \quad (2)$$

where

- V_{EN} is the enable threshold voltage of 1.25 V

The external start and stop voltages are approximate. The actual start and stop voltages can vary.

7.3.5 Programmable Slow Start Using SS Pin

Programming the slow-start time externally is highly recommended because no slow-start time is implemented internally. The TPS54531 device effectively uses the lower voltage of the internal voltage reference or the SS pin voltage as the reference voltage of the power supply that is fed into the error amplifier and regulates the output accordingly. A capacitor (C_{SS}) on the SS pin to ground implements a slow-start time. The TPS54531 device has an internal pullup current source of 2 µA that charges the external slow-start capacitor. Use 方程式 3 to calculate the slow-start time (10% to 90%).

$$T_{SS}\left(ms\right) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)} \quad (3)$$

where

- V_{REF} = 0.8 V
- I_{SS} = 2 µA

The slow-start time must be set between 1 ms to 10 ms to ensure good startup behavior. The value slow-start capacitor must not exceed 27 nF.

During normal operation, the TPS54531 device stops switching if the input voltage drops below the VIN UVLO threshold, the EN pin is pulled below 1.25 V, or a thermal shutdown event occurs.

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7.3.6 Error Amplifier

The TPS54531 device has a transconductance amplifier for the error amplifier. The error amplifier compares the VSENSE voltage to the internal effective voltage reference presented at the input of the error amplifier. The transconductance of the error amplifier is 92 μA/V during normal operation. Frequency compensation components are connected between the COMP pin and ground.

7.3.7 Slope Compensation

To prevent the sub-harmonic oscillations when operating the device at duty cycles greater than 50%, the TPS54531 device adds a built-in slope compensation which is a compensating ramp to the switch-current signal.

7.3.8 Current-Mode Compensation Design

The device is able to work with various types of output capacitors with appropriate compensation designs. For designs using ceramic output capacitors, proper derating of ceramic output capacitance is recommended when performing the stability analysis because the actual ceramic capacitance drops considerably from the nominal value when the applied voltage increases. For the detailed guidelines, see the *节 8.2.2* section.

7.3.9 Overcurrent Protection and Frequency Shift

The TPS54531 device implements current mode control that uses the COMP pin voltage to turn off the high-side MOSFET on a cycle-by-cycle basis. During each cycle the switch current and the COMP pin voltage are compared. When the peak inductor current intersects the COMP pin voltage, the high-side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, causing the switch current to increase. The COMP pin has a maximum clamp internally, which limits the output current.

The TPS54531 device provides robust protection during short circuits. Overcurrent runaway is possible in the output inductor during a short circuit at the output. The TPS54531 device solves this issue by increasing the off time during short-circuit conditions by lowering the switching frequency. The switching frequency is divided by 1, 2, 4, and 8 as the voltage ramps from 0 V to 0.8 V on VSENSE pin. The relationship between the switching frequency and the VSENSE pin voltage is listed in 表 7-1.

表 7-1. Switching Frequency Conditions

SWITCHING FREQUENCY	VSENSE PIN VOLTAGE
570 kHz	VSENSE ⩾ 0.6 V
570 kHz / 2	0.6 V > VSENSE ⩾ 0.4 V
570 kHz / 4	0.4 V > VSENSE ⩾ 0.2 V
570 kHz / 8	0.2 V > VSENSE

7.3.10 Overvoltage Transient Protection

The TPS54531 device incorporates an overvoltage transient-protection (OVTP) circuit to minimize output voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP circuit includes an overvoltage comparator to compare the VSENSE pin voltage and internal thresholds. When the VSENSE pin voltage goes above 109% × V_{ref}, the high-side MOSFET is forced off. When the VSENSE pin voltage falls below 107% × V_{ref}, the high-side MOSFET is enabled again.

7.3.11 Thermal Shutdown

The device implements an internal thermal shutdown to protect the device if the junction temperature exceeds 165°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. When the die temperature decreases below 165°C, the device reinitiates the power-up sequence.

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7.4 Device Functional Modes

7.4.1 Eco-mode

The TPS54531 is designed to operate in pulse skipping Eco-mode at light load currents to boost light load efficiency. When the peak inductor current is lower than 160 mA (typical), the COMP pin voltage falls to 0.5 V (typical) and the device enters Eco-mode . When the device is in Eco-mode, the COMP pin voltage is clamped at 0.5-V internally which prevents the high-side integrated MOSFET from switching. The peak inductor current must rise above 160 mA for the COMP pin voltage to rise above 0.5 V and exit Eco-mode. Because the integrated current comparator catches the peak inductor current only, the average load current entering Eco-mode varies with the applications and external output filters.

7.4.2 Operation With V_{IN} < 3.5 V

The device is recommended to operate with input voltages above 3.5 V. The typical VIN UVLO threshold is not specified and the device can operate at input voltages down to the UVLO voltage. At input voltages below the actual UVLO voltage, the device does not switch. If the EN pin is externally pulled up or left floating, the device becomes active when the VIN pin passes the UVLO threshold. Switching begins when the slow-start sequence is initiated.

7.4.3 Operation With EN Control

The enable threshold voltage is 1.25 V (typical). With the EN pin is held below that voltage the device is disabled and switching is inhibited even if the VIN pin is above the UVLO threshold. The IC quiescent current is reduced in this state. If the EN voltage increases above the threshold while the VIN pin is above the UVLO threshold, the device becomes active. Switching is enabled, and the slow-start sequence is initiated.

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8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The TPS54531 device is typically used as a step-down converter, which converts a voltage from 3.5 V to 28 V to a lower voltage. WEBENCH® software is available to aid in the design and analysis of circuits.

For additional design needs, see the following devices:

	TPS54231	TPS54232	TPS54233	TPS54531	TPS54332
I(max)	2 A	2 A	2 A	5 A	3.5 A
Input voltage range	3.5 to 28 V	3.5 to 28 V	3.5 to 28 V	3.5 to 28 V	3.5 to 28 V
Switching frequency (typical)	570 kHz	1000 kHz	285 kHz	570 kHz	1000 kHz
Switch current limit (minimum)	2.3 A	2.3 A	2.3 A	5.5 A	4.2 A
Pin and package	8SOIC	8SOIC	8SOIC	8SO PowerPAD integrated circuit package	8SO PowerPAD integrated circuit package

8.2 Typical Application

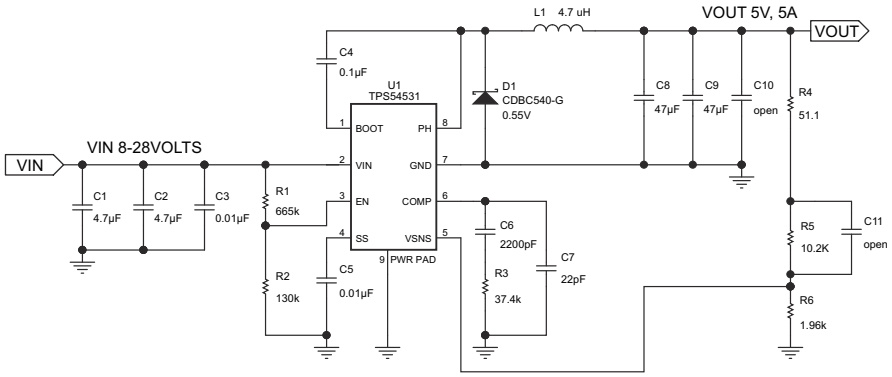


图 8-1. Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the values listed in 表 8-1 as the input parameters

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	8 to 28 V
Output voltage	5 V
Transient response, 2.5-A load step	ΔV_{OUT} = ±5%
Input ripple voltage	400 mV
Output ripple voltage	30 mV
Output current rating	5 A
Operating Frequency	570 kHz

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8.2.2 Detailed Design Procedure

The following design procedure can be used to select component values for the TPS54531 device. Alternately, the WEBENCH software can be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the WEBENCH Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, users are able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Switching Frequency

The switching frequency for the TPS54531 is fixed at 570 kHz.

8.2.2.3 Output Voltage Set Point

The output voltage of the TPS54531 device is externally adjustable using a resistor divider network. As shown in 图 8-1, this divider network is comprised of R5 and R6. The relationship of the output voltage to the resistor divider is given by 方程式 4 and 方程式 5:

$$R6 = \frac{R5 \times V_{REF}}{V_{OUT} - V_{REF}} \tag{4}$$

$$V_{OUT} = V_{REF} \times \left(\frac{R5}{R6} + 1\right) \tag{5}$$

Select a value of R5 to be approximately 10 kΩ. Slightly increasing or decreasing the value of R5 can result in closer output-voltage matching when using standard value resistors. In this design, R5 = 10.2 kΩ and R6 = 1.96 kΩ, resulting in a 4.96 V output voltage. The 51.1-Ω resistor, R4, is provided as a convenient location to break the control loop for stability testing.

8.2.2.4 Undervoltage Lockout Set Point

The undervoltage lockout (UVLO) can be adjusted using the external voltage divider network of R1 and R2. R1 is connected between the VIN and EN pins of the TPS54531 device and R2 is connected between the EN and GND pins. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the design example, the minimum input voltage is 8 V. Therefore the start voltage threshold is set to 7 V with 2-V hysteresis. Use 方程式 1 and 方程式 2 to calculate the values for the upper and lower resistor values of R1 and R2.

8.2.2.5 Input Capacitors

The TPS54531 device requires an input decoupling capacitor and, depending on the application, a bulk input capacitor. The typical recommended value for the decoupling capacitor is 10 µF. A high-quality ceramic type X5R or X7R is recommended. The voltage rating must be greater than the maximum input voltage. A smaller value can be used as long as all other requirements are met; however 10 µF has been shown to work well in a

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wide variety of circuits. Additionally, some bulk capacitance can be required, especially if the TPS54531 circuit is not located within about 2 inches from the input voltage source. The value for this capacitor is not critical but must be rated to handle the maximum input voltage including ripple voltage, and must filter the output so that input ripple voltage is acceptable. For this design two 4.7-μF capacitors are used for the input decoupling capacitor. The capacitors are X7R dielectric rated for 50 V. The equivalent series resistance (ESR) is approximately 2 mΩ and the current rating is 3 A. Additionally, a small 0.01 μF capacitor is included for high frequency filtering.

Use 方程式 6 to calculate the input ripple voltage.

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times F_{SW}} + \left(I_{OUT(MAX)} \times ESR_{MAX}\right) \quad (6)$$

where

- $I_{OUT(MAX)}$ is the maximum load current
- C_{BULK} is the bulk capacitor value
- F_{SW} is the switching frequency
- ESR_{MAX} is the maximum series resistance of the bulk capacitor

The maximum RMS ripple current must also be checked. For worst case conditions, use 方程式 7 to calculate the maximum-RMS input ripple current, $I_{CIN(RMS)}$.

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{2} \quad (7)$$

In this case, the input ripple voltage is 243 mV and the RMS ripple current is 2.5 A.

备注

The actual input voltage ripple is greatly affected by parasitics associated with the layout and the output impedance of the voltage source.

The actual input voltage ripple for this circuit is listed in 表 8-1 and is larger than the calculated value. This measured value is still below the specified input limit of 300 mV. The maximum voltage across the input capacitors is $V_{IN(MAX)} + \Delta V_{IN} / 2$. The selected bulk and bypass capacitors are each rated for 50 V and the ripple current capacity is greater than 3 A, both providing ample margin. The maximum ratings for voltage and current must not be exceeded under any circumstance.

8.2.2.6 Output Filter Components

Two components must be selected for the output filter, L_{OUT} and C_{OUT}. Because the TPS54531 is an externally compensated device, a wide range of filter component types and values can be supported.

8.2.2.6.1 Inductor Selection

To calculate the minimum value of the output inductor, use 方程式 8

$$L_{MIN} = \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times F_{SW}} \quad (8)$$

where

- K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current

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In general, this value is at the discretion of the designer; however, the following guidelines can be used. For designs using low-ESR output capacitors such as ceramics, a value as high as K_{IND} = 0.3 can be used. When using higher ESR output capacitors, K_{IND} = 0.2 yields better results.

For this design example, use K_{IND} = 0.3 and the minimum inductor value is calculated as 4.8 μH. For this design, a close, standard value was chosen: 4.7 μH.

For the output filter inductor, do not exceed the RMS current and saturation current ratings. Use 方程式 9 to calculate the inductor ripple current (I_{RIPPLE}).

$$I_{RIPPLE} = \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times 0.8} \tag{9}$$

Use 方程式 10 to calculate the RMS inductor current.

$$I_{L(RMS)} = \sqrt{I_{OUT(MAX)}^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times 0.8}\right)^2} \tag{10}$$

Use 方程式 11 to calculate the peak inductor current.

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{1.6 \times V_{IN(MAX)} \times L_{OUT} \times F_{SW}} \tag{11}$$

For this design, the RMS inductor current is 5.03 A and the peak inductor current is 5.96 A. The selected inductor is a Wurth 4.7 μH. This inductor has a saturation current rating of 19 A and an RMS current rating of 7 A, which meets these requirements. Smaller or larger inductor values can be used depending on the amount of ripple current the designer wants to allow, so long as the other design requirements are met. Larger value inductors have lower AC current and result in lower output voltage ripple, while smaller inductor values increase AC current and output voltage ripple. In general, inductor values for use with the TPS54531 device are in the range of 1 μH to 47 μH.

8.2.2.6.2 Capacitor Selection

Selecting the value of the output capacitor is based on three primary considerations. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance must be selected based on the more stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor must supply the load with current when the regulator can not. This situation occurs if desired hold-up times occur for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily not able to supply sufficient output current if a large, fast increase occurs in the current needs of the load, such as a transition from no load to full load. The regulator usually requires two or more clock cycles for the control loop to respond to the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of drop in the output voltage. Use 方程式 12 to calculate minimum output capacitance (C_O) required in this case.

$$C_O > \frac{2 \times \Delta I_{OUT}}{F_{SW} \times \Delta V_{OUT}} \tag{12}$$

where

- ΔI_{OUT} is the change in output current
- F_{SW} is the switching frequency of the regulator

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- ΔV_{OUT} is the allowable change in the output voltage

For this example, the transient load response is specified as a 5% change in V_{OUT} for a load step of 2.5 A. For this example, ΔI_{OUT} = 2.5 A and ΔV_{OUT} = 0.05 x 5 = 0.25 V. Using these values results in a minimum capacitance of 35 µF. This value does not consider the ESR of the output capacitor in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Use 方程式 13 to calculate the minimum output capacitance needed to meet the output voltage ripple specification. In this case, the maximum output voltage ripple is 30 mV. Under this requirement 方程式 13, yields 14 µF.

$$C_O > \frac{1}{8 \times F_{SW}} \times \frac{1}{\frac{V_{OUTRIPPLE}}{I_{RIPPLE}}} \tag{13}$$

where

- F_{SW} is the switching frequency
- $V_{OUTRIPPLE}$ is the maximum allowable output voltage ripple
- I_{RIPPLE} is the inductor ripple current

Use 方程式 14 to calculate the maximum ESR an output capacitor can have to meet the output-voltage ripple specification. 方程式 14 indicates the ESR must be less than 15.6 mΩ. In this case, the ESR of the ceramic capacitor is much smaller than 15.6 mΩ.

$$R_{ESR} < \frac{V_{OUTRIPPLE}}{I_{RIPPLE}} \tag{14}$$

Additional capacitance deratings for aging, temperature, and DC bias must be considered which increases this minimum value. For this example, two 47-µF 10-V X5R ceramic capacitors with 3 mΩ of ESR are used. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS (root mean square) value of the maximum ripple current. Use 方程式 15 to calculate the RMS ripple current that the output capacitor must support. For this application, 方程式 15 yields 554 mA.

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT} \right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times N_C} \right) \tag{15}$$

8.2.2.7 Compensation Components

Several possible methods exist to design closed loop compensation for DC/DC converters. For the ideal current mode control, the design equations can be easily simplified. The power stage gain is constant at low frequencies, and rolls off at –20 dB/decade above the modulator pole frequency. The power stage phase is 0 degrees at low frequencies and begins to fall one decade below the modulator pole frequency reaching a minimum of –90 degrees one decade above the modulator pole frequency. Use 方程式 16 to calculate the modulator pole frequency.

$$F_{P_MOD} = \frac{I_{OUT(MAX)}}{2 \times \pi \times V_{OUT} \times C_{OUT}} \tag{16}$$

For the TPS54531 device, most circuits have relatively high amounts of slope compensation. As more slope compensation is applied, the power stage characteristics deviate from the ideal approximations. The phase loss of the power stage now approaches –180 degrees, making compensation more difficult. The power stage transfer function can be solved but requires a tedious calculation. Use the PSpice model to accurately model the power-stage gain and phase so that a reliable compensation circuit can be designed. Alternately, a direct

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measurement of the power stage characteristics can be used. That is the technique used in this design procedure. For this design, the calculate values are as follows:

L1 = 4.7 µH

C8 and C9 = 47 µF (each)

ESR = 3 mΩ

图 8-2 shows the power stage characteristics.

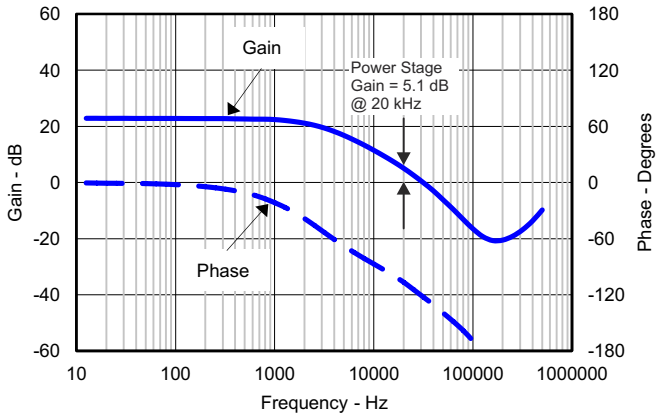


图 8-2. Power Stage Gain and Phase Characteristics

For this design, the intended crossover frequency is 20 kHz. From the power stage gain and phase plots, the gain at 20 kHz is 5.1 dB and the phase is about –100 degrees. For 60 degrees of phase margin, additional phase boost from a feed-forward capacitor in parallel with the upper resistor of the voltage set point divider is not needed. R3 sets the gain of the compensated error amplifier to be equal and opposite the power stage gain at crossover. Use 方程式 17 to calculate the required value of R3.

$$R_3 = \frac{10^{\frac{-G_{PWRSTG}}{20}}}{gm_{EA}} \times \frac{V_{OUT}}{V_{REF}} \tag{17}$$

To maximize phase gain, the compensator zero is placed one decade below the crossover frequency of 20 kHz. Use 方程式 18 to calculate the required value for C6.

$$C_6 = \frac{1}{2 \times \pi \times R_3 \times \frac{F_{CO}}{10}} \tag{18}$$

To maximize phase gain the high frequency pole is placed one decade above the crossover frequency of 20 kHz. The pole can also be useful to offset the ESR of aluminum electrolytic output capacitors. Use 方程式 19 to calculate the value for C7.

$$C_7 = \frac{1}{2 \times \pi \times R_3 \times 10 \times F_{CO}} \tag{19}$$

For this design, the calculated values are as follows:

R3 = 37.4 kΩ

C6 = 2200 pF

C7 = 22 pF

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8.2.2.8 Bootstrap Capacitor

Every TPS54531 design requires a bootstrap capacitor, C4. The bootstrap capacitor value must be 0.1 μF. The bootstrap capacitor is located between the PH and BOOT pins. The bootstrap capacitor must be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

8.2.2.9 Catch Diode

The TPS54531 device sis designed to operate using an external catch diode between the PH and GND pins. The selected diode must meet the absolute maximum ratings for the application. The reverse voltage must be higher than the maximum voltage at the PH pin, which is $V_{IN(MAX)}$ + 0.5 V. Peak current must be greater than $I_{O(MAX)}$ plus on half the peak-to-peak inductor current. The forward-voltage drop must be small for higher efficiencies. The catch diode conduction time is (typically) longer than the high-side FET on time, so attention paid to diode parameters can make a marked improvement in overall efficiency. Additionally, check that the selected device is capable of dissipating the power losses. For this design, a CDBC540-G was selected, with a reverse voltage of 40 V, forward current of 5 A, and a forward-voltage drop of 0.55 V.

8.2.2.10 Slow-Start Capacitor

The slow-start capacitor determines the minimum amount of time required for the output voltage to reach the nominal programmed value during power up which is useful if a load requires a controlled voltage slew rate. The slow-start capacitor is also used if the output capacitance is very large and requires large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor can make the TPS54531 device reach the current limit. Excessive current draw from the input power supply can cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems. Use 方程式 3 to calculate the value of the slow-start capacitor. For the example circuit, the slow-start time is not too critical because the output capacitor value is 2 × 47 μF which does not require much current to charge to 5 V. The example circuit has the slow-start time set to an arbitrary value of 4 ms which requires a 10-nF capacitor. For the TPS54531 device, I_{SS} is 2 μA and V_{ref} is 0.8 V.

8.2.2.11 Output Voltage Limitations

Because of the internal design of the TPS54531 device, any give voltage has both upper and lower output voltage limits for any given input voltage. The upper limit of the output-voltage set point is constrained by the maximum duty cycle of 91% and is calculated with 方程式 20. The equation assumes the maximum ON resistance for the internal high-side FET.

$$V_{O(MAX)} = 0.91 \times \left(\left(V_{IN(MIN)} - I_{O(MAX)} \times R_{DS(ON)MAX}\right) + V_D\right) - \left(I_{O(MAX)} \times R_L\right) - V_D \quad (20)$$

where

- $V_{IN(MIN)}$ = Minimum input voltage
- $I_{O(MAX)}$ = Maximum load current
- V_D = Catch diode forward voltage
- R_L = Output inductor series resistance

The lower limit is constrained by the minimum controllable on time which can be as high as 130 ns. The approximate minimum output voltage for a given input voltage and minimum load current is given by 方程式 21.

$$V_{O(MIN)} = 0.089 \times \left(\left(V_{IN(MAX)} - I_{O(MIN)} \times R_{DS(ON)MIN}\right) + V_D\right) - \left(I_{O(MIN)} \times R_L\right) - V_D \quad (21)$$

where

- $V_{IN(MAX)}$ = Maximum input voltage
- $I_{O(MIN)}$ = Minimum load current
- V_D = Catch diode forward voltage
- R_L = Output inductor series resistance

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This equation assumes nominal on-resistance for the high-side FET and accounts for worst case variation of operating frequency set point. Any design operating near the operational limits of the device must be carefully checked to ensure proper functionality.

8.2.2.12 Power Dissipation Estimate

The following formulas show how to estimate the device power dissipation under continuous-conduction mode (CCM) operations. These formulas must not be used if the device is working in the discontinuous-conduction mode (DCM) or pulse-skipping Eco-mode.

The device power dissipation includes:

1. Conduction loss:

$$Pcon = I_{OUT}^{2} \times R_{DS(on)} \times V_{OUT} / V_{IN}$$

   - where
   - I_{OUT} is the output current (A)
   - $R_{DS(on)}$ is the on-resistance of the high-side MOSFET (Ω)
   - V_{OUT} is the output voltage (V)
   - V_{IN} is the input voltage (V)

2. Switching loss:

$$Psw = 0.5 \times 10^{-9} \times V_{IN}^{2} \times I_{OUT} \times f_{SW}$$

   - where
   - f_{SW} is the switching frequency (Hz)

3. Gate charge loss:

$$Pgc = 22.8 \times 10^{-9} \times f_{SW}$$

4. Quiescent current loss:

$$Pq = 0.11 \times 10^{-3} \times V_{IN}$$

Therefore:

$$Ptot = Pcon + Psw + Pgc + Pq$$

where

- Ptot is the total device power dissipation (W)

For given T_A:

$$T_J = T_A + Rth \times Ptot$$

where

- T_J is the junction temperature (°C)
- T_A is the ambient temperature (°C)
- Rth is the thermal resistance of the package (°C/W)

For given T_{JMAX} = 150°C:

$$T_{AMAX} = T_{JMAX} - Rth \times Ptot$$

where

- T_{JMAX} is maximum junction temperature (°C)
- T_{AMAX} is maximum ambient temperature (°C)

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8.2.3 Application Curves

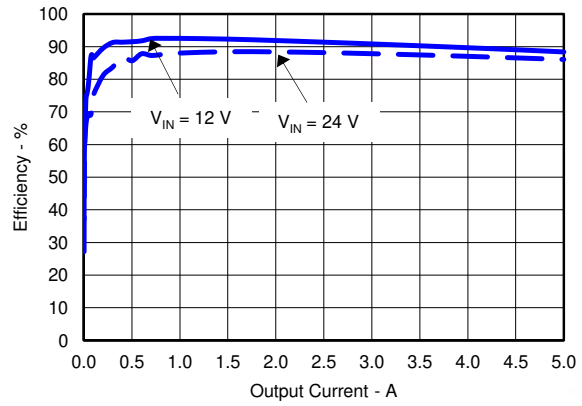


图 8-3. Efficiency

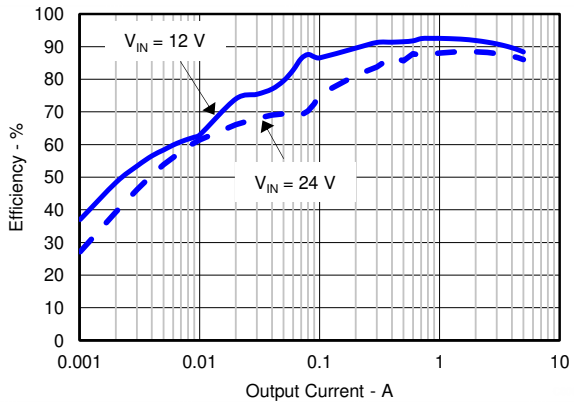


图 8-4. Low-Current Efficiency

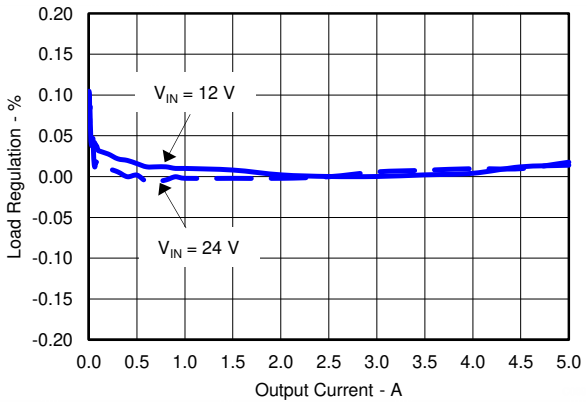


图 8-5. Load Regulation

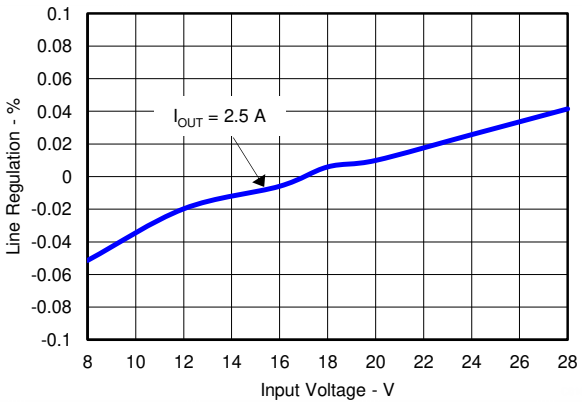


图 8-6. Line Regulation

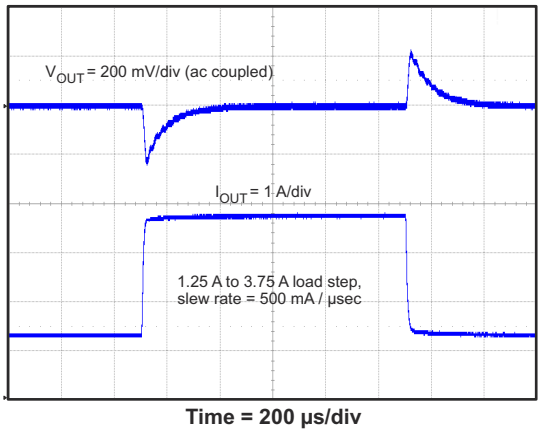


图 8-7. Transient Response

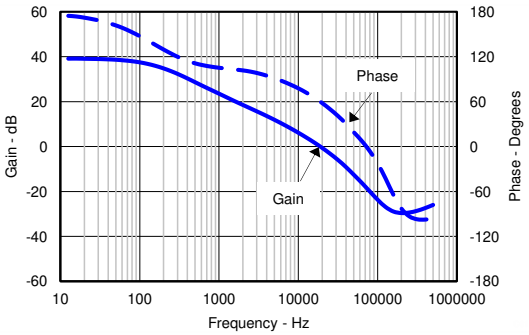


图 8-8. Loop Response

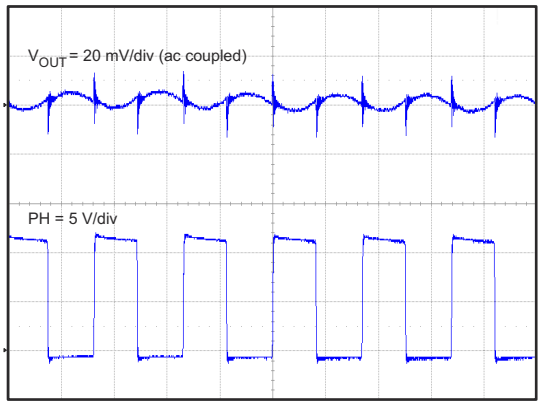


图 8-9. Full-Load Output Ripple

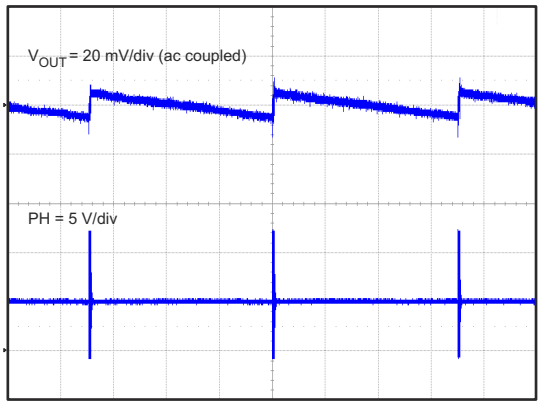


图 8-10. Eco-mode Output Ripple

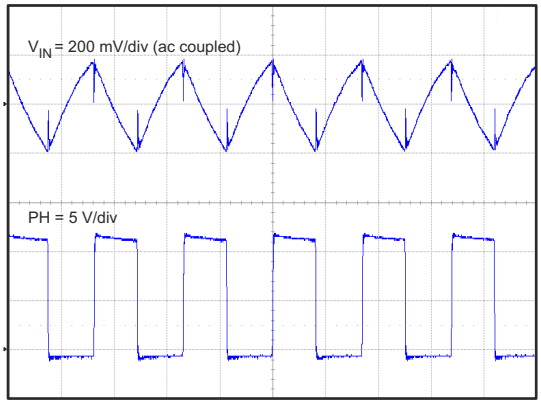


图 8-11. Full-Load Input Ripple

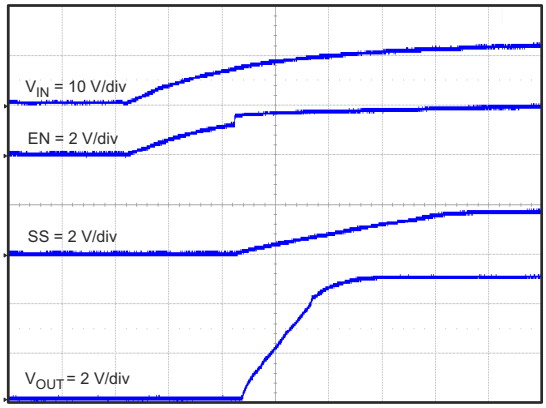


图 8-12. Startup Relative to VIN

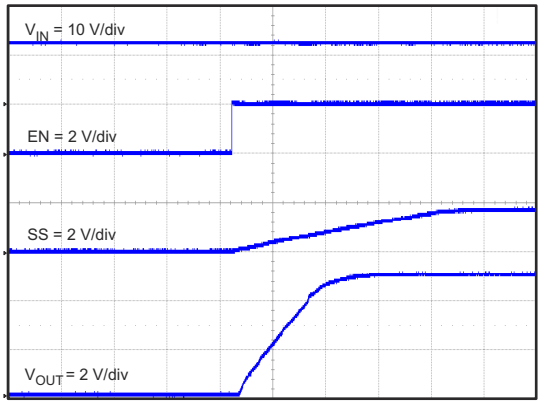


图 8-13. Startup Relative to Enable

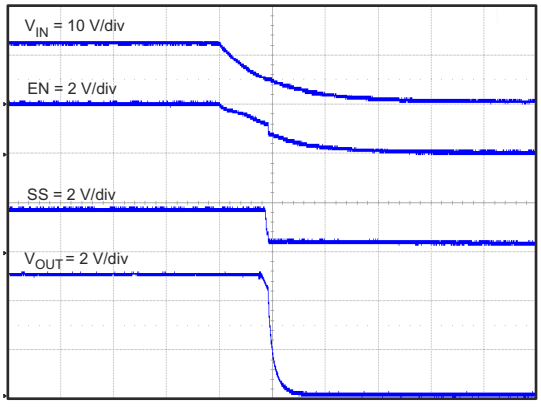


图 8-14. Shut Down Relative to VIN

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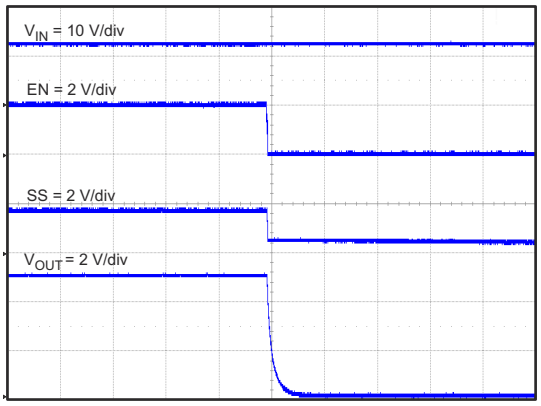


图 8-15. Shut Down Relative to EN

8.3 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range between 3.5 V and 28 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 μF is a typical choice.

8.4 Layout

8.4.1 Layout Guidelines

The VIN pin must be bypassed to ground with a low-ESR ceramic bypass capacitor. Care must be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the anode of the catch diode. The typical recommended bypass capacitance is 10-μF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN pins and the source of the anode of the catch diode. 图 8-16 shows a PCB layout example. The GND pin must be tied to the PCB ground plane at the pin of the device. The PH pin must be routed to the cathode of the catch diode and to the output inductor. Because the PH connection is the switching node, the catch diode and output inductor must be located very close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. For operation at full rated load, the exposed thermal pad must be soldered directly to the top-side ground area under the device. Use thermal vias to connect the top-side ground area to an internal or bottom-layer ground plane. The total copper area must provide adequate heat dissipation. Additional vias adjacent to the device can be used to improve heat transfer to the internal or bottom-layer ground plane . The additional external components can be placed approximately as shown. Obtaining acceptable performance with alternate layout schemes can be possible, however this layout has been shown to produce good results and is intended as a guideline.

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8.4.2 Layout Example

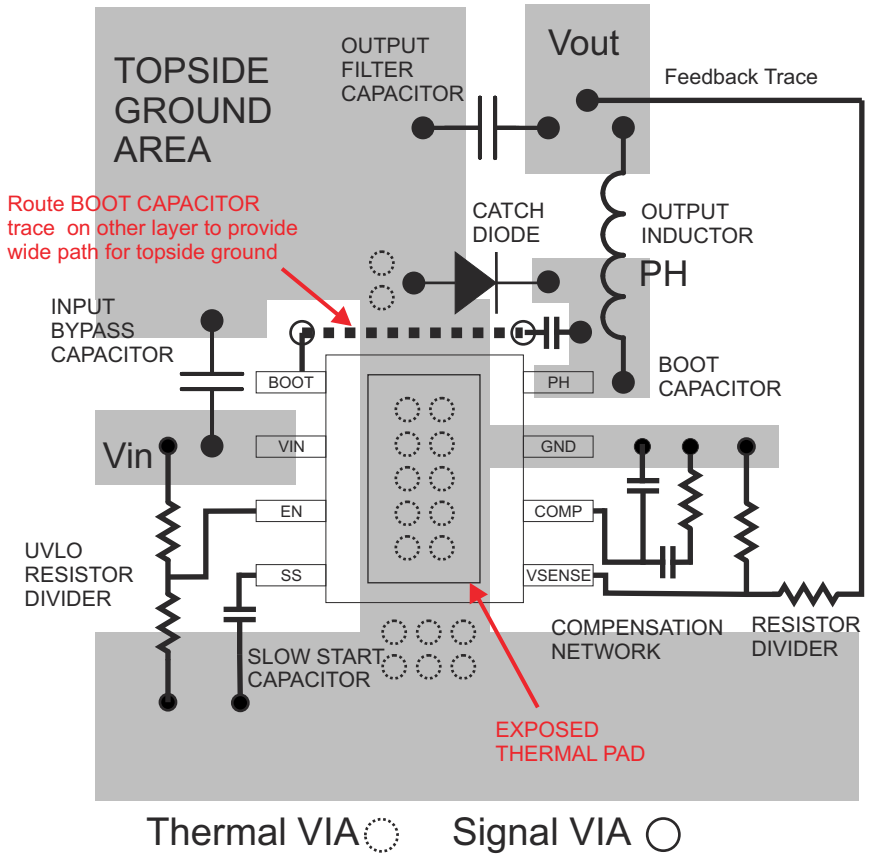


图 8-16. TPS54531DDA Board Layout

8.4.3 Electromagnetic Interference (EMI) Considerations

As EMI becomes a rising concern in more and more applications, the internal design of the TPS54531 device includes features to reduce the EMI. The high-side MOSFET gate drive is designed to reduce the PH pin voltage ringing. The internal IC rails are isolated to decrease the noise sensitivity. A package bond wire scheme is used to lower the parasitics effects.

To achieve the best EMI performance, external component selection and board layout are equally important. Follow the steps listed in the 节 8.2.2 section to prevent potential EMI issues.

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9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 Custom Design With WEBENCH® Tools

Create a custom design with the TPS54531 using the WEBENCH® Power Designer

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer gives a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

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9.3 支持资源

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS54531DDA	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	54531
TPS54531DDA.A	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	54531
TPS54531DDA.B	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	54531
TPS54531DDAR	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	54531
TPS54531DDAR.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	54531
TPS54531DDAR.B	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	54531
TPS54531DDARG4	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	54531
TPS54531DDARG4.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	54531
TPS54531DDARG4.B	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	54531

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

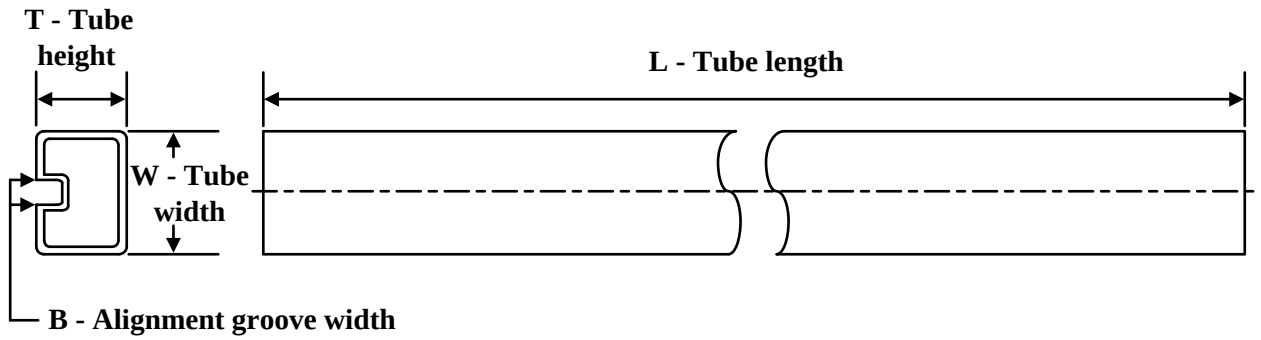
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE

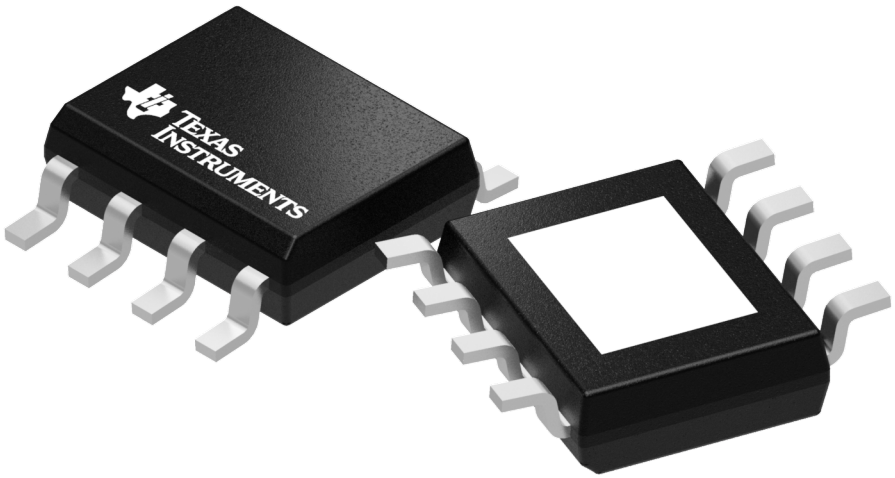


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS54531DDA	DDA	HSOIC	8	75	507	8	3940	4.32
TPS54531DDA	DDA	HSOIC	8	75	517	7.87	635	4.25
TPS54531DDA.A	DDA	HSOIC	8	75	507	8	3940	4.32
TPS54531DDA.A	DDA	HSOIC	8	75	517	7.87	635	4.25
TPS54531DDA.B	DDA	HSOIC	8	75	507	8	3940	4.32
TPS54531DDA.B	DDA	HSOIC	8	75	517	7.87	635	4.25

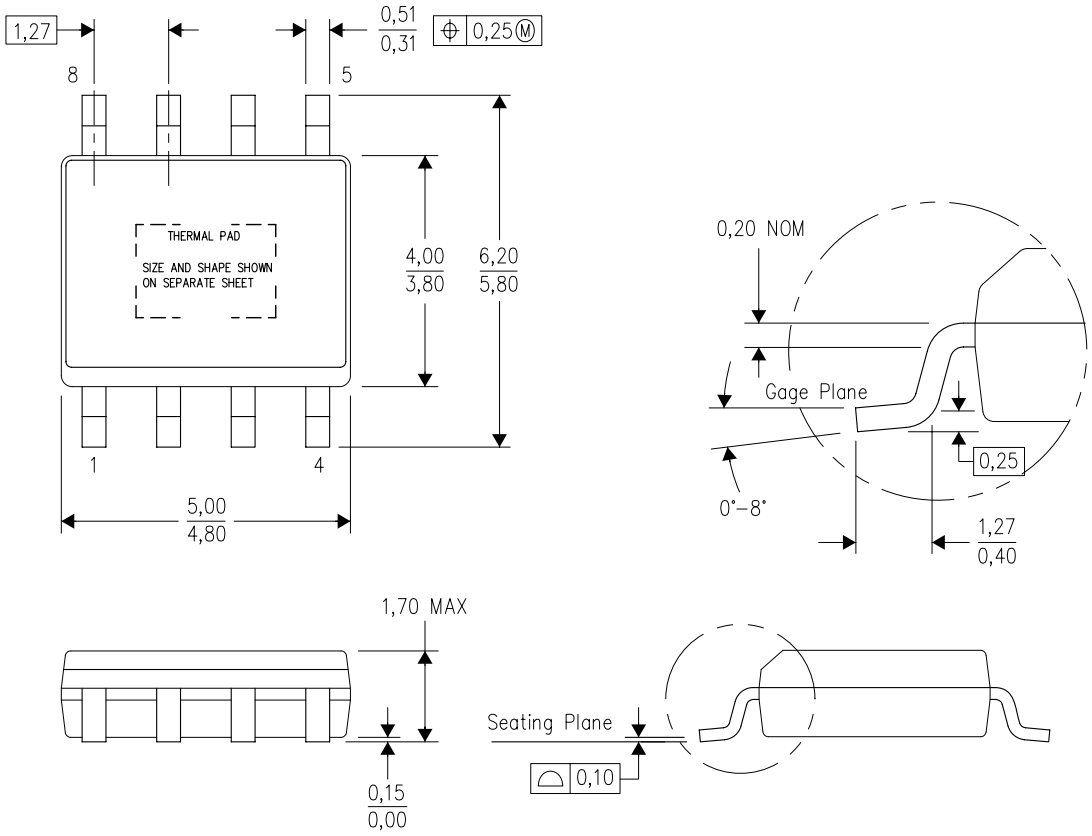
DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

PowerPAD is a trademark of Texas Instruments.

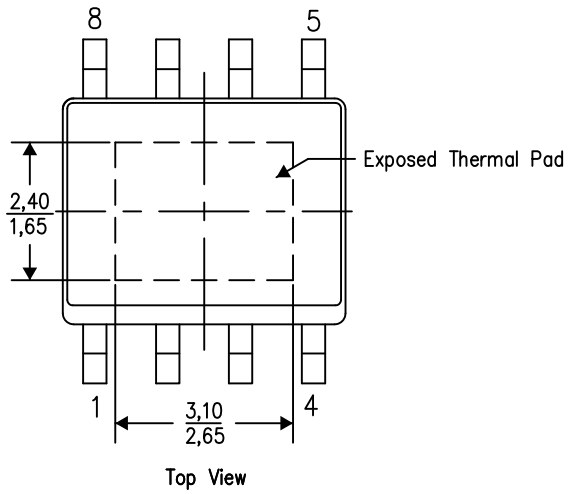
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



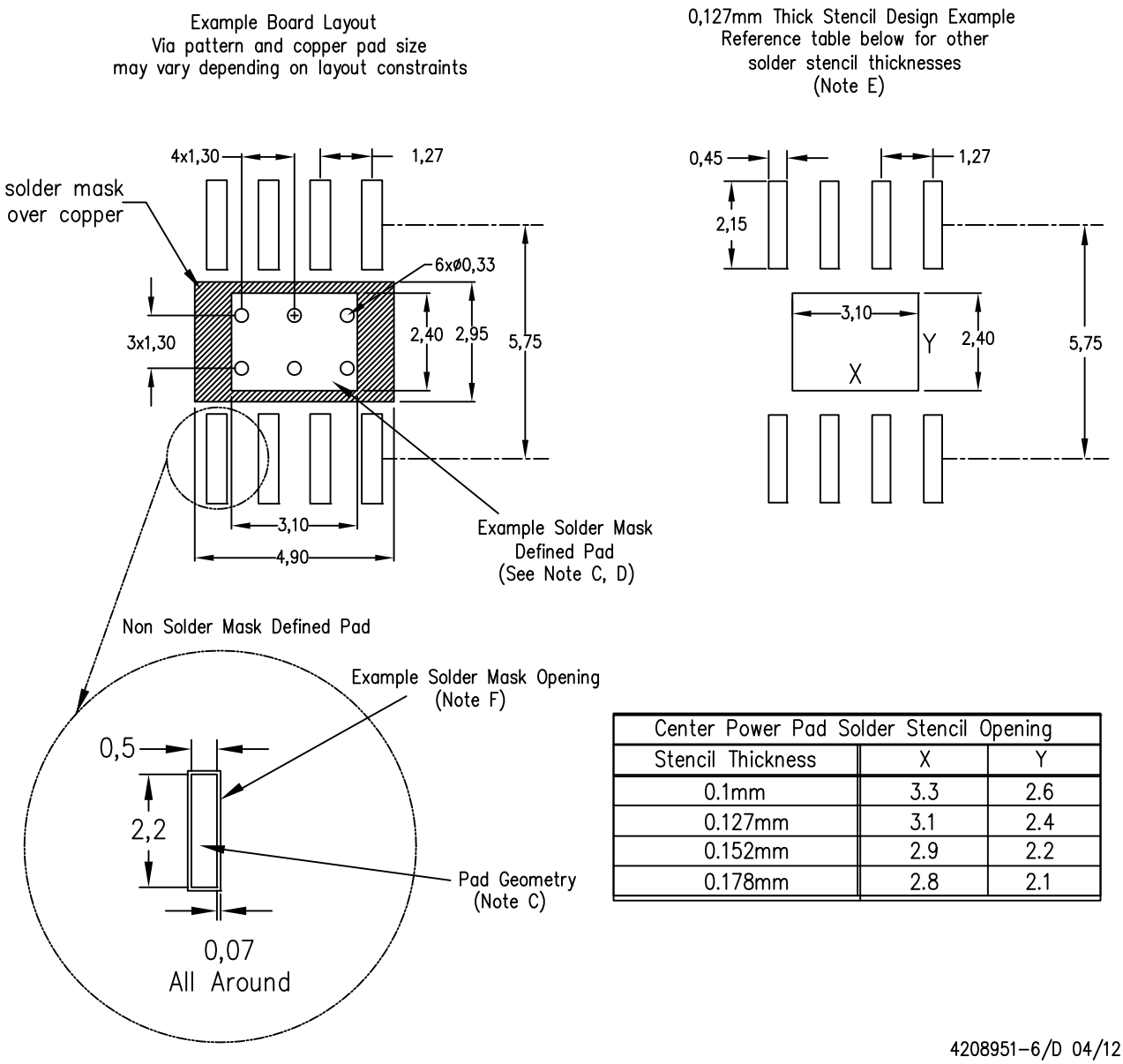
Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

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DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

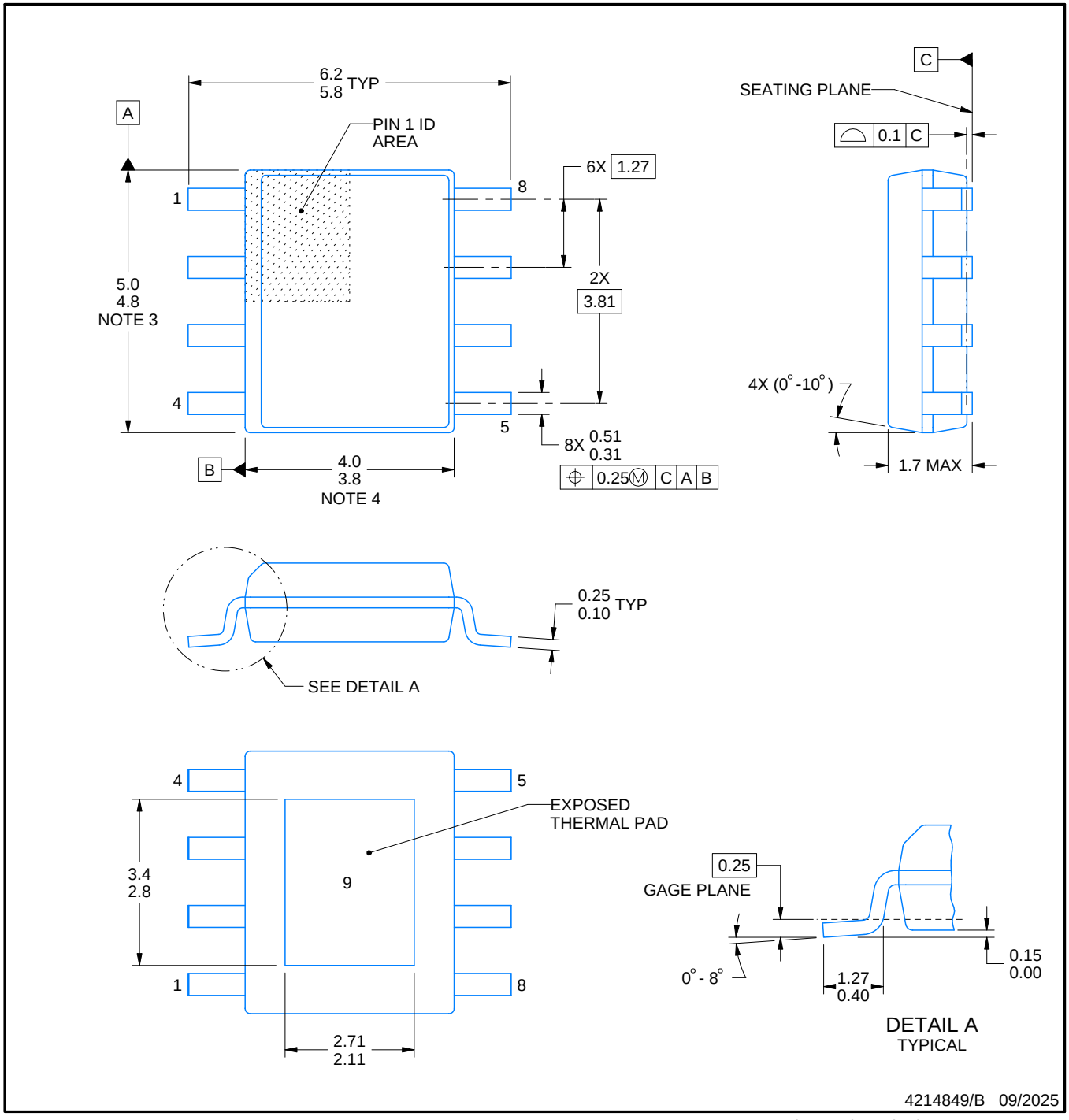
PowerPAD is a trademark of Texas Instruments.

PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

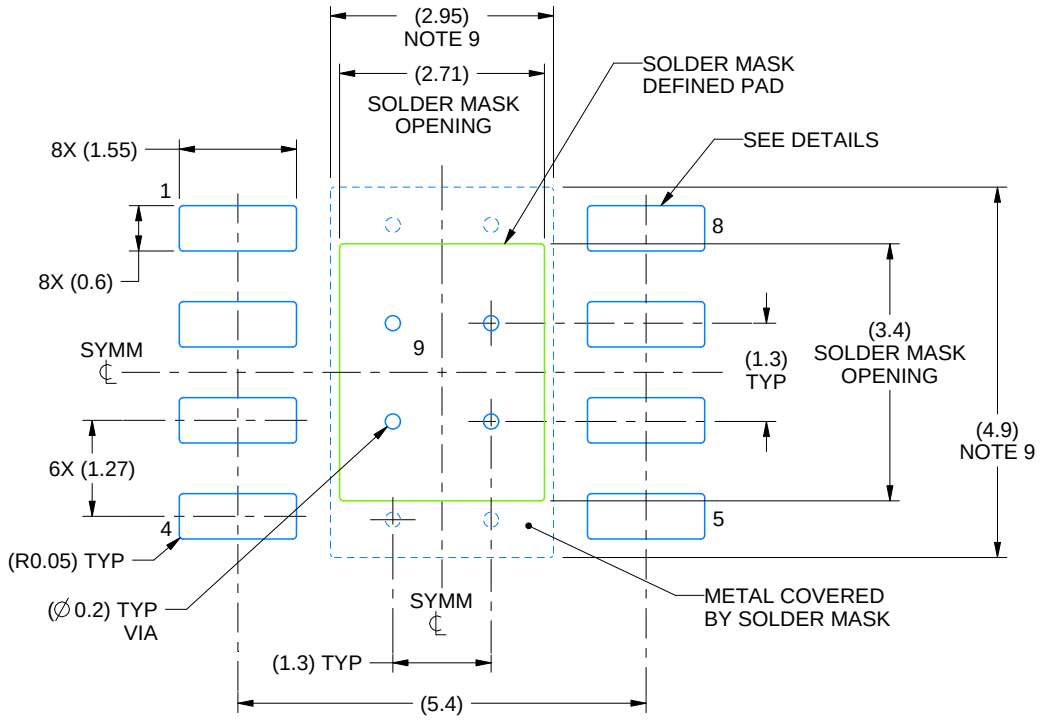
PLASTIC SMALL OUTLINE



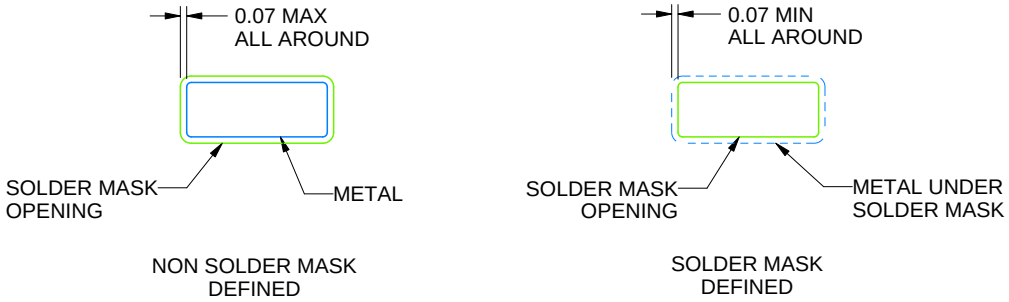
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

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NOTES: (continued)

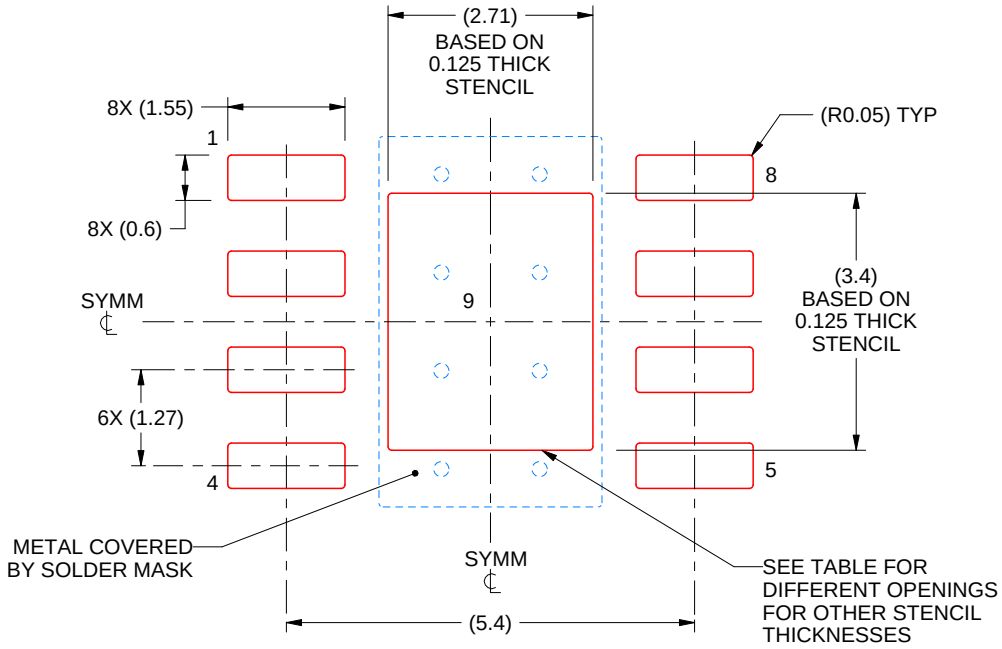
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/B 09/2025

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月