TPS5410 1A 宽输入范围降压转换器

1 特性

- 5.5V 到 36V 的宽输入电压范围
- 高达 1A 的连续（1.2A 峰值）输出电流
- 通过 110mΩ 集成式 MOSFET 开关实现高达 95% 的高效率
- 宽输出电压范围：可调节为低至 1.22V，初始精度为 1.5%
- 内部补偿可最大限度减少外部器件数量
- 适用于小型滤波器尺寸的固定 500kHz 开关频率
- 通过输入电压前馈改进线路稳压和瞬态响应
- 系统受过流限制、过压保护和热关断的保护
- –40°C 至 125°C 的工作结温范围
- 采用小型 8 引脚 SOIC 封装

2 应用

- 消费类：机顶盒、DVD、LCD 显示屏
- 工业用和车载音频电源
- 电池充电器、大功率 LED 电源
- 12V 和 24V 分布式电源系统

3 说明

TPS5410 是一款高输出电流 PWM 转换器，集成了低电阻高侧 N 沟道 MOSFET。具有所列特性的基板上还包括高性能电压误差放大器（可在瞬态条件下提供高稳压精度）、欠压锁定电路（用于防止在输入电压达到 5.5V 前启动）、内部设置的慢启动电路（用于限制浪涌电流）以及电压前馈电路（用于改进瞬态响应）。通过使用 ENA 引脚，关断电源电流通常可减少到 18 µA。其他特性包括高电平有效使能端、过流限制、过压保护和热关断。为降低设计复杂性并减少外部元件数量，TPS5410 反馈环路进行了内部补偿。

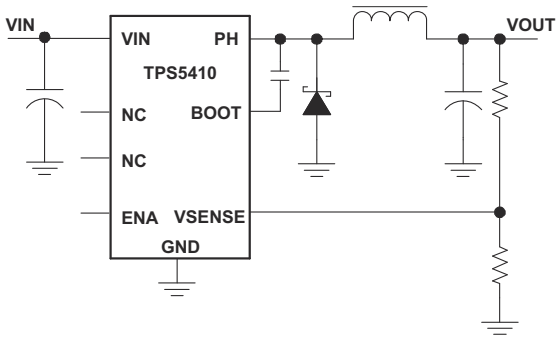
TPS5410 器件采用易于使用的 8 引脚 SOIC 封装。TI 提供评估模块和软件工具，有助于快速实现高性能电源设计，可满足迫切的设备开发周期要求。

封装信息

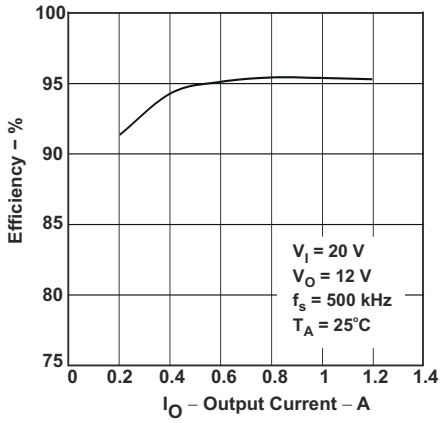
器件型号	封装(1)	封装尺寸(2)
TPS5410	D（SOIC，8）	4.9mm × 6mm

(1) 有关更多信息，请参阅 节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。

Simplified Schematic



Efficiency vs Output Current



本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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4 Pin Configuration and Functions

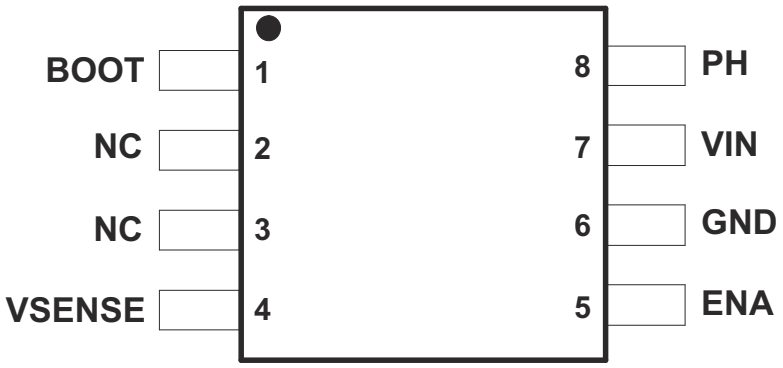


图 4-1. D Package, 8 Pin SOIC Top View

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	O	Boost capacitor for the high-side FET gate driver. Connect 0.01 μF low ESR capacitor from BOOT pin to PH pin.
NC	2, 3	—	Not connected internally.
VSENSE	4	I	Feedback voltage for the regulator. Connect to output voltage divider.
ENA	5	I	On and off control. Below 0.5 V, the device stops switching. Float the pin to enable.
GND	6	—	Ground.
VIN	7	I	Input supply voltage. Bypass VIN pin to GND pin close to device package with a high quality, low ESR ceramic capacitor.
PH	8	O	Source of the high side power MOSFET. Connected to external inductor and diode.

5 Specifications

5.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN(2) to GND	–0.3	40	V
Input voltage	ENA to GND	–0.3	7	V
Input voltage	VSENSE to GND	–0.3	3	V
Output voltage	BOOT to PH	–0.3	6	V
Output voltage	PH to GND, (Steady-state)(2)	–0.6	40	V
Output voltage	PH to GND, (transient < 10ns)	–1.2		V
Source current	PH		Internally Limited	
Source current	PH Leakage current		10	μA
T_J	Operating virtual junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) Approaching the absolute maximum rating for the VIN pin may cause the voltage on the PH pin to exceed the absolute maximum rating.

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5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	Input voltage range	5.5		36	V
T_J	Operating junction temperature	-40		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		TPS5410 D (SOIC) 8 PINs	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (Custom Board)(2)	75	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JESD 51-7)	106	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics*
(2) Refer to the TPS5420's EVM User's Guide for board layout and additional information. For thermal design information please see the Maximum Ambient Temperature section.

5.5 Electrical Characteristics

T_J = –40°C to +125°C, V_{IN} = 5.5 V to 36 V. Typical values are at T_J = 25°C and V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
$I_{Q(VIN)}$	VIN quiescent current	Non-switching, V_{SENSE} = 2 V, PH pin open		2	4.4	mA
$I_{SD(VIN)}$	VIN shutdown supply current	Shutdown, ENA = 0 V		15	50	µA
UVLO						
$VIN_{UVLO(R)}$	VIN UVLO rising threshold	V_{VIN} rising		5.3	5.5	V
$VIN_{UVLO(H)}$	VIN UVLO hysteresis			0.35		V
VOLTAGE REFERENCE						
V_{FB}	FB voltage	T_J = 25°C	1.202	1.221	1.239	V
V_{FB}	FB voltage	T_J = –40°C to 125°C	1.196	1.221	1.245	V
OSCILLATOR						
f_{SW}	Switching frequency		400	500	600	kHz
$t_{ON(min)}$	Minimum ON pulse width			150	200	ns
D_{MAX}	Maximum Duty Cycle	f_{SW} = 500kHz	85%	89%		
ENABLE (ENA PIN)						
$V_{EN(R)}$	ENA voltage rising threshold				1.3	V

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5.5 Electrical Characteristics（续）

T_J = –40°C to +125°C, V_{IN} = 5.5 V to 36 V. Typical values are at T_J = 25°C and V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{EN(F)}$	ENA voltage falling threshold		0.5			V
$V_{EN(H)}$	ENA voltage hysteresis			325		mV
t_{SS}	Internal slow-start time (0~100%)		6.6	8	10	ms
OVERCURRENT PROTECTION						
$I_{HS(OC)}$	High-side peak current limit		1.2	1.55	1.9	A
	Hiccup time before re-start		13	16	20	ms
OUTPUT MOSFET						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	V_{IN} = 12 V, $V_{BOOT-SW}$ = 4.5 V		100	230	mΩ
$R_{DSON(HS)}$	High-side MOSFET on-resistance	V_{IN} = 5.5 V, $V_{BOOT-SW}$ = 4.0 V		125		mΩ
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold (1)	Temperature rising	135	162		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis (1)			14		°C

(1) Parameter specified by design, statistical analysis and production testing of correlated parameters. Not production tested.

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5.6 Typical Characteristics

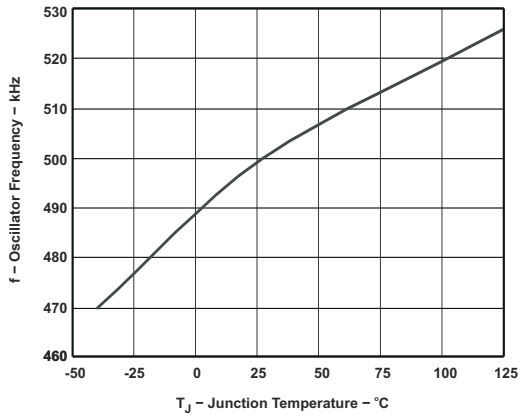


图 5-1. Oscillator Frequency vs Junction Temperature

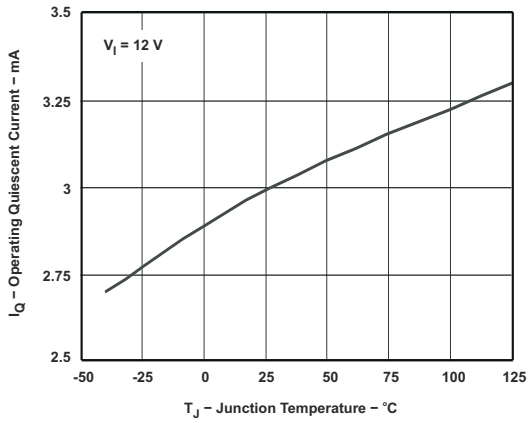


图 5-2. Operating Quiescent Current vs Junction Temperature

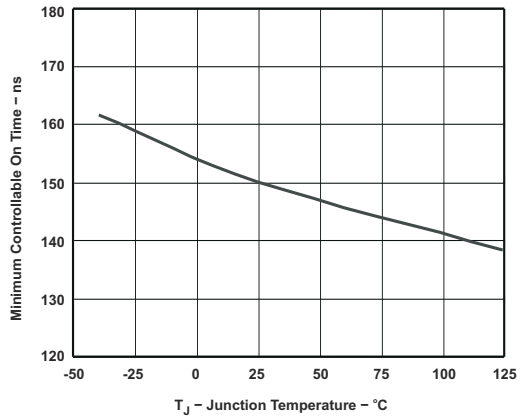


图 5-3. Minimum Controllable On Time vs Junction Temperature

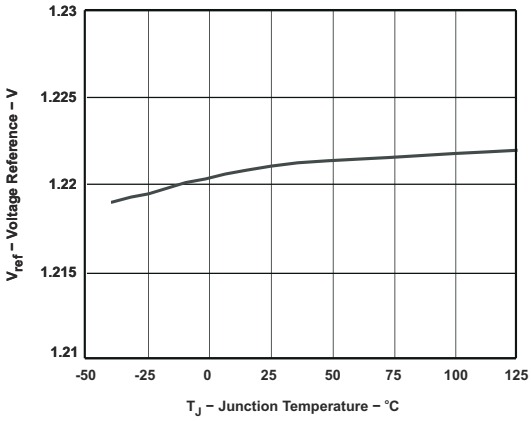


图 5-4. Voltage Reference vs Junction Temperature

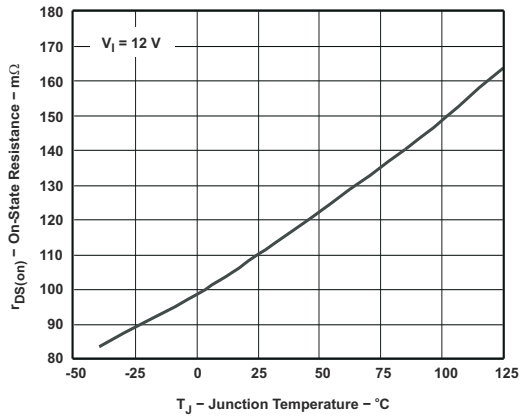


图 5-5. On State Resistance vs Junction Temperature

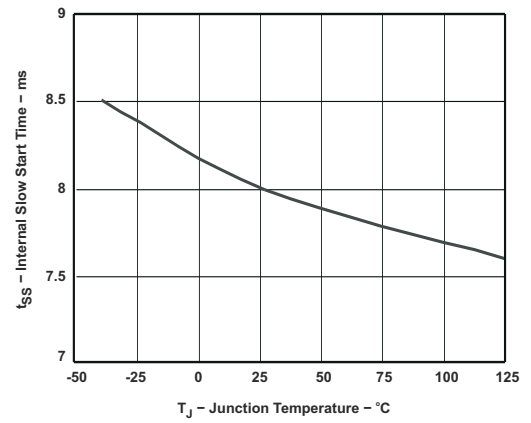


图 5-6. Internal Slow-Start Time vs Junction Temperature

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5.6 Typical Characteristics (continued)

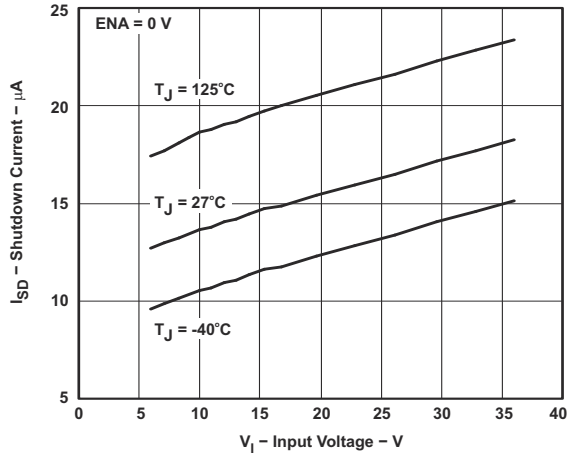


图 5-7. Shutdown Quiescent Current vs Input Voltage

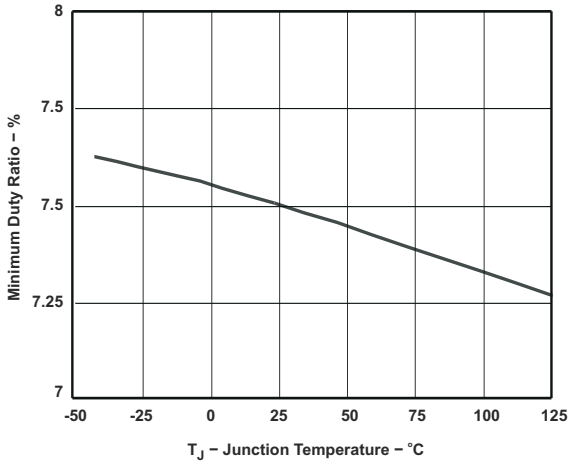


图 5-8. Minimum Controllable Duty Ratio vs Junction Temperature

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6 Detailed Description

6.1 Overview

The TPS5410 is a 36-V, 1-A step-down (buck) regulator with an integrated, high-side, N-channel MOSFET. These devices implement constant-frequency voltage-mode control with voltage feed-forward for improved line regulation and line transient response. Internal compensation reduces design complexity and external component count.

The integrated 110-mΩ high-side MOSFET supports high-efficiency power-supply designs capable of delivering 1-A of continuous current to a load. The gate-drive bias voltage for the integrated high-side MOSFET is supplied by a bootstrap capacitor connected from the BOOT to PH pins. The TPS5410 reduces the external component count by integrating the bootstrap recharge diode.

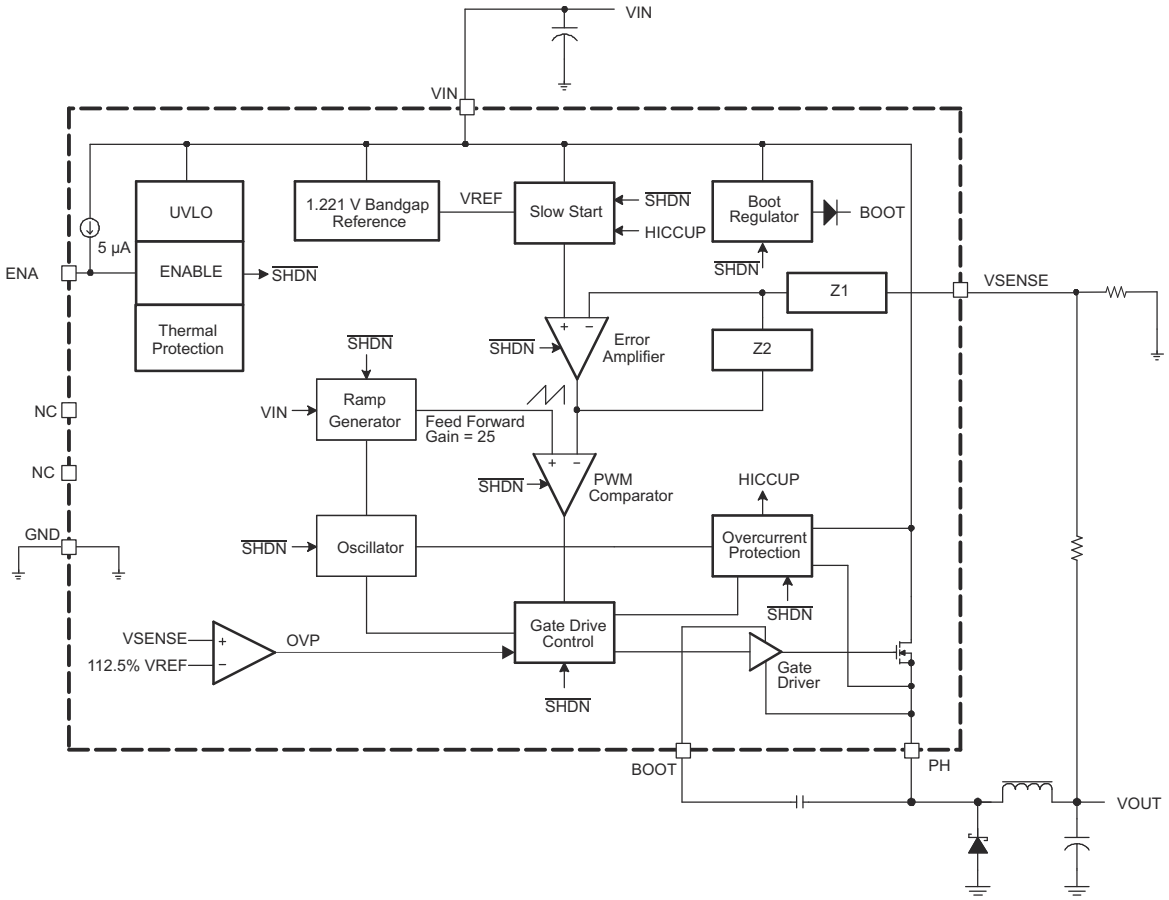
The TPS5410 has a default input start-up voltage of 5.3-V typical. The ENA pin can be used to disable the TPS5410 reducing the supply current to 18 µA. An internal pullup current source enables operation when the ENA pin is floating. The TPS5410 includes an internal slow-start circuit that slows the output rise time during start up to reduce in rush current and output voltage overshoot.

The minimum output voltage is the internal 1.221-V feedback reference. Output overvoltage transients are minimized by an Overvoltage Protection (OVP) comparator. When the OVP comparator is activated, the high-side MOSFET is turned off and remains off until the output voltage is less than 112.5% of the desired output voltage.

Internal cycle-by-cycle overcurrent protection limits the peak current in the integrated high-side MOSFET. For continuous overcurrent fault conditions the TPS5410 enters hiccup mode overcurrent limiting. Thermal protection protects the device from overheating.

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6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Oscillator Frequency

The internal free running oscillator sets the PWM switching frequency at 500 kHz. The 500-kHz switching frequency allows less output inductance for the same output ripple requirement resulting in a smaller output inductor.

6.3.2 Voltage Reference

The voltage reference system produces a precision reference signal by scaling the output of a temperature stable bandgap circuit. The bandgap and scaling circuits are trimmed during production testing to an output of 1.221 V at room temperature.

6.3.3 Enable (ENA) and Internal Slow-Start

The ENA pin provides electrical on/off control of the regulator. After the ENA pin voltage exceeds the threshold voltage, the regulator starts operation and the internal slow-start begins to ramp. If the ENA pin voltage is pulled below the threshold voltage, the regulator stops switching and the internal slow-start resets. Connecting the pin to ground or to any voltage less than 0.5 V disables the regulator and activate the shutdown mode. The quiescent current of the TPS5410 in shutdown mode is typically 18 µA.

The ENA pin has an internal pullup current source, allowing the user to float the ENA pin. If an application requires controlling the ENA pin, use open drain or open collector output logic to interface with the pin. To limit the start-up inrush current, an internal slow-start circuit is used to ramp up the reference voltage from 0 V to its final value linearly. The internal slow-start time is 8 ms typically.

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6.3.4 Undervoltage Lockout (UVLO)

The TPS5410 incorporates an undervoltage lockout circuit to keep the device disabled when VIN (the input voltage) is below the UVLO start voltage threshold. During power up, internal circuits are held inactive and the internal slow-start is grounded until VIN exceeds the UVLO start threshold voltage. After the UVLO start threshold voltage is reached, the internal slow-start is released and device start-up begins. The device operates until VIN falls below the UVLO stop threshold voltage. The typical hysteresis in the UVLO comparator is 330 mV.

6.3.5 Boost Capacitor (BOOT)

Connect a 0.01- μ F low-ESR ceramic capacitor between the BOOT pin and PH pin. This capacitor provides the gate drive voltage for the high-side MOSFET. TI recommends X7R or X5R grade dielectrics due to their stable values over temperature.

6.3.6 Output Feedback (VSENSE)

The output voltage of the regulator is set by feeding back the center point voltage of an external resistor divider network to the VSENSE pin. In steady-state operation, the VSENSE pin voltage must be equal to the voltage reference 1.221 V.

6.3.7 Internal Compensation

The TPS5410 implements internal compensation to simplify the regulator design. Because the TPS5410 uses voltage mode control, a type 3 compensation network has been designed on chip to provide a high crossover frequency and a high phase margin for good stability. See the *节 7.2.1.2.7.2* in the Applications section for more details.

6.3.8 Voltage Feed-Forward

The internal voltage feed-forward provides a constant DC power stage gain despite any variations with the input voltage. This greatly simplifies the stability analysis and improves the transient response. Voltage feed-forward varies the peak ramp voltage inversely with the input voltage so that the modulator and power stage gain are constant at the feed-forward gain, for example:

$$\text{Feed Forward Gain} = \frac{\text{VIN}}{\text{Ramp}_{\text{pk-pk}}} \quad (1)$$

The typical feed-forward gain of TPS5410 is 25.

6.3.9 Pulse-Width-Modulation (PWM) Control

The regulator employs a fixed frequency pulse-width-modulator (PWM) control method. First, the feedback voltage (VSENSE pin voltage) is compared to the constant voltage reference by the high gain error amplifier and compensation network to produce a error voltage. Then, the error voltage is compared to the ramp voltage by the PWM comparator. In this way, the error voltage magnitude is converted to a pulse width which is the duty cycle. Finally, the PWM output is fed into the gate drive circuit to control the on-time of the high-side MOSFET.

6.3.10 Overcurrent Limiting

Overcurrent limiting is implemented by sensing the drain-to-source voltage across the high-side MOSFET. The drain to source voltage is then compared to a voltage level representing the overcurrent threshold limit. If the drain-to-source voltage exceeds the overcurrent threshold limit, the overcurrent indicator is set true. The system ignores the overcurrent indicator for the leading edge blanking time at the beginning of each cycle to avoid any turn-on noise glitches.

After overcurrent indicator is set true, overcurrent limiting is triggered. The high-side MOSFET is turned off for the rest of the cycle after a propagation delay. The overcurrent limiting scheme is called cycle-by-cycle current limiting.

Sometimes under serious overload conditions such as short-circuit, the overcurrent runaway can still happen when using cycle-by-cycle current limiting. A second mode of current limiting is used, for example hiccup mode

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overcurrent limiting. During hiccup mode overcurrent limiting, the voltage reference is grounded and the high-side MOSFET is turned off for the hiccup time. After the hiccup time duration is complete, the regulator restarts under control of the slow-start circuit.

6.3.11 Overvoltage Protection

The TPS5410 has an overvoltage protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions. The OVP circuit includes an overvoltage comparator to compare the VSENSE pin voltage and a threshold of 112.5% × VREF. After the VSENSE pin voltage is higher than the threshold, the high-side MOSFET is forced off. When the VSENSE pin voltage drops lower than the threshold, the high-side MOSFET enables again.

6.3.12 Thermal Shutdown

The TPS5410 protects itself from overheating with an internal thermal shutdown circuit. If the junction temperature exceeds the thermal shutdown trip point, the voltage reference is grounded and the high-side MOSFET is turned off. The part is restarted under control of the slow-start circuit automatically when the junction temperature drops 14°C below the thermal shutdown trip point.

6.4 Device Functional Modes

6.4.1 Minimum Input Voltage

TI recommends the TPS5410 to operate with input voltages above 5.5 V. The typical VIN UVLO threshold is 5.3 V and the device can operate at input voltages down to the UVLO voltage. At input voltages below the actual UVLO voltage the device do not switch. If ENA is floating or externally pulled up to greater up than 1.3 V, when $V_{(VIN)}$ passes the UVLO threshold the TPS5410 becomes active. Switching is enabled and the slow-start sequence is initiated. The TPS5410 starts linearly ramping up the internal reference voltage from 0 V to its final value over the internal slow-start time period.

6.4.2 ENA Control

T The enable start threshold voltage is 1.3 V max. With ENA held below the 0.5 V minimum stop threshold voltage the TPS5410 is disabled and switching is inhibited even if VIN is above its UVLO threshold. The quiescent current is reduced in this state. If the ENA voltage is increased above the max start threshold while $V_{(VIN)}$ is above the UVLO threshold, the device becomes active. Switching is enabled and the slow-start sequence is initiated. The TPS5410 starts linearly ramping up the internal reference voltage from 0 V to its final value over the internal slow-start time period.

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7 Applications and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

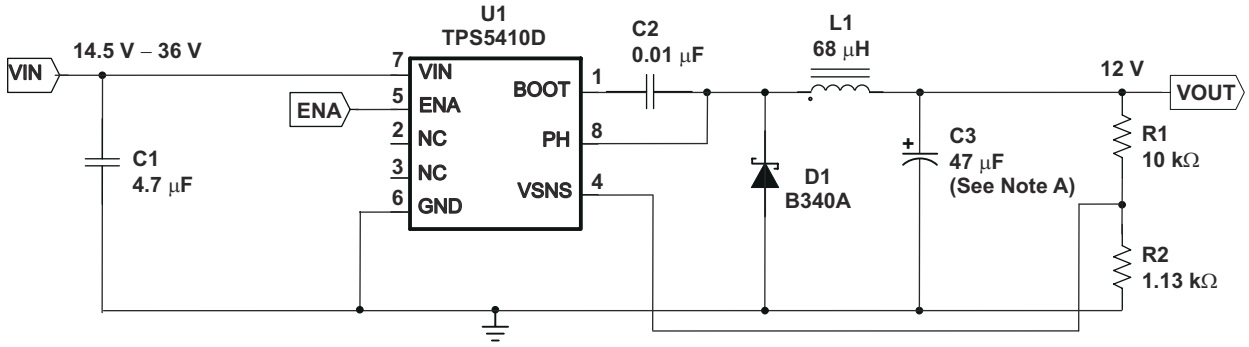
7.1 Application Information

The TPS5410 is a 1-A, step down regulator with an integrated high-side MOSFET. This device is typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 1 A. Example applications are: High Density Point-of-Load Regulators for Set-top Box, DVD, LCD and Plasma Displays, High Power LED Supply, Car Audio, Battery Chargers, and other 12-V and 24-V Distributed Power Systems. Use the following design procedure to select component values for the TPS5410. This procedure illustrates the design of a high frequency switching regulator. Alternatively, use the WEBENCH software to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design.

7.2 Typical Applications

7.2.1 Application Circuit

图 7-1 shows the schematic for a typical TPS5410 application. The TPS5410 can provide up to 1-A output current at a nominal output voltage of 12 V.



A. C3 = Tantalum AVX TPSE476M020R0150

图 7-1. Application Circuit, 14.5 V — 36 V to 12 V

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7.2.1.1 Design Requirements

For this design example, use the following as the input parameters:

表 7-1. Design Requirements

DESIGN PARAMETER(1)	EXAMPLE VALUE
Input voltage range	14.5 V to 36 V
Output voltage	12 V
Input ripple voltage	300 mV
Output ripple voltage	50 mV
Output current rating	1 A
Operating frequency	500 kHz

(1) As an additional constraint, the design is set up to be small size and low component height.

7.2.1.2 Detailed Design Procedure

7.2.1.2.1 Switching Frequency

The switching frequency for the TPS5410 is internally set to 500 kHz. Adjusting the switching frequency is not possible.

7.2.1.2.2 Input Capacitors

The TPS5410 requires an input decoupling capacitor and, depending on the application, a bulk input capacitor. The minimum recommended value for the decoupling capacitor is 4.7 μF. A high quality ceramic type X5R or X7R is required. For some applications, a smaller value decoupling capacitor can be used, if the input voltage and current ripple ratings are not exceeded. The voltage rating must be greater than the maximum input voltage, including ripple. For this design, a 4.7 μF capacitor, C1 issued to allow for smaller 1812 case size to be used while maintaining a 50-V rating.

This input ripple voltage can be approximated by 方程式 2 :

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{SW}} + \left(I_{OUT(MAX)} \times ESR_{MAX}\right) \quad (2)$$

Where $I_{OUT(MAX)}$ is the maximum load current, f_{SW} is the switching frequency, C_I is the input capacitor value and ESR_{MAX} is the maximum series resistance of the input capacitor.

The maximum RMS ripple current also must be checked. For worst case conditions, this is approximated by 方程式 3:

$$I_{CIN} = \frac{I_{OUT(MAX)}}{2} \quad (3)$$

In this example, the calculated input ripple voltage is 137 mV, and the RMS ripple current is 0.5 A. The maximum voltage across the input capacitors is VIN max plus delta VIN/2. The chosen input decoupling capacitors are rated for 50 V, and the ripple current capacity for each is 3 A at 500 kHz, providing ample margin. The actual measured input ripple voltage can be larger than the calculated value due to the output impedance of the input voltage source, decrease in actual capacitance due to bias voltage and parasitics associated with the layout.

> **小心**
>
> The maximum ratings for voltage and current are not to be exceeded under any circumstance.

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Additionally, some bulk capacitance can be needed, especially if the TPS5410 circuit is not located within approximately 2 inches from the input voltage source. The value for this capacitor is not critical but must be rated to handle the maximum input voltage including ripple voltage and must filter the output so that input ripple voltage is acceptable.

7.2.1.2.3 Output Filter Components

Two components must be selected for the output filter, L1 and C3. Because the TPS5410 is an internally compensated device, a limited range of filter component types and values can be supported.

7.2.1.2.3.1 Inductor Selection

To calculate the minimum value of the output inductor, use 方程式 4:

$$L_{MIN} = \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(max)} \times K_{IND} \times I_{OUT} \times F_{SW} \times 0.8} \quad (4)$$

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. Three things must be considered when determining the amount of ripple current in the inductor: the peak to peak ripple current affects the output ripple voltage amplitude, the ripple current affects the peak switch current, and the amount of ripple current determines at what point the circuit becomes discontinuous. For designs using the TPS5410, K_{IND} of 0.2 to 0.3 yields good results. Low output ripple voltages is obtained when paired with the proper output capacitor, the peak switch current is below the current limit set point, and low load currents can be sourced before discontinuous operation.

For this design example, use K_{IND} = 0.3, and the minimum inductor value is 66 μH. The next highest standard value used in this design is 68 μH.

For the output filter inductor, the RMS current and saturation current ratings not being exceeded is important. The RMS inductor current can be found from 方程式 5:

$$I_{L(RMS)} = \sqrt{I^2_{OUT(MAX)} + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times 0.8}\right)^2} \quad (5)$$

and the peak inductor current can be determined using 方程式 6:

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{1.6 \times V_{IN(MAX)} \times L_{OUT} \times F_{SW}} \quad (6)$$

For this design, the RMS inductor current is 1.004 A, and the peak inductor current is 1.147 A. The chosen inductor is a Coilcraft MSS1260-683 type. The nominal inductance is 68 μH. It has a saturation current rating of 2.3 A and a RMS current rating of 2.3 A, which meets the requirements. Inductor values for use with the TPS5410 are in the range of 10 μH to 100 μH.

7.2.1.2.3.2 Capacitor Selection

The important design factors for the output capacitor are dc voltage rating, ripple current rating, and equivalent series resistance (ESR). The dc voltage and ripple current ratings cannot be exceeded. The ESR is important because along with the inductor ripple current it determines the amount of output ripple voltage. The actual value of the output capacitor is not critical, but some practical limits do exist. Consider the relationship between the desired closed loop crossover frequency of the design and LC corner frequency of the output filter. Due to the design of the internal compensation, TI recommends to keep the closed loop crossover frequency in the range

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3 kHz to 30 kHz as this frequency range has adequate phase boost to allow for stable operation. For this design example, the intended closed loop crossover frequency is between 2590 Hz and 24 kHz, and below the ESR zero of the output capacitor. Under these conditions, the closed loop crossover frequency is related to the LC corner frequency as:

$$f_{CO} = \frac{f_{LC}^{2}}{85\ V_{OUT}} \tag{7}$$

and the desired output capacitor value for the output filter to:

$$C_{OUT} = \frac{1}{3357 \times L_{OUT} \times f_{CO} \times V_{OUT}} \tag{8}$$

For a desired crossover of 10 kHz and a 68-μH inductor, the calculated value for the output capacitor is 36.5 μF. The capacitor type must be chosen so that the ESR zero is above the loop crossover. The maximum ESR is:

$$ESR_{MAX} = \frac{1}{2\pi \times C_{OUT} \times f_{CO}} \tag{9}$$

The maximum ESR of the output capacitor also determines the amount of output ripple as specified in the initial design parameters. The output ripple voltage is the inductor ripple current times the ESR of the output filter. Check that the maximum specified ESR as listed in the capacitor data sheet results in an acceptable output ripple voltage:

$$V_{PP}(MAX) = \frac{ESR_{MAX} \times V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{N_C \times V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times 0.8} \tag{10}$$

Where:

ΔV_{PP} is the desired peak-to-peak output ripple.

N_C is the number of parallel output capacitors.

F_{SW} is the switching frequency.

The minimum ESR of the output capacitor must also be considered. For a good phase margin, if the ESR is zero when the ESR is at its minimum, it must not be above the internal compensation poles at 24 kHz and 54 kHz.

The selected output capacitor must also be rated for a voltage greater than the desired output voltage plus one half the ripple voltage. Any derating amount must also be included. The maximum RMS ripple current in the output capacitor is given by 方程式 11:

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left[\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times 0.8 \times N_C}\right] \tag{11}$$

Where:

N_C is the number of output capacitors in parallel.

F_{SW} is the switching frequency.

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For this design example, a single 47-μF output capacitor is chosen for C3. This value is close to the calculated value of 36.5 μF and yields an actual closed loop cross over frequency of 10.05 kHz. The calculated RMS ripple current is 84.9 mA and the maximum ESR required is 339 mΩ. A capacitor that meets these requirements is a AVX TPSE476M020R0150, rated at 20 V with a maximum ESR of 150 mΩ and a ripple current rating of 1.369 A. This capacitor results in a peak-to-peak output ripple of 44 mV using equation 10. An additional small 0.1-μF ceramic bypass capacitor can also used, but is not included in this design.

Other capacitor types can be used with the TPS5410, depending on the needs of the application.

7.2.1.2.4 Output Voltage Setpoint

The output voltage of the TPS5410 is set by a resistor divider (R1 and R2) from the output to the VSENSE pin. Calculate the R2 resistor value for the output voltage of 12 V using 方程式 12:

$$R2 = \frac{R1 \times 1.221}{V_{OUT} - 1.221} \tag{12}$$

For any TPS5410 design, start with an R1 value of 10 kΩ. R2 is then 1.13 kΩ.

7.2.1.2.5 Boot Capacitor

The boot capacitor must be 0.01 μF.

7.2.1.2.6 Catch Diode

The TPS5410 is designed to operate using an external catch diode between PH and GND. The selected diode must meet the absolute maximum ratings for the application: Reverse voltage must be higher than the maximum voltage at the PH pin, which is VINMAX + 0.5 V. Peak current must be greater than IOUTMAX plus on half the peak-to-peak inductor current. Forward voltage drop must be small for higher efficiencies. It is important to note that the catch diode conduction time is typically longer than the high-side FET on time; therefore, the diode parameters improve the overall efficiency. Additionally, check that the device chosen is capable of dissipating the power losses. For this design, a Diodes, Inc. B340A is chosen, with a reverse voltage of 40 V, forward current of 3 A, and a forward voltage drop of 0.5 V.

7.2.1.2.7 Advanced Information

7.2.1.2.7.1 Output Voltage Limitations

Due to the internal design of the TPS5410, there are both upper and lower output voltage limits for any given input voltage. The upper limit of the output voltage set point is constrained by the maximum duty cycle of 87% and is given by:

$$V_{OUTMAX} = 0.87 \times \left(\left(V_{INMIN} - I_{OMAX} \times 0.230\right) + V_D\right) - \left(I_{OMAX} \times R_L\right) - V_D \tag{13}$$

Where:

V_{INMIN} = minimum input voltage

I_{OMAX} = maximum load current

V_D = catch diode forward voltage.

R_L = output inductor series resistance.

This equation assumes maximum on resistance for the internal high side FET.

The lower limit is constrained by the minimum controllable on time which can be as high as 200 ns. The approximate minimum output voltage for a given input voltage and minimum load current is given by:

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$$V_{OUTMIN} = 0.12 \times \left(\left(V_{INMAX} - I_{OMIN} \times 0.110\right) + V_D\right) - \left(I_{OMIN} \times R_L\right) - V_D \quad (14)$$

Where:

V_{INMAX} = maximum input voltage

I_{OMIN} = minimum load current

V_D = catch diode forward voltage.

R_L= output inductor series resistance.

This equation assumes nominal on resistance for the high side FET and accounts for worst case variation of operating frequency set point. Any design operating near the operational limits of the device must be checked to assure proper functionality.

7.2.1.2.7.2 Internal Compensation Network

The design equations given in the example circuit can be used to generate circuits using the TPS5410. These designs are based on certain assumptions, and always select output capacitors within a limited range of ESR values. If a different capacitor type is desired, it can be possible to fit one to the internal compensation of the TPS5410. 方程式 15 gives the nominal frequency response of the internal voltage-mode type III compensation network:

$$H(s) = \frac{\left(1 + \frac{s}{2\pi \times Fz1}\right) \times \left(1 + \frac{s}{2\pi \times Fz2}\right)}{\left(\frac{s}{2\pi \times Fp0}\right) \times \left(1 + \frac{s}{2\pi \times Fp1}\right) \times \left(1 + \frac{s}{2\pi \times Fp2}\right) \times \left(1 + \frac{s}{2\pi \times Fp3}\right)} \quad (15)$$

Where

Fp0 = 2165 Hz, Fz1 = 2170 Hz, Fz2 = 2590 Hz

Fp1 = 24 kHz, Fp2 = 54 kHz, Fp3 = 440 kHz

Fp3 represents the non-ideal parasitics effect.

Using this information along with the desired output voltage, feed-forward gain and output filter characteristics, the closed loop transfer function can be derived.

7.2.1.2.7.3 Thermal Calculations

The following formulas show how to estimate the device power dissipation under continuous conduction mode operations. Do not use the formulas if the device is working at light loads in the discontinuous conduction mode.

Conduction Loss: $P_{con} = I_{OUT}^2 \times R_{ds(on)} \times V_{OUT} / V_{IN}$

Switching Loss: $P_{sw} = V_{IN} \times I_{OUT} \times 0.01$

Quiescent Current Loss: $P_q = V_{IN} \times 0.01$

Total Loss: $P_{tot} = P_{con} + P_{sw} + P_q$

Given T_A => Estimated Junction Temperature: $T_J = T_A + R_{th} \times P_{tot}$

Given T_{JMAX} = 125°C => Estimated Maximum Ambient Temperature: $T_{AMAX} = T_{JMAX} - R_{th} \times P_{tot}$

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7.2.1.3 Application Curves

The performance graphs in 图 7-2 to 图 7-9 are applicable to the circuit in 图 7-1. T_A = 25 °C. unless otherwise specified.

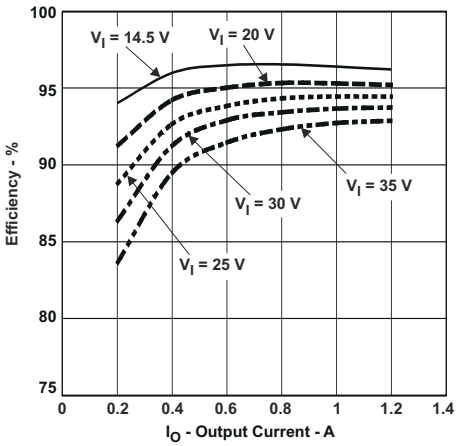


图 7-2. Efficiency vs Output Current

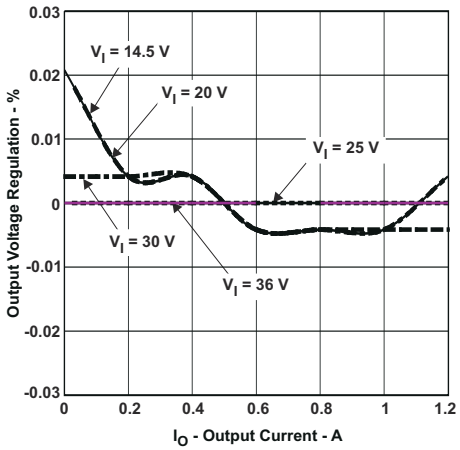


图 7-3. Output Voltage Regulation % vs Output Current

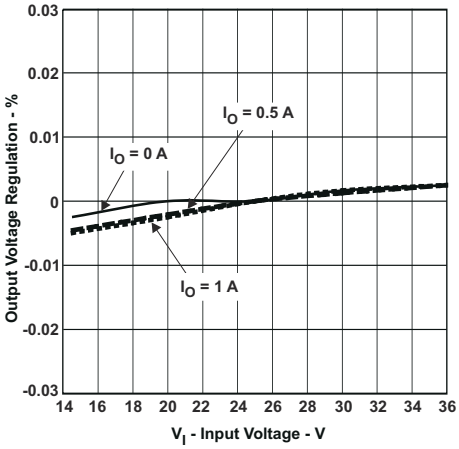


图 7-4. Output Voltage Regulation % vs Input Voltage

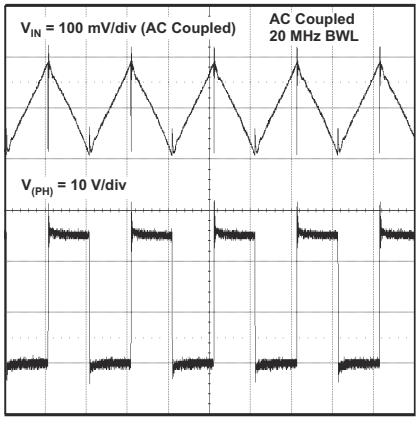


图 7-5. Input Voltage Ripple and PH Node, I_O = 1 A

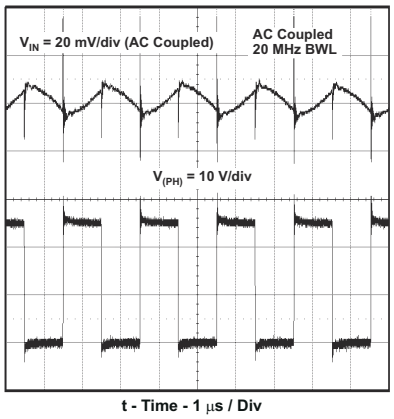


图 7-6. Output Voltage Ripple and PH Node, I_O = 1 A

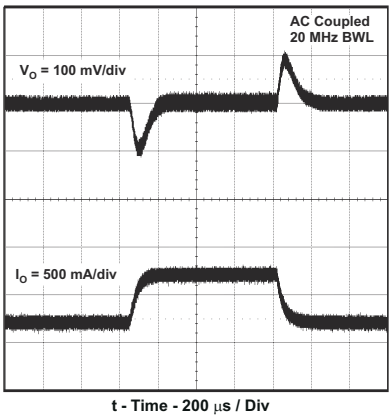


图 7-7. Transient Response, I_O Step 0.25 to 0.75 A

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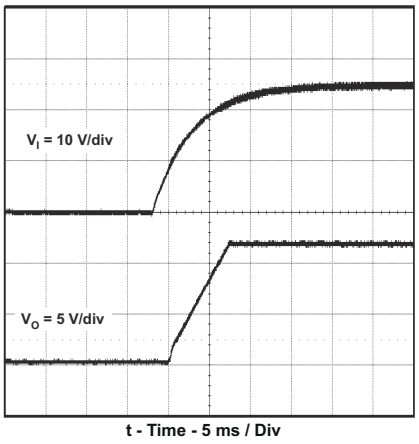


图 7-8. Start-up Waveform, V_I and V_O

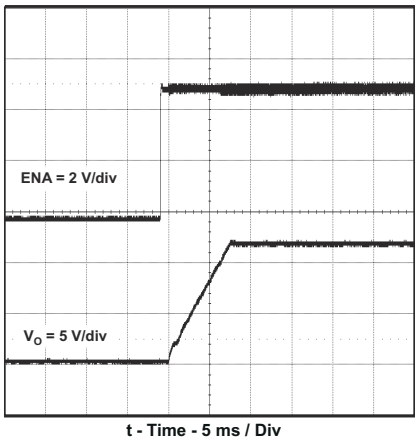
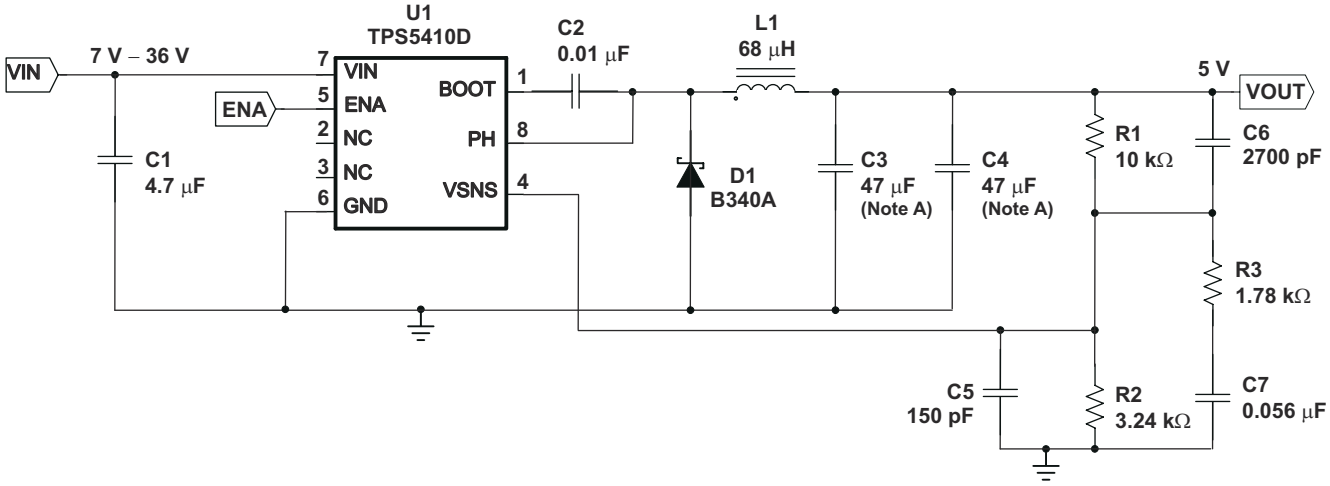


图 7-9. Start-up Waveform, ENA and V_O

7.2.2 Using All Ceramic Capacitors

图 7-10 shows an application circuit using all ceramic capacitors for the input and output filters. The design procedure is similar to those given for the design example, except for the selection of the output filter capacitor values and the design of the additional compensation components required to stabilize the circuit.



A. C3, C4 = Ceramic TDKC4532X5R1A476MT

图 7-10. 7-V — 36-V Input to 5-V Output Application Circuit with Ceramic Capacitors

7.2.2.1 Design Requirements

For this design example, use 表 7-1 as the input parameters.

7.2.2.2 Detailed Design Procedure

7.2.2.2.1 Output Filter Capacitor Selection

When using ceramic output filer capacitors, the recommended LC resonant frequency must be no more than 7 kHz. Because the output inductor is already selected at 68 µH, this limits the minimum output capacitor value to:

$$C_O\,(MIN) \geq \frac{1}{(2\pi \times 7000)^2 \times L_O} \tag{16}$$

The minimum capacitor value is calculated to be 7.6 µF. For this circuit a larger value of capacitor yields better transient response. Two output capacitors are used for C3 and C4 with a value of 47 uF each. Note that the actual capacitance of ceramic capacitors decreases with applied voltage. In this case the effective value used for the calculations is approximately 70 % of the rated value or 70 µF.

7.2.2.2.2 External Compensation Network

When using ceramic output capacitors, additional circuitry is required to stabilize the closed loop system. For this circuit the external components are R3, C5, C6 and C7. To determine the value of these components, first calculate the LC resonant frequency of the output filter:

$$F_{LC} = \frac{1}{2\pi \sqrt{L_O \times C_O\,(EFF)}} \tag{17}$$

For this example the effective resonant frequency is calculated as 2306 Hz

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The network composed of R1, R2, R3, C5, C6 and C7 has two poles and two zeros that are used to tailor the overall response of the feedback network to accommodate the use of the ceramic output capacitors. The pole and zero locations are given by the following equations:

$$Fp1 = 500000 \times \frac{V_O}{F_{LC}} \quad (18)$$

$$Fz1 = 0.7 \times F_{LC} \quad (19)$$

$$Fz2 = 2.5 \times F_{LC} \quad (20)$$

The final pole is located at a frequency too high to be of concern. The values for R1 and R2 are fixed by the 5-V output voltage as calculated using 方程式 12. Now the values of R3, C5, C6 and C7 are determined using 方程式 21, 方程式 22, and 方程式 23:

$$C7 = \frac{1}{2\pi \times Fp1 \times (R1 \parallel R2)} \quad (21)$$

$$R3 = \frac{1}{2\pi \times Fz1 \times C7} \quad (22)$$

$$C6 = \frac{1}{2\pi \times Fz2 \times R1} \quad (23)$$

For this design, using the closest standard values, C7 is 0.056 μF, R3 is 1.76 kΩ and C6 is 2700 pF. C5 is added to improve load regulation performance. C5 is effectively in parallel with C6 in the location of the second pole frequency, so it must be small in relationship to C6. C5 must be less the 1/10 the value of C6. For this example, 150 pF works well.

For additional information on external compensation of the TPS5410 or other wide voltage range devices, see *Using TPS5410/20/30/31/50 With Aluminum/Ceramic Output Capacitors* application report.

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7.2.2.3 Application Curves

The performance graphs in 图 7-11 to 图 7-16 are applicable to the circuit in 图 7-10. T_A = 25 °C. unless otherwise specified.

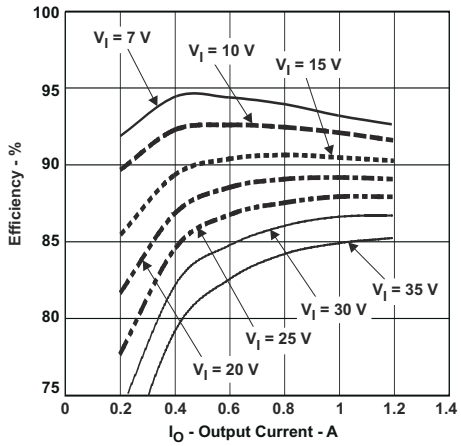


图 7-11. Efficiency vs Output Current

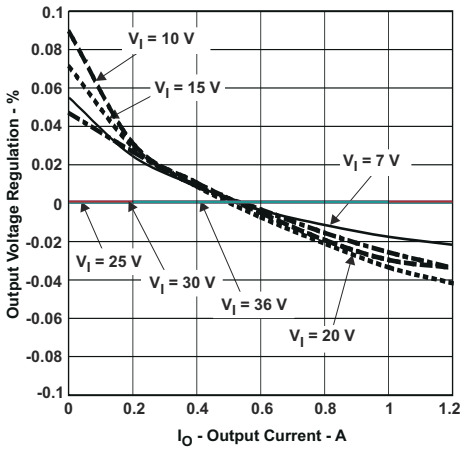


图 7-12. Output Voltage Regulation % vs Output Current

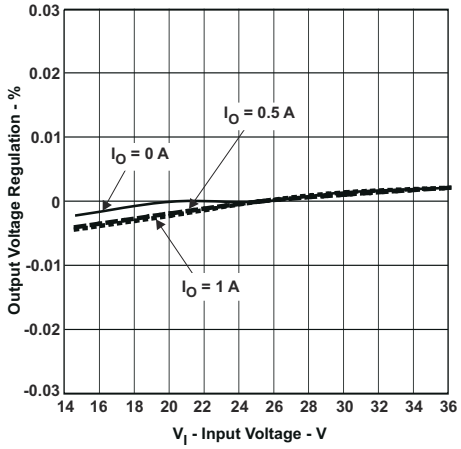


图 7-13. Output Voltage Regulation % vs Input Voltage

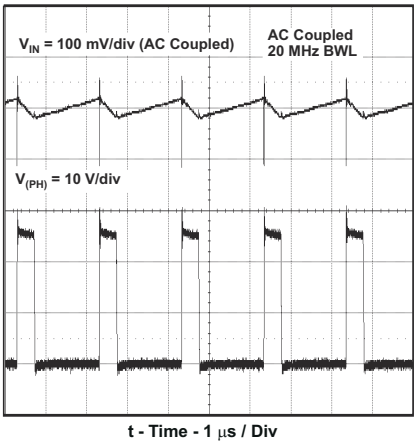


图 7-14. Input Voltage Ripple and PH Node, I_O = 1 A

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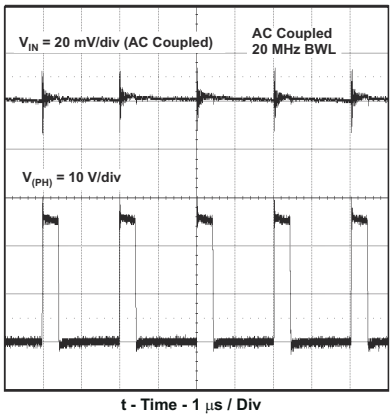


图 7-15. Output Voltage Ripple and PH Node, I_O = 1 A

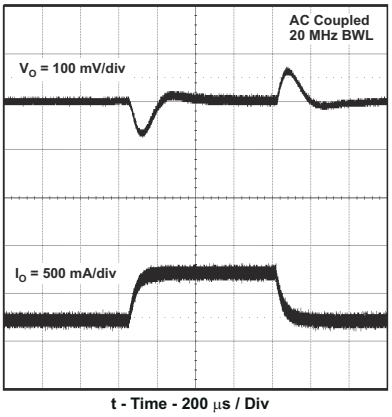


图 7-16. Transient Response, I_O Step 0.25 to 0.75 A

7.3 Power Supply Recommendations

The TPS5410 is designed to operate from an input voltage supply range between 5.5 V and 36 V. This input supply must remain within the input voltage supply range. If the input supply is located more than a few inches from the TPS5410 converter bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 µF is a typical choice.

7.4 Layout

7.4.1 Layout Guidelines

Connect a low ESR ceramic bypass capacitor to the VIN pin. Care must be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the TPS5410 ground pin. The best way to do this is to extend the top side ground area from under the device adjacent to the VIN trace, and place the bypass capacitor as close as possible to the VIN pin. The minimum recommended bypass capacitance is 4.7 µF ceramic with a X5R or X7R dielectric.

There must be a ground area on the top layer directly underneath the IC to connect the GND pin of the device and the anode of the catch diode. Tie the GND pin to the PCB ground by connecting it to the ground area under the device as shown in 图 7-17.

Route the PH pin to the output inductor, catch diode and boot capacitor. Because the PH connection is the switching node, the inductor must be located close to the PH pin, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The catch diode must also be placed close to the device to minimize the output current loop area. Connect the boot capacitor between the phase node and the BOOT pin as shown. Keep the boot capacitor close to the IC and minimize the conductor trace lengths. The component placements and connections shown work well, but other connection routings can also be effective.

Connect the output filter capacitors as shown between the VOUT trace and GND. Keep the loop formed by the PH pin, Lout, Cout and GND as small as is practical.

Connect the VOUT trace to the VSENSE pin using the resistor divider network to set the output voltage. Do not route this trace too close to the PH trace. Due to the size of the IC package and the device pinout, the trace can must be routed under the output capacitor. The routing can be done on an alternate layer if a trace under the output capacitor is not desired.

If the grounding scheme shown is used through a connection to a different layer to route to the ENA pin.

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7.4.2 Layout Example

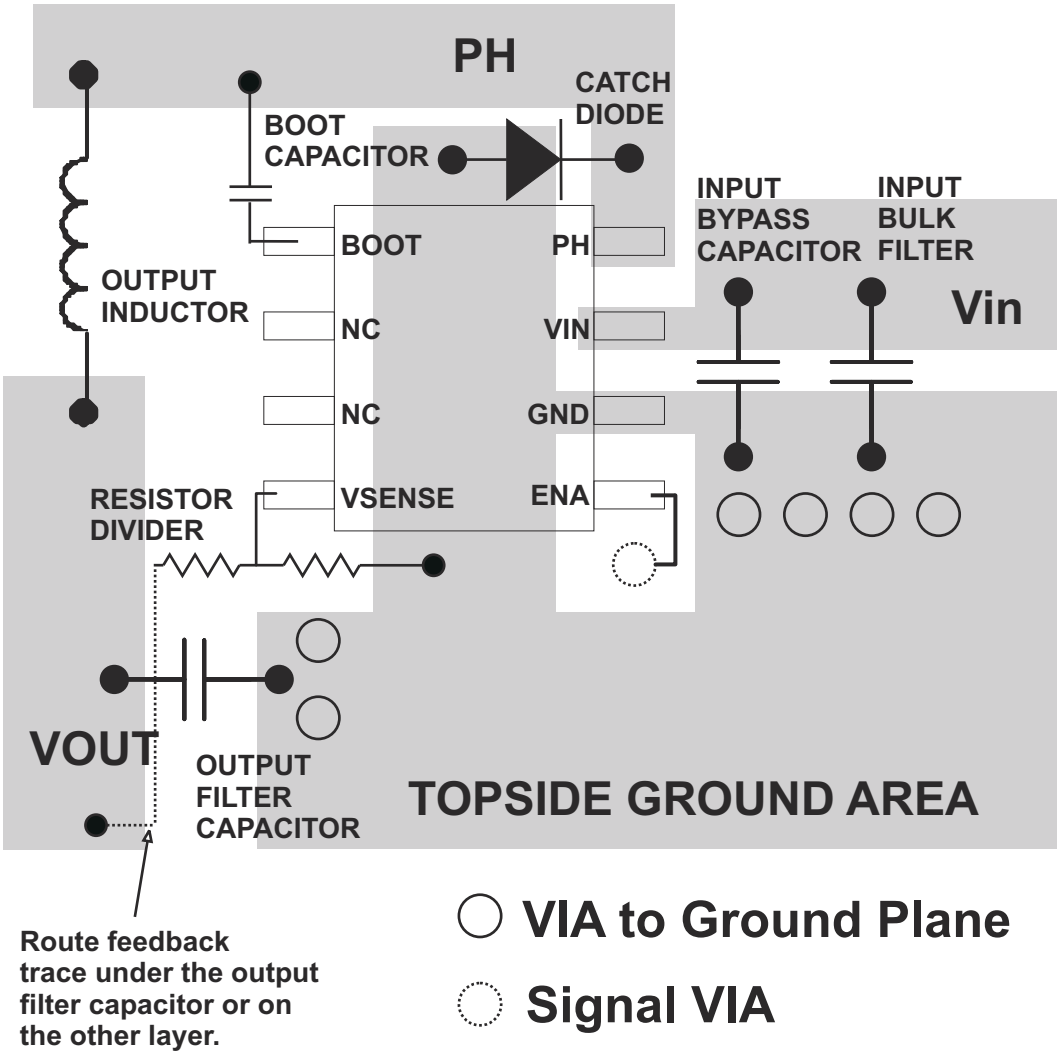


图 7-17. Design Layout

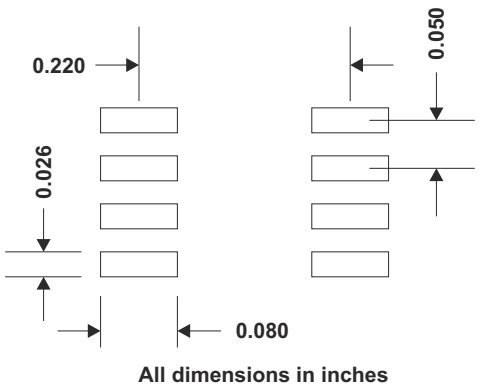


图 7-18. TPS5410 Land Pattern

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8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

Texas Instruments, *Using TPS5410/20/30/31/50 With Aluminum/Ceramic Output Capacitors* application report

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.4 Trademarks

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8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (November 2014) to Revision E (January 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• Updated to new format which does not include specific parameter names and does include min and max columns; TJ called out in header Pin names are used rather than signal names; BOOT and PH voltages now marked as output voltage; Footnotes updated and Note 2 removed	3
• Changed BOOT to PH Absolute Maximum to 6 V maximum	3
• Changed CDM ESD to ±750 V	4
• Added Recommended operating V_I input voltage	4
• Updated footnotes to match current TI standards, replaced custom board specifications with EVM information and JEDEC standard information	4
• Changed $R_{\theta JC(top)}$, $R_{\theta JB}$, ψ_{JT}, ψ_{JB}	4
• Added condition for typical specifications EC table’s header, added parameter names, and used pin names in parameter descriptions. Footnote added	4
• Updated the following test conditions: V_{FB}, D_{MAX}, and $R_{DSON(HS)}$	4
• Updated the following typical specifications in the EC table: $I_{Q(VIN)}$, $I_{SD(VIN)}$, $VIN_{UVLO(H)}$, $V_{EN(H)}$, and $R_{DSON(HS)}$	4
• Updated typical and maximum ISH(OC) in the EC table	4

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Changes from Revision C (September 2013) to Revision D (November 2014)	Page
• 添加了“ESD 等级”表、“特性说明”部分、“器件功能模式”、“应用和实施”部分、“电源相关建议”部分、“布局”部分、“器件和文档支持”部分以及“机械、封装和可订购信息”部分	1

Changes from Revision B (January 2013) to Revision C (September 2013)	Page
• 从数据表标题、特性和说明中删除了 SWIFT	1
• Updated the following test conditions: V_{FB}, D_{MAX}, and $R_{DSON(HS)}$	4

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS5410D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(5410, TPS5410)
TPS5410D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(5410, TPS5410)
TPS5410DG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(5410, TPS5410)
TPS5410DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(5410, TPS5410)
TPS5410DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(5410, TPS5410)
TPS5410DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(5410, TPS5410)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS5410 :

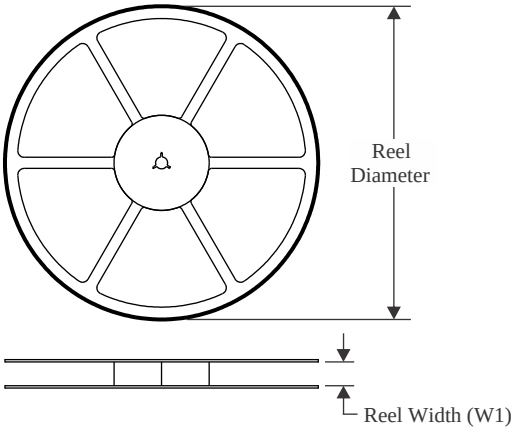
- Automotive : TPS5410-Q1
- Enhanced Product : TPS5410-EP

NOTE: Qualified Version Definitions:

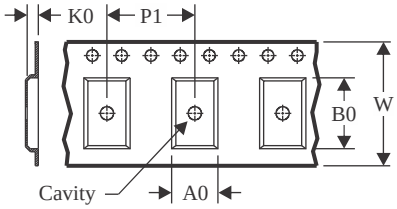
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

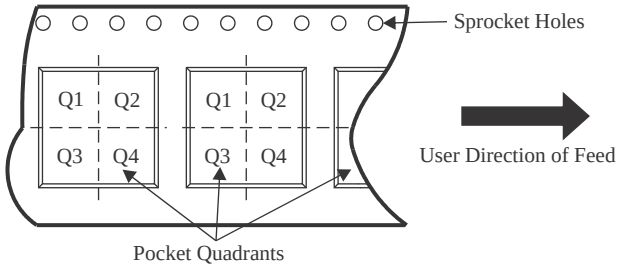


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

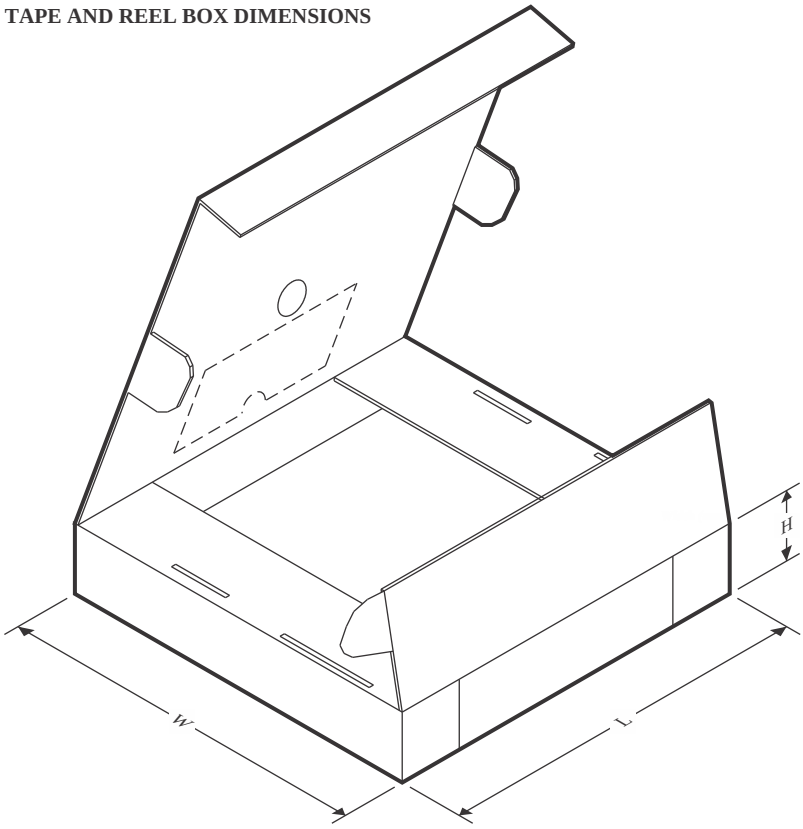
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS5410DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

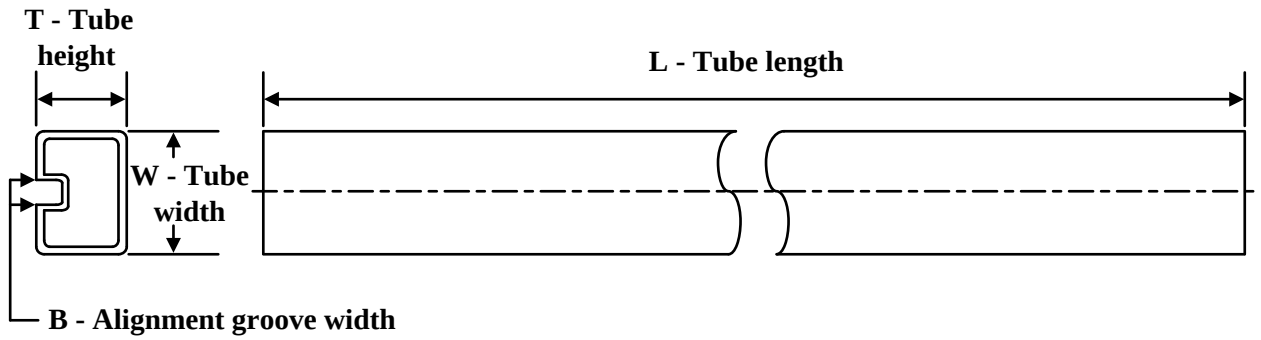
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

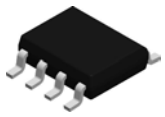
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS5410DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS5410D	D	SOIC	8	75	506.6	8	3940	4.32
TPS5410D.A	D	SOIC	8	75	506.6	8	3940	4.32
TPS5410DG4	D	SOIC	8	75	506.6	8	3940	4.32

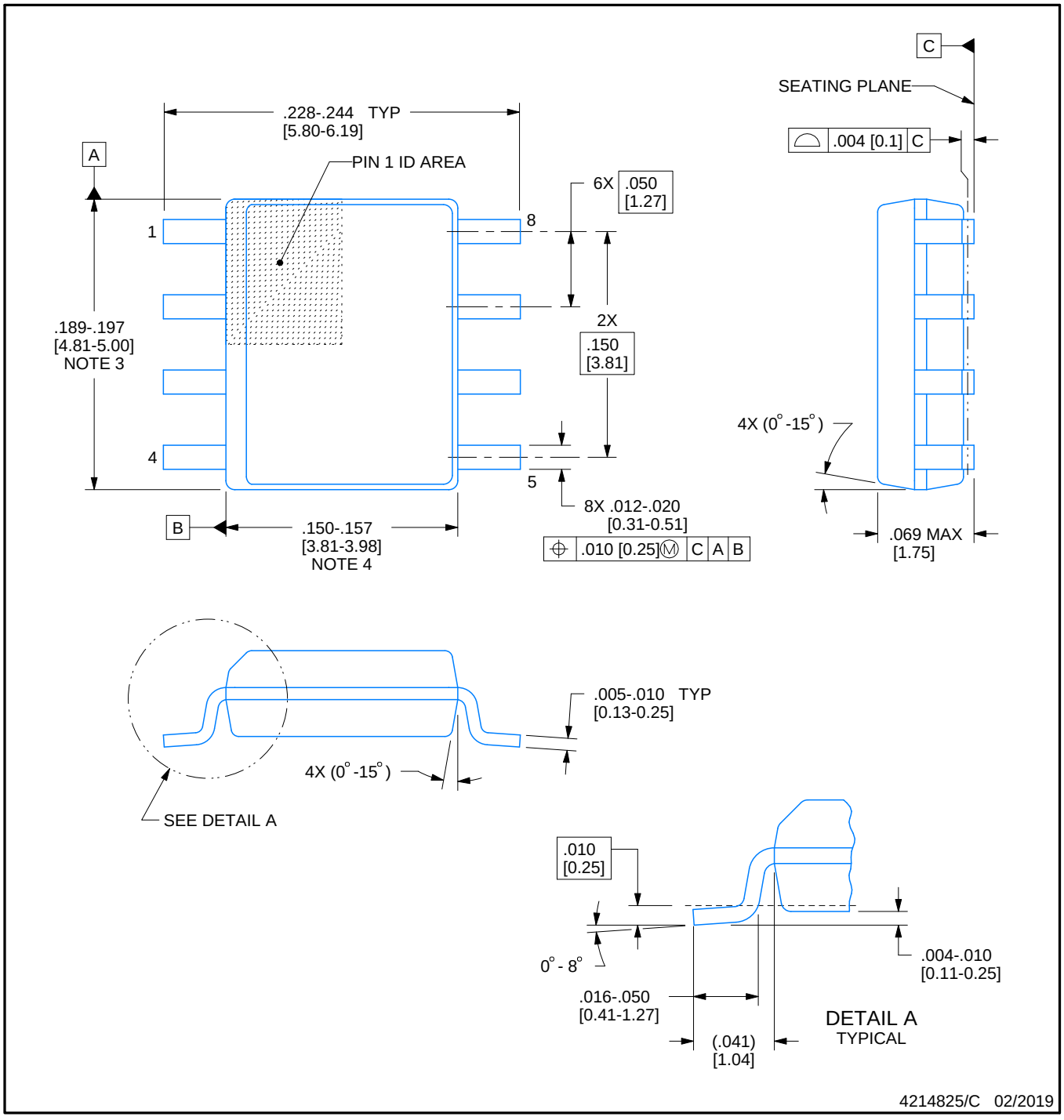


PACKAGE OUTLINE

D0008A

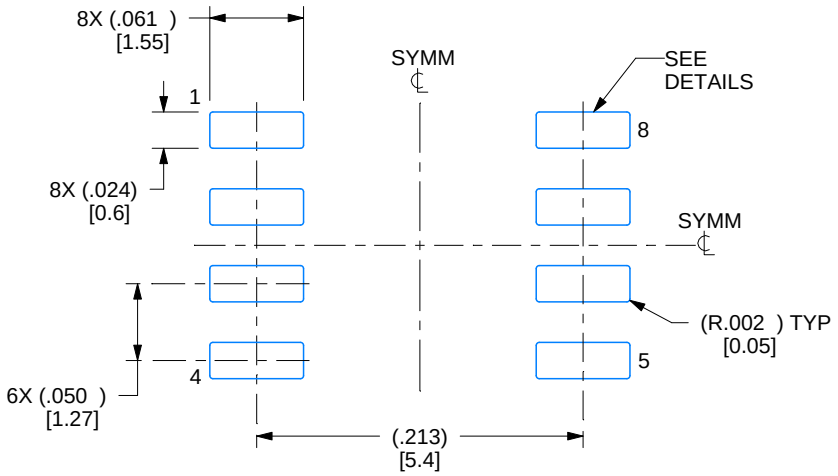
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

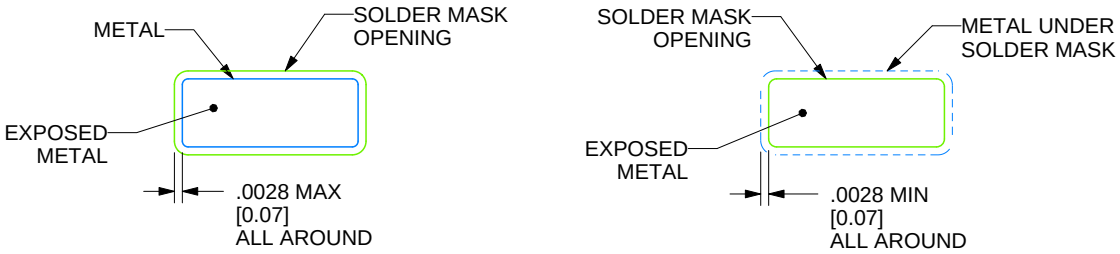


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

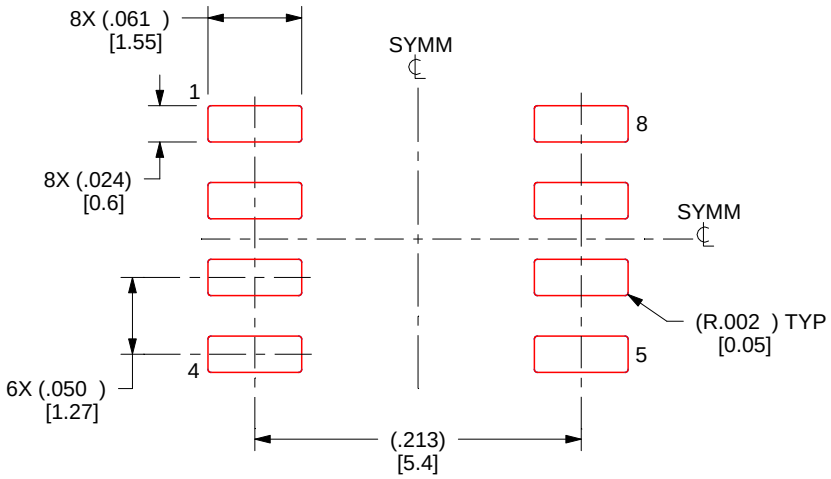
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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