TPS536C9T 具有 TLVR 支持、PMBus® 和 VR14 SVID 接口的双通道（N + M ≤ 12 相）D-CAP+™、降压多相控制器

1 特性

- 输入电压范围：4.5V 至 17V
- 输出电压范围：0.25V 至 5.5V
- 支持 N+M 相位配置（N+M ≤ 12，M ≤ 6）的双路输出
- 与 TI 智能功率级完全兼容
- 支持电压源和电流源 Imon 功率级，具有内部 1kΩ 电阻器
- 支持布线长度大于 12 英寸的双侧电力输送
- 符合 Intel® VR14 SVID 标准且支持 PSYS
- 向后兼容 VR13.HC/VR13.0 SVID
- 自动 NVM 故障状态记录
- 增强型 D-CAP+ 控制可提供卓越的瞬态性能和出色的动态电流共享
- 可通过可编程阈值实现动态切相，从而提高轻负载和重负载下的效率
- 可通过非易失性存储器 (NVM) 进行配置，从而减少外部组件数量
- 单独的每相位 IMON 校准，具有多斜率增益校准以提高系统精度
- 具有可编程超时的二极管制动，可减少瞬态过冲
- 可编程的每相位谷值电流限制 (OCL)
- PMBus® v1.3.1 系统接口，用于遥测电压、电流、功率、温度和故障条件
- 过压故障的新软关断选项
- 可通过 PMBus 对环路补偿进行编程
- 6.00mm × 6.00mm，48 引脚，QFN 封装

2 应用

- 数据中心和企业计算 机架式服务器
- 硬件加速器
- 网络接口卡 (NIC)
- ASIC 和 高性能客户端

3 说明

TPS536C9T 是一款符合 VR14 SVID 标准的降压控制器，具有跨电感稳压器 (TLVR) 拓扑支持、双通道、内置非易失性存储器 (NVM) 和 PMBus® 接口，而且与 TI 智能功率级完全兼容。D-CAP+ 架构等高级控制特性可提供快速瞬态响应、低输出电容和良好的动态电流共享。还本地支持输出电压转换率和自适应电压定位的可调控制。此外，该器件还支持 PMBus 通信接口，可向主机系统报告遥测的电压、电流、功率、温度和故障状况。所有可编程参数均可通过 PMBus 接口进行配置，而且可作为新的默认值存储在 NVM 中，以尽可能减少外部组件数量。

封装信息

器件型号	封装(1)	封装尺寸(2)
TPS536C9T	RSL（QFN，48）	6.00mm × 6.00mm

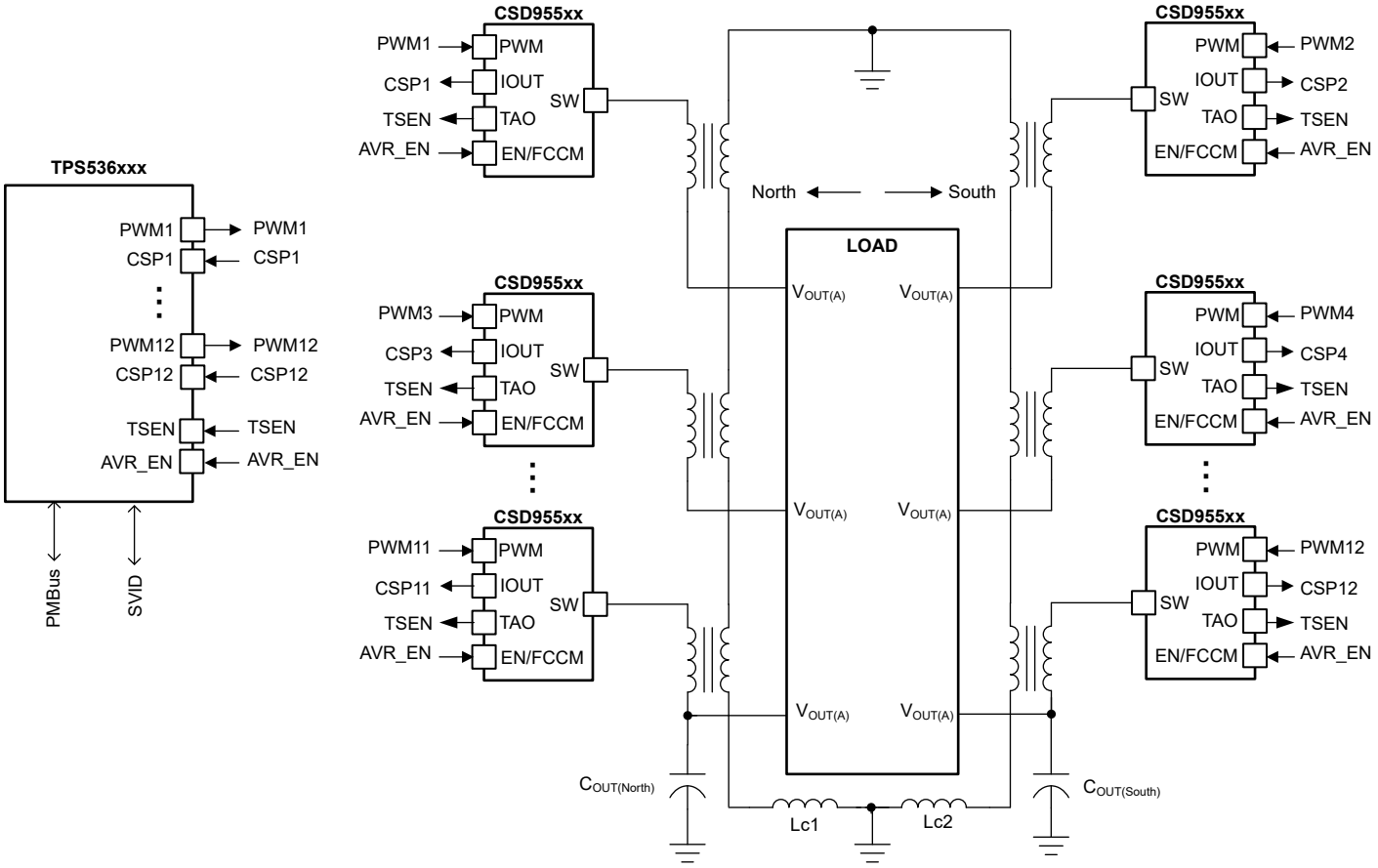
(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。

器件信息

器件型号(1)	相位数
TPS536C9T	12 个相位

(1) 请参阅*器件比较表*

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简化版应用（交错式 TLVR）

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4 器件和文档支持

TI 提供广泛的开发工具。下面列出了用于评估器件性能、生成代码和开发解决方案的工具和软件。

4.1 文档支持

4.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

4.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

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Intel® is a registered trademark of Intel Corporation.
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静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

4.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

5 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

6 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (September 2023) to Revision A (July 2025)	Page
• 向过压故障添加了新的关断选项	1

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS536C9TRSLR	Active	Production	VQFN (RSL) | 48	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 536C9T
TPS536C9TRSLR.A	Active	Production	VQFN (RSL) | 48	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 536C9T

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

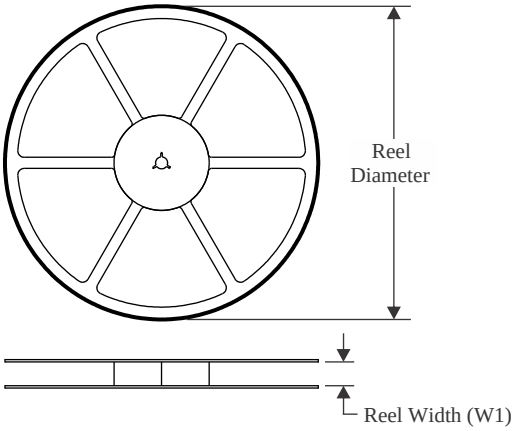
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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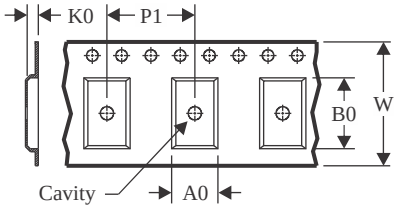
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

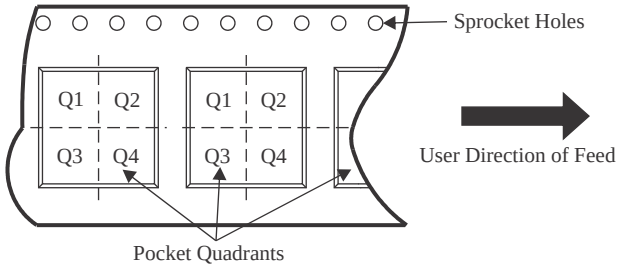


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

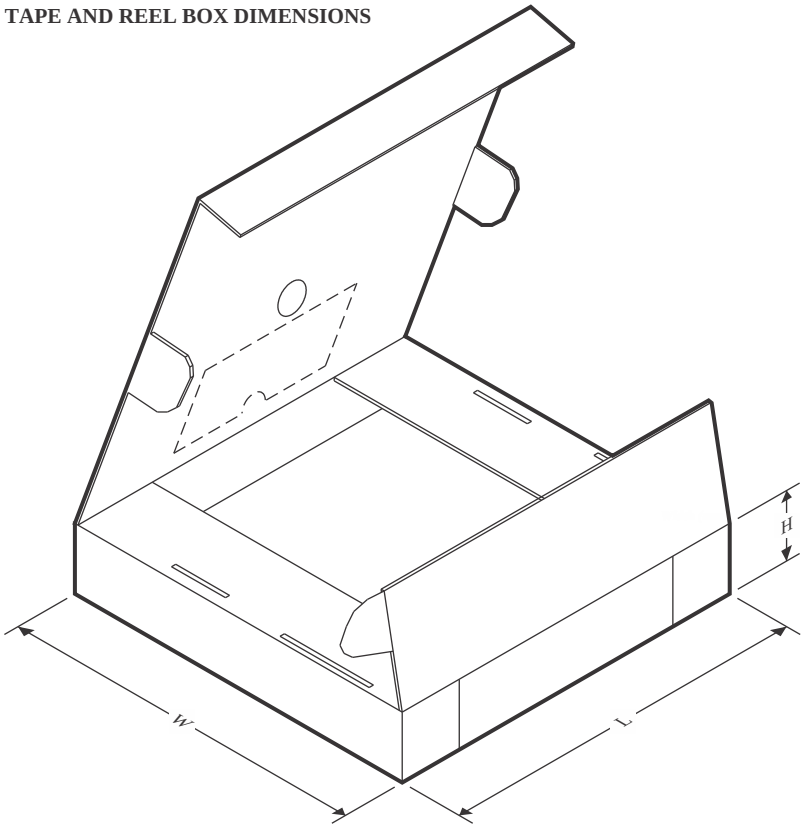
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS536C9TRSLR	VQFN	RSL	48	3000	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS536C9TRSLR	VQFN	RSL	48	3000	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS536C9TRSLR	VQFN	RSL	48	3000	360.0	360.0	36.0
TPS536C9TRSLR	VQFN	RSL	48	3000	367.0	367.0	38.0

GENERIC PACKAGE VIEW

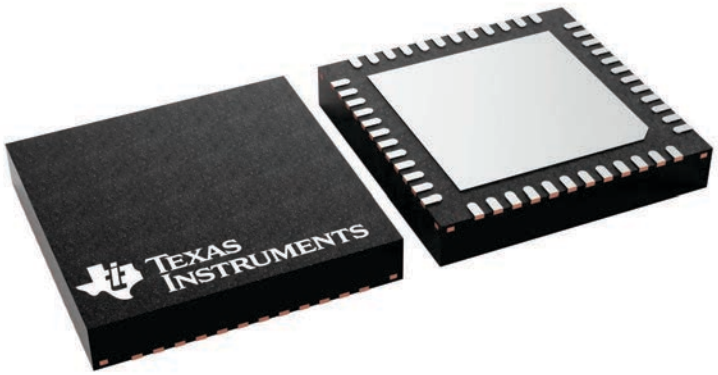
RSL 48

VQFN - 1 mm max height

6 x 6, 0.4 mm pitch

QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



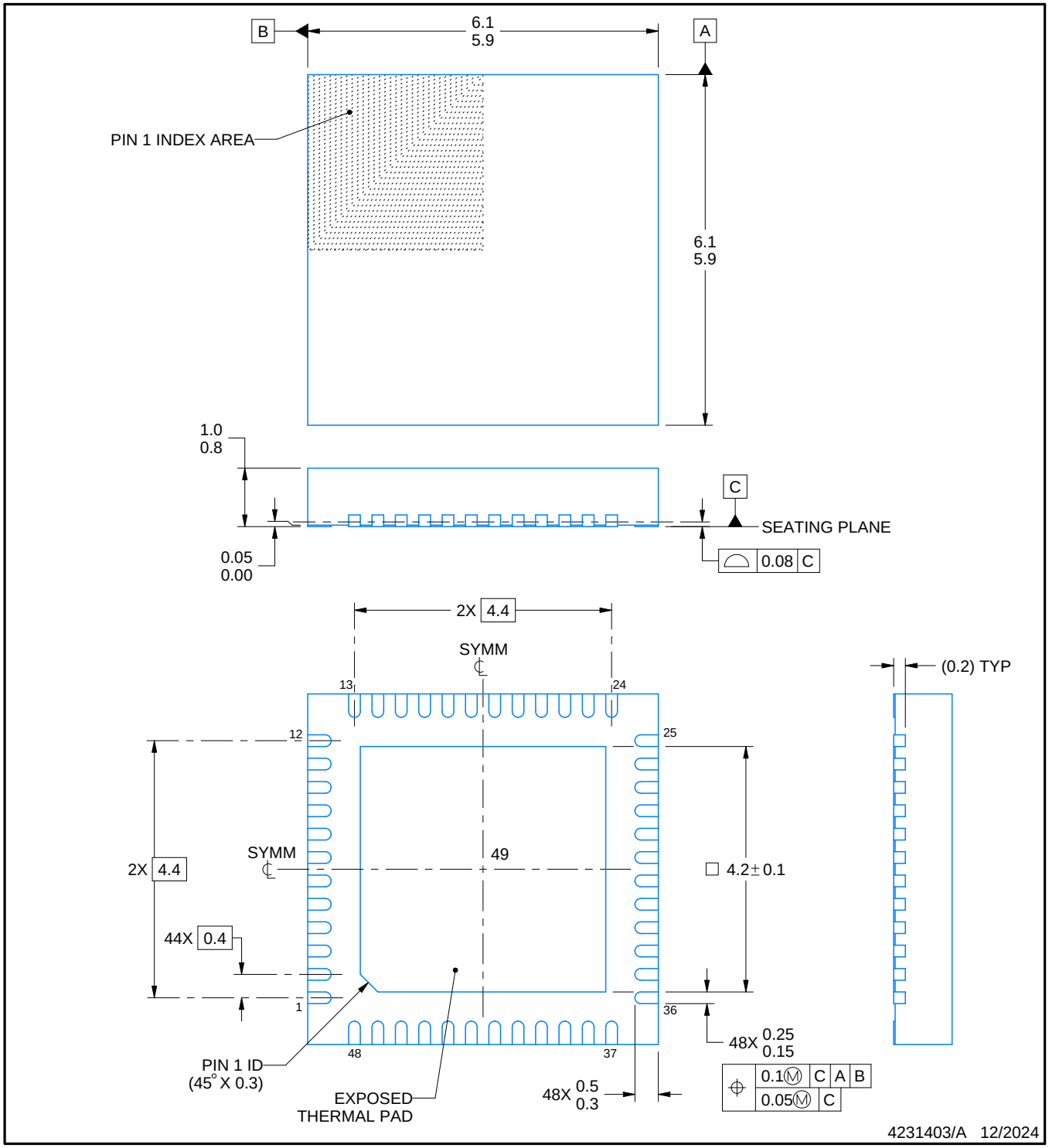
4225749/A

RSL0048G

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

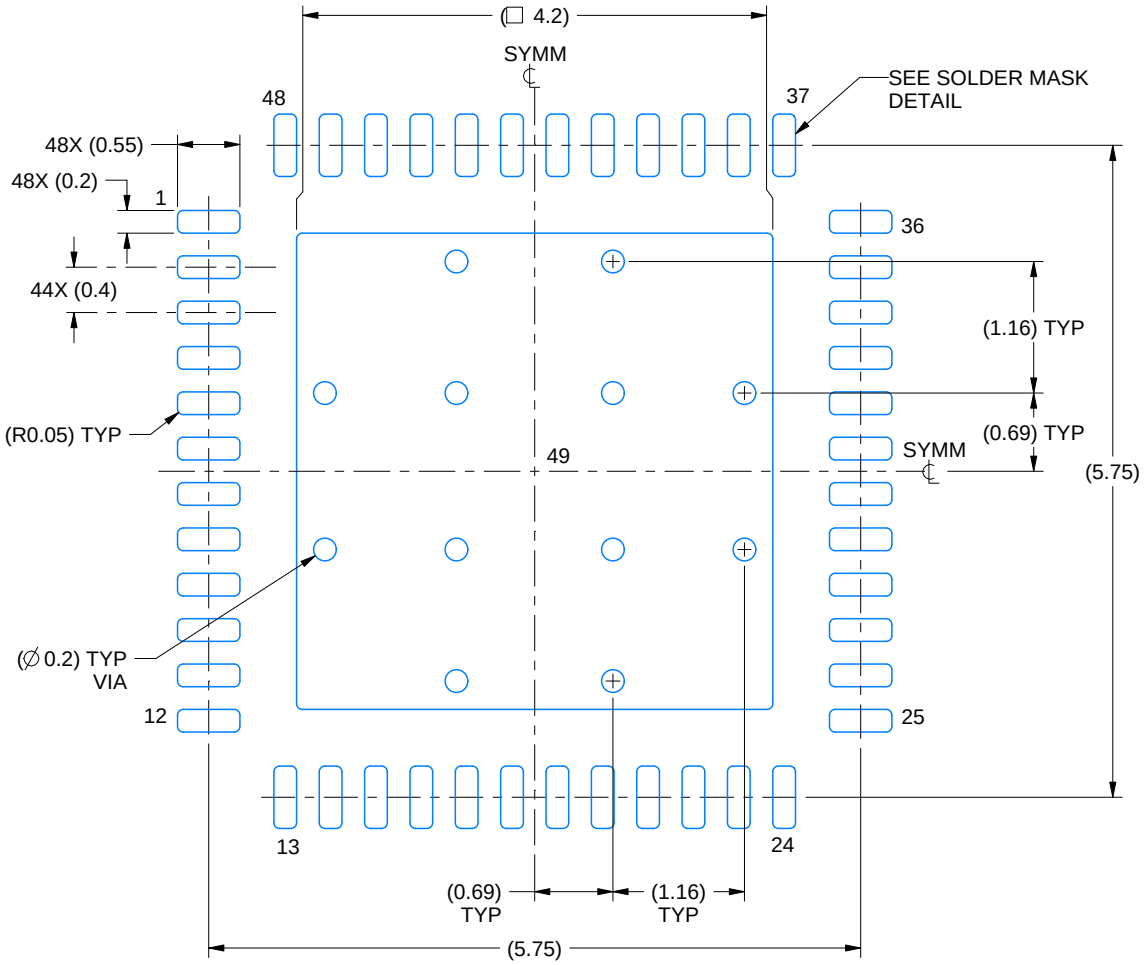
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

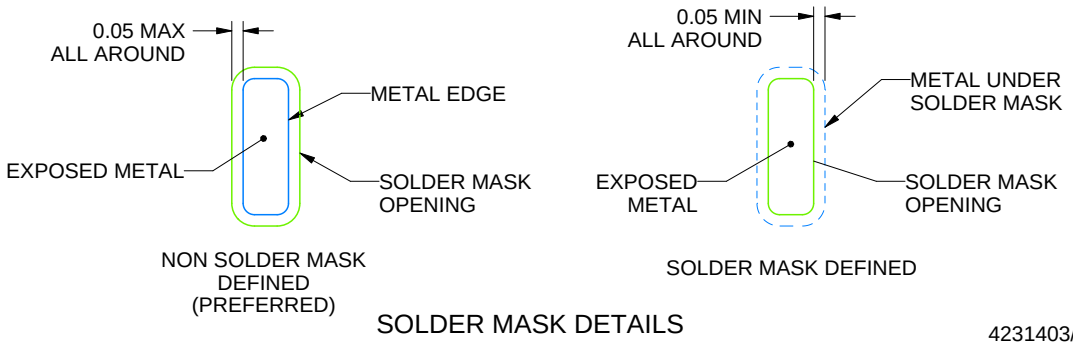
RSL0048G

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

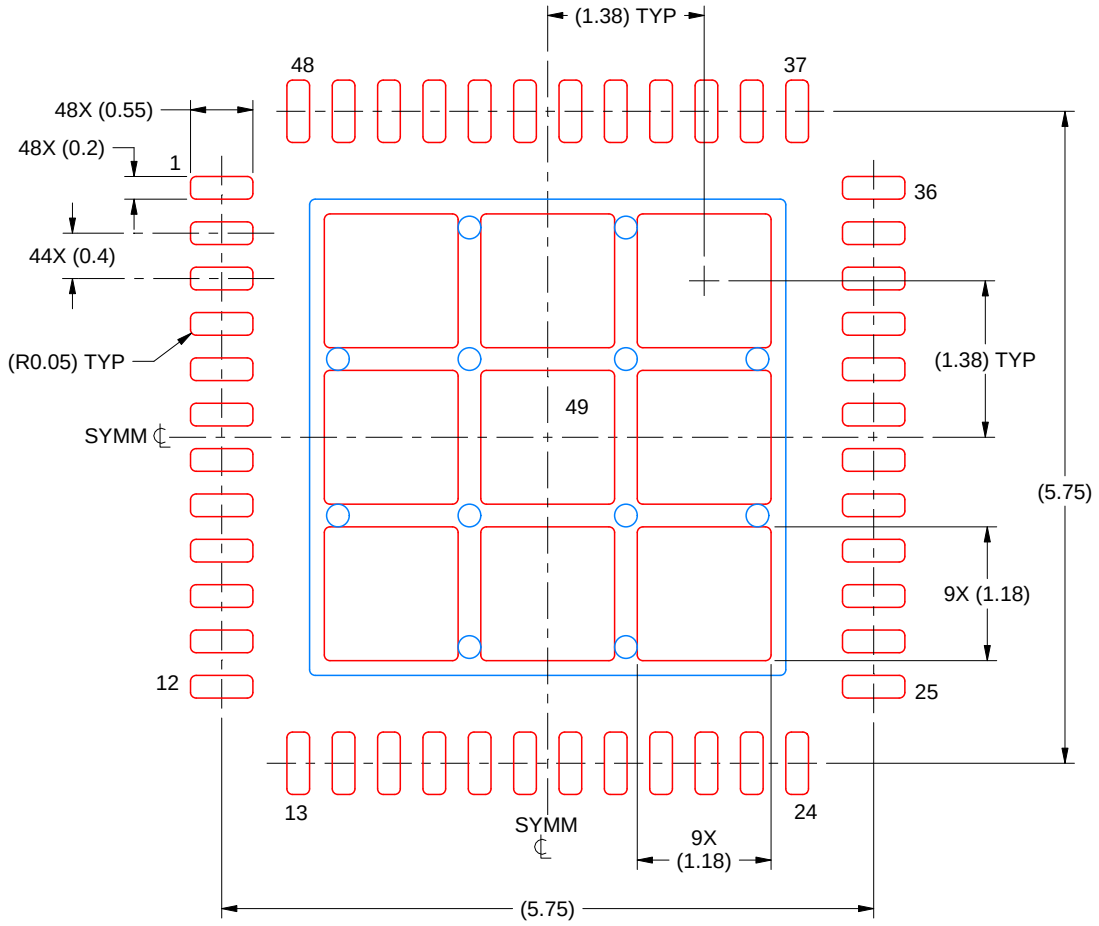


SOLDER MASK DETAILS

4231403/A 12/2024

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 49
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4231403/A 12/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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