TPS53685 具有 AMD-SVI3 和 PMBus 接口的双通道（N + M ≤ 8 相）D-CAP+™、降压多相控制器

1 特性

- 输入电压范围：4.5V 至 17V
- 输出电压范围：0.25V 至 5.5V
- 支持 N+M ≤ 8 相、M ≤ 4 相的双路输出
- 自带跨电感稳压器 (TLVR) 拓扑支持
- 符合 AMD® SVI3 标准
- 增强型 D-CAP+™ 控制可提供卓越的瞬态性能和出色的动态电流共享
- 可编程环路补偿
- 灵活的相位触发时序控制
- 单独的相电流校准和报告
- 可通过可编程电流阈值实现动态切相，从而提高轻负载和重负载下的效率
- 快速增相可实现下冲衰减
- 无驱动器配置，有助于实现高效的高频开关
- 与 TI NexFET™ 功率级完全兼容，可实现高密度解决方案
- 精确可调电压定位
- 获得专利的 AutoBalance™ 相电流平衡
- 每相位电流限值可选
- PMBus™ 系统接口，用于遥测电压、电流、功率、温度和故障条件
- 5.00 × 5.00 mm、40 引脚 0.4 mm 间距 QFN 封装

2 应用

- 机架式服务器
- 微服务器和塔式服务器
- 高性能计算
- 基带单元 (BBU)

3 说明

TPS53685 是一款完全符合 AMD SVI3 标准的降压控制器，具有跨电感稳压器 (TLVR) 拓扑支持、双通道、内置非易失性存储器 (NVM) 和 PMBus™ 接口，而且与 TI 的 NexFET™ 智能功率级完全兼容。D-CAP+™ 架构和下冲衰减 (USR) 等高级控制特性可提供快速瞬态响应和良好的电流共享，从而更大程度降低对输出电容的要求。该器件还提供全新的相位交错策略和动态切相功能，可提升不同负载条件下的效率。V_{CORE} 压摆率和电压定位的可调节控制符合 AMD SVI3 标准。此外，该器件还支持 PMBus 通信接口，可向系统报告遥测的电压、电流、功率、温度和故障状况。所有可编程参数均可通过 PMBus 接口进行配置，而且可作为新的默认值存储在 NVM 中，以尽可能减少外部组件数量。

TPS53685 器件采用热增强型 40 引脚 QFN 封装，额定工作温度为 –40°C 至 125°C。

器件信息

器件型号(1)	封装	封装尺寸（标称值）
TPS53685	QFN (40)	5.00 × 5.00 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

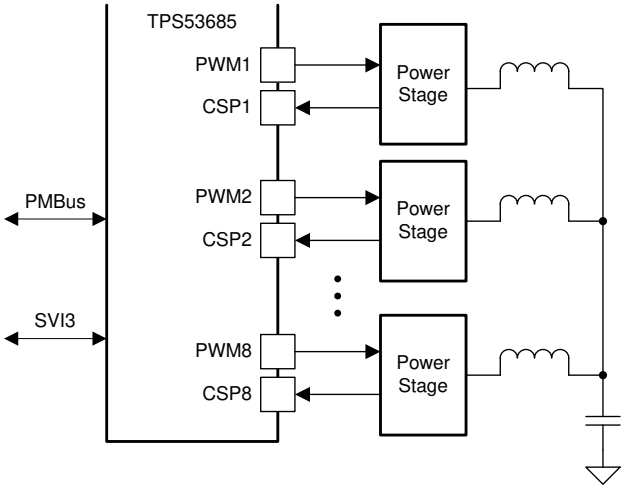


图 3-1. 简化的示例应用

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
December 2022	*	Initial release

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5 Device and Documentation Support

5.1 Documentation Support

5.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, Dual channel DCAP+ multiphase controllers: TPS53685, TPS536C5 Technical Reference Manual SLUUCN5

5.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

5.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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AMD® is a registered trademark of Advanced Micro Devices, Inc..
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5.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.6 术语表

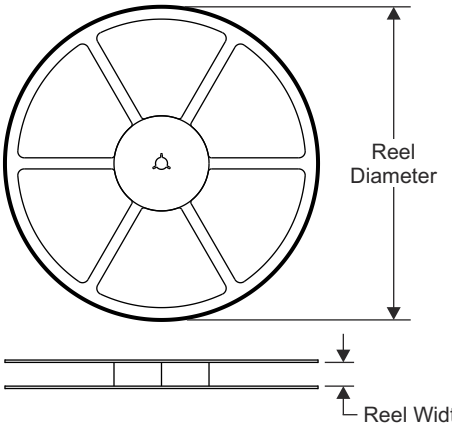
TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

6 Mechanical, Packaging, and Orderable Information

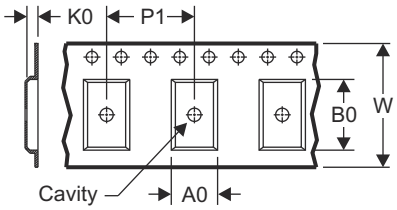
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

6.1 Tape and Reel Information

REEL DIMENSIONS

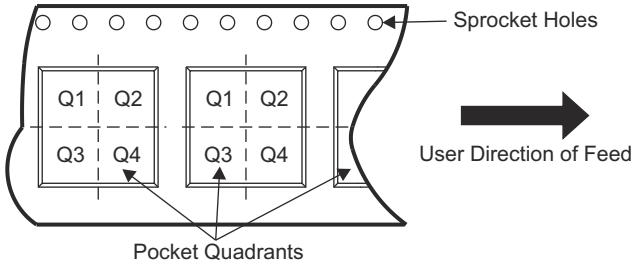


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

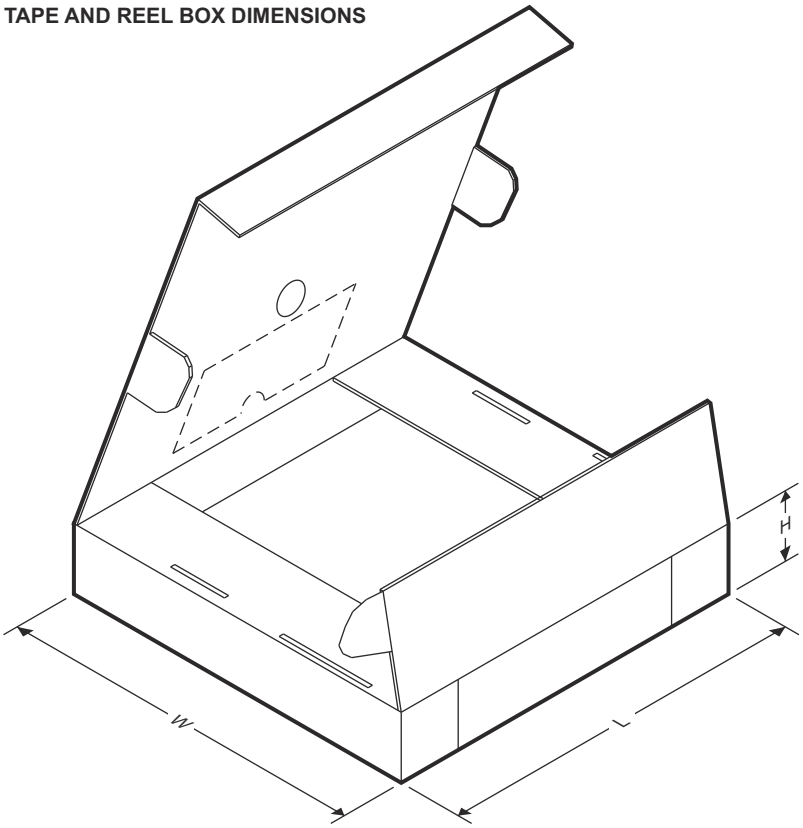
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53685RSBR	WQFN	RSB	40	3000	330.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2

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TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53685RSBR	WQFN	RSB	40	3000	338.0	355.0	50.0

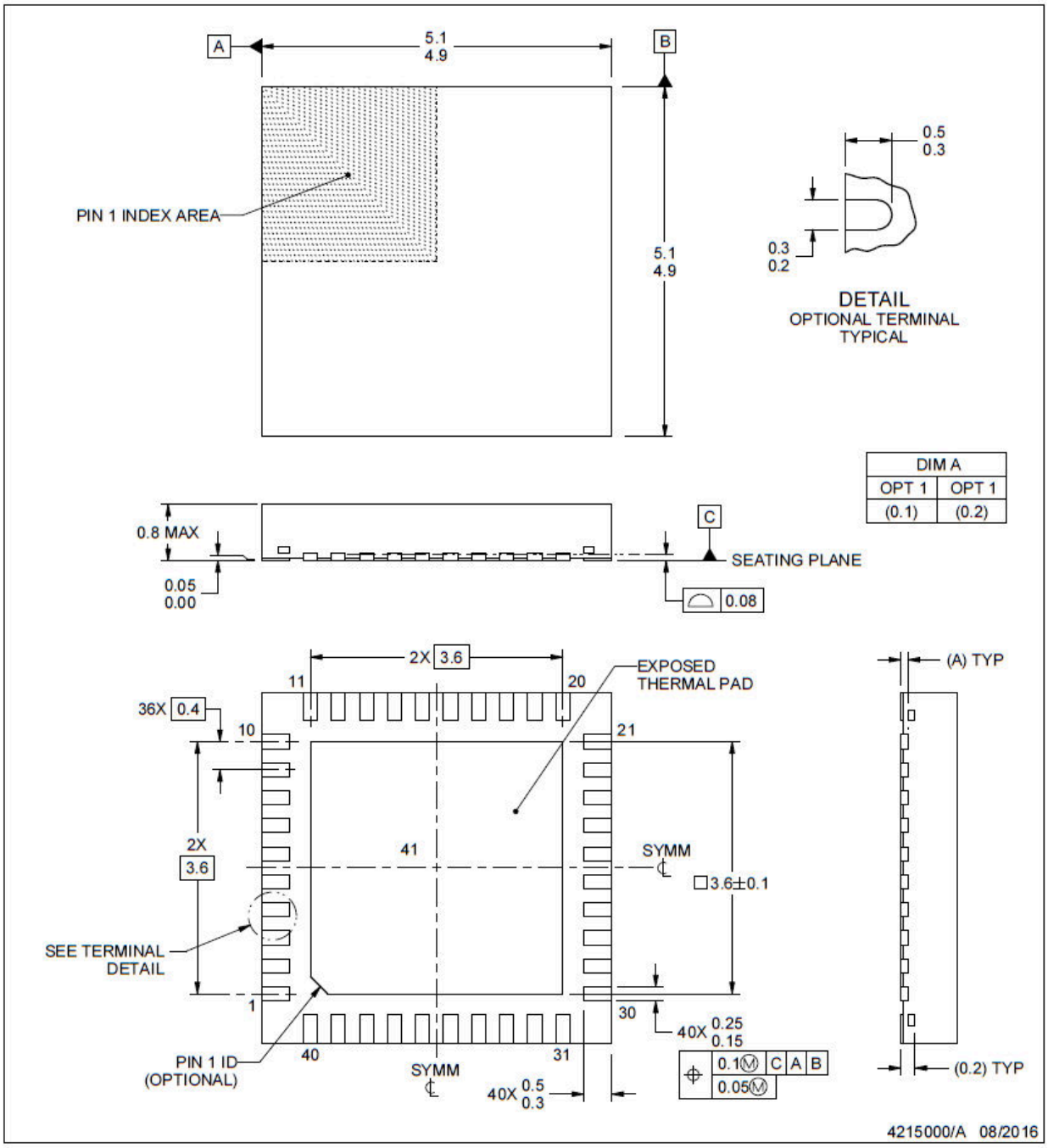
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PACKAGE OUTLINE

RSB0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

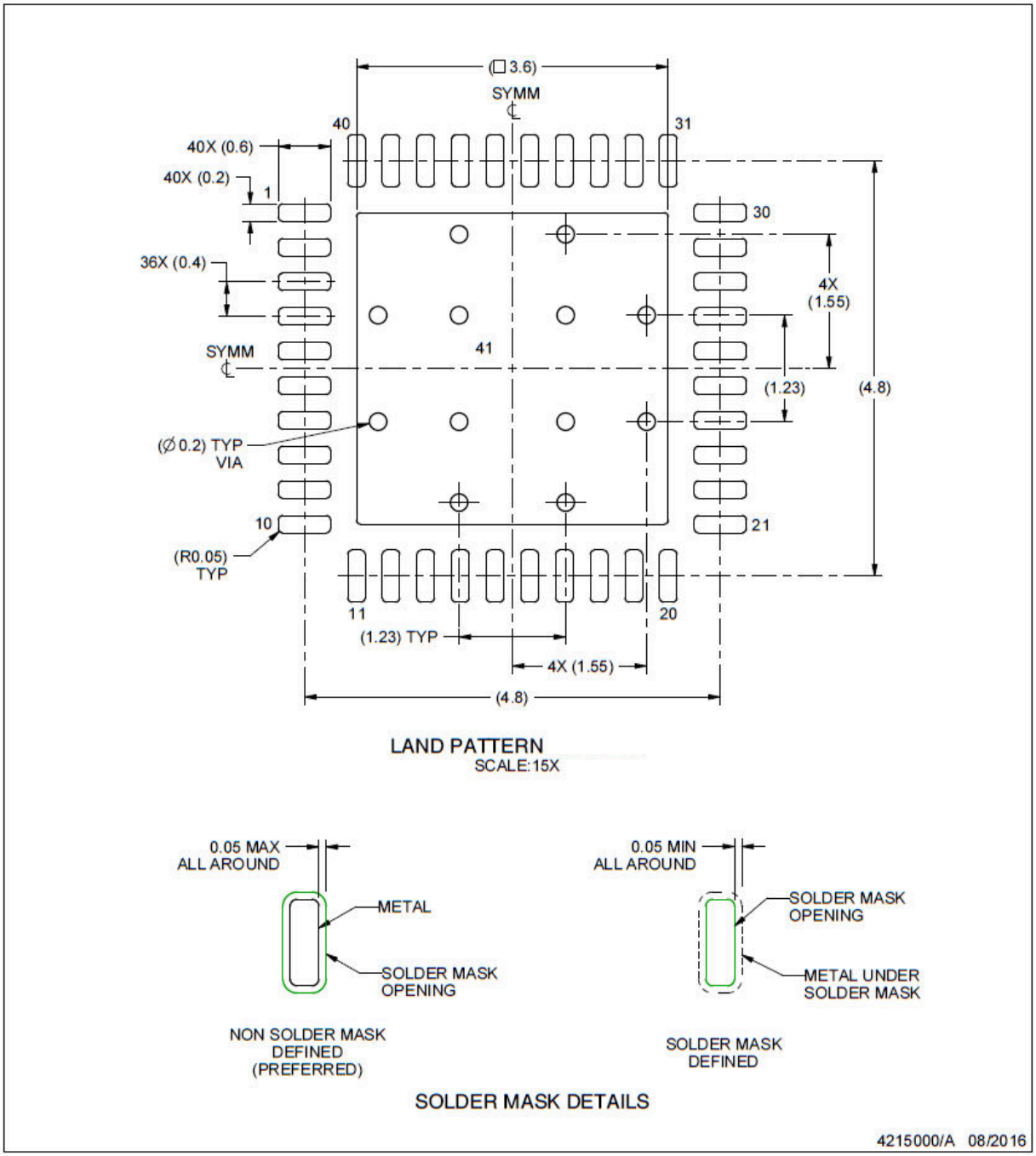
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BOARD LAYOUT

RSB0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

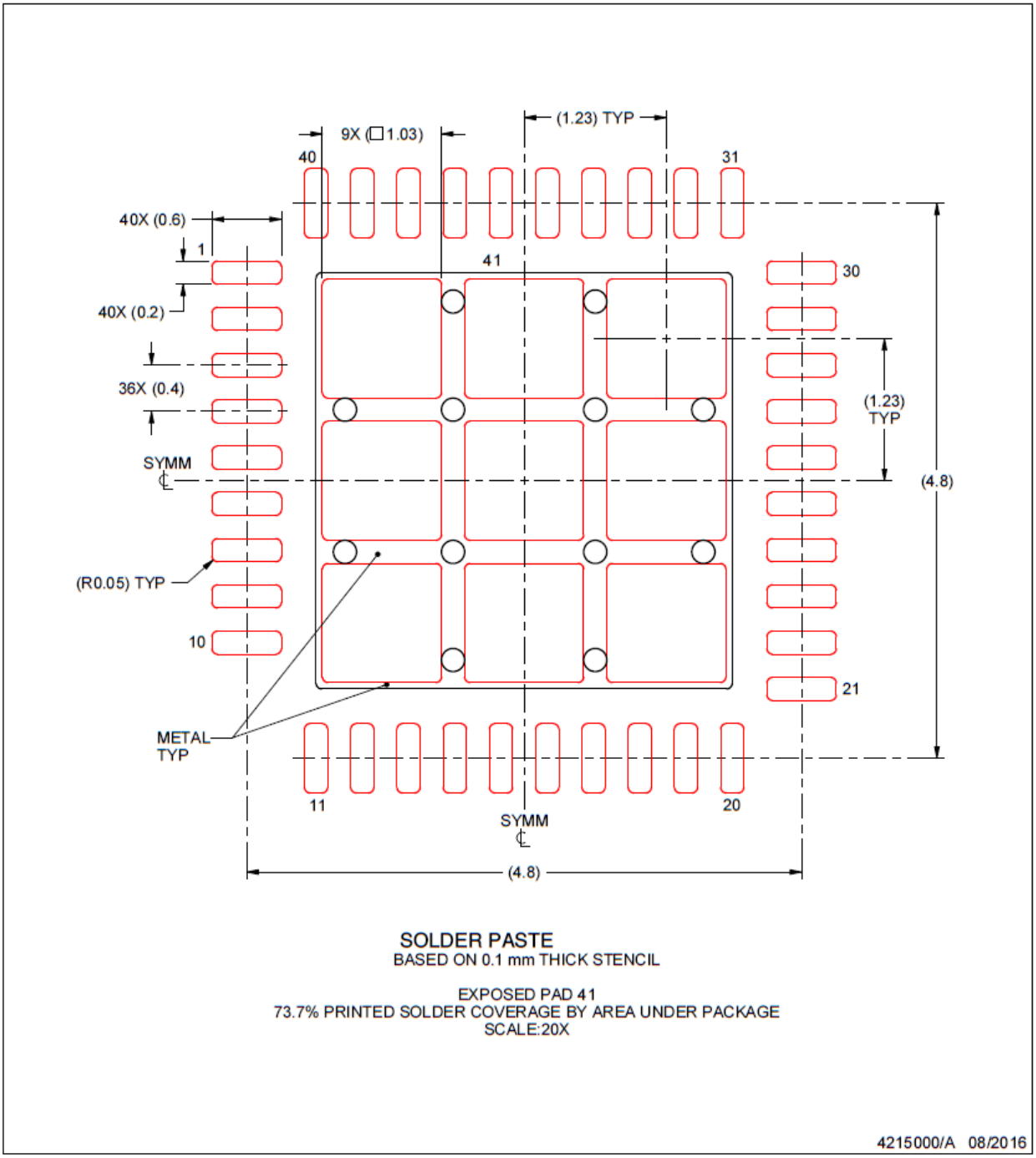
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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STENCIL DESIGN

RSB0040A — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS53685RSBR	Active	Production	WQFN (RSB) | 40	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	TPS 53685
TPS53685RSBR.A	Active	Production	WQFN (RSB) | 40	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	TPS 53685

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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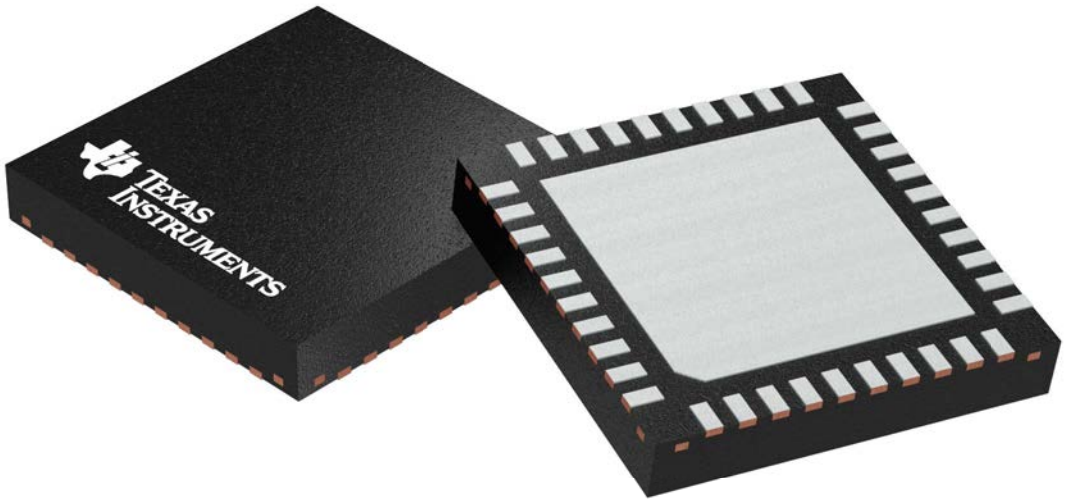
GENERIC PACKAGE VIEW

RSB 40

WQFN - 0.8 mm max height

5 x 5 mm, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



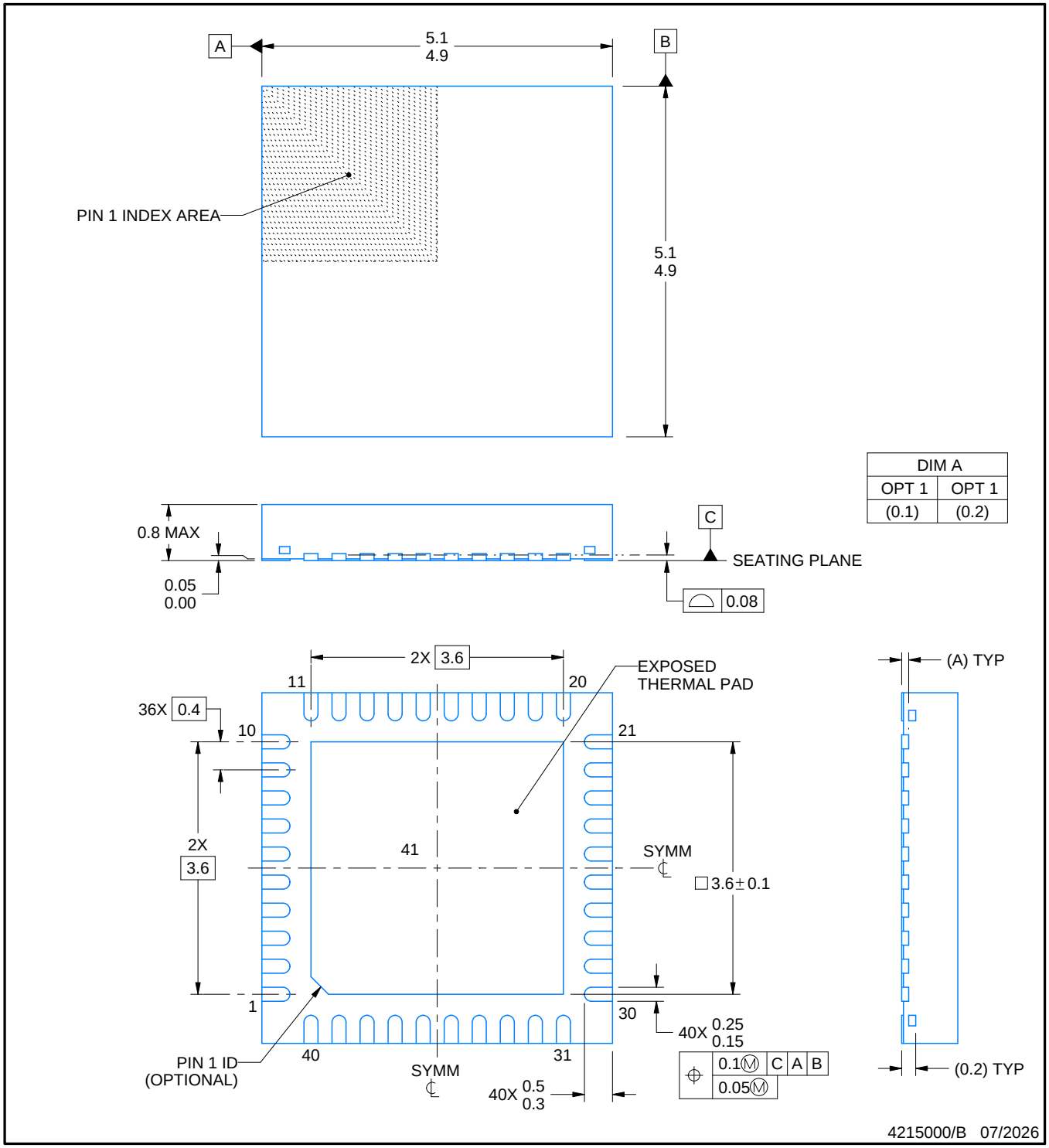
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RSB0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

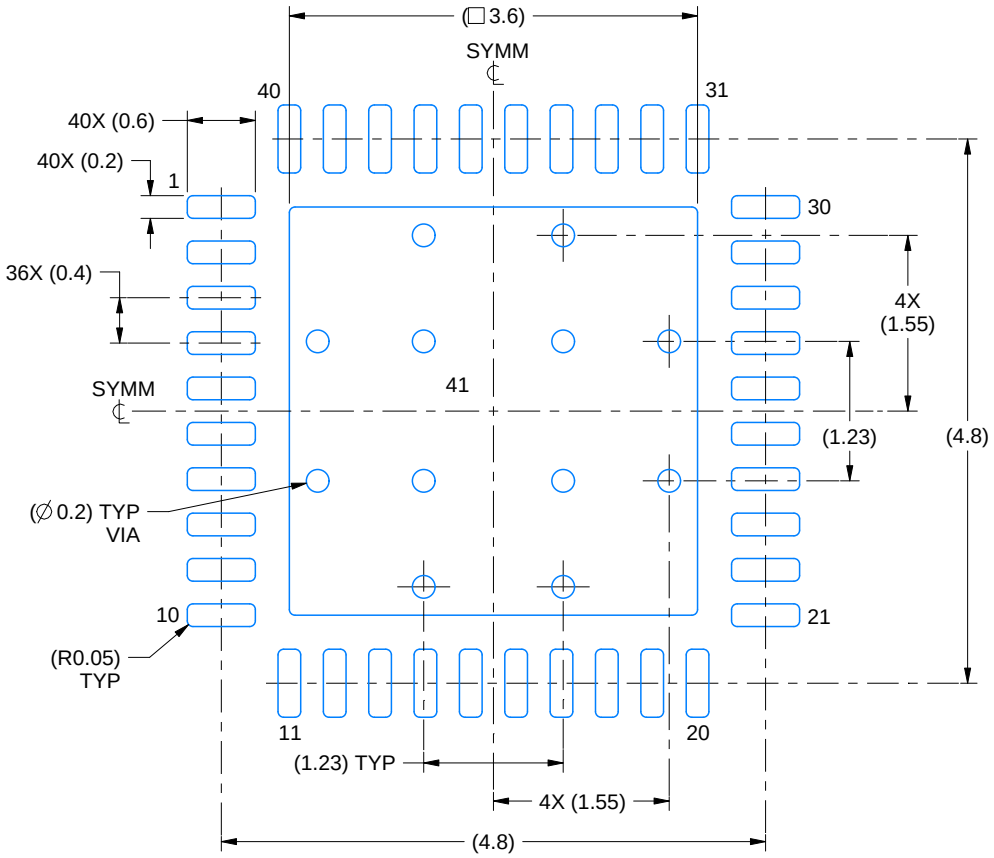
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

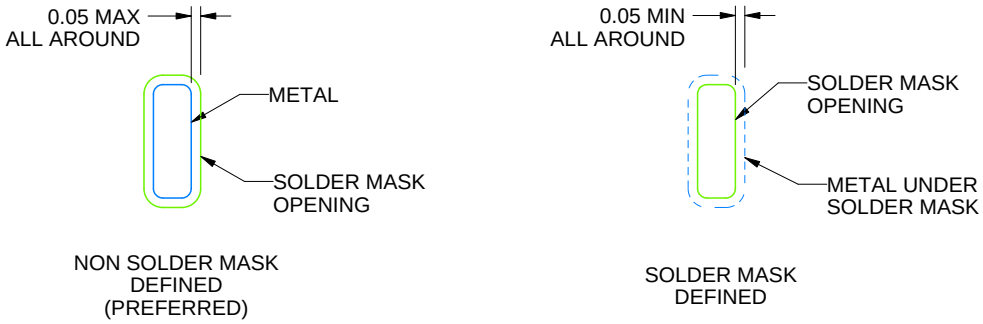
RSB0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:15X

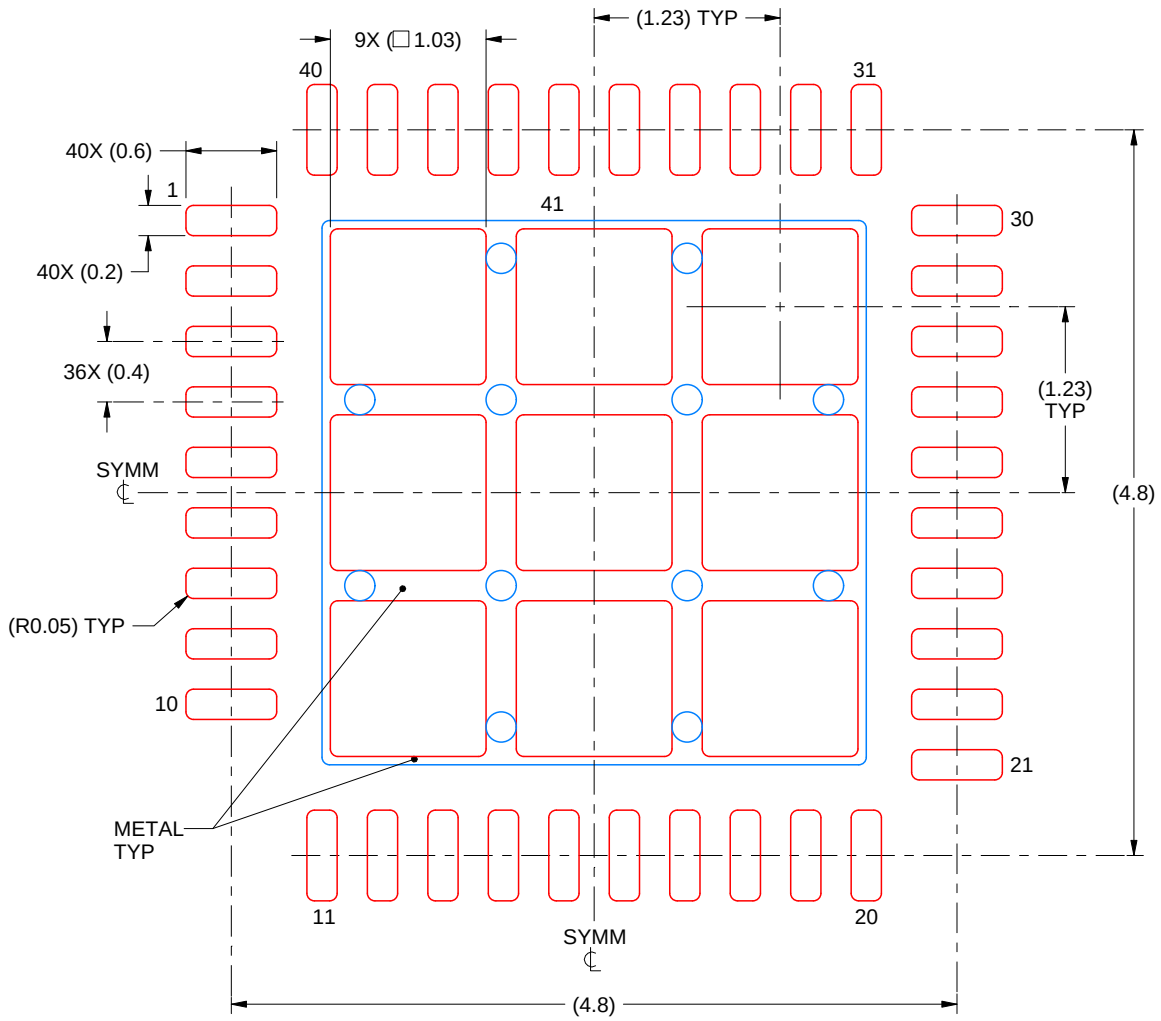


SOLDER MASK DETAILS

4215000/B 07/2026

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 41
73.7% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4215000/B 07/2026

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月