

支持可调节滞后的双路电压检测器

 查询样品: [TPS3806I33-Q1](#)

特性

- 符合汽车应用要求
- 具有符合 **AEC-Q100** 的下列结果:
 - 器件温度 1 级: **-40°C 至 125°C** 的环境运行温度范围
 - 器件人体模型 (HBM) 静电放电 (ESD) 分类等级 **H2**
 - 器件充电器件模型 (CDM) ESD 分类等级 **C4B**
- 具有可调滞后, **3.3V** 可调和 **2V** 可调的双路电压检测器
- **V_{DD}=0.8V** 时复位
- 电源电流: **V_{DD}=3.3V** 时的典型值为 **3μA**
- 独立开漏复位输出
- **6** 引脚小外形尺寸晶体管 (SOT)-23 封装

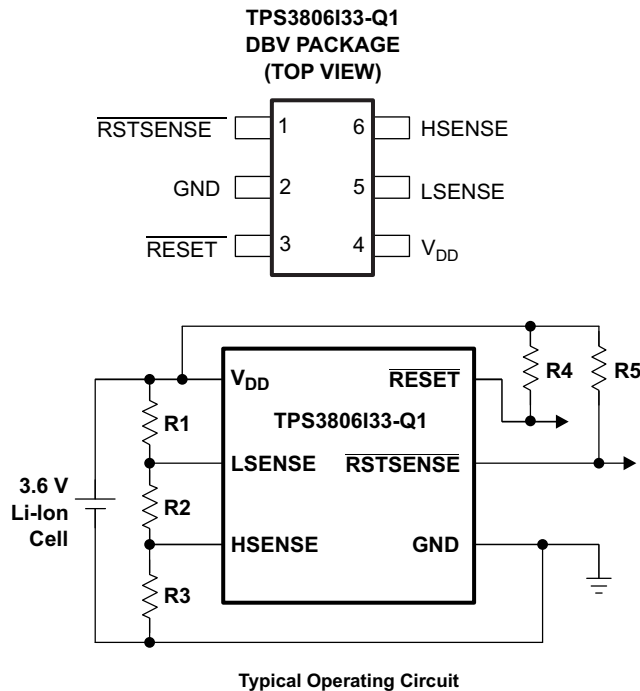
应用范围

- 电压监控器
- 电压检测器
- 电池监控器

说明

TPS3806I33-Q1 集成了 2 个独立的电压检测器用于电池电压监控。加电时, 此器件在电源电压 V_{DD} 或 $LSENSE$ 输入上的电压变为高于 $0.8V$ 时将 \overline{RESET} 和 $\overline{RSTSENSE}$ 置为有效。此后, 监控电路监视 V_{DD} 和 $LSENSE$, 只要 V_{DD} 和 $LSENSE$ 保持低于电压阈值, V_{IT} , 就将 \overline{RESET} 和 $\overline{RSTSENSE}$ 保持有效。只要 V_{DD} 或 $LSENSE$ 上升到高于阈值电压 V_{IT} , 此器件分别将 \overline{RESET} 或 $\overline{RSTSENSE}$ 置为无效。TPS3806I33-Q1 器件有一个固定感测阈值电压 V_{IT} , 此阈值电压由 V_{DD} 上的一个内部分压器和一个可调第二 $LSENSE$ 输入设定。此外, 用户可在 $HSENSE$ 上设置一个较高电压阈值以实现一个宽泛可调滞后窗口。

此器件采用 6 引脚 SOT-23 封装。TPS3806I33-Q1 器件的特点是可在 -40°C 至 125°C 的温度范围内运行。



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



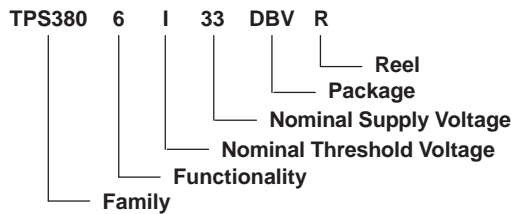
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Table 1. ORDERING INFORMATION⁽¹⁾

| T _A | PACKAGE | QUANTITY | PART NUMBER | TOP-SIDE SYMBOL | STATUS |
|----------------|--------------|--------------|-------------------|-----------------|--------|
| -40°C to 125°C | DBV (SOT-23) | Reel of 3000 | TPS3806I33QDBVRQ1 | PZHQ | Active |

(1) For the most-current package and ordering information, see the Package Option Addendum located at the end of this data sheet or refer to the TI Web site at www.ti.com.



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | TPS3806I33-Q1 | UNIT |
|---|--|-------|
| Supply voltage, V _{DD} ⁽²⁾ | 7 | V |
| All other pins ⁽²⁾ | -0.3 to 7 | V |
| Maximum low-output current, I _{OL} | 5 | mA |
| Maximum high-output current, I _{OH} | -5 | mA |
| Input clamp current, I _{IK} (V _I < 0 or V _I > V _{DD}) | ±10 | mA |
| Output clamp current, I _{OK} (V _O < 0 or V _O > V _{DD}) | ±10 | mA |
| Operating free-air temperature range, T _A | -40 to 125 | °C |
| Storage temperature range, T _{stg} | -65 to 150 | °C |
| Electrostatic discharge rating, ESD | Human-body model (HBM) AEC-Q100 Classification Level H2 | 2 kV |
| | Charged-device model (CDM) AEC-Q100 Classification Level C4B | 750 V |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND. For reliable operation, the device must not be continuously operated at 7 V for more than t = 1000 h.

THERMAL INFORMATION

| THERMAL METRIC ⁽¹⁾ | | TPS3806133-Q1 | |
|-------------------------------|---|---------------|------|
| | | DBV | UNIT |
| | | 6 PINS | |
| θ_{JA} | Junction-to-ambient thermal resistance ⁽²⁾ | 188.9 | °C/W |
| θ_{JCTop} | Junction-to-case (top) thermal resistance ⁽³⁾ | 130.9 | °C/W |
| θ_{JB} | Junction-to-board thermal resistance ⁽⁴⁾ | 34.2 | °C/W |
| ψ_{JT} | Junction-to-top characterization parameter ⁽⁵⁾ | 25.4 | °C/W |
| ψ_{JB} | Junction-to-board characterization parameter ⁽⁶⁾ | 33.8 | °C/W |
| θ_{JCbott} | Junction-to-case (bottom) thermal resistance ⁽⁷⁾ | N/A | °C/W |

- (1) 有关传统和新的热 度量的更多信息，请参阅 *IC 封装热量应用报告*，[SPRA953](#)。
- (2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的指定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然 对流条件下的结至环境热阻。
- (3) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。不存在特定的 JEDEC 标准测试，但 可在 ANSI SEMI 标准 G30-88 中找到内容接近的说明。
- (4) 按照 JESD51-8 中的说明，通过 在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结板热阻。
- (5) 结至顶部特征参数， ψ_{JT} ，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中提取出该参数以便获得 θ_{JA} 。
- (6) 结至电路板特征参数， ψ_{JB} ，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中提取出该参数以便获得 θ_{JA} 。
- (7) 通过在外露（电源）焊盘上进行冷板测试仿真来获得 结至芯片外壳（底部）热阻。不存在特定的 JEDEC 标准 测试，但可在 ANSI SEMI 标准 G30-88 中找到内容接近的说明。

RECOMMENDED OPERATING CONDITIONS

| | MIN | MAX | UNIT |
|---|-----|----------------|------|
| Supply voltage, V_{DD} | 1.3 | 6 | V |
| Input voltage, V_I | 0 | $V_{DD} + 0.3$ | V |
| Operating free-air temperature range, T_A | -40 | 125 | °C |

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|---------------------------------------|---|--|---------------------------------|-------|-------|-------|---|
| V _{OL} | Low-level output voltage | V _{DD} = 1.5 V, I _{OL} = 1 mA | | | | V | |
| | | V _{DD} = 3.3 V, I _{OL} = 2 mA | | | 0.3 | | |
| | | V _{DD} = 6 V, I _{OL} = 3 mA | | | | | |
| Power-up reset voltage ⁽¹⁾ | | V _{DD} ≥ 0.8 V, I _{OL} = 50 μA | | | 0.2 | V | |
| V _{IT} | Negative-going input threshold voltage ⁽²⁾ | LSENSE | T _A = 25°C | 1.198 | 1.207 | 1.216 | V |
| | | TPS3806I33-Q1 | | 2.978 | 3 | 3.022 | |
| | | LSENSE | T _A = 0°C to 70°C | 1.188 | 1.207 | 1.226 | |
| | | TPS3806I33-Q1 | | 2.952 | 3 | 3.048 | |
| | | LSENSE | T _A = -40°C to 125°C | 1.183 | 1.207 | 1.231 | |
| | | TPS3806I33-Q1 | | 2.94 | 3 | 3.06 | |
| V _{hys} | Hysteresis | 1.2 V < V _{IT} < 2.5 V | | 60 | | mV | |
| | | 2.5 V < V _{IT} < 3.5 V | | 90 | | | |
| I _I | Input current | LSENSE, HSENSE | -25 | | 25 | nA | |
| I _{OH} | High-level output current | V _{DD} = V _{IT} + 0.2 V, V _{OH} = V _{DD} | | | 300 | nA | |
| I _{DD} | Supply current | V _{DD} = 3.3 V, output unconnected | | 3 | 5 | μA | |
| | | V _{DD} = 6 V, output unconnected | | 4 | 6 | | |
| C _i | Input capacitance | V _I = 0 V to V _{DD} | | 1 | | pF | |

(1) The lowest supply voltage at which $\overline{\text{RESET}}$ becomes active. $t_{r,VDD} \geq 15 \mu\text{s/V}$

(2) To ensure best stability of the threshold voltage, place a bypass capacitor (ceramic, 0.1 μF) near the supply terminals.

SWITCHING CHARACTERISTICS

at R_L = 1 MΩ, C_L = 50 pF, T_A = -40°C to 125°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--|--|--|-----|-----|------|
| t _{PHL} | Propagation (delay) time, high-to-low-level output | V _{DD} to $\overline{\text{RESET}}$ delay | V _{IH} = 1.05 × V _{IT} , V _{IL} = 0.95 × V _{IT} | 5 | 100 | μs |
| | | LSENSE to $\overline{\text{RSTSENSE}}$ delay | | | | |
| t _{PLH} | Propagation (delay) time, low-to-high-level output | V _{DD} to $\overline{\text{RESET}}$ delay | | | | |
| | | HSENSE to $\overline{\text{RSTSENSE}}$ delay | | | | |

TIMING REQUIREMENTS

at R_L = 1 MΩ, C_L = 50 pF, T_A = -40°C to 125°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|----------------|--------------------|---|-----|-----|------|
| t _w | Pulse duration | At V _{DD} | V _{IH} = 1.05 × V _{IT} , V _{IL} = 0.95 × V _{IT} | 5.5 | | μs |
| | | At SENSE | | | | |

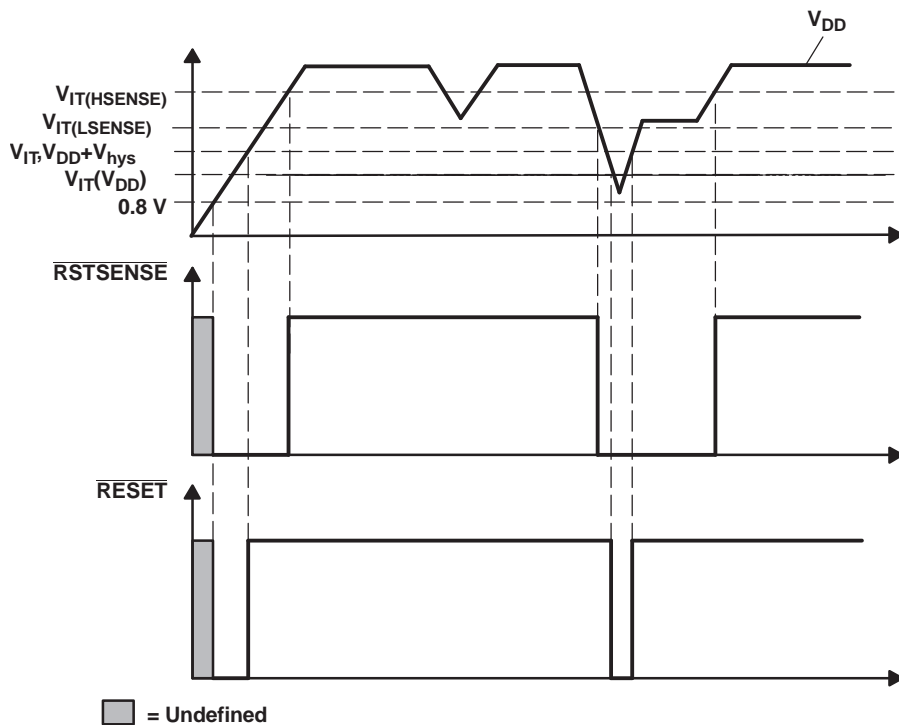


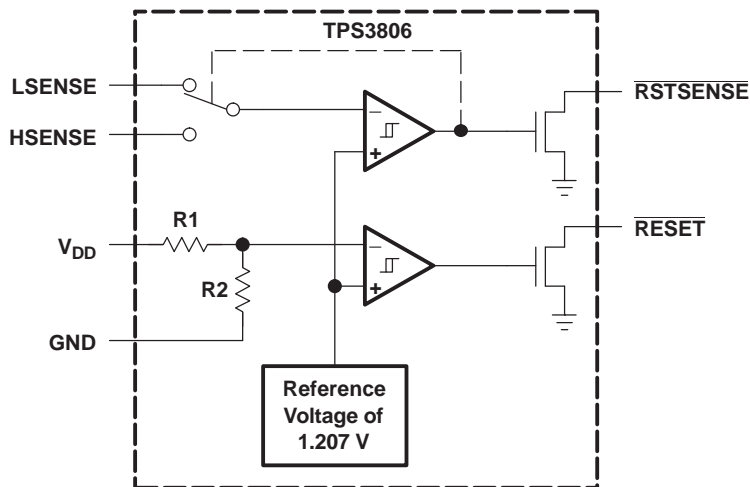
Table 2. TERMINAL FUNCTIONS

| TERMINAL | | I/O | DESCRIPTION |
|-----------------------|-----|-----|---|
| NAME | NO. | | |
| GND | 2 | I | Ground |
| HSENSE | 6 | I | Adjustable hysteresis input |
| LSENSE | 5 | I | Adjustable sense input |
| \overline{RESET} | 3 | O | Active-low open-drain reset output (from V_{DD}) |
| $\overline{RSTSENSE}$ | 1 | O | Active-low open-drain reset output (from LSENSE) |
| V_{DD} | 4 | I | Input supply voltage and fixed sense input |

FUNCTION AND TRUTH TABLE

| TPS3806133-Q1 | | | |
|-------------------|--------------------|-------------------|-----------------------|
| $V_{DD} > V_{IT}$ | \overline{RESET} | $LSENSE > V_{IT}$ | $\overline{RSTSENSE}$ |
| 0 | L | 0 | L |
| 1 | H | 1 | H |

FUNCTIONAL BLOCK DIAGRAM



Detailed Description

Operation

The TPS3806I33-Q1 monitors battery voltage and asserts $\overline{\text{RESET}}$ when a battery becomes discharged below a certain threshold voltage. A comparator monitors the battery voltage via an external resistor divider. When the voltage at the LSENSE input drops below the internal reference voltage, the $\overline{\text{RSTSENSE}}$ output pulls low. The output remains low until the battery is replaced, or recharged above a second higher trip-point, set at HSENSE. One can monitor a second voltage at V_{DD} . The independent $\overline{\text{RESET}}$ output pulls low when the voltage at V_{DD} drops below the fixed threshold voltage. Because the TPS3806I33-Q1 outputs are open-drain MOSFETs, most applications may require a pullup resistor.

Programming the Threshold Voltage Levels

Calculate the low-voltage threshold at LSENSE according to [Equation 1](#):

$$V_{(\text{LSENSE})} = V_{\text{ref}} \left(\frac{R1 + R2 + R3}{R2 + R3} \right) \quad (1)$$

where $V_{\text{ref}} = 1.207 \text{ V}$

Calculate the high-voltage threshold at HSENSE as shown in [Equation 2](#):

$$V_{(\text{HSENSE})} = V_{\text{ref}} \left(\frac{R1 + R2 + R3}{R3} \right) \quad (2)$$

where $V_{\text{ref}} = 1.207 \text{ V}$

To minimize battery current draw, TI recommends using $1 \text{ M}\Omega$ as the total resistor value $R_{(\text{tot})}$, with $R_{(\text{tot})} = R1 + R2 + R3$.

TYPICAL CHARACTERISTICS

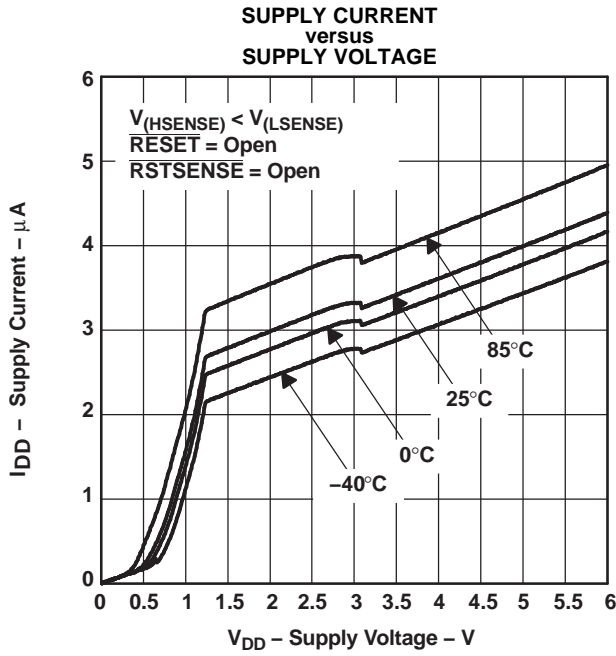


Figure 1.

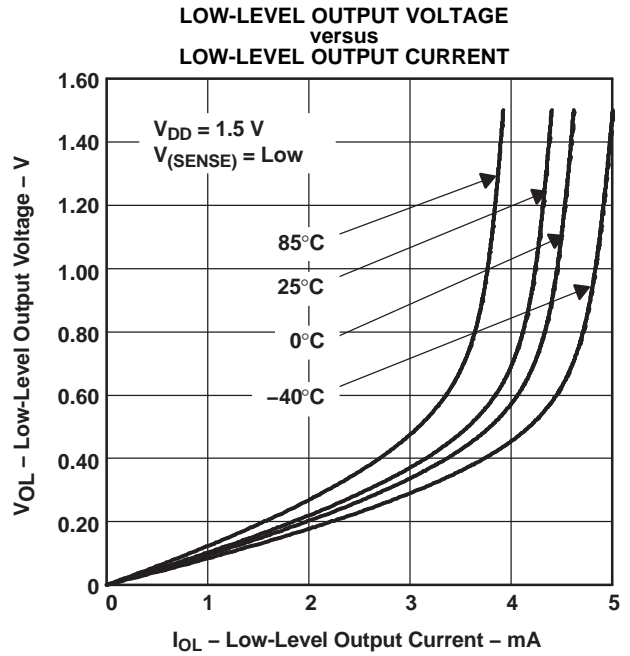


Figure 2.

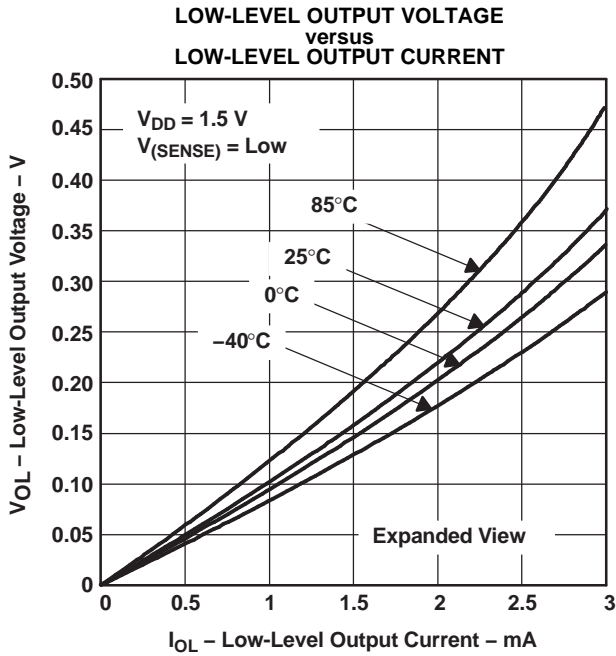


Figure 3.

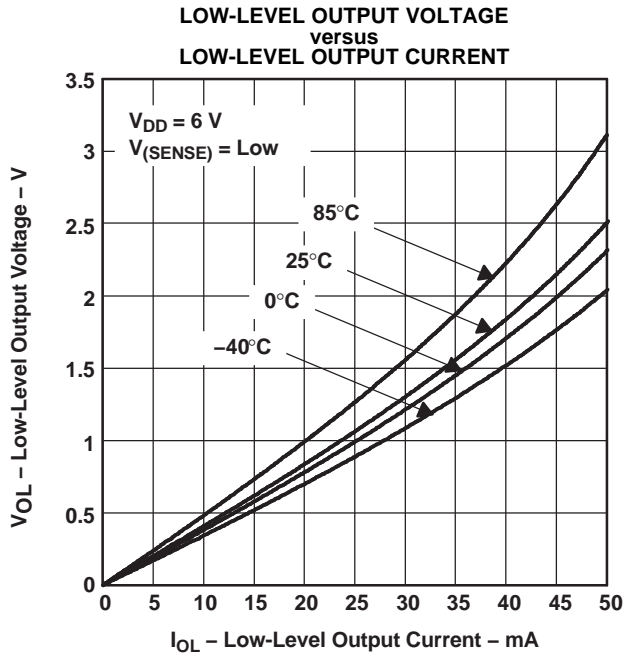


Figure 4.

TYPICAL CHARACTERISTICS (continued)

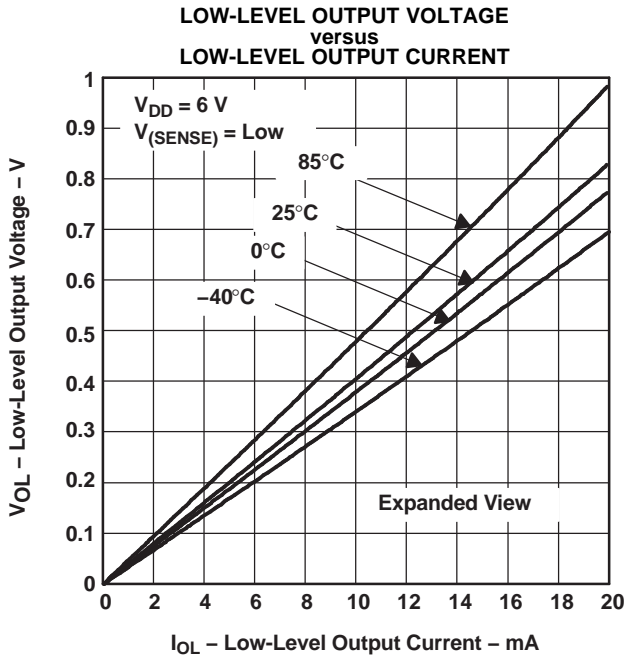


Figure 5.

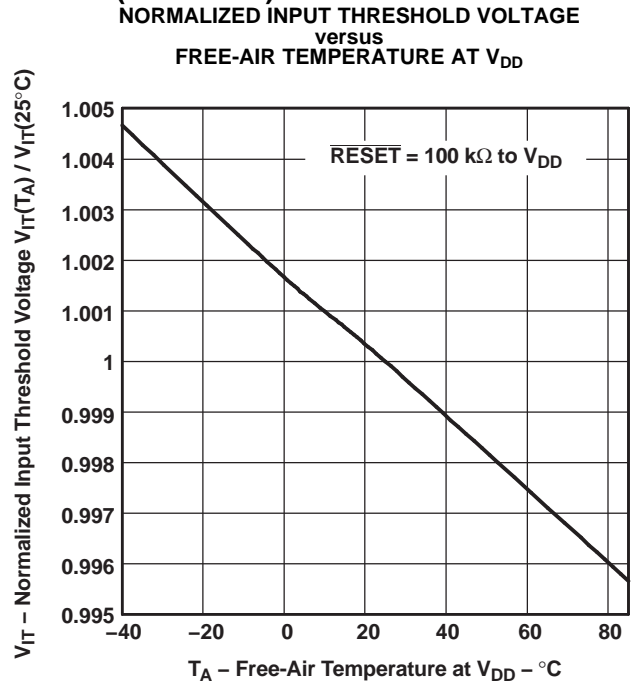


Figure 6.

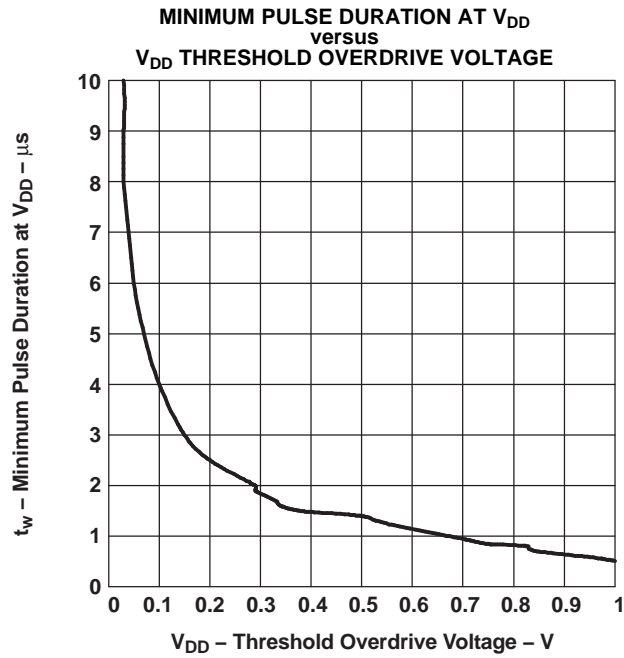


Figure 7.

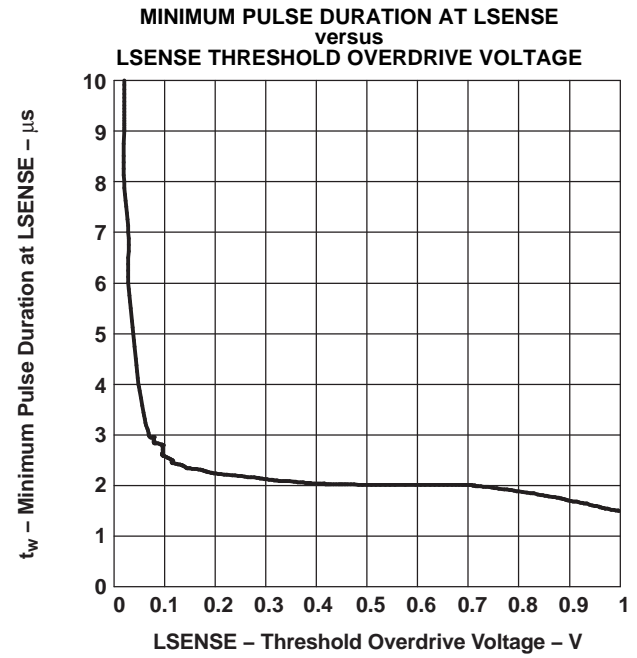


Figure 8.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| TPS3806I33QDBVRQ1 | Active | Production | SOT-23 (DBV) 6 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PZHQ |
| TPS3806I33QDBVRQ1.B | Active | Production | SOT-23 (DBV) 6 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PZHQ |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

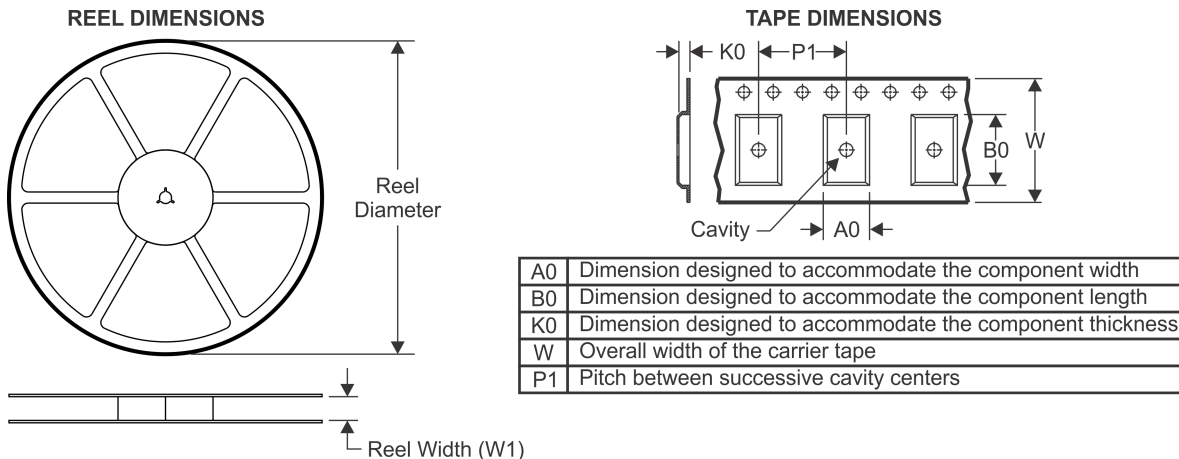
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS3806I33QDBVRQ1 | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS3806I33QDBVRQ1 | SOT-23 | DBV | 6 | 3000 | 180.0 | 180.0 | 18.0 |

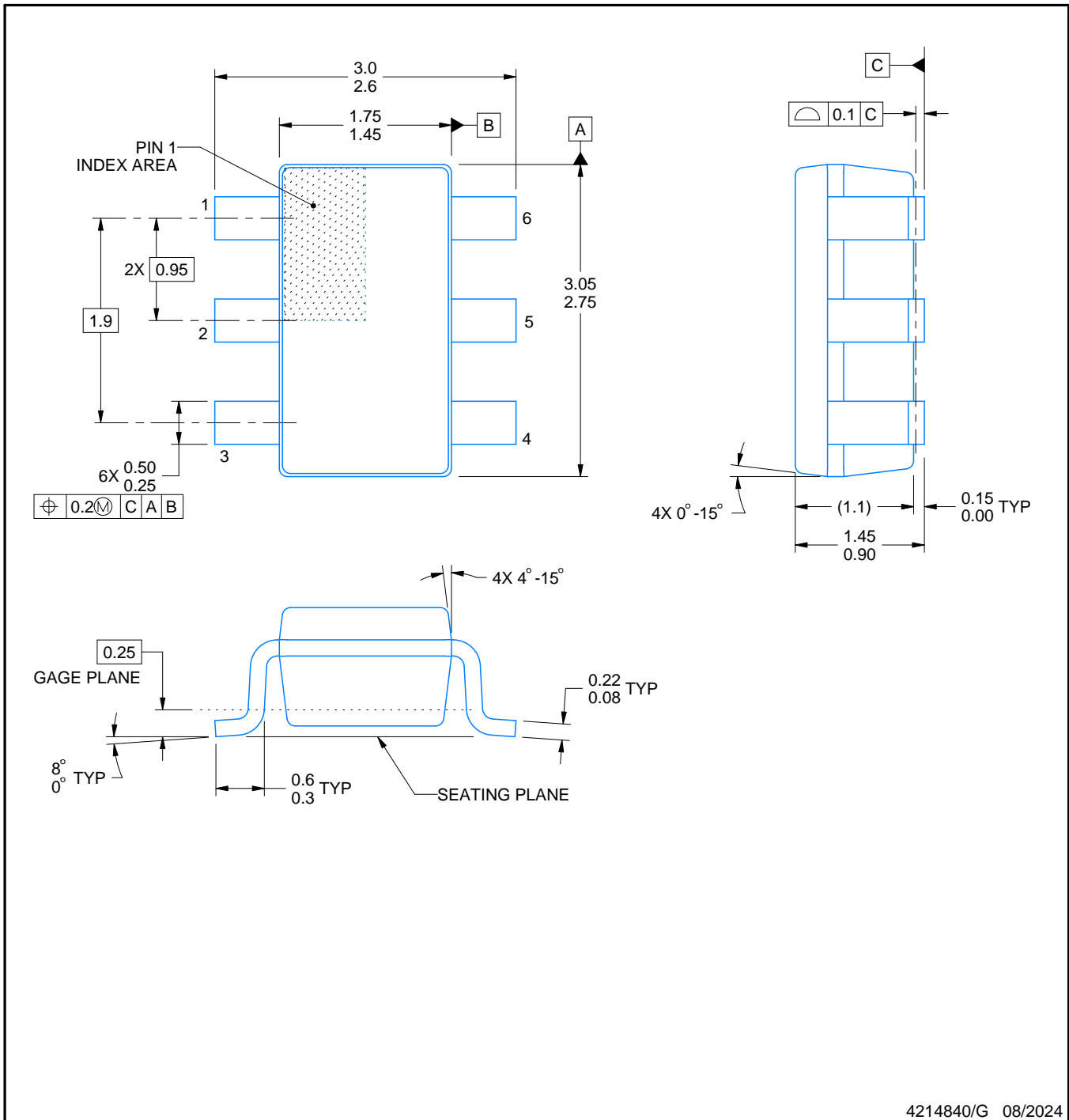
DBV0006A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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NOTES:

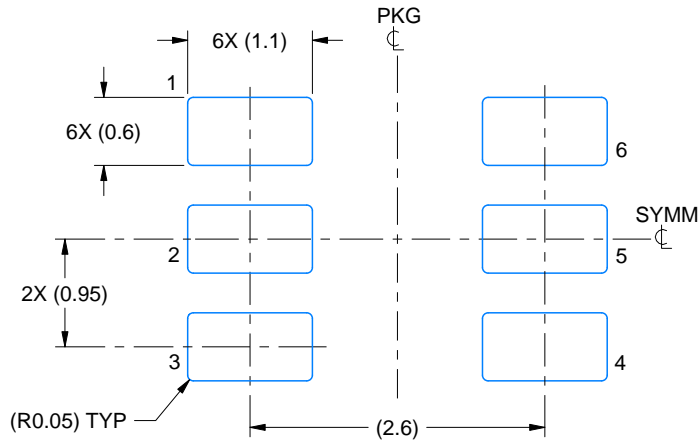
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

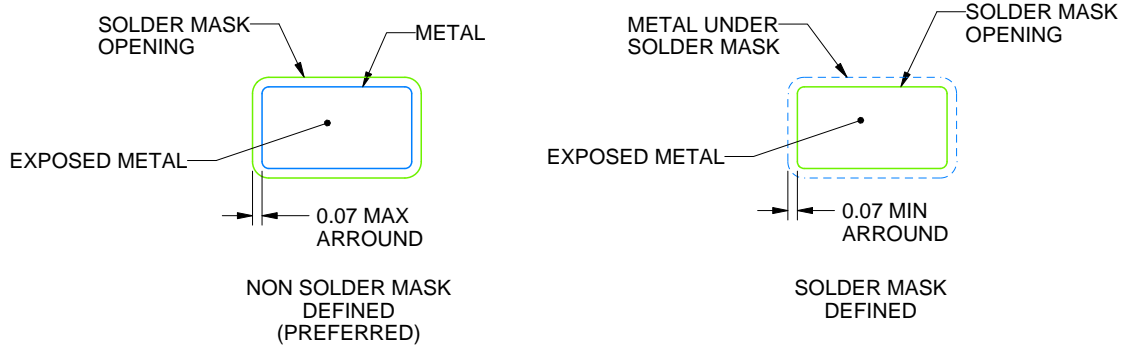
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

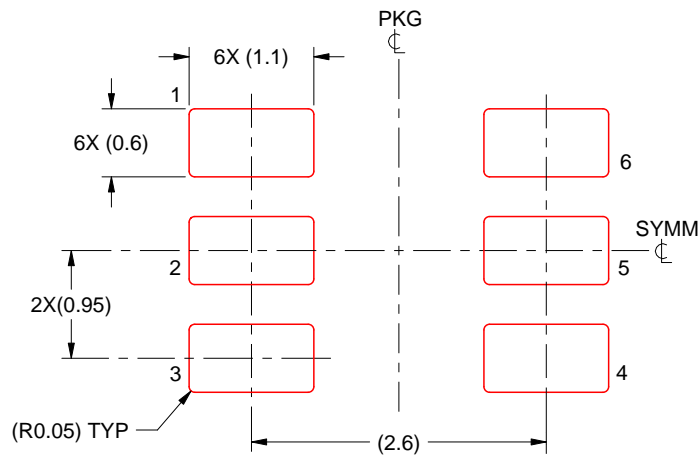
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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